HI-508/883

Single 8-Channel CMOS Analog Multiplexer

FN8290
Rev.0.00
May 3, 2012

The HI-508/883 is an eight channel single-ended multiplexer. This monolithic CMOS multiplexer includes an array of eight analog switches, a digital decode circuit for channel selection, a voltage reference for logic thresholds, and an ENABLE input for device selection when several multiplexers are present.

The Dielectric Isolation (DI) process used in fabrication of this device eliminates the problem of latch-up. Also, DI offers much lower substrate leakage and parasitic capacitance than conventional junction-isolated CMOS. Switches are guaranteed to break-before-make, so that two channels are never shorted together. The switching threshold for each digital input is established by an internal +5V reference, providing a guaranteed minimum 2.4V for logic “1” and Maximum 0.8V for logic “0”. This allows direct interface without pull-up resistors to signals from most logic families: CMOS, TTL, DTL and some PMOS. For protection against transient overvoltage, the digital inputs include a series 200Ω resistor and a diode clamp to each supply. If input overvoltage protection is needed, the HI-548/883 and HI-549/883 multiplexers are recommended. For further information see Application Note AN520.

Features

- This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Low On Resistance (Max). 400Ω
- Wide Analog Signal Range . . . . . ±15V
- TTL/CMOS Compatible . . . . . 2.4V (Logic “1”)
- Access Time (Max) 1.0µs
- 44V Maximum Power Supply
- Break-Before-Make Switching
- No Latch-up

Applications

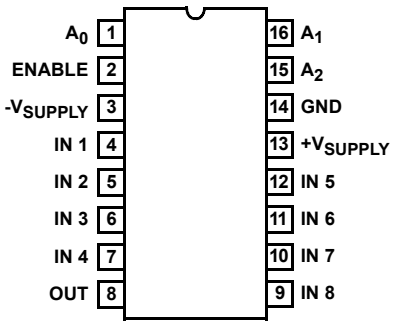
- Data Acquisition Systems
- Precision Instrumentation
- Demultiplexing
- Selector Switch

Ordering Information

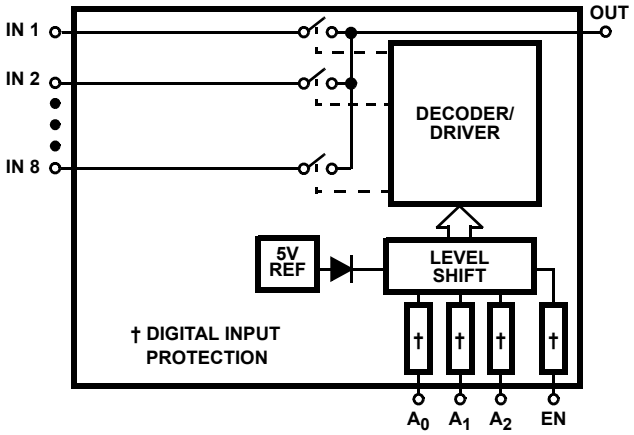
PART #	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
HI1-0508/883	HI1-508/883	-55 to 125	16 Ld CerDIP	F16.3

Pin Configuration

HI-508/883
(16 LD CERDIP)
TOP VIEW



Functional Diagram



TRUTH TABLE HI-508/883

A_2	A_1	A_0	EN	“ON” CHANNEL
X	X	X	L	None
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

Absolute Maximum Ratings

Voltage Between Supply Pins 44V
$+V_{SUPPLY}$ to Ground 22V
$-V_{SUPPLY}$ to Ground 22V
Analog Input Voltage, $+V_S$ . . . . . $+V_{SUPPLY}$ +2V
$-V_S$ . . . . . $-V_{SUPPLY}$ -2V
Digital Input Voltage, $+V_{EN}$, $+V_A$ . . . . . $+V_{SUPPLY}$ +4V
$-V_{EN}$, $-V_A$ . . . . . $-V_{SUPPLY}$ +4V
or 20mA, whichever occurs first
Continuous Current, S or D 20mA
Peak Current, S or D (Pulsed at 1ms, 10% Duty Cycle Max) 40mA
ESD Classification . . . . . ≤2000V

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CerDIP Package	83	21

Power Dissipation (At +75°C)
CerDIP Package 1.20W
Power Dissipation Derating Factor (Above +75°C)
CerDIP Package . . . . . 12.0mW/°C
Junction Temperature . . . . . +175°C
Storage Temperature Range . . . . . -65°C to +150°C
Lead Temperature (Soldering 10s) . . . . . +275°C

Recommended Operating Conditions

Operating Temperature Range . . . . . -55°C to +125°C
Operating Supply Voltage ($\pm V_{SUPPLY}$) . . . . . ±15V
Analog Input Voltage (V_S) . . . . . $\pm V_{SUPPLY}$
Logic Low Level (V_{AL}) . . . . . 0V to 0.8V
Logic High Level (V_{AH}) . . . . . 2.4V to $+V_{SUPPLY}$
Max RMS Current, S or D 8mA

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

TABLE 1. D.C. ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Tested at: $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = −15V, V_{EN} = 2.4V, unless otherwise specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE (°C)	MIN	MAX	UNITS
Input Leakage Current	I_{IH}	Measure inputs sequentially, connect all unused inputs to GND	1, 2, 3	+25, +125, -55	-1.0	1.0	µA
	I_{IL}		1, 2, 3	+25, +125, -55	-1.0	1.0	µA
Source "OFF" Leakage Current	$+I_{S(OFF)}$	V_S = +10V, V_D = -10V, V_{EN} = 0.8V, All unused inputs = -10V	1	+25	-10	10	nA
			2, 3	+125, -55	-50	50	nA
	$-I_{S(OFF)}$	V_S = -10V, V_D = +10V, V_{EN} = 0.8V, All unused inputs = +10V	1	+25	-10	10	nA
			2, 3	+125, -55	-50	50	nA
Drain "OFF" Leakage Current	$+I_{D(OFF)}$	V_D = +10V, V_{EN} = 0.8V, All unused inputs = -10V	1	+25	-10	10	nA
			2, 3	+125, -55	-200	200	nA
	$-I_{D(OFF)}$	V_D = -10V, V_{EN} = 0.8V, All unused inputs = +10V	1	+25	-10	10	nA
			2, 3	+25 to +125	-200	200	nA
Channel "ON" Leakage Current	$+I_{D(ON)}$	V_S = V_D = +10V All unused inputs = -10V	1	+25	-10	10	nA
			2, 3	+125, -55	-200	200	nA
	$-I_{D(ON)}$	V_S = V_D = -10V All unused inputs = +10V	1	+25	-10	10	nA
			2, 3	+125, -55	-200	200	nA
Positive Supply Current	+I	V_A = 0V, V_{EN} = 2.4V	1, 2, 3	+25, +125, -55	-	2.4	mA
Negative Supply Current	-I	V_A = 0V, V_{EN} = 2.4V	1, 2, 3	+25, +125, -55	-1.0	-	mA
Standby Positive Supply Current	$+I_{SBY}$	V_A = 0V, V_{EN} = 0V	1, 2, 3	+25, +125, -55		2.4	mA
Standby Negative Supply Current	$-I_{SBY}$	V_A = 0V, V_{EN} = 0V	1, 2, 3	+25, +125, -55	-1.0	-	mA
Switch "ON" Resistance	$+R_{DS1}$	V_S = 10V, I_D = 1mA	1	+25	-	300	Ω
			2, 3	+125, -55	-	400	Ω
	$-R_{DS1}$	V_S = -10V, I_D = -1mA	1	+25	-	300	Ω
			2, 3	+125, -55	-	400	Ω

TABLE 1. D.C. ELECTRICAL PERFORMANCE SPECIFICATIONS (Continued)

Device Tested at: $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = −15V, V_{EN} = 2.4V, unless otherwise specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE (°C)	MIN	MAX	UNITS
Logic Level Voltage	V_{AL}	Note 1	1, 2, 3	+25, +125	-	0.8	V
	V_{AH}	Note 1	1, 2, 3	-55	2.4	-	V

TABLE 2. A.C. ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Tested at: $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = −15V, V_{EN} = 2.4V, unless otherwise specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE (°C)	MIN	MAX	UNITS
Break-Before-Make Time Delay	t_D	R_L = 200Ω, C_L = 12.5pF	9	+25	25		ns
Propagation Delay Times: Address Inputs to I/O Channel Times	t_A	R_L = 10MΩ, C_L = 14pF	9	+25		500	ns
			10, 11	+125, -55		1000	ns
Enable to I/O	$t_{ON(EN)}$	R_L = 200Ω, C_L = 12.5pF	9	+25		500	ns
			10, 11	+125, -55		1000	ns
	$t_{OFF(EN)}$	R_L = 200Ω, C_L = 12.5pF	9	+25		500	ns
			10, 11	+125, -55		1000	ns

TABLE 3. ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Tested at: $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = −15V, V_{EN} = 2.4V, unless otherwise specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTE	TEMPERATURE (°C)	MIN	MAX	UNITS
Capacitance Address Input	C_A	V+ = V- = 0V, f = 1MHz	2	+25		10	pF
Capacitance Output Switch	C_{OS}	V+ = V- = 0V f = 1MHz	2	+25		45	pF
Capacitance Input Switch	C_{IS}	V+ = V- = 0V, f = 1MHz	2	+25		12	pF
Charge Transfer Error	V_{CTE}	V_S = GND, V_{GEN} = 0V to 5V	2	+25		10	mV
Off Isolation	V_{ISO}	V_{EN} = 0.8V, R_L = 1kΩ, C_L = 15pF, V_S = $7V_{RMS}$, f = 100kHz	2, 3	+25	-50		dB

NOTES:

1. Used for forcing conditions for all DC Tests, unless otherwise specified.
2. The parameters listed in this table are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.
3. Worst case isolation occurs on channel 4 due to proximity of the output pins.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

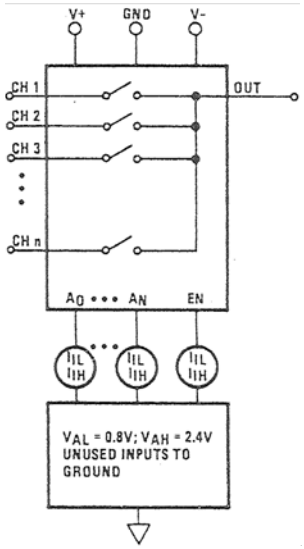
MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (See Tables 1, 2, 3)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1 (Note 4), 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C & D Endpoints	1

NOTE:

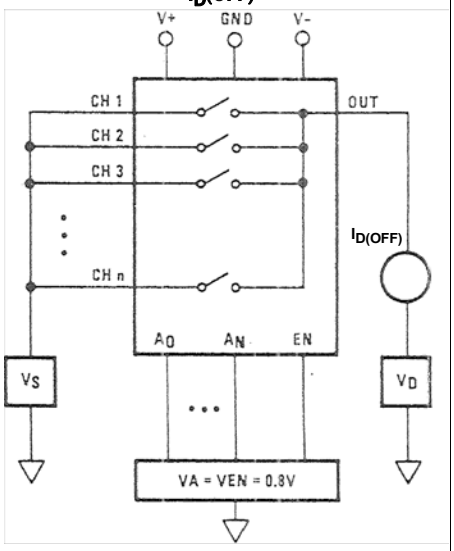
4. PDA applies to Subgroup 1 only. No other subgroups are included in PDA.

Test Circuits

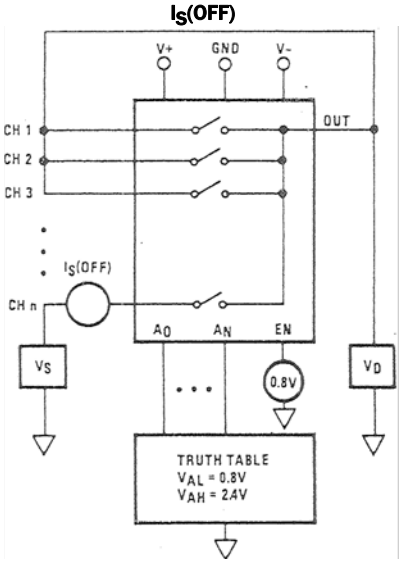
INPUT LEAKAGE CURRENT



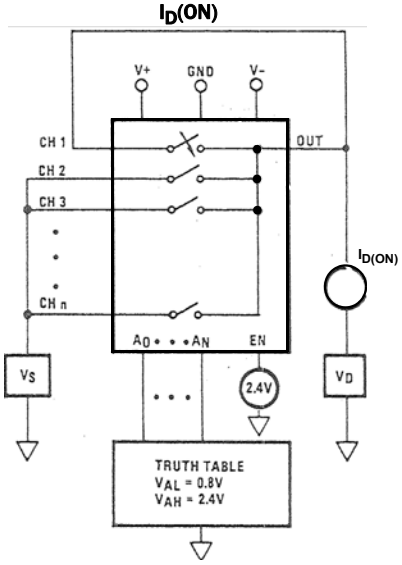
$I_{D(OFF)}$



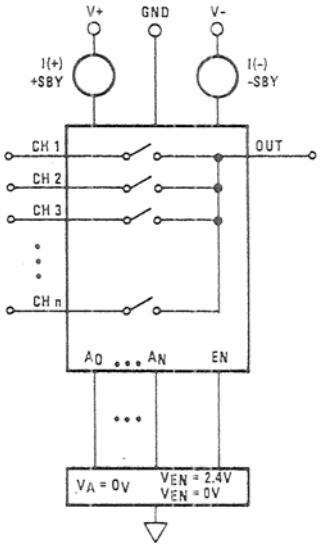
$I_{S(OFF)}$



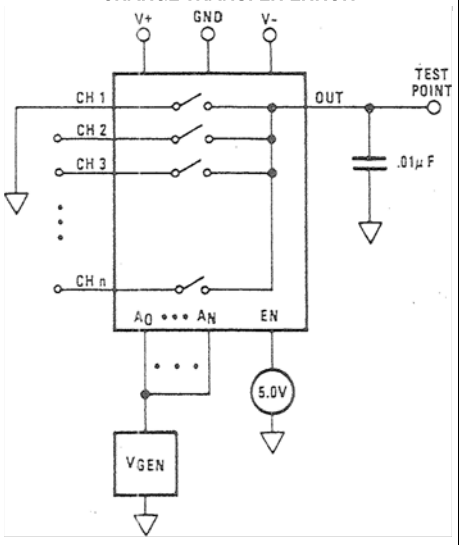
$I_{D(ON)}$



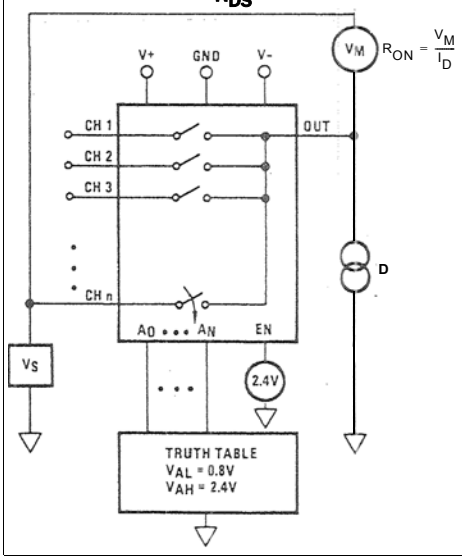
SUPPLY CURRENTS



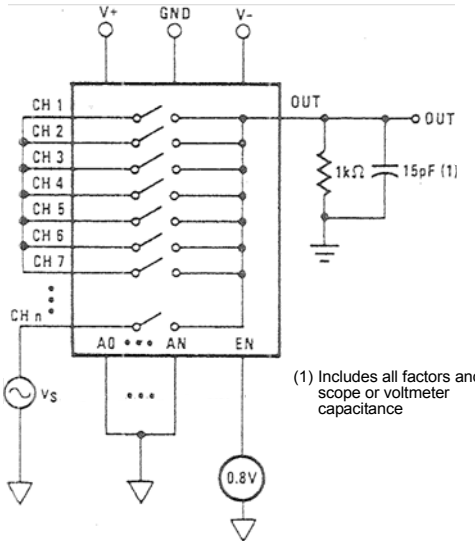
CHARGE TRANSFER ERROR



R_{DS}

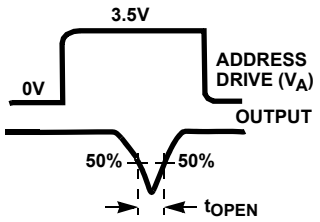


OFF CHANNEL ISOLATION

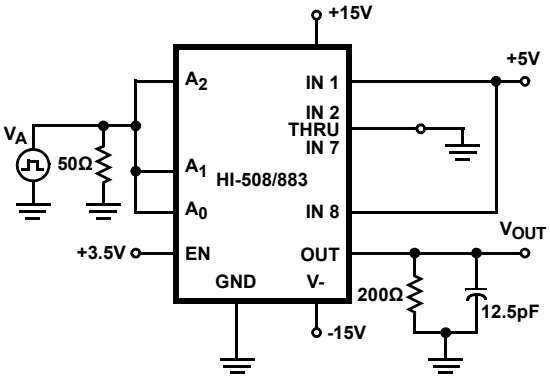


(1) Includes all factors and scope or voltmeter capacitance

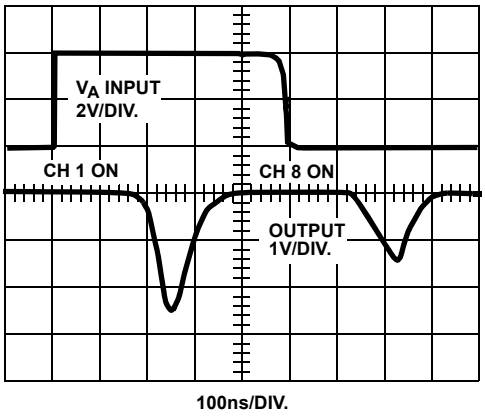
Switching Waveforms

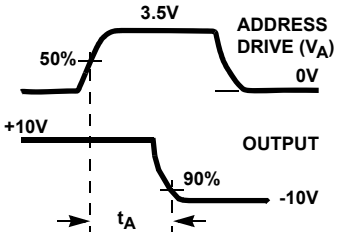


BREAK-BEFORE-MAKE DELAY (t_{OPEN})

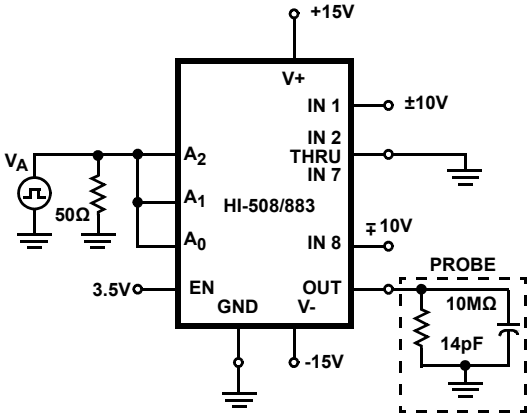


BREAK-BEFORE-MAKE DELAY (t_{OPEN})

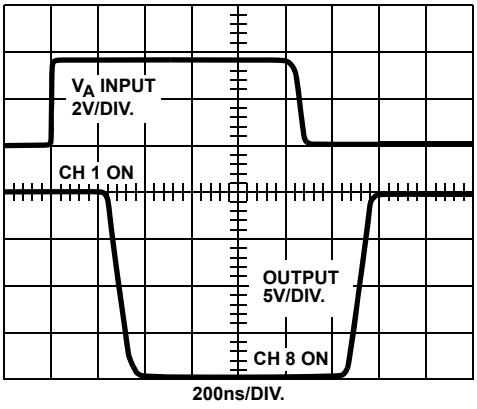




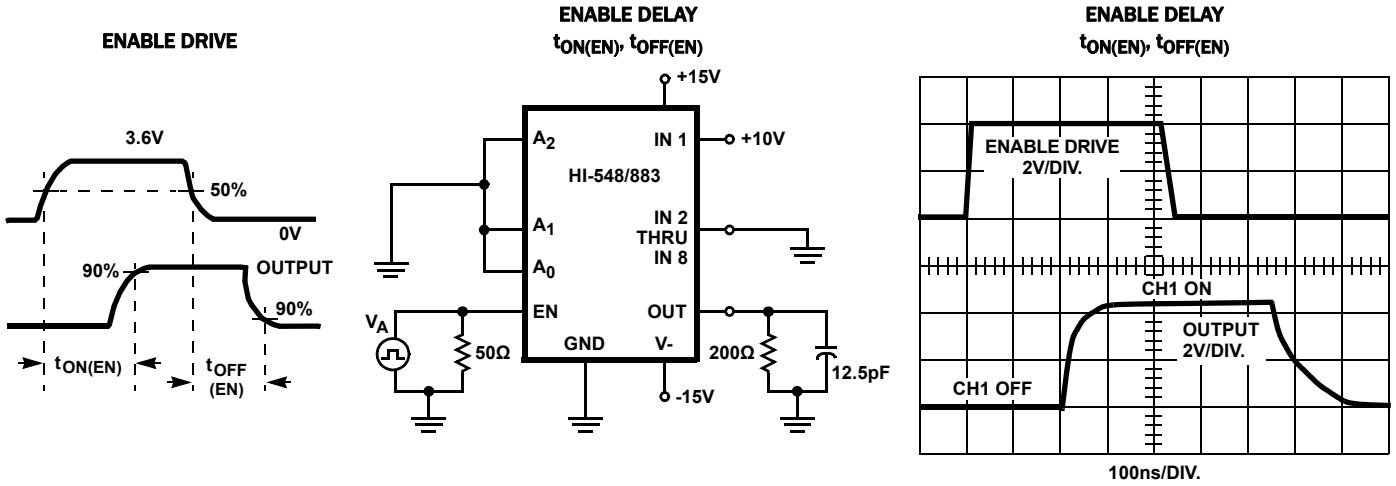
ACCESS TIME vs LOGIC LEVEL (HIGH)



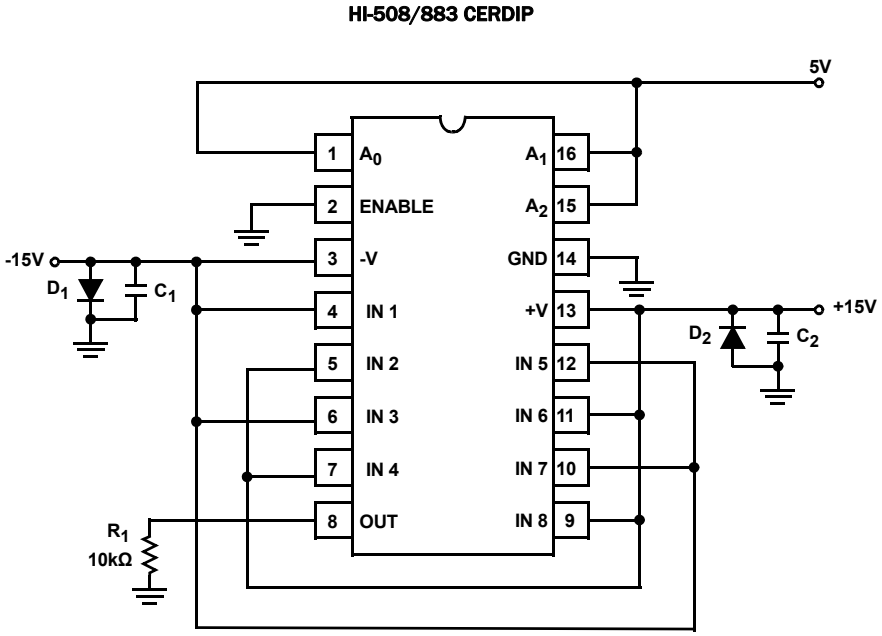
ACCESS TIME



Switching Waveforms



Burn-In Circuit

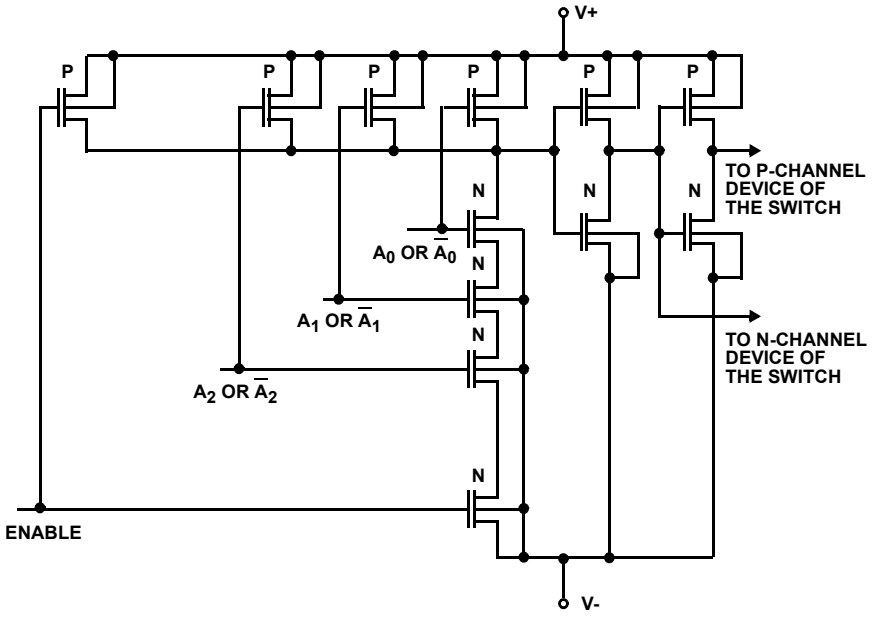


NOTES:

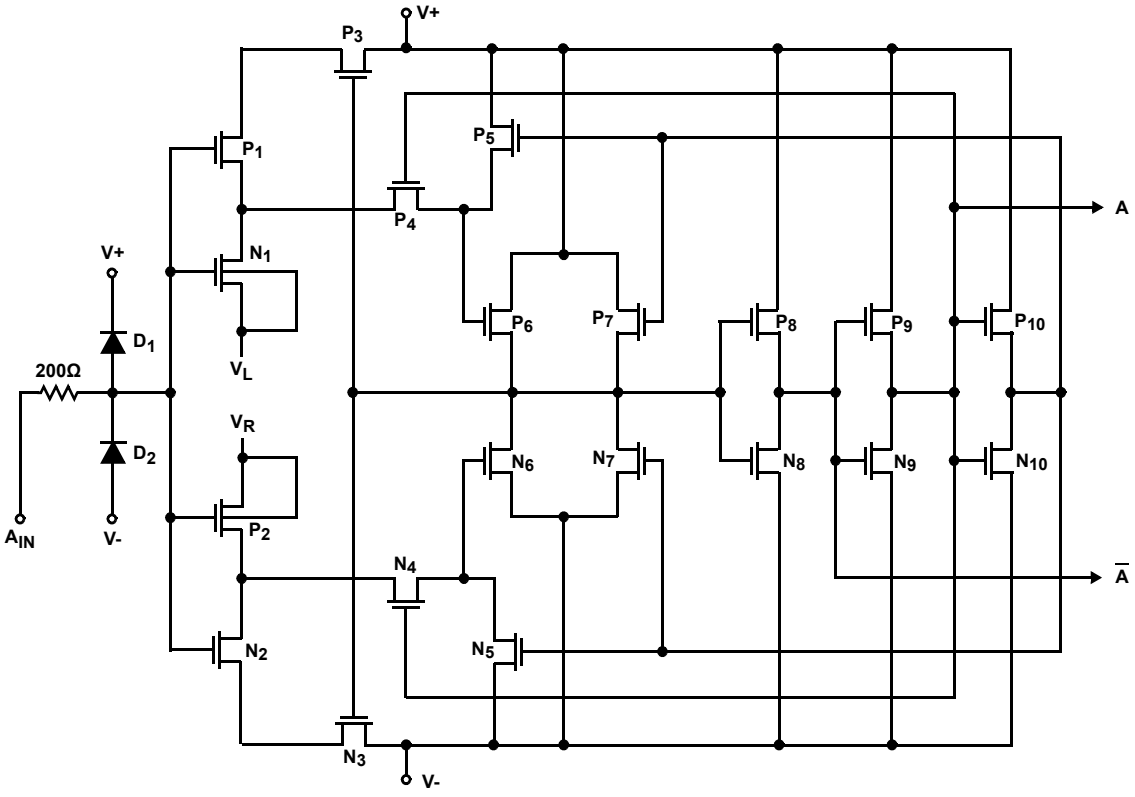
R_1 = 10kΩ ± 5% 1/2W or 1/4W (per socket)
C_1, C_2 = 0.01µF (per socket) or 0.1µF (per row)
D_1, D_2 = 1N4002 (or equivalent) (per board)

Schematic Diagrams

ADDRESS DECODER



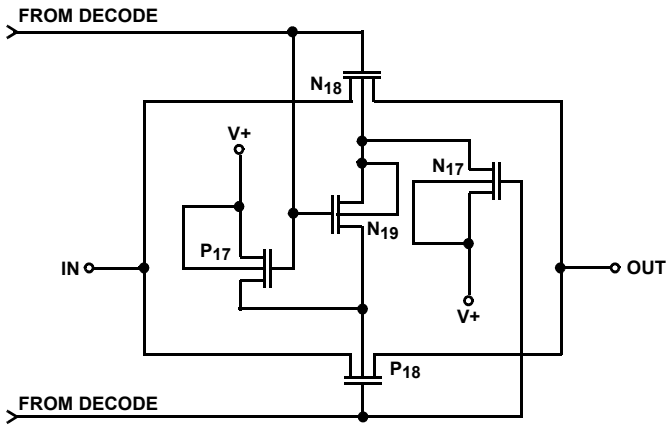
ADDRESS INPUT BUFFER AND LEVEL SHIFTER



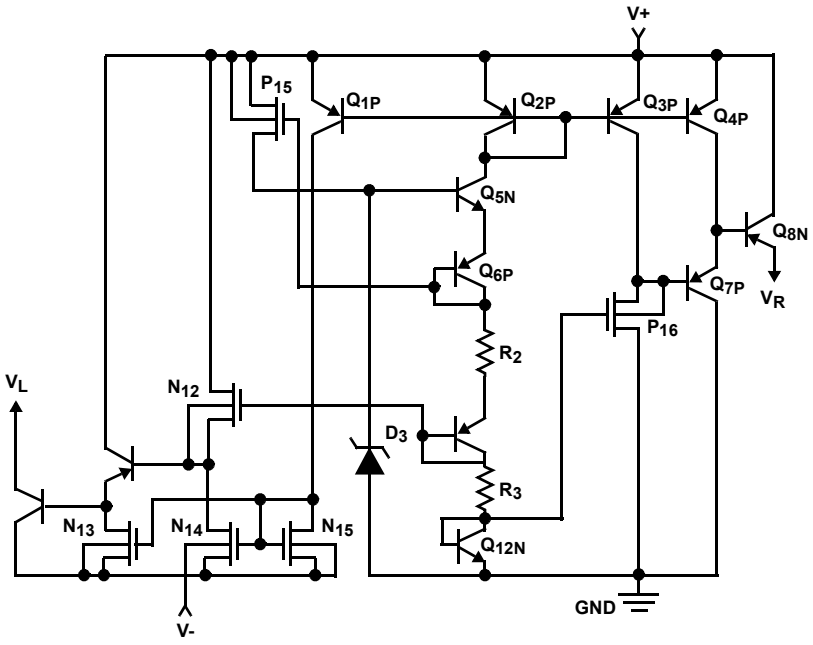
All N-Channel bodies to V-, all P-Channel bodies to V+, unless otherwise indicated.

Schematic Diagrams (Continued)

MULTIPLEX SWITCH



TTL REFERENCE CIRCUIT



Die Characteristics

DIE DIMENSIONS:

81.9mils x 90.2mils x 19mils

METALLIZATION:

Type: Al
Thickness: 16kÅ ±2kÅ

GLASSIVATION:

Type: Nitride
Thickness: 7kÅ ± 0.7kÅ

WORST CASE CURRENT DENSITY:

1.4×10^5 A/cm^2

TRANSISTOR COUNT:

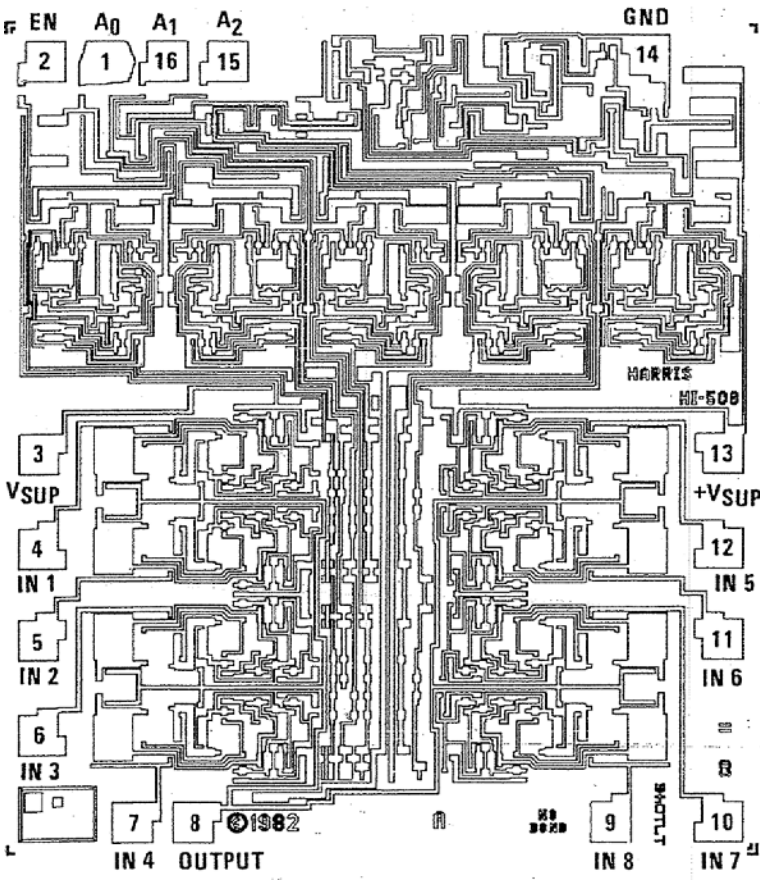
243

PROCESS:

CMOS-DI

Metallization Mask Layout

HI-508/883



Design Information

The information contained in this section has been developed through characterization and is for use as application and design information only. No guarantee is implied.

Typical Performance Curves

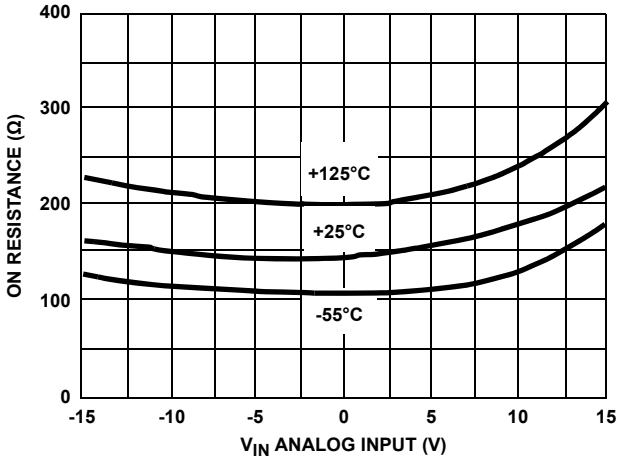


FIGURE 1. ON RESISTANCE vs ANALOG INPUT VOLTAGE, TEMPERATURE

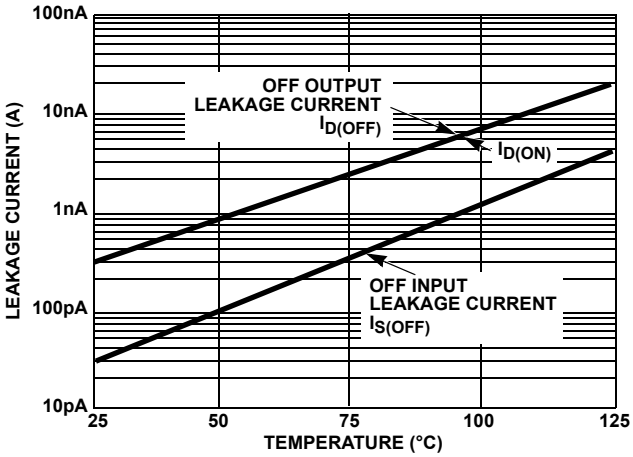


FIGURE 2. LEAKAGE CURRENT vs TEMPERATURE

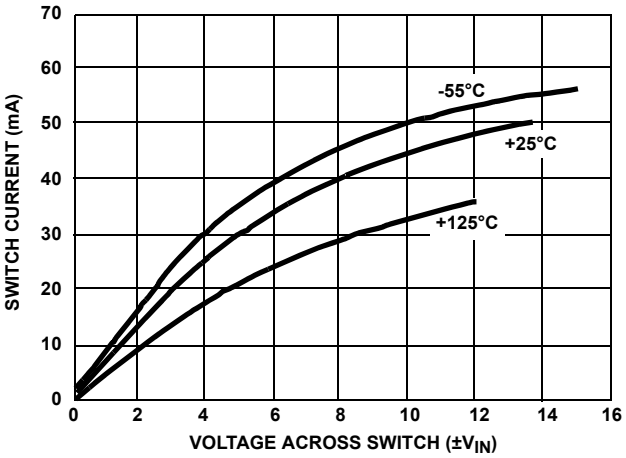


FIGURE 3. ON CHANNEL CURRENT vs VOLTAGE

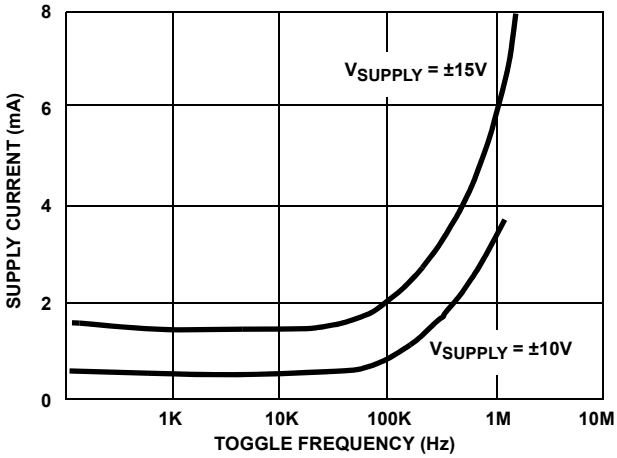
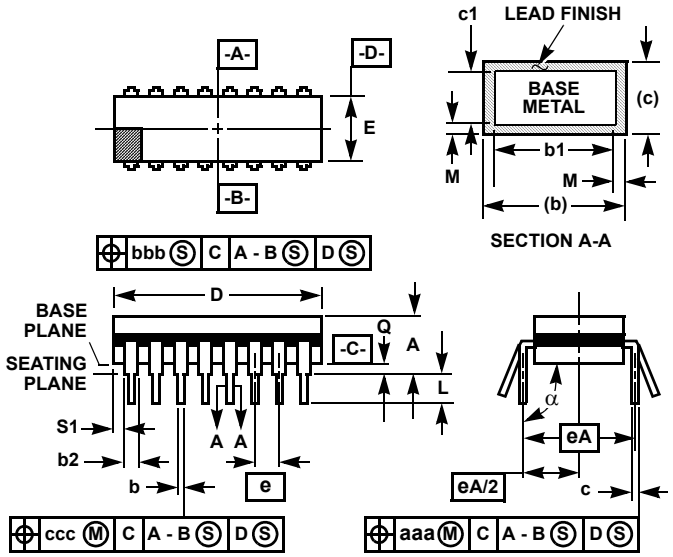


FIGURE 4A. SUPPLY CURRENT vs TOGGLE FREQUENCY

Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

F16.3 MIL-STD-1835 GDIP1-T16 (D-2, CONFIGURATION A)
16 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	16		16		8

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