HI-548/883, HI-549/883

Single 8/Differential 4-Channel CMOS Analog Multiplexers with Active Overvoltage Protection

FN8256
Rev.0.00
April 9, 2012

The HI-548/883 and HI-549/883 are analog multiplexers with active overvoltage protection and guaranteed r_{ON} matching. Analog input levels may greatly exceed either power supply without damaging the device or disturbing the signal path of other channels. Active protection circuitry assures that signal fidelity is maintained even under fault conditions that would destroy other multiplexers.

Analog inputs can withstand constant $70V_{P-P}$ levels with ±15V supplies. Digital inputs will also sustain continuous faults up to 4V greater than either supply. In addition, signal sources are protected from short circuiting should multiplexer supply loss occur. Each input presents 1kΩ of resistance under this condition. These features make the HI-548/883 and HI-549/883 ideal for use in systems where the analog inputs originate from external equipment or separately powered circuitry. Both devices are fabricated with 44V Dielectrically Isolated CMOS technology. The HI-548/883 is an 8-channel device, and the HI-549/883 is a 4-channel differential version. If input overvoltage protection is not needed, the HI-508/883 and HI-509/883 multiplexers are recommended. For further information see Application Note AN520.

Features

- This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- No Channel Interaction During Overvoltage
- Guaranteed r_{ON} Matching
- 44V Maximum Power Supply
- Break-Before-Make Switching
- Analog Signal Range . . . . . ±15V
- Access Time (Max) 1.0µs
- Power Dissipation (Max) 45mW

Applications

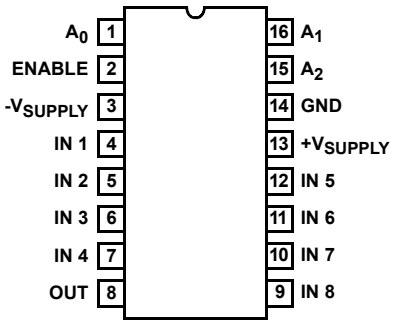
- Data Acquisition Systems
- Control Systems
- Telemetry

Ordering Information

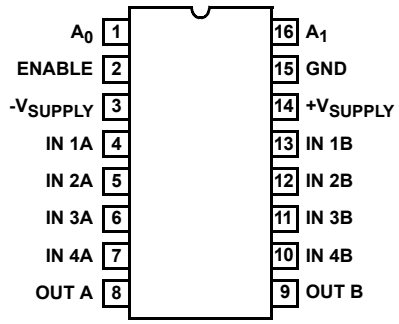
PART #	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
HI1-0548/883	HI1-548/883	-55 to 125	16 Ld CerDIP	F16.3
HI4-0548/883	HI4-0548 /883	-55 to 125	20 Ld CLCC	J20.A
HI1-0549/883	HI1-549/883	-55 to 125	16 Ld CerDIP	F16.3

Pin Configurations

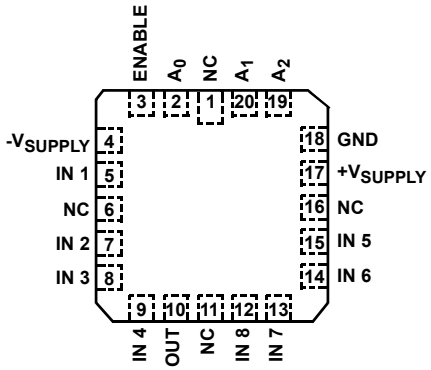
HI-548/883
(16 LD CERDIP)
TOP VIEW



HI-549/883
(16 LD CERDIP)
TOP VIEW

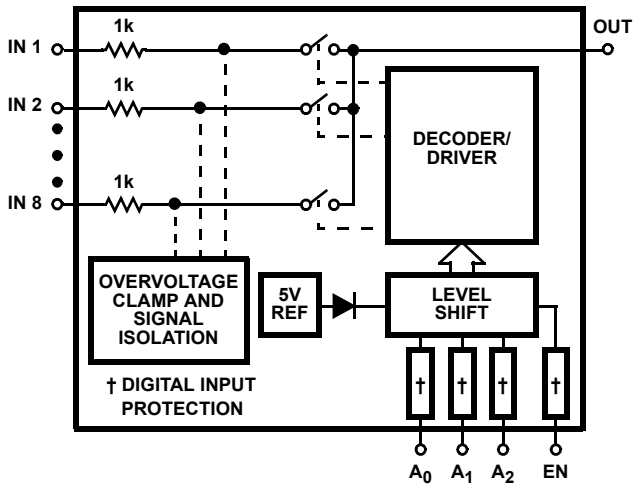


HI-548/883
(20 LD CLCC)
TOP VIEW



Functional Diagrams

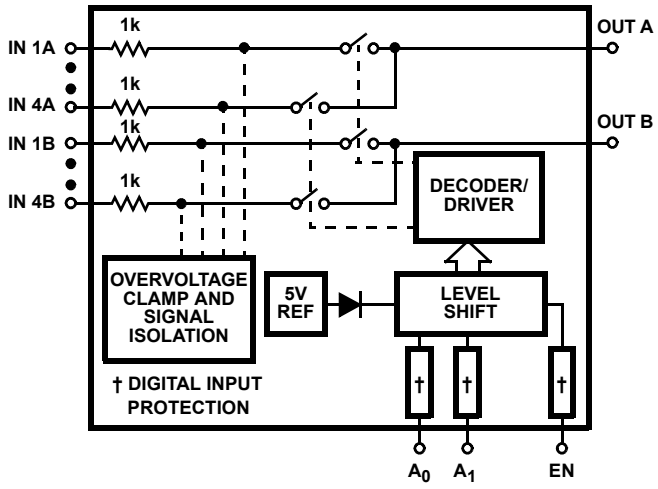
HI-548/883



TRUTH TABLE HI-548/883

A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	L	None
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

HI-549/883



TRUTH TABLE HI-549/883

A_1	A_0	EN	"ON" CHANNEL PAIR
X	X	L	None
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

Absolute Maximum Ratings

Voltage Between Supply Pins 44V
$+V_{SUPPLY}$ to Ground 22V
$-V_{SUPPLY}$ to Ground 25V
Analog Input Voltage, $+V_S$ . . . . . $+V_{SUPPLY}$ +20V
$-V_S$ . . . . . $-V_{SUPPLY}$ -20V
Digital Input Voltage, $+V_{EN}$, $+V_A$ . . . . . $+V_{SUPPLY}$ +4V
$-V_{EN}$, $-V_A$ . . . . . $-V_{SUPPLY}$ +4V
or 20mA, whichever occurs first
Continuous Current, S or D 20mA
Peak Current, S or D (Pulsed at 1ms, 10% Duty Cycle Max) 40mA
ESD Classification . . . . . ≤2000V

Recommended Operating Conditions

Operating Temperature Range . . . . . -55°C to +125°C
Operating Supply Voltage ($\pm V_{SUPPLY}$) . . . . . ±15V
Analog Input Voltage (V_S) . . . . . $\pm V_{SUPPLY}$
Logic Low Level (V_{AL}) . . . . . 0V to 0.8V
Logic High Level (V_{AH}) . . . . . +4V to $+V_{SUPPLY}$
Max RMS Current, S or D 8mA

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CerDIP Package	80	26
CLCC Package	76	19

Power Dissipation (AT +75°C)
CerDIP Package 1.25W
CLCC Package 1.32W
Power Dissipation Derating Factor (Above +75°C)
CerDIP Package . . . . . 12.5mW/°C
CLCC Package . . . . . 13.2mW/°C
Junction Temperature . . . . . +175°C
Storage Temperature Range . . . . . -65°C to +150°C
Lead Temperature (Soldering 10s) . . . . . +275°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

TABLE 1. D.C. ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Tested at: $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = −15V, V_{EN} = 4.0V, unless otherwise specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE (°C)	MIN	MAX	UNITS
Input Leakage Current	I_{IH}	Measure inputs sequentially, connect all unused inputs to GND	1, 2, 3	+25, +125, -55	-1.0	1.0	µA
	I_{IL}		1, 2, 3	+25, +125, -55	-1.0	1.0	µA
Source "OFF" Leakage Current	$+I_{S(OFF)}$	V_S = +10V, V_D = -10V, V_{EN} = 0.8V, All unused inputs = -10V	1	+25	-10	10	nA
			2, 3	+125, -55	-50	50	nA
	$-I_{S(OFF)}$	V_S = -10V, V_D = +10V, V_{EN} = 0.8V, All unused inputs = +10V	1	+25	-10	10	nA
			2, 3	+125, -55	-50	50	nA
Drain "OFF" Leakage Current	$+I_{D(OFF)}$	V_D = +10V, V_{EN} = 0.8V, All unused inputs = -10V	1	+25	-10	10	nA
		HI-548/883	2, 3	+125, -55	-200	200	nA
		HI-549/883	2, 3	+125, -55	-100	100	nA
	$-I_{D(OFF)}$	V_D = -10V, V_{EN} = 0.8V, All unused inputs = +10V	1	+25	-10	10	nA
		HI-548/883	2, 3	+25 to +125	-200	200	nA
		HI-549/883	2, 3	+125, -55	-100	100	nA
Channel "ON" Leakage Current	$+I_{D(ON)}$	V_S = V_D = +10V All unused inputs = -10V	1	+25	-10	10	nA
		HI-548/883	2, 3	+125, -55	-200	200	nA
		HI-549/883	2, 3	+125, -55	-100	100	nA
	$-I_{D(ON)}$	V_S = V_D = -10V All unused inputs = +10V	1	+25	-10	10	nA
		HI-548/883	2, 3	+125, -55	-200	200	nA
		HI-549/883	2, 3	+125, -55	-100	100	nA

TABLE 1. D.C. ELECTRICAL PERFORMANCE SPECIFICATIONS (Continued)

Device Tested at: $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = −15V, V_{EN} = 4.0V, unless otherwise specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE (°C)	MIN	MAX	UNITS
Overvoltage Protected, Leakage Current Into the Drain Terminal of an "OFF" Switch	I_D(OFF) Overvoltage	V_S = 33V, V_D = 0V, V_{EN} = 0.8V V_S applied at ≤25% duty cycle	1, 2, 3	+25, +125, -55	-2.0	2.0	µA
		V_S = -33V, V_D = 0V, V_{EN} = 0.8V V_S applied at ≤25% duty cycle	1, 2, 3	+25, +125, -55	-2.0	2.0	µA
Positive Supply Current	+I	V_A = 0V, V_{EN} = 4.0V	1, 2, 3	+25, +125, -55	-	2.0	mA
Negative Supply Current	-I	V_A = 0V, V_{EN} = 4.0V	1, 2, 3	+25, +125, -55	-1.0	-	mA
Standby Positive Supply Current	$+I_{SBY}$	V_A = 0V, V_{EN} = 0V	1, 2, 3	+25, +125, -55		2.0	mA
Standby Negative Supply Current	$-I_{SBY}$	V_A = 0V, V_{EN} = 0V	1, 2, 3	+25, +125, -55	–1.0	-	mA
Switch "ON" Resistance	$+r_{DS1}$	V_S = 10V, I_D = 100µA	1	+25	-	1500	Ω
			2, 3	+125, -55	-	1800	Ω
	$-r_{DS1}$	V_S = -10V, I_D = -100µA	1	+25	-	1500	Ω
			2, 3	+125, -55	-	1800	Ω
Logic Level Voltage	V_{AL}	Notes 1, 2	1, 2, 3	+25, +125, -55	-	0.8	V
	V_{AH}	Notes 1, 2	1, 2, 3	+25, +125, -55	4.0	-	V
Difference in Switch "ON" Resistance Between Channels	$+\Delta r_{DS1}$	$\frac{(+r_{DS1}MAX) - (+r_{DS1}MIN) \times 100}{+r_{DS1}AVE}$	1	+25	-	7	%
	$-\Delta r_{DS1}$	$\frac{(-r_{DS1}MAX) - (-r_{DS1}MIN) \times 100}{-r_{DS1}AVE}$	1	+25	-	7	%

TABLE 2. A.C. ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Tested at: $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = −15V, V_{EN} = 4.0V, unless otherwise specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE (°C)	MIN	MAX	UNITS
Break-Before-Make Time Delay	t_D	R_L = 1kΩ, C_L = 12.5pF	9	+25	25		ns
Propagation Delay Times: Address Inputs to I/O Channel Times	t_A	R_L = 10MΩ, C_L = 14pF	9	+25		500	ns
			10, 11	+125, -55		1000	ns
Enable to I/O	$t_{ON(EN)}$	R_L = 1kΩ, C_L = 12.5pF	9	+25		500	ns
			10, 11	+125, -55		1000	ns
	$t_{OFF(EN)}$	R_L = 1kΩ, C_L = 12.5pF	9	+25		500	ns
			10, 11	+125, -55		1000	ns

TABLE 3. ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Tested at: $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = −15V, V_{EN} = 4.0V,, unless otherwise specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTE	TEMPERATURE (°C)	MIN	MAX	UNITS
Capacitance Address Input	C_A	V+ = V- = 0V, f = 1MHz	3	+25		10	pF
Capacitance Output Switch	C_{OS}	V+ = V- = 0V HI-548/883	3	+25		45	pF
		f = 1MHz HI-549/883	3	+25		25	pF
Capacitance Input Switch	C_{IS}	V+ = V- = 0V, f = 1MHz	3	+25		15	pF
Charge Transfer Error	V_{CTE}	V_S = GND, V_{GEN} = 0V to 5V, f = 200kHz	3	+25		10	mV
Off Isolation	V_{ISO}	V_{EN} = 0.8V, R_L = 1kΩ, C_L = 15pF, V_S = $7V_{RMS}$, f = 100kHz	3, 4	+25	-50		dB

NOTES:

1. Used for forcing conditions for all DC Tests, unless otherwise specified.
2. To drive from DTL/TTL circuits, 1kΩ pull-up resistors to +5.0V supply are recommended.
3. The parameters listed in this table are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.
4. Worst case isolation occurs on channel 8B due to proximity of the output pins.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

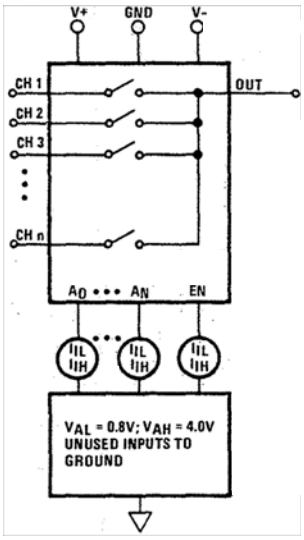
MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (See Tables 1, 2, 3)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1 (Note 5), 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C & D Endpoints	1

NOTE:

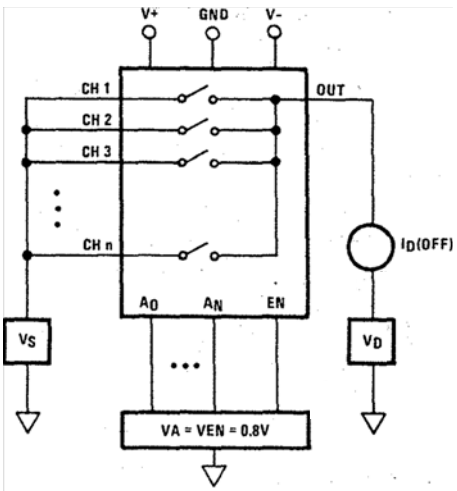
5. PDA applies to Subgroup 1 only. No other subgroups are included in PDA.

Test Circuits

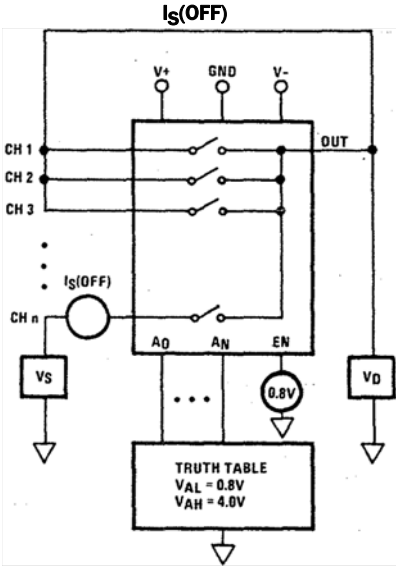
INPUT LEAKAGE CURRENT



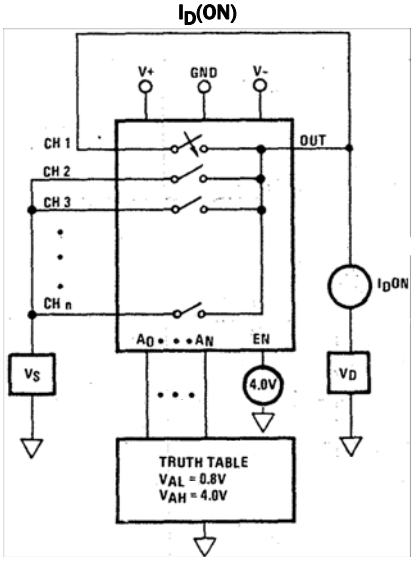
I_D(OFF)



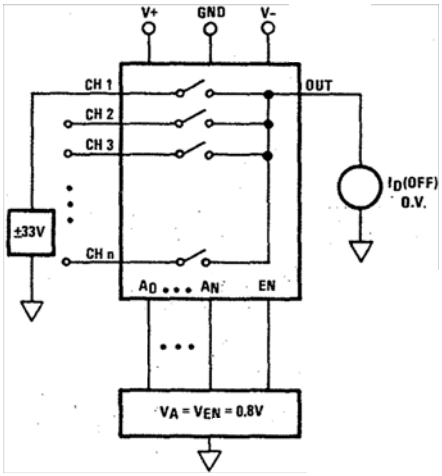
I_S(OFF)



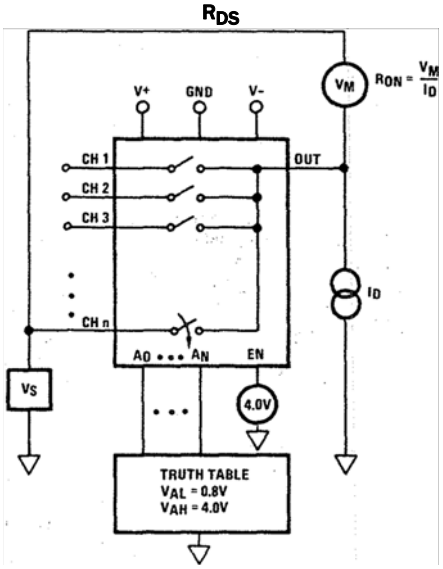
I_D(ON)



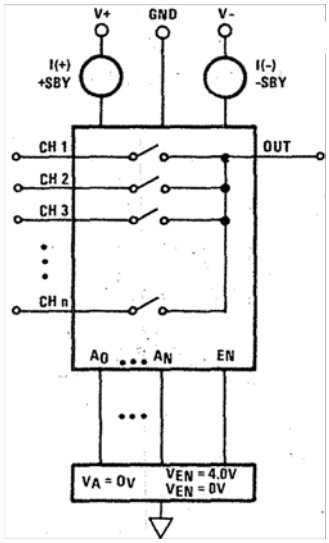
I_D(OFF) OVERVOLTAGE



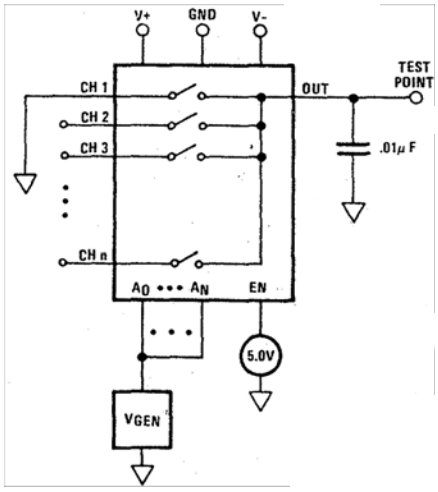
R_{DS}



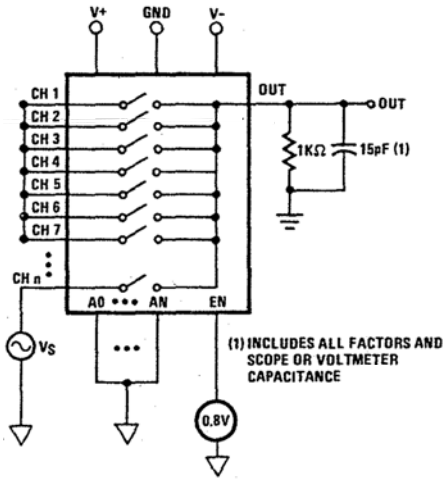
SUPPLY CURRENTS



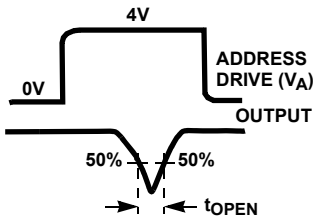
CHARGE TRANSFER ERROR



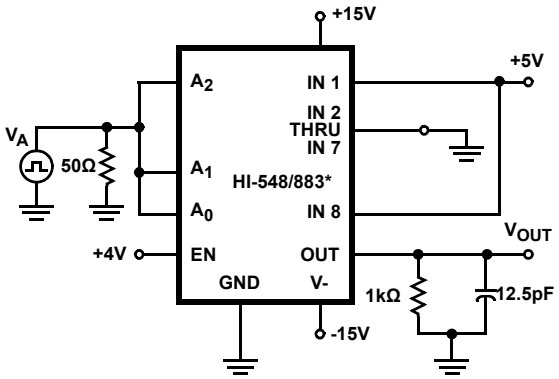
OFF CHANNEL ISOLATION



Switching Waveforms

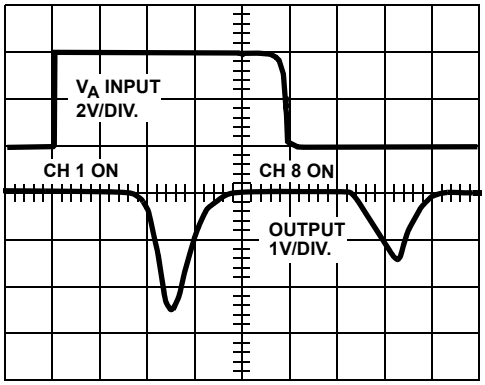


BREAK-BEFORE-MAKE DELAY (t_{OPEN})

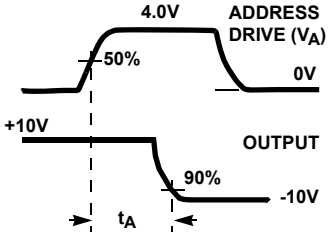


*SIMILAR CONNECTION FOR HI-549/883

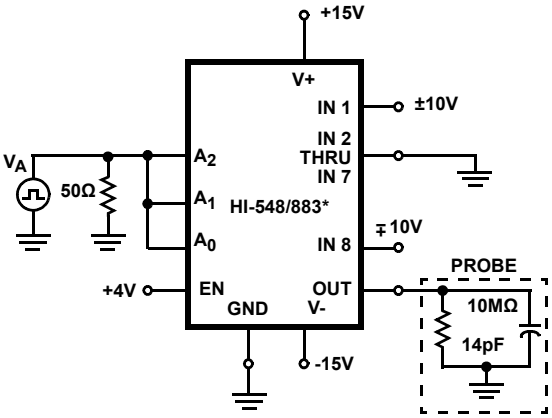
BREAK-BEFORE-MAKE DELAY (t_{OPEN})



100ns/DIV.

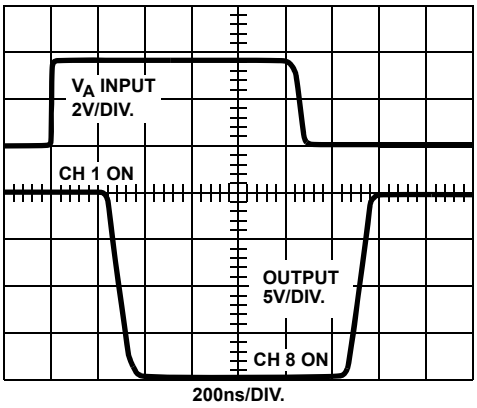


ACCESS TIME vs LOGIC LEVEL (HIGH)



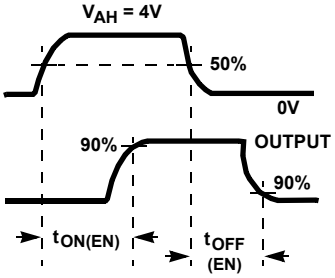
*SIMILAR CONNECTION FOR HI-549/883

ACCESS TIME

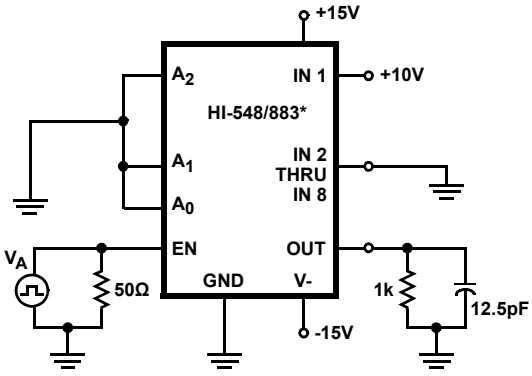


200ns/DIV.

ENABLE DRIVE

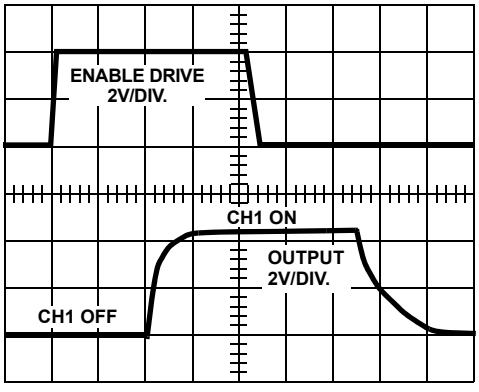


ENABLE DELAY
$t_{ON(EN)}$, $t_{OFF(EN)}$



*SIMILAR CONNECTION FOR HI-549/883

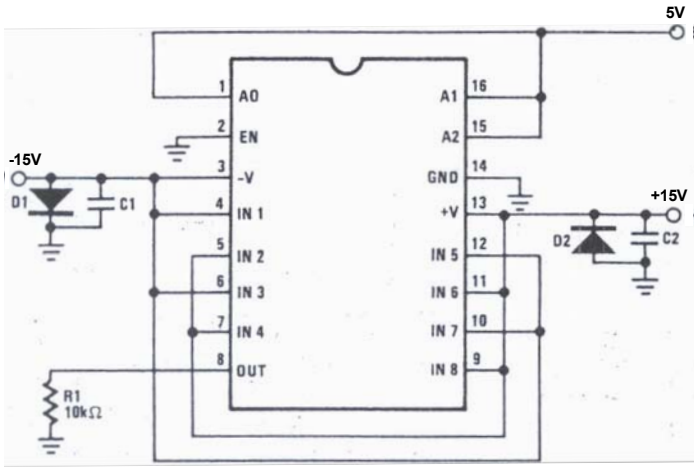
ENABLE DELAY
$t_{ON(EN)}$, $t_{OFF(EN)}$



100ns/DIV.

Burn-In Circuits

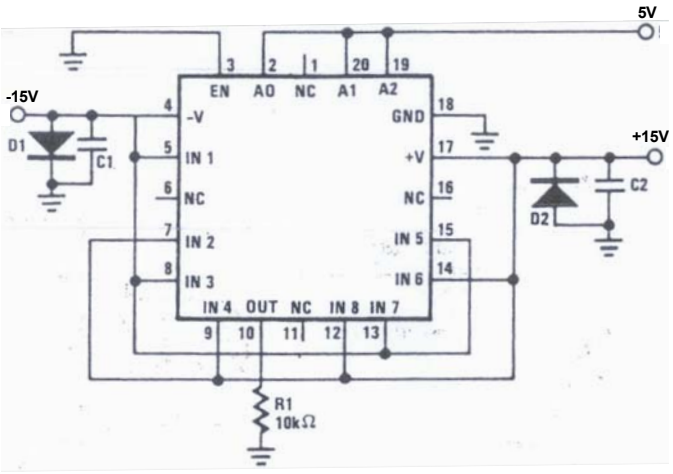
HI-548/883 CERDIP



NOTES:

R1 = 10kΩ ± 5% 1/2W or 1/4W (per socket)
C1, C2 = 0.01µF (per socket) or 0.1µF (per row)
D1, D2 = 1N4002 (or equivalent) (per board)

HI-548/883 CLCC



NOTES:

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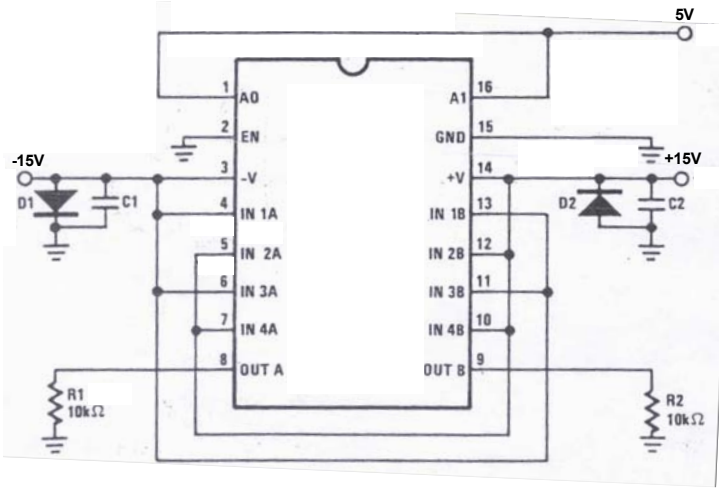
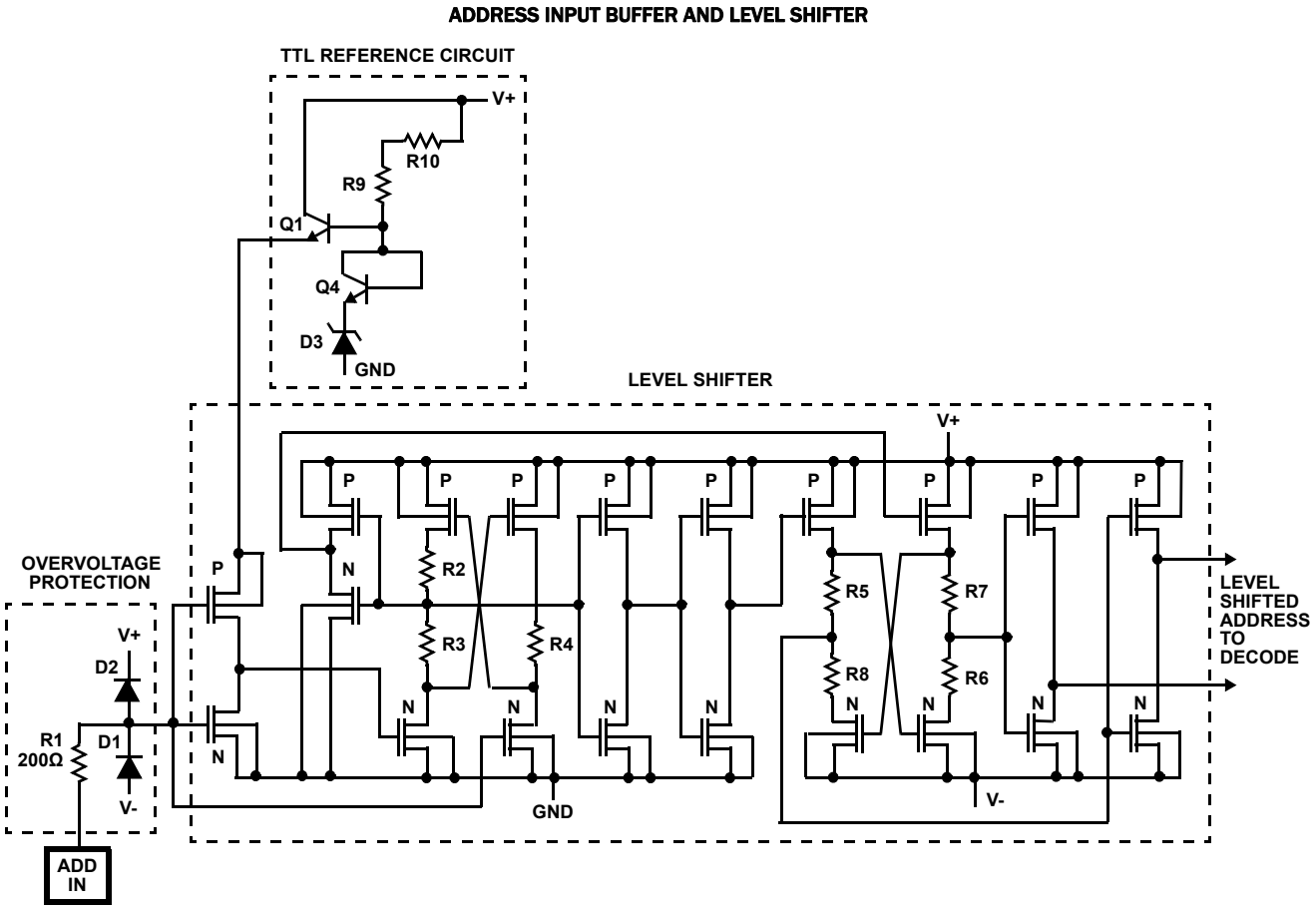
HI-549/883 CERDIP

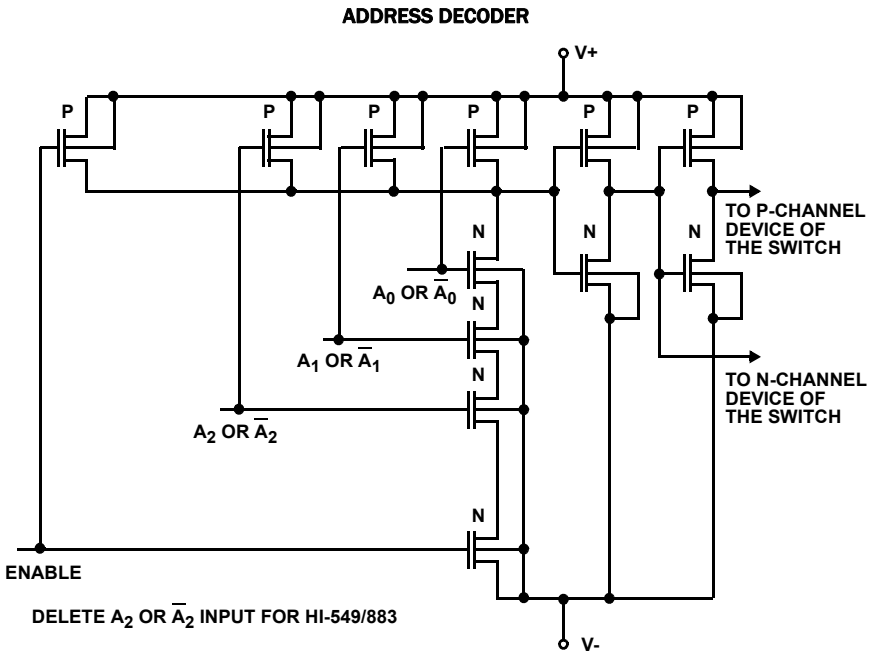


NOTES:

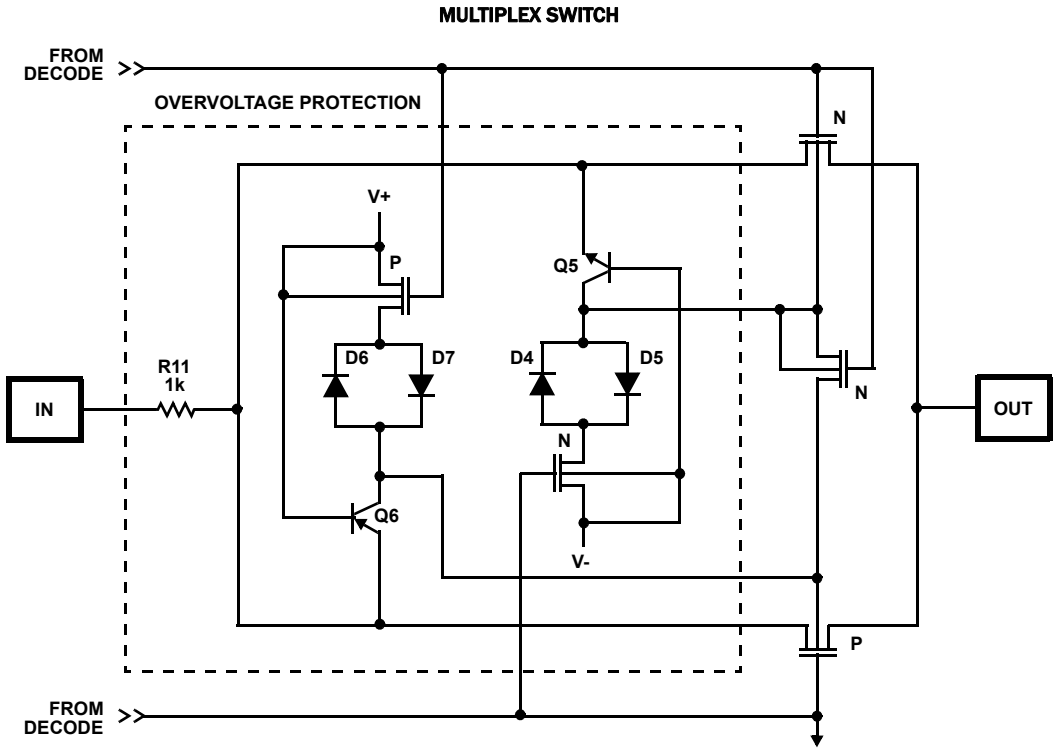
R1, R2 = 10kΩ ± 5% 1/2W or 1/4W (per socket)
C1, C2 = 0.01µF (per socket) or 0.1µF (per row)
D1, D2 = 1N4002 (or equivalent) (per board)

Schematic Diagrams





Schematic Diagrams (Continued)



Typical Performance Curves

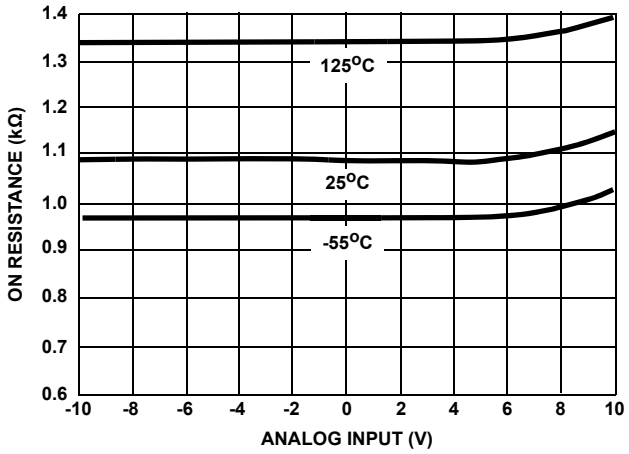


FIGURE 1. ON RESISTANCE vs ANALOG INPUT VOLTAGE

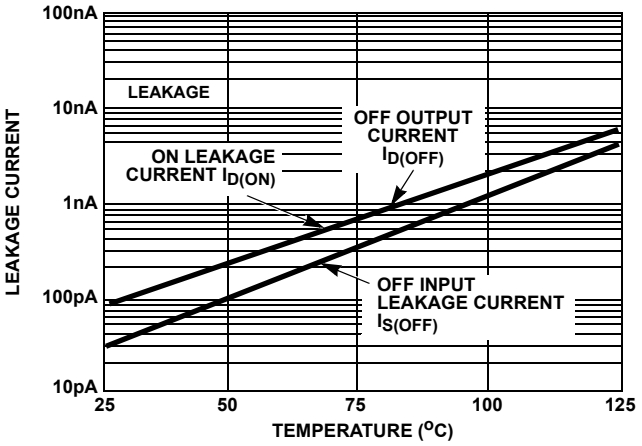


FIGURE 2. LEAKAGE CURRENT vs TEMPERATURE

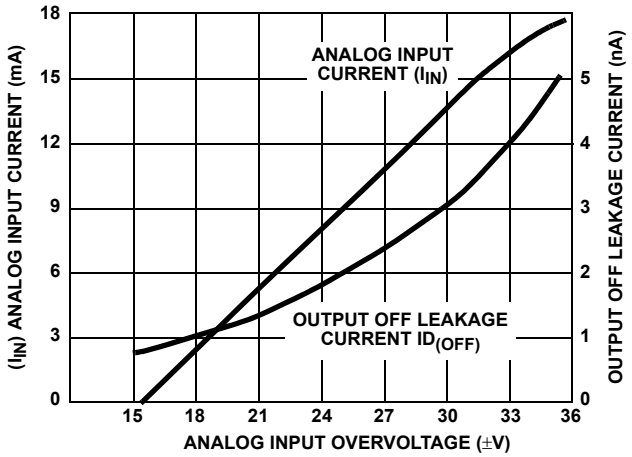


FIGURE 3. ANALOG INPUT OVERVOLTAGE CHARACTERISTICS

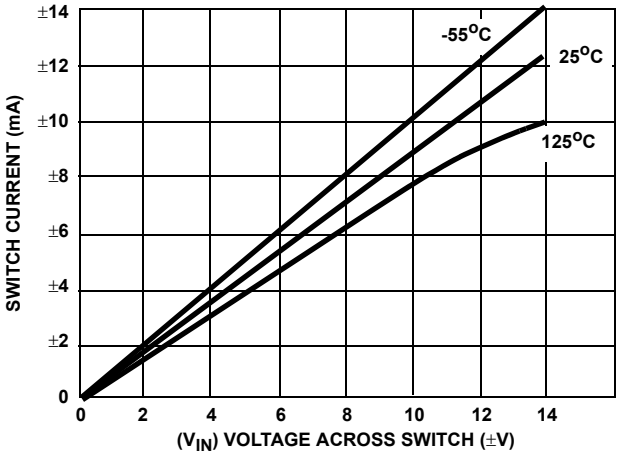


FIGURE 4. ON CHANNEL CURRENT vs VOLTAGE

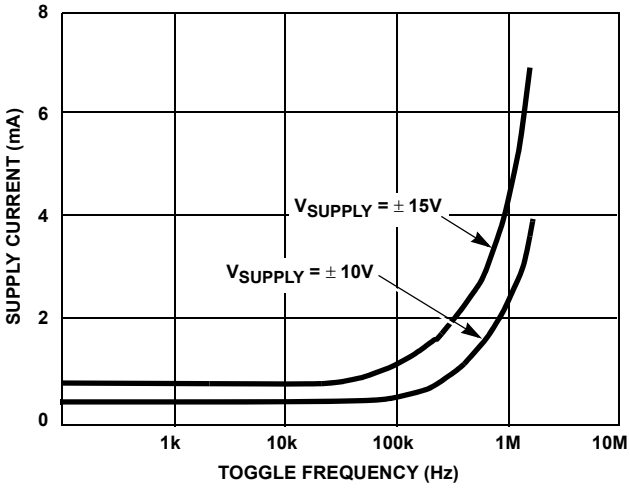


FIGURE 5. SUPPLY CURRENT vs TOGGLE FREQUENCY

Die Characteristics

DIE DIMENSIONS:

83 mils x 108 mils x 19 mils

METALLIZATION:

Type: Al
Thickness: 16kÅ ±2kÅ

GLASSIVATION:

Type: Nitride
Thickness: 7kÅ ± 0.7kÅ

WORST CASE CURRENT DENSITY:

1.4×10^5 A/cm^2

TRANSISTOR COUNT:

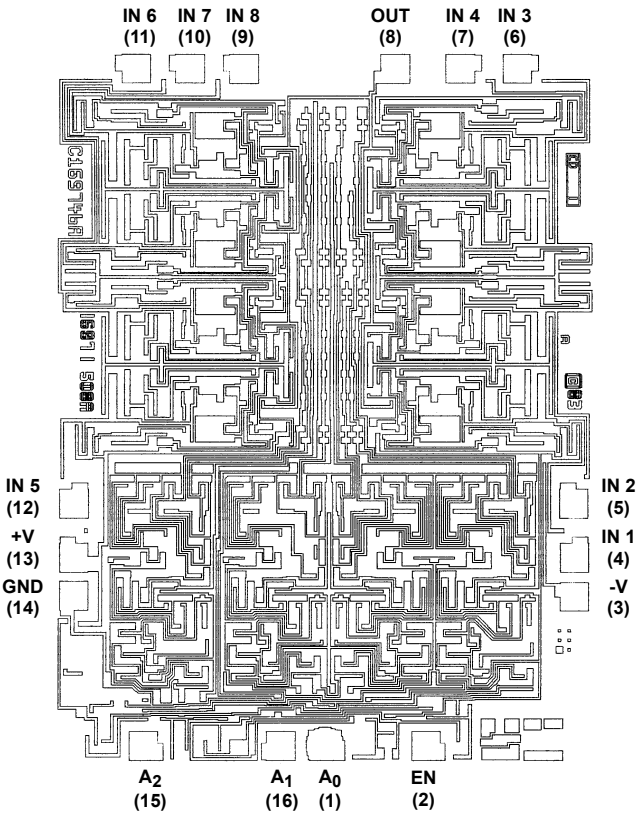
HI-548/883 - 253
HI-549/883 - 253

PROCESS:

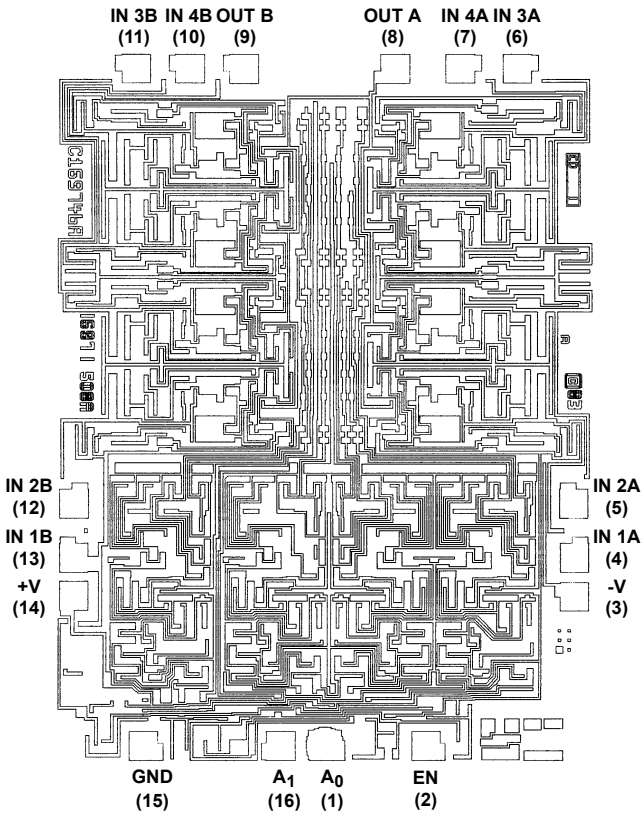
CMOS-DI

Metallization Mask Layouts

HI-548/883

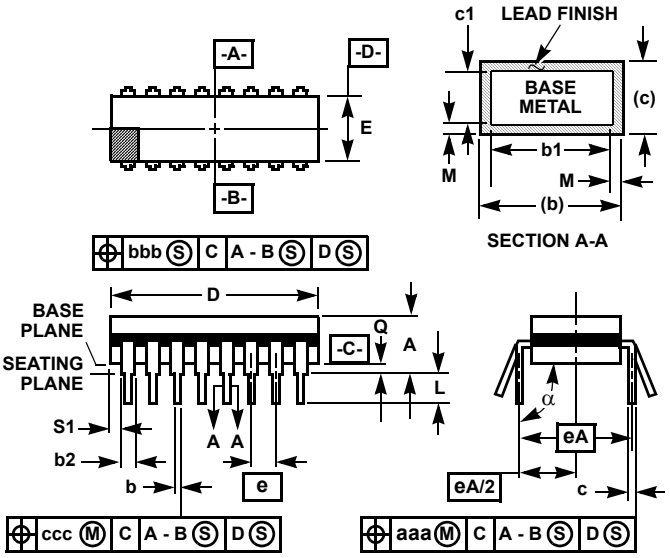


HI-549/883



NOTE: Pad numbers correspond to CerDIP numbers only.

Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

F16.3 MIL-STD-1835 GDIP1-T16 (D-2, CONFIGURATION A)
16 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	16		16		8

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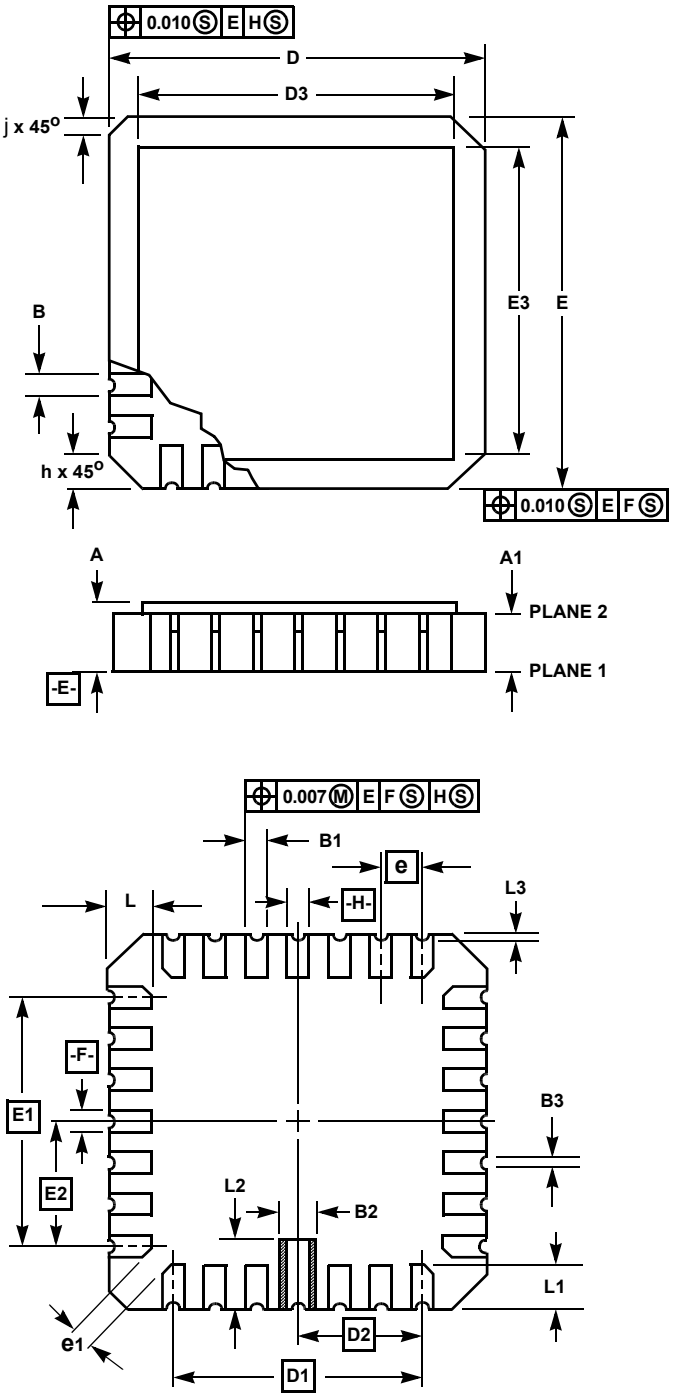
Ceramic Leadless Chip Carrier Packages (CLCC)



J20.A **MIL-STD-1835 CQCC1-N20 (C-2)**
20 PAD CERAMIC LEADLESS CHIP CARRIER PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.060	0.100	1.52	2.54	6, 7
A1	0.050	0.088	1.27	2.23	-
B	-	-	-	-	-
B1	0.022	0.028	0.56	0.71	2, 4
B2	0.072 REF		1.83 REF		-
B3	0.006	0.022	0.15	0.56	-
D	0.342	0.358	8.69	9.09	-
D1	0.200 BSC		5.08 BSC		-
D2	0.100 BSC		2.54 BSC		-
D3	-	0.358	-	9.09	2
E	0.342	0.358	8.69	9.09	-
E1	0.200 BSC		5.08 BSC		-
E2	0.100 BSC		2.54 BSC		-
E3	-	0.358	-	9.09	2
e	0.050 BSC		1.27 BSC		-
e1	0.015	-	0.38	-	2
h	0.040 REF		1.02 REF		5
j	0.020 REF		0.51 REF		5
L	0.045	0.055	1.14	1.40	-
L1	0.045	0.055	1.14	1.40	-
L2	0.075	0.095	1.91	2.41	-
L3	0.003	0.015	0.08	0.38	-
ND	5		5		3
NE	5		5		3
N	20		20		3

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NOTES:

1. Metallized castellations shall be connected to plane 1 terminals and extend toward plane 2 across at least two layers of ceramic or completely across all of the ceramic layers to make electrical connection with the optional plane 2 terminals.
2. Unless otherwise specified, a minimum clearance of 0.015 inch (0.38mm) shall be maintained between all metallized features (e.g., lid, castellations, terminals, thermal pads, etc.)
3. Symbol “N” is the maximum number of terminals. Symbols “ND” and “NE” are the number of terminals along the sides of length “D” and “E”, respectively.
4. The required plane 1 terminals and optional plane 2 terminals (if used) shall be electrically connected.
5. The corner shape (square, notch, radius, etc.) may vary at the manufacturer’s option, from that shown on the drawing.
6. Chip carriers shall be constructed of a minimum of two ceramic layers.
7. Dimension “A” controls the overall package thickness. The maximum “A” dimension is package height before being solder dipped.
8. Dimensioning and tolerancing per ANSI Y14.5M-1982.
9. Controlling dimension: INCH.