

HIP4081A

80V/2.5A Peak, High Frequency Full Bridge FET Driver

FN3659 Rev 8.00 September 15, 2015

The HIP4081A is a high frequency, medium voltage Full Bridge N-Channel FET driver IC, available in 20 lead plastic SOIC and DIP packages. The HIP4081A can drive every possible switch combination except those which would cause a shoot-through condition. The HIP4081A can switch at frequencies up to 1MHz and is well suited to driving Voice Coil Motors, high-frequency switching power amplifiers, and power supplies.

For example, the HIP4081A can drive medium voltage brush motors, and two HIP4081As can be used to drive high performance stepper motors, since the short minimum "on-time" can provide fine micro-stepping capability.

Short propagation delays of approximately 55ns maximizes control loop crossover frequencies and dead-times which can be adjusted to near zero to minimize distortion, resulting in rapid, precise control of the driven load.

A similar part, the HIP4080A, includes an on-chip input comparator to create a PWM signal from an external triangle wave and to facilitate "hysteresis mode" switching.

The Application Note for the HIP4081A is the AN9405.

Ordering Information

PART NUMBER	TEMP RANGE (°C)	PACKAGE	PKG. DWG.#
HIP4081AIP (No longer available, recommended replacement: HIP4081AIPZ)	-40 to 85	20 Ld PDIP	E20.3
HIP4081AIPZ (Note)	-40 to 85	20 Ld PDIP (Pb-free)	E20.3
HIP4081AIB	-40 to 85	20 Ld SOIC (W)	M20.3
HIP4081AIBZ (Note)	-40 to 85	20 Ld SOIC (W) (Pb-free)	M20.3

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which is compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J Std-020B.

Features

- Independently Drives 4 N-Channel FET in Half Bridge or Full Bridge Configurations
- Bootstrap Supply Max Voltage to 95V_{DC}
- Drives 1000pF Load at 1MHz in Free Air at 50°C with Rise and Fall Times of Typically 10ns
- User-Programmable Dead Time
- On-Chip Charge-Pump and Bootstrap Upper Bias Supplies
- DIS (Disable) Overrides Input Control
- Input Logic Thresholds Compatible with 5V to 15V Logic Levels
- Very Low Power Consumption
- · Undervoltage Protection
- · Pb-free Available

Applications

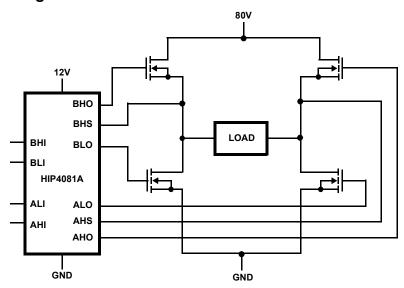
- · Medium/Large Voice Coil Motors
- · Full Bridge Power Supplies
- · Switching Power Amplifiers
- High Performance Motor Controls
- · Noise Cancellation Systems
- · Battery Powered Vehicles
- · Peripherals
- U.P.S.

Pinout

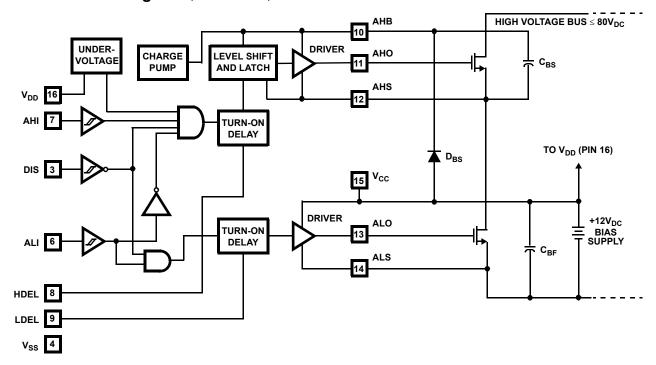
(PDIP, SOIC) TOP VIEW вно внв 11 20 вні **BHS** 19 12 18 DIS BLO v_{ss} 17 BLS BLI 16 V_{DD} ALI 15 v_{cc} ALS ΔНΙ 14 ALO **HDEL** 13 LDEL AHS 12 AHO AHB 11

HIP4081A

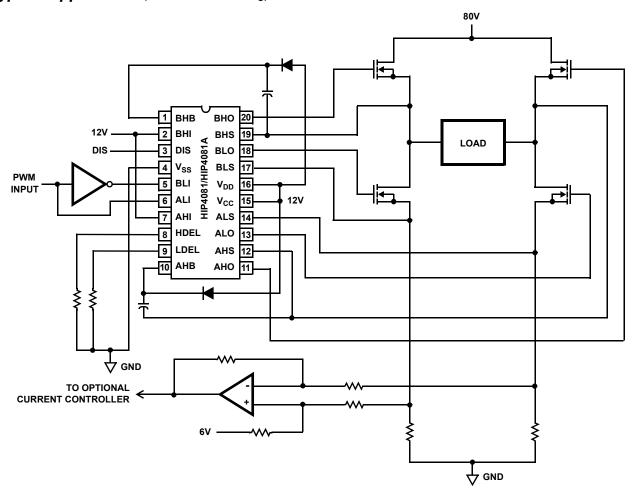
Application Block Diagram



Functional Block Diagram (1/2 HIP4081A)



Typical Application (PWM Mode Switching)



Absolute Maximum Ratings

Thermal Information

Thermal Resistance (Typical, Note 1)	θ _{JA} (°C/W)
SOIC Package	85
DIP Package	
Storage Temperature Range65	
Operating Max. Junction Temperature	125°C
Lead Temperature (Soldering 10s))	300°C
(For SOIC - Lead Tips Only	

Operating Conditions

Supply Voltage, V _{DD} and V _{CC}	+9.5V to +15V
Voltage on ALS, BLS	1.0V to +1.0V
Voltage on AHB, BHB	V _{AHS, BHS} +5V to V _{AHS, BHS} +15V
Input Current, HDEL and LDEL	500μA to -50μA
Operating Ambient Temperature F	Range40°C to 85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

			T _J = 25°C		T _{JS} = -4 12!	0°C TO 5°C			
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	MIN	MAX	UNITS	
SUPPLY CURRENTS AND CHAR	SUPPLY CURRENTS AND CHARGE PUMPS								
V _{DD} Quiescent Current	I _{DD}	All inputs = 0V	8.5	10.5	14.5	7.5	14.5	mA	
V _{DD} Operating Current	I _{DDO}	Outputs switching f = 500kHz	9.5	12.5	15.5	8.5	15.5	mA	
V _{CC} Quiescent Current	Icc	All Inputs = 0V, I _{ALO} = I _{BLO} = 0	-	0.1	10	-	20	μΑ	
V _{CC} Operating Current	I _{cco}	f = 500kHz, No Load	1	1.25	2.0	0.8	3	mA	
AHB, BHB Quiescent Current - Qpump Output Current	I _{AHB} , I _{BHB}	All Inputs = 0V, $I_{AHO} = I_{BHO} = 0$ $V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 10V$	-50	-30	-11	-60	-10	μА	
AHB, BHB Operating Current	I _{AHBO} , I _{BHBO}	f = 500kHz, No Load	0.6	1.2	1.5	0.5	1.9	mA	
AHS, BHS, AHB, BHB Leakage Current	I _{HLK}	$V_{BHS} = V_{AHS} = 80V,$ $V_{AHB} = V_{BHB} = 93V$	-	0.02	1.0	-	10	μΑ	
AHB-AHS, BHB-BHS Qpump Output Voltage	V _{AHB} -V _{AHS} V _{BHB} -V _{BHS}	I _{AHB} = I _{AHB} = 0, No Load	11.5	12.6	14.0	10.5	14.5	V	
INPUT PINS: ALI, BLI, AHI, BHI,	AND DIS								
Low Level Input Voltage	V _{IL}	Full Operating Conditions	-	-	1.0	-	0.8	V	
High Level Input Voltage	V _{IH}	Full Operating Conditions	2.5	-	-	2.7	-	V	
Input Voltage Hysteresis			-	35	-	-	-	mV	
Low Level Input Current	I _{IL}	V _{IN} = 0V, Full Operating Conditions	-130	-100	-75	-135	-65	μΑ	
High Level Input Current	I _{IH}	V _{IN} = 5V, Full Operating Conditions	-1	-	+1	-10	+10	μА	
TURN-ON DELAY PINS: LDEL A	ND HDEL		•				•		
LDEL, HDEL Voltage	V _{HDEL} , V _{LDEL}	$I_{HDEL} = I_{LDEL} = -100 \mu A$	4.9	5.1	5.3	4.8	5.4	V	
GATE DRIVER OUTPUT PINS: A	LO, BLO, AHO,	AND BHO							
Low Level Output Voltage	V _{OL}	I _{OUT} = 100mA	0.7	0.85	1.0	0.5	1.1	V	
High Level Output Voltage	V _{CC} -V _{OH}	I _{OUT} = -100mA	0.8	0.95	1.1	0.5	1.2	V	
Peak Pullup Current	I _O +	V _{OUT} = 0V	1.7	2.6	3.8	1.4	4.1	Α	



			T _J = 25°C		$T_{JS} = -40^{\circ}C \text{ TO}$ $T_{JS} = -40^{\circ}C \text{ TO}$ $125^{\circ}C$				
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	MIN	MAX	UNITS	
Peak Pulldown Current	I ₀ -	V _{O UT} = 12V	1.7	2.4	3.3	1.3	3.6	Α	
Undervoltage, Rising Threshold	UV+		8.1	8.8	9.4	8.0	9.5	V	
Undervoltage, Falling Threshold	UV-		7.6	8.3	8.9	7.5	9.0	V	
Undervoltage, Hysteresis	HYS		0.25	0.4	0.65	0.2	0.7	V	

			T _J = 25°C			T _{JS} = -40°C TO 125°C			
PARAMETER	SYMBOL	TEST CONDITIONS	MIN TYP MAX		MAX	MIN MAX		UNITS	
Lower Turn-off Propagation Delay (ALI-ALO, BLI-BLO)	T _{LPHL}		-	30	60	-	80	ns	
Upper Turn-off Propagation Delay (AHI-AHO, BHI-BHO)	T _{HPHL}		-	35	70	-	90	ns	
Lower Turn-on Propagation Delay (ALI-ALO, BLI-BLO)	T _{LPLH}	R _{HDEL} = R _{LDEL} = 10K	-	45	70	-	90	ns	
Upper Turn-on Propagation Delay (AHI-AHO, BHI-BHO)	T _{HPLH}	R _{HDEL} = R _{LDEL} = 10K	-	60	90	-	110	ns	
Rise Time	T _R		-	10	25	-	35	ns	
Fall Time	T _F		-	10	25	-	35	ns	
Turn-on Input Pulse Width	T _{PWIN-ON}	R _{HDEL} = R _{LDEL} = 10K	50	-	-	50	-	ns	
Turn-off Input Pulse Width	T _{PWIN-OFF}	R _{HDEL} = R _{LDEL} = 10K	40	-	-	40	-	ns	
Turn-on Output Pulse Width	T _{PWOUT-ON}	R _{HDEL} = R _{LDEL} = 10K	40	-	-	40	-	ns	
Turn-off Output Pulse Width	T _{PWOUT-OFF}	R _{HDEL} = R _{LDEL} = 10K	30	-	-	30	-	ns	
Disable Turn-off Propagation Delay (DIS - Lower Outputs)	T _{DISLOW}		-	45	75	-	95	ns	
Disable Turn-off Propagation Delay (DIS - Upper Outputs)	T _{DISHIGH}		-	55	85	-	105	ns	
Disable to Lower Turn-on Propagation Delay (DIS - ALO and BLO)	T _{DLPLH}		-	40	70	-	90	ns	
Refresh Pulse Width (ALO and BLO)	T _{REF-PW}		240	410	550	200	600	ns	
Disable to Upper Enable (DIS - AHO and BHO)	T _{UEN}		-	450	620	-	690	ns	

TRUTH TABLE

	INI	ОИТРИТ			
ALI, BLI	ALI, BLI AHI, BHI U/V DIS			ALO, BLO	АНО, ВНО
X	X	X	1	0	0
1	Х	0	0	1	0
0	1	0	0	0	1
0	0	0	0	0	0
Х	Х	1	Х	0	0

NOTE: X signifies that input can be either a "1" or "0".



Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
1	ВНВ	B High-side Bootstrap supply. External bootstrap diode and capacitor are required. Connect cathode of bootstrap diode and positive side of bootstrap capacitor to this pin. Internal charge pump supplies 30μA out of this pin to maintain bootstrap supply. Internal circuitry clamps the bootstrap supply to approximately 12.8V.
2	ВНІ	B High-side Input. Logic level input that controls BHO driver (Pin 20). BLI (Pin 5) high level input overrides BHI high level input to prevent half-bridge shoot-through, see Truth Table. DIS (Pin 3) high level input overrides BHI high level input. The pin can be driven by signal levels of 0V to 15V (no greater than V_{DD}).
3	DIS	DISable input. Logic level input that when taken high sets all four outputs low. DIS high overrides all other inputs. When DIS is taken low the outputs are controlled by the other inputs. The pin can be driven by signal levels of 0V to $15V$ (no greater than V_{DD}).
4	V_{SS}	Chip negative supply, generally will be ground.
5	BLI	B Low-side Input. Logic level input that controls BLO driver (Pin 18). If BHI (Pin 2) is driven high or not connected externally then BLI controls both BLO and BHO drivers, with dead time set by delay currents at HDEL and LDEL (Pin 8 and 9). DIS (Pin 3) high level input overrides BLI high level input. The pin can be driven by signal levels of 0V to 15V (no greater than V _{DD}).
6	ALI	A Low-side Input. Logic level input that controls ALO driver (Pin 13). If AHI (Pin 7) is driven high or not connected externally then ALI controls both ALO and AHO drivers, with dead time set by delay currents at HDEL and LDEL (Pin 8 and 9). DIS (Pin 3) high level input overrides ALI high level input. The pin can be driven by signal levels of 0V to 15V (no greater than V _{DD}).
7	AHI	A High-side Input. Logic level input that controls AHO driver (Pin 11). ALI (Pin 6) high level input overrides AHI high level input to prevent half-bridge shoot-through, see Truth Table. DIS (Pin 3) high level input overrides AHI high level input. The pin can be driven by signal levels of 0V to 15V (no greater than V _{DD}).
8	HDEL	High-side turn-on DELay. Connect resistor from this pin to V _{SS} to set timing current that defines the turn-on delay of both high-side drivers. The low-side drivers turn-off with no adjustable delay, so the HDEL resistor guarantees no shoot-through by delaying the turn-on of the high-side drivers. HDEL reference voltage is approximately 5.1V.
9	LDEL	Low-side turn-on DELay. Connect resistor from this pin to V _{SS} to set timing current that defines the turn-on delay of both low-side drivers. The high-side drivers turn-off with no adjustable delay, so the LDEL resistor guarantees no shoot-through by delaying the turn-on of the low-side drivers. LDEL reference voltage is approximately 5.1V.
10	AHB	A High-side Bootstrap supply. External bootstrap diode and capacitor are required. Connect cathode of bootstrap diode and positive side of bootstrap capacitor to this pin. Internal charge pump supplies 30µA out of this pin to maintain bootstrap supply. Internal circuitry clamps the bootstrap supply to approximately 12.8V.
11	AHO	A High-side Output. Connect to gate of A High-side power MOSFET.
12	AHS	A High-side Source connection. Connect to source of A High-side power MOSFET. Connect negative side of bootstrap capacitor to this pin.
13	ALO	A Low-side Output. Connect to gate of A Low-side power MOSFET.
14	ALS	A Low-side Source connection. Connect to source of A Low-side power MOSFET.
15	V _{CC}	Positive supply to gate drivers. Must be same potential as V _{DD} (Pin 16). Connect to anodes of two bootstrap diodes.
16	V_{DD}	Positive supply to lower gate drivers. Must be same potential as V _{CC} (Pin 15). De-couple this pin to V _{SS} (Pin 4).
17	BLS	B Low-side Source connection. Connect to source of B Low-side power MOSFET.
18	BLO	B Low-side Output. Connect to gate of B Low-side power MOSFET.
19	BHS	B High-side Source connection. Connect to source of B High-side power MOSFET. Connect negative side of bootstrap capacitor to this pin.
20	вно	B High-side Output. Connect to gate of B High-side power MOSFET.



Timing Diagrams

X = A OR B, A AND B HALVES OF BRIDGE CONTROLLER ARE INDEPENDENT

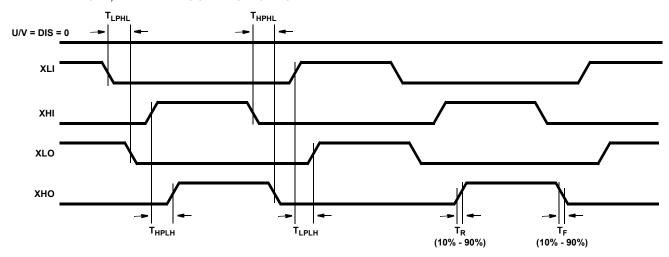


FIGURE 1. INDEPENDENT MODE

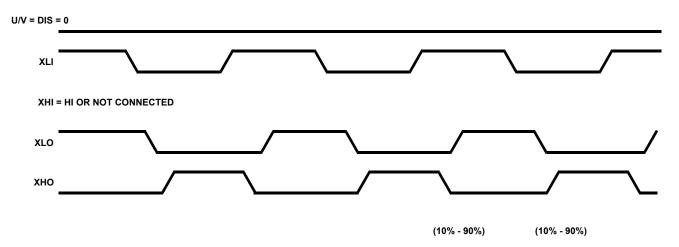


FIGURE 2. BISTATE MODE

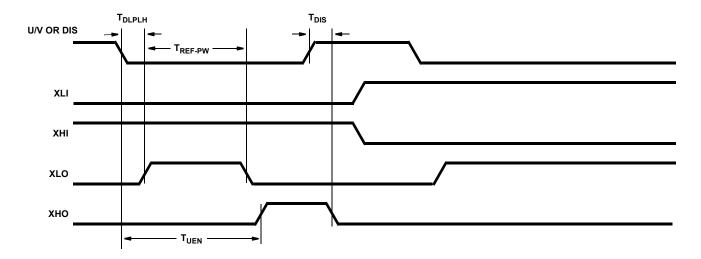


FIGURE 3. DISABLE FUNCTION



Typical Performance Curves $V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = 0V$, $V_{BHS} = 0V$, $V_{BHDEL} = 100K$ and $V_{AHS} = 12V$, $V_{AHS} = 12V$, V

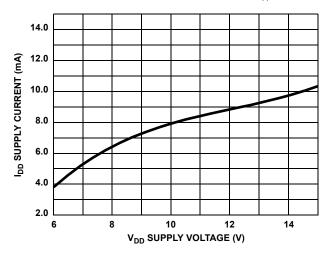


FIGURE 4. QUIESCENT I_{DD} SUPPLY CURRENT vs V_{DD} SUPPLY VOLTAGE

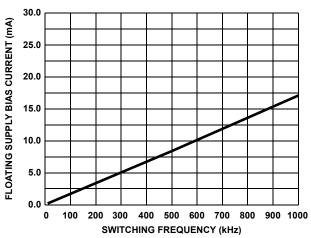


FIGURE 6. SIDE A, B FLOATING SUPPLY BIAS CURRENT vs FREQUENCY (LOAD = 1000pF)

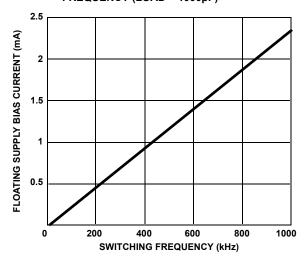


FIGURE 8. I_{AHB} , I_{BHB} , NO-LOAD FLOATING SUPPLY BIAS CURRENT vs FREQUENCY

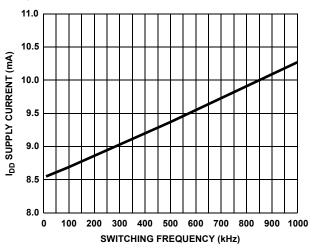


FIGURE 5. I_{DDO} , NO-LOAD I_{DD} SUPPLY CURRENT vs FREQUENCY (kHz)

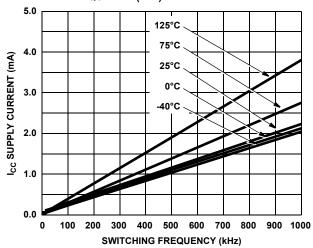


FIGURE 7. I_{CCO} , NO-LOAD I_{CC} SUPPLY CURRENT vs FREQUENCY (kHz) TEMPERATURE

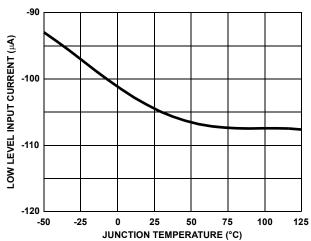


FIGURE 9. ALI, BLI, AHI, BHI LOW LEVEL INPUT CURRENT $I_{\rm IL}$ vs TEMPERATURE

Typical Performance Curves $V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = 0V$, $V_{BHS} = 0V$, $V_{BHS} = 10V$, V_{BHS}

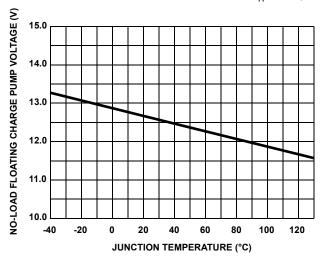


FIGURE 10. AHB - AHS, BHB - BHS NO-LOAD CHARGE PUMP VOLTAGE vs TEMPERATURE

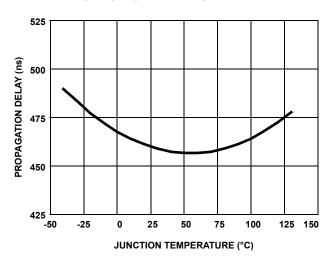


FIGURE 12. DISABLE TO UPPER ENABLE, T_{UEN},
PROPAGATION DELAY vs TEMPERATURE

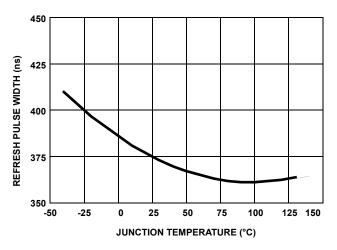


FIGURE 14. T_{REF-PW} REFRESH PULSE WIDTH vs TEMPERATURE

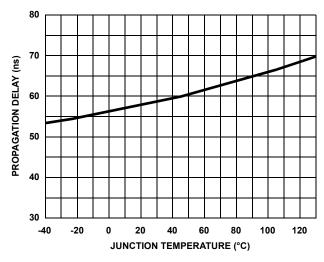


FIGURE 11. UPPER DISABLE TURN-OFF PROPAGATION DELAY T_{DISHIGH} vs TEMPERATURE

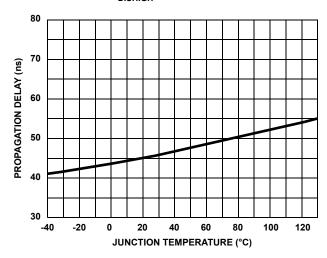


FIGURE 13. LOWER DISABLE TURN-OFF PROPAGATION DELAY $T_{\mbox{\scriptsize DISLOW}}$ vs TEMPERATURE

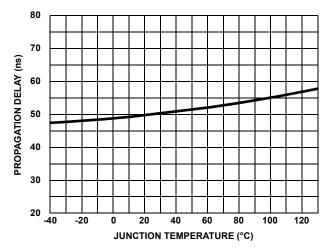


FIGURE 15. DISABLE TO LOWER ENABLE T_{DLPLH}
PROPAGATION DELAY vs TEMPERATURE

Typical Performance Curves $V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V, V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = 0V, R_{HDEL} = R_{LDEL} = 10K$ and $T_A = 25^{\circ}C$, Unless Otherwise Specified (Continued)

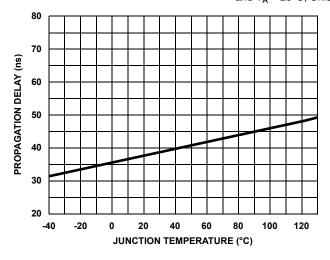


FIGURE 16. UPPER TURN-OFF PROPAGATION DELAY T_{HPHL} vs TEMPERATURE

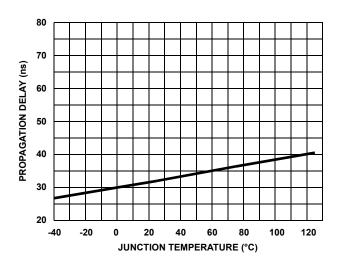


FIGURE 18. LOWER TURN-OFF PROPAGATION DELAY T_{LPHL} vs TEMPERATURE

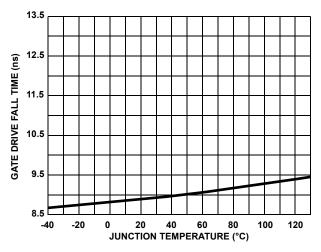


FIGURE 20. GATE DRIVE FALL TIME $T_{\rm F}$ vs TEMPERATURE

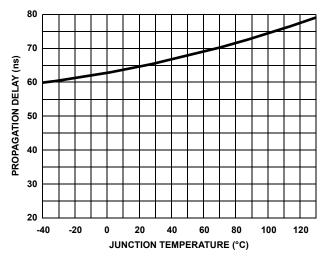


FIGURE 17. UPPER TURN-ON PROPAGATION DELAY $\mathsf{T}_{\mathsf{HPLH}}$ vs $\mathsf{TEMPERATURE}$

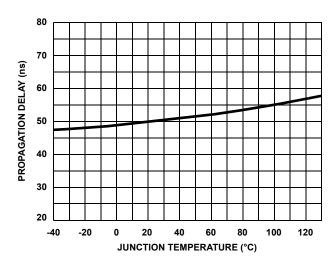


FIGURE 19. LOWER TURN-ON PROPAGATION DELAY T_{LPLH} vs T_{LPLH} vs

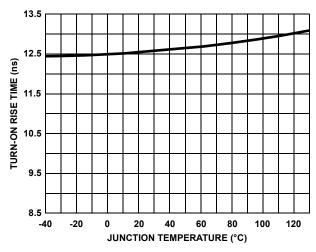


FIGURE 21. GATE DRIVE RISE TIME T_{R} vs TEMPERATURE

Typical Performance Curves $V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = 0V$, $V_{BHS} = 0V$, $V_{BHDEL} = V_{BLDEL} = 100$ K and $V_{AB} = 10$ (Unless Otherwise Specified

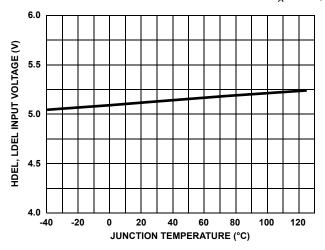


FIGURE 22. V_{LDEL} , V_{HDEL} VOLTAGE vs TEMPERATURE

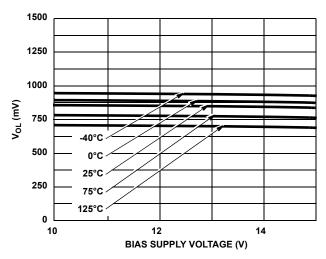


FIGURE 24. LOW LEVEL OUTPUT VOLTAGE V_{OL} vs BIAS SUPPLY AND TEMPERATURE AT 100mA

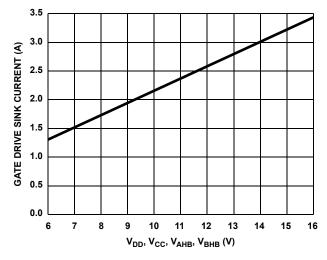


FIGURE 26. PEAK PULLUP CURRENT I_{O+} vs BIAS SUPPLY VOLTAGE

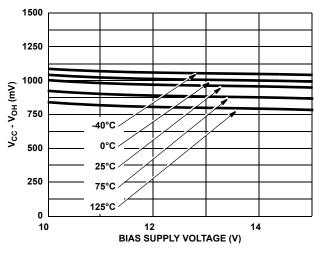


FIGURE 23. HIGH LEVEL OUTPUT VOLTAGE $V_{\rm CC}$ - $V_{\rm OH}$ vs BIAS SUPPLY AND TEMPERATURE AT 100mA

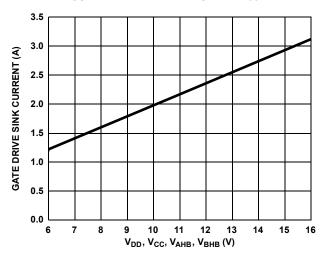


FIGURE 25. PEAK PULLDOWN CURRENT I_O vs BIAS SUPPLY VOLTAGE

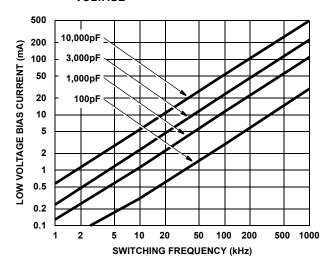


FIGURE 27. LOW VOLTAGE BIAS CURRENT I_{DD} (LESS QUIESCENT COMPONENT) vs FREQUENCY AND GATE LOAD CAPACITANCE



Typical Performance Curves $V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V$, $V_{BHDEL} = V_{BLEL} = 100$ K and $V_{AB} = 10$ (Continued)

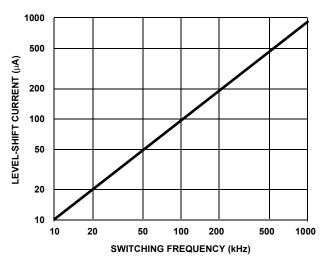
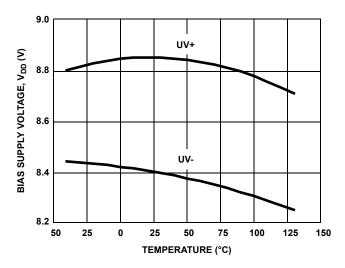


FIGURE 28. HIGH VOLTAGE LEVEL-SHIFT CURRENT VS FREQUENCY AND BUS VOLTAGE





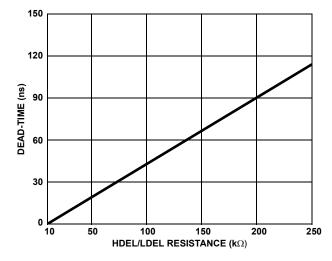


FIGURE 30. MINIMUM DEAD-TIME vs DEL RESISTANCE

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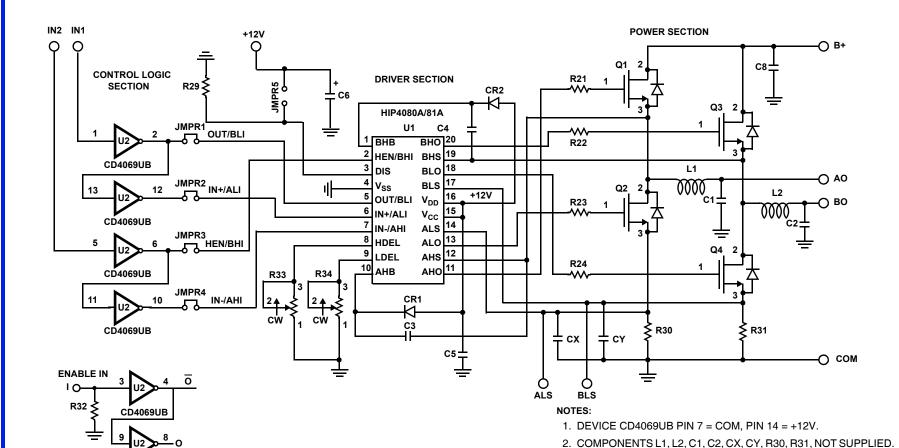


FIGURE 31. HIP4081A EVALUATION PC BOARD SCHEMATIC

REFER TO APPLICATION NOTE FOR DESCRIPTION OF INPUT

LOGIC OPERATION TO DETERMINE JUMPER LOCATIONS FOR

JMPR1 - JMPR4.

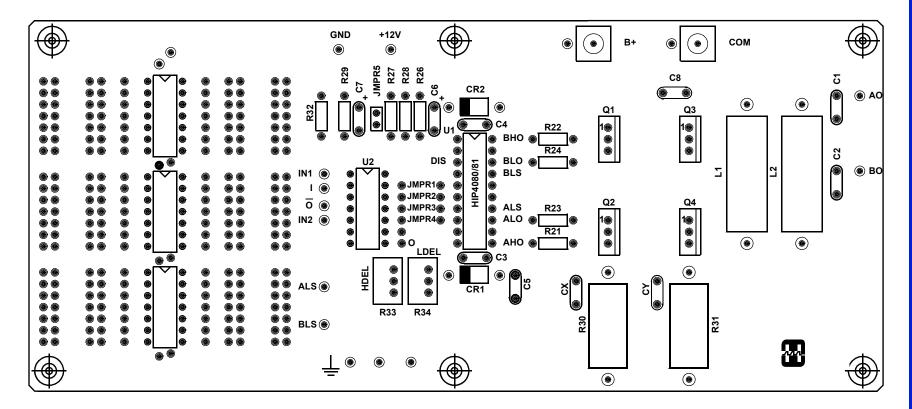


FIGURE 32. HIP4081A EVALUATION BOARD SILKSCREEN

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
September 15, 2015	FN3659.8	Updated Ordering Information Table on page 1. Added Revision History and About Intersil sections. Updated POD M20.3 from rev 1 to rev 3. Changes since rev 1:
		Top View: Corrected "7.50 BSC" to "7.60/7.40" (no change from rev 2; error was introduced in conversion) Changed "10.30 BSC" to "10.65/10.00" (no change from rev 2; error was introduced in conversion) Side View:
		Changed "12.80 BSC" to "13.00/12.60" (no change from rev 2; error was introduced in conversion) Changed "2.65 max" to "2.65/2.35" (no change from rev 2; error was introduced in conversion)
		Changed Note 1 from "ANSI Y14.5M-1982." to "ASME Y14.5M-1994"
		Updated to new POD format by moving dimensions from table onto drawing and adding land pattern

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

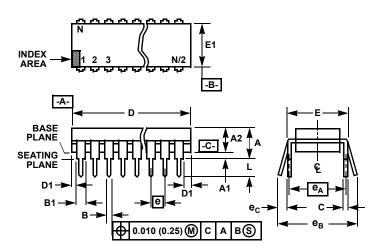
For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support



Dual-In-Line Plastic Packages (PDIP)



NOTES:

- Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
- 2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
- 3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
- 4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
- D, D1, and E1 dimensions do not include mold flash or protrusions.
 Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
- 6. E and $\boxed{e_A}$ are measured with the leads constrained to be perpendicular to datum $\boxed{-C_-}$.
- e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
- 8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
- 9. N is the maximum number of terminal positions.
- Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E20.3 (JEDEC MS-001-AD ISSUE D)
20 LEAD DUAL-IN-LINE PLASTIC PACKAGE

	INC	HES	MILLIM		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
Α	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
В	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.55	1.77	8
С	0.008	0.014	0.204	0.355	-
D	0.980	1.060	24.89	26.9	5
D1	0.005	-	0.13	-	5
Е	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
е	0.100	BSC	2.54	BSC	-
e _A	0.300	BSC	7.62	BSC	6
e _B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	2	0	2	9	

Rev. 0 12/93

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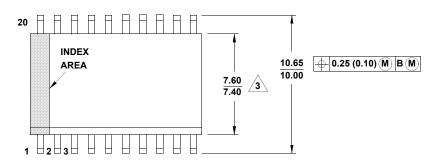
For information regarding Intersil Corporation and its products, see www.intersil.com



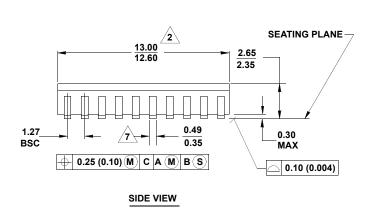
Package Outline Drawing

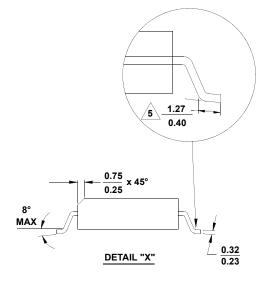
M20.3

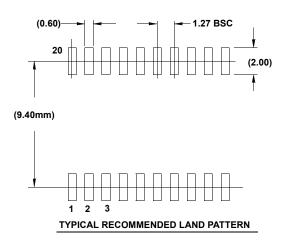
20 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE (SOIC) Rev 3, 2/11



TOP VIEW







NOTES:

- 1. Dimensioning and tolerancing per ASME Y14.5M-1994.
- 2. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
- 3. Dimension does not include interlead lash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
- 4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
- 5. Dimension is the length of terminal for soldering to a substrate.
- 6. Terminal numbers are shown for reference only.
- 7. The lead width as measured 0.36mm (0.14 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
- 8. Controlling dimension: MILLIMETER.
- 9. Dimensions in () for reference only.
- 10. JEDEC reference drawing number: MS-013-AC.