HS-1145RH

Radiation Hardened, High Speed, Low Power, Current Feedback Video Operational Amplifier with Output Disable

The HS-1145RH is a high speed, low power current feedback amplifier built with the Renesas proprietary complementary bipolar UHF-1 (DI bonded wafer) process. These devices are QML approved and are processed and screened in full compliance with MIL-PRF-38535.

This amplifier features a TTL/CMOS compatible disable control, pin 8, which when pulled low, reduces the supply current and forces the output into a high impedance state. This allows easy implementation of simple, low power video switching and routing systems. Component and composite video systems also benefit from this op amp's excellent gain flatness, and good differential gain and phase specifications. Multiplexed A/D applications will also find the HS-1145RH useful as the A/D driver/multiplexer.

Features

- Electrically Screened to SMD # 5962-96830
- QML Qualified per MIL-PRF-38535 Requirements
- Low Supply Current: 5.9mA (Typ)
- Wide -3dB Bandwidth: 360MHz (Typ)
- High Slew Rate: 1000V/µs (Typ)
- Excellent Gain Flatness (to 50MHz): ±0.07dB (Typ)
- Excellent Differential Gain: 0.02% (Typ)
- Excellent Differential Phase: 0.03 Degrees (Typ)
- High Output Current: 60mA (Typ)
- Output Enable/Disable Time: 180ns/35ns (Typ)
- TID Rad Hard Assurance (RHA) testing
  - HDR (50-300rad(Si)/s): 300krad(Si)
- Latch Up: None (DI Technology)

Applications

- Multiplexed Flash A/D Driver
- RGB Multiplexers/Preamps
- Video Switching and Routing
- Pulse and Video Amplifiers
- Wideband Amplifiers
- RF/IF Signal Processing
- Imaging Systems

Contents

1. Pin Information

1.1 Pin Assignments

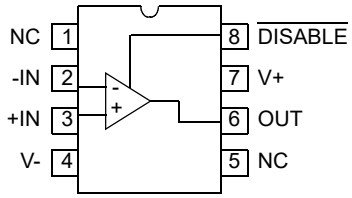


Figure 1. Pin Assignments - Top View

1.2 Pin Descriptions

Pin Number	Pin Name	Description
1, 5	NC	No Connect
2	-IN	Inverting input
3	+IN	Non-inverting input
4	V-	Negative power supply
6	OUT	Amplifier output
7	V+	Positive power supply
8	$\overline{\text{DISABLE}}$	Disable control pin. HIGH = Amplifier enable, LOW = Reduces amplifier supply current and puts the amplifier output in a high-impedance state.

2. Application Information

2.1 Optimum Feedback Resistor

Although a current feedback amplifier's bandwidth dependency on closed loop gain isn't as severe as that of a voltage feedback amplifier, there can be an appreciable decrease in bandwidth at higher gains. This decrease may be minimized by taking advantage of the current feedback amplifier's unique relationship between bandwidth and R_F. All current feedback amplifiers require a feedback resistor, even for unity gain applications, and R_F, in conjunction with the internal compensation capacitor, sets the dominant pole of the frequency response. Therfore, the amplifier's bandwidth is inversely proportional to R_F. The HS-1145RH design is optimized for R_F = 510Ω at a gain of +2. Decreasing R_F decreases stability, resulting in excessive peaking and overshoot (Note: Capacitive feedback will cause the same problems due to the feedback impedance decrease at higher frequencies). At higher gains, however, the amplifier is more stable so R_F can be decreased in a trade-off of stability for bandwidth.

Table 1 lists recommended R_F values for various gains, and the expected bandwidth. For a gain of +1, a resistor ($+R_S$) in series with +IN is required to reduce gain peaking and increase stability.

Table 1. Recommended RF values for Various Gains

Gain (A_{CL})	R_F (Ω)	Bandwidth (MHz)
-1	425	300
+1	510 ($+R_S$ = 510Ω)	270
+2	510	330
+5	200	300
+10	180	130

2.2 Non-Inverting Input Source Impedance

For best operation, the DC source impedance seen by the non-inverting input should be ≥50Ω. This is especially important in inverting gain configurations where the non-inverting input would normally be connected directly to GND.

2.3 $\overline{\text{DISABLE}}$ Input TTL Compatibility

The HS-1145RH derives an internal GND reference for the digital circuitry as long as the power supplies are symmetrical about GND. With symmetrical supplies the digital switching threshold ($V_{TH} = (V_{IH} + V_{IL})/2 = (2.0 + 0.8)/2$) is 1.4V, which ensures the TTL compatibility of the $\overline{\text{DISABLE}}$ input. If asymmetrical supplies (such as +10V, 0V) are used, the switching threshold becomes:

(EQ. 1) $$V_{TH} = \frac{V+ + V-}{2} + 1.4V$$

and the V_{IH} and V_{IL} levels are V_{TH} ±0.6V, respectively.

2.4 Optional GND Pad (Die Use Only) for TTL Compatibility

The die version of the HS-1145RH provides the user with a GND pad for setting the disable circuitry GND reference. With symmetrical supplies the GND pad may be left unconnected, or tied directly to GND. If asymmetrical supplies (such as +10V, 0V) are used, and TTL compatibility is desired, die users must connect the GND pad to GND. With an external GND, the $\overline{\text{DISABLE}}$ input is TTL compatible regardless of supply voltage used.

2.5 Pulse Undershoot and Asymmetrical Slew Rates

The HS-1145RH utilizes a quasi-complementary output stage to achieve high output current while minimizing quiescent supply current. In this approach, a composite device replaces the traditional PNP pull-down transistor. The composite device switches modes after crossing 0V, resulting in added distortion for signals swinging below ground, and an increased undershoot on the negative portion of the output waveform (See Figure 6, Figure 9, and Figure 12). This undershoot is not present for small bipolar signals, or large positive signals. Another artifact of the composite device is asymmetrical slew rates for output signals with a negative voltage component. The slew rate degrades as the output signal crosses through 0V (See Figure 6, Figure 9, and Figure 12), resulting in a slower overall negative slew rate. Positive only signals have symmetrical slew rates as illustrated in the large signal positive pulse response graphs (See Figure 5, Figure 8, and Figure 11).

2.6 Driving Capacitive Loads

Capacitive loads, such as an A/D input, or an improperly terminated transmission line will degrade the amplifier's phase margin resulting in frequency response peaking and possible oscillations. In most cases, the oscillation can be avoided by placing a resistor (R_S) in series with the output prior to the capacitance.

Figure 2 details starting points for the selection of this resistor. The points on the curve indicate the R_S and C_L combinations for the optimum bandwidth, stability, and settling time, but experimental fine tuning is recommended. Picking a point above or to the right of the curve yields an over-damped response, while points below or left of the curve indicate areas of under-damped performance.

R_S and C_L form a low pass network at the output, thus limiting system bandwidth well below the amplifier bandwidth of 270MHz (for A_V = +1). By decreasing R_S as C_L increases (as illustrated in the curves), the maximum bandwidth is obtained without sacrificing stability. In spite of this, the bandwidth decreases as the load capacitance increases. For example, at A_V = +1, R_S = 62Ω, C_L = 40pF, the overall bandwidth is limited to 180MHz, and bandwidth drops to 75MHz at A_V = +1, R_S = 8Ω, C_L = 400pF.

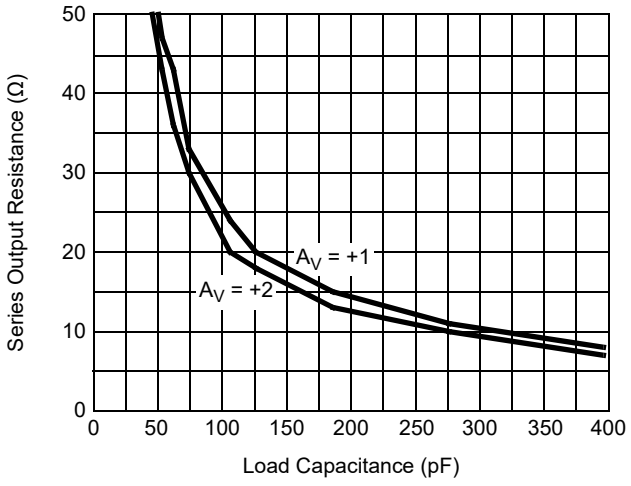


Figure 2. Recommended Series Output Resistor vs Load Capacitance

3. PC Board Layout

This amplifier's frequency response depends greatly on the care taken in designing the PC board.

IMPORTANT: The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!

Attention should be given to decoupling the power supplies. A large value (10µF) tantalum in parallel with a small value (0.1µF) chip capacitor works well in most cases.

Terminated micro-strip signal lines are recommended at the device's input and output connections. Capacitance, parasitic or planned, connected to the output must be minimized, or isolated as discussed in the next section.

Care must also be taken to minimize the capacitance to ground at the amplifier's inverting input (-IN), as this capacitance causes gain peaking, pulse overshoot, and if large enough, instability. To reduce this capacitance, the designer should remove the ground plane under traces connected to -IN, and keep connections to -IN as short as possible.

An example of a good high frequency layout is shown in Figure 3.

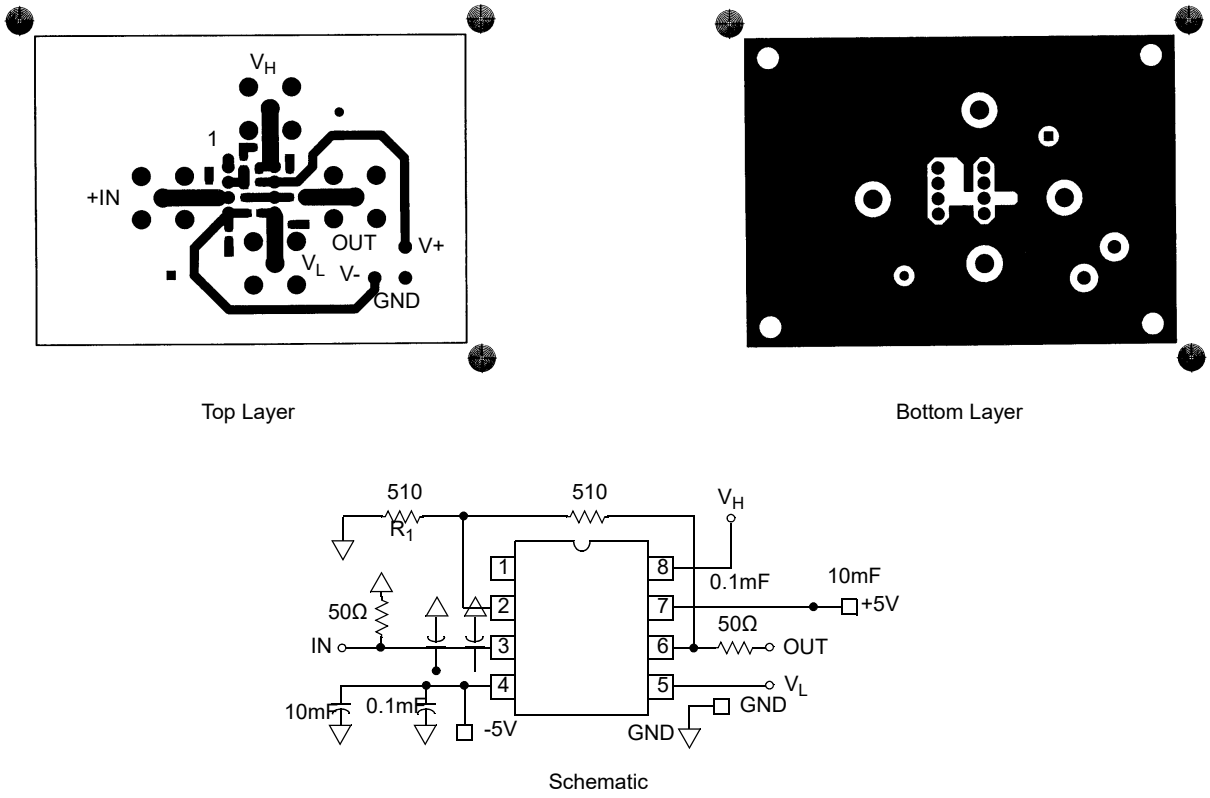


Figure 3. Evaluation Board Schematic and Layout

4. Typical Performance Curves

V_{SUPPLY} = ±5V, R_F = 510Ω, T_A = 25°C, R_L = 100Ω, Unless Otherwise Specified

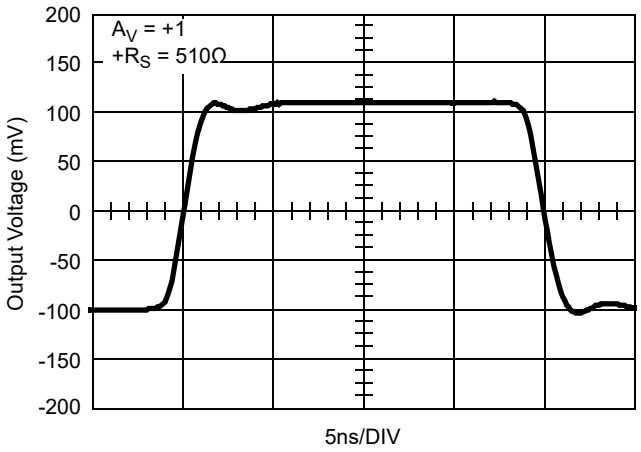


Figure 4. Small Signal Pulse Response

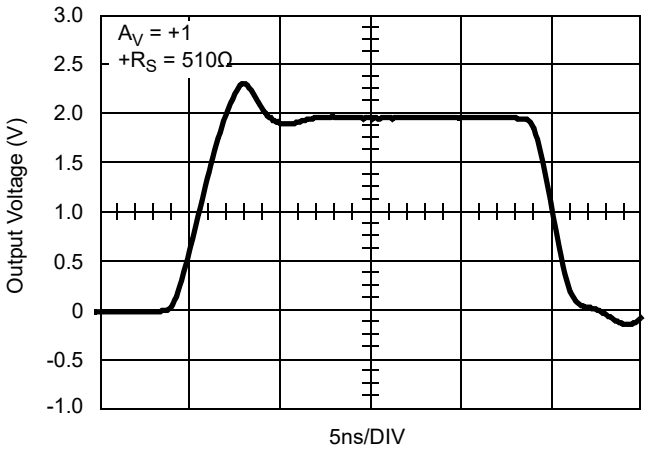


Figure 5. Large Signal Positive Pulse Response

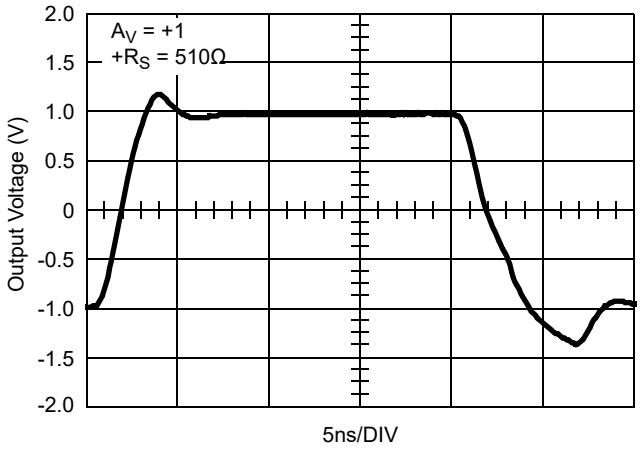


Figure 6. Large Signal Bipolar Pulse Response

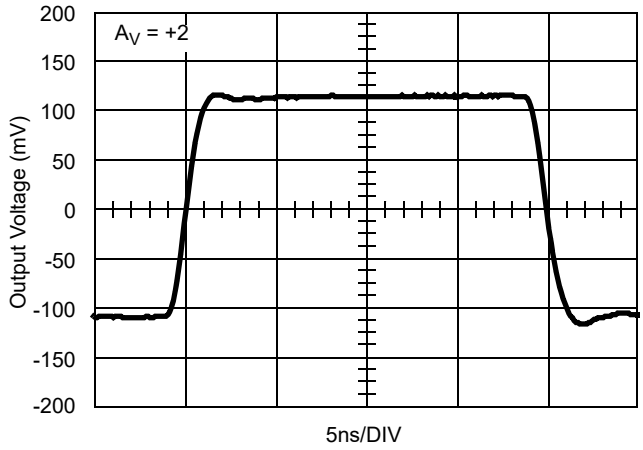


Figure 7. Small Signal Pulse Response

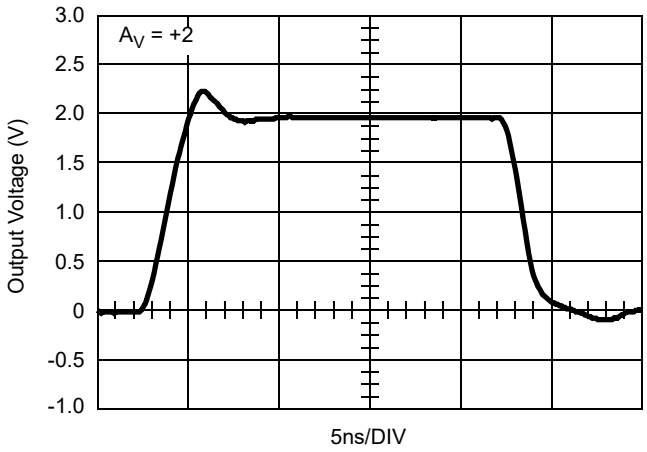


Figure 8. Large Signal Positive Pulse Response

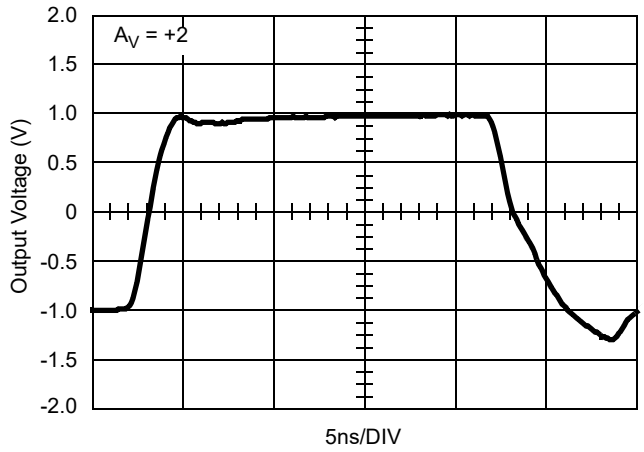


Figure 9. Large Signal Bipolar Pulse Response

V_{SUPPLY} = ±5V, R_F = 510Ω, T_A = 25°C, R_L = 100Ω, Unless Otherwise Specified (Cont.)

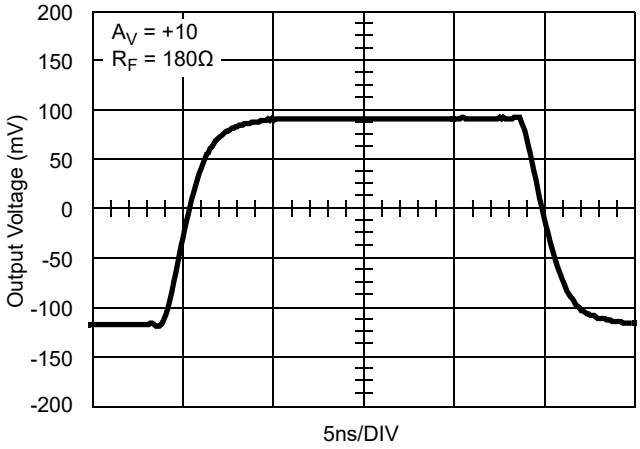


Figure 10. Small Signal Pulse Response

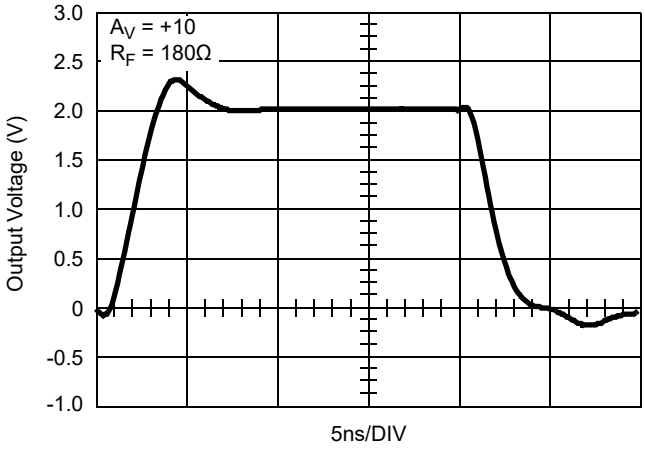


Figure 11. Large Signal Positive Pulse Response

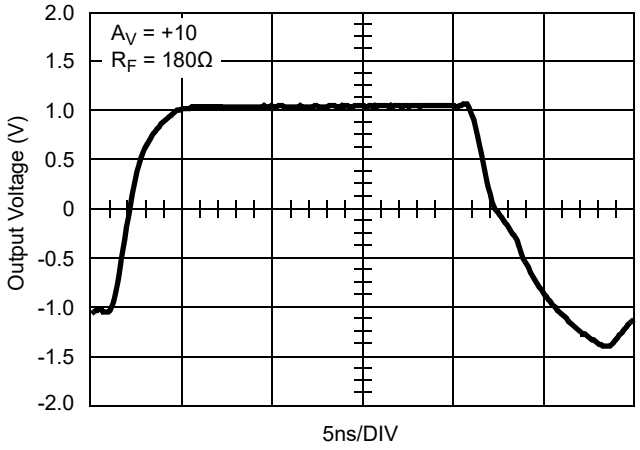


Figure 12. Large Signal Bipolar Pulse Response

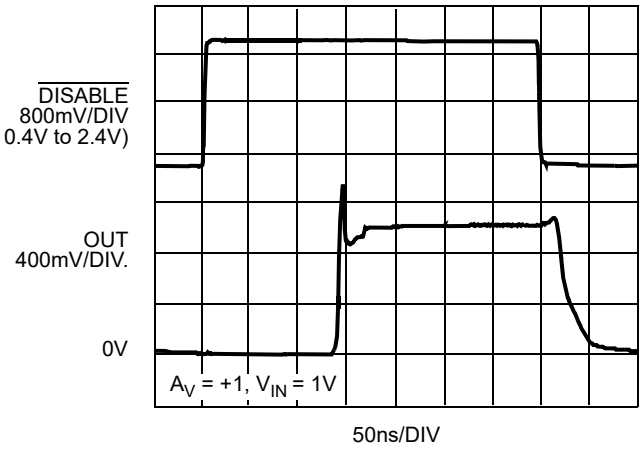


Figure 13. Output Enable and Disable Response

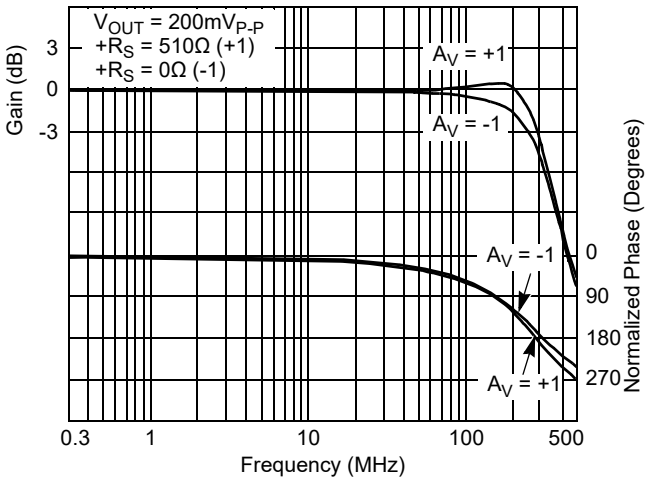


Figure 14. Frequency Response

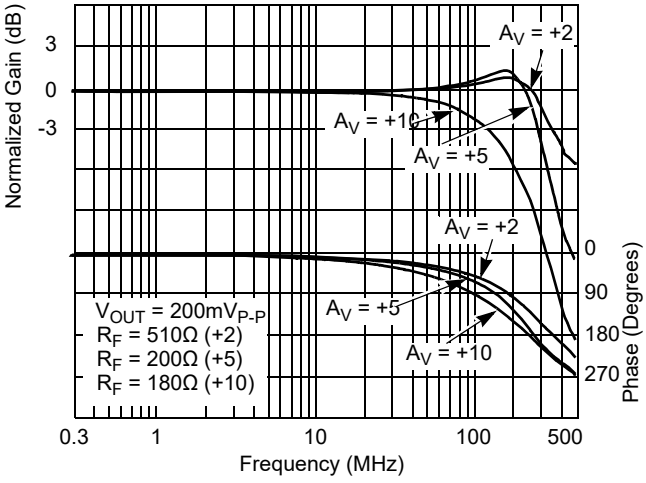


Figure 15. Frequency Response

V_{SUPPLY} = ±5V, R_F = 510Ω, T_A = 25°C, R_L = 100Ω, Unless Otherwise Specified (Cont.)

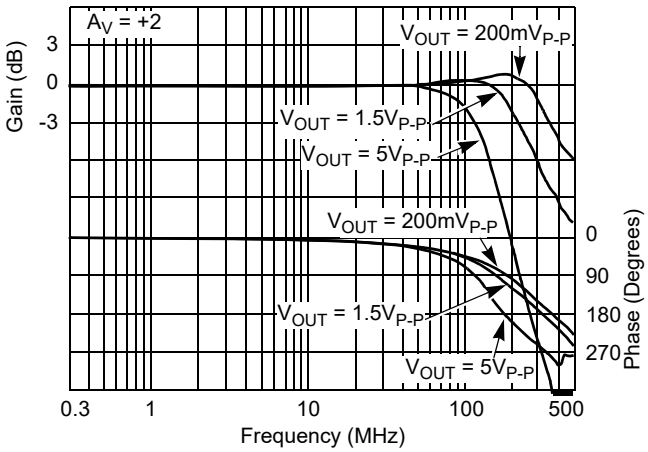


Figure 16. Frequency Response for Various Output Voltages

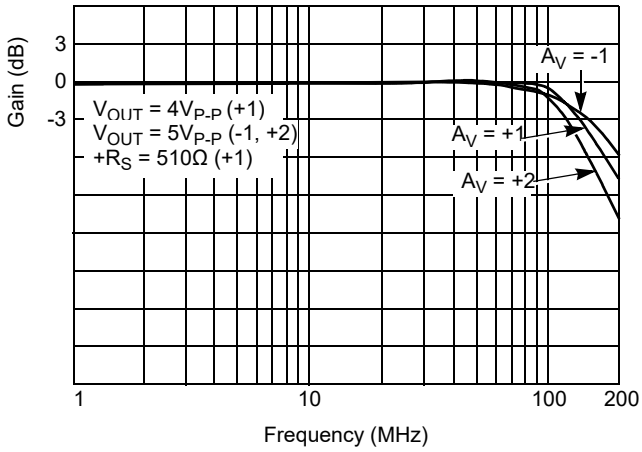


Figure 17. Full Power Bandwidth

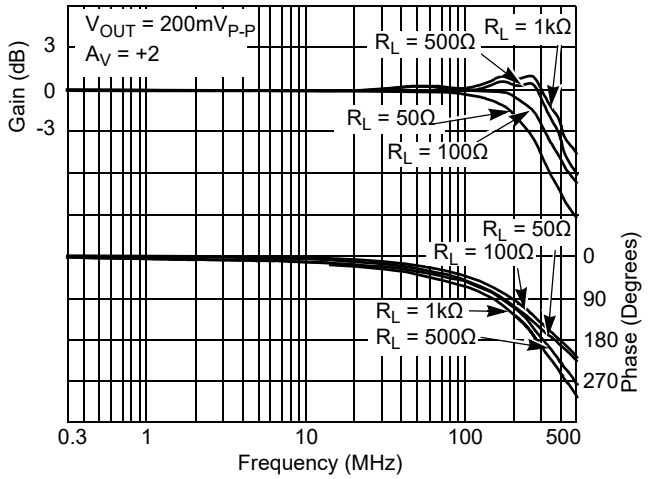


Figure 18. Frequency Response for Various Load Resistors

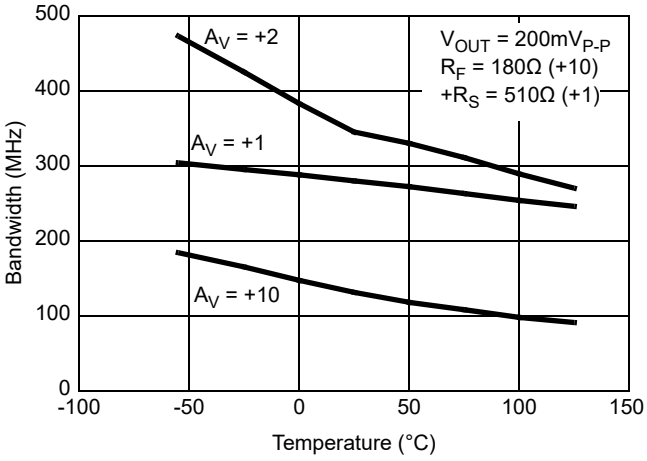


Figure 19. -3dB Bandwidth vs Temperature

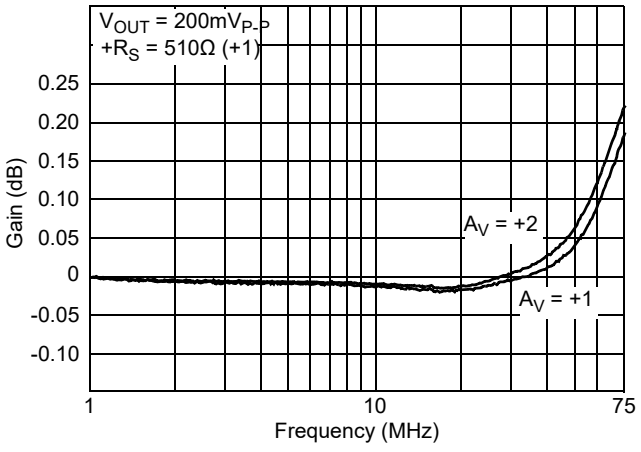


Figure 20. Gain Flatness

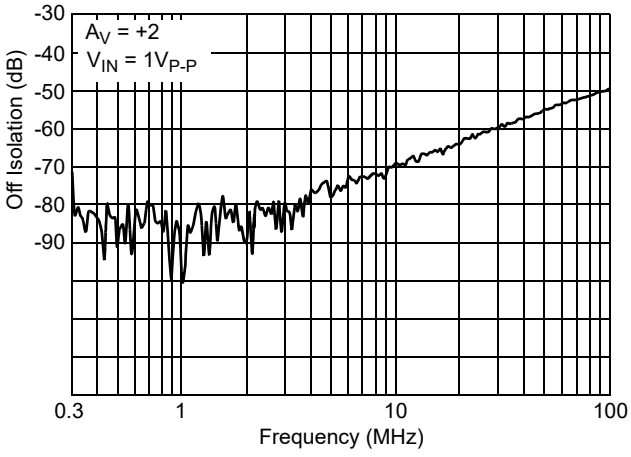


Figure 21. Off Isolation

V_{SUPPLY} = ±5V, R_F = 510Ω, T_A = 25°C, R_L = 100Ω, Unless Otherwise Specified (Cont.)

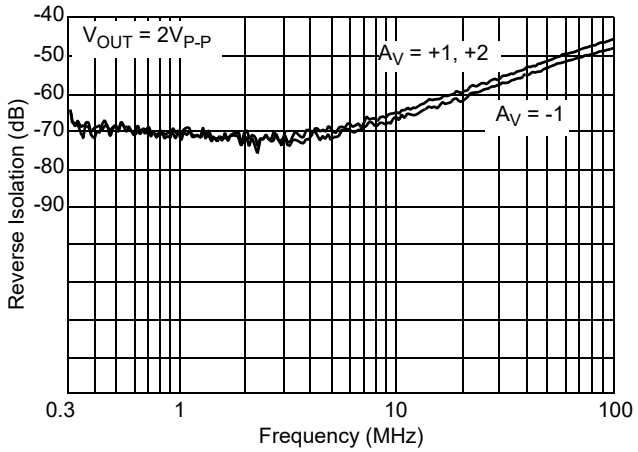


Figure 22. Reverse Isolation

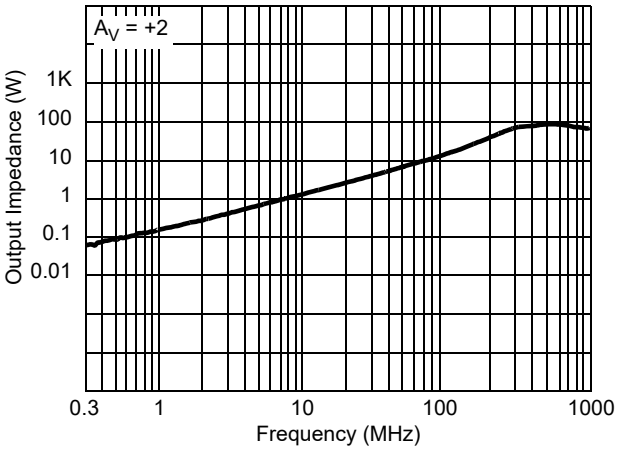


Figure 23. Enabled Output Impedance

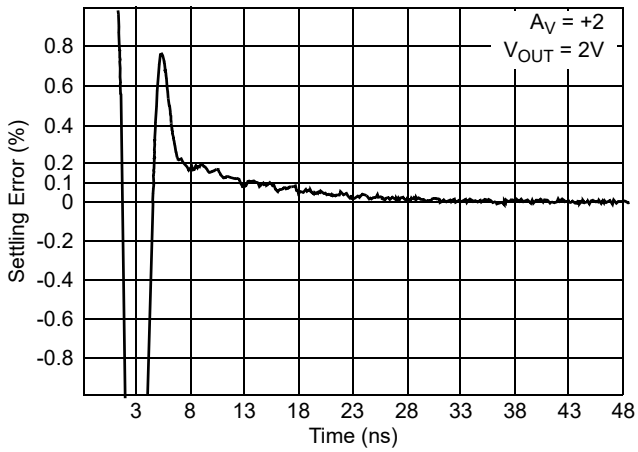


Figure 24. Settling Response

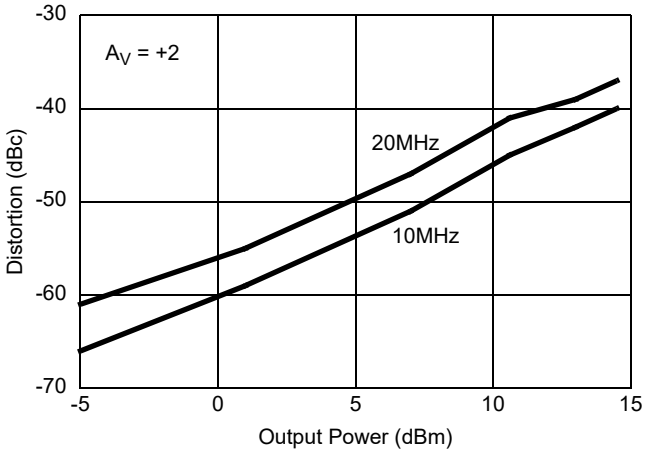


Figure 25. Second Harmonic Distortion vs P_{OUT}

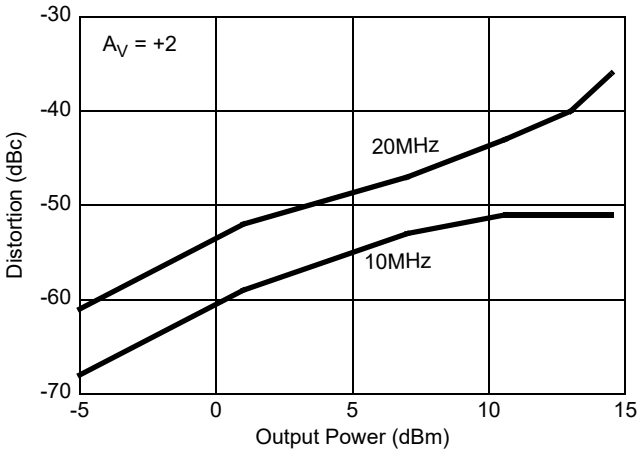


Figure 26. Third Harmonic Distortion vs P_{OUT}

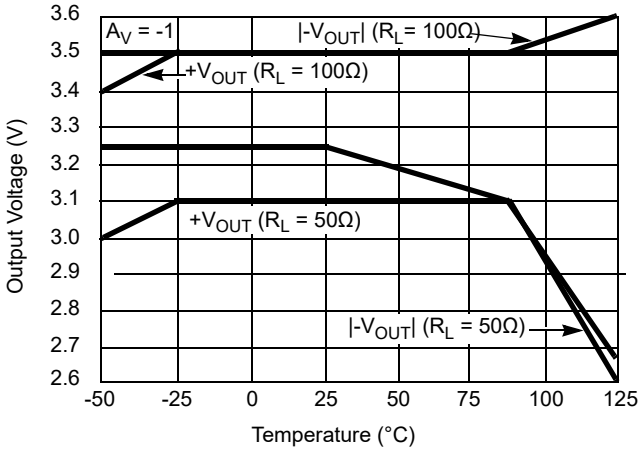


Figure 27. Output Voltage vs Temperature

V_{SUPPLY} = ±5V, R_F = 510Ω, T_A = 25°C, R_L = 100Ω, Unless Otherwise Specified (Cont.)

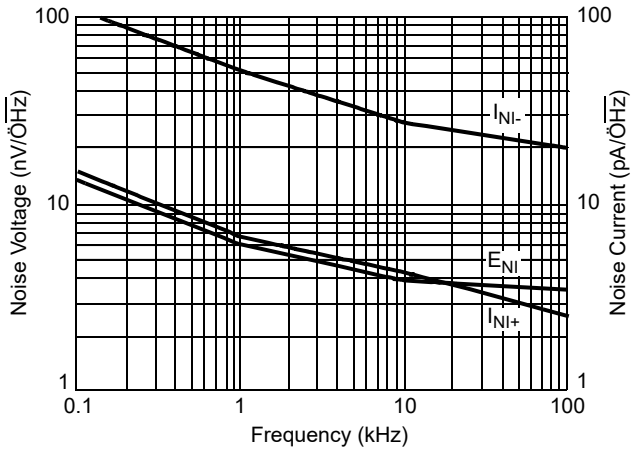


Figure 28. Input Noise Characteristics

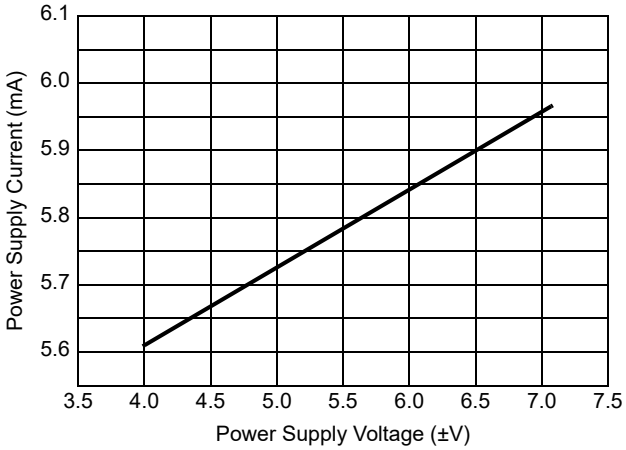
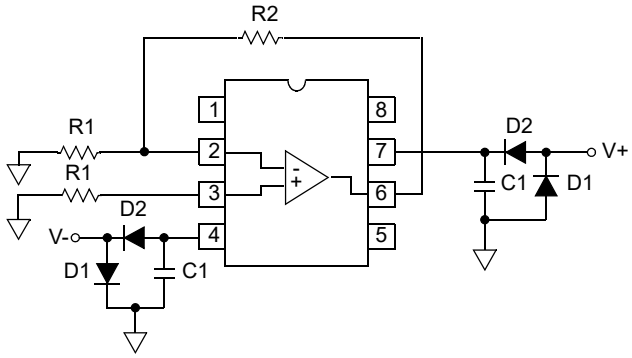


Figure 29. Supply Current vs Supply Voltage

5. Burn-In Circuit

HS-1145RH CERDIP

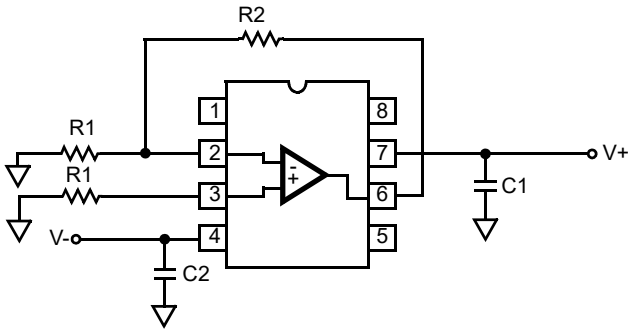


Notes:

- R1 = 1kΩ, ±5% (Per Socket)
- R2 = 10kΩ, ±5% (Per Socket)
- C1 = 0.01µF (Per Socket) or 0.1µF (Per Row) Minimum
- D1 = 1N4002 or Equivalent (Per Board)
- D2 = 1N4002 or Equivalent (Per Socket)
- V+ = +5.5V ±0.5V
- V- = -5.5V ±0.5V

6. Irradiation Circuit

HS-1145RH CERDIP



Notes:

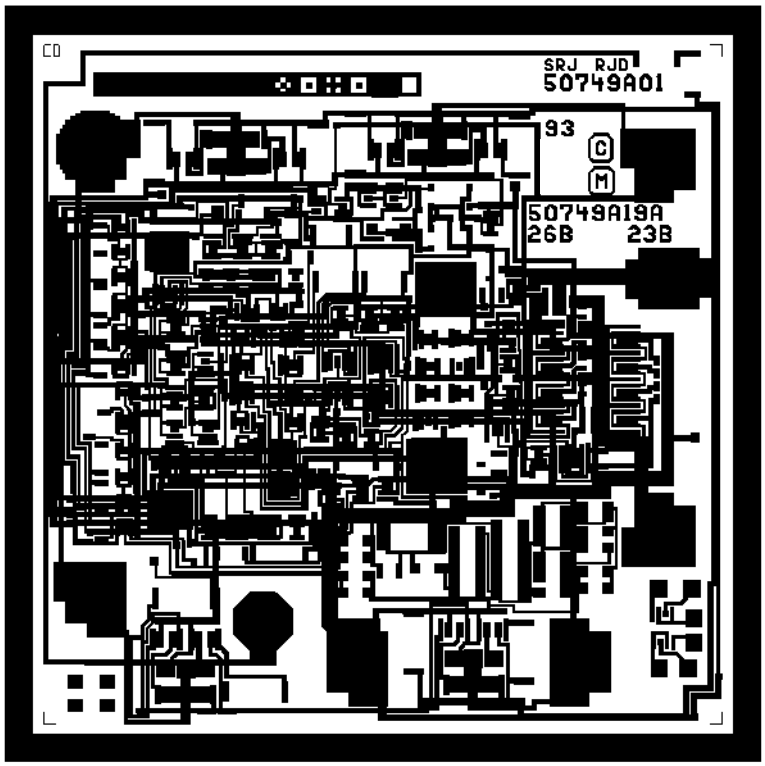
- R1 = 1kΩ, ±5%
- R2 = 10kΩ, ±5%
- C1 = C2 = 0.01µF
- V+ = +5.0V ±0.5V
- V- = -5.0V ±0.5V

7. Die and Assembly Characteristics

Table 2. Die and Assembly Related Information

Die Information	
Dimension	59 mils×59 mils×14 mils ±1 mil (1500µm×1500µm ×483µm ±25.4µm)
Interface Materials	
Glassivation	Type: Nitride Thickness: 4kÅ ±0.5kÅ
Top Metallization	Type: Metal 1: AlCu(2%)/TiW Thickness: Metal 1: 8kÅ ±0.4kÅ Type: Metal 2: AlCu(2%) Thickness: Metal 2: 16kÅ ±0.8kÅ
Substrate	UHF-1, Bonded Wafer, DI
Assembly Information	
Substrate Potential	Floating (Recommend Connection to V-)
Additional Information	
Transistor Count	75

7.1 Metallization Mask Layout



Note: This pad is not bonded out on packaged units. Die users may set a GND reference, using this pad, to ensure the TTL compatibility of the $\overline{DIS}$ input when using asymmetrical supplies (such as V+ = 10V, V- = 0V). See the Application Information section for details.

8. Ordering Information

SMD Ordering Number[1]	Internal Part Number[2]	Radiation Hardness (Total Ionizing Dose)	Package Description (RoHS Compliant)	Package Drawing	Carrier Type	Temp. Range
5962F9683001VPC	HS7B-1145RH-Q	HDR to 300krad(Si)	8 Lead Ceramic Dual-In-Line Metal Seal Package	D8.3	Tray	-55 to 125°C
N/A	HS7B-1145RH/PROTO[3]	N/A				

1. SMD Ordering Note - Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed must be used when ordering.
2. These Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
3. The /PROTO part is not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. This part is intended for engineering evaluation purposes only. The /PROTO part meets the electrical limits and conditions across temperature specified in the DLA SMD and are in the same form and fit as the qualified device. This part type does not come with a Certificate of Conformance because they are not DLA qualified devices.

9. Revision History

Revision	Date	Description
3.00	May 1, 2024	Placed in the latest template. Updated Feature bullet. Added Pin Description table. Updated Ordering Information table. Updated PC Board Layout section. Added Revision history section.

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Contact Information

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