# HS-139RH, HS-139EH

Radiation Hardened Quad Voltage Comparator

The Radiation Hardened HS-139RH, HS-139EH consists of four independent single or dual supply voltage comparators on a single monolithic substrate. The common mode input voltage range includes ground, even when operated from a single supply and the low supply current makes these comparators suitable for low power applications. These types were designed to directly interface with TTL and CMOS.

The HS-139RH, HS-139EH are fabricated on our dielectrically isolated Rad Hard Silicon Gate (RSG) process, which provides an immunity to Single Event Latch-up and the capability of highly reliable performance in any radiation environment.

**Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed below must be used when ordering.**

**Detailed Electrical Specifications for the HS-139RH, HS-139EH are contained in SMD 5962-98613. A "hot-link" is provided on our homepage with instructions for downloading.**

## Features

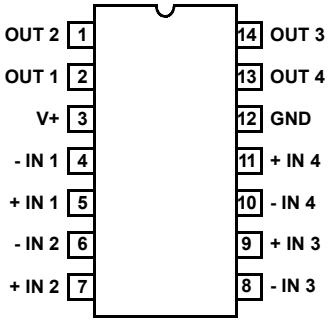
- QML qualified per MIL-PRF-38535 requirements
- Radiation environment
  - Latch-up free under any conditions
  - Total dose (Max). . . . . $3 \times 10^5$ RAD(Si)
  - SEU LET threshold . . . . . 20MeV/$cm^2$/mg
  - Low dose rate effects immunity
- 100V output voltage withstand capability
- ESD protection to >3000V
- Differential input voltage range equal to the supply voltage
- Input offset voltage ($V_{IO}$). . . . . 2mV (Max)
- Quiescent supply current . . . . . 2mA (Max)
- Pb-Free (RoHS Compliant)

## Applications

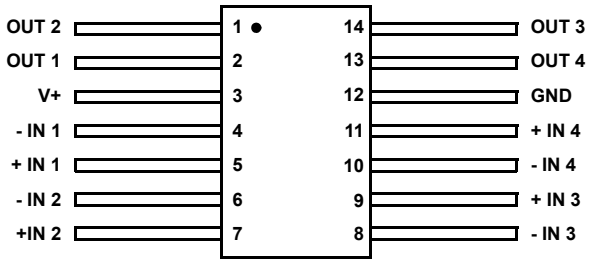
- Pulse generators
- Timing circuitry
- Level shifting
- Analog-to-digital conversion

## Pin Configurations

HS-139RH, HS-139EH
(SBDIP CDIP2-T14)
TOP VIEW




HS-139RH, HS-139EH
(FLATPACK CDFP3-F14)
TOP VIEW



# Ordering Information

| ORDERING SMD NUMBER (Note 1) | PART NUMBER (Note 2) | PACKAGE DESCRIPTION (RoHS Compliant) | PKG. DWG. # | CARRIER TYPE | TEMP. RANGE (°C) |
|---|---|---|---|---|---|
| 5962F9861303VCC | HS1-139EH-Q | 14 Ld SBDIP | D14.3 | Tube | -55 to +125 |
| 5962F9861301VCC | HS1-139RH-Q | 14 Ld SBDIP | D14.3 | Tube | -55 to +125 |
| 5962F9861301QCC | HS1-139RH-8 | 14 Ld SBDIP | D14.3 | Tube | -55 to +125 |
| HS1-139RH/PROTO (Note 3) | HS1-139RH/PROTO | 14 Ld SBDIP | D14.3 | Tube | -55 to +125 |
| 5962F9861301VXC | HS9-139RH-Q | 14 Ld FLATPACK | K14.A | Tray | -55 to +125 |
| 5962F9861301QXC | HS9-139RH-8 | 14 Ld FLATPACK | K14.A | Tray | -55 to +125 |
| 5962F9861303VXC | HS9-139EH-Q | 14 Ld FLATPACK | K14.A | Tray | -55 to +125 |
| HS9-139RH/PROTO (Note 3) | HS9-139RH/PROTO | 14 Ld FLATPACK | K14.A | Tray | -55 to +125 |
| 5962F9861303V9A (Note 4) | HS0-139EH-Q | Die | N/A | N/A | -55 to +125 |
| 5962F9861301V9A (Note 4) | HS0-139RH-Q | Die | N/A | N/A | -55 to +125 |
| HS0-139RH/SAMPLE (Notes 3, 4) | HS0-139RH/SAMPLE | Die | N/A | N/A | -55 to +125 |

NOTES:

1. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed in the table must be used when ordering.
2. These Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
3. The /PROTO and /SAMPLE are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions across temperature specified in the DLA SMD and are in the same form and fit as the qualified device. The /SAMPLE parts are capable of meeting the electrical limits and conditions specified in the DLA SMD. The /SAMPLE parts do not receive 100% screening across temperature to the DLA SMD electrical limits. These part types do not come with a Certificate of Conformance because they are not DLA qualified devices.
4. Die product tested at $T_A$ = + 25°C. The wafer probe test includes functional and parametric testing sufficient to make the die capable of meeting the electrical performance outlined in SMD.

# Die Characteristics

**DIE DIMENSIONS:**

3750µm x 2820µm (148 mils x 111 mils)
483µm ±25.4µm (19 mils ±1 mil)

**INTERFACE MATERIALS:**

**Glassivation:**

Type: Silox ($SiO_2$)
Thickness: 8.0kÅ ±1.0kÅ

**Top Metallization:**

Type: AlSiCu
Thickness: 16.0kÅ ±2kÅ

**Substrate:**

Radiation Hardened Silicon Gate, Dielectric Isolation

**Backside Finish:**

Silicon

**ASSEMBLY RELATED INFORMATION:**

**Substrate Potential:**

Unbiased (DI)

**ADDITIONAL INFORMATION:**

**Worst Case Current Density:**

<2.0 x $10^5$ A/$cm^2$

**Transistor Count:**

49

# Metallization Mask Layout

**HS-139RH, HS-139EH**

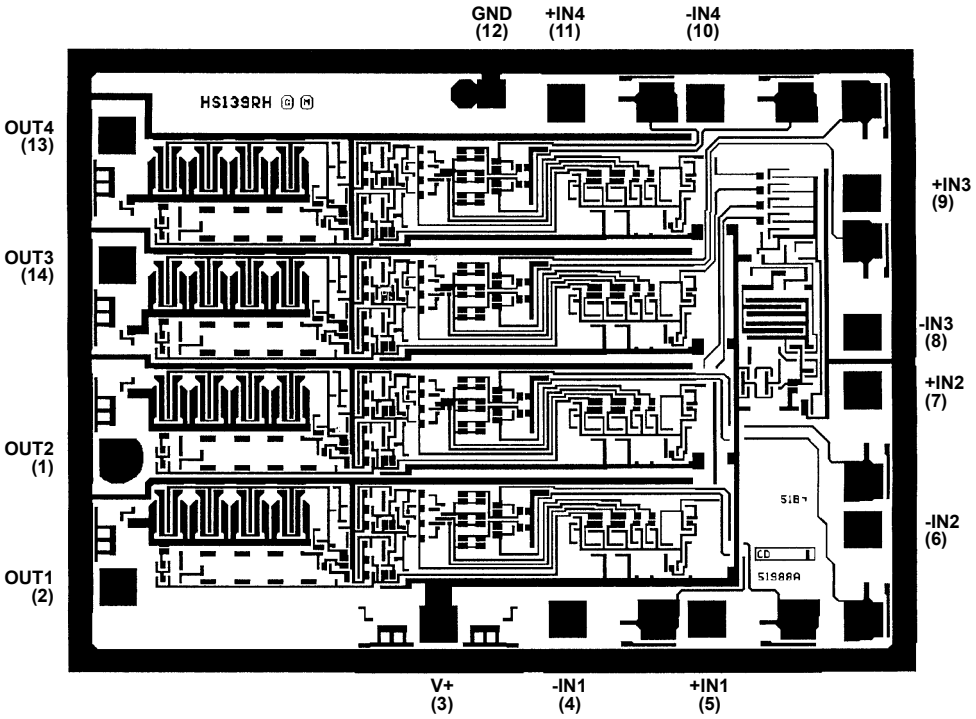


TABLE 1. HS-139RH, HS-139EH PAD COORDINATES

| PIN NUMBER | PAD NAME | RELATIVE TO PIN 1 | |
|---|---|---|---|
| | | X COORDINATES | Y COORDINATES |
| 1 | OUT 2 | 0 | 0 |
| 2 | OUT 1 | 0 | -535 |
| 3 | V+ | 1323 | -688 |
| 4 | -IN 1 | 1862 | -670 |
| 5 | +IN 1 | 2439 | -670 |
| 6 | -IN 2 | 3084 | -299 |
| 7 | +IN 2 | 3084 | 278 |
| 8 | -IN 3 | 3084 | 518 |
| 9 | +IN 3 | 3084 | 1095 |
| 10 | -IN 4 | 2439 | 1466 |
| 11 | +IN 4 | 1862 | 1466 |
| 12 | GND | 1550 | 1503 |
| 13 | OUT 4 | 0 | 1331 |
| 14 | OUT 3 | 0 | 796 |

NOTE: Dimensions in microns

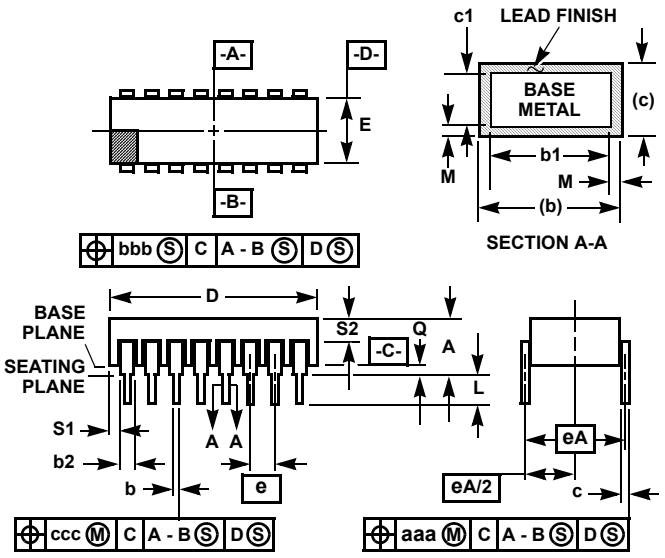
# Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

# Revision History

| REVISION | DATE | DESCRIPTION |
|---|---|---|
| 6.01 | May 5, 2025 | Updated Ordering Information table notes.<br>Added Revision History Section.<br>Updated POD K14.A to the latest revision; changes are as follows:<br>-Applied latest template<br>-Corrected typo in the mm value for dimension E1 from 7.11 to 7.37mm (i.e. the dim equivalent to E1 from the table in the previous revision) to make it equal to the 0.290 inch dim & compliant to MIL-STD-1835.<br>-Corrected typo in the dimension of the bottom ceramic pedestal width. |

## *Ceramic Dual-In-Line Metal Seal Packages (SBDIP)*




NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.

**D14.3 MIL-STD-1835 CDIP2-T14 (D-1, Configuration C)**
**14 Lead Ceramic Dual In-Line Metal Seal Package**

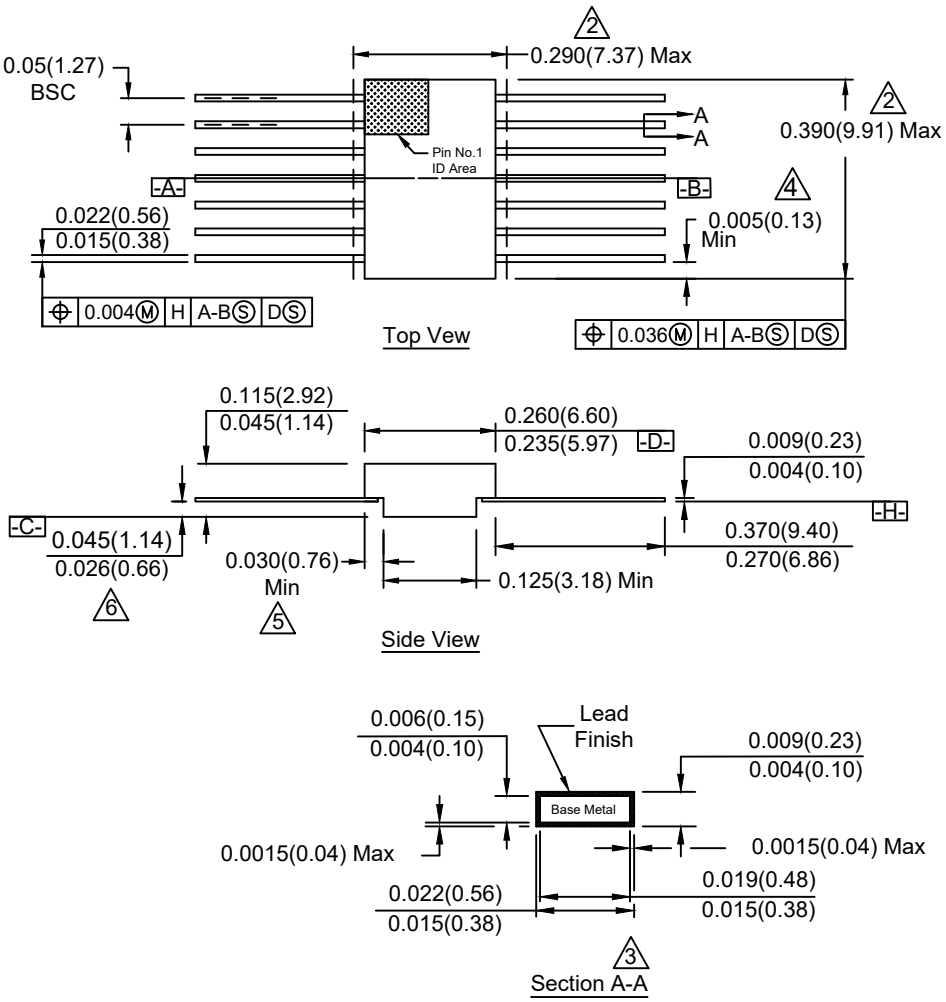
| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | |
| A | - | 0.200 | - | 5.08 | - |
| b | 0.014 | 0.026 | 0.36 | 0.66 | 2 |
| b1 | 0.014 | 0.023 | 0.36 | 0.58 | 3 |
| b2 | 0.045 | 0.065 | 1.14 | 1.65 | - |
| b3 | 0.023 | 0.045 | 0.58 | 1.14 | 4 |
| c | 0.008 | 0.018 | 0.20 | 0.46 | 2 |
| c1 | 0.008 | 0.015 | 0.20 | 0.38 | 3 |
| D | - | 0.785 | - | 19.94 | - |
| E | 0.220 | 0.310 | 5.59 | 7.87 | - |
| e | 0.100 BSC | | 2.54 BSC | | - |
| eA | 0.300 BSC | | 7.62 BSC | | - |
| eA/2 | 0.150 BSC | | 3.81 BSC | | - |
| L | 0.125 | 0.200 | 3.18 | 5.08 | - |
| Q | 0.015 | 0.060 | 0.38 | 1.52 | 5 |
| S1 | 0.005 | - | 0.13 | - | 6 |
| S2 | 0.005 | - | 0.13 | - | 7 |
| $\alpha$ | $90^o$ | $105^o$ | $90^o$ | $105^o$ | - |
| aaa | - | 0.015 | - | 0.38 | - |
| bbb | - | 0.030 | - | 0.76 | - |
| ccc | - | 0.010 | - | 0.25 | - |
| M | - | 0.0015 | - | 0.038 | 2 |
| N | 14 | | 14 | | 8 |

Rev. 0 4/94

# Package Outline Drawing

14 Lead Ceramic Metal Seal Flatpack Package

POD Number: K14.A, Revision no: 02, Date Created: Mar 4, 2025




Notes:

1 Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacture's identification shall not be used as a pin one identification mark.

2 This dimension allows for off-center lid, meniscus, and glass overrun.

3 The maximum limits of lead dimensions (section A-A) shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate finish is applied.

4 Measure dimension at all four corners.

5 For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.

6 This dimension shall be measured at the point of exit (beyond the meniscus) of the lead from the body. This dimension's minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.

7. Dimensioning and tolerancing per ANSI Y14.5M - 1982.

8. Dimensions: INCH(mm). Controlling dimension: INCH.

9. Compliant to MIL-STD-1835 CDFP3-F14 (F-2A, CONFIGURATION B).

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