HS-201HSRH, HS-201HSEH

Radiation Hardened High Speed, Quad SPST, BiCMOS Analog Switch

The HS-201HSRH and HS-201HSEH are monolithic BiCMOS analog switches featuring power-off high input impedance, very fast switching speeds and low ON-resistance. Fabrication on our DI RSG process ensures SEL immunity and only very slight low dose rate sensitivity (ELDRS). These Class V/Q devices are tested and guaranteed for 300krad(Si) total dose performance.

Power-off high input impedance enables the use of this device in redundant circuits without causing data bus signal degradation. ESD protection, overvoltage protection, fast switching times, low ON-resistance, and guaranteed radiation hardness make the HS-201HSRH ideal for any space application that requires improved switching performance.

Applications

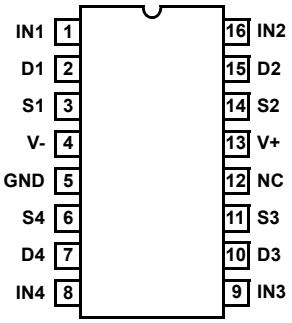
- High speed multiplexing
- Sample and hold circuits
- Digital filters
- Operational amplifier gain switching networks
  - Integrator reset circuits

Features

- Electrically screened to DLA SMD# 5962-99618
- QML qualified per MIL-PRF-38535
- TID Rad Hard Assurance (RHA) testing (HS-201HSRH)
  - HDR (50-300rad(Si)/s) . . . . . 300krad(Si)
- TID Rad Hard Assurance (RHA) testing (HS-201HSEH)
  - HDR (50-300rad(Si)/s) . . . . . 300krad(Si)
  - LDR (0.01rad(Si)/s) . . . . . 50krad(Si)
- SEL immune: DI RSG process
- Overvoltage protection (power on, switch off) . . . . . ±30V
- Power off high impedance . . . . . ±17V
- Fast switching times
  - t_{ON} . . . . . 110ns (max)
  - t_{OFF} . . . . . 80ns (max)
- Low ON-resistance . . . . . 50Ω (max)
- Pin compatible with industry-standard 201 types
- Operating supply range . . . . . ±10V to ±15V
- Wide analog voltage range (±15V supplies) . . . . . ±15V
- TTL compatible

Pin Configuration

HS1-201HSRH, HS1-201HSEH SBDIP (CDIP2-T16)
HS9-201HSRH, HS9-201HSEH FLATPACK (CDFP4-F16)
TOP VIEW



Ordering Information

ORDERING SMD NUMBER (Note 2)	INTERNAL PART NUMBER (Note 1)	RADIATION HARDNESS (Total Ionizing Dose)	PACKAGE DESCRIPTION (RoHS COMPLIANT)	PKG. DWG. #	TEMP. RANGE
5962F9961801VEC	HS1-201HSRH-Q	HDR to 300krad(Si)	16 Ld SBDIP	D16.3	-55 to +125°C
5962F9961802VEC	HS1-201HSEH-Q	HDR to 300krad(Si) LDR to 50krad(Si)			
5962F9961801QEC	HS1-201HSRH-8	HDR to 300krad(Si)			
5962F9961801VXC	HS9-201HSRH-Q	HDR to 300krad(Si)	16 Ld Flatpack	K16.A	
5962F9961802VXC	HS9-201HSEH-Q	HDR to 300krad(Si) LDR to 50krad(Si)			
5962F9961801QXC	HS9-201HSRH-8	HDR to 300krad(Si)			
5962F9961801V9A	HS0-201HSRH-Q (Note 4)	HDR to 300krad(Si)	Die	-	
5962F9961802V9A	HS0-201HSEH-Q (Note 4)	HDR to 300krad(Si) LDR to 50krad(Si)			
N/A	HS1-201HSRH/PROTO (Note 3)	N/A	16 Ld SBDIP	D16.3	
	HS9-201HSRH/PROTO (Note 3)		16 Ld Flatpack	K16.A	
	HS0-201HSRH/SAMPLE (Notes 3, 4)		Die	-	

NOTES:

1. These Intersil Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
2. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The listed SMD numbers must be used when ordering.
3. /PROTO and /SAMPLE note - The /PROTO and /SAMPLE are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions across temperature specified in the DLA SMD and are in the same form and fit as the qualified device. The /SAMPLE parts can meet the electrical limits and conditions specified in the DLA SMD. The /SAMPLE parts do not receive 100% screening across temperature to the DLA SMD electrical limits. These part types do not come with a Certificate of Conformance because they are not DLA qualified devices.
4. Die product tested at T_A = + 25°C. The wafer probe test includes functional and parametric testing sufficient to make the die capable of meeting the electrical performance outlined in the SMD.

Die Characteristics

Die Dimensions

4950µm x 2970µm (195 mils x 117 mils)
Thickness: 483µm ±25.4µm (19 mils ±1 mil)

Interface Materials

GLASSIVATION

Type: Phosphorus Silicon Glass (PSG)
Thickness: 8.0kÅ ±1.0kÅ

METALLIZATION

Type: AlSiCu
Thickness: 16.0kÅ ±2kÅ

SUBSTRATE

Rad Hard Silicon Gate, Dielectric Isolation

BACKSIDE FINISH

Silicon

Assembly Related Information

SUBSTRATE POTENTIAL

Unbiased (DI)

Additional Information

WORST CASE CURRENT DENSITY

$<2.0 \times 10^5 A/cm^2$

TRANSISTOR COUNT

328

Metallization Mask Layout

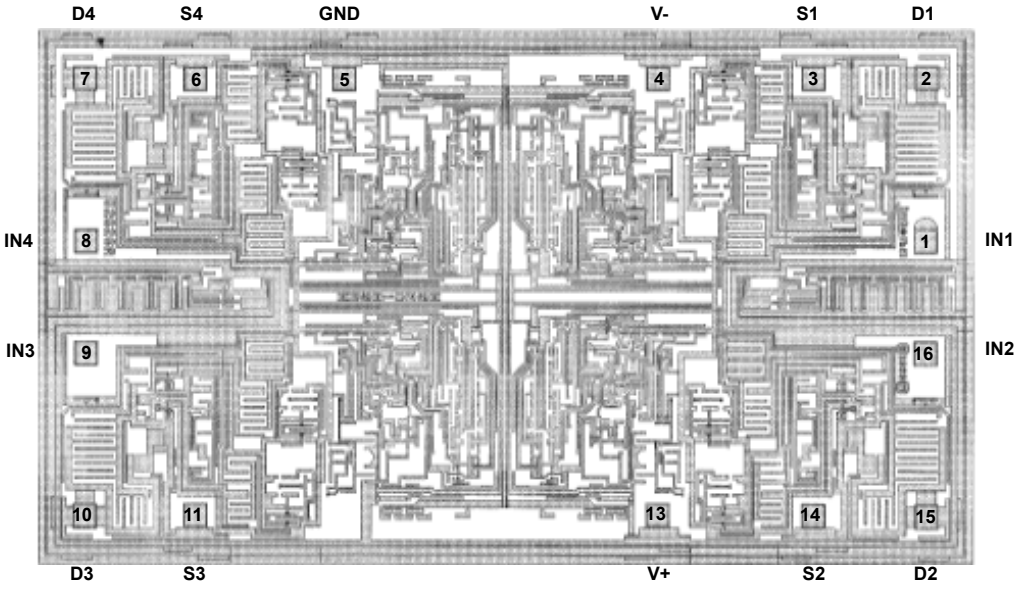


FIGURE 1. HS-201HSRH AND HS-201HSEH MASK LAYOUT

TABLE 1. LAYOUT X-Y COORDINATES

PAD NUMBER	PAD NAME	X (µm)	Y (µm)
01	IN1	365.5	1080.5
02	D1	364.5	277
03	S1	935	280
04	V-	1733	280
05	GND	3345	280
06	S4	4097	280
07	D4	4667.5	277
08	IN4	4666.5	1080.5
09	IN3	4666.5	1632.5
10	D3	4667.5	2436
11	S3	4097	2433
12	No Pad	-	-
13	V+	1733	2433
14	S2	935	2433
15	D2	364.5	2436
16	IN2	365.5	1632.5

NOTES:

5. Origin of coordinates is the upper right hand corner of the die.
6. Pad numbers are increased counter clockwise around the die.

Revision History

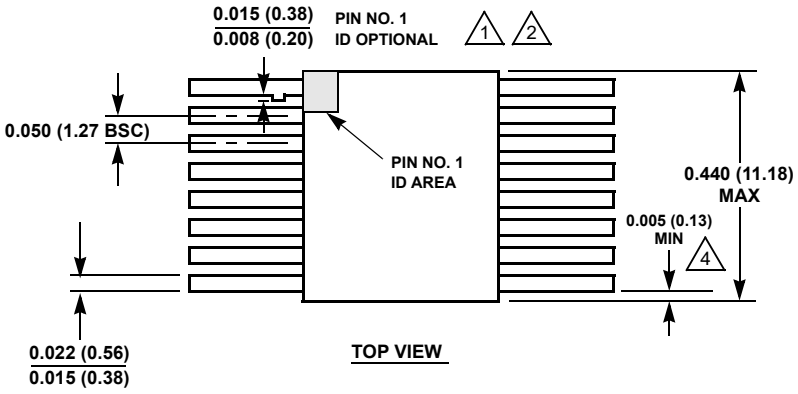
The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure that you have the latest revision.

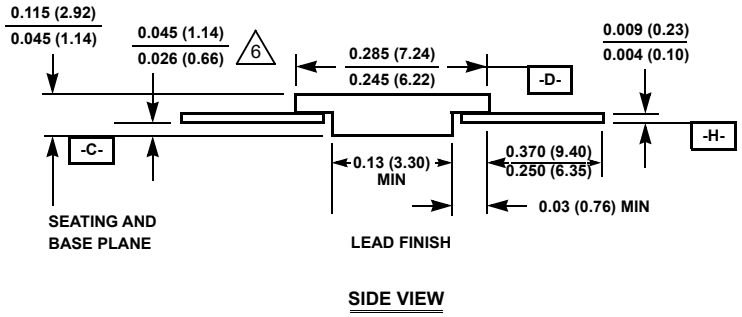
DATE	REVISION	CHANGE
May 8, 2024	4.01	Fixed hyperlinks throughout. Updated Features bullets. Removed Related Literature Updated Ordering Information table. Removed About Intersil section.
Feb 21, 2017	4.00	Changed die dimension from 2790µm x 4950µm (110 mils x 195 mils) to 4950µm x 2970µm (195mils x 117 mils). Added Table 1 “LAYOUT X-Y COORDINATES”. Changed pin names to match the pin names in the SMD data sheet. Added Revision History and About Intersil sections.

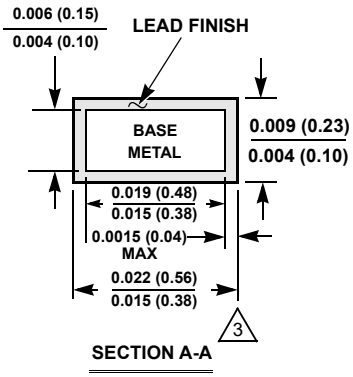
Package Outline Drawings

For the most recent package outline drawing, see K16.A.

K16.A
16 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE
Rev 2, 1/10





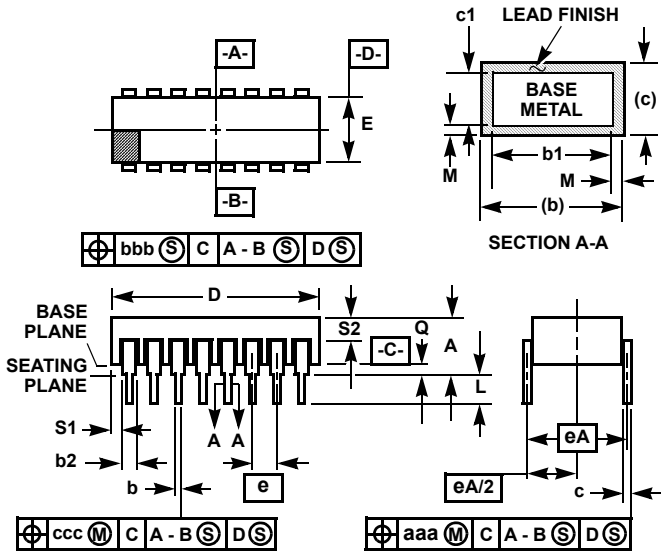


NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of the tab dimension do not apply.
3. The maximum limits of lead dimensions (section A-A) shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
4. Measure dimension at all four corners.
5. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
6. Dimension shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
7. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
8. Controlling dimension: INCH.

Ceramic Dual-In-Line Metal Seal Packages (SBDIP)

For the most recent package outline drawing, see D16.3.



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.

D16.3 MIL-STD-1835 CDIP2-T16 (D-2, CONFIGURATION C)
16 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	-
E	0.220	0.310	5.59	7.87	-
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	5
S1	0.005	-	0.13	-	6
S2	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	16		16		8

Rev. 0 4/94

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01 Jan 2024)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.