

HS-26CLV31RH, HS-26CLV31EH

Radiation Hardened 3.3V Quad Differential Line Drivers

Description

The [HS-26CLV31RH](#), [HS-26CLV31EH](#) are radiation hardened 3.3V quad differential line drivers designed for digital data transmission over balanced lines, in low voltage RS-422 protocol applications. CMOS processing assures low power consumption, high speed, and reliable operation in the most severe radiation environments.

The HS-26CLV31RH and HS-26CLV31EH accept CMOS level inputs and converts them to differential outputs. Enable pins allow several devices to be connected to the same data source and addressed independently. These devices have unique outputs that become high impedance when the driver is disabled or powered-down ($V_{DD} = 0V$), maintaining signal integrity in multi-driver applications.

Detailed Electrical Specifications for these devices are contained in SMD 5962-96663. A link is provided on our homepage for downloading.

Features

- Electrically screened to SMD #[5962-96663](#)
- QML qualified per MIL-PRF-38535 requirements
- 1.2 micron radiation hardened CMOS
- Extremely low stand-by current: 100 μ A (maximum)
- Operating supply range: 3.0V to 3.6V
- CMOS level inputs: $V_{IH} > (0.7) (V_{DD})$; $V_{IL} < (0.3) (V_{DD})$
- Differential outputs: $V_{OH} > 1.8V$; $V_{OL} < 0.5V$
- High impedance outputs when disabled or powered down ($V_{DD} = 0V$)
- Low output impedance: 10 Ω or less
- Radiation acceptance testing - HS-26C31RH
 - HDR (50-300rad(Si)/s): 300krad(Si)
- Radiation acceptance testing - HS-26C31EH
 - HDR (50-300rad(Si)/s): 300krad(Si)
 - LDR (0.01rad(Si)/s): 50krad(Si)
- SEL immune to LET: 100MeV $\cdot$ cm²/mg
- Full -55°C to +125°C military temperature range
- Pb-free (RoHS compliant)

Applications

- Line transmitter for MIL-STD-1553 serial data bus
- Line Transmitter for RS-422

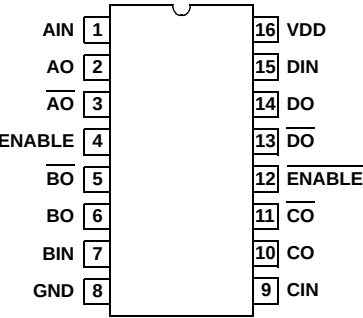
Contents

1.	Pin Information	3
1.1	Pin Assignments	3
1.2	Pin Descriptions	3
2.	Specifications	5
2.1	Absolute Maximum Ratings	5
2.2	Recommended Operating Conditions	5
2.3	Thermal Specifications	5
2.4	Electrical Specifications	5
2.5	Timing and Load Circuit Diagrams	7
3.	Typical Performance Graphs	8
4.	Application Information	9
4.1	Typical V_{OH} and V_{OL} Values	9
4.2	Enable Pins	9
4.3	Paralleling Unpowered Driver (Cold Sparing)	10
4.4	Line Terminations	10
4.5	Ground Potential Difference (GPD) Considerations	12
5.	Die and Assembly Characteristics	12
5.1	Metallization Mask Layout	13
6.	Package Outline Drawings	14
7.	Ordering Information	16
8.	Revision History	16

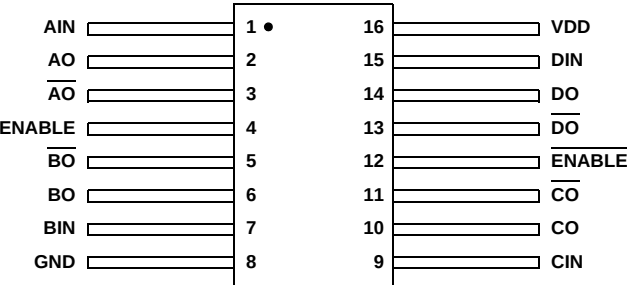
1. Pin Information

1.1 Pin Assignments

HS1-26CLV31RH, HS1-26CLV31EH
(16 LD SBDIP)
CDIP2-T16- Top View



HS9-26CLV31RH, HS9-26CLV31EH
(16 LD Flatpack)
CDFP4-F16 - Top View



1.2 Pin Descriptions

Pin Number	Pin Name
1	AIN
2	AO
3	AO
4	ENABLE
5	BO
6	BO
7	BIN
8	GND
9	CIN
10	CO
11	CO
12	ENABLE
13	DO
14	DO
15	DIN
16	VDD

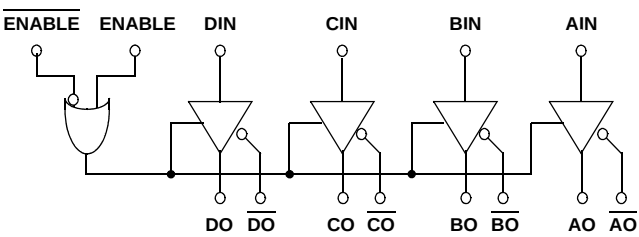


Figure 1. Logic Diagram

Table 1. Truth Table^[1]

Device Power On/Off	Inputs			Outputs	
	ENABLE	$\overline{\text{ENABLE}}$	IN	OUT	$\overline{\text{OUT}}$
ON	0	1	X	HI-Z	HI-Z
ON	1	X	0	0	1
ON	X	0	0	0	1
ON	1	X	1	1	0
ON	X	0	1	1	0
OFF (0V)	X	X	X	HI-Z	HI-Z

1. X = Don't Care, 0 = Low, 1 = High

2. Specifications

2.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
Supply Voltage	-0.5	7.0	V _{DC}
INPUTS, E, $\overline{E}$ Voltage	-0.5	V _{DD} + 0.5	V _{DC}
Output Voltage with Power On or Off (0V)	-0.5	7.0	V _{DC}
DC Diode Input Current (any input)	-	±20	mA
DC Drain Current (any one output)	-	350	mA
DC VDD or Ground Current	-	400	mA
Junction Temperature	-	175	°C
Storage Temperature	-65	150	°C
Human Body Model (Tested per MIL-PRF-883 3015.7)	-	300	V

2.2 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Supply Voltage, V _{DD}	3.0	3.6	V
Ambient Temperature	-55	+125	°C
Low Input Voltage	0	0.3 V _{DD} Maximum	V
High Input Voltage	V _{DD}	0.7 V _{DD} Minimum	V

2.3 Thermal Specifications

Parameter	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance	16Ld Flatpack Package	$\theta_{JA}^{[1]}$	Junction to ambient	114	°C/W
		$\theta_{JC}^{[2]}$	Junction to case	29	°C/W
Thermal Resistance	16Ld SBDIP Package	$\theta_{JA}^{[1]}$	Junction to ambient	73	°C/W
		$\theta_{JC}^{[2]}$	Junction to case	24	°C/W

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board (two buried 1oz copper planes) with direct attach features (package base mounted to PCB thermal land with a 10 mil gap fill material having a k of 1W/m-K. See [TB379](#)).
2. For θ_{JC} , the case temperature location is the center of the package underside.

2.4 Electrical Specifications

Test Conditions: V_{DD} = 3.0V to 3.6V; Typical values are at T_A = +25°C; unless otherwise specified^[1]. **Boldface limits apply across the operating temperature range, -55°C to +125°C; over a total ionizing dose of 50krad(Si) at +25°C with exposure at a low dose rate of <10mrads(Si)/s.; and over a total ionizing dose of 300krad(Si) at +25°C with exposure at a high dose rate of 50rad(Si)/s to 300rad(Si)/s.**

Parameter	Symbol	Test Conditions	Temp (°C)	Min ^[2]	Typ ^[3]	Max ^[2]	Unit
High Level Output Voltage	V _{OH}	VDD = 3.0V and 3.6V, IO = -20mA ^{[4][5]}	Full	1.8	-	-	V
Low Level Output Voltage	V _{OL}	VDD = 3.0V and 3.6V, IO = 20mA ^{[4][5]}	Full	-	-	0.5	V
Differential Output Voltage	V _T , $\overline{V_T}$	VDD = V _{IH} = 3.0V, RL = R1 + R2, VIL = 0V ^[6]	Full	1.8	-	-	V
Difference in Differential Output	V _T - $\overline{V_T}$	VDD = V _{IH} = 3.0V, RL = R1 + R2, VIL = 0V ^[6]	Full	-	-	0.4	V

Test Conditions: $V_{DD} = 3.0V$ to $3.6V$; Typical values are at $T_A = +25^\circ C$; unless otherwise specified^[1]. **Boldface limits apply across the operating temperature range, $-55^\circ C$ to $+125^\circ C$; over a total ionizing dose of 50krad(Si) at $+25^\circ C$ with exposure at a low dose rate of $<10\text{mrad(Si)/s}$; and over a total ionizing dose of 300krad(Si) at $+25^\circ C$ with exposure at a high dose rate of 50rad(Si)/s to 300rad(Si)/s.**

Parameter	Symbol	Test Conditions	Temp (°C)	Min ^[2]	Typ ^[3]	Max ^[2]	Unit
Common Mode Output Voltage	$V_{OS}, \overline{V_{OS}}$	$V_{DD} = V_{IH} = 3.0V, R_L = R_1 + R_2, V_{IL} = 0V^{[6]}$	Full	-	-	3.0	V
Difference in Common Mode Output Voltage	$ V_{OS} - V_{OS} $	$V_{DD} = V_{IH} = 3.0V, R_L = R_1 + R_2, V_{IL} = 0V^{[6]}$	Full	-	-	0.4	V
High Level Input Voltage	V_{IH}	$V_{DD} = 3.0V, 3.6V^{[7]}$	Full	0.7VDD	-	-	V
Low Level Input Voltage	V_{IL}	$V_{DD} = 3.0V, 3.6V^{[7]}$	Full	-	-	0.3VDD	V
Standby Supply Current	I_{DDSB}	$V_{DD} = 3.6V$, Output = OPEN, $V_{IN} = V_{DD}$ or GND	Full	-	-	100	μA
Three-state Output Leakage Current	I_{OZ}	$V_{DD} = 3.6V$, Force Voltage = 0V or $V_{DD}^{[8]}$	Full	-	-	± 5	μA
Input Leakage	I_{IN}	$V_{DD} = 3.6V, V_{IN} = V_{DD}$ or GND	Full	-	-	± 1.0	μA
Output Leakage Current Power OFF	I_{OFF}	$V_{DD} = 0V, V_{OUT} = 6V, -250mV$ inputs = GND	Full	-100	-	+100	μA
Input Clamp Voltage	V_{IC}	At -1.0mA	Full	-	-	-1.5	V
		At +1.0mA	Full	-	-	+1.5	V
Input Capacitance	C_{IN}	$V_{DD} = \text{OPEN}, f = 1MHz^{[9][10]}$	Full	-	-	12	pF
Output Capacitance	C_{OUT}	$V_{DD} = \text{OPEN}, f = 1MHz^{[9][10]}$	Full	-	-	12	pF
Operating Short Circuit	I_{OS}	$V_{DD} = 3.6V, V_{IN} = V_{DD}$ or GND ^{[9][10][11]}	Full	-30	-	-150	mA
On-state Resistance	R_{ON}	$V_{DD} = 3.0V, V_{OUT} = 1.5V, V_{IN} = V_{DD}$ or GND ^{[9][10]}	Full	-	-	10	Ω
Propagation Delay	t_{PLH}, t_{PHL}	$V_{DD} = 3.0V^{[12]}$	Full	2	-	30	ns
	t_{PZH}, t_{PZL}	-	Full	5	-	42	ns
	t_{PHZ}, t_{PLZ}	-	Full	2	-	28	ns
Output Skew	t_{SKEW}	$V_{DD} = 3.0V, R_L = 100\Omega, C_L = 40pF^{[12][13]}$	Full	-	-	7	ns
Rise and Fall Times	t_{THL}, t_{TLH}	$V_{DD} = 3.0V^{[12]}$	Full	1	-	14	ns

1. All voltages are referenced to device ground unless otherwise specified.
2. Parameters with MIN and/or MAX limits are 100% tested at $-55^\circ C, +25^\circ C$ and $+125^\circ C$, unless otherwise specified.
3. Typical values are at 3.3V. Parameters with a single entry in the "TYP" column apply to 3.3V. Typical values shown are not guaranteed.
4. Force / measure functions may be interchanged.
5. $V_{IL} = 0.3 V_{DD}, V_{IH} = 0.7V_{DD}$.
6. These test conditions are detailed in EIA specification RS-422. $R_1 = R_2 = 50\Omega$.
7. This parameter tested as inputs levels in $V_{OL} / V_{OH}, I_{OZ}$, functional test and/or discrete voltage level.
8. The input is conditioned to have the output in the opposite state of the forcing I_{OZ} condition.
9. These parameters are controlled through design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major design or process changes that affect these parameters.
10. Post irradiation electrical performance testing not performed for these parameters.
11. Only one output at a time may be shorted.
12. See table EIA RS-422. See [Figure 2](#) and [Figure 3](#).
13. Skew is defined as the difference in propagation delays between complementary outputs at the 50% point.

2.5 Timing and Load Circuit Diagrams

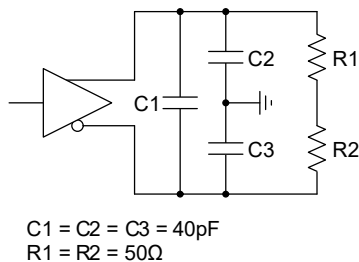


Figure 2. Propagation Delay Load Circuit

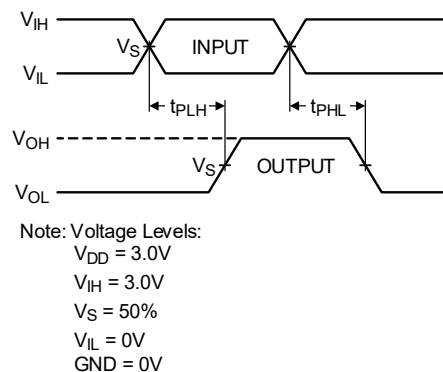


Figure 3. Propagation Delay Timing Diagram

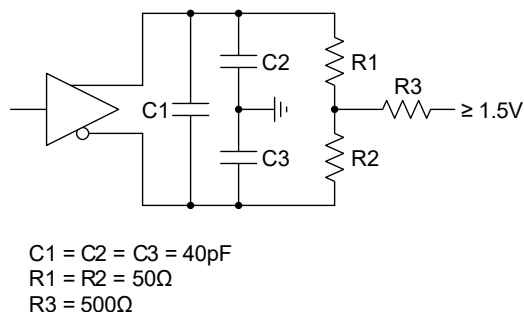


Figure 4. Tri-State Low Load Circuit

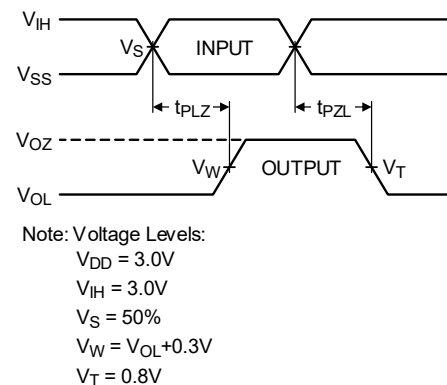


Figure 5. Tri-State Low Timing Diagram

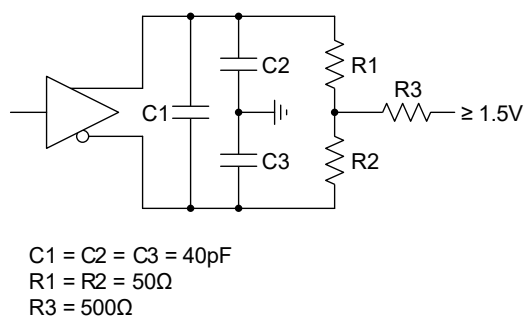


Figure 6. Tri-State High Load Circuit

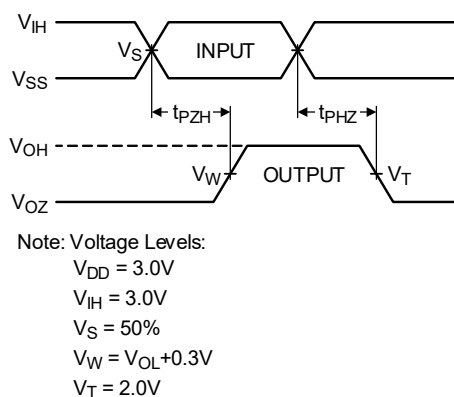


Figure 7. Tri-State High Timing Diagram

3. Typical Performance Graphs

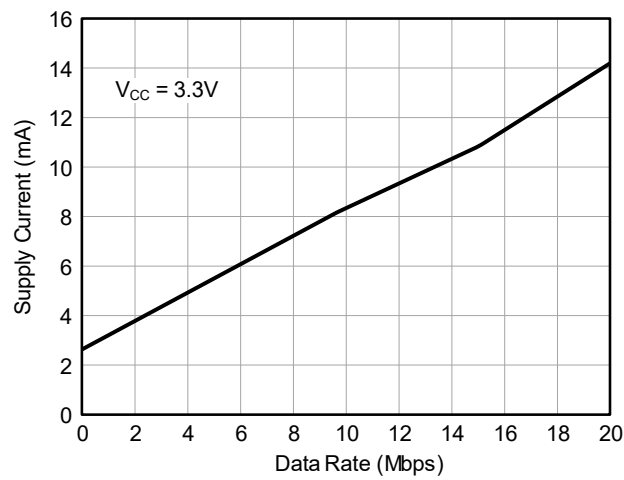


Figure 8. Supply Current (One Channel)

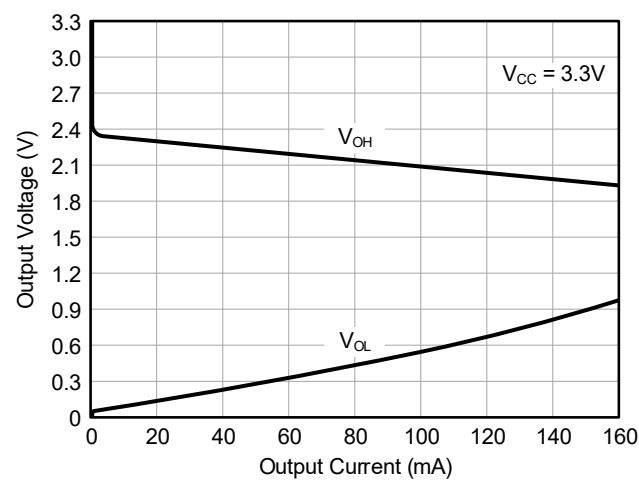


Figure 9. Driver Single Output Load Characteristic

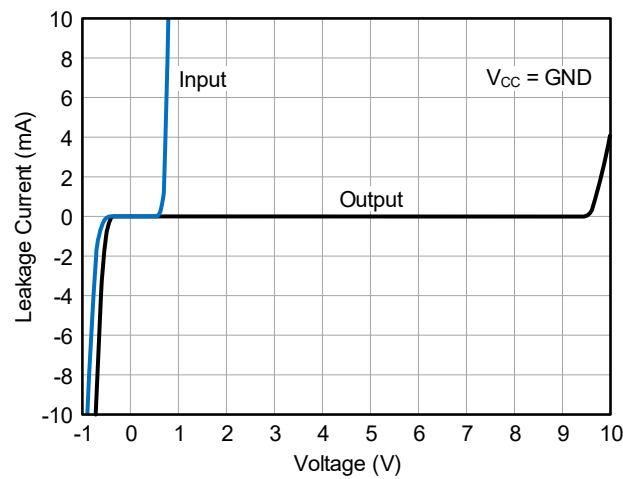


Figure 10. Cold-Spare Leakage Current

4. Application Information

4.1 Typical V_{OH} and V_{OL} Values

To derive the typical high and low output voltages for either the inverting or non-inverting output, determine the differential output voltage, $V_{OD} = V_{OH} - V_{OL}$, from the curves in Figure 9.

Note: The V_{OD} curve in Figure 11 also represents the differential output resistance of the driver, which is in series with the external 100Ω load resistance.

Draw the 100Ω load line from the origin. The current at the intersection of the load line and the V_{OD} curve is the differential output current, I_{OD} . In the V_{OH} and V_{OL} plot, draw a vertical line at I_{OD} . The points at which this line intersects the V_{OH} and V_{OL} curves indicate the typical V_{OH} and V_{OL} values. For the HS-26CLV31, these values are $V_{OH} = 2.3V$ and $V_{OL} = 0.15V$.

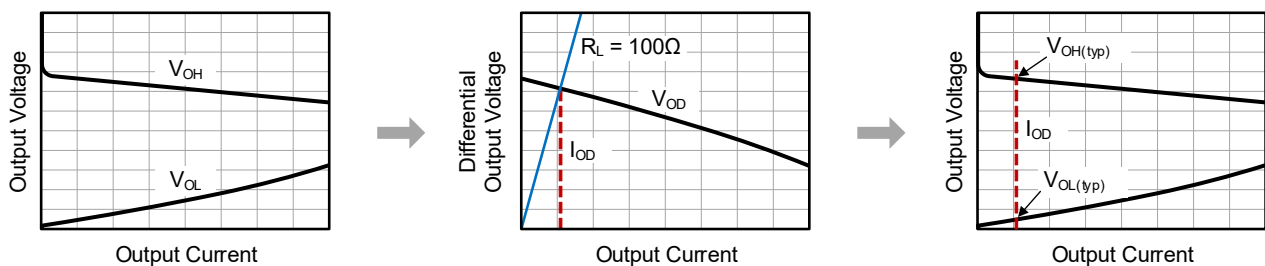


Figure 11. Deriving Typical Values for V_{OH} and V_{OL}

4.2 Enable Pins

The enable pins of the HS-26CLV31 are internally OR-gated, allowing the device to be activated through either active-high or active-low logic levels (see Figure 12).

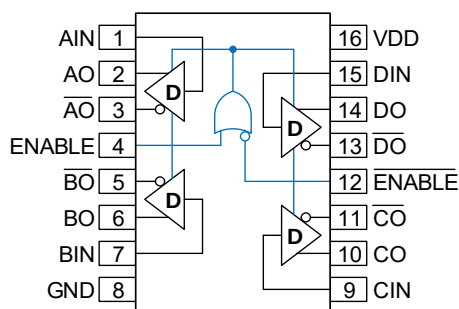


Figure 12. HS-26CLV31 Diagram

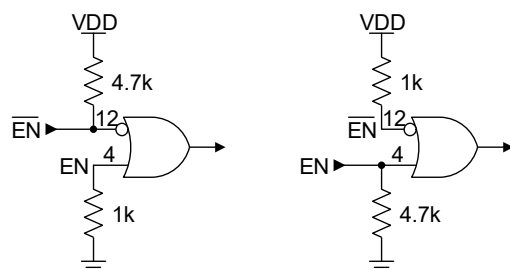


Figure 13. Enable Pin Configurations

Connect unused enable pins to one of the supply rails to disable their function. That is, connect $\overline{\text{ENABLE}}$ to VDD or ENABLE to GND. If large transients are expected on either supply rail, use a series resistor that limits the transient current into the device's internal ESD diodes (see Figure 13).

Enable pins that are dynamically controlled by an FPGA or microcontroller (MCU) should be pulled high or pulled low using a $4.7k\Omega$ resistor. This value provides a balance between protection during power-up sequencing and the current-drive capability of the controlling device.

4.3 Paralleling Unpowered Driver (Cold Sparing)

In space systems, a common technique for mitigating single-point failures is the use of redundant bus drivers and receivers in parallel, commonly referred to as cold sparing. In this configuration, an unpowered driver and receiver are connected in parallel with a powered driver and receiver pair.

The HS-26CLV31 provides RS-422-compliant output characteristics and power-off isolation. Figure 10 shows the input and output leakage-current characteristics of an unpowered transmitter ($V_{DD} = 0V$). Over the output voltage range of 0V to 6V, the output leakage current of the unpowered transmitter remains below $\pm 10nA$, minimizing the loading effect on the active bus driver.

4.4 Line Terminations

Line terminations are necessary to prevent signal reflections on the bus lines that could otherwise interfere with the transmitter's output signal and cause data errors. A variety of termination techniques exist, each of which presents certain benefits and disadvantages.

The parallel termination shown in Figure 14 is the simplest termination method. However, it requires the driver to remain continuously enabled to generate sufficient differential bus voltage and ensure a defined receiver output state at all times.

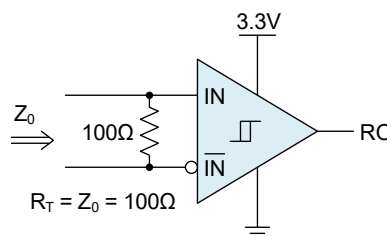


Figure 14. Parallel Termination

The power termination shown in Figure 15 eliminates this requirement by forming a voltage divider that generates sufficient input voltage, referred to as the idle-bus failsafe voltage, to ensure a defined receiver output state when the driver is disabled. A slight disadvantage of this approach is the continuous current drawn from the receiver supply to generate this failsafe voltage.

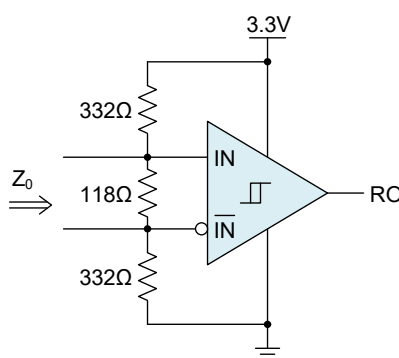


Figure 15. Power Termination

The AC termination shown in [Figure 16](#) eliminates the DC current consumption associated with power termination. In this configuration, the bus line is terminated only during signal transitions, while DC current flow is blocked during steady-state conditions. The 100Ω termination resistor matches the characteristic impedance of the cable. The value of the termination capacitor (C_T), however, depends on the cable length and signal propagation velocity.

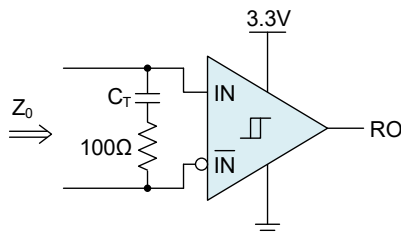


Figure 16. AC Termination

$$(EQ. 1) \quad C_T = \frac{2L_{\text{cable}}}{R_T \times v \times c}$$

$$(EQ. 2) \quad DR = \frac{0.1}{R_T \times C_T}$$

- L_{cable} = cable length (m)
- v = cable velocity factor (typical 0.7)
- c = speed of light ($3 \times 10^8 \text{m/s}$)
- R_T = Termination Resistor (typical 100Ω)
- DR = Data Rate (bps)

If the driver is disabled, both receiver inputs float. In this condition, the receiver generates its own open-bus failsafe voltage to ensure a defined receiver output state.

As the RC network forms a low-pass filter, the maximum data rate of this termination technique is limited to a few hundred kilobits per second. Its component values, however, are independent of the receiver supply voltage.

The alternate termination shown in [Figure 17](#) allows the receiver to detect both bus-fault and driver-disabled conditions. If the bus is shorted, the 102Ω termination resistor is shunted, and the shorted-bus failsafe voltage is generated across the two 562Ω resistors. If the driver is disabled, the idle-bus failsafe voltage is generated across the entire termination network consisting of the 102Ω and the two 562Ω resistors.

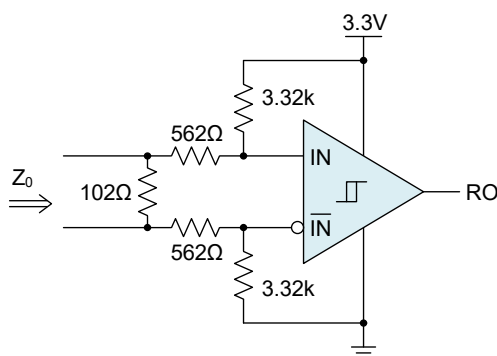


Figure 17. Alternate Termination

4.5 Ground Potential Difference (GPD) Considerations

While an RS-422 receiver must withstand large input voltages of up to $\pm 12\text{V}$ without damage, the breakdown voltage of an RS-422 driver is limited by its supply rails.

Figure 18 shows the common-mode voltage relations on the bus when the driver is enabled. Applying the high and low driver output voltages of **Typical V_{OH} and V_{OL} Values** with $V_{OH} = 2.3\text{V}$ and $V_{OL} = 0.15\text{V}$ results in a driver common-mode output voltage of $V_{OC} = (V_{OH} + V_{OL})/2 = (2.3\text{V} + 0.15\text{V})/2 = 1.225\text{V}$. Then, with a projected ground potential difference of $\text{GPD} = \pm 7\text{V}$, the common-mode voltage range at the receiver inputs is $+8.225\text{V} \leq V_{IC} \leq -5.775\text{V}$. This value is well within the specified $\pm 12\text{V}$ range.

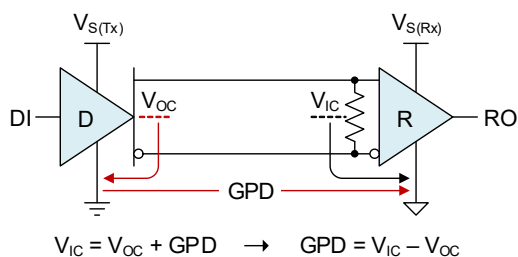


Figure 18. Common-Mode Voltages for Enabled Driver

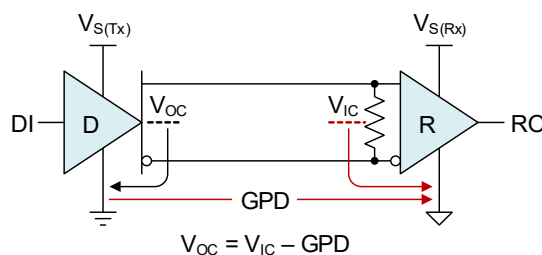


Figure 19. Common-Mode Voltages for Disabled Driver

If the driver is disabled (Figure 19), the driver outputs are high impedance and must withstand the sum of the GPD and the voltage at the terminated receiver inputs, V_{IC} , which is half the receiver supply voltage or 1.65V .

Consequently, the sum of V_{IC} and GPD results in a driver common-mode output of $-5.35\text{V} \leq V_{OC} \leq +8.65\text{V}$, with both values lying well outside the absolute maximum ratings of the driver's supply rails of 7V and 0V .

IMPORTANT: Always start the interface design with the driver disabled and limit any ground potential difference to between -2V and $+4\text{V}$.

5. Die and Assembly Characteristics

Table 2. Die and Assembly Related Information

Die Information	
Dimensions	96.5 mils x 195 mils x 19 mils $\pm 1\text{mil}$ 2451 μm x 4953 μm x 483 μm $\pm 25\mu\text{m}$
Interface Materials	
Glassivation	Type: PSG (Phosphorus Silicon Glass) Thickness: 8k $\text{\AA}$ $\pm 1\text{k}\text{\AA}$
Metallization	M1: Mo/TiW (Bottom) Thickness: 5800 $\text{\AA}$ $\pm 1\text{k}\text{\AA}$ M2: AlSiCu (Top) Thickness: 10k $\text{\AA}$ $\pm 1\text{k}\text{\AA}$
Substrate	AVLSI1RA
Backside Finish	Silicon
Assembly Information	
Substrate Potential (Powered Up)	Internally tied to V_{DD}
Additional Information	
Worst Case Current Density	$< 2.0 \times 10^5 \text{A/cm}^2$
Bond Pad Size	110 μm x 100 μm

5.1 Metallization Mask Layout

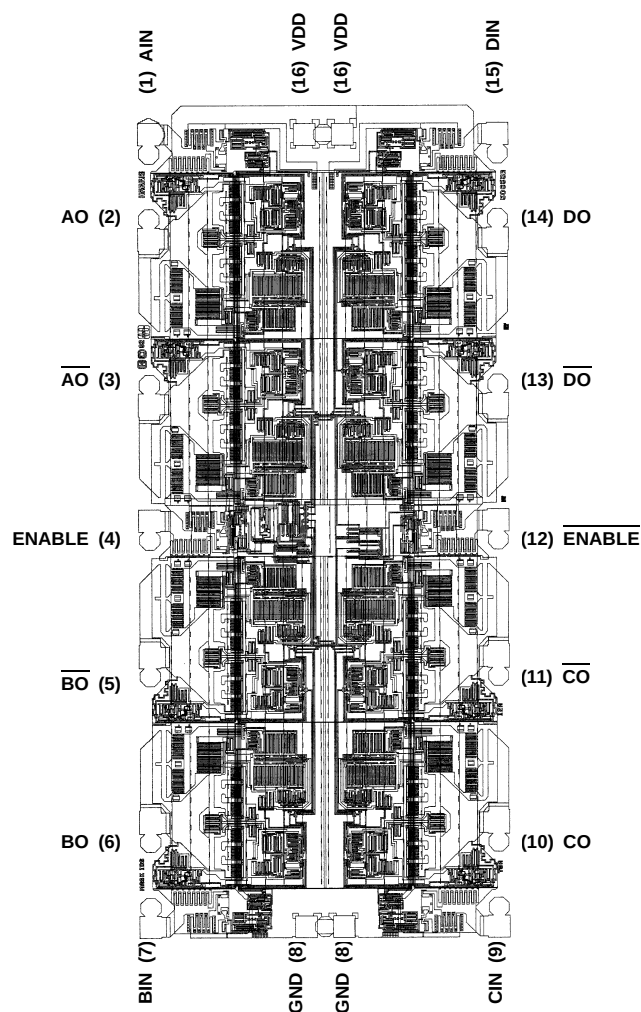


Table 3. HS-26CLV31RH, HS-26CLV31EH Pad Coordinates

Pin Number	Pad Name	Relative To Pin 1 ^[1]	
		X Coordinates	Y Coordinates
1	AIN	0	0
2	A0	0	-570.7
3	$\overline{A0}$	0	-1483.5
4	ENABLE	0	-2124.8
5	$\overline{B0}$	0	-2873.5
6	B0	0	-3786.3
7	BIN	0	-4357
8	GND	852.4	-4357
8	GND	1062.4	-4357
9	CIN	1912.8	-4357
10	$\overline{C0}$	1912.8	-3786.3
11	C0	1912.8	-2873.5
12	$\overline{ENABLE}$	1912.8	-2124.8
13	$\overline{D0}$	1912.8	-1483.5
14	D0	1912.8	-570.7
15	DIN	1912.8	0
16	VIN	1062.4	0
16	VIN	852.4	0

1. Dimensions in microns.

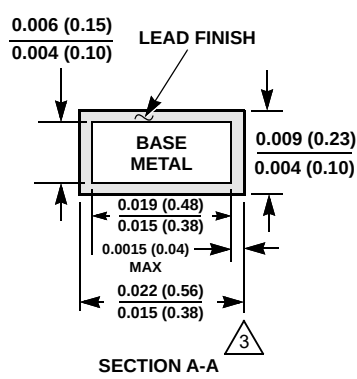
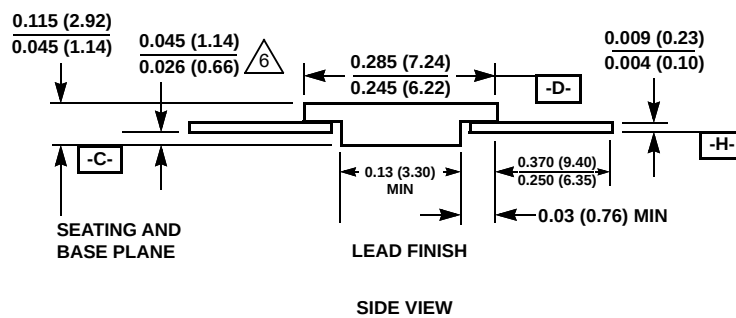
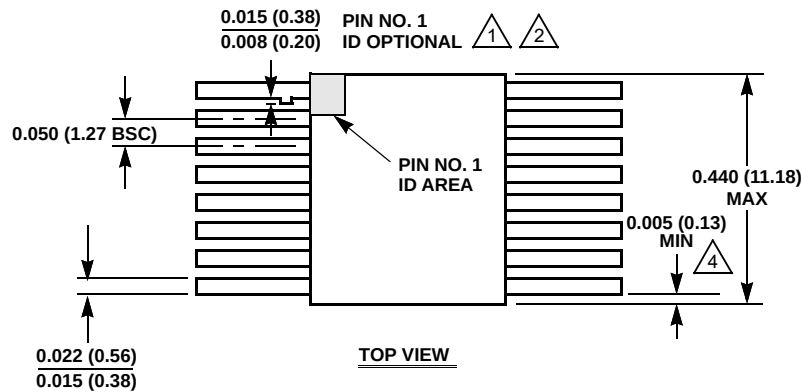
6. Package Outline Drawings

For the most recent package outline drawing, see [K16.A](#).

K16.A

16 Lead Ceramic Metal Seal Flatpack Package

Rev 2, 1/10

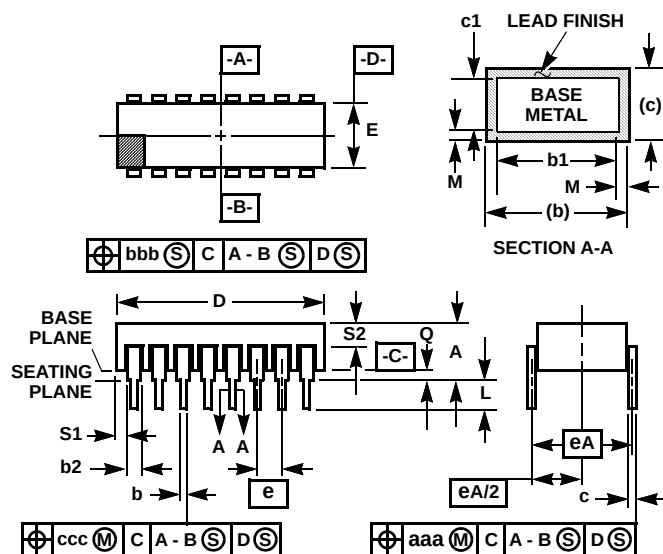


NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of the tab dimension do not apply.
3. The maximum limits of lead dimensions (section A-A) shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
4. Measure dimension at all four corners.
5. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
6. Dimension shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
7. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
8. Controlling dimension: INCH.

For the most recent package outline drawing, see [D16.3](#).

Ceramic Dual-In-Line Metal Seal Packages (SBDIP)



Notes:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.

D16.3 MIL-STD-1835 CDIP2-T16 (D-2, CONFIGURATION C) 16 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE

Symbol	Inches		Millimeters		Notes
	Min	Max	Min	Max	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	-
E	0.220	0.310	5.59	7.87	-
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	5
S1	0.005	-	0.13	-	6
S2	0.005	-	0.13	-	7
a	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	16		16		8

Rev. 0 4/94

7. Ordering Information

SMD Part Number ^[1]	Part Number ^[2]	Radiation Hardness (Total Ionizing Dose)	Package Description (RoHS Compliant)	Package Drawing	Carrier Type	Temp. Range
5962F9666302QEC	HS1-26CLV31RH-8	HDR to 300krad(Si)	16 Ld SBDIP	D16.3	Tube	-55 to +125°C
5962F9666302QXC	HS9-26CLV31RH-8		16 Ld FLATPACK	K16.A	Tray	
5962F9666302VEC	HS1-26CLV31RH-Q		16 Ld SBDIP	D16.3	Tube	
5962F9666302VXC	HS9-26CLV31RH-Q		16 Ld FLATPACK	K16.A	Tray	
5962F9666302V9A	HS0-26CLV31RH-Q ^[3]		Die	N/A	N/A	
5962F9666302VYC	HS9G-26CLV31RH-Q ^[4]		16 Ld FLATPACK	K16.A	Tray	
N/A	HS0-26CLV31RH/SAMPLE ^{[3][5]}	N/A	Die	N/A	N/A	-55 to +125°C
	HS1-26CLV31RH/PROTO ^[5]		16 Ld SBDIP	D16.3	Tube	
	HS9-26CLV31RH/PROTO ^[5]		16 Ld FLATPACK	K16.A	Tray	
	HS9G-26CLV31RH/PROTO ^{[4][5]}		16 Ld FLATPACK	K16.A	Tray	
5962F9666304VEC	HS1-26CLV31EH-Q	HDR to 300krad(Si) LDR to 50krad(Si)	16 Ld SBDIP	D16.3	Tube	-55 to +125°C
5962F9666304VXC	HS9-26CLV31EH-Q		16 Ld FLATPACK	K16.A	Tray	
5962F9666304V9A	HS0-26CLV31EH-Q ^[3]		Die	N/A	N/A	
5962F9666304VYC	HS9G-26CLV31EH-Q ^[4]		16 Ld FLATPACK	K16.A	Tray	

- Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed must be used when ordering.
- These Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
- Die product tested at $T_A = +25^\circ\text{C}$. The wafer probe test includes functional and parametric testing sufficient to make the die capable of meeting the electrical performance outlined in SMD.
- The lid of these packages are connected to the ground pin of the device.
- The /PROTO and /SAMPLE are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions across the temperature range specified in the DLA SMD and are in the same form and fit as the qualified device. The /SAMPLE parts are capable of meeting the electrical limits and conditions specified in the DLA SMD. The /SAMPLE parts do not receive 100% screening across temperature to the DLA SMD electrical limits. These part types do not come with a certificate of conformance because they are not DLA qualified devices.

8. Revision History

Revision	Date	Change
6.04	Oct 20, 2026	Added Typical Performance Graphs and Application Information sections.
6.03	May 30, 2025	Updated Figures 2 through 7.
6.02	Apr 15, 2025	- Placed into the latest template. - Added Pin Descriptions table, Absolute Maximum Ratings, Electrical Specifications, and Timing and Load Circuit Diagrams.
6.01	Aug 5, 2022	Updated Table 1.

Revision	Date	Change
6.00	Oct 21, 2021	- Removed Related Literature section. - Added Radiation acceptance testing bullets for RH and EH parts to the features section. - Updated Ordering Information table by adding carrier type and radiation testing information columns, verified part numbers in table are correct, and added Note 3 and updated Note 5. - Added Truth Table. - Updated the Die Characteristics information as follows: - Die thickness changed from:21mils, to:19mils. - Updated Substrate Potential (Powered Up) information.
5.00	Oct 26, 2018	- Added Related Literature section. - Updated Ordering Information table: - Added HS9G-26CLV31EH-Q part and added Notes 1 and 4. - Removed part Marking column. - Added Revision History. - Added PODs D16.3 and K16.A - Updated Disclaimer.

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