HS-26CLV32RH, HS-26CLV32EH

Radiation Hardened 3.3V Quad Differential Line Receivers

Description

The HS-26CLV32RH, HS-26CLV32EH are radiation hardened 3.3V quad differential line receivers designed for digital data transmission over balanced lines, in low voltage, RS-422 protocol applications. Radiation hardened CMOS processing assures low power consumption, high speed, and reliable operation in the most severe radiation environments.

The HS-26CLV32RH, HS-26CLV32EH have an input sensitivity of 200mV (typical) over a common-mode input voltage range of -4V to +7V. The receivers are also equipped with input fail-safe circuitry, which causes the outputs to go to a logic “1” when the inputs are open. The device has unique inputs that remain high impedance when the receiver is disabled or powered-down, maintaining signal integrity in multi-receiver applications.

Applications

- Line receiver for MIL-STD-1553 serial data bus
- Line receiver for RS-422

Features

- Electrically screened to SMD # 5962-95689
- QML qualified per MIL-PRF-38535 requirements
- 1.2 micron radiation hardened CMOS
- Low stand-by current: 13mA (max)
- Operating supply range: 3.0V to 3.6V
- Differential input voltage thresholds: ±400mV
- CMOS output levels: V_{OH} > 2.55V, V_{OL} < 0.4V
- Input fail-safe circuitry
- High impedance inputs when disabled or powered-down
- Radiation acceptance testing – HS-26CLV32RH
  - HDR (50-300rad (Si)/s): 300krad(Si)
- Radiation acceptance testing – HS-26CLV32EH
  - HDR (50-300rad(Si)/s): 300krad(Si)
  - LDR (0.01rad(Si)/s): 50krad(Si)
- SEL immune to LET: 100MeV•cm^2/mg
- Full -55°C to +125°C military temperature range
- Pb-free (RoHS compliant)

Contents

1. Pin Information

1.1 Pin Assignments

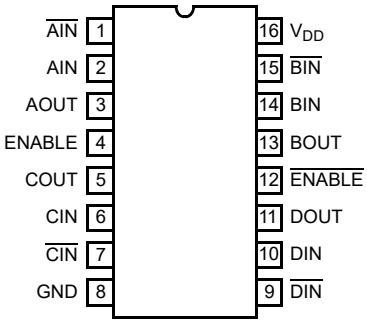


Figure 1. 16 LD SBDIP, MIL-STD-1835: CDIP2-T16 Top View[1][2]

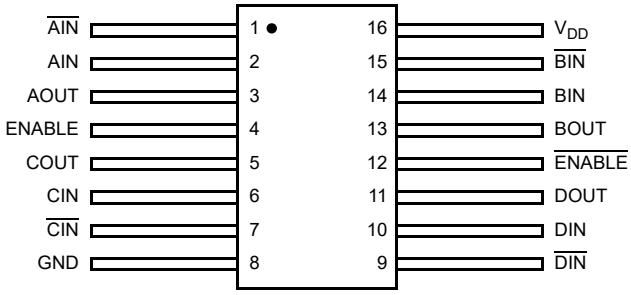


Figure 2. 16 LD FLATPACK, MIL-STD-1835: CDFP4-F16 Top View[1][2][3]

1. For details on the input output structures, refer to AN9520.
2. For details on the package dimensions, refer to MIL-STD-1835.
3. For 16 Ld Flatpack, there are two options; 1) Lid not grounded (noted as Case X in SMD and 2) Lid is grounded (noted as Case Y in SMD).

1.2 Pin Descriptions

Pin Number	Pin Name
1	$\overline{\text{AIN}}$
2	AIN
3	AOUT
4	ENABLE
5	COUT
6	CIN
7	$\overline{\text{CIN}}$
8	GND
9	$\overline{\text{DIN}}$
10	DIN
11	DOUT
12	$\overline{\text{ENABLE}}$
13	BOUT
14	BIN
15	$\overline{\text{BIN}}$
16	VDD

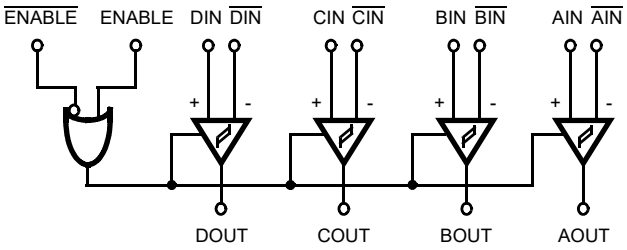


Figure 3. Logic Diagram

Table 1. Truth Table

Device Power On/off	Inputs[1]			Output
	ENABLE	$\overline{\text{ENABLE}}$	Input	Out
ON	0	1	X	HI-Z
ON	1	X	VID ≥ VTH (Max)	1
ON	1	X	VID ≤ VTH (Min)	0
ON	X	0	VID ≥ VTH (Max)	1
ON	X	0	VID ≤ VTH (Min)	0
ON	1	X	Open	1
ON	X	0	Open	1
OFF	X	X	X	HI-Z

1. X = Don't Care, 0 = Low, 1 = High

2. Specifications

2.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter		Minimum	Maximum	Unit
Supply Voltage		-0.5	+7.0	V
Differential Input Voltage		-12	+12	V
Common Mode Range		-12	+12	V
Enable Pins Input Voltage		-0.5	V_{DD} + 0.5	V
DC Drain Current (any one output)		-25	+25	mA
DC Diode Input Current Enable Pin		-20	+20	mA
Maximum Package Power Dissipation at T_A = +125°C	16 Ld SBDIP	-	0.6	W
	16 Ld Flatpack	-	0.5	W
Maximum Device Power Dissipation (PD)[1]		-	0.32	W
Human Body Model (Tested per MIL-PRF-883 3015.7)		-	750	V

1. Maximum device power dissipation is defined as V_{DD} x I_{CC} and must withstand the added P_D due to output current test; I_O at T_A = +125°C.

2.2 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Ambient Temperature Range	-55	+125	°C
V_{DD} Supply Voltage	+3.0	+3.6	V
Common Mode Range	-4.0	+7.0	V
Input Low Voltage (V_{IL})	0	0.3 V_{DD} max	V
Input High Voltage (V_{IH})	V_{DD}	+0.7 V_{DD} min	V
Input Rise and Fall Time	-	500	ns

2.3 Thermal Specifications

Parameter	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance	16 Ld Flatpack Package	θ_{JA}[1]	Junction to ambient	103	°C/W
		θ_{JC}[2]	Junction to case	26	°C/W
Thermal Resistance	16 Ld SBDIP Package	θ_{JA}[1]	Junction to ambient	80	°C/W
		θ_{JC}[2]	Junction to case	20	°C/W

1. θ_{JA} is measured with the component mounted on a low-effective thermal conductivity test board. See TB379 for details.
2. For θ_{JC}, the case temperature location is the center of the package underside.

2.4 Electrical Specifications

Test Conditions: V_{DD} = 3.0V to 3.6V; Typical values are at T_A = +25°C; unless otherwise specified[2]. **Boldface limits apply across the operating temperature range, -55°C to +125°C; over a total ionizing dose of 50krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s; and over a total ionizing dose of 300krad(SI) at +25°C with exposure of a high dose rate of 50krad(SI)/s to 300krad(SI)/s.**

Parameter	Symbol	Test Conditions	Temp (°C)	Min[1]	Typ[2]	Max[1]	Unit
High Level Output Voltage	V_{OH}	V_{DD} = 3.0V, V_{DIFF} = 1.0V, I_O = -6mA[3]	Full	**2.55**	-	-	V
Low Level Output Voltage	V_{OL}	V_{DD} = 3.0V, V_{DIFF} = -1.0V, I_O = 6mA[3]	Full	-	-	**0.4**	V
Input Voltage Threshold (Differential Input)	V_{TH}	V_{DD} = V_{IH} = 3.0V, -4.0V < V_{CM} < 7.0V	Full	**-400**	-	**+400**	mV
High Level Input Voltage (Logic Inputs)	V_{IH}	V_{DD} = 3.0V, 3.6V[4]	Full	**0.7 VDD**	-	-	V
Low Level Input Voltage (Logic Inputs)	V_{IL}	V_{DD} = 3.0V, 3.6V[4]	Full	-	-	**0.3 VDD**	V
Input Current High (Differential Inputs)	I_{INH}	V_{DD} = 3.6V, +V = 10V, -V = 0V and +V = 0V, -V = 10V	Full	-	-	**1.8**	mA
Input Current Low (Differential Inputs)	I_{INL}	V_{DD} = 3.6V, +V = -10V, -V = 0V and +V = 0V, -V = -10V	Full	**-2.7**	-	-	mA
Input Leakage Current, Enable Pins	I_{IN}	V_{DD} = 3.6V, V_{IN} = 0V, 3.6V	Full	**-1.0**	-	**+1.0**	µA
Three-state Output Leakage Current	I_{OZ}	V_{DD} = 3.6V, V_O = V_{DD} or GND	Full	**-5.0**	-	**5.0**	µA
Standby Supply Current	I_{DDSB}	V_{DD} = 3.6V, V_{DIFF} = 1.0V, Outputs = open	Full	-	-	**13**	mA
Enable Clamp Voltage	V_{IC}	At - 1mA	Full	**-1.5**	-	-	V
		At 1mA	Full	-	-	**+1.5**	
Input Hysteresis	V_{HYST}	-	Full	**20**[5]	-	**100**	mV
Input Resistance	R_{IN}	-4.0V < V_{CM} < 7.0V	Full	4	-	**20**	kΩ
Propagation Delay Time[6]	t_{PLH}, t_{PHL}	V_{DD} = 3.0V, V_{DIFF} = 2.5V, See Figure 5 through Figure 8.	Full	**6**	-	**65**	ns
	t_{PZH}, t_{PZL}		Full	**3**	-	**40**	
	t_{PHZ}, t_{PLZ}		Full	**6**	-	**38**	
Propagation Delay Time,[6] t_{RISE}/t_{FALL}	t_{THL} t_{TLH}	V_{DD} = 3.0V, V_{DIFF} = 2.5V	Full	**2**	-	**15**	ns
Input Capacitance[7]	C_{IN}	V_{DD} = open, f - 1MHz	Full	-	-	**12**	pF
Output Capacitance[7]	C_{OUT}	V_{DD} = open, f - 1MHz	Full	-	-	**12**	pF
Fail Safe	F_{SAFE}	+ and - Inputs are open, V_{OUT} = logic “1”	Full	**2.55**	-	-	V

1. Parameters with Min and/or Max Limits are 100% tested at -55°C, +25°C, and +125°C, unless otherwise specified.
2. Typical values are at 3.3V. Parameters with a supply entry in the typical column apply to 3.3V. Typical values shown are not guaranteed.
3. V_{IL} = 0.3V_{DD}, V_{IH} = 0.7V_{DD}.
4. This parameter tested as inputs for the V_{OL} and V_{OH} tests.
5. If not tested, it is guaranteed to the limits specified.
6. Reference EIA RS-422.
7. Parameter is guaranteed by design or process, but not tested.

3. Timing and Load Circuit Diagrams

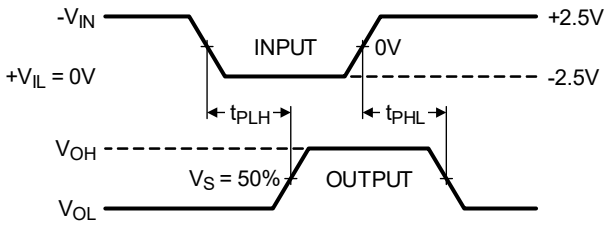
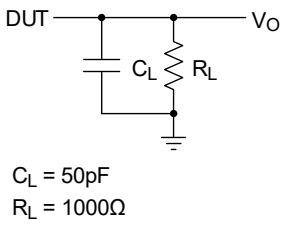
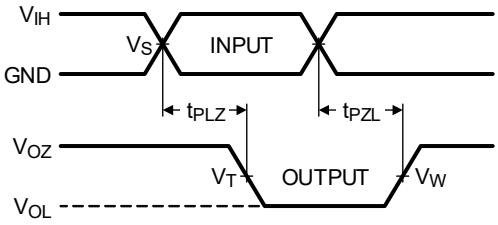


Figure 4. Propagation Delay Timing Diagram



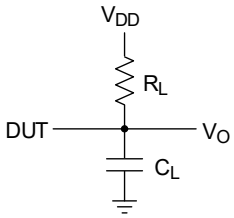
C_L = 50pF
R_L = 1000Ω

Figure 5. Propagation Delay Load Circuit



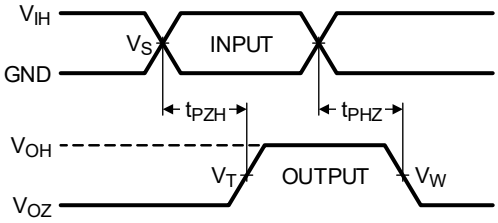
Note: Voltage Levels:
V_{DD} = 3.0V
V_{IH} = 3.0V
V_S = 50%
V_T = 50%
$V_W = V_{OL}$ + 0.5V
GND = 0V

Figure 6. Tri-State Low Timing Diagram



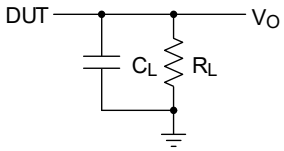
C_L = 50pF
R_L = 1000Ω

Figure 7. Tri-State Low Load Circuit



Note: Voltage Levels:
V_{DD} = 3.0V
V_{IH} = 3.0V
V_S = 50%
V_T = 50%
$V_W = V_{OH}$ - 0.5V
GND = 0V

Figure 8. Tri-State High Timing Diagram



C_L = 50pF
R_L = 1000Ω

Figure 9. Tri-State High Load Circuit

4. Die Characteristics

Table 2. Die and Assembly Related Information

Die Information	
Dimensions	78 mils x 123 mils x 19mils ±1mil (1981µm x 3124µm x 483µm ±25µm)
Interface Materials	
Glassivation	Type: PSG (Phosphorus Silicon Glass) Thickness: 8kÅ ±1kÅ
Metallization	M1: Mo/TiW (Bottom) Thickness: 5800Å ±1kÅ M2: AlSiCu (Top) Thickness: 10kÅ ±1kÅ
Substrate	AVLSI1RA
Backside Finish	Silicon
Assembly Information	
Substrate Potential (Powered Up)	Internally tied to V_{DD}
Additional Information	
Worst Case Current Density	< 2.0e5A/cm^2
Bond Pad Size	110µm x 100µm
Transistor Count	315

4.1 Metallization Mask Layout

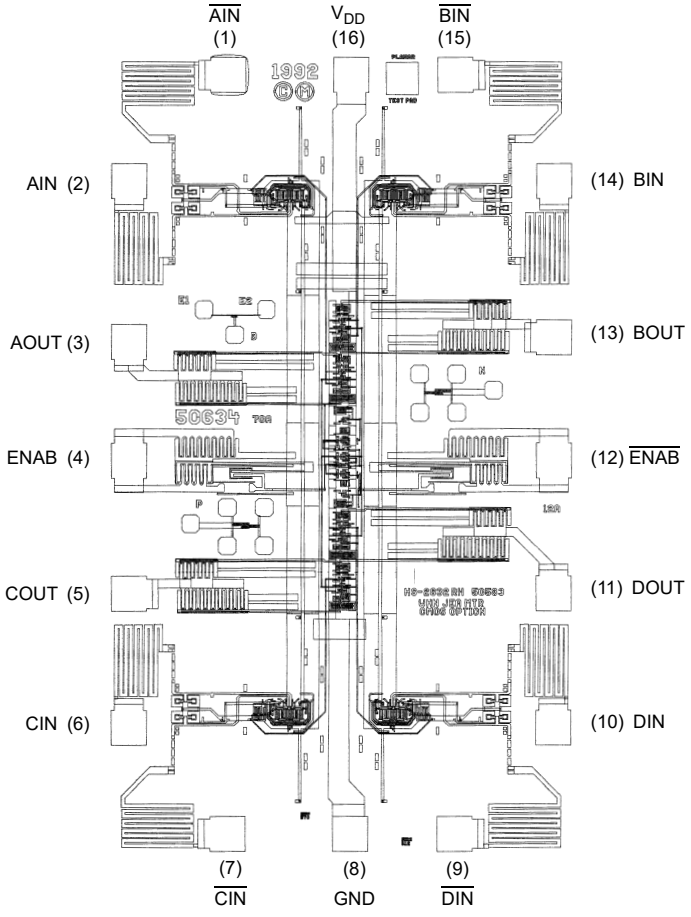


Table 3. HS-26CLV32RH, HS-26CLV32EH Pad Coordinates

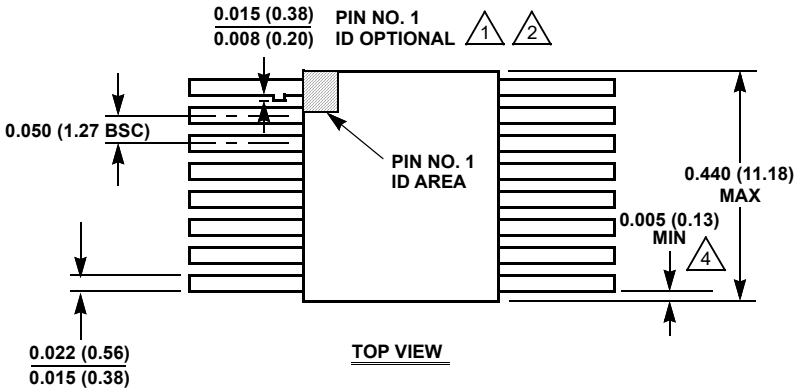
Pin Number	Pad Name	Relative to Pin 1[1]	
		X Coordinates	Y Coordinates
1	$\overline{AIN}$	0	0
2	AIN	-337.1	-362
3	AOUT	-337.1	-912.5
4	ENABLE	-337.1	-1319.3
5	COUT	-337.1	-1774.4
6	CIN	-337.1	-2233.7
7	$\overline{CIN}$	0	-2595.7
8	GND	418.4	-2596.7
9	$\overline{DIN}$	776.4	-2595.7
10	DIN	1113.5	-2233.7
11	DOUT	1113.5	-1774.4
12	$\overline{ENABLE}$	1113.5	-1319.3
13	BOUT	1113.5	-898.4
14	BIN	1113.5	-362
15	$\overline{BIN}$	776.4	0
16	V_{DD}	420.2	1

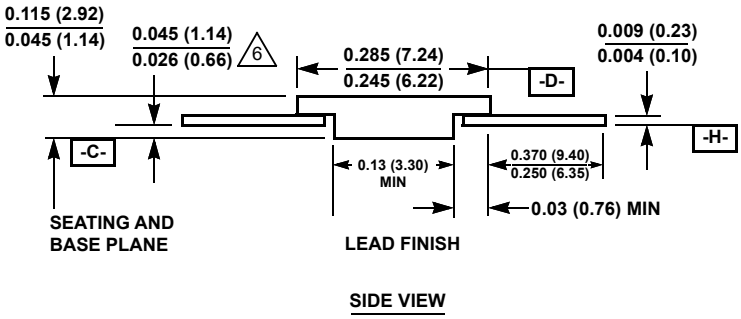
1. Dimensions in microns.

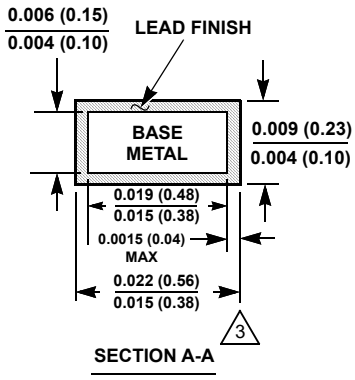
5. Package Outline Drawings

For the most recent package outline drawing, see K16.A.

16 Lead Ceramic Metal Seal Flatpack Package
Rev 2, 1/10





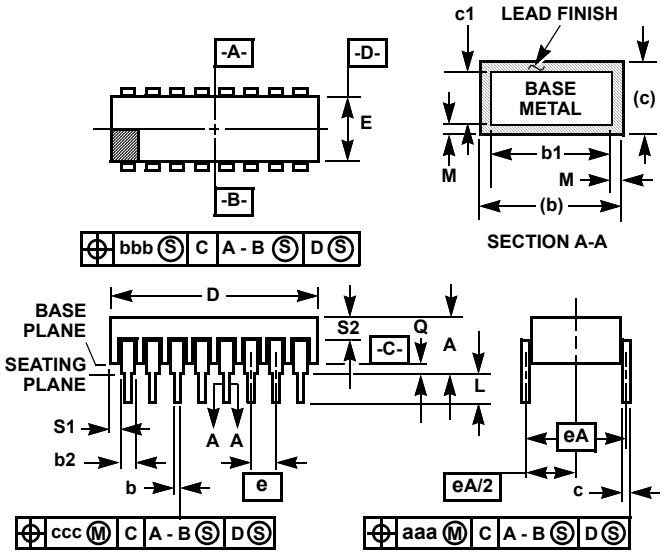


NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of the tab dimension do not apply.
3. The maximum limits of lead dimensions (section A-A) shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
4. Measure dimension at all four corners.
5. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
6. Dimension shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
7. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
8. Controlling dimension: INCH.

For the most recent package outline drawing, see D16.3.

Ceramic Dual-In-Line Metal Seal Packages (SBDIP)



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.

D16.3 MIL-STD-1835 CDIP2-T16 (D-2, CONFIGURATION C)
16 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	-
E	0.220	0.310	5.59	7.87	-
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	5
S1	0.005	-	0.13	-	6
S2	0.005	-	0.13	-	7
α	90º	105º	90º	105º	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	16		16		8

Rev. 0 4/94

6. Ordering Information

Ordering SMD Number[1]	Part Number[2]	Radiation Hardness (Total Ionizing Dose)	Package Description (RoHS Compliant)	Pkg. Dwg. #	Carrier Type	Temp. Range
5962F9568902QEC	HS1-26CLV32RH-8	HDR to 300krad(Si)	16 Ld SBDIP	D16.3	Tube	-55 to +125°C
5962F9568902QXC	HS9-26CLV32RH-8		16 Ld Flatpack	K16.A	Tray	-55 to +125°C
5962F9568902VEC	HS1-26CLV32RH-Q		16 Ld SBDIP	D16.3	Tube	-55 to +125°C
5962F9568902VXC	HS9-26CLV32RH-Q		16 Ld Flatpack	K16.A	Tray	-55 to +125°C
5962F9568902V9A	HS0-26CLV32RH-Q[3]		Die	N/A	N/A	-55 to +125°C
5962F9568902VYC	HS9G-26CLV32RH-Q[4]		16 Ld Flatpack	K16.A	Tray	-55 to +125°C
N/A	HS0-26CLV32RH/SAMPLE[3][5]	N/A	Die	N/A	N/A	-55 to +125°C
	HS1-26CLV32RH/PROTO[5]		16 Ld SBDIP	D16.3	Tube	-55 to +125°C
	HS9-26CLV32RH/PROTO[5]		16 Ld Flatpack	K16.A	Tray	-55 to +125°C
	HS9G-26CLV32RH/PROTO[4][5]		16 Ld Flatpack	K16.A	Tray	-55 to +125°C
5962F9568904VEC	HS1-26CLV32EH-Q	HDR to 300krad(Si) LDR to 50krad(Si)	16 Ld SBDIP	D16.3	Tube	-55 to +125°C
5962F9568904VXC	HS9-26CLV32EH-Q		16 Ld Flatpack	K16.A	Tray	-55 to +125°C
5962F9568904V9A	HS0-26CLV32EH-Q[3]		Die	N/A	N/A	-55 to +125°C
5962F9568904VYC	HS9G-26CLV32EH-Q[4]		16 Ld Flatpack	K16.A	Tray	-55 to +125°C

1. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed must be used when ordering.
2. These Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
3. Die product tested at T_A = + 25°C. The wafer probe test includes functional and parametric testing sufficient to make the die capable of meeting the electrical performance outlined in SMD.
4. The lid of these packages are connected to the ground pin of the device.
5. The /PROTO and /SAMPLE are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions across the temperature range specified in the DLA SMD and are in the same form and fit as the qualified device. The /SAMPLE parts are capable of meeting the electrical limits and conditions specified in the DLA SMD. The /SAMPLE parts do not receive 100% screening across temperature to the DLA SMD electrical limits. These part types do not come with a certificate of conformance because they are not DLA qualified devices.

7. Revision History

Revision	Date	Description
7.01	May 14, 2025	Applied latest template. Added Pin Information, ABS Max Ratings, Thermal Info, and Electrical Specifications sections. Updated timing and load circuit diagrams.
7.00	Oct 21, 2021	Removed Related Literature section. In Features section on page 1 added Radiation acceptance testing bullets for RH and EH parts. In Ordering Information table on page 2 verified the part numbers in the table are correct, added carrier type and radiation testing information columns, and re-ordered the notes in the table and added notes 3 and 5. Added Truth Table, Timing Diagrams, and Load Circuit Diagrams. Updated the Die Characteristics information as follows: -Changed the die thickness from: 21mils, to: 19mils -Updated Worst Case Current Density. -Added Transistor count. Removed About Intersil section.
6.00	Feb 6, 2017	Added Related Literature section. Updated Ordering Information table on page 2. Added Note 2 on page 2. Added Revision History and About Intersil sections. Added POD drawings.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.