HS-302AEH

Radiation Hardened BiCMOS Dual DPST Analog Switch

Description

The HS-302AEH is a dual Double-Pole, Single-Throw (DPST) analog switch fabricated using the Renesas dielectrically isolated Radiation Hardened Silicon Gate (RSG) process technology to ensure latch-up free operation. The HS-302AEH is pin compatible and functionally equivalent to the HS-302RH.

The HS-302AEH offers convenient switching controlled by 5V digital inputs and low-resistance switching performance for analog voltages up to the supply rails. ON-resistance is low and stays reasonably constant across the full range of operating voltage and current and as over exposure to radiation.

The HS-302AEH is available in a 14 Ld CDFP or die form and operates across the extended temperature range of -55°C to +125°C.

Applications

- Signal processing applications
- Power supply control

Features

- Qualified & Screened to DLA SMD 5962-95812
- No latch-up, dielectrically isolated device islands
- Pin and functionally compatible with Renesas HS-302RH series analog switches
- Analog signal range equal to the supply voltage range
- Low leakage: 150nA (maximum, post-rad)
- Low r_{ON}: 60Ω (maximum, post-rad)
- Low standby supply current: ±150µA (maximum, post-rad)
- TID Rad Hard Assurance (RHA) wafer-by-wafer testing
  - HDR (50rad(Si)/s to 300rad(Si)/s): 100krad(Si)
  - LDR (<0.01rad(Si)/s): 50krad(Si)
- Single event effects
  - SEE for LET = 60MeV·cm^2/mg at 60° incident angle, <150pC charge transferred to the output of an off switch (based on SOI design calculations)

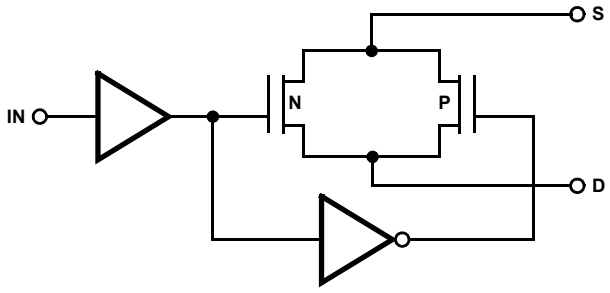


Figure 1. Logic Circuit

Table 1. Truth Table

Logic	All Switches
0	OFF
1	ON

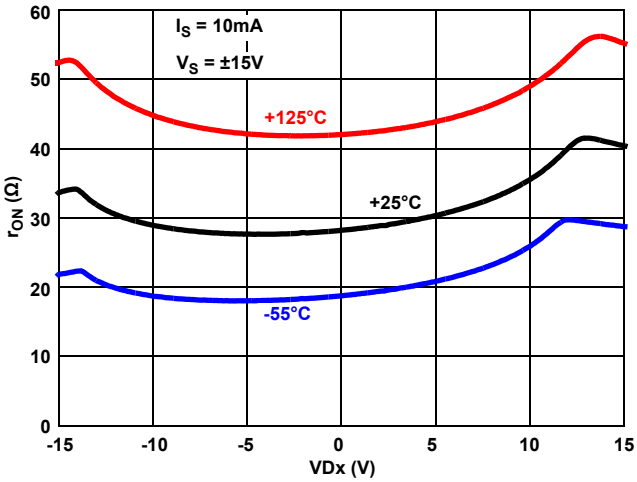


Figure 2. r_{ON} vs Signal Level vs Temperature

Contents

1. Pin Information

1.1 Pin Assignments

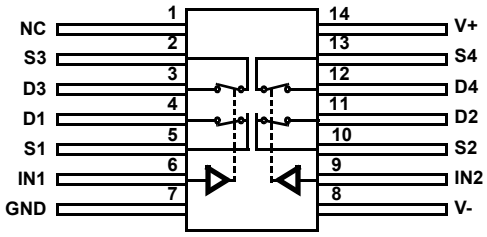


Figure 3. Pin Assignments - Top View

1.2 Pin Descriptions

Pin Number	Pin Name	Pin Description
1	NC	Not electrically connected
2	S3	Analog switch: source connection
5	S1	
10	S2	
13	S4	
3	D3	Analog switch: drain connection
4	D1	
11	D2	
12	D4	
6	IN1	Digital control input for SW1 and SW3
7	GND	Ground
8	V-	Negative power supply
9	IN2	Digital control input for SW2 and SW4
14	V+	Positive power supply
N/A	LID	Electrically floating

2. Specifications

2.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
Voltage Between V+ and V- Terminals	-	35	V
$\pm V_{SUPPLY}$ to Ground (V+, V-)	-	±17.5	V
Analog Input Voltage, ($+V_S$)	-	$+V_{SUPPLY}$ + 1.5	V
Analog Input Voltage, ($-V_S$)	-	$-V_{SUPPLY}$ - 1.5	V
Peak Current (S or D), (Pulse at 1ms, 10% Duty Cycle Max)	-	40	mA
Continuous Current	-	10	mA
Digital Input Voltage, ($+V_A$)	-	$+V_{SUPPLY}$ + 4	V
Digital Input Voltage, ($-V_A$)	-	$-V_{SUPPLY}$ - 4	V
Human Body Model (Tested per MIL-PRF-883 TM 3015.7)	-	2	kV
Machine Model (Tested per EIA/JESD22-A115-A)	-	200	V
Charged Device Model (Tested per JESD22-C101D)	-	1	kV

2.2 Thermal Information

Parameter	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance	Flatpack Package	θ_{JA}[1]	Junction to ambient	105	°C/W
		θ_{JC}[2]	Junction to case	17	°C/W

1. θ_{JA} is measured in free air with the component mounted on a low-effective thermal conductivity test board in free air. See TB379.
2. For θ_{JC}, the case temperature location is the center of the package underside.

Parameter	Minimum	Maximum	Unit
Package Power Dissipation at 125°C, Flatpack Package	-	0.48	W
Junction Temperature (T_J)	-	+175	°C
Storage Temperature Range	-65	+150	°C

2.3 Recommended Operation Conditions

Parameter	Minimum	Maximum	Unit
Operating Temperature Range	-55	+125	°C
Operating Supply Voltage Range ($\pm V_{SUPPLY}$)	-	±15	V
Analog Input Voltage (V_S)	-	$\pm V_{SUPPLY}$	V
Logic Low Level (V_{AL})	0	0.8	V
Logic High Level (V_{AH})	4.0	$+V_{SUPPLY}$	V

2.4 Electrical Specifications

V_{SUPPLY} = ±15V unless otherwise specified. **Boldface limits either apply across the operating temperature range -55°C to +125°C or across a total ionizing dose of 100krad(Si) with exposure of a high dose rate of 50 to 300rad(Si)/s and a total ionizing dose of 50krad(Si) with exposure at a low dose rate of <10mrad(Si)/s.**

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Switch On-Resistance	$+r_{DS(ON)}$	V_D = 10V, I_S = -10mA, T_A = +25°C	-	-	50	Ω
		T_A = -55°C to +125°C	-	35	**75**	Ω
		T_A = 25°C, post radiation	-	-	**60**	Ω
Switch On-Resistance	$-r_{DS(ON)}$	V_D = -10V, I_S = 10mA, T_A = +25°C	-	-	50	Ω
		T_A = -55°C to +125°C	-	35	**75**	Ω
		T_A = 25°C, post radiation	-	-	**60**	Ω
Leakage Current into Source Terminal of an OFF Switch	$+I_{S(OFF)}$	V_S = +14V, V_D = -14V, T_A = +25°C	-100	-	100	nA
		V_S = +14V, V_D = -14V, T_A = -55°C to +125°C	**-150**	0.05	**150**	nA
		V_S = +14V, V_D = -14V, T_A = +25°C, post radiation	**-150**	-	**150**	nA
		V_S = +15V, V_D = -15V, T_A = +25°C	-1	-	1	µA
		V_S = +15V, V_D = -15V, T_A = -55°C to +125°C	**-20**	-	**20**	µA
		V_S = +15V, V_D = -15V, T_A = +25°C, post radiation	**-20**	-	**20**	µA
Leakage Current into Source Terminal of an OFF Switch	$-I_{S(OFF)}$	V_S = -14V, V_D = +14V, T_A = +25°C	-100	-	100	nA
		V_S = -14V, V_D = +14V, T_A = -55°C to +125°C	**-150**	0.05	**150**	nA
		V_S = -14V, V_D = +14V, T_A = +25°C, post radiation	**-150**	-	**150**	nA
		V_S = -15V, V_D = +15V, T_A = +25°C	-1	-	1	µA
		V_S = -15V, V_D = +15V, T_A = -55°C to +125°C	**-20**	-	**20**	µA
		V_S = -15V, V_D = +15V, T_A = +25°C, post radiation	**-20**	-	**20**	µA
Leakage Current into Drain Terminal of an OFF Switch	$+I_{D(OFF)}$	V_S = +14V, V_D = -14V, T_A = +25°C	-100	-	100	nA
		V_S = +14V, V_D = -14V, T_A = -55°C to +125°C	**-150**	0.05	**150**	nA
		V_S = +14V, V_D = -14V, T_A = +25°C, post radiation	**-150**	-	**150**	nA
		V_S = +15V, V_D = -15V, T_A = +25°C	-1	-	1	µA
		V_S = +15V, V_D = -15V, T_A = -55°C to +125°C	**-20**	-	**20**	µA
		V_S = +15V, V_D = -15V, T_A = +25°C, post radiation	**-20**	-	**20**	µA
Leakage Current into Drain Terminal of an OFF Switch	$-I_{D(OFF)}$	V_S = -14V, V_D = +14V, T_A = +25°C	-100	-	100	nA
		V_S = -14V, V_D = +14V, T_A = -55°C to +125°C	**-150**	0.5	**150**	nA
		V_S = -14V, V_D = +14V, T_A = +25°C, post radiation	**-150**	-	**150**	nA
		V_S = -15V, V_D = +15V, T_A = +25°C	-1	-	1	µA
		V_S = -15V, V_D = +15V, T_A = -55°C to +125°C	**-20**	-	**20**	µA
		V_S = -15V, V_D = +15V, T_A = +25°C, post radiation	**-20**	-	**20**	µA
Leakage Current from an ON Driver into the Switch (Drain and Source)	$+I_{D(ON)}$	V_S = +14V, V_D = +14V, T_A = +25°C	-20	-	20	nA
		V_S = +14V, V_D = +14V, T_A = -55°C to +125°C	**-100**	-0.1	**100**	nA
		V_S = +14V, V_D = +14V, T_A = +25°C, post radiation	**-100**	-	**100**	nA

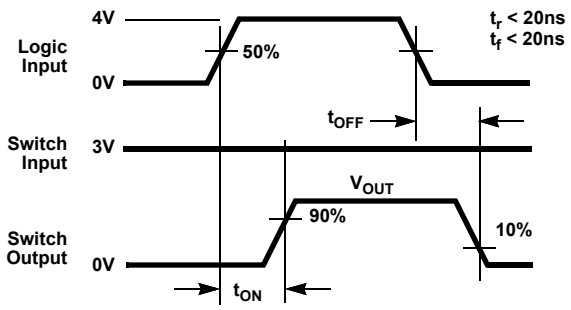
V_{SUPPLY} = ±15V unless otherwise specified. **Boldface limits either apply across the operating temperature range -55°C to +125°C or across a total ionizing dose of 100krad(Si) with exposure of a high dose rate of 50 to 300rad(Si)/s and a total ionizing dose of 50krad(Si) with exposure at a low dose rate of <10mrad(Si)/s. (Cont.)**

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Leakage Current from an ON Driver into the Switch (Drain and Source)	$-I_{D(ON)}$	V_S = -14V, V_D = -14V, T_A = +25°C	-20	-	20	nA
		V_S = -14V, V_D = -14V, T_A = -55°C to +125°C	**-100**	-0.1	**100**	nA
		V_S = -14V, V_D = -14V, T_A = +25°C, post radiation	**-100**	-	**100**	nA
Low Level Input Address Current	I_{AL}	All Channels V_A = 0.8V, T_A = -55°C to +125°C	**-1**	-	**1**	µA
		All Channels V_A = 0.8V, T_A = +25°C, post radiation	**-1**	-	**1**	µA
High Level Input Address Current	I_{AH}	All Channels V_A = 4.0V, T_A = -55°C to +125°C	**-1**	-	**1**	µA
		All Channels V_A = 4.0V, T_A = +25°C, post radiation	**-1**	-	**1**	µA
Positive Supply Current	I+	All Channels V_A = 0.8V, T_A = +25°C	-	-	100	µA
		All Channels V_A = 0.8V, T_A = -55°C to +125°C	-	45	**150**	µA
		All Channels V_A = 0.8V, T_A = +25°C, post radiation	-	-	**150**	µA
		V_{A1} = 0V, V_{A2} = 4V, V_{A1} = 4V, V_{A2} = 0V, T_A = +25°C	-	-	0.4	mA
		V_{A1} = 0V, V_{A2} = 4V, V_{A1} = 4V, V_{A2} = 0V, T_A = -55°C to +125°C	-	0.15	**0.6**	mA
		V_{A1} = 0V, V_{A2} = 4V, V_{A1} = 4V, V_{A2} = 0V, T_A = +25°C, post radiation	-	-	**0.6**	mA
Negative Supply Current	I-	All Channels V_A = 0.8V, T_A = +25°C	-	-	-10	µA
		All Channels V_A = 0.8V, T_A = -55°C to +125°C	-	-0.1	**-100**	µA
		All Channels V_A = 0.8V, T_A = +25°C, post radiation	-	-	**-100**	µA
		V_{A1} = 0V, V_{A2} = 4V, V_{A1} = 4V, V_{A2} = 0V, T_A = +25°C	-	-	-10	µA
		V_{A1} = 0V, V_{A2} = 4V, V_{A1} = 4V, V_{A2} = 0V, T_A = -55°C to +125°C	-	-0.1	**-100**	µA
		V_{A1} = 0V, V_{A2} = 4V, V_{A1} = 4V, V_{A2} = 0V, T_A = +25°C, post radiation	-	-	**-100**	µA
Switch Input Capacitance[2]	$C_{IS(OFF)}$	From Source to GND	-	-	28	pF
Driver Input Capacitance[2]	C_{C1}	V_A = 0V	-	-	10	pF
Driver Input Capacitance[2]	C_{C2}	V_A = 15V	-	-	10	pF
Switch Output[2]	C_{OS}	Measured Drain to GND	-	-	32	pF
Off Isolation[2]	V_{ISO}	V_{GEN} = $1V_{P-P}$, f = 1MHz	40	-	-	dB
Cross Talk[2]	V_{CR}	V_{GEN} = $1V_{P-P}$, f = 1MHz	40	-	-	dB
Charge Transfer Error[2]	V_{CTE}	V_S = GND, C_L= 0.01µF	-	-	15	mV
Switch Turn-On Time	t_{ON}	R_L = 300Ω, V_S = 3V, V_{AH} = 4V, V_{AL} = 0V, T_A = +25°C	-	-	375	ns
		T_A = -55°C to +125°C	-	250	**500**	ns
		T_A = +25°C, post radiation	-	-	**1**	µs
Switch Turn-Off Time	t_{OFF}	R_L = 300Ω, V_S = 3V, V_{AH} = 4V, V_{AL} = 0V	-	-	300	ns
		T_A = -55°C to +125°C	-	200	**450**	ns
		T_A = +25°C, post radiation	-	-	**1**	µs

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.
2. V_{AL} = 0V and V_{AH} = 4V.

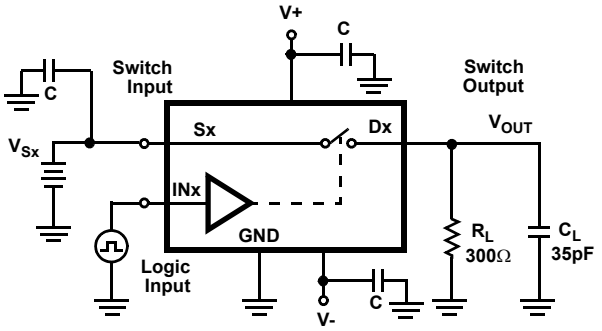
3. Test Circuits and Waveforms

3.1 Switching Times



Logic input waveform is inverted for switches that have the opposite logic sense.

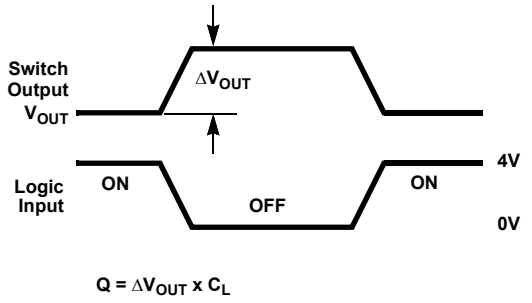
Figure 4. Switching Times Measurement Points



Repeat test for all switches. C_L includes fixture and stray capacitance.

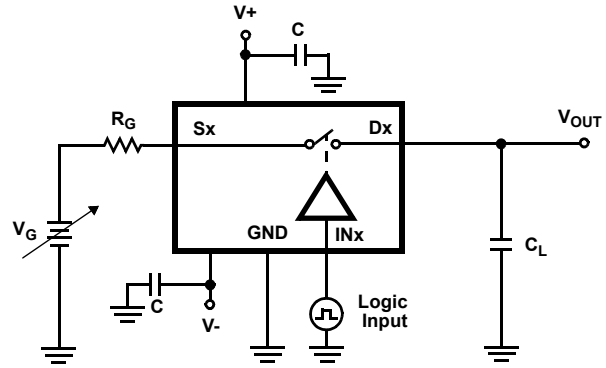
$$V_{OUT} = V_{(NO\ or\ NC)} \frac{R_L}{R_L + r_{ON}}$$

Figure 5. Switching Times Test Circuit



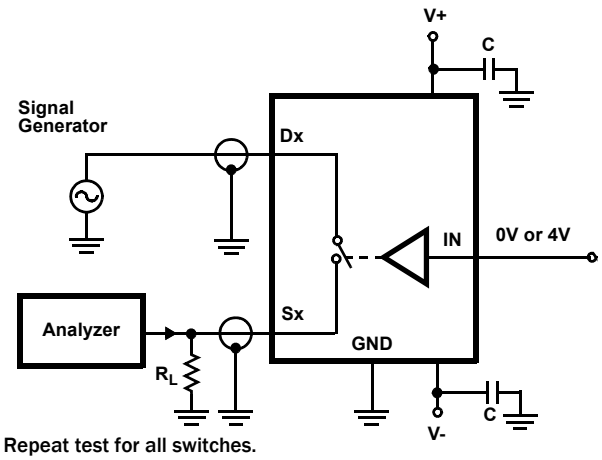
Logic input waveform is inverted for switches that have the opposite logic sense.

Figure 6. Charge Transfer Error Measurement Points



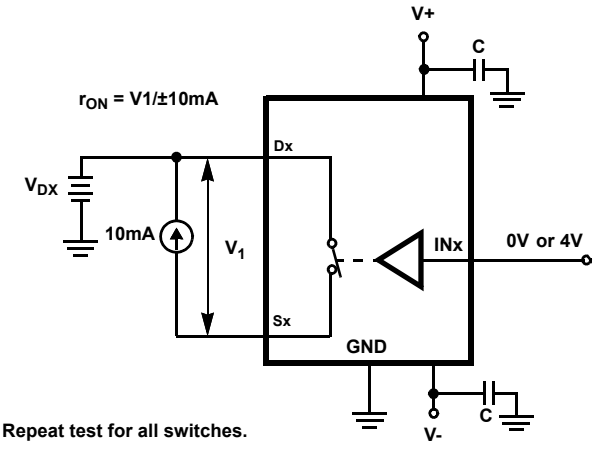
Repeat test for all switches. C_L includes fixture and stray capacitance.

Figure 7. Charge Transfer Error Test Circuit



Repeat test for all switches.

Figure 8. Off Isolation Test Circuit



Repeat test for all switches.

Figure 9. r_{ON} Test Circuit

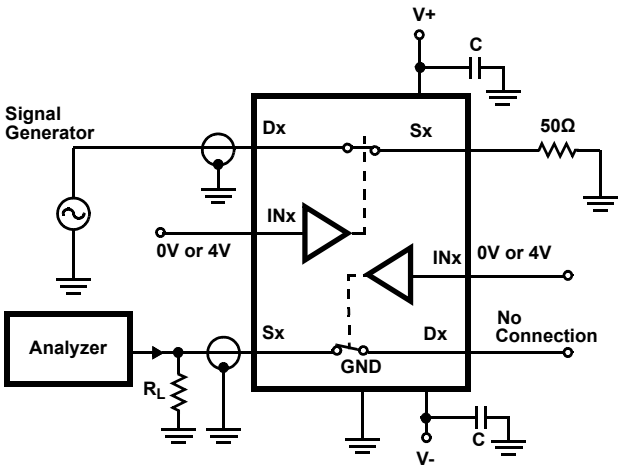


Figure 10. Crosstalk Test Circuit

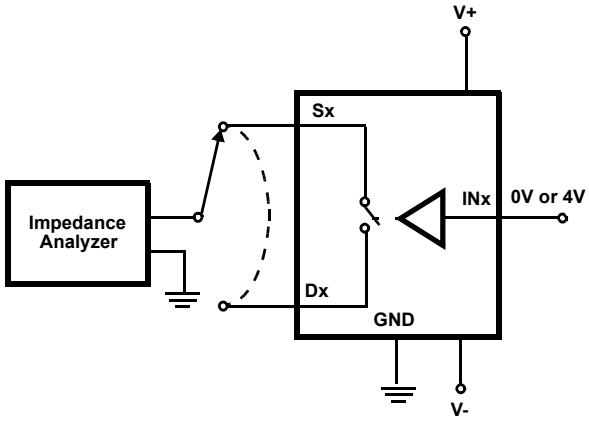


Figure 11. Capacitance Test Circuit

4. Typical Performance Curves

V_S = ±15V, V_{CM} = 0V, R_L = Open, T_A = +25°C, unless otherwise specified.

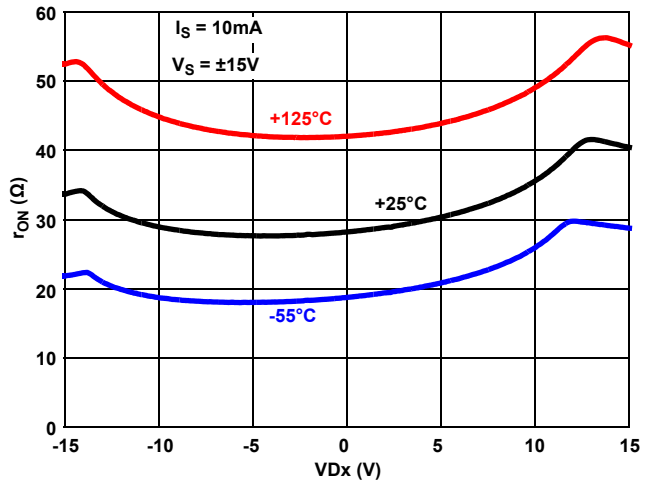


Figure 12. r_{ON} vs Signal Level vs Temperature

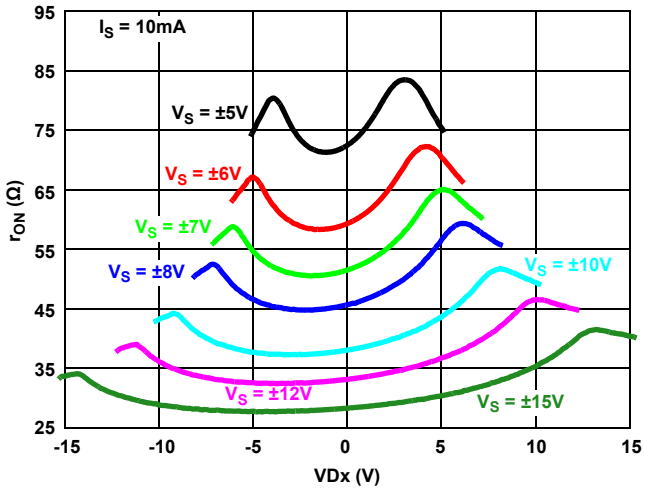


Figure 13. r_{ON} vs Signal Level vs Supply Voltages

V_S = ±15V, V_{CM} = 0V, R_L = Open, T_A = +25°C, unless otherwise specified. (Cont.)

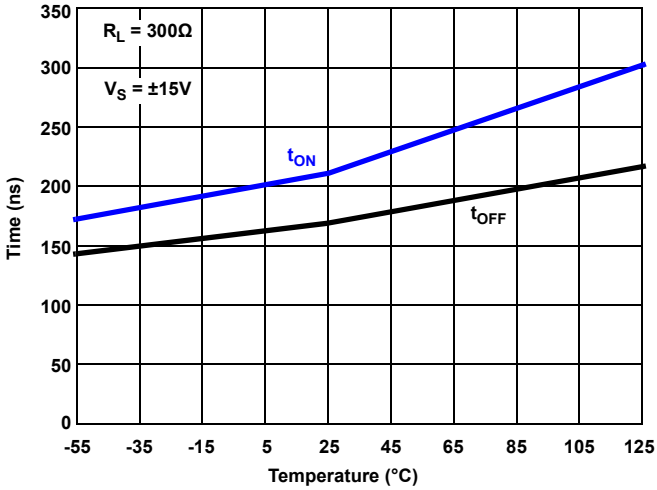


Figure 14. t_{ON} and t_{OFF} vs Temperature

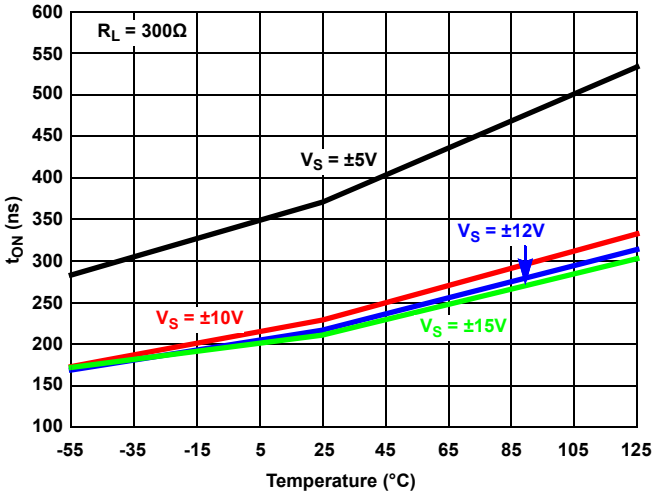


Figure 15. t_{ON} vs Temperature vs Supply Voltages

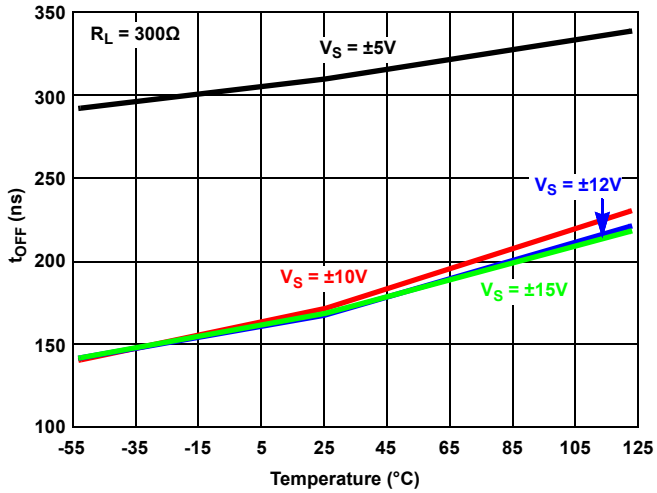


Figure 16. t_{OFF} vs Temperature vs Supply Voltages

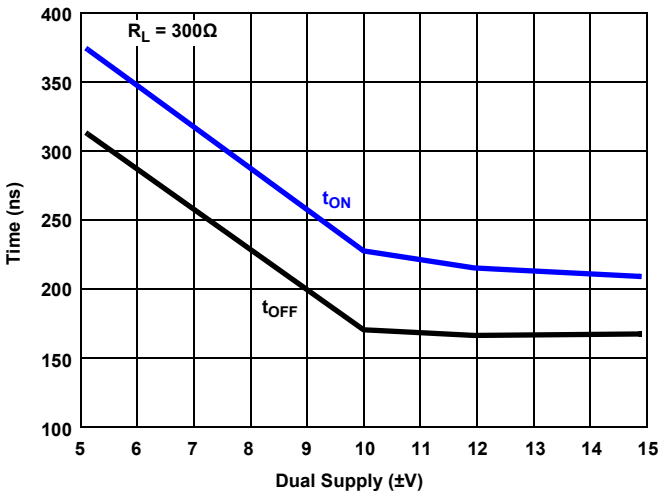


Figure 17. t_{ON} and t_{OFF} vs Temperature

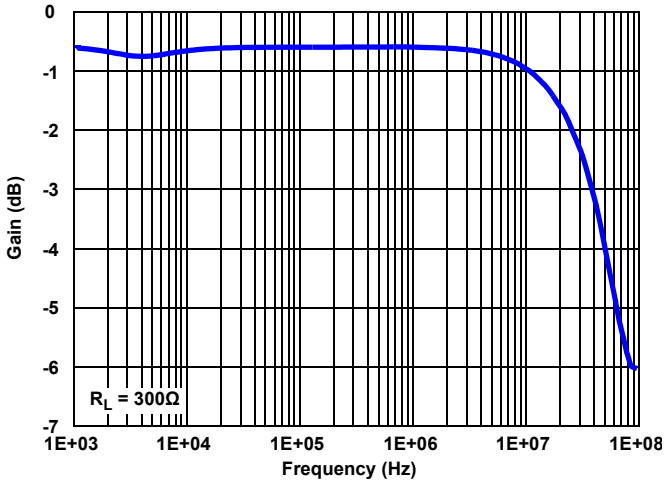


Figure 18. Frequency Response vs Frequency

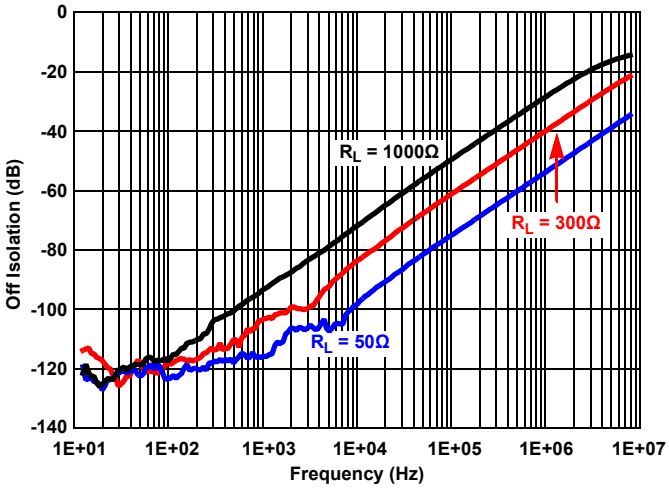


Figure 19. Off Isolation vs Frequency

V_S = ±15V, V_{CM} = 0V, R_L = Open, T_A = +25°C, unless otherwise specified. (Cont.)

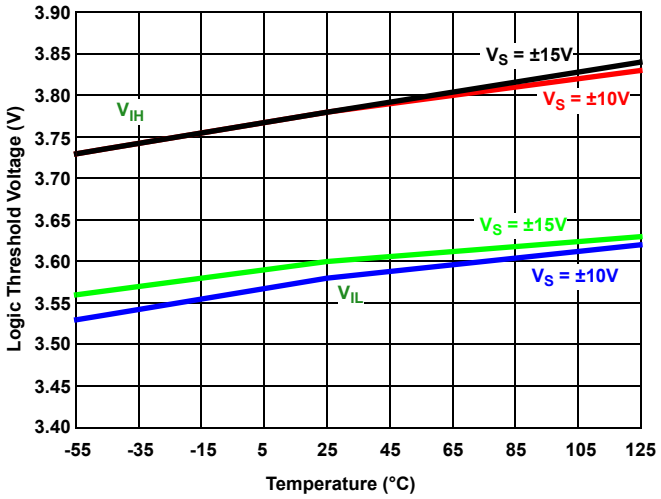


Figure 20. V_{IH} / V_{IL} vs Temperature vs Supply Voltages

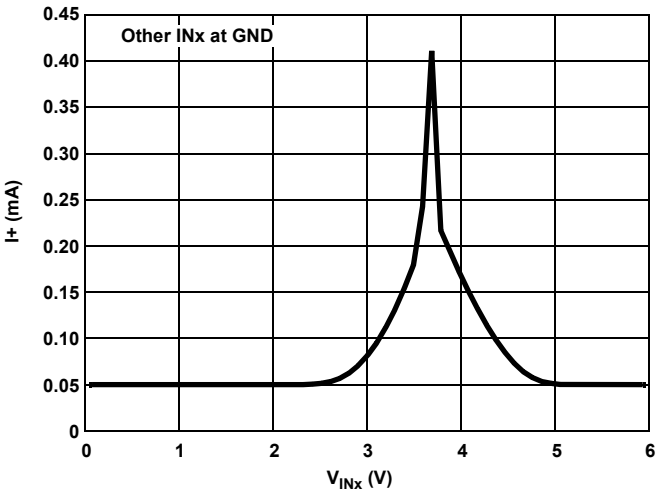


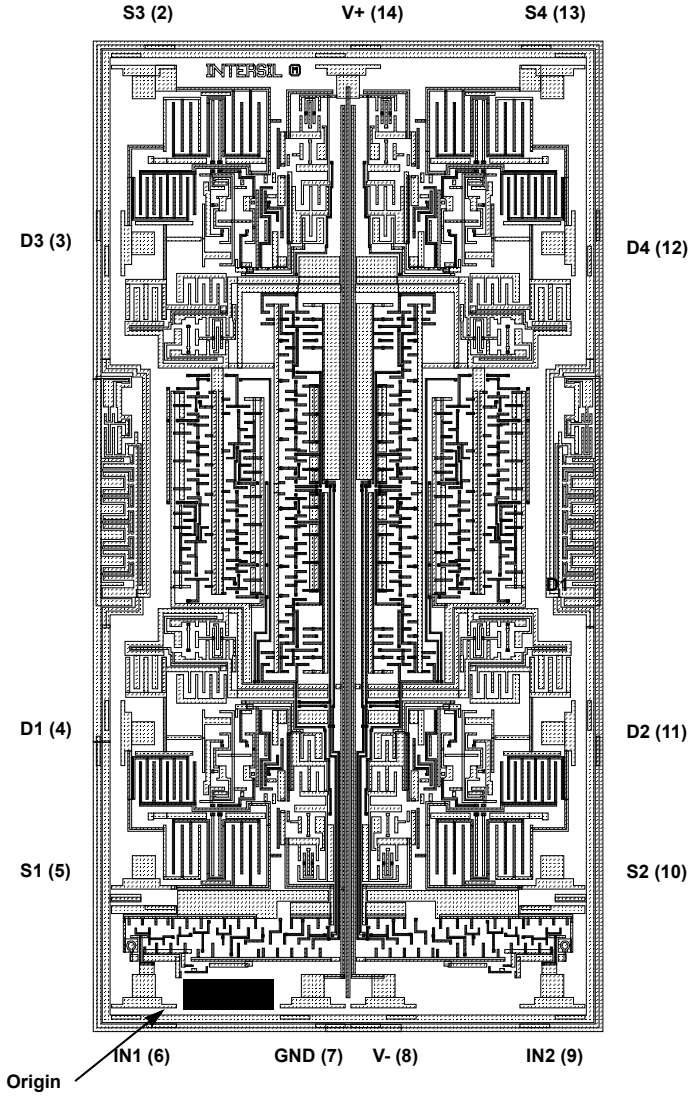
Figure 21. I+ vs Logic In

5. Die Characteristics

Table 2. Die and Assembly Related Information

Die Information	
Dimensions	2815µm x 5325µm (110.83mils x 209.65mils) Thickness: 483µm ±25.4µm (19 mils ±1 mil)
Interface Materials	
Glassivation	Type: PSG (Phosphorous Silicon Glass) Thickness: 8.0kÅ ±1.0kÅ
Top Metallization	Type: AlSiCu Thickness: 16.0kÅ ±2kÅ
Backside Finish	Silicon
Substrate	Radiation Hardened Silicon Gate, Dielectric Isolation
Assembly Information	
Substrate Potential	Unbiased (DI)
Additional Information	
Worst Case Current Density	<2.0 x 10^5 A/cm^2
Transistor Count	348
Package Lid Potential	Floating

6. Metallization Mask Layout



6.1 Layout Characteristics

Step and Repeat: 2815µmx5325µm

Table 3. Layout X-Y Coordinates

Pad Name	X (µm)	Y (µm)	DX (µm)	DY (µm)
S3	0	4672.5	109	109
D3	-4.5	3861	109	109
D1	-4.5	1314	109	109
S1	0	617.5	109	109
IN1[1]	0	0	109	109
GND	878	0	109	109
V-	1246	0	109	109
IN2	2124	0	109	109
S2	2124	617.5	109	109
D2	2128.5	1314	109	109
D4	2128.5	3861	109	109
S4	2124	4672	109	109
V+	1062	4675	109	109

1. Origin as labeled in the Metallization Mask layout is the centroid of the pad labeled IN1.

7. Package Outline Drawing

The package outline drawing is located at the end of this document and is accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

8. Ordering Information

Ordering SMD Number[1]	Part Number[2]	Radiation Hardness (Total Ionizing Dose)	Package Description (RoHS Compliant)	Pkg. Dwg. #	Carrier Type	Temp. Range
5962R9581205VXC	HS9-302AEH-Q	HDR to 100krad(Si) LDR to 50krad(Si)	14 Ld Flatpack	K14.A	Tray	-55 to +125°C
5962R9581205V9A	HS0-302AEH-Q[3]		Die	N/A	N/A	
N/A	HS9-302AEH/PROTO[4]	N/A	14 Ld Flatpack	K14.A	Tray	
N/A	HS0-302AEH/SAMPLE[3][4]		Die	N/A	N/A	

1. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed must be used when ordering.
2. These Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
3. Die product tested at T_A = + 25°C. The wafer probe test includes functional and parametric testing sufficient to make the die capable of meeting the electrical performance outlined in Electrical Specifications.
4. The /PROTO and /SAMPLE are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions across temperature specified in the DLA SMD and are in the same form and fit as the qualified device. The /SAMPLE parts are capable of meeting the electrical limits and conditions specified in the DLA SMD. The /SAMPLE parts do not receive 100% screening across temperature to the DLA SMD electrical limits. These part types do not come with a Certificate of Conformance because they are not DLA qualified devices.

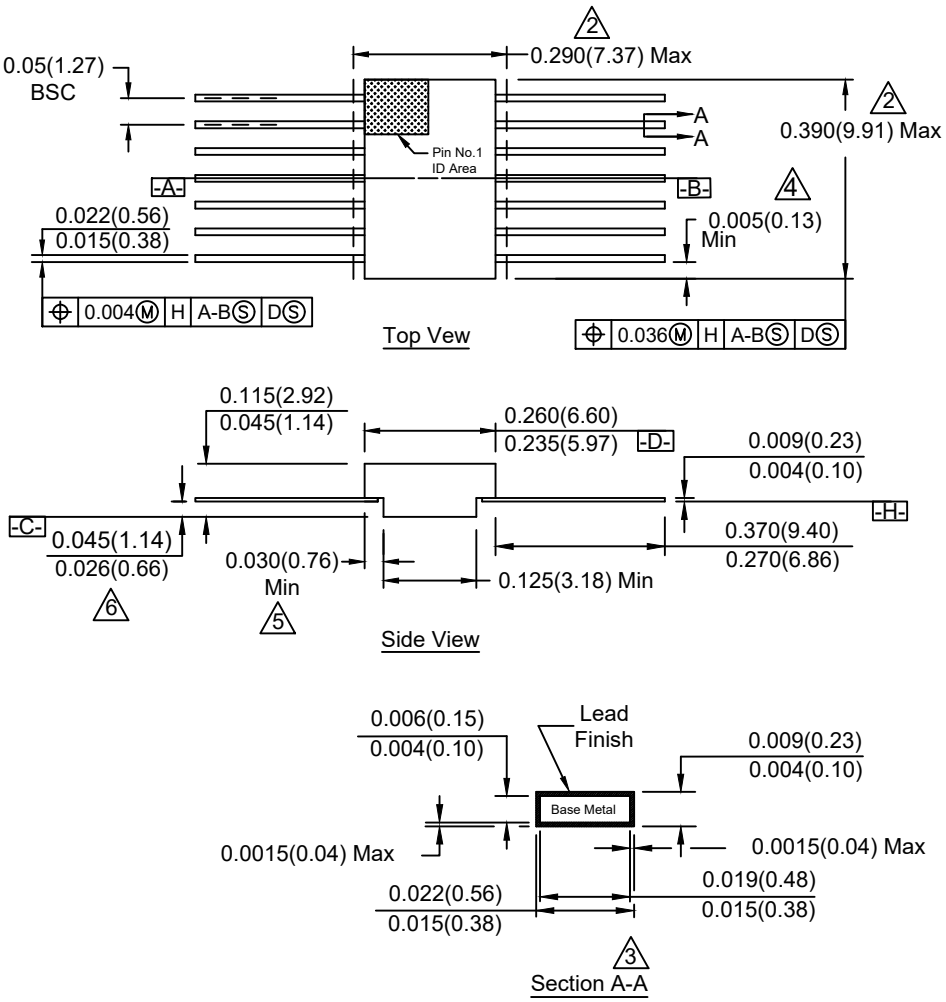
9. Revision History

Revision	Date	Change
3.01	Mar 14, 2025	Applied the latest template. Updated Feature bullet. Updated Ordering Information table. Updated POD to the latest version; changes are as follows: ▪ Applied latest template ▪ Corrected typo in the mm value for dimension E1 from 7.11 to 7.37mm ▪ Corrected typo in the dimension of the bottom ceramic pedestal width.
3.00	Jul 7, 2021	Removed Related Literature section. Updated Ordering information table format, added Rad hard information, and updated notes. On page 11 in table 2, Die Characteristics in the Dimensions row change from (106mils x 205mils) to (110.83mils x 209.65mils).
2.00	Jul 18, 2019	Updated single event effects information on page 1. Updated links. Removed About Intersil section. Applied new template.
1.00	Mar 17, 2017	Changed the title from “CMOS” to “BiCMOS” Added “Related Literature” section Added Note 5.
0.00	Jul 15, 2016	Initial release

Package Outline Drawing

14 Lead Ceramic Metal Seal Flatpack Package

POD Number: K14.A, Revision no: 02, Date Created: Mar 4, 2025



Notes:

1 Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacture's identification shall not be used as a pin one identification mark.

2 This dimension allows for off-center lid, meniscus, and glass overrun.

3 The maximum limits of lead dimensions (section A-A) shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate finish is applied.

4 Measure dimension at all four corners.

5 For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.

6 This dimension shall be measured at the point of exit (beyond the meniscus) of the lead from the body. This dimension's minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.

7. Dimensioning and tolerancing per ANSI Y14.5M - 1982.

8. Dimensions: INCH(mm). Controlling dimension: INCH.

9. Compliant to MIL-STD-1835 CDFP3-F14 (F-2A, CONFIGURATION B).

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