HS-5104ARH, HS-5104AEH

Radiation Hardened, Low Noise Quad Operational Amplifiers

The HS-5104ARH, HS-5104AEH are radiation hardened, monolithic quad operational amplifiers that provide highly reliable performance in harsh radiation environments. Excellent noise characteristics coupled with a unique array of dynamic specifications make these amplifiers well-suited for a variety of satellite system applications. Dielectrically isolated, bipolar processing makes these devices immune to Single Event Latch-Up.

The HS-5104ARH, HS-5104AEH show almost no change in offset voltage after exposure to 100kRAD(Si) gamma radiation, with only a minor increase in current. Complementing these specifications is a post radiation open loop gain in excess of 40k.

These quad operational amplifiers are available in an industry standard pinout, allowing for immediate interchangeability with most other quad operational amplifiers.

The HS-5104AEH replaces the obsoleted HS-5104ARH.

Features

- Electrically screened to SMD # 5962-95690
- QML qualified per MIL-PRF-38535 requirements
- Radiation acceptance testing - HS-5104AEH
  - High dose rate (50-300rad(Si)/s). . . . . 100krad(Si)
  - Low dose rate (0.01rad(Si)/s) . . . . . .50krad(Si)
- Radiation acceptance testing - HS-5104ARH
  - High dose rate (50-300rad(Si)/s). . . . . 100krad(Si)
- No latch-up, dielectrically isolated device islands
- Low noise
  - At 1kHz . . . . . .4.3nV/$\sqrt{Hz}$ (Typ)
  - At 1kHz . . . . . .0.6pA/$\sqrt{Hz}$ (Typ)
- Low offset voltage . . . . . .3.0mV (Max)
- High slew rate . . . . . 2.0V/µs (Typ)
- Gain bandwidth product . . . . . 8.0MHz (Typ)

Applications

- High Q, active filters
- Voltage regulators
- Integrators
- Signal generators
- Voltage references
- Space environment

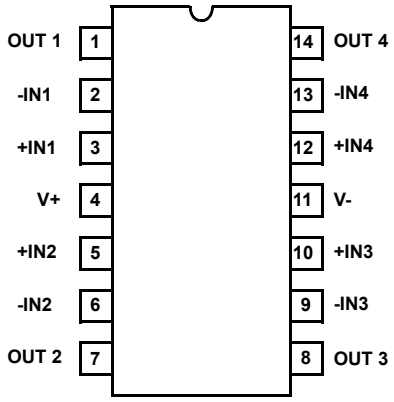
Ordering Information

ORDERING/SMD NUMBER (Note 1)	INTERNAL MKT. NUMBER (Note 2)	RADIATION HARDNESS (Total Ionizing Dose)	PACKAGE DESCRIPTION (RoHS Compliant)	PKG. DWG. #	CARRIER TYPE	TEMP. RANGE
5962R9569002VXC	HS9-5104AEH-Q	HDR to 100krad(Si), LDR to 50krad(Si)	14 Ld Flatpack	K14.A	Tray	-55 to +125°C
5962R9569002VCC	HS1-5104AEH-Q		14 Ld SBDIP	D14.3	Tube	-55 to +125°C
5962R9569002V9A	HS0-5104AEH-Q (Note 3)		Die	-	-	-55 to +125°C
N/A	HS1-5104AEH/PROTO (Note 4)	N/A	14 Ld SBDIP	D14.3	Tube	-55 to +125°C
	HS0-5104AEH/SAMPLE (Notes 3, 4)		Die	-	-	-55 to +125°C
	HS9-5104AEH/PROTO (Note 4)		14 Ld Flatpack	K14.A	Tray	-55 to +125°C
5962R9569001VXC	HS9-5104ARH-Q **No longer available or supported**	HDR to 100krad(Si)	14 Ld Flatpack	K14.A	Tray	-55 to +125°C
5962R9569001VCC	HS1-5104ARH-Q **No longer available or supported**		14 Ld SBDIP	D14.3	Tube	-55 to +125°C
5962R9569001V9A	HS0-5104ARH-Q (Note 3) **No longer available or supported**		Die	-	-	-55 to +125°C
NA	HS1-5104ARH/PROTO (Note 4) **No longer available or supported**	N/A	14 Ld SBDIP	D14.3	Tube	-55 to +125°C
	HS0-5104ARH/SAMPLE (Notes 3, 4) **No longer available or supported**		Die	-	-	-55 to +125°C
	HS9-5104ARH/PROTO (Note 4) **No longer available or supported**		14 Ld Flatpack	K14.A	Tray	-55 to +125°C

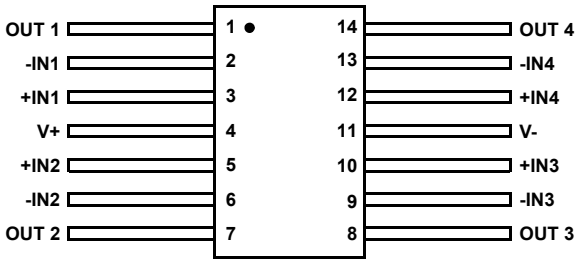
1. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed must be used when ordering.
2. These Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
3. Die product tested at T_A = + 25°C. The wafer probe test includes functional and parametric testing sufficient to make the die capable of meeting the electrical performance outlined in the SMD.
4. The /PROTO and /SAMPLE are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions across temperature specified in the DLA SMD and are in the same form and fit as the qualified device. The /SAMPLE parts are capable of meeting the electrical limits and conditions specified in the DLA SMD. The /SAMPLE parts do not receive 100% screening across temperature to the DLA SMD electrical limits. These part types do not come with a Certificate of Conformance because they are not DLA qualified devices.

Pin Configuration

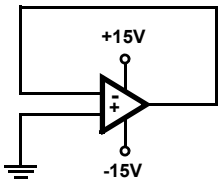
HS1-5104ARH, HS1-5104AEH
(14 LD SBDIP)
TOP VIEW



HS9-5104ARH, HS9-5104AEH
(14 LD FLATPACK)
TOP VIEW



Irradiation Circuit

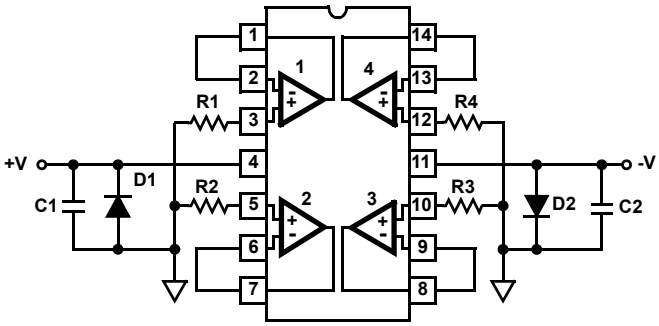


(ONE OF FOUR)

NOTES:

5. +V = 15V
6. -V = -15V
7. Group E Sample Size = 4 Die Per Wafer

Burn In Circuit



NOTES:

8. R1 = R2 = R3 = R4 = 1MW, 5%, 1/4W (Min)
9. C1 = C2 = 0.01µF/Socket (Min) or 0.1µF/Row (Min)
10. D1 = D2 = IN4002 or Equivalent/Board
11. |(V+) - (V-)| = 31V ±1V

Die Characteristics

DIE DIMENSIONS:

95 mils x 99 mils x 19 mils ±1 mils (2420µm x 2530µm x 483µm ±25.4µm)

INTERFACE MATERIALS:

Glassivation:

Type: Silox (SIO2) 1:6:1
Thickness: 8kÅ ±0.8kÅ (1kÅ undopped, 6kÅ dopped, cap 1kÅ undopped)

Top Metalization:

Type: Al/Cu 16kÅ ±2kÅ

Substrate:

HFSTD: Single poly dielectrically isolated complementary bipolar.

Backside Finish:

Silicon

ASSEMBLY RELATED INFORMATION:

Substrate potential:

Insulator

Special assembly instructions:

None

ADDITIONAL INFORMATION:

Worst Case Current Density:

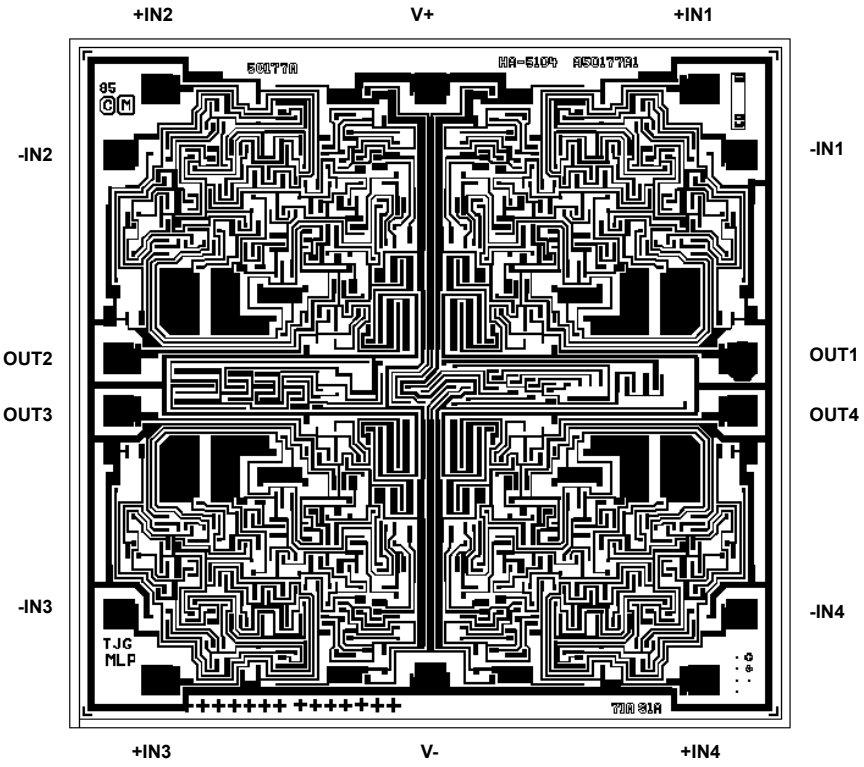
$< 2.0 \times 10^5$ A/cm^2

Transistor Count:

175

Metalization Mask Layout

HS-5104ARH, HS-5104AEH



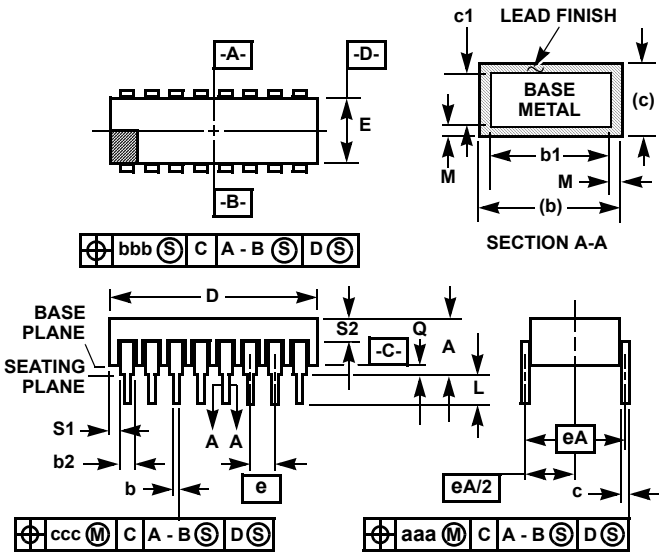
Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

Revision History

REVISION	DATE	DESCRIPTION
6.01	May 19, 2025	Updated POD K14.A to the latest version; changes are as follows: -Applied latest template -Corrected typo in the mm value for dimension E1 from 7.11 to 7.37mm
6.00	May 18, 2021	Updated Radiation Acceptance testing features bullets. Updated the Ordering Information table. Updated Die Characteristics for Glassivation, Top Metalization, Substrate, and Assembly Related Information. Added Revision History.

Ceramic Dual-In-Line Metal Seal Packages (SBDIP)



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.

D14.3 MIL-STD-1835 CDIP2-T14 (D-1, Configuration C)
14 Lead Ceramic Dual In-Line Metal Seal Package

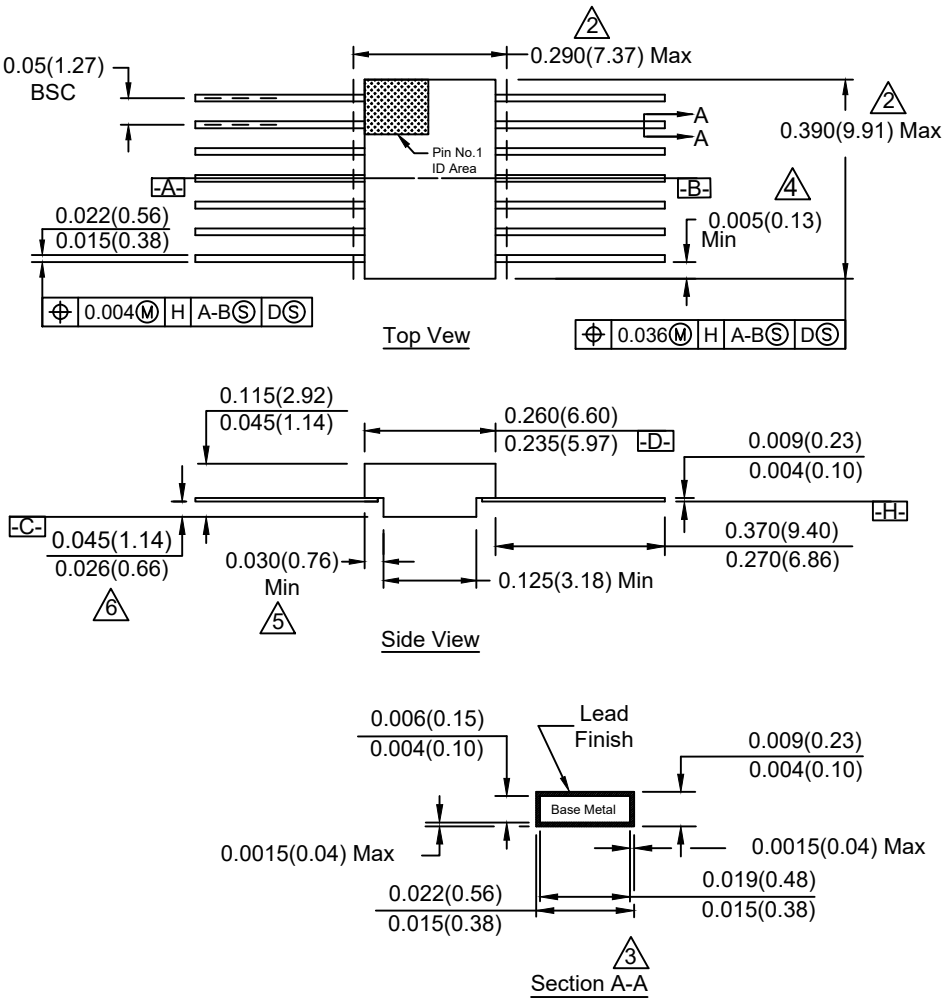
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.785	-	19.94	-
E	0.220	0.310	5.59	7.87	-
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	5
S1	0.005	-	0.13	-	6
S2	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	14		14		8

Rev. 0 4/94

Package Outline Drawing

14 Lead Ceramic Metal Seal Flatpack Package

POD Number: K14.A, Revision no: 02, Date Created: Mar 4, 2025



Notes:

1 Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacture's identification shall not be used as a pin one identification mark.

2 This dimension allows for off-center lid, meniscus, and glass overrun.

3 The maximum limits of lead dimensions (section A-A) shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate finish is applied.

4 Measure dimension at all four corners.

5 For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.

6 This dimension shall be measured at the point of exit (beyond the meniscus) of the lead from the body. This dimension's minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.

7. Dimensioning and tolerancing per ANSI Y14.5M - 1982.

8. Dimensions: INCH(mm). Controlling dimension: INCH.

9. Compliant to MIL-STD-1835 CDFP3-F14 (F-2A, CONFIGURATION B).

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