General Description

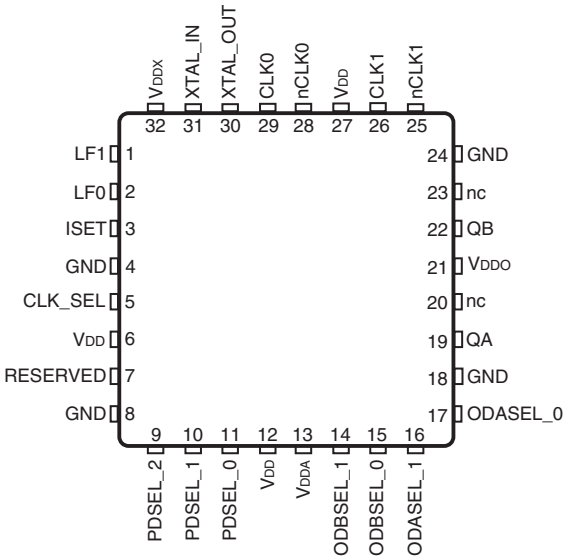
The ICS810N252I-02 device uses IDT's fourth generation FemtoClock® NG technology for optimal high clock frequency and low phase noise performance, combined with a low power consumption and high power supply noise rejection. The ICS810N252I-02 is a PLL based synchronous multiplier that is optimized for PDH or SONET to Ethernet clock jitter attenuation and frequency translation.

The ICS810N252I-02 contains two internal frequency multiplication stages that are cascaded in series. The first stage is a jitter attenuator, capable of jitter attenuation down to 10Hz using the external loop filter. The second stage is a FemtoClock NG® frequency multiplier that provides the low jitter, high frequency Ethernet output clock that easily meets Gigabit and 10 Gigabit Ethernet jitter requirements. Pre-divider and output divider multiplication ratios are selected using device selection control pins. The multiplication ratios are optimized to support most common clock rates used in PDH, SONET and Ethernet applications. The device requires the use of an external, inexpensive fundamental mode 27MHz crystal. The device is packaged in a space-saving 32-VFQFN package and supports industrial temperature range.

Features

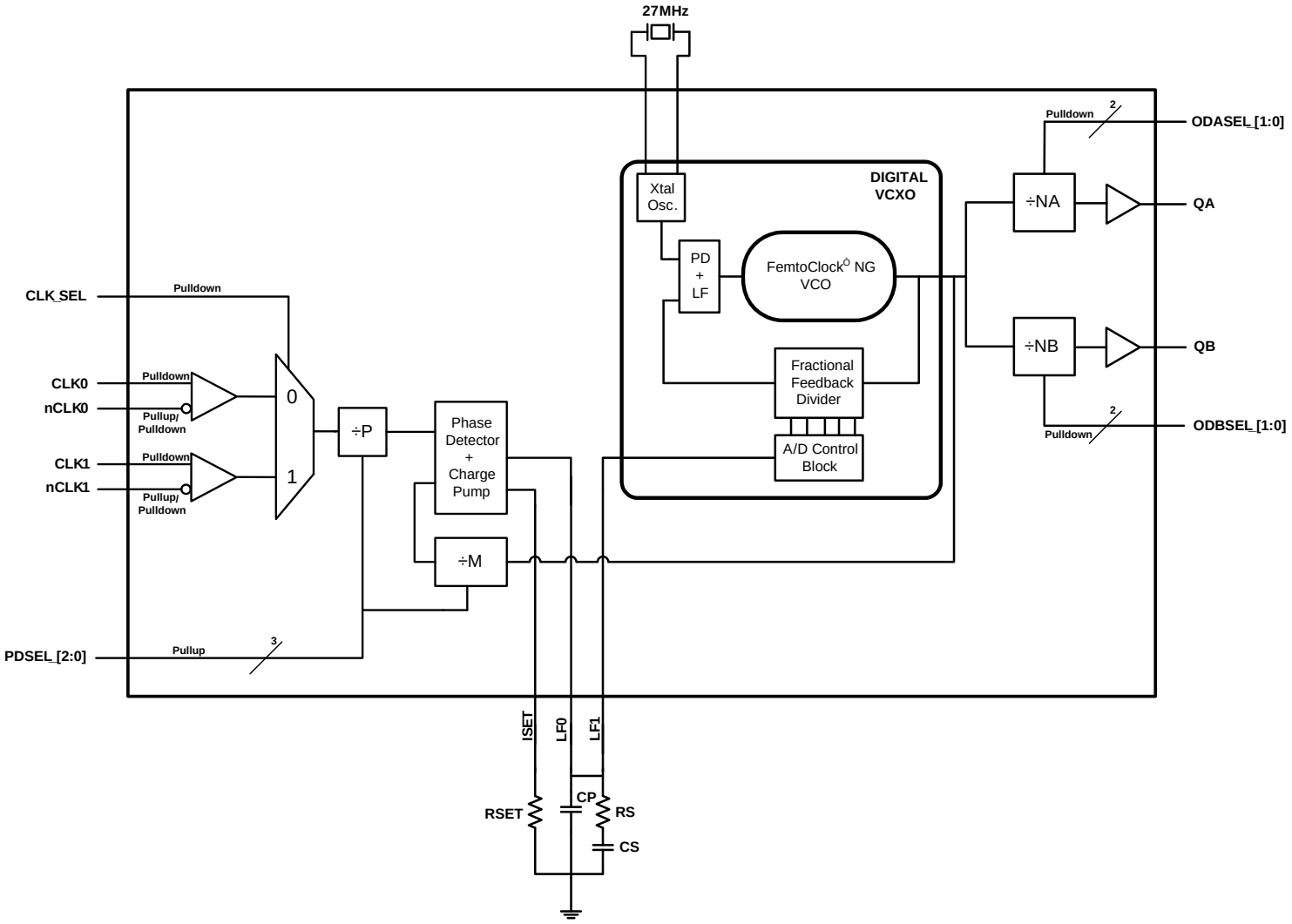
- Fourth generation FemtoClock® NG technology
- Two single-ended LVCMOS/LVTTL outputs
- Each output supports independent frequency selection at 25MHz, 125MHz, 156.25MHz and 312.5MHz
- Two differential inputs support the following input types: LVPECL, LVDS, LVHSTL, HCSL
- Accepts input frequencies from 8kHz to 155.52MHz including 8kHz, 1.544MHz, 2.048MHz, 19.44MHz, 25MHz, 77.76MHz, 125MHz and 155.52MHz
- Crystal interface designed for a 27MHz crystal
- Attenuates the phase jitter of the input clock by using a low-cost fundamental mode crystal
- Customized settings for jitter attenuation and reference tracking using an external loop filter connection
- FemtoClock NG frequency multiplier provides low jitter, high frequency output
- Absolute pull range: ±50ppm
- Power supply noise ratio (PSNR): -85dB
- FemtoClock NG VCO frequency: 625MHz
- RMS phase jitter @ 125MHz, using a 27MHz crystal (12kHz – 20MHz): 0.67ps (typical)
- 3.3V supply voltage
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Pin Assignment



ICS810N252I-02
32 Lead VFQFN
5mm x 5mm x 0.925mm package body
3.15mm x 3.15mm ePad size
K Package
Top View

Block Diagram



Pin Description and Pin Characteristic Tables

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2	LF1, LF0	Analog Input/Output		Loop filter connection node pins. LF0 is the output. LF1 is the input.
3	ISET	Analog Input/Output		Charge pump current setting pin.
4, 8, 18, 24	GND	Power		Power supply ground.
5	CLK_SEL	Input	Pulldown	Input clock select. When HIGH selects CLK1, nCLK1. When LOW, selects CLK0, nCLK0. LVCMOS / LVTTL interface levels.
6, 12, 27	V_{DD}	Power		Core supply pins.
7	RESERVED	Reserve		Reserved pin.
9, 10, 11	PDSEL_2, PDSEL_1, PDSEL_0	Input	Pullup	Pre-divider select pins. LVCMOS/LVTTL interface levels. See Table 3A.
13	V_{DDA}	Power		Analog supply pin.
14, 15	ODBSEL_1, ODBSEL_0	Input	Pulldown	Frequency select pins for Bank B output. See Table 3B. LVCMOS/LVTTL interface levels.
16, 17	ODASEL_1, ODASEL_0	Input	Pulldown	Frequency select pins for Bank A output. See Table 3B. LVCMOS/LVTTL interface levels.
19	QA	Output		Single-ended Bank A clock output. LVCMOS/LVTTL interface levels.
20, 23	nc	Unused		No connect.
21	V_{DDO}	Power		Output supply pin.
22	QB	Output		Single-ended Bank B clock output. LVCMOS/LVTTL interface levels.
25	nCLK1	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{DD}/2$ bias voltage when left floating.
26	CLK1	Input	Pulldown	Non-inverting differential clock input.
28	nCLK0	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{DD}/2$ bias voltage when left floating.
29	CLK0	Input	Pulldown	Non-inverting differential clock input.
30, 31	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input. XTAL_OUT is the output.
32	V_{DDX}	Power		Power supply pin for crystal oscillator.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			3.5		pF
C_{PD}	Power Dissipation Capacitance (per output)	V_{DDO} = 3.465V		8		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{OUT}	Output Impedance	V_{DDO} = 3.3V		14		Ω

Function Tables

Table 3A. Pre-Divider Selection Function Table

Inputs			Pre-Divider Value
PDSEL_2	PDSEL_1	PDSEL_0	
0	0	0	1
0	0	1	193
0	1	0	256
0	1	1	1944
1	0	0	2500
1	0	1	7776
1	1	0	12500
1	1	1	15552 (default)

Table 3B. Output Divider Function Table

Inputs		Output Divider Value
ODxSEL_1	ODxSEL_0	
0	0	25 (default)
0	1	5
1	0	4
1	1	2

Table 3C. Frequency Function Table

Input Frequency (MHz)	Pre-Divider Value	VCXO Frequency (MHz)	FemtoClock Feedback Divider Value	FemtoClock VCO Frequency (MHz)	Output Divider Value	Output Frequency (MHz)
0.008	1	27	25	625	25	25
0.008	1	27	25	625	5	125
0.008	1	27	25	625	4	156.25
0.008	1	27	25	625	2	312.5
1.544	193	27	25	625	25	25
1.544	193	27	25	625	5	125
1.544	193	27	25	625	4	156.25
1.544	193	27	25	625	2	312.5
2.048	256	27	25	625	25	25
2.048	256	27	25	625	5	125
2.048	256	27	25	625	4	156.25
2.048	256	27	25	625	2	312.5
19.44	1944	27	25	625	25	25
19.44	1944	27	25	625	5	125
19.44	1944	27	25	625	4	156.25
19.44	1944	27	25	625	2	312.5
25	2500	27	25	625	25	25
25	2500	27	25	625	5	125
25	2500	27	25	625	4	156.25
25	2500	27	25	625	2	312.5
77.76	7776	27	25	625	25	25
77.76	7776	27	25	625	5	125
77.76	7776	27	25	625	4	156.25
77.76	7776	27	25	625	2	312.5
125	12500	27	25	625	25	25
125	12500	27	25	625	5	125
125	12500	27	25	625	4	156.25
125	12500	27	25	625	2	312.5
155.52	15552	27	25	625	25	25
155.52	15552	27	25	625	5	125
155.52	15552	27	25	625	4	156.25
155.52	15552	27	25	625	2	312.5

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	3.63V
Inputs, V_I	-0.5V to V_{DD}+ 0.5V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	33.1°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. LVPECL Power Supply DC Characteristics, $V_{DD} = V_{DDO} = V_{DDX} = 3.3V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage	PLL Mode	V_{DD} – 0.30	3.3	V_{DD}	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
V_{DDX}	Crystal Oscillator Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				230	mA
I_{DDA}	Analog Supply Current	V_{DDA} = HIGH			30	mA
I_{DDO}	Output Supply Current	V_{DDA} = LOW, PDSEL[2:0] = 000, ODxSEL[1:0] = 11			15	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, $V_{DD} = V_{DDO} = V_{DDX} = 3.3V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	CLK_SEL, ODASEL_[1:0], ODBSEL_[1:0]	$V_{DD} = V_{IN}$ = 3.465V			150	µA
		PDSEL_[2:0]	$V_{DD} = V_{IN}$ = 3.465V			5	µA
I_{IL}	Input Low Current	CLK_SEL, ODASEL_[1:0], ODBSEL_[1:0]	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		PDSEL_[2:0]	V_{DD} = 3.465, V_{IN} = 0V	-150			µA
V_{OH}	Output High Voltage; NOTE 1			2.6			V
V_{OL}	Output Low Voltage; NOTE 1					0.5	V

NOTE 1: Outputs terminated with 50Ω to V_{DDO}/2. See Parameter Measurement Information section, *Output Load Test Circuit diagram.*

Table 4C. Differential DC Characteristics, $V_{DD} = V_{DDO} = V_{DDX} = 3.3V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK0, nCLK0, CLK1, nCLK1	$V_{DD} = V_{IN} = 3.465V$			150	µA
I_{IL}	Input Low Current	CLK0, CLK1	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-5			µA
		nCLK0, nCLK1	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-150			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1			0.5		V_{DD} – 0.85	V

NOTE 1. Common mode voltage is defined at the crosspoint.

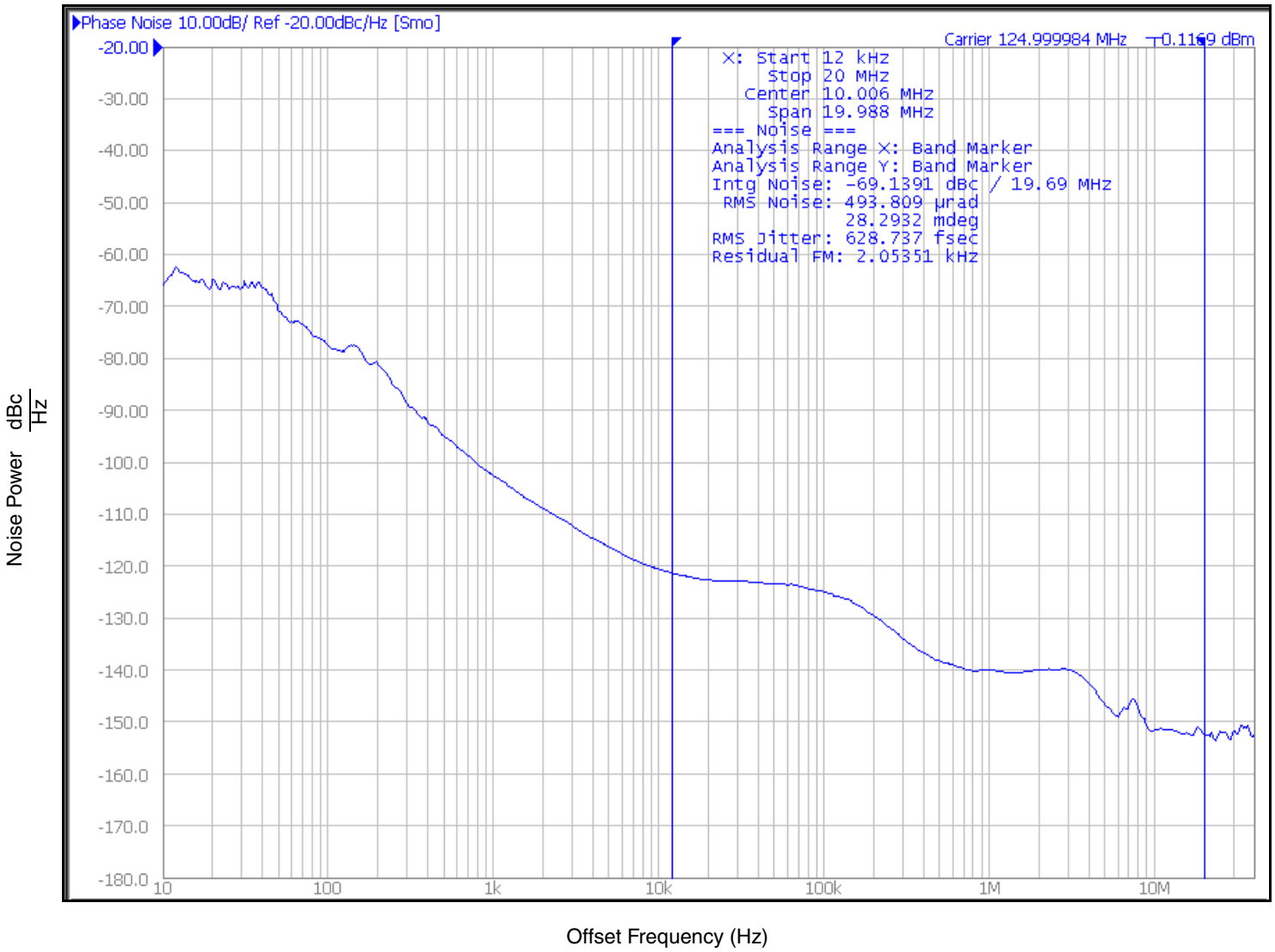
AC Electrical Characteristics

Table 5. AC Characteristics, $V_{DD} = V_{DDO} = V_{DDX} = 3.3V \pm 5\%$, T_A = -40°C to 85°C

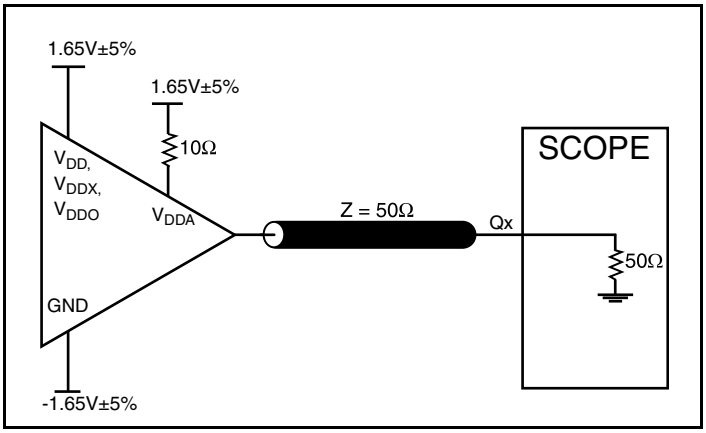
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{IN}	Input Frequency		0.008		155.52	MHz
f_{OUT}	Output Frequency		25		312.5	MHz
*t*jit(Ø)	RMS Phase Jitter, (Random), NOTE 1	125MHz f_{OUT}, 27MHz crystal, Integration Range: 12kHz – 20MHz		0.668	0.762	ps
		156.25MHz f_{OUT}, 27MHz crystal, Integration Range: 12kHz – 20MHz		0.684	0.797	ps
		312.5MHz f_{OUT}, 27MHz crystal, Integration Range: 12kHz – 20MHz		0.643	0.730	ps
PSNR	Power Supply Rejection Ratio	V_{PP} = 50mV Sine Wave, Integration Range: 10kHz – 10MHz		-85		dB
*t*sk(o)	Output Skew; NOTE 2, 3				70	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	200		550	ps
odc	Output Duty Cycle	$f_{OUT} \leq 156.25MHz$	48		52	%
		$f_{OUT} = 312.5MHz$	45		55	%
t_{LOCK}	VCXO & FemtoClock PLL Lock Time; NOTE 4	Reference Clock Input is ±50ppm from Nominal Frequency, Bandwidth Low		9		s

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: Characterized with outputs at the same frequency using the loop filter components for the 44Hz loop bandwidth.
Refer to Jitter Attenuator Loop Bandwidth Selection Table.
NOTE 1: Outputs switching to same frequency. Refer to the Phase Noise Plot.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 4: Lock Time measured from power-up to stable output frequency, LOW bandwidth setting.

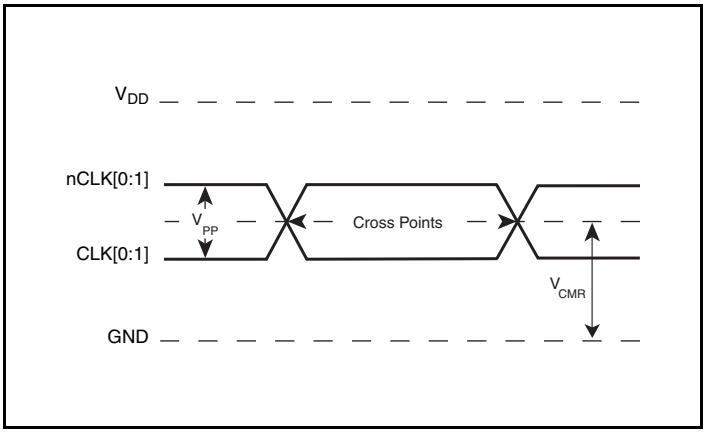
Typical Phase Noise at 125MHz



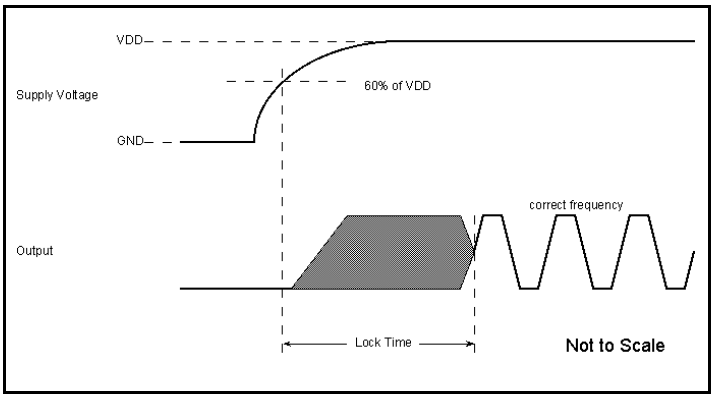
Parameter Measurement Information



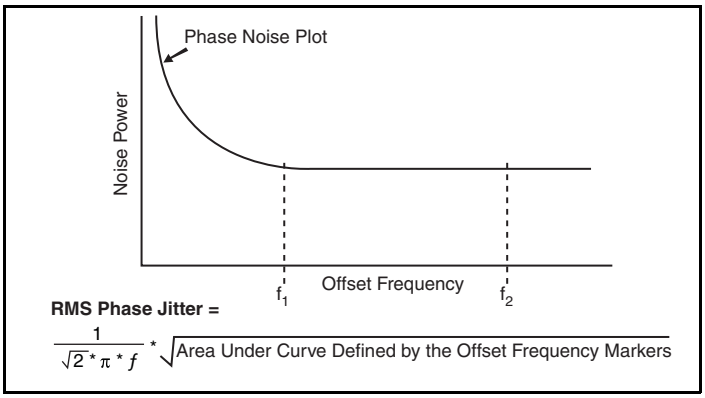
3.3V LVCMOS Output Load Test Circuit



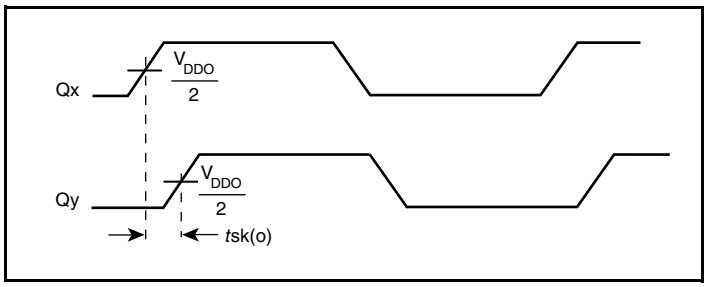
Differential Input Level



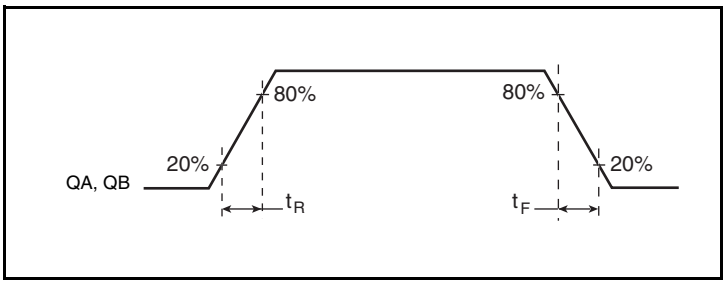
VCXO & FemtoClock PLL Lock Time



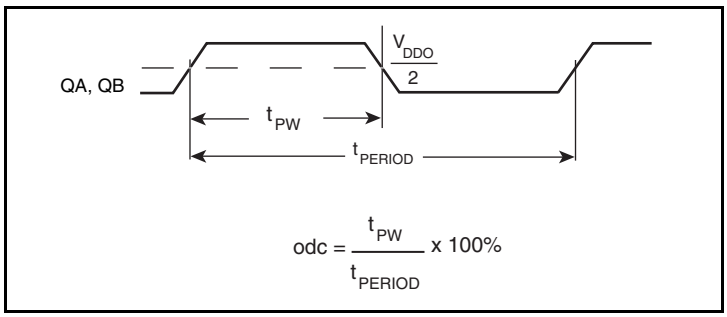
RMS Phase Jitter



Output Skew



LVCMOS Output Rise/Fall Time



Output Duty Cycle/Pulse Width/Period

Applications Information

Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_1 = V_{DD}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_1 in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{DD} = 3.3V, R1 and R2 value should be adjusted to set V_1 at 1.25V. The values below are for when both the single ended swing and V_{DD} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{DD} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

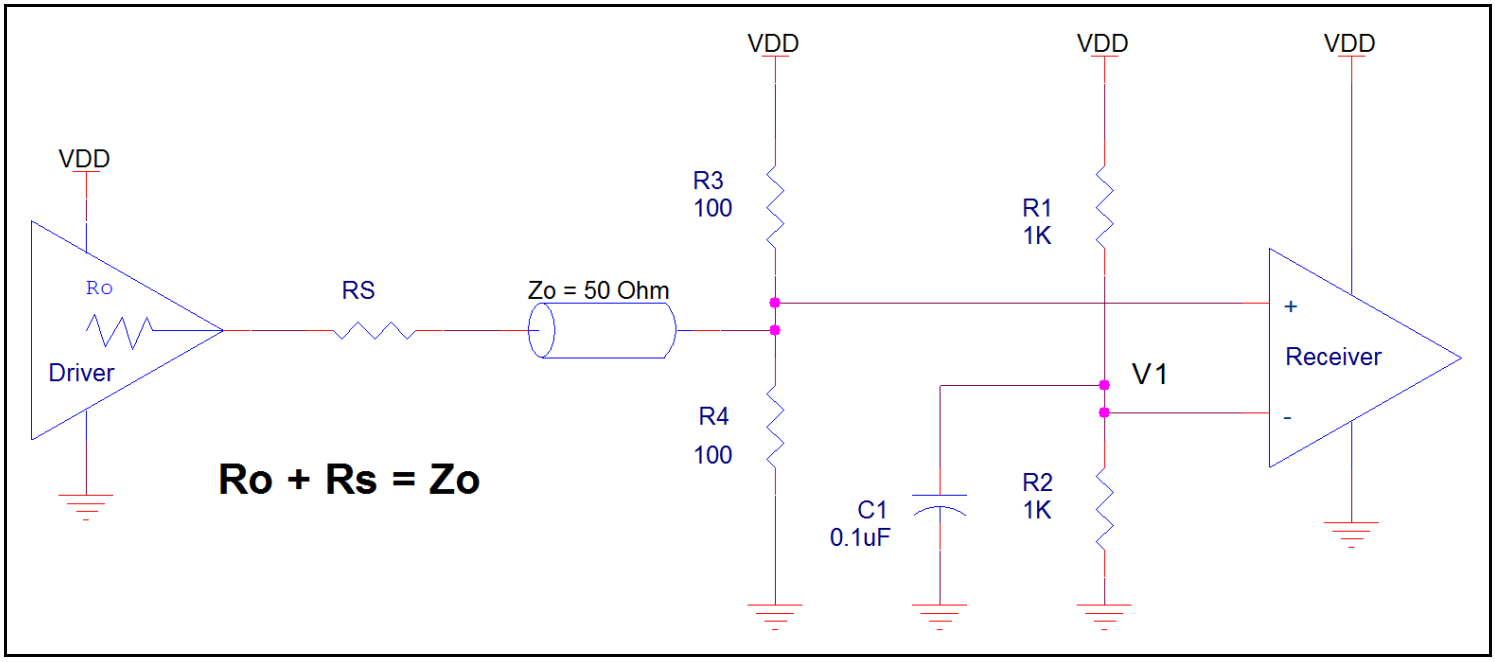


Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, HCSL and other differential signals. Both differential signals must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2E* show interface examples for the input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 2A, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

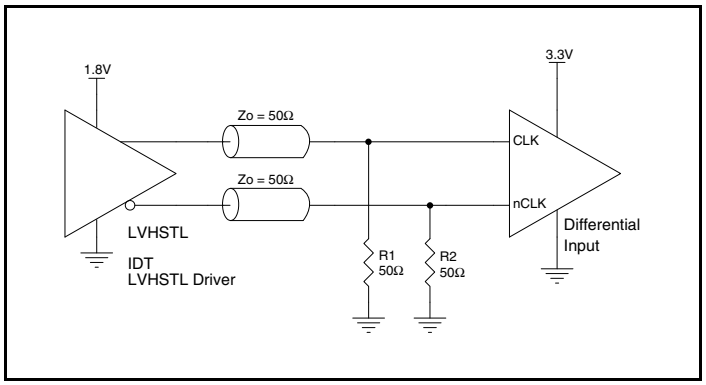


Figure 2A. CLK/nCLK Input Driven by an IDT Open Emitter LVHSTL Driver

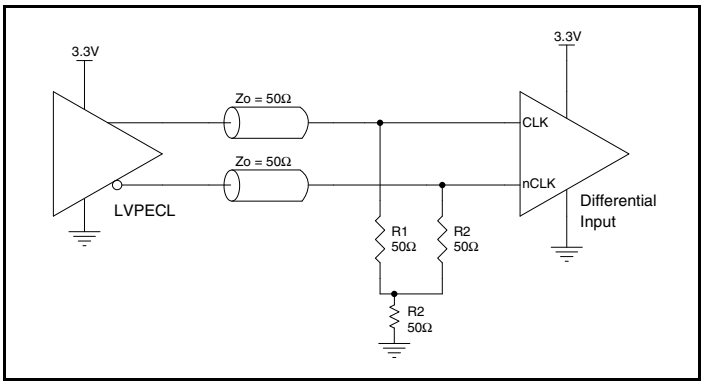


Figure 2B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

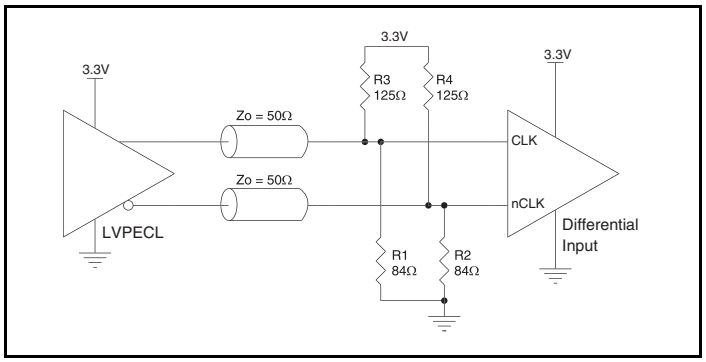


Figure 2C. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

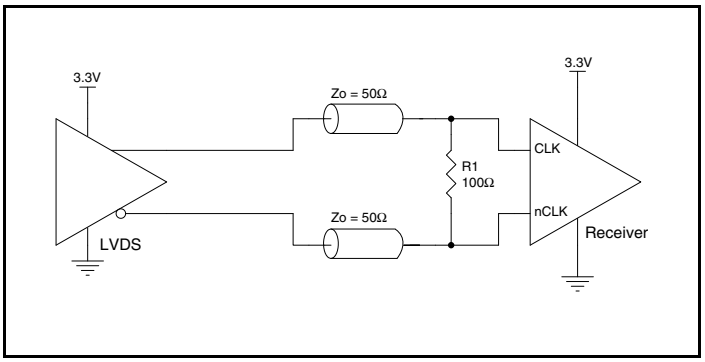


Figure 2D. CLK/nCLK Input Driven by a 3.3V LVDS Driver

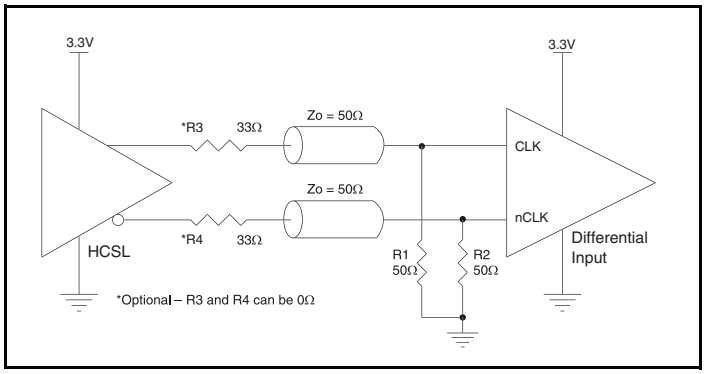


Figure 2E. CLK/nCLK Input Driven by a 3.3V HCSL Driver

Recommendations for Unused Input and Output Pins

Inputs:

CLK/nCLK Inputs

For applications not requiring the use of both differential inputs, it is recommended that the CLK1 and nCLK1 inputs be used for optimal performance. CLK0 and nCLK0 can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK0 to ground.

LVCMOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVCMOS Outputs

All unused LVCMOS outputs can be left floating. There should be no trace attached.

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 3*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

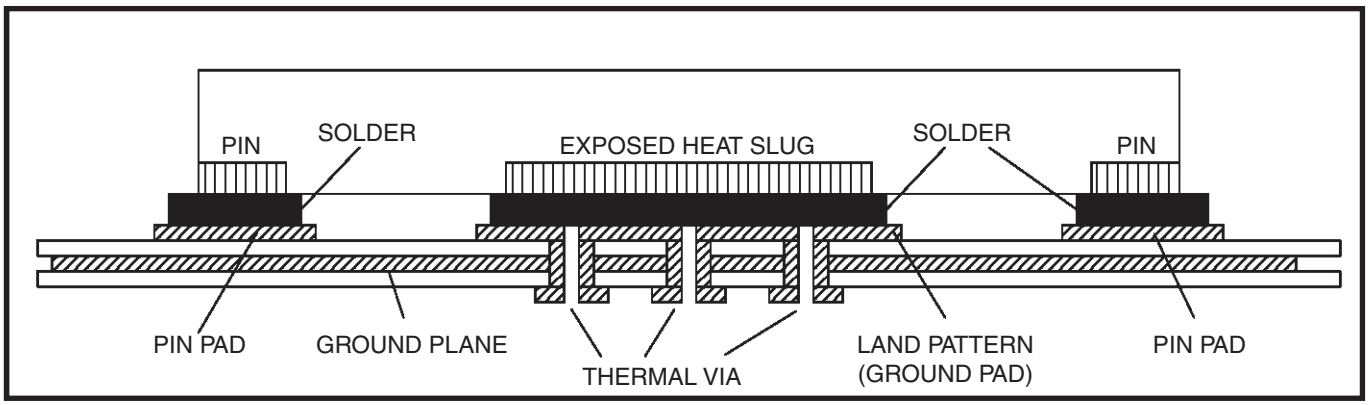
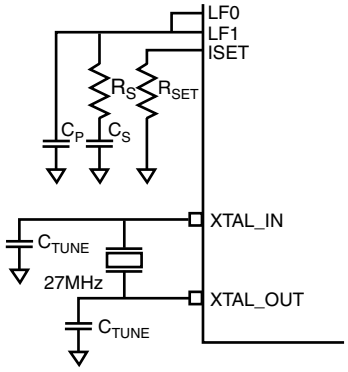


Figure 3. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Jitter Attenuator External Components

Choosing the correct external components and having a proper printed circuit board (PCB) layout is a key task for quality operation of the Jitter Attenuator. In choosing a crystal, special precaution must be taken with load capacitance (C_L), frequency accuracy and temperature range.

The crystal's C_L characteristic determines its resonating frequency and is closely related to the center tuning of the crystal. The total external capacitance ($C_{EXTERNAL}$) seen by the crystal when installed on a PCB is the sum of the stray board capacitance, IC package lead capacitance, internal device capacitance and any installed tuning capacitors (C_{TUNE}). The recommended C_L in the Crystal Parameter Table balances the tuning range by centering the tuning curve for a typical PCB. If the crystal C_L is greater than the total external capacitance ($C_L > C_{EXTERNAL}$), the crystal will oscillate at a higher frequency than the specification. If the crystal C_L is lower than the total external capacitance ($C_L < C_{EXTERNAL}$), the crystal will oscillate at a lower frequency than the specification. Mismatches between C_L and $C_{EXTERNAL}$ require adjustments in C_{TUNE} in order to center the tuning curve. In addition, the frequency accuracy specification in the crystal characteristics table are used to calculate the APR (Absolute Pull Range). It is recommended that the crystal CL is not to exceed the value stated in the Crystal Parameter Table because it can lead to a reduced APR.



Crystal Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
	Mode of Oscillation			Fundamental		
f_N	Frequency			27		MHz
f_T	Frequency Tolerance				±20	ppm
f_S	Frequency Stability				±20	ppm
	Operating Temperature Range		-40		+85	^{0}C
C_L	Load Capacitance			10		pF
C_O	Shunt Capacitance			4		pF
ESR	Equivalent Series Resistance				40	Ω
	Drive Level				1	mW
	Aging @ 25 ^{0}C	First Year			±3	ppm

The VCXO-PLL Loop Bandwidth Selection Table shows R_S, C_S,C_P and R_{SET} values for recommended high, mid and low loop bandwidth configurations. The device has been characterized using these parameters. In addition, the digital VCXO gain (K_{VCXO}) has been provided for additional loop filter requirements.

Jitter Attenuator Characteristics Table

Symbol	Parameter	Typical	Units
k_{VCXO}	VCXO Gain	2.78	kHz/V

Jitter Attenuator Loop Bandwidth Selection Table (2nd Order Loop Filter)

Bandwidth	Crystal Frequency	R_S (kΩ)	C_S (µF)	C_P (µF)	R3 (kΩ)	C3 (µF)	R_{SET} (kΩ)
15Hz (Low)	27MHz	215	10	0.022	0	DEPOP	2.74
30Hz (Mid)	27MHz	432	2.2	0.0047	0	DEPOP	2.74
60Hz (High)	27MHz	470	1	0.0022	0	DEPOP	1.5

NOTE: See Application Schematic to identify loop filter components R_S, C_S, C_P, R3, C3 and R_{SET}.

For applications in which there is substantial low frequency jitter in the input reference and the phase detector frequency of 8kHz or 10kHz lies in or near a jitter mask, a three pole filter is recommended.

Suggested part values are in the table below. Note that the option of a three pole filter can be left open by laying out the three pole filter but setting R3 to 0Ω and not populating C3. Refer to the application schematic for a specific example.

Jitter Attenuator Loop Bandwidth Selection Table (3rd Order Loop Filter)

Bandwidth	Crystal Frequency	R_S (kΩ)	C_S (µF)	C_P (µF)	R3 (kΩ)	C3 (µF)	R_{SET} (kΩ)
15Hz (Low)	27MHz	196	10	0.022	82.5	0.010	2.74
30Hz (Mid)	27MHz	392	2.2	0.0047	165	0.0022	2.74
60Hz (High)	27MHz	432	1	0.0022	182	0.001	1.5

NOTE: See Application Schematic to identify loop filter components R_S, C_S, C_P, R3, C3 and R_{SET}.

The crystal and external loop filter components should be kept as close as possible to the device. Loop filter and crystal traces should be kept short and separated from each other. Other signal traces should be kept separate and not run underneath the device, loop filter or crystal components.

Schematic Example

Figure 4 shows an example of the ICS810N252I-02 application schematic. In this example, the device is operated at V_{DD}= V_{DDA} = V_{DDX} = V_{DDO} = 3.3V. The inputs are driven by a 3.3V LVPECL driver and an LVDS driver.

A three pole loop filter is used for the greater reduction of 8kHz or 10kHz phase detector spurs relative to that afforded by a two pole loop filter. It is recommended that the loop filter components be laid out for the 3-pole option, which will also allow a 2-pole filter to be used The loop filter components are to be laid out on the ICS810N252I-02 side of the PCB directly adjacent to the LF0 and LF1 pins.

As with any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS810N252I-02 provides separate V_{DD}, V_{DDA}, V_{DDX} and V_{DDO} power supplies for each jitter attenuator to isolate any high switching noise from coupling into the internal PLLs.

In order to achieve the best possible filtering, it is highly recommended that the 0.1uF capacitors on the device side of the ferrite beads be placed on the device side of the PCB as close to the power pins as possible. This is represented by the placement of these capacitors in the schematic. If space is limited, the ferrite beads, 10uF and 0.1uF capacitor connected to 3.3V can be placed on the opposite side of the PCB. If space permits, place all filter components on the device side of the board.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for a wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.

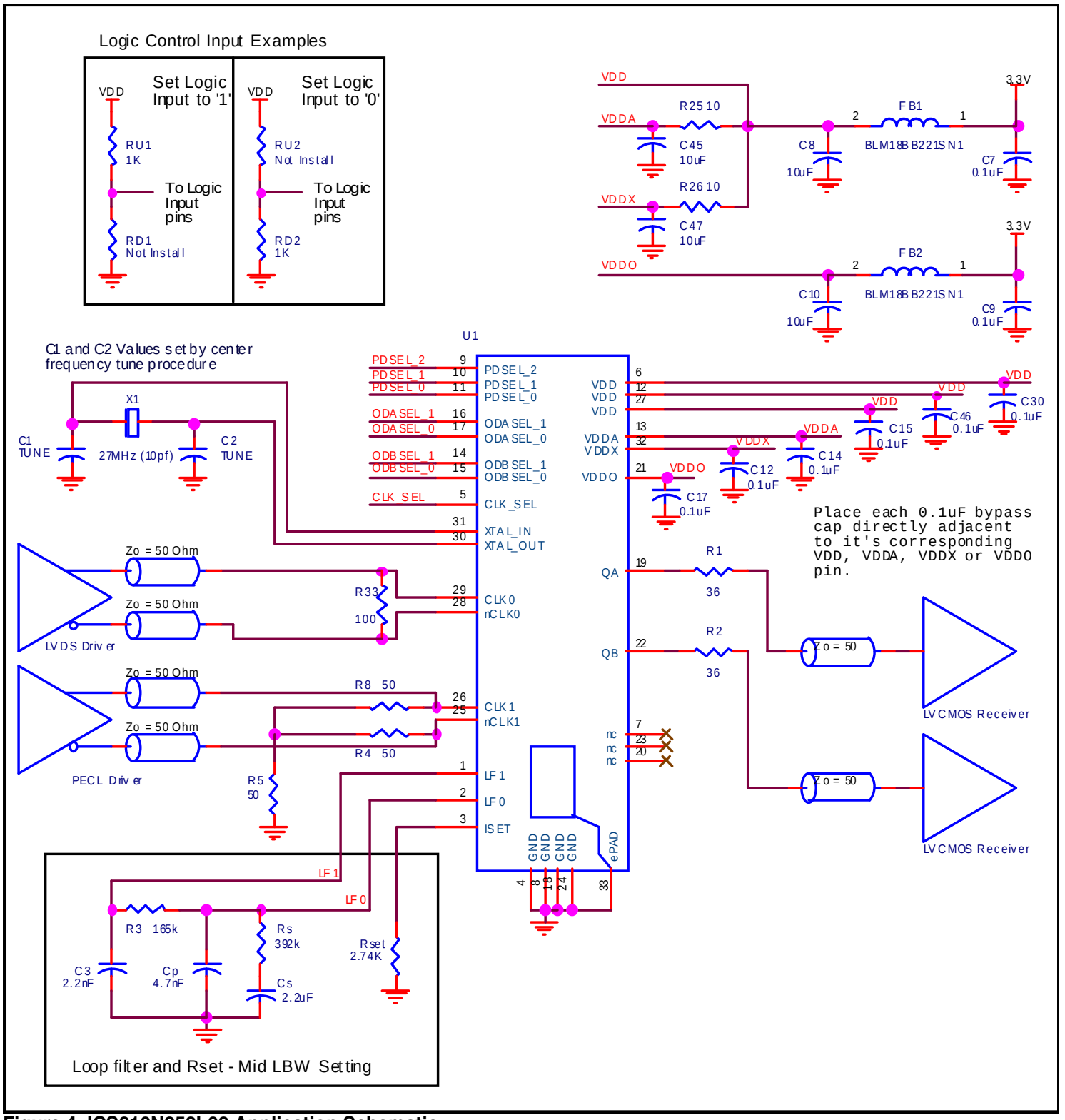


Figure 4. ICS810N252I-02 Application Schematic.

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS810N252I-02.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS810N252I-02 is the sum of the core power plus the power dissipation due to the load. The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

Core Output Power Dissipation

- Power $(core)_{MAX} = V_{DD\_MAX} * (I_{DD} + I_{DDA})$ = 3.465V *(230mA + 30mA) = **900.9mW**
- Power $(output)_{MAX} = V_{DDO\_MAX} * I_{DDO\_MAX}$ = 3.465V * 15mA = **51.98mW**

LVCMOS Output Power Dissipation

- Output Impedance R_{OUT} Power Dissipation due to Loading 50Ω to $V_{DD}/2$
  Output Current $I_{OUT} = V_{DD\_MAX} / [2 * (50Ω + R_{OUT})]$ = 3.465V / [2 * (50Ω + 14Ω)] = **27.07mA**
- Power Dissipation on the R_{OUT} per LVCMOS output
  Power $(R_{OUT}) = R_{OUT} * (I_{OUT})^2$ = 14Ω * (27.07mA)^2 = **10.26mW per output**
  Total Power (R_{OUT}) = 10.26mW * 2 = 20.52mW
- Dynamic Power Dissipation at 312.5MHz
  Power (312.5MHz) = C_{PD} * Frequency * $(V_{DDO})^2$ = 8pF * 312.5MHz * (3.465V)^2 = **30.02mW per output**
  Total Power (312.5MHz) = 30.02mW * 2 = 60.04mW

Total Power

= Power $(core)_{MAX}$ + Power $(output)_{MAX}$ + Power (R_{OUT}) + Total Power (312.5MHz)
= 900.0mW + 51.98mW + 20.52mW + 60.04mW
= 1033.4mW

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 33.1°C/W per Table 76 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 1.033W * 33.1°C/W = 119.2°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 32 Lead VFQFN, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**3**
Multi-Layer PCB, JEDEC Standard Test Boards	33.1°C/W	28.1°C/W	25.4°C/W

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 32 Lead VFQFN

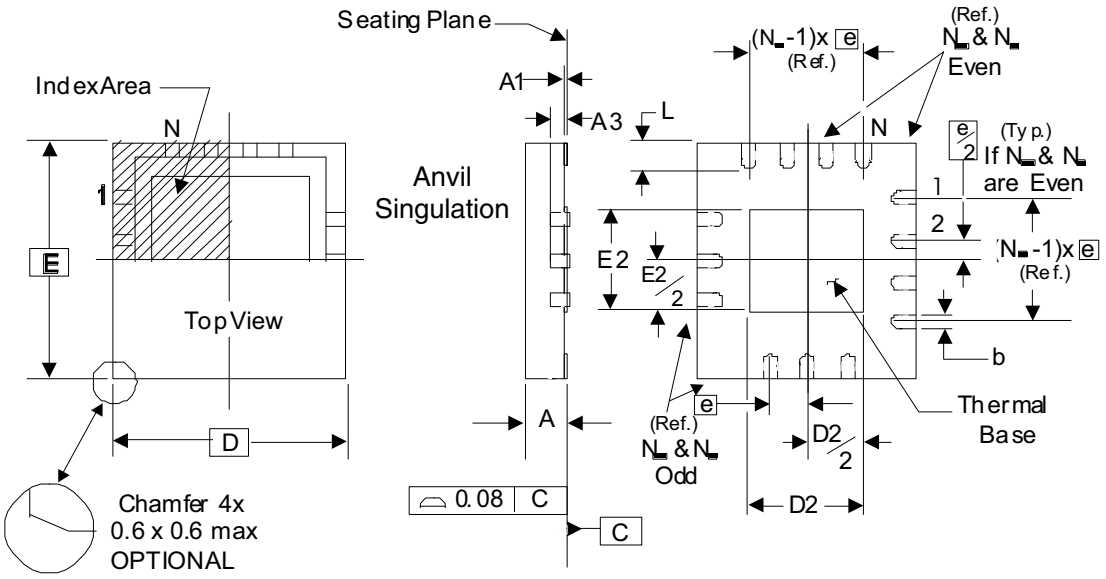
θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**3**
Multi-Layer PCB, JEDEC Standard Test Boards	33.1°C/W	28.1°C/W	25.4°C/W

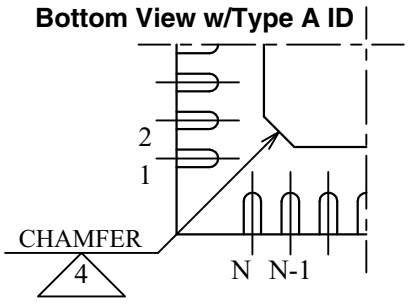
Transistor Count

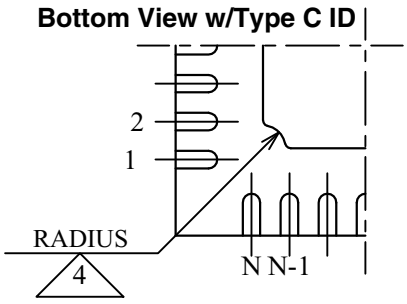
The transistor count for ICS810N252I-02 is: 44,740

Package Outline and Package Dimensions

Package Outline - K Suffix for 32 Lead VFQFN







There are 2 methods of indicating pin 1 corner at the back of the VFQFN package:

1. Type A: Chamfer on the paddle (near pin 1)
2. Type C: Mouse bite on the paddle (near pin 1)

Table 8. Package Dimensions

JEDEC Variation: VHHD-2/-4 All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N		32	
A	0.80		1.00
A1	0		0.05
A3		0.25 Ref.	
b	0.18	0.25	0.30
N_D & N_E			8
D & E		5.00 Basic	
D2 & E2	3.0		3.3
e		0.50 Basic	
L	0.30	0.40	0.50

Reference Document: JEDEC Publication 95, MO-220

NOTE: The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pin out are shown on the front page. The package dimensions are in Table 8.

Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
810N252CKI-02LF	ICS252CI02L	“Lead-Free” 32 Lead VFQFN	Tray	-40°C to 85°C
810N252CKI-02LFT	ICS252CI02L	“Lead-Free” 32 Lead VFQFN	Tape & Reel	-40°C to 85°C

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