General Description

The ICS872S480 is a Zero Delay Clock Generator with hitless input clock switching capability. The ICS872S480 is ideal for use in redundant, fault tolerant clock trees where low jitter frequency synthesis are critical. The device receives two differential clock signals from which it generates two outputs with “zero” delay. The output and feedback dividers are configured to allow for a 1:1 frequency generation ratio.

The ICS872S480 Dynamic Clock Switch (DCS) circuit continuously monitors both input clock signals. Upon detection of an invalid clock input (stuck LOW or HIGH for at least one complete clock period of the VCO feedback frequency), the loss of reference monitor will be set HIGH. If that clock is the primary clock, the DCS will switch to the good secondary clock and phase/frequency alignment will occur with minimal output phase disturbance. Once the primary clock is restored to a good state, the DCS will automatically switch back to the primary clock input.

The low jitter characteristics with input clock monitoring and DCS capability make the ICS872S480 an ideal choice for DDR3 applications requiring fault tolerant reference clocks.

Function Table

Input	Output Divider	Input & Output Frequency (MHz)	
FREQ_SEL		Minimum	Maximum
0	2	485	950
1 (default)	4	350	562.5

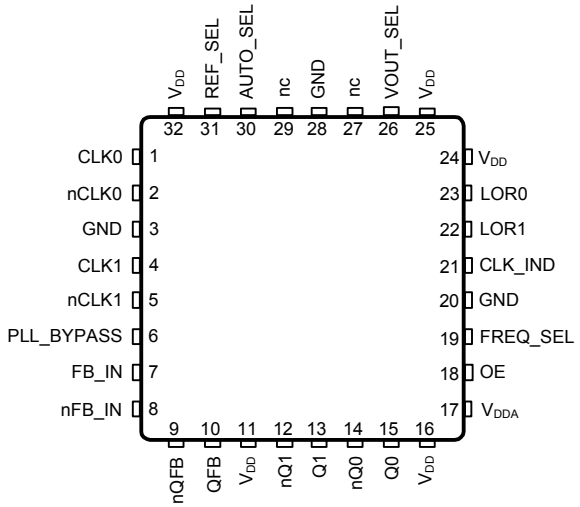
Output Voltage Table

Input	
VOUT_SEL	HSTL Output Style
0 (default)	1.5V
1	1.35V

Features

- Three differential HSTL output pairs
- Selectable differential CLKx, nCLKx input pairs
- CLKx, nCLKx pairs can accept the following differential input levels: LVPECL, LVDS, HSTL, HCSL
- Output frequency range: 350MHz to 950MHz
- Input frequency range: 350MHz to 950MHz
- VCO range: 970MHz to 2250MHz
- External feedback for “zero delay” clock regeneration with configurable frequencies
- Static phase offset: ±100ps (maximum)
- Cycle-to-cycle jitter: 25ps (maximum)
- Output skew: 20ps (maximum)
- 3.3V operating voltage supply
- Selectable DDR3 or DDR3 low voltage output
- 0°C to 70°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Pin Assignment



ICS872S480

32-Lead VFQFN
5mm x 5mm x 0.925mm package body
K Package
Top View

Block Diagram

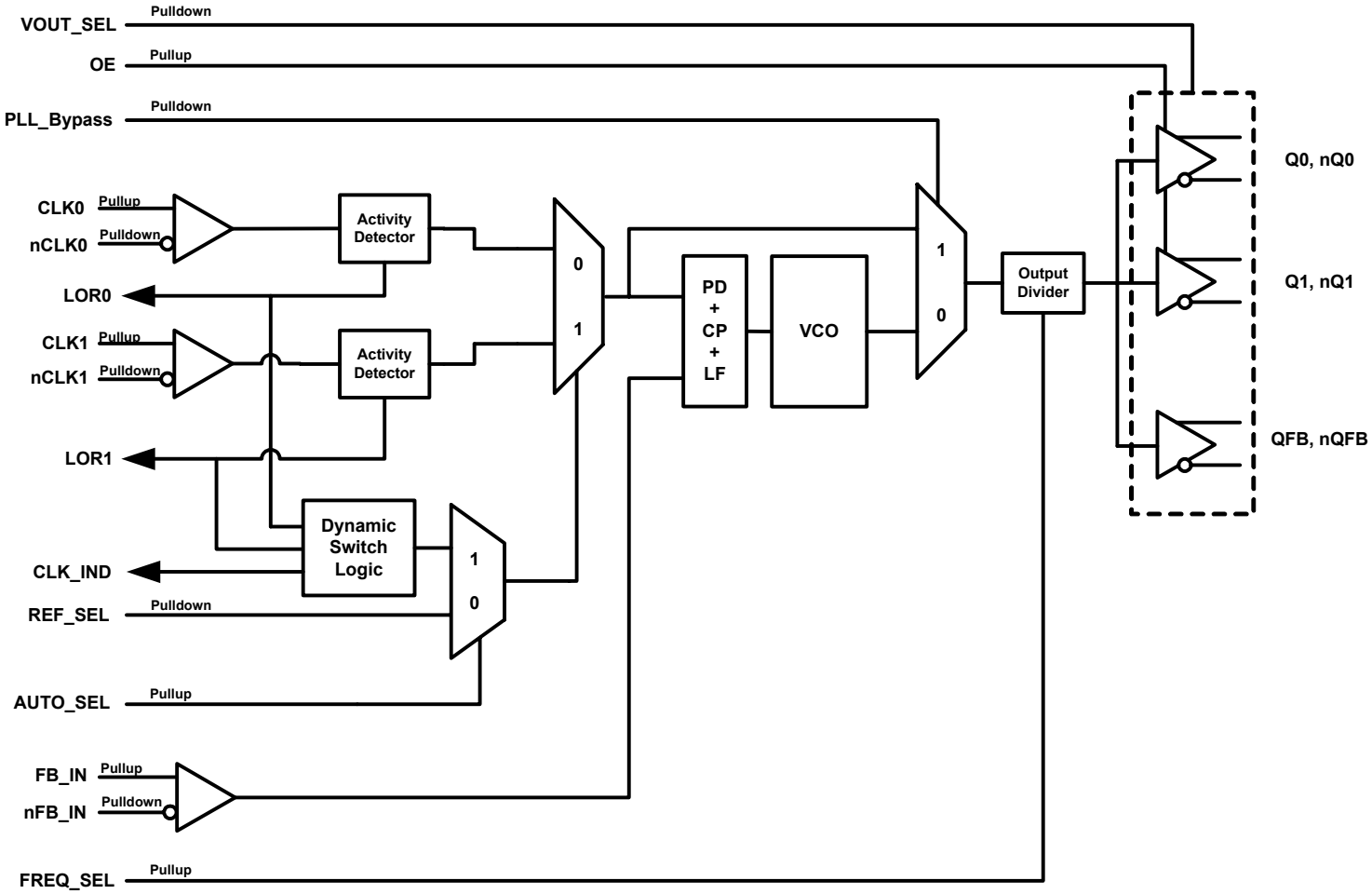


Table 1. Pin Descriptions

Number	Name	Type		Description
1	CLK0	Input	Pulldown	Non-inverting differential clock input.
2	nCLK0	Input	Pullup	Inverting differential clock input.
3, 20, 28	GND	Power		Power supply ground.
4	CLK1	Input	Pulldown	Non-inverting differential clock input.
5	nCLK1	Input	Pullup	Inverting differential clock input.
6	PLL_BYPASS	Input	Pulldown	PLL bypass pin. When HIGH, the PLL is bypassed and the reference clock is passed directly to the output dividers. LVCMOS/LVTTL interface levels.
7	FB_IN	Input	Pulldown	Non-inverting differential external feedback input.
8	nFB_IN	Input	Pullup	Inverting differential external feedback input.
9, 10	nQFB, QFB	Output		Differential feedback output pair. HSTL interface levels. See Table 4D.
11, 16, 24, 25, 32	V_{DD}	Power		Core supply pins.
12, 13	nQ1, Q1	Output		Differential output pair. HSTL interface levels.
14, 15	nQ0, Q0	Output		Differential output pair. HSTL interface levels.
17	V_{DDA}	Power		Analog supply pin.
18	OE	Input	Pullup	Output enable pin. LVCMOS/LVTTL interface levels.
19	FREQ_SEL	Input	Pullup	Frequency select pin. LVCMOS/LVTTL interface levels.
21	CLK_IND	Output		Clock indicator pin. When LOW, CLK0, nCLK0 is selected. When HIGH, CLK1, nCLK1 is selected.
22	LOR1	Output		Loss of Reference Indicator for CLK1, nCLK1. LVCMOS/LVTTL interface levels.
23	LOR0	Output		Loss of Reference Indicator for CLK0, nCLK0. LVCMOS/LVTTL interface levels.
26	VOUT_SEL	Input	Pulldown	Output voltage select pin. LVCMOS/LVTTL interface levels.
27, 29	nc	Unused		No connect.
30	AUTO_SEL	Input	Pullup	Dynamic Clock switch enable pin. When LOW, disables internal Dynamic Clock Switch circuitry and CLK_INDICATOR will track REF_SEL. When HIGH, Dynamic Clock Switch is enabled. LVCMOS/LVTTL interface levels.
31	REF_SEL	Input	Pulldown	Reference clock select pin. When LOW selects CLK0, nCLK0, when HIGH selects CLK1, nCLK1. LVCMOS/LVTTL interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			2		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to V_{DD} + 0.5V
Package Thermal Impedance, θ_{JA}	42.7°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} –0.25	3.3	V_{DD}	V
I_{DD}	Power Supply Current	Outputs terminated 50Ω to GND			275	mA
I_{DDA}	Analog Supply Current				25	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2.2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	PLL_BYPASS, REF_SEL, VOUT_SEL	V_{DD} = V_{IN} = 3.465V			150	µA
		OE, FREQ_SEL, AUTO_SEL	V_{DD} = V_{IN} = 3.465V			10	µA
I_{IL}	Input Low Current	PLL_BYPASS, REF_SEL, VOUT_SEL	V_{DD} = 3.465V, V_{IN} = 0V	-10			µA
		OE, FREQ_SEL, AUTO_SEL	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA

Table 4C. Differential DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK0, CLK1, FB_IN	$V_{DD} = V_{IN}$ = 3.465V			150	µA
		nCLK0, nCLK1, nFB_IN	$V_{DD} = V_{IN}$ = 3.465V			10	µA
I_{IL}	Input Low Current	CLK0, CLK1, FB_IN	V_{DD} = 3.465V, V_{IN} = 0V	-10			µA
		nCLK0, nCLK1, nFB_IN	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Voltage; NOTE 1			0.15		1.75	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			0.3		V_{DD} – 0.85	V

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2: Common mode input voltage is defined as V_{IH}.

Table 4D. HSTL DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OX}	Output Crosspoint Voltage, NOTE 1	VOUT_SEL = 0	0.7	0.8	0.9	V
		VOUT_SEL = 1	0.6	0.7	0.8	V
V_{OD}	Differential Output Voltage; NOTE 1	VOUT_SEL = 0	0.8	0.9	1.0	V
		VOUT_SEL = 1	0.8	0.9	1.0	V

NOTE 1: Outputs terminated with 50Ω to ground.

Table 5. Input Frequency Characteristics, V_{DD} = 3.3V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
F_{IN}	Input Frequency	CLK0, nCLK0, CLK1, nCLK1	FSEL = 1	485		950	MHz
			FSEL = 0	350		562.5	MHz

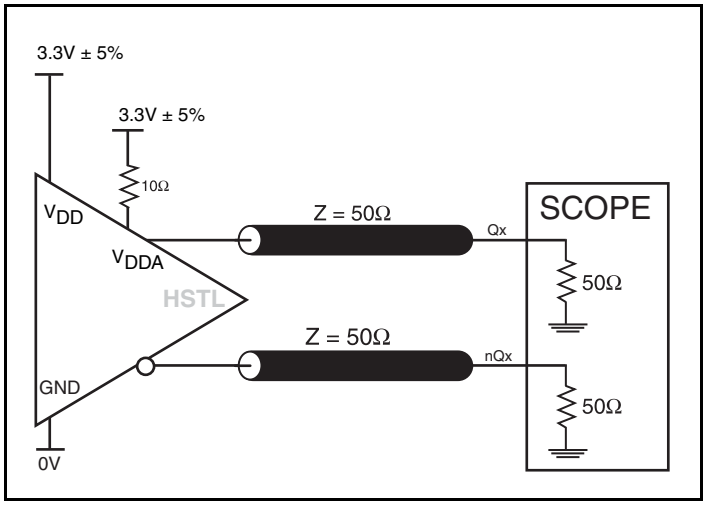
AC Electrical Characteristics

Table 6. AC Characteristics, V_{DD} = 3.3V ± 5%, T_A = 0°C to 70°C

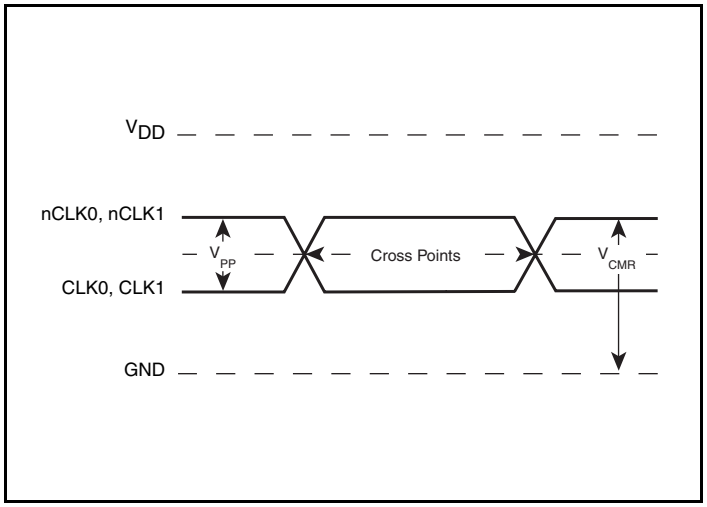
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency			350		950	MHz
t(Ø)	Static Phase Offset; NOTE 1, 2		f_{OUT} = 400MHz	-25		75	ps
			f_{OUT} = 533.3MHz	-50		50	ps
			f_{OUT} = 666.6MHz	-50		50	ps
			f_{OUT} = 800MHz	-50		50	ps
tdyn(Ø)	Dynamic Phase Offset; NOTE 7		f_{OUT} = 400MHz			±20	ps
			f_{OUT} = 533.3MHz			±25	ps
			f_{OUT} = 666.6MHz			±20	ps
			f_{OUT} = 800MHz			±20	ps
pdev	Output Period Deviation; NOTE 3, 7					100	ps
*t*sk(o)	Output Skew; NOTE 2, 4					20	ps
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 3, 7					25	ps
t_L	PLL Lock Time; NOTE 7					3	ms
t_{Ldcs}	DCS PLL Lock Time; NOTE 6, 7				1.7		µs
t_{SLEW}	Output Slew Rate; NOTE 5	VOUT_SEL = 0	f_{OUT} = 400MHz	2.00	3.50	5.75	V/ns
			f_{OUT} = 533.3MHz	2.00	4.25	6.50	V/ns
			f_{OUT} = 666.6MHz	2.00	4.25	6.75	V/ns
			f_{OUT} = 800MHz	2.50	5.25	8.65	V/ns
		VOUT_SEL = 1	f_{OUT} = 400MHz	2.00	3.85	6.35	V/ns
			f_{OUT} = 533.3MHz	2.00	4.50	6.85	V/ns
			f_{OUT} = 666.6MHz	2.50	4.65	7.25	V/ns
			f_{OUT} = 800MHz	3.00	5.65	8.25	V/ns
odc	Output Duty Cycle			47		53	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Defined as the time difference between the input reference clock and the averaged feedback input signal across all conditions, when the PLL is locked and the input reference frequency is stable. Characterized using HSTL input level of 900mV, swing centered around 0.6V.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: This parameter is defined as the maximum output period deviation during a dynamic switch event with reference inputs 180° out of phase. This does not factor in any cycle-to-cycle jitter seen on the input or output.
NOTE 4: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 5: Output slew rate is measured at V_{OX} ± 150mV for VOUT_SEL = 0 and V_{OX} ±135mV for VOUT_SEL = 1.
NOTE 6: This parameter is defined as PLL lock time after a dynamic switch event with reference inputs 180° out of phase.
NOTE 7: This parameter is guaranteed by characterization. Not tested in production.

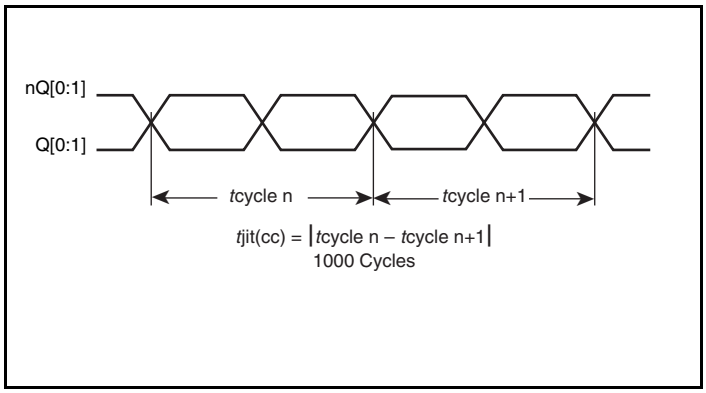
Parameter Measurement Information



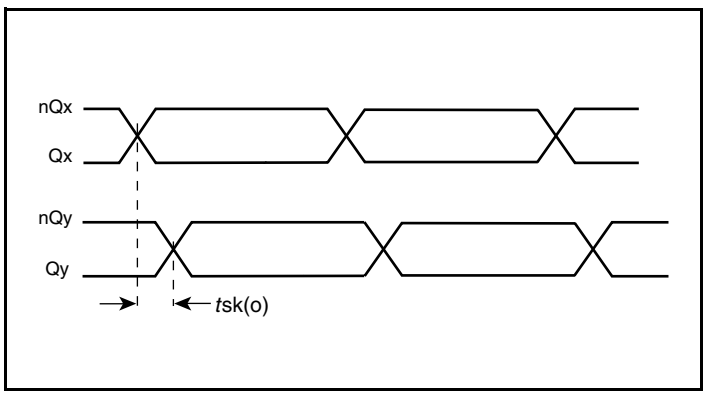
3.3V Output Load AC Test Circuit



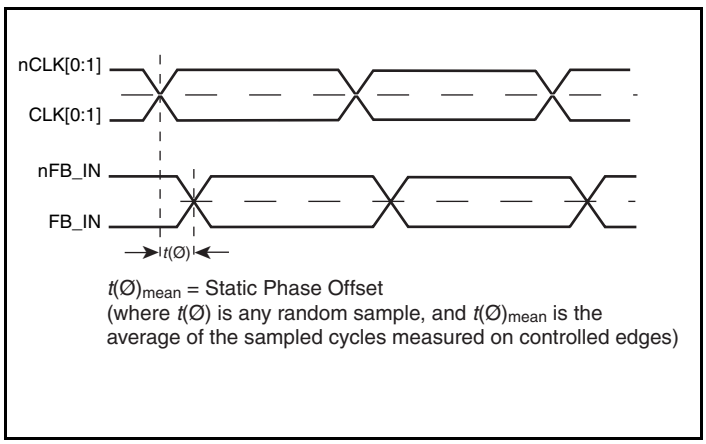
Differential Input Level



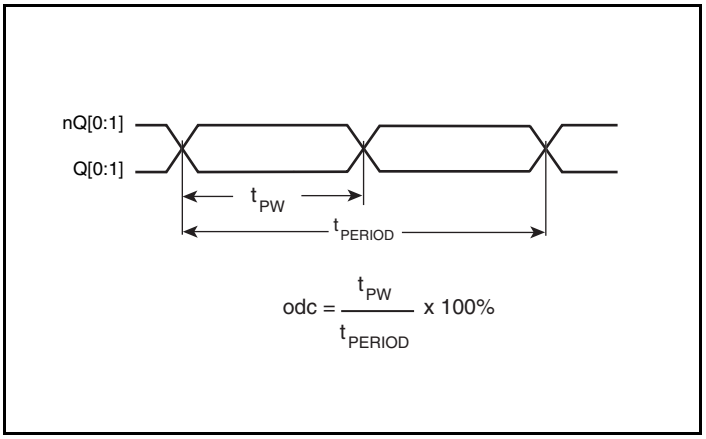
Cycle-to-Cycle Jitter



Output Skew

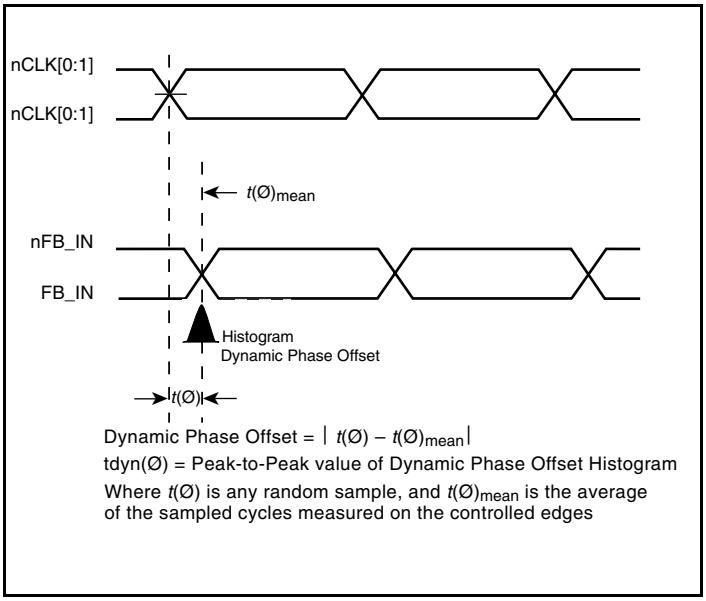


Static Phase Offset

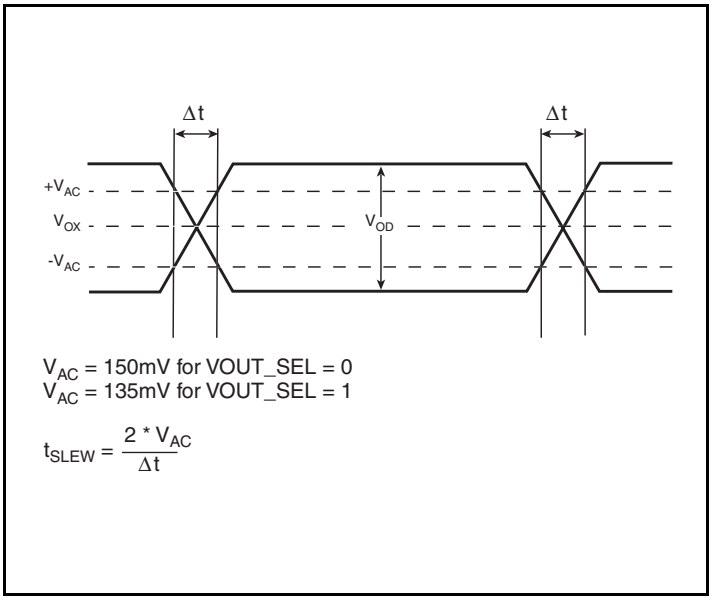


Output Duty Cycle/Pulse Width/Period

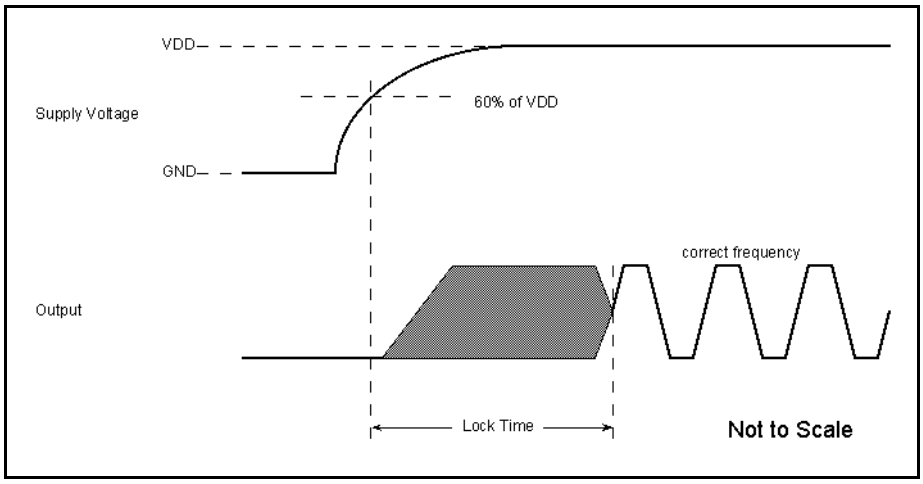
Parameter Measurement Information, continued



Dynamic Phase Offset



Slew Rate



PLL Lock Time

Applications Information

Clock Redundancy and Reference Selection

The ICS872S480 accepts two differential input clocks, CLK0, nCLK0 and CLK1, nCLK1, for the purpose of redundancy. Only one of these clocks can be selected at any given time for use as the reference. CLK0, nCLK0 is defined as the initial, or primary clock, while the remaining clock is the redundant or secondary clock. The output signal CLK_IND indicates which clock input is being used as the reference (LOW = CLK0, nCLK0, HIGH = CLK1, nCLK1).

Failure Detection and Alarm Signaling

Within the ICS872S480 device, CLK0, nCLK0 and CLK1, nCLK1 are continuously monitored for failures. A failure on either of these clocks is detected when one of the clock signals is stuck HIGH or LOW for at least 1 period of the feedback. Upon detection of a failure, the corresponding loss-of-reference signal, LOR0 or LOR1, will be set HIGH. The input clocks are continuously monitored and the loss-of-reference signals will continue to reflect the real-time status of each input clock.

Manual Clock Switching

When input signal AUTO_SEL is driven LOW, the clock specified by REF_SEL will always be used as the reference, even when a clock failure is detected at the reference. In order to switch between CLK0, nCLK0 and CLK1, nCLK1 as the reference clock, the level on REF_SEL must be driven to the appropriate level. When the level on REF_SEL is changed, the selection of the new clock will take place, and CLK_IND will be updated to indicate which clock is now supplying the reference to the PLL.

Dynamic Clock Switching

The Dynamic Clock Switching (DCS) process serves as an automatic safety mechanism to protect the stability of the PLL when a failure occurs on the reference.

When input signal AUTO_SEL is not driven HIGH, an internal pullup pulls it HIGH so that DCS is enabled. If DCS is enabled and a failure occurs on the initial clock, the ICS872S480 device will check the status of the secondary clock. If the secondary clock is detected as a good input clock, the ICS872S480 will automatically de-select the initial clock as the reference and multiplex in the secondary clock. When a successful switch from the initial to secondary clock has been accomplished, CLK_IND will be updated to indicate the new reference. If and when the fault on the initial clock is corrected, the corresponding loss-of-reference flag will be updated to represent this clock as good again. Once updated, the DCS will undergo an automatic clock switch. See the Dynamic Clock Switch State Diagram and for additional details on the functionality of the Dynamic Clock Switching circuit.

Output Transitioning

After a successful DCS initiated clock switch, the internal PLL of the ICS872S480 will begin slewing to phase/frequency alignment of the newly selected clock input. The PLL will achieve lock to the new input with minimal phase disturbance at the outputs.

Recommended Power-up Sequence

1. Before startup, set AUTO_SEL low so the PLL will operate in manual switch mode, plus set REF_SEL low to ensure that the primary reference clock, CLK0, nCLK0, is selected. This will ensure that during startup, the PLL will acquire lock using the primary reference clock input.

2. Once powered-up, and assuming a stable clock is present at the primary clock input, the PLL will begin to phase/frequency slew as it attempts to achieve lock with the input reference clock.

3. Drive AUTO_SEL HIGH to enable DCS mode.

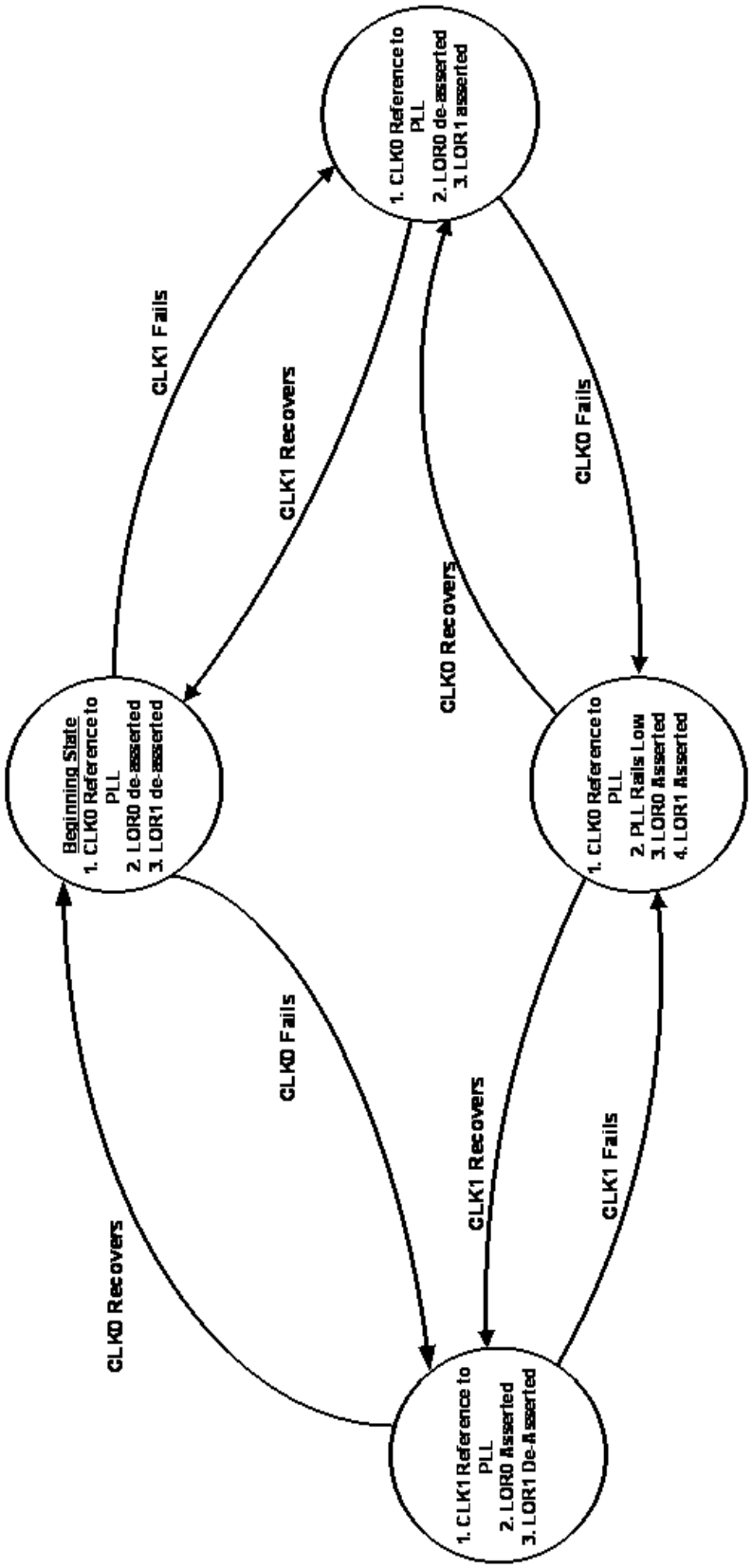
Alternate Power-up Sequence

If both input clocks are valid before power up, the part may be powered-up in DCS mode. However, it cannot be guaranteed that the PLL will achieve lock with one specific input clock.

1. Before startup, leave AUTO_SEL floating and the internal pullup will enable DCS mode.

2. Once powered up, the PLL will begin to phase/frequency slew as it attempts to achieve lock with one of the input reference clocks.

State Diagram



Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_{REF} = V_{DD}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{DD} = 3.3V, R1 and R2 value should be adjusted to set V_{REF} at 1.25V. The values below are for when both the single ended swing and V_{DD} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{DD} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

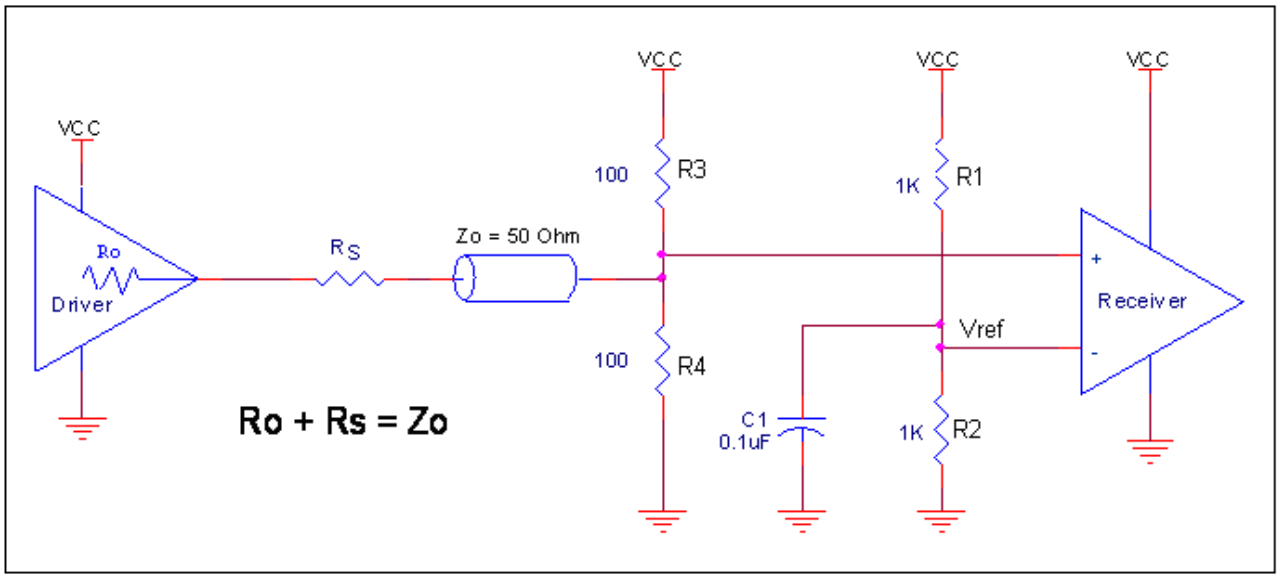


Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, HSTL, HCSL and other differential signals. Both differential signals must meet the V_{PP} and V_{CMR} input requirements. *Figures 3A to 3E* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 3A, the input termination applies for IDT open emitter HSTL drivers. If you are using an HSTL driver from another vendor, use their termination recommendation.

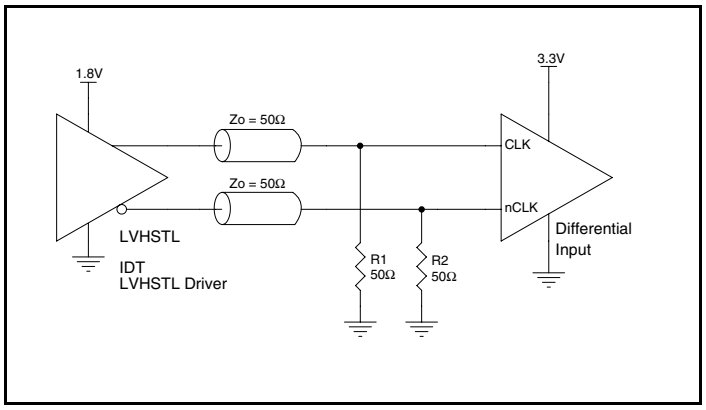


Figure 3A. CLK/nCLK Input Driven by an IDT Open Emitter HSTL Driver

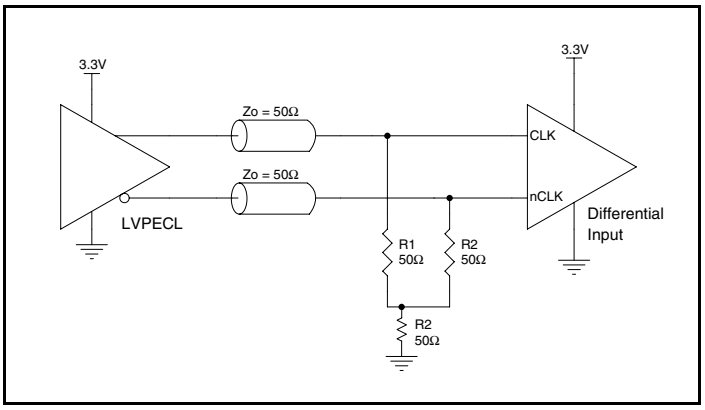


Figure 3B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

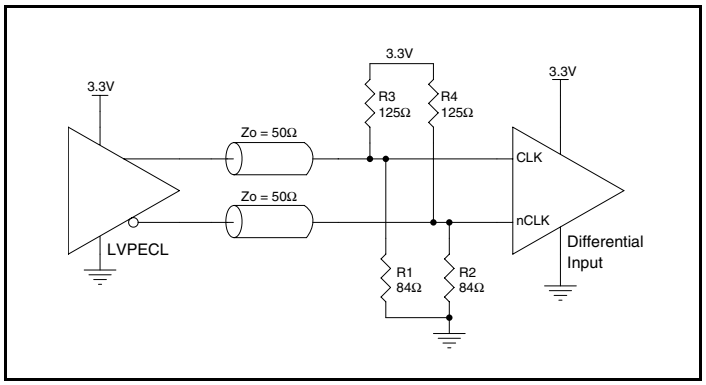


Figure 3C. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

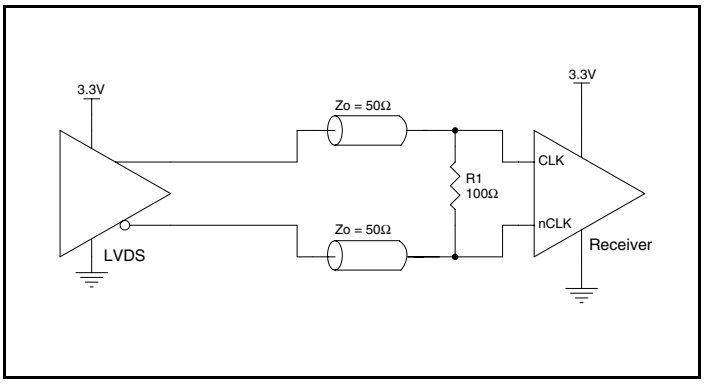


Figure 3D. CLK/nCLK Input Driven by a 3.3V LVDS Driver

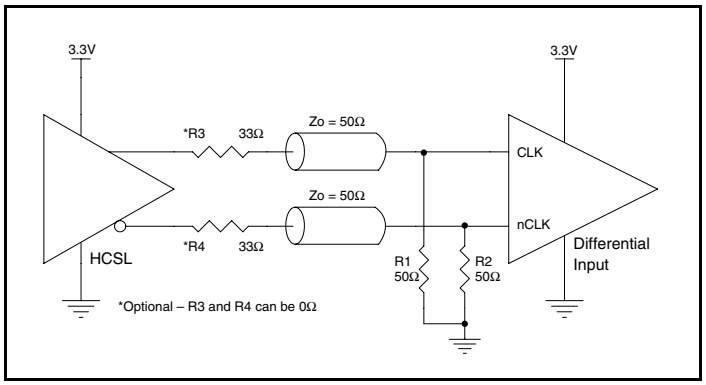


Figure 3E. CLK/nCLK Input Driven by a 3.3V HCSL Driver

Recommendations for Unused Input Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

Outputs:

HSTL Outputs

All unused HSTL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

HSTL Output Termination

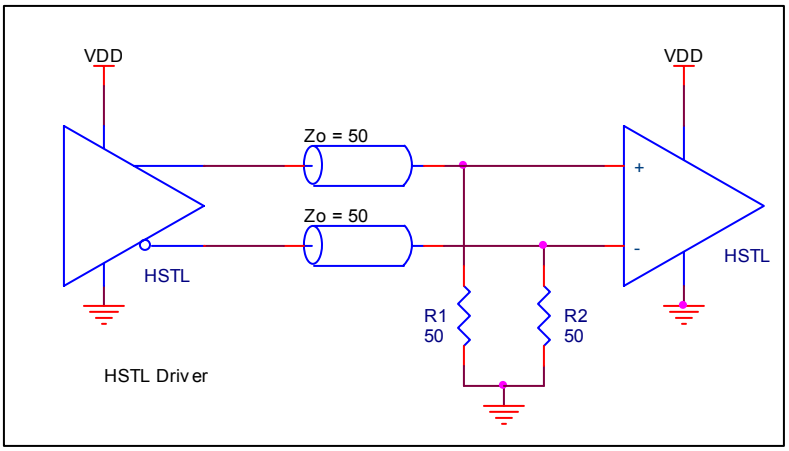


Figure 4. Output Termination

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 5.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

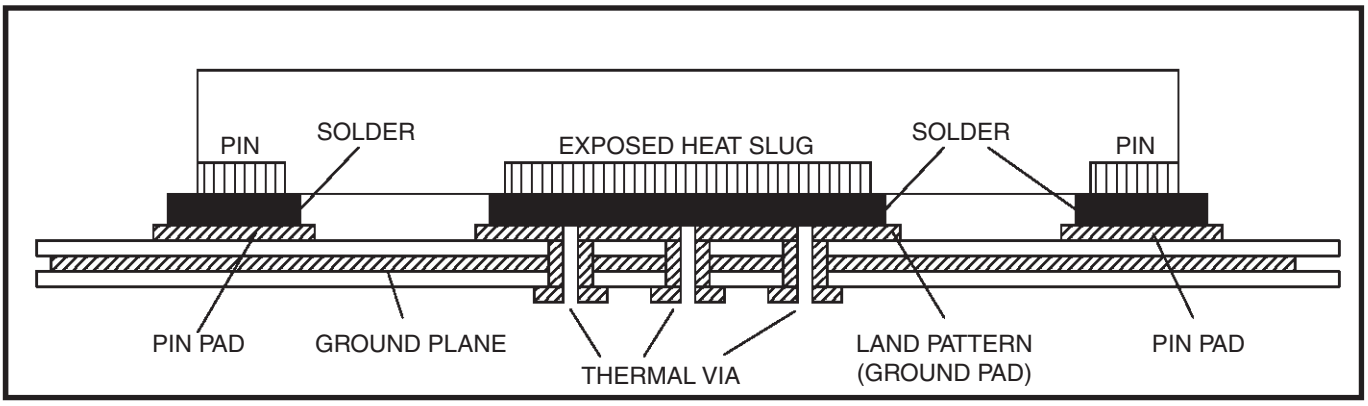


Figure 5. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Schematic Example

Figure 6 shows an example of ICS872S480 application schematic. In this example, the device is operated at V_{DD} = 3.3V. As with any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS872S480 provides separate power supplies to isolate from coupling into the internal PLL.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1uf capacitor in each power pin filter should be placed on the device side of the PCB and the other components can be placed on the opposite side.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for a wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.

The schematic example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure that the logic control inputs are properly set.

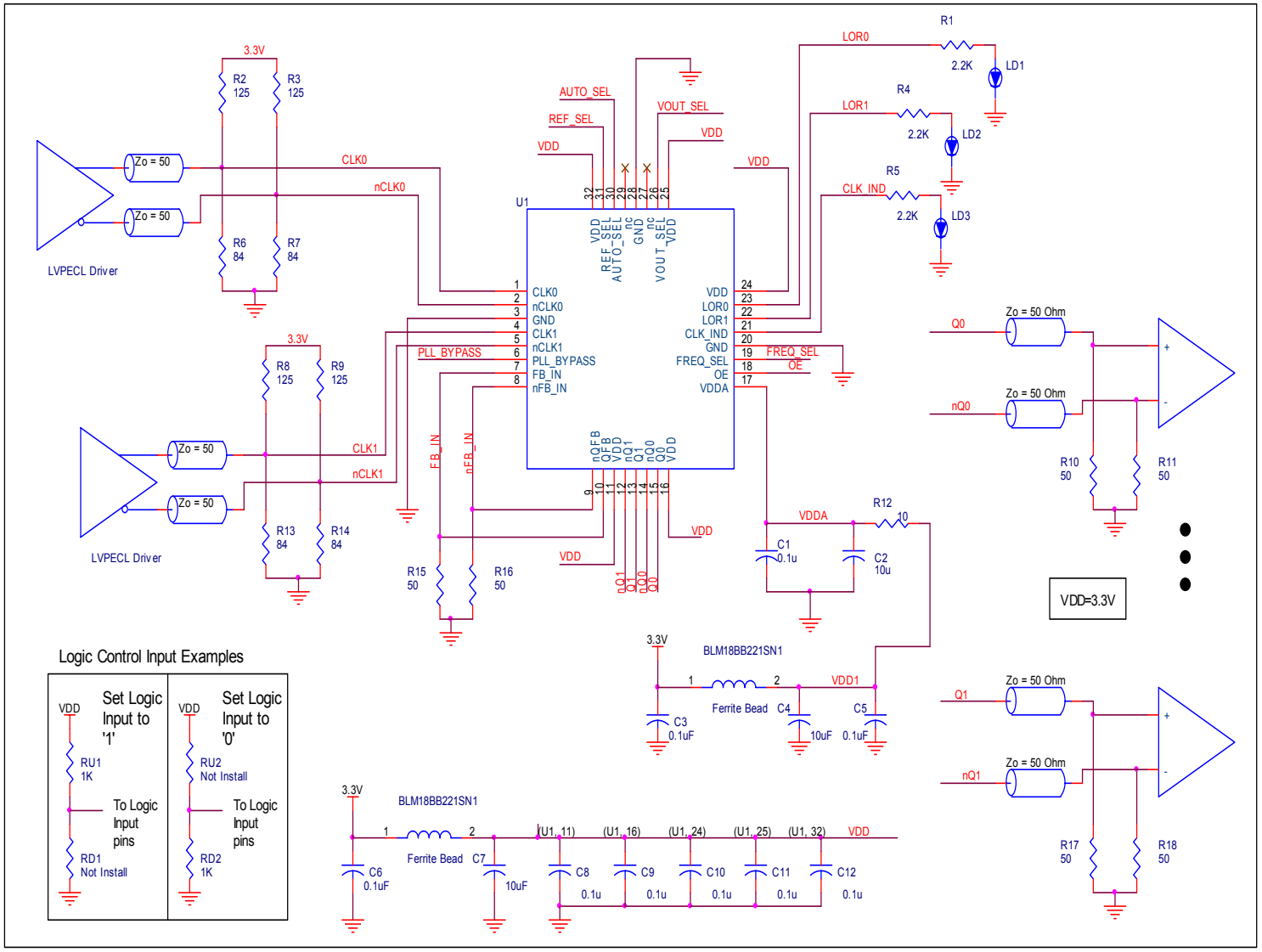


Figure 6. ICS872S480 Schematic Layout

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS872S480.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for theICS872S480 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

- Power $(core)_{MAX} = V_{DD\_MAX} * (I_{DD\_MAX} + I_{DDA\_MAX})$= 3.465V * (275mA + 25mA) = **1039.5mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 42.7°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:

70°C + 1.040W * 42.7°C/W = 114.4°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 7. Thermal Resistance θ_{JA} for 32 Lead VFQFN, Forced Convection

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	42.7°C/W	37.3°C/W	33.5°C/W

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for a 32-lead VFQFN

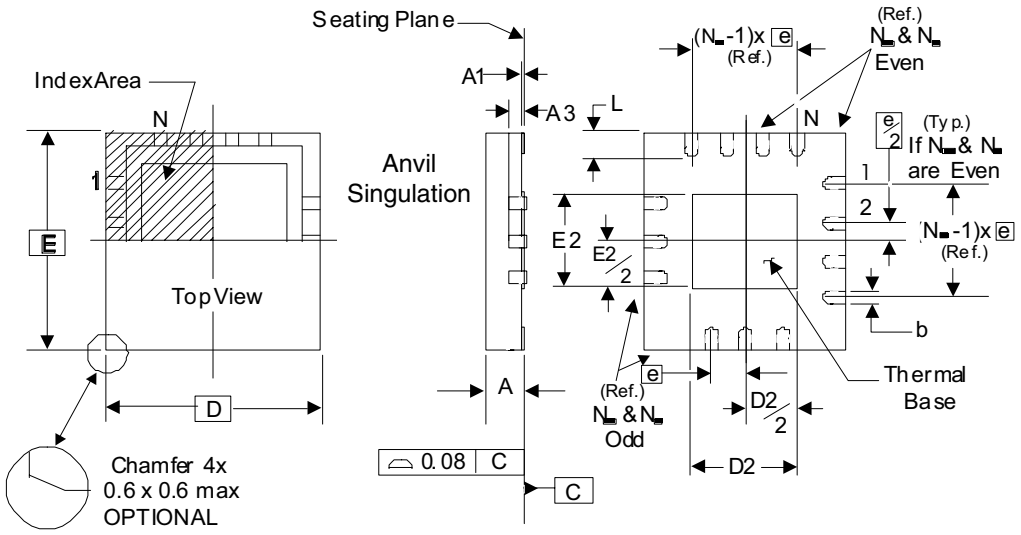
θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	42.7°C/W	37.3°C/W	33.5°C/W

Transistor Count

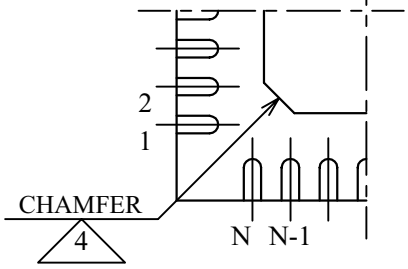
The transistor count for ICS872S480 is: 2110

Package Outline and Package Dimensions

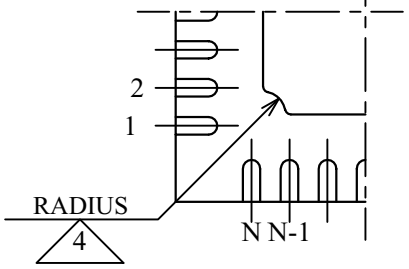
Package Outline - K Suffix for 32 Lead VFQFN



Bottom View w/Type A ID



Bottom View w/Type C ID



There are 2 methods of indicating pin 1 corner at the back of the VFQFN package are:

1. Type A: Chamfer on the paddle (near pin 1)
2. Type C: Mouse bite on the paddle (near pin 1)

Table 9. Package Dimensions

JEDEC Variation: VHHD-2/-4 All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N		32	
A	0.80		1.00
A1	0		0.05
A3		0.25 Ref.	
b	0.18	0.25	0.30
N_D & N_E			8
D & E		5.00 Basic	
D2 & E2	3.0		3.3
e		0.50 Basic	
L	0.30	0.40	0.50

Reference Document: JEDEC Publication 95, MO-220

NOTE: The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pinout are shown on the front page. The package dimensions are in Table 9.

Ordering Information

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
872S480BKLF	ICS72S480BL	“Lead-Free” 32 Lead VFQFN	Tray	0°C to 70°C
872S480BKLFT	ICS72S480BL	“Lead-Free” 32 Lead VFQFN	2500 Tape & Reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.