

General Description

The ICS874003-05 is a high performance Differential-to-LVDS Jitter Attenuator designed for use in PCI Express systems. In some PCI Express systems, such as those found in desktop PCs, the PCI Express clocks are generated from a low bandwidth, high phase noise PLL frequency synthesizer. In these systems, a jitter attenuator may be required to attenuate high frequency random and deterministic jitter components from the PLL synthesizer and from the system board. The ICS874003-05 has a bandwidth of 6.2MHz with <1dB peaking, easily meeting PCI Express Gen2 PLL requirements.

The ICS874003-05 uses IDT's 3rd Generation FemtoClock™ PLL technology to achieve the lowest possible phase noise. The device is packaged in a 20-Lead TSSOP package, making it ideal for use in space constrained applications such as PCI Express add-in cards.

Features

- Three differential LVDS output pairs
- One differential clock input
- CLK/nCLK can accept the following differential input levels: LVPECL, LVDS, LVHSTL, HCSL, SSTL
- Input frequency range: 98MHz to 128MHz
- Output frequency range: 98MHz to 320MHz
- VCO range: 490MHz - 640MHz
- Supports PCI-Express Spread-Spectrum Clocking
- High PLL bandwidth allows for better input tracking
- PCI Express (2.5 Gb/s) and Gen 2 (5 Gb/S) jitter compliant
- 0°C to 70°C ambient operating temperature
- Full 3.3V operating supply
- Available in lead-free (RoHS 6) packages

F_SEL[2:0] Function Table

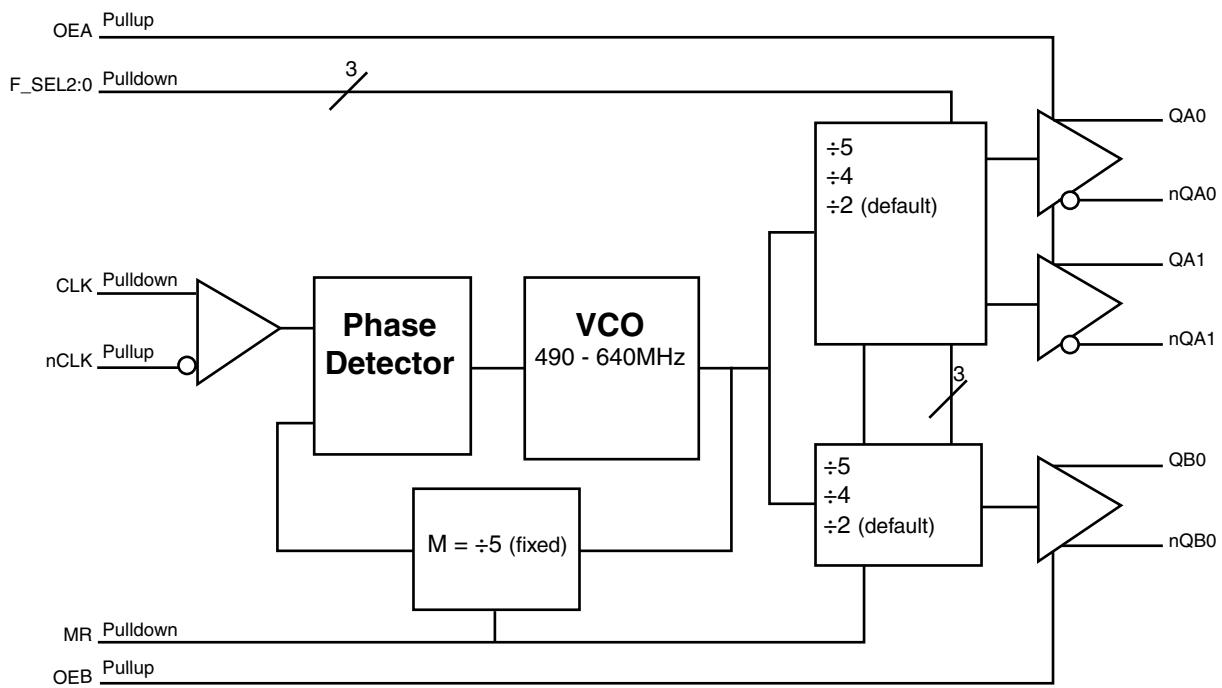
Inputs			Outputs	
F_SEL2	F_SEL1	F_SEL0	QA[0:1], nQA[0:1]	QB0, nQB0
0 (default)	0 (default)	0 (default)	÷2	÷2
1	0	0	÷5	÷2
0	1	0	÷4	÷2
1	1	0	÷2	÷4
0	0	1	÷2	÷5
1	0	1	÷5	÷4
0	1	1	÷4	÷5
1	1	1	÷4	÷4

Pin Assignment

QA1	1	20	nQA1
V _{DDO}	2	19	V _{DDO}
QA0	3	18	QB0
nQA0	4	17	nQB0
MR	5	16	F_SEL2
F_SEL0	6	15	OEB
nc	7	14	GND
V _{DDA}	8	13	nCLK
F_SEL1	9	12	CLK
V _{DD}	10	11	OEA

ICS874003-05
20-Lead TSSOP
6.5mm x 4.4mm x 0.925mm package body
G Package
Top View

Block Diagram



Pin Descriptions and Characteristics

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 20	QA1, nQA1	Output		Bank A differential output pair. LVDS interface levels.
2, 19	V _{DDO}	Power		Output supply pins.
3, 4	QA0, nQA0	Output		Bank A differential output pair. LVDS interface levels.
5	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs (nQ _x) to go low and the inverted outputs (Q _x) to go high. When logic LOW, the internal dividers and the outputs are enabled. LVC MOS/LVTTL interface levels.
6, 9, 16	F_SEL0, F_SEL1, F_SEL2	Input	Pulldown	Frequency select pin for QA _x /nQA _x and QB ₀ /nQB ₀ outputs. LVC MOS/LVTTL interface levels.
7	nc	Unused		No connect.
8	V _{DDA}	Power		Analog supply pin.
10	V _{DD}	Power		Core supply pin.
11	OEA	Input	Pullup	Output enable pin for QA pins. When HIGH, the QA _x /nQA _x outputs are active. When LOW, the QA _x /nQA _x outputs are in a high-impedance state. LVC MOS/LVTTL interface levels.
12	CLK	Input	Pulldown	Non-inverting differential clock input.
13	nCLK	Input	Pullup	Inverting differential clock input.
14	GND	Power		Power supply ground.
15	OEB	Input	Pullup	Output enable pin for QB ₀ pins. When HIGH, the QB ₀ /nQB ₀ outputs are active. When LOW, the QB ₀ /nQB ₀ outputs are in a high-impedance state. LVC MOS/LVTTL interface levels.
17, 18	nQB ₀ , QB ₀	Output		Bank B differential output pair. LVDS interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C _{IN}	Input Capacitance			4		pF
R _{PULLUP}	Input Pullup Resistor			51		kΩ
R _{PULLDOWN}	Input Pulldown Resistor			51		kΩ

Table 3. Output Enable Function Table

Inputs		Outputs	
OEA	OEB	QA[0:1], nQA[0:1]	QB0, nQB0
0	0	High Impedance	High Impedance
1 (default)	1 (default)	Enabled	Enabled

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to $V_{DD} + 0.5V$
Outputs, I_O (LVDS) Continuos Current Surge Current	10mA 15mA
Package Thermal Impedance, θ_{JA}	86.7°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. LVDS Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ to $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		$V_{DD} - 0.16$	3.3	V_{DD}	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				75	mA
I_{DDA}	Analog Supply Current				16	mA
I_{DDO}	Output Supply Current				75	mA

Table 4B. LVC MOS/LV TTL DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ to $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		2		$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage		-0.3		0.8	V
I_{IH}	Input High Current	OEA, OEB	$V_{DD} = V_{IN} = 3.465V$		5	μA
		F_SEL0, F_SEL1, F_SEL2, MR	$V_{DD} = V_{IN} = 3.465V$		150	μA
I_{IL}	Input Low Current	OEA, OEB	$V_{DD} = 3.465V, V_{IN} = 0V$	-150		μA
		F_SEL0, F_SEL1, F_SEL2, MR	$V_{DD} = 3.465V, V_{IN} = 0V$	-5		μA

Table 4C. Differential DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0^\circ\text{C}$ to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK	$V_{DD} = V_{IN} = 3.465V$			150	μA
		nCLK	$V_{DD} = V_{IN} = 3.465V$			5	μA
I_{IL}	Input Low Current	CLK	$V_{DD} = 3.465V, V_{IN} = 0V$	-5			μA
		nCLK	$V_{DD} = 3.465V, V_{IN} = 0V$	-150			μA
V_{PP}	Peak-to-Peak Voltage; NOTE 1			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		$V_{DD} - 0.85$	V

NOTE 1: V_{IL} should not be less than -0.3V.NOTE 2: Common mode input voltage is defined as V_{IH} .**Table 4D. LVDS DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0^\circ\text{C}$ to 70°C**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		275	375	485	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.20	1.35	1.50	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

Table 5. AC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0^\circ\text{C}$ to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency		98		320	MHz
$j_{IT(cc)}$	Cycle-to-Cycle Jitter; NOTE 4				35	ps
$tsk(o)$	Output Skew; NOTE 4, 5				145	ps
$tsk(b)$	Bank Skew; NOTE 4, 6	Bank A			55	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	200		600	ps
odc	Output Duty Cycle		47		53	%
t_j	Phase Jitter Peak-to-Peak; NOTE 1, 3	100MHz output, Evaluation Band: 0Hz - Nyquist (clock frequency/2)		13.54		ps
		125MHz output, Evaluation Band: 0Hz - Nyquist (clock frequency/2)		13.13		ps
		250MHz output, Evaluation Band: 0Hz - Nyquist (clock frequency/2)		12.87		ps
$t_{REFCLK_HF_RMS}$	Phase Jitter RMS; NOTE 2, 3	100MHz output, High Band: 1.5MHz - Nyquist (clock frequency/2)		1.22		ps
		125MHz output, High Band: 1.5MHz - Nyquist (clock frequency/2)		1.17		ps
		250MHz output, High Band: 1.5MHz - Nyquist (clock frequency/2)		1.11		ps
$t_{REFCLK_LF_RMS}$	Phase Jitter RMS; NOTE 2, 3	100MHz output, Low Band: 10kHz - 1.5MHz		0.25		ps
		125MHz output, Low Band: 10kHz - 1.5MHz		0.22		ps
		250MHz output, Low Band: 10kHz - 1.5MHz		0.22		ps

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: Peak-to-peak jitter after applying system transfer function for the Common Clock Architecture. Maximum limit for PCI Express Gen 1 is 86ps peak-to-peak for a sample size of 10^6 clock periods. See IDT Application Note *PCI Express Reference Clock Requirements*, and also the *PCI Express Application section* of this datasheet which show each individual transfer function and the overall composite transfer function.

NOTE 2: RMS jitter after applying the two evaluation bands to the two transfer functions defined in the Common Clock Architecture and reporting the worst case results for each evaluation band. Maximum limit for PCI Express Generation 2 is 3.1ps rms for $t_{REFCLK_HF_RMS}$ (High Band) and 3.0 ps RMS for $t_{REFCLK_LF_RMS}$ (Low Band). See IDT Application Note *PCI Express Reference Clock Requirements* and also the *PCI Express Application section* of this datasheet which show each individual transfer function and the overall composite transfer function.

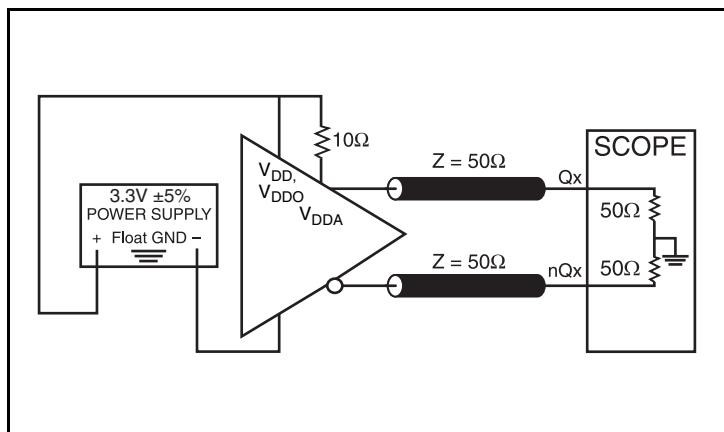
NOTE 3: Guaranteed only when input clock source is PCI Express Gen 2 compliant.

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

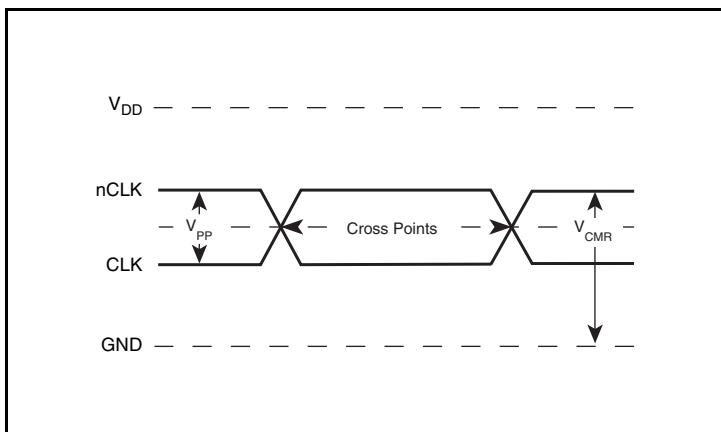
NOTE 5: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross points.

NOTE 6: Defined as skew within a bank of outputs at the same supply voltage and with equal load conditions.

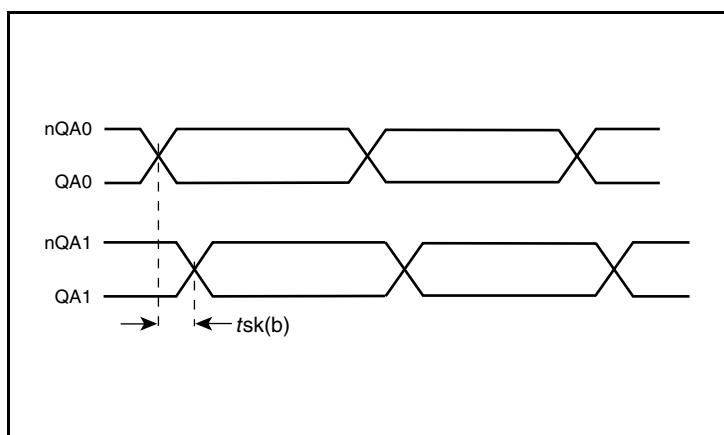
Parameter Measurement Information



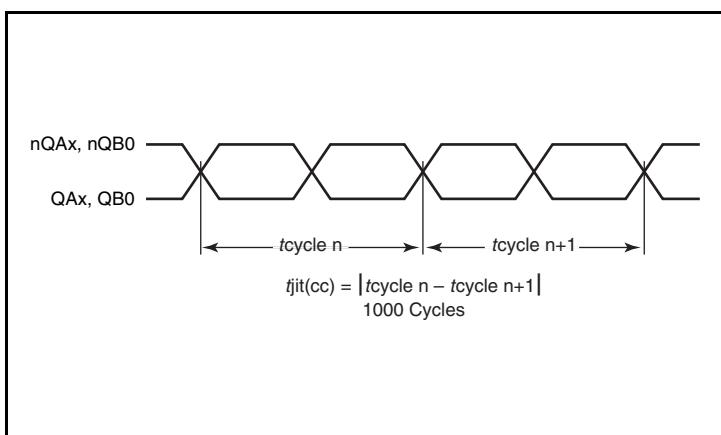
3.3V LVDS Output Load AC Test Circuit



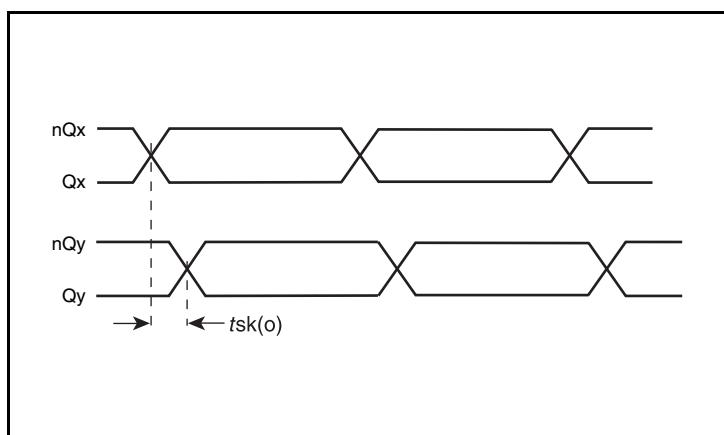
Differential Input Level



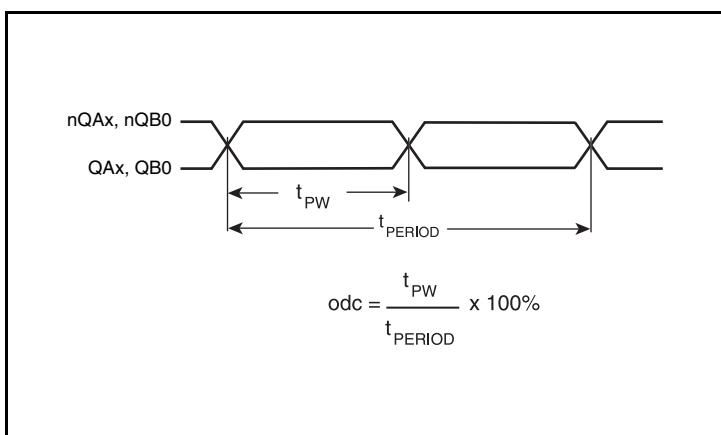
Bank Skew



Cycle-to-Cycle Jitter

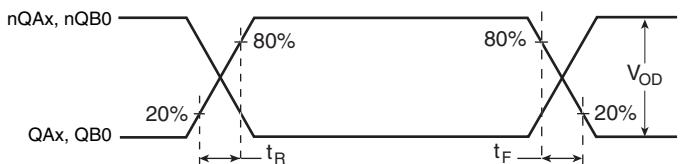


Output Skew

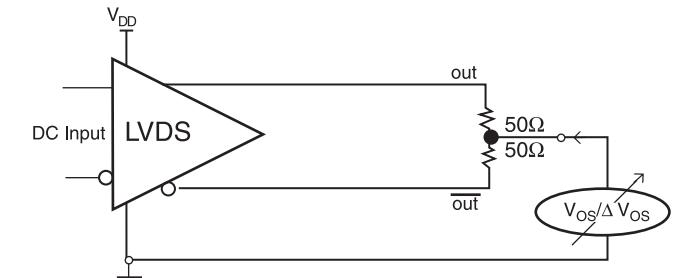


Output Duty Cycle/Pulse Width/Period

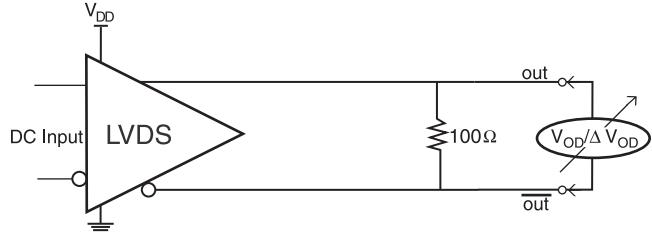
Parameter Measurement Information, continued



Output Rise/Fall Time



Offset Voltage Setup



Differential Output Voltage Setup

Application Information

Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS874003-05 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD} , V_{DDA} and V_{DDO} should be individually connected to the power supply plane through vias, and $0.01\mu F$ bypass capacitors should be used for each pin. Figure 1 illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional 10Ω resistor along with a $10\mu F$ bypass capacitor be connected to the V_{DDA} pin.

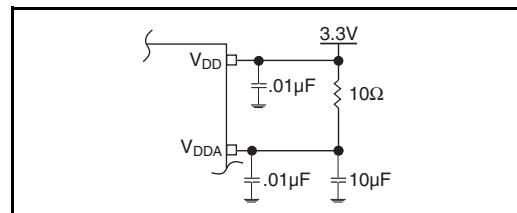


Figure 1. Power Supply Filtering

Wiring the Differential Input to Accept Single-Ended Levels

Figure 2 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_1 = V_{CC}/2$ is generated by the bias resistors $R1$ and $R2$. The bypass capacitor ($C1$) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of $R1$ and $R2$ might need to be adjusted to position the V_1 in the center of the input voltage swing. For example, if the input clock swing is 2.5V and $V_{CC} = 3.3V$, $R1$ and $R2$ value should be adjusted to set V_1 at 1.25V. The values below are for when both the single ended swing and V_{CC} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (R_o) and the series resistance (R_s) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, $R3$ and $R4$ in parallel should equal the transmission line

impedance. For most 50Ω applications, $R3$ and $R4$ can be 100Ω . The values of the resistors can be increased to reduce the loading for slower and weaker LVC MOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVC MOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than $-0.3V$ and V_{IH} cannot be more than $V_{CC} + 0.3V$. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

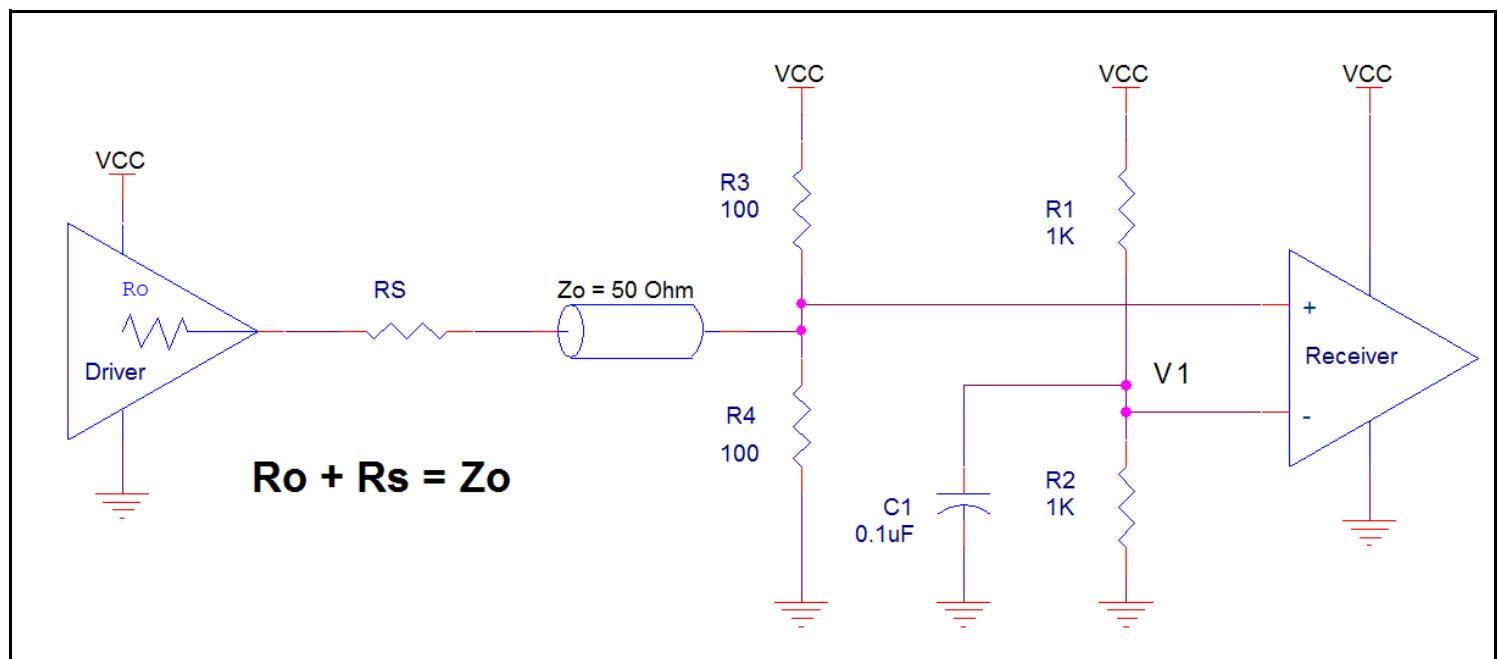


Figure 2. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both signals must meet the V_{PP} and V_{CMR} input requirements. Figures 3A to 3F show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the

vendor of the driver component to confirm the driver termination requirements. For example, in Figure 3A, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

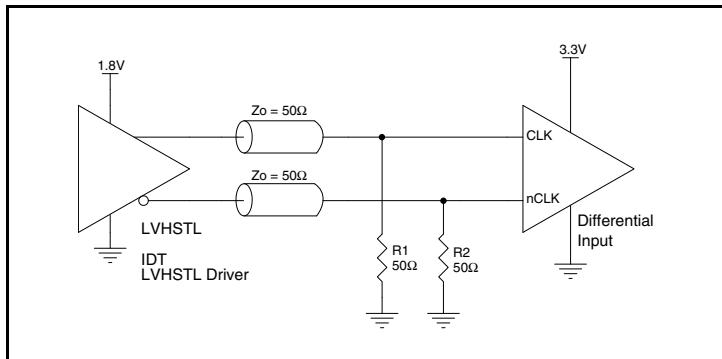


Figure 3A. CLK/nCLK Input Driven by an IDT Open Emitter LVHSTL Driver

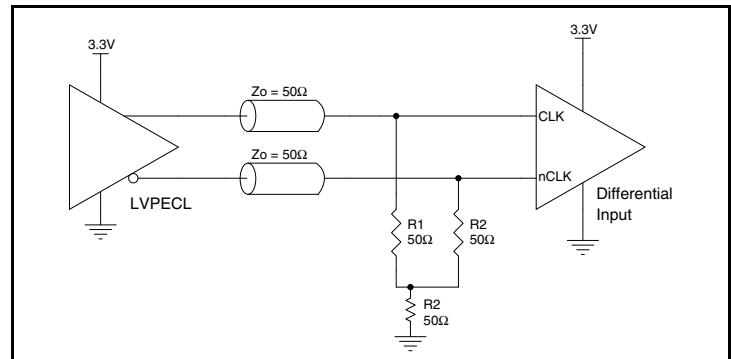


Figure 3B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

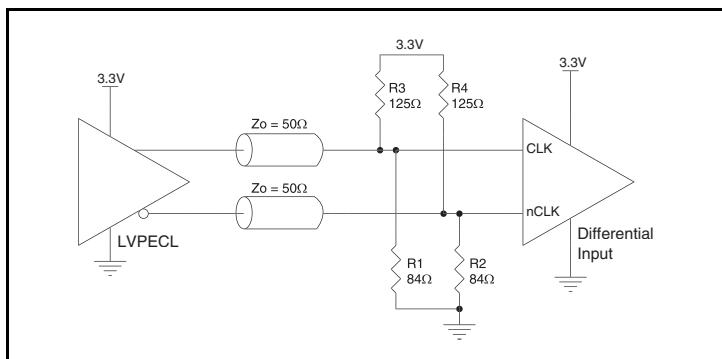


Figure 3C. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

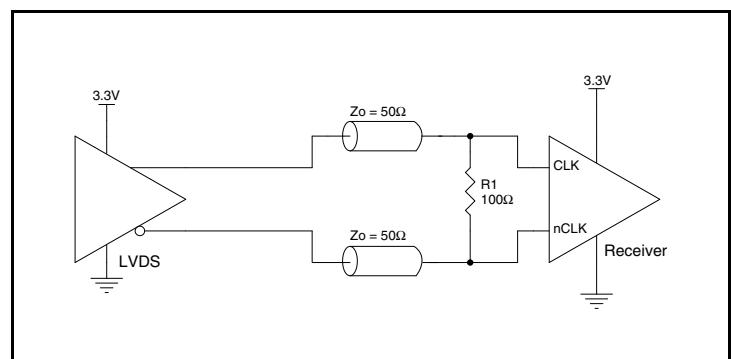


Figure 3D. CLK/nCLK Input Driven by a 3.3V LVDS Driver

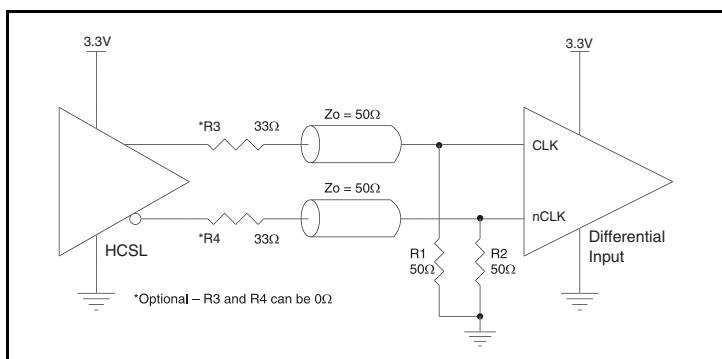


Figure 3E. CLK/nCLK Input Driven by a 3.3V HCSL Driver

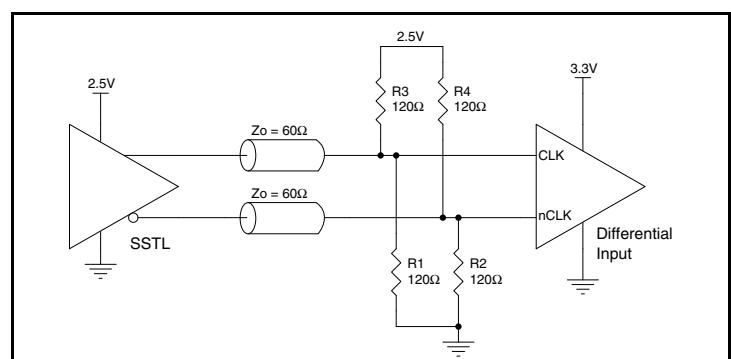


Figure 3F. CLK/nCLK Input Driven by a 2.5V SSTL Driver

Recommendations for Unused Input and Output Pins

Inputs:

LVC MOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A $1\text{k}\Omega$ resistor can be used.

Outputs:

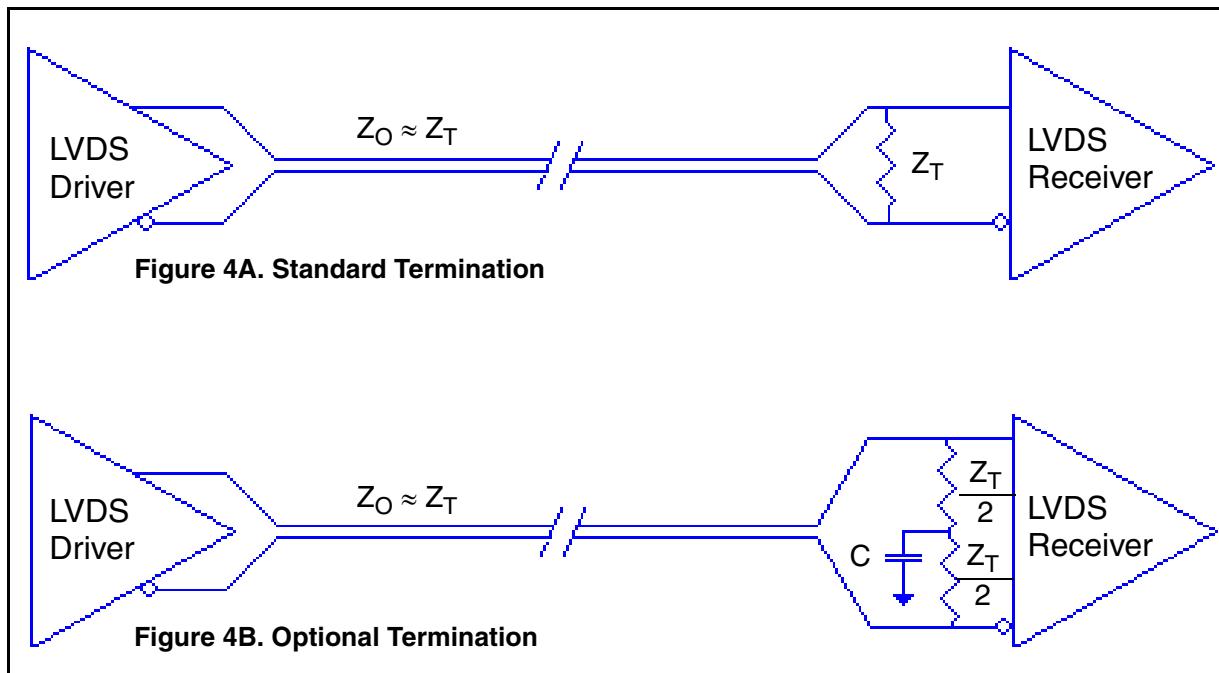
LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, there should be no trace attached.

LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω . The actual value should be selected to match the differential impedance (Z_0) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard

termination schematic as shown in *Figure 4A* can be used with either type of output structure. *Figure 4B*, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF . If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.



LVDS Termination

Schematic Example

Figure 5 shows an example of ICS874003-05 application schematic. In this example, the device is operated at $V_{DD} = 3.3V$. The decoupling capacitors should be located as close as possible to the power pin.

Two examples of LVDS terminations are shown in this schematic. The input is driven either by a 3.3V LVPECL driver or a 3.3V LVCMS.

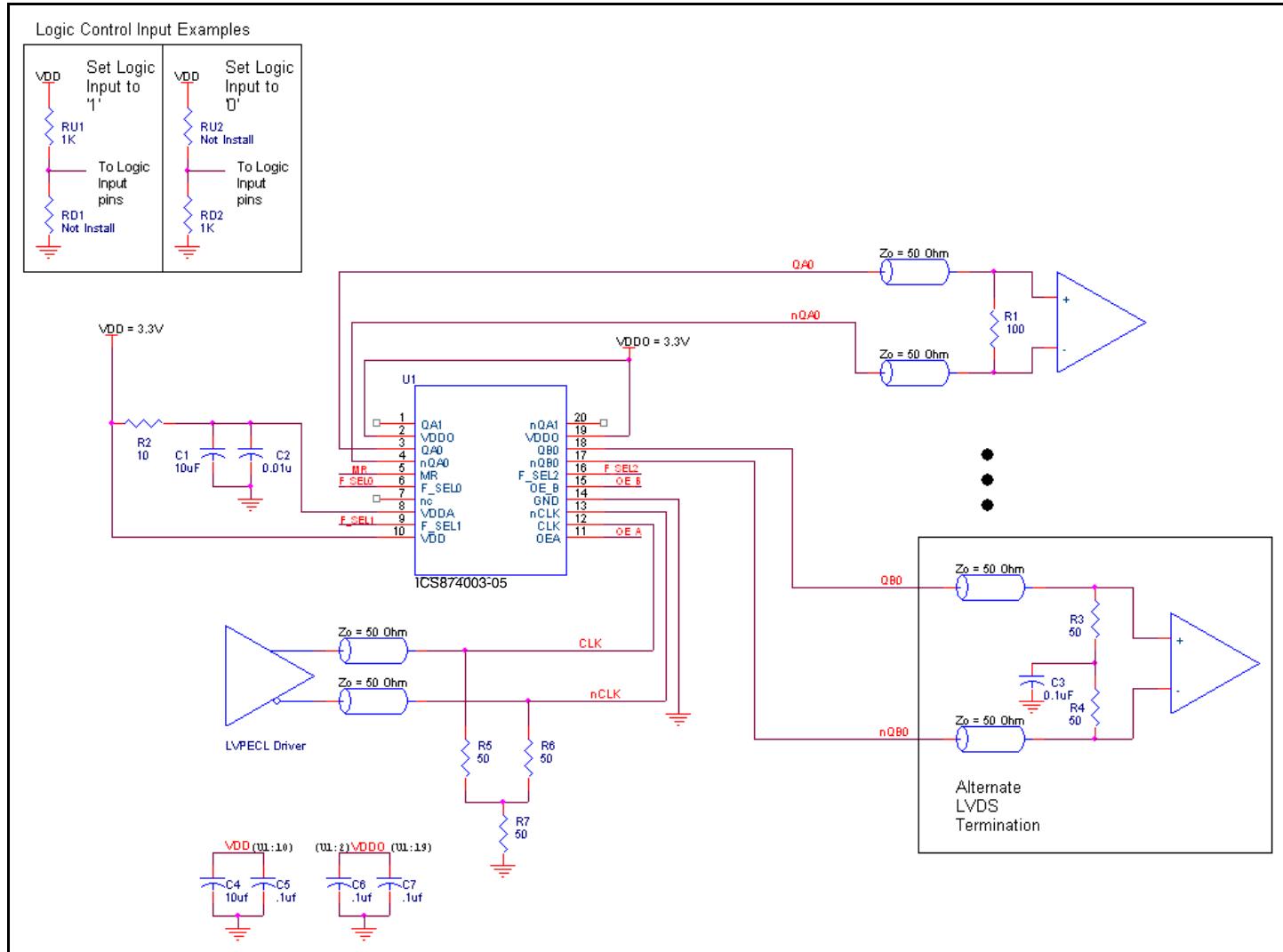


Figure 5. ICS874003-05 Schematic Example

PCI Express Application Note

PCI Express jitter analysis methodology models the system response to reference clock jitter. The block diagram below shows the most frequently used *Common Clock Architecture* in which a copy of the reference clock is provided to both ends of the PCI Express Link.

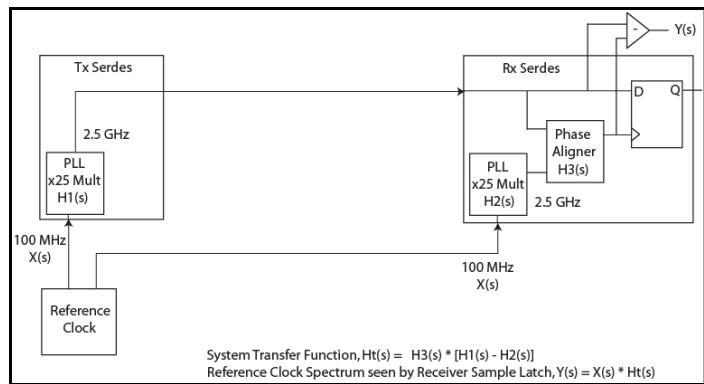
In the jitter analysis, the transmit (Tx) and receive (Rx) serdes PLLs are modeled as well as the phase interpolator in the receiver. These transfer functions are called H1, H2, and H3 respectively. The overall system transfer function at the receiver is:

$$Ht(s) = H3(s) \times [H1(s) - H2(s)]$$

The jitter spectrum seen by the receiver is the result of applying this system transfer function to the clock spectrum X(s) and is:

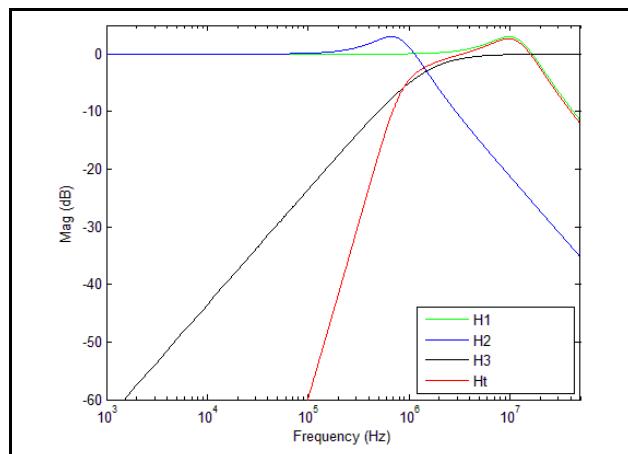
$$Y(s) = X(s) \times H3(s) \times [H1(s) - H2(s)]$$

In order to generate time domain jitter numbers, an inverse Fourier Transform is performed on $X(s) \times H3(s) \times [H1(s) - H2(s)]$.



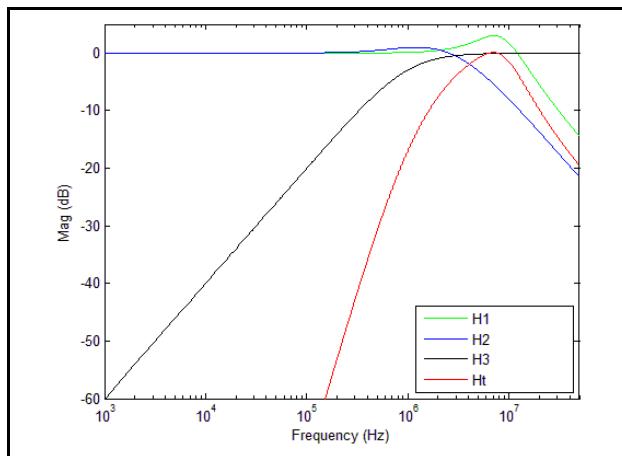
PCI Express Common Clock Architecture

For **PCI Express Gen 1**, one transfer function is defined and the evaluation is performed over the entire spectrum: DC to Nyquist (e.g. for a 100MHz reference clock: 0Hz – 50MHz) and the jitter result is reported in peak-peak.

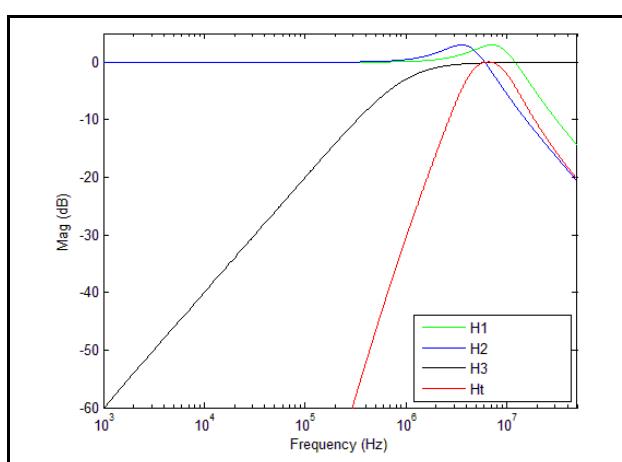


PCIe Gen 1 Magnitude of Transfer Function

For **PCI Express Gen 2**, two transfer functions are defined with 2 evaluation ranges and the final jitter number is reported in rms. The two evaluation ranges for PCI Express Gen 2 are 10kHz – 1.5MHz (Low Band) and 1.5MHz – Nyquist (High Band). The plots show the individual transfer functions as well as the overall transfer function Ht.

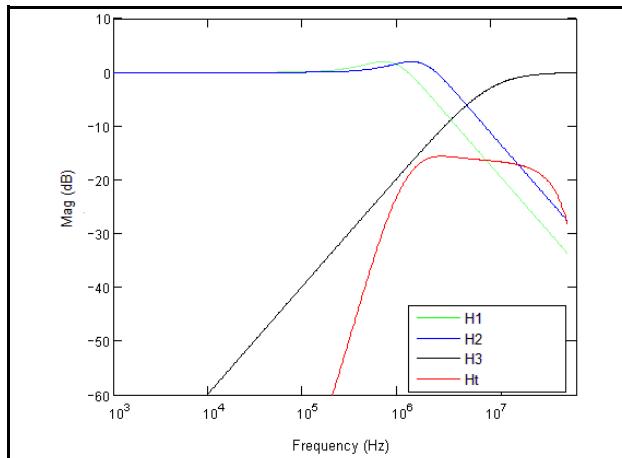


PCIe Gen 2A Magnitude of Transfer Function



PCIe Gen 2B Magnitude of Transfer Function

For **PCI Express Gen 3**, one transfer function is defined and the evaluation is performed over the entire spectrum. The transfer function parameters are different from Gen 1 and the jitter result is reported in RMS.



PCIe Gen 3 Magnitude of Transfer Function

For a more thorough overview of PCI Express jitter analysis methodology, please refer to IDT Application Note *PCI Express Reference Clock Requirements*.

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS874003-05. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS74003-05 is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for $V_{DD} = 3.3V + 5\% = 3.465V$, which gives worst case results.

- Power (core)_{MAX} = $V_{DD_MAX} * (I_{DD_MAX} + I_{DDA_MAX}) = 3.465V * (75mA + 16mA) = 315.315\text{mW}$
- Power (outputs)_{MAX} = $V_{DDO_MAX} * I_{DDO_MAX} = 3.465V * 75mA = 259.875\text{mW}$

Total Power_{MAX} = 315.3mW + 259.9mW = **575.2mW**

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2. Junction Temperature.

Junction temperature, T_j , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for devices is 125°C.

The equation for T_j is as follows: $T_j = \theta_{JA} * P_{d_total} + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

P_{d_total} = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 86.7°C/W per Table 6 below.

Therefore, T_j for an ambient temperature of 70°C with all outputs switching is:

$70^\circ\text{C} + 0.575\text{W} * 86.7^\circ\text{C/W} = 119.9^\circ\text{C}$. This is below the limit of 125°C.

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board.

Table 6. Thermal Resistance θ_{JA} for 20-Lead TSSOP, Forced Convection

θ_{JA} by Velocity			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	86.7°C/W	82.4°C/W	80.2°C/W

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Table 7. θ_{JA} vs. Air Flow Table for a 20-Lead TSSOP

θ_{JA} by Velocity			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	86.7°C/W	82.4°C/W	80.2°C/W

Transistor Count

The transistor count for ICS874003-05 is: 1418

Package Outline and Package Dimensions

Package Outline - G Suffix for 20-Lead TSSOP

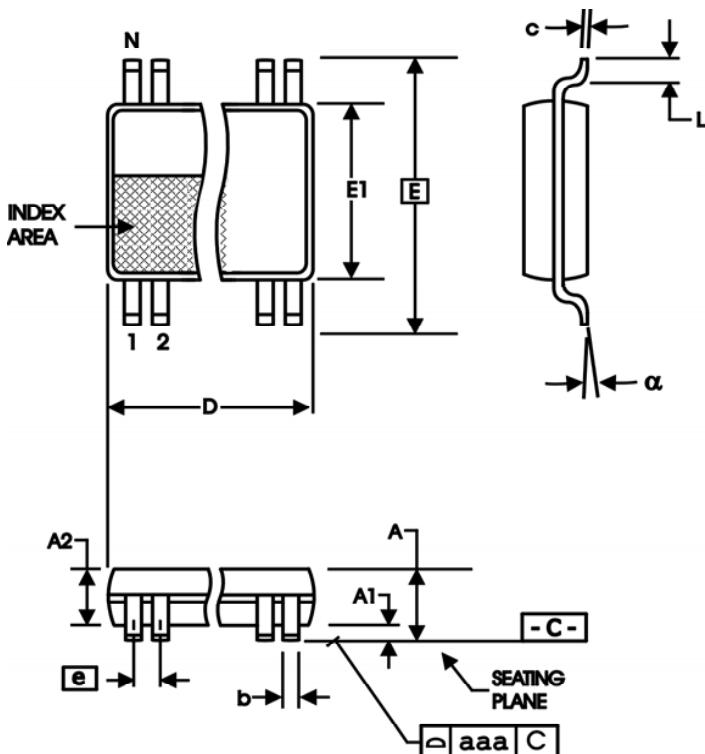


Table 8. Package Dimensions

All Dimensions in Millimeters		
Symbol	Minimum	Maximum
N	20	
A		1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
alpha	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
874003BG-05LF	ICS74003B05L	“Lead-Free” 20-Lead TSSOP	Tube	0°C to 70°C
874003BG-05LFT	ICS74003B05L	“Lead-Free” 20-Lead TSSOP	Tape & Reel	0°C to 70°C

Revision History Sheet

Rev	Table	Page	Description of Change	Date
B	T9	17	Corrected marking information in ordering table to accurately match the ABS document	11/09/11
B	T9	9 11 13 16	Updated the 'Wiring the Differential Input to Accept Single-Ended Levels' Note. Updated the 'LVDS Driver Termination' Note. Updated the 'PCI Express Application' Note. Added ICS prefix to marking information in the Ordering Table. Deleted quantity from Tape and Reel.	3/21/14

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