Programmable Multi Channel PMIC for Tablet PCs

Advanced Datasheet

IDTP9165

Features

- Operates from a 2.7V to 5.25V supply
- Five programmable, current-mode, step-down converters
  - Dynamic voltage scaling (12.5mV steps)
  - Automatic PWM/PFM transition at light load
  - 0.75V to 3.3V software programmable output voltage range
  - Two converters with 1.5A output current
  - One converter with 5A output current
  - One 10A or two 5A output current converters
  - Remote voltage sensing
  - Support for external power modules to increase DCD1 rail output current up to 20A
- 11 programmable general purpose LDOs
  - Eight 200mA, and three 160mA capable LDOs
  - DCD0 or DCD1 Tracking LDO
  - 1.0V to 5.25V input voltage range
  - 0.75V to 3.3V software programmable output voltage range
  - Always-on LDO for RTC with coin cell/SuperCap charging capability
- Low power RTC module
  - Counts seconds, minutes, hours, day, date, month and year
- 10-bit ADC
- Host interface and system management
  - Interrupt controller with mask-able interrupts,
  - Reset function
  - Power good monitoring
  - Programmable sequencing of output rails
- High speed I²C interface, 3.4Mbit/s
- Eight programmable GPIOs
- 84-lead 7mm x 7mm x 0.8mm dual-row QFN package

Applications

- Tablet PCs
- ClamShell
- SoC power management

Description

IDTP9165 is a programmable, multiple channel power management IC (PMIC). It includes 5 integrated, synchronous, step-down DC/DC regulators (DCD0a, DCD0b, DCD1 through DCD3), 11 LDOs (LDO0 through LDO9, and LDOTR), a Real Time Clock (RTC), a 10-bit ADC,, eight GPIOs (GPIO0 through GPIO7), and a high speed I²C interface (I²C bus address: 0x4F). The product is ideal for Tablet PCs and other multi rail applications and is specifically designed to support the power management requirements of quad-core processor platforms.

The PMIC DC/DC regulators can support the output current requirements for the CPU (DCD0) and SOC (DCD1) of the application processor with up to 10A and 5A, respectively. The output voltages are programmable from 0.7V to 1.5V.

DCD0 can be configured as a dual-phase, step-down regulator or as two single-phase regulators (DCD0a and DCD0b). Both DCD0 and DCD1 offer remote sensing of the rail voltage and dynamic voltage scaling (DVS) in 12.5mV steps. The DVS set output voltage slew rate is software adjustable. Furthermore, DCD1 supports the addition of external power modules (IDTP9167) to increase the output current to over 20A.

There are two step-down regulators (DCD2, DCD3) with output currents of up to 1.5A. Those regulators are output voltage software adjustable in 12.5mV steps. All step down switching regulators are current-mode controlled with a switching frequency of 2.1MHz.

Also integrated in the IDTP9165 are 11 software programmable LDOs with a wide output voltage range and with output currents capabilities up to 280mA. All LDOs are low noise, high PSRR, and low dropout regulators.

The output voltages of all regulators as well as device sequencing can be software programmable by writing to volatile registers through the I²C interface (Default address: 0x4F) or permanently programmed by OTP (One Time Programmable fuse cells). The PMIC operates from a single 2.7V to 5.25V supply. Additionally, the device has an internal high voltage regulator to supply the ONKEY button and RTC circuitry. This feature allows the complete shutdown of the pre-regulator in a dual-cell or triple-cell battery system, thus increasing the battery life of the tablet. IDTP9165 also provides a dedicated pin to sequence the DDR memory power supply.

The package for the IDTP9165 is a 7mm x 7mm, 84 lead, dual row QFN package. Operation through the commercial temperature range -40°C to +85°C is guaranteed.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings (AMR) are stress ratings only. Stresses greater than those listed below (Tables 1 and 2) may cause permanent damage to the device. Operation of the IDTP9165 at AMR is not implied. Exposure to AMR may affect long-term reliability.

Table 1 – Absolute Maximum Ratings.

PINS	MAXIMUM RATING	UNIT
VSEN0 to VGND, VSEN1 to VGND VINB to VGND XTAL0 to VGND, XTAL1 to VGND	-0.3 to 2.2	V
VBAT to VGND	-0.3 to 20	V
LDO0 to VGND, LDO1 to VGND	-0.3 to VINA + 0.3	V
LDO0 to VGND, LDOTR to VGND	-0.3 to VSYS + 0.3	V
LDO3 to VGND, LDO4 to VGND	-0.3 to VINB + 0.3	V
LDO5 to VGND	-0.3 to VINC + 0.3	V
LDO6 to VGND, LDO7 to VGND	-0.3 to VIND + 0.3	V
LDO8 to VGND, LDO9 to VGND	-0.3 to VINE + 0.3	V
GPIO0 through GPIO7 to VGND	-0.3 to VSYS + 0.3	V
PGNDA to VGND, PGNDB to VGND, PGND1 to VGND PGND2 to VGND, PGND3 to VGND, EP to VGND	-0.3 to 0.3	V
All Other Pins to VGND	-0.3V to 6.0	V

Table 2- Package Thermal Information

SYMBOL	DESCRIPTION	MAXIMUM RATING	UNIT
θ_{JA}	Thermal Resistance Junction to Ambient (NQG84 – QFN)	30.6	°C/W
θ_{JC}	Thermal Resistance Junction to Case (NQG84 – QFN)	21.9	°C/W
θ_{JB}	Thermal Characterization Junction to Board (NQG84 – QFN)	1.2	°C/W
T_J	Junction Temperature	-40 to +125	°C
T_A	Ambient Operating Temperature	-40 to +85	°C
T_{STG}	Storage Temperature	-55 to +150	°C
T_{LEAD}	Lead Temperature (soldering, 10s)	+300	°C

Note: The maximum power dissipation is $P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$ where $T_{J(MAX)}$ is 125°C. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the device will enter thermal shutdown.This thermal rating was calculated on a JEDEC 4 layer board (4.5”x4.0”), using a 0.169”x0.169” ePad soldered down, with 16 PCB Thermal vias, arranged in a 4x4 symmetrical array.Actual thermal resistance is affected by PCB size, solder joint quality, layer count, copper thickness, air flow, altitude, and other unlisted variables.

Table 3 – ESD Information

TEST MODEL	PINS	MAXIMUM RATING	UNIT
(HBM) Human Body Model	All (except PVIN2, PVIN3)	±2000	V
	PVIN2, PVIN3	±1000	
(CDM) Charge Device Model	All	±500	

ELECTRICAL CHARACTERISTICS

V_{INA}, V_{INC}, V_{IND}, V_{INE} = 5V, T_J = -40 to +125°C, unless otherwise noted. Typical values are at 25°C, unless otherwise noted.

Table 4. General Electrical Characteristics

SYMBOL	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
V_{BAT}	Input voltage operating range ***Note: Default option is C=1. Contact IDT marketing for other device options.***	Single-cell option (C=1)	2.7		6	V
		Two-cell option (C=2)	2.7		12	
		Three-cell option (C=3)	2.7		18	
	UVLO threshold, VBAT rising	Register UVLO [2:0] = 000 (default)		(2.8 x C)		
		Register UVLO [2:0] = 001		(2.9 x C)		
		Register UVLO [2:0] = 010		(3.0 x C)		
		Register UVLO [2:0] = 011		(3.1 x C)		
		Register UVLO [2:0] = 100		(3.2 x C)		
		Register UVLO [2:0] = 101		(3.3 x C)		
		Register UVLO [2:0] = 110		(3.4 x C)		
		Register UVLO [2:0] = 111		(3.5 x C)		
	UVLO Hysteresis, VBAT falling			-10		%
	Additional hysteresis (added to 10% UVLO hysteresis)	Register UVLOHYS [1:0] = 00		0		mV
		Register UVLOHYS [1:0] = 01		(100 x C)		
		Register UVLOHYS [1:0] = 10		(200 x C)		
		Register UVLOHYS [1:0] = 11		(300 x C)		
$I_{Q(VBAT)}$	VBAT quiescent current	Device in OFF state, RTC running, backup charger turned-on.		10		µA
V_{SYS}	Input voltage operating range		2.7		5.25	V
$I_{Q(VSYS)}$	VSYS quiescent current	Device in OFF state		1		µA
		Device in ON state, ADC disabled		125		µA
		Device in ON state, ADC enabled		190		µA
$V_{IL(PGPRE)}$	Low level input voltage				0.65	V
$V_{IH(PGPRE)}$	High level input voltage		1.35			V
V_{BAK}	UVLO threshold, VBAK rising	For RTC to start working	1.2		1.6	V
T_{SDN}	Thermal shutdown	Temperature increasing (Guaranteed by design)	125	132		°C
$t_{SDNfilt}$	Thermal shutdown filter time			3		ms

ELECTRICAL CHARACTERISTICS – DCD0,1,2,3 REGULATORS

Table 5. DCD0, (Dual Phase, 10A, DVS capable, Trim Options 1 & 2) Electrical Characteristics

$C_{O(DCD0)}$ = 47µFX4, L = 0.47µH, $V_{O(DCD0)}$ = 1.000V, V_{PVIN0} = V_{PVINA} = V_{PVINB} = 5V, T_A = 25°C

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
V_{PVIN0}	Input voltage range			2.7		5.25	V
$V_{O(DCD0)}$	Output voltage range			0.76		1.55	V
	Regulation voltage accuracy			-2		+2	%
	Line Regulation	V_{PVIN0} = 3V to 5V			0.03		%/V
	Load Regulation	I_{OUT} = 0.5A to 6A, PWM mode *(see **PWM definition**)*			0.3		mV/A
	Voltage resolution				12.5		mV
	Offset voltage in PFM mode $V_{O(PFM)}=V_{O(PWM)}+V_{offset}$	PFM mode *(see **PFM definition**)*			15		mV
$I_{SHDN(DCD0)}$	Shutdown current				1		µA
$SR_{(DCD0)}$	Slew rate during DVS	Register DCD0_SR [1:0]	00		12.5[1]		mV/µs
			01		25.0[1]		mV/µs
			10		37.5[1]		mV/µs
			11		50.0[1]		mV/µs
$I_{Q(DCD0)}$	Quiescent Current *(see **PWM definition**)*	No load, Forced PWM mode			30		mA
	*(see **PFM definition**)*	No load, Forced PFM mode			120		µA
$I_{OP(DCD0)}$	Continuous operating DC current	T_J < 115°C				8	A
$I_{PULSE(DCD0)}$	Pulsed Load Current	t_{LOAD} < 1ms			10[2]		A
$R_{(on)}$	High side switch	Per phase			60	80	mΩ
	Low side switch	Per phase			35	60	mΩ
$R_{DIS(DCD0)}$	Output discharge resistance				570	650	Ω
$f_{SW(DCD0)}$	Switching frequency	Forced PWM mode			2		MHz
$T_{ssr(DCD0)}$	Soft-start ramp rate				5		mV/µs
ΔV_{SEN0}	VSEN0 pin diff. voltage range				250		mV
Z_{VSEN0}	VSEN0 pin input impedance				1		MΩ
I_{FB0}	FB0 input bias current				2		µA
$V_{PGD(DCD0)}$	Power good voltage rising threshold	Output voltage increasing to programmed output voltage		-10	-8	-6	%

Table 6. DCD0a (Single Phase, 5A, DVS capable, Trim Option 3) Electrical Characteristics

$C_{O(DCD0)}$ = 47µFx2, L = 0.47µH, $V_{O(DCD0A)}$ = 1.000V, V_{PVIN0} = V_{PVINA} = V_{PVINB} = 5V, T_A = 25°C

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
V_{PVINA}	Input voltage range			2.7		5.25	V
$V_{O(DCD0a)}$	Output voltage range			0.76		1.55	V
	Regulation voltage accuracy			-2		+2	%
	Line Regulation	V_{PVIN0} = 3V to 5V			0.03		%/V
	Load Regulation	I_{OUT} = 0.5A to 6A, PWM mode			0.3		mV/A
	Voltage resolution				12.5		mV
	Offset voltage in PFM mode $V_{O(PFM)}=V_{O(PWM)}+V_{offset}$	PFM mode			15		mV
$I_{SHDN(DCD0a)}$	Shutdown current				1		µA
$SR_{(DCD0)}$	Slew rate during DVS	Register DCD0_SR [1:0]	00		12.5[1]		mV/µs
			01		25.0[1]		mV/µs
			10		37.5[1]		mV/µs
			11		50.0[1]		mV/µs
$I_{Q(DCD0a)}$	Quiescent Current	No load, Forced PWM mode			15		mA
		PFM mode			80		µA
$I_{OP(DCD0a)}$	Continuous operating DC current	T_J < 115°C				4	A
$I_{PULSE(DCD0a)}$	Pulsed Load Current	t_{Load} < 1ms			5[3]		A
$R_{(on)}$	High side switch				60	80	mΩ
	Low side switch				35	60	mΩ
$R_{DIS(DCD0a)}$	Output discharge resistance				570	650	Ω
$f_{SW(DCD0a)}$	Switching frequency	PWM mode			2		MHz
$T_{ssr(DCD0a)}$	Soft-start ramp rate				5[3]		mV/µs
ΔV_{SENA}	VSENA pin diff. voltage range				250		mV
Z_{VSENA}	VSENA pin input impedance				1		MΩ
I_{FBA}	FBA input bias current				1	1.8	µA

Table 7. DCD0b (Single Phase, 5A, NOT DVS capable, Trim Option 3) Electrical Characteristics

$C_{O(DCD0b)}$ = 47µFx2, L = 0.47µH, $V_{O(DCD0b)}$ = 1.000V, V_{PVIN0} = V_{PVINA} = V_{PVINB} = 5V, T_A = 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{PVIN0}	Input voltage range		2.7		5.25	V
$V_{O(DCD0b)}$	Output voltage range		0.76		1.55	V
	Regulation voltage accuracy		-2		+2	%
	Line Regulation	V_{PVIN0} = 3V to 5V		0.03		%/V
	Load Regulation	I_{OUT} = 0.5A to 6A, PWM mode		0.3		mV/A
	Voltage resolution			12.5		mV
	Offset voltage in PFM mode $V_{O(PFM)}=V_{O(PWM)}+V_{offset}$	PFM mode		15		mV
$I_{SHDN(DCD0b)}$	Shutdown current			1		µA
$I_{Q(DCD0a)}$	Quiescent Current	No load, Forced PWM mode		15		mA
		No load, Forced PFM mode		80		µA
$I_{OP(DCD0a)}$	Continuous operating DC current	T_J < 115°C			4	A
$I_{PULSE(DCD0a)}$	Pulsed Load Current	t_{Load} < 1ms		5[3]		A
$R_{(on)}$	High side switch			60	80	mΩ
	Low side switch			35	60	mΩ
$R_{DIS(DCD0a)}$	Output discharge resistance			570	650	Ω
$f_{SW(DCD0a)}$	Switching frequency	PWM mode		2		MHz
$T_{ssr(DCD0a)}$	Soft-start ramp rate			5		mV/µs
I_{FBB}	FBA input bias current			1	1.8	µA

Table 8. DCD1 (Single-Phase Step-Down Regulator) Electrical Characteristics

$C_{O(DCD1)}$ = 47µFx 2, L = 1µH, $V_{O(DCD1)}$ = 1.000V, V_{PVIN1} = 5V, T_A = 25°C

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
$V_{IN(DCD1)}$	Input voltage range			2.7		5.25	V
$V_{O(DCD1)}$	Output voltage range	LDOTR tracking disabled		0.76		1.55	V
		LDOTR tracking enabled		0.6		1.5	V
	Regulation voltage accuracy			-2		+2	%
	Line Regulation	V_{PVIN1} = 3V to 5V			0.03		%/V
	Load Regulation	I_{OUT} = 0.5A to 3A, PWM mode			0.3		mV/A
	Voltage resolution				12.5		mV
	Offset voltage in PFM mode $V_{O(PFM)} = V_{O(PWM)} + V_{offset}$	PFM mode			15		mV
$I_{SHDN(DCD1)}$	Shutdown current				1		µA
$SR_{(DCD1)}$	Slew rate during DVS	Resgister DCD0_SR [1:0]	00		12.5[1]		mV/µs
			01		25.0[1]		mV/µs
			10		37.5[1]		mV/µs
			11		50.0[1]		mV/µs
$I_{Q(DCD1)}$	Quiescent Current	No load, Forced PWM mode			15		mA
		No load, Forced PFM mode			80		µA
$I_{OP(DCD1)}$	Continuous operating DC current	T_J < 115°C				4	A
$I_{PULSE(DCD1)}$	Pulsed Load Current	t_{Load} < 1ms			5.0[3]		A
$R_{(on)}$	High side switch				60	80	mΩ
	Low side switch				35	60	mΩ
$R_{DIS(DCD1)}$	Output discharge resistance				570	650	Ω
$f_{SW(DCD1)}$	Switching frequency	PWM mode			2		MHz
$T_{ssr(DCD1)}$	Soft-start ramp rate				5		mV/µs
ΔV_{SEN1}	VSEN1 diff. voltage range				250		mV
Z_{VSEN1}	VSEN1 input impedance				1		MΩ
I_{FB1}	FB1 input bias current				1	1.8	µA

Table 9. DCD2 (Single-Phase Step-Down Regulator) Electrical Characteristics

$C_{O(DCD2)}$ = 22µF, L = 2.2µH, $V_{O(DCD2)}$ = 1.8V, V_{PVIN2} = 5V, T_A = 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{PVIN2}	Input voltage range		2.7		5.25	V
$V_{O(DCD2)}$	Output voltage range		0.76		3.3	V
	Regulation voltage accuracy	DCD2_RNG[1:0] = 01	-2		+2	%
	Line Regulation	V_{PVIN2} = 3V to 5V		0.03		%/V
	Load Regulation	I_{OUT} = 0.2A to 1.5A, PWM mode		0.3		mV/A
	Offset voltage in PFM mode $V_{O(PFM)} = V_{O(PWM)} + V_{offset}$	PFM mode		15		mV
$I_{SHDN(DCD2)}$	Shutdown current			1		µA
$I_{Q(DCD2)}$	Quiescent Current	No load, PFM mode		60		µA
$I_{OP(DCD2)}$	Continuous operating DC current	T_J < 115°C			1.5	A
$I_{PULSE(DCD2)}$	Pulsed Load Current	t_{Load} < 1ms		2		A
$R_{(on)}$	High side switch			125	160	mΩ
	Low side switch			75	100	mΩ
$R_{DIS(DCD2)}$	Output discharge resistance			1000	1300	Ω
$f_{SW(DCD2)}$	Switching frequency	PWM mode		2		MHz
$T_{ssr(DCD2)}$	Soft-start ramp rate			5		mV/µs
I_{FB2}	FB2 input bias current	$V_{O(DCD2)}$ > 2.6625V		3	4	µA

Table 10. DCD3 (Single-Phase Step-Down Regulator) Electrical Characteristics

$C_{O(DCD3)}$ = 22µF, L = 2.2µH, $V_{O(DCD3)}$ = 1.35V, V_{PVIN3} = 5V, T_A = 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{PVIN3}	Input voltage range		2.7		5.25	V
$V_{O(DCD3)}$	Output voltage range		0.76		3.3	V
	Regulation voltage accuracy		-2		+2	%
	Line Regulation	V_{PVIN3} = 3V to 5V		0.03		%/V
	Load Regulation	I_{OUT} = 0.2A to 1.5A, PWM mode		0.3		mV/A
	Offset voltage in PFM mode $V_{O(PFM)} = V_{O(PWM)} + V_{offset}$	PFM mode		15		mV
$I_{SHDN(DCD3)}$	Shutdown current			1		µA
$I_{Q(DCD3)}$	Quiescent Current	No load, Forced PFM mode		60		µA
$I_{OP(DCD3)}$	Continuous operating DC current	T_J < 115°C			1.5	A
$I_{PULSE(DCD3)}$	Pulsed Load Current	t_{Load} < 1ms		2		A
$R_{(on)}$	High side switch			125	160	mΩ
	Low side switch			75	100	mΩ
$R_{DIS(DCD3)}$	Output discharge resistance			1000	1300	Ω
$f_{SW(DCD3)}$	Switching frequency	Forced PWM mode		2		MHz
$T_{ssr(DCD3)}$	Soft-start ramp rate			5		mV/µs
I_{FB3}	FB3 input bias current	$V_{O(DCD3)}$ > 2.6625V		3	4	µA

ELECTRICAL CHARACTERISTICS -LDO Regulators

Table 11. LDO0, 1, 2, 5 Electrical Characteristics

C_O = 1µF, V_{IN} > V_O + 0.3V, T_A = 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range		2.40		5.25	V
V_O	Output voltage range		1.00		3.35	V
I_{SHDN}	Shutdown current			0.1		µA
I_Q	Quiescent current	No Load		18		µA
	Regulation voltage accuracy		-2		+2	%
	Line regulation			30	160	ppm/V
	Load regulation	LDO1, 5		2	4	µV/mA
		LDO0, 2		5	30	
I_O	Output current				200	mA
I_{LIM}	Internal current limit		260			mA
V_{drop}	Dropout voltage	I_O = 200mA, V_{IN} > 2.8V			300	mV
R_{DIS}	Output discharge resistance			10		kΩ
PSRR	Ripple rejection ratio	1V input to output, I_O = 40mA				dB
		< 200Hz		> 120		
		1kHz		120		
		10kHz		90		
		100kHz		53		
	Output noise voltage	V_O = 1.2V, V_{IN} > 2.8V I_O = 100µA, BW = 10Hz to 100kHz		52		$µV_{RMS}$
T_{ss}	Start-up time				120	µs
T_{ssr}	LDO soft-start ramp rate			35		mV/µs
C_O	External output capacitor	De-rated value	0.7		1.2	µF

Table 12. LDOTR (Tracking LDO) Electrical Characteristics

C_O = 2.2µF, V_{IN} > V_O + 0.3V, T_A = 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range		2.4		5.25	V
V_O	Output voltage range		0.6		1.5	V
I_{SHDN}	Shutdown current			0.1		µA
I_Q	Quiescent current	No Load		23		µA
	Regulation voltage accuracy		-2		+2	%
	Line regulation			15	90	ppm/V
	Load regulation			2	4	µV/mA
I_O	Output current				160	mA
I_{LIM}	Internal current limit		280			mA
R_{DIS}	Output discharge resistance			10		kΩ
PSRR	Ripple rejection ratio	1V input to output, I_O = 40mA				dB
		< 200Hz		> 120		
		1kHz		120		
		10kHz		90		
		100kHz		53		
	Output noise voltage	V_O = 0.90V, V_{IN} > 2.8V I_O = 100µA, BW = 10Hz to 100kHz, Tracking disabled		32		μV_{RMS}
T_{ss}	Start-up time	(GBD)			120	µs
T_{ssr}	LDO soft-start ramp rate			35		mV/µs
C_O	External output capacitor	De-rated value	1.6		2.5	µF

Table 13– LDO3, 4 Electrical Characteristics

C_O = 2.2µF, V_{IN} > V_O + 0.3V, T_A = 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range		1.0		2.0	V
V_O	Output voltage range		1.000		1.475	V
I_{SHDN}	Shutdown current			0.5		µA
I_Q	Quiescent current	No Load		19		µA
	Regulation voltage accuracy		-2		+2	%
	Line regulation			1	300	ppm/V
	Load regulation			6	20	µV/mA
I_O	Output current				160	mA
I_{LIM}	Internal current limit		200			mA
V_{drop}	Dropout voltage	I_O = 160mA, V_{IN} > 1.2V			120	mV
R_{DIS}	Output discharge resistance			10		kΩ
PSRR	Ripple rejection ratio	1V input to output, I_O = 30mA				dB
		< 200Hz		> 120		
		1kHz		120		
		10kHz		95		
		100kHz		57		
	Output noise voltage	V_O = 1.0V, V_{IN} = 1.8V I_O = 100µA, BW = 10Hz to 100kHz		28		μV_{RMS}
T_{ss}	Start-up time	(GBD)			120	µs
T_{ssr}	LDO soft-start ramp rate			30		mV/µs
C_O	External output capacitor	De-rated value	1.6		2.5	µF

Table 14– LDO6, 7, 8, 9 Electrical Characteristics

C_O = 1µF, V_{IN} > V_O + 0.3V, T_A = 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range		1.7		5.25	V
V_O	Output voltage range		1.00		3.35	V
I_{SHDN}	Shutdown current			0.1		µA
I_Q	Quiescent current	No Load		19		µA
	Regulation voltage accuracy		-2		+2	%
	Line regulation			50	100	ppm/V
	Load regulation	LDO7, 9		1	3	µV/mA
		LDO6, 8		1	50	
I_O	Output current				200	mA
I_{LIM}	Internal current limit		260			mA
V_{drop}	Dropout voltage	I_O = 200mA, V_{IN} > 1.8V			440	mV
R_{DIS}	Output discharge resistance			10		kΩ
PSRR	Ripple rejection ratio	1V input to output, I_O = 40mA				dB
		< 200Hz		> 120		
		1kHz		120		
		10kHz		90		
		100kHz		53		
	Output noise voltage	V_O = 1.2V, V_{IN} > 2.8V I_O = 100µA, BW = 10Hz to 100kHz		34		$µV_{RMS}$
T_{ss}	Start-up time	(GBD)			120	µs
T_{ssr}	LDO soft-start ramp rate			35		mV/µs
C_O	External output capacitor	De-rated value	0.7		1.2	µF

ELECTRICAL CHARATERISTICS - Charger

Table 15– Charger Module Electrical Characteristics

T_A = 25°C

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
$V_{O(BAK)}$	Output voltage setting	VBAK_VCHG[1:0]	00		Disabled		V
			01		2.6		
			10		3.0		
			11		3.3		
	Regulation voltage accuracy			-1.5		+1.5	%
$I_{O(BAK)}$	Maximum Output current	CC mode		0.7	1.2	1.9	A
$I_{LIM(BAK)}$	Internal series resistance	VBAK_RCHG[1:0]	00		250		Ω
			01		1K		
			10		2K		
			11		4K		
$C_{O(BAK)}$	External output capacitor	Optional			1.0		µF

ELECTRICAL CHARACTERISTICS - GPIO

Table 16– GPIO Interface Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OL(GPIO)}$	Low level output voltage	$I_{OL(GPIO)}$ = 12mA, OD mode			0.4	V
		$I_{OL(GPIO)}$ = 4mA, PP mode			0.4	V
$V_{OH(GPIO)}$	High level output voltage	$I_{OH(GPIO)}$ = -4mA	VIO-0.4V			V
$V_{IL(GPIO)}$	Low level input voltage				0.6	V
$V_{IH(GPIO)}$	High level input voltage		1.5			V
$I_{LK(GPIO)}$	Input leakage current				1	µA
$I_{SK(GPIO)}$	Sink current	GPIO in input mode		1		µA
V_{IO1}	VIO1 supply input range		1.5		VSYS	V
V_{IO2}	VIO2 supply input range		1.5		VSYS	V

ELECTRICAL CHARACTERISTICS - ADC

Table 17– ADC Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{REF}	ADC reference voltage	Internally provided		1.2		V
$I_{DD(ADC)}$	Supply Current	Full scale current		60		µA
RES	ADC resolution	External pins ANLGx		10		Bits
INL	Integral Non Linearity	External pins ANLGx (GBD)	-2		+2	LSB
DNL	Differential Non Linearity	External pins ANLGx (GBD)	-1		+1	LSB
Gain	Gain Error	External pins ANLGx (GBD)	-2		+2	LSB
F_S	Conversion rate			50		kS/s
$V_{MEAS(ADC)}$	ADC input voltage	External pins ANLGx (GBD)	0		1.2	V
		VSYS (GBD)	0		5.6	V
		VBAT (GBD)	0		4.4	V
SF	Voltage scale factor	External pins ANLGx		1.0		V/V
		VSYS		3/14		V/V
		VBAT		3/11		V/V
$R_{IN(ANLGx)}$	ANLGx input resistance			10		MΩ

ELECTRICAL CHARACTERISTICS – RTC

Table 18– RTC Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
T_A = 25°C						
$V_{IN(RTC)}$	RTC supply voltage		1.6		VBAK	V
$I_{DD(RTC)}$	RTC supply current			4	5	µA
UVLO		Voltage rising	2.0		2.4	V
		Voltage falling	1.2		1.6	V
Crystal oscillator						
f_O	Crystal frequency			32.768		kHz
ESR	Crystal series resistor		5		70	kΩ
C_{PIN}	Effective total capacitance per pin to ground			7.2		pF
$t_{Start(OSC)}$	Oscillator startup time				400	ms
CK32 output						
V_{CK32}	CK32 output voltage				VIO0/1	V
$V_{OL(CK32)}$	Low level output voltage	$I_{OL(CK32)}$ = 12mA, OD mode			0.4	V
		$I_{OL(CK32)}$ = 4mA, PP mode			0.4	V
$V_{OH(CK32)}$	High level output voltage	$I_{OH(CK32)}$ = -4mA	VIO-0.4V			V
t_r/t_f	CK32 rise and fall time	CL_{CK32} = 35pF			tbd	ns

ELECTRICAL CHARACTERISTICS - I²C Interface

Table 19– I²C Electrical Characteristics

Unless otherwise specified, typical values at T_A = 25°C, V_{DD}=V_{IO1}, T_A = 40°C to +85°C.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Low level input voltage	$I_{OL(GPIO)}$ = 3mA	-0.5		0.3V_{DD}	V
V_{IH}	High level input voltage		0.7V_{DD}		V_{DD}+0.5	V
V_{HYS}	Input hysteresis		0.1V_{DD}			V
V_{OL}	Low-level output voltage	V_{DD} > 2V, 3mA sink current, (open-drain)	0		0.4	V
		V_{DD} < 2V, 3mA sink current, (open-drain)	0		0.2V_{DD}	V
t_{FDA}	Fall time of SDAH signal	Capacitive load from 10pF to 100pF	10		80	ns
		Capacitive load of 400pF	20		160	ns
t_{SP}	Pulse width of spikes that must be suppressed by the pulse width input filter	SDAH and SDAL	0		10	ns
I_I	Input current each I/O pin				10	mA
C_I	Capacitance for each I/O pin				10	pF

I²C – Interface Timing

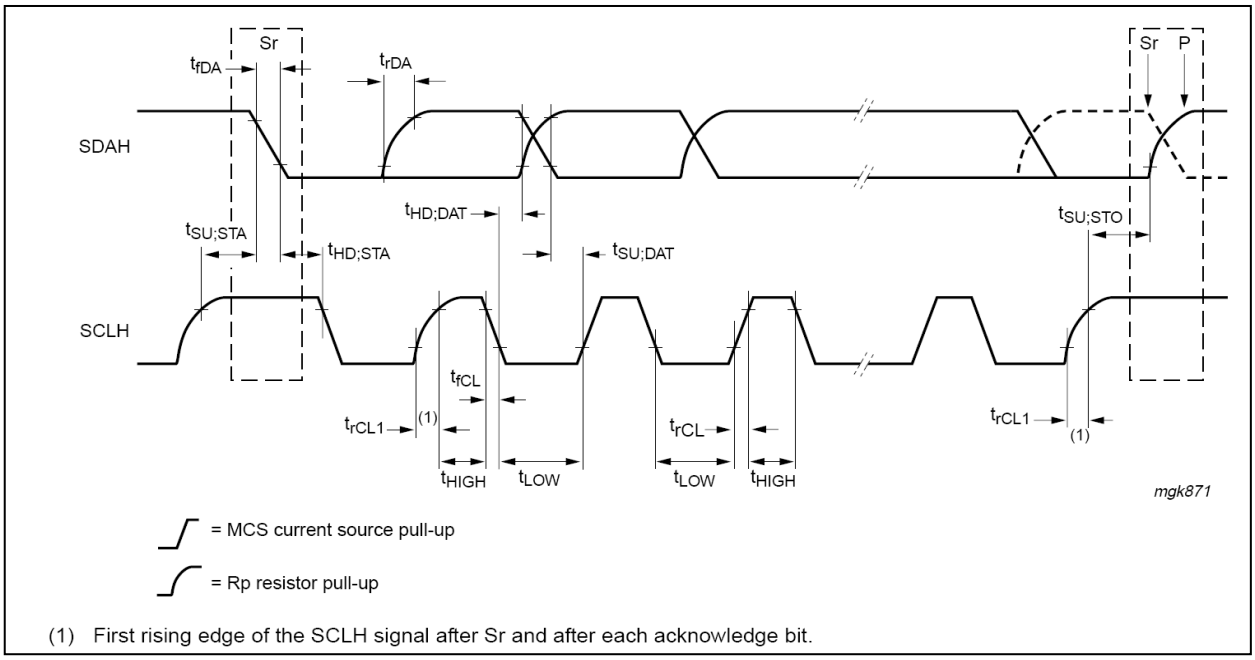


Figure 1. I²C Interface Timing

TYPICAL PERFORMANCE CHARACTERISTICS – DCD0

$C_{O(DCD0)}$ = 150µF, L = 0.47µH, $V_{O(DCD0)}$ = 1.000V, V_{PVIN0} = V_{PVINA} = V_{PVINB} = 5V, T_A = 25°C

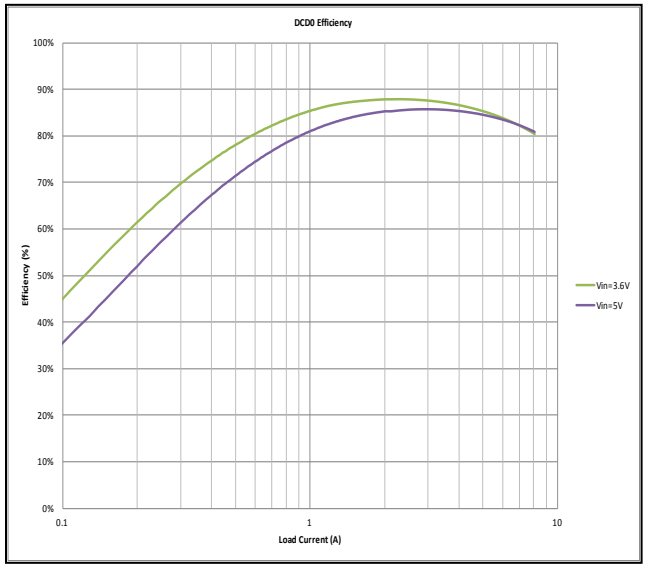


Figure 2. Efficiency

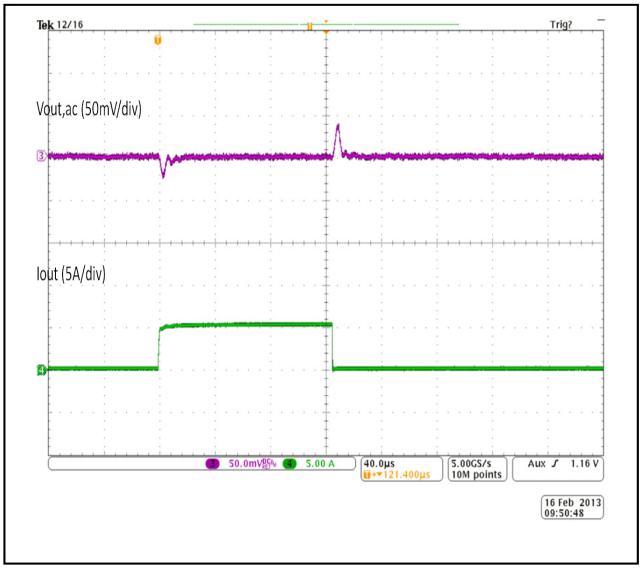


Figure 3. Transient Response (100mA-6A)

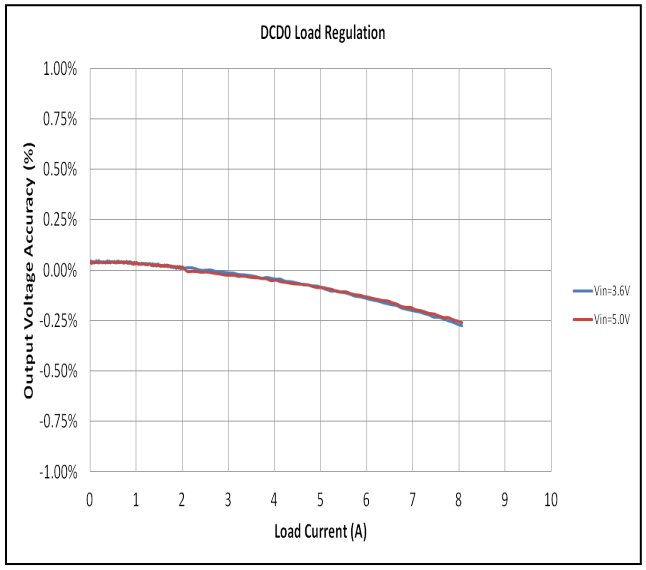


Figure 4. Load Regulation

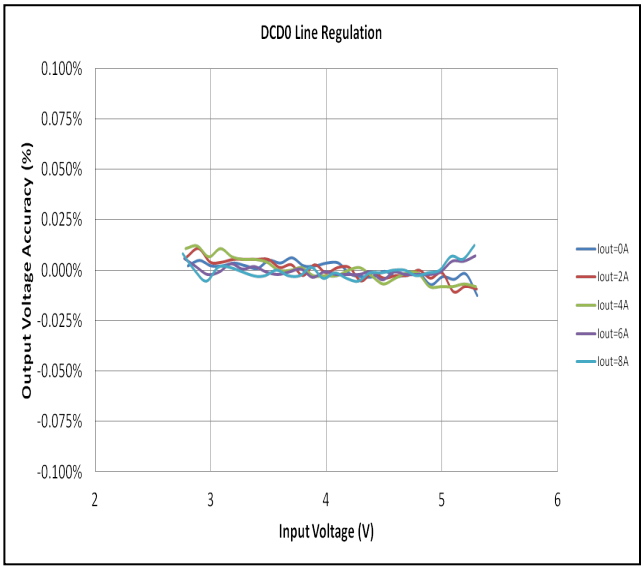


Figure 5. Line Regulation

TYPICAL PERFORMANCE CHARACTERISTICS – DCD1

$C_{O(DCD1)}$ = 68µF, L = 1µH, $V_{O(DCD1)}$ = 1.000V, V_{PVIN1} = 5V, T_A = 25°C

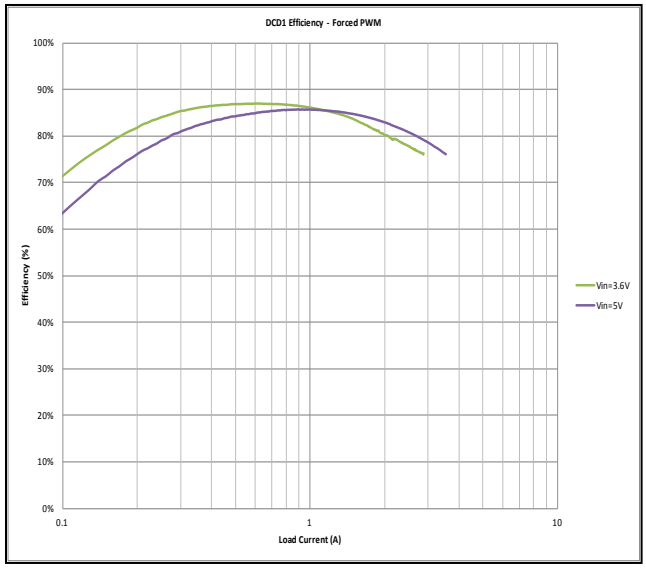


Figure 6. Efficiency

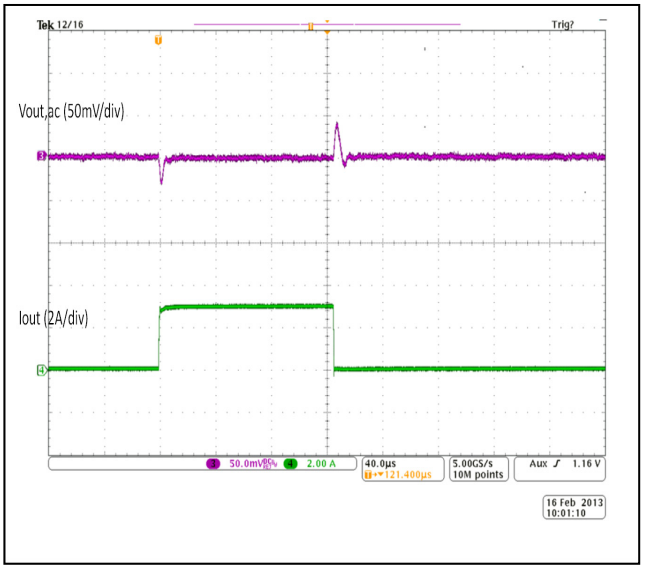


Figure 7. Transient Response (100mA – 3A)

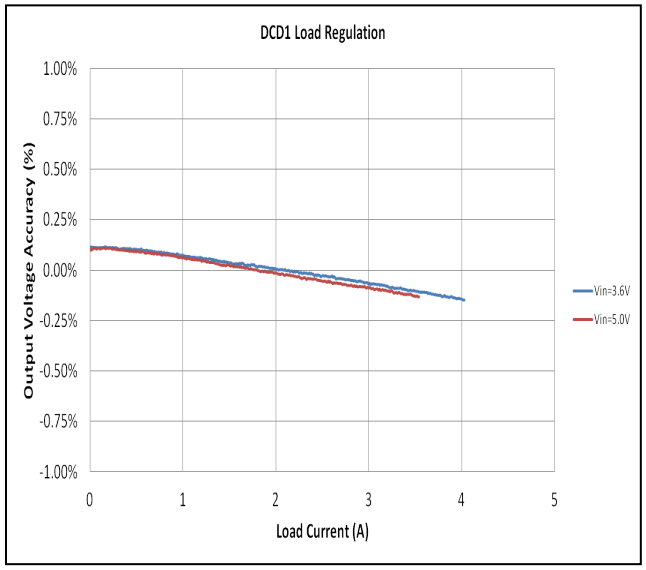


Figure 8. Load Regulation

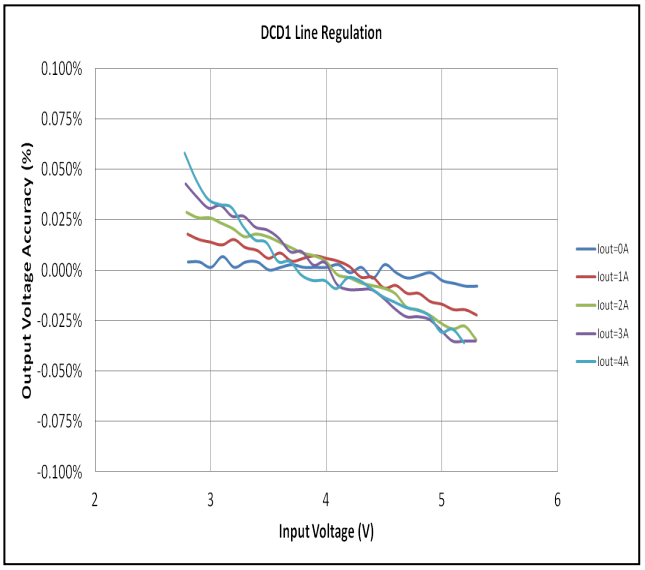


Figure 9. Line Regulation

TYPICAL PERFORMANCE CHARACTERISTICS – DCD2

$C_{O(DCD2)}$ = 22µF, L = 2.2µH, $V_{O(DCD2)}$ = 1.8V, V_{PVIN2} = 5V, T_A = 25°C

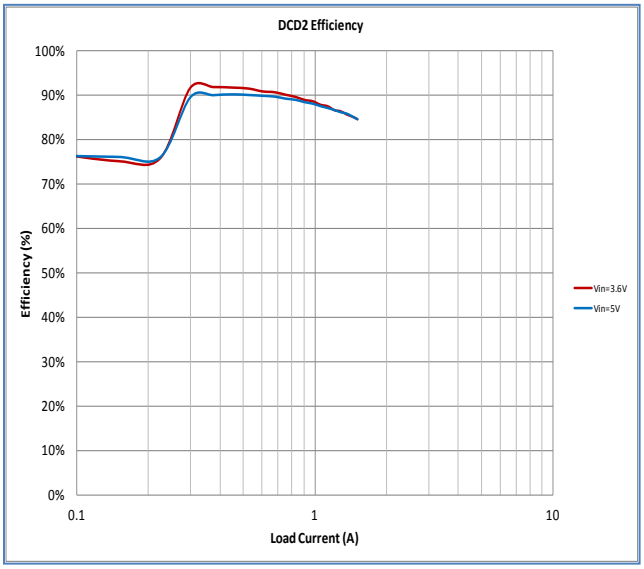


Figure 10. Efficiency

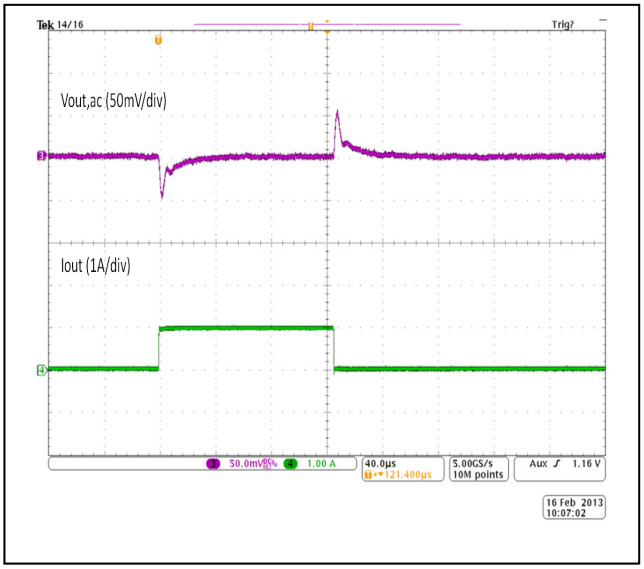


Figure 11. Transient Response (100mA – 1A)

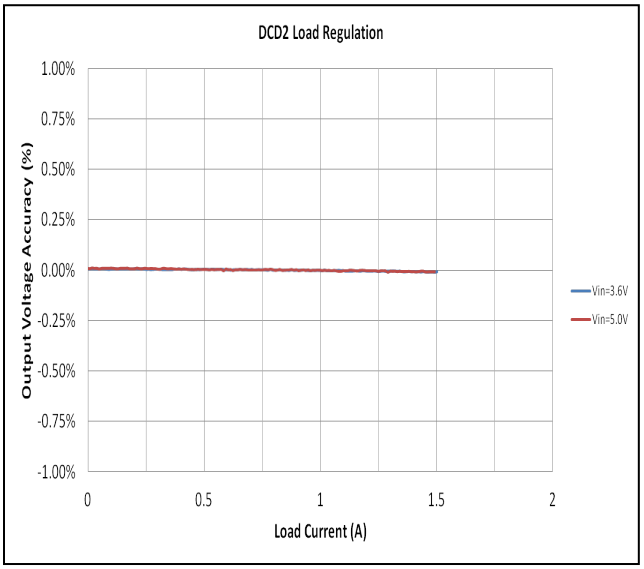


Figure 12. Load Regulation

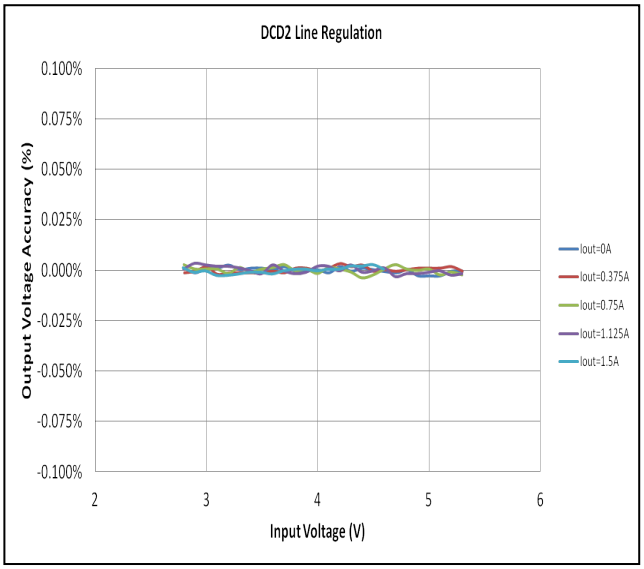


Figure 13. Line Regulation

TYPICAL PERFORMANCE CHARACTERISTICS – DCD3

$C_{O(DCD3)}$ = 22µF, L = 2.2µH, $V_{O(DCD3)}$ = 1.35V, V_{PVIN3} = 5V, T_A = 25°C

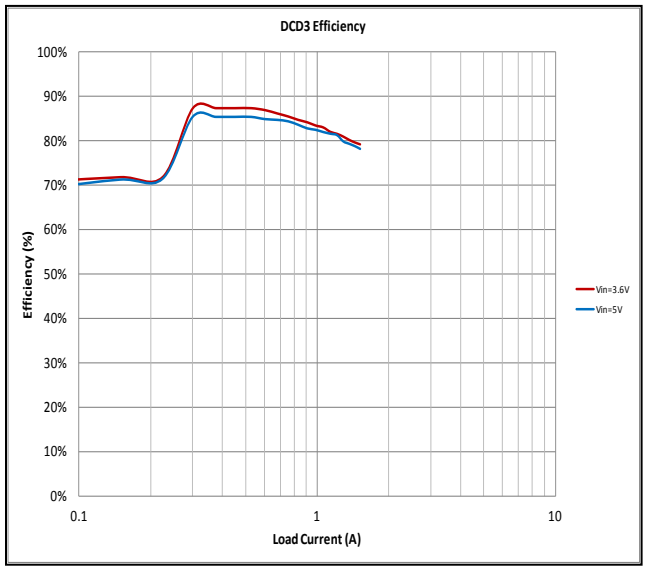


Figure 14. Efficiency

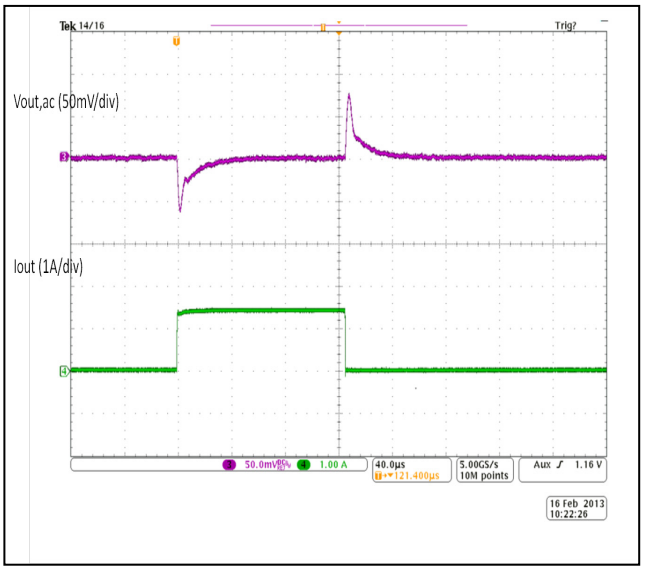


Figure 15. Transient Response (100mA – 1.5A)

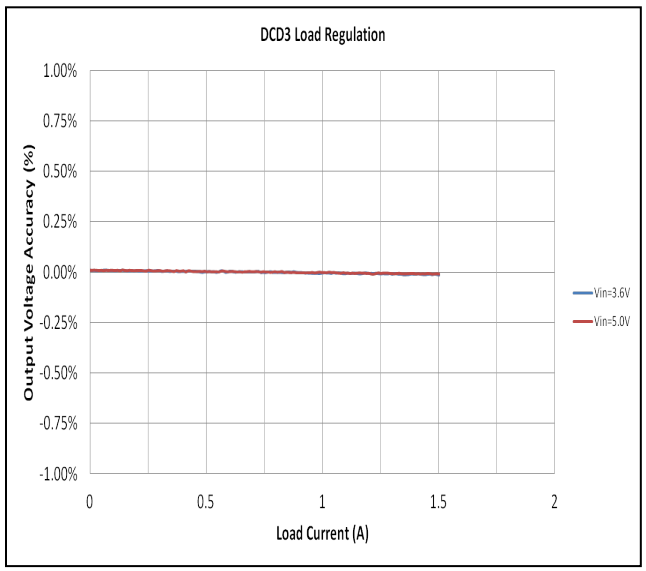


Figure 16. Load Regulation

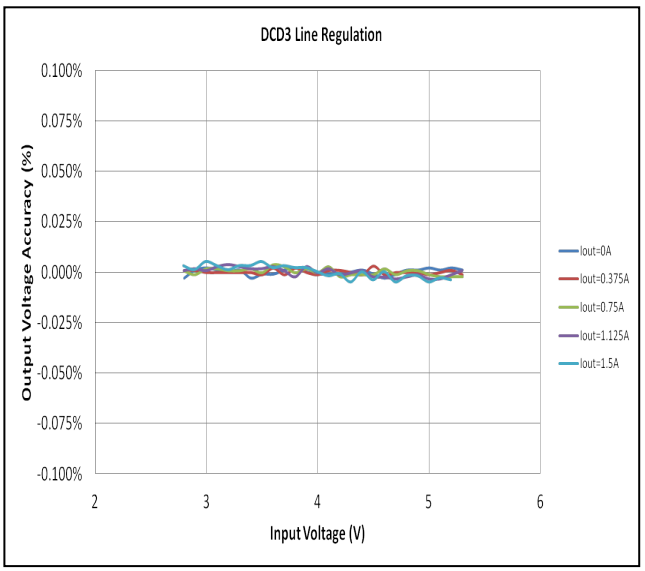


Figure 17. Line Regulation

OVERVIEW OF POWER SUPPLIES

Table 20– Power Supply, Inductance, and Output Capacitance Summary

NAME	I_{OUT} [A] Cont/Pulse	OUTPUT	$V_{O(MIN)}$ [V]	$V_{O(MAX)}$ [V]	V_{STEPS} [mV]	PFM	DVS	C/L
DCD0[4]	8.0/10.0	Programmable	0.76	1.55	12.5	no	yes	150µF/2x0.47µH
DCD0a[5]	4.0/5.0	Programmable	0.76	1.55	12.5	no	yes	68µF/0.47µH
DCD0b[5]						yes	no	68µF/0.47µH
DCD1	4.0/5.0	Programmable	0.76	1.55	12.5	yes	yes	68µF/0.47µH
DCD2	1.5/2.1	Programmable	0.76	3.3	12.5	yes	no	22µF/2.2µH
DCD3	1.5/2.1	Programmable	0.76	3.3	12.5	yes	no	22µF/2.2µH
LDOTR	0.16/0.28	Programmable/ Tracking DCD0 or DCD1	0.6	1.5	12.5	-	yes	2.2µF
LDO0	0.2/0.26	Programmable	1.0	3.35	50	-	-	1µF
LDO1	0.2/0.26	Programmable	1.0	3.35	50	-	-	1µF
LDO2	0.2/0.26	Programmable	1.0	3.35	50	-	-	1µF
LDO3	0.16/0.2	Programmable	1.0	1.475	25	-	-	2.2µF
LDO4	0.16/0.2	Programmable	1.0	1.475	25	-	-	2.2µF
LDO5	0.2/0.26	Programmable	1.0	3.35	50	-	-	1µF
LDO6	0.2/0.26	Programmable	1.0	3.35	50	-	-	1µF
LDO7	0.2/0.26	Programmable	1.0	3.35	50	-	-	1µF
LDO8	0.2/0.26	Programmable	1.0	3.35	50	-	-	1µF
LDO9	0.2/0.26	Programmable	1.0	3.35	50	-	-	1µF

PIN CONFIGURATION AND DESCRIPTION

Trim option 1: DCD0 is a 10A Buck with DVS capability. There is no ability to control external power ICs.

Trim option 2: The same as option 1 with the exception that GPIO6 becomes DIO and GPIO7 becomes DIF. These are the data (DIO) and clock (DIF) serial communication lines which enable IDTP9165 to control external IDTP9167 type power ICs.

Trim option 3: The same as option 2 except that DCD0 is split into two 5A Bucks – DCD0a and DCD0b. Only DCD0a is capable of DVS control (as well as the usual I²C interface). DCD0b is controlled only through the I²C interface.

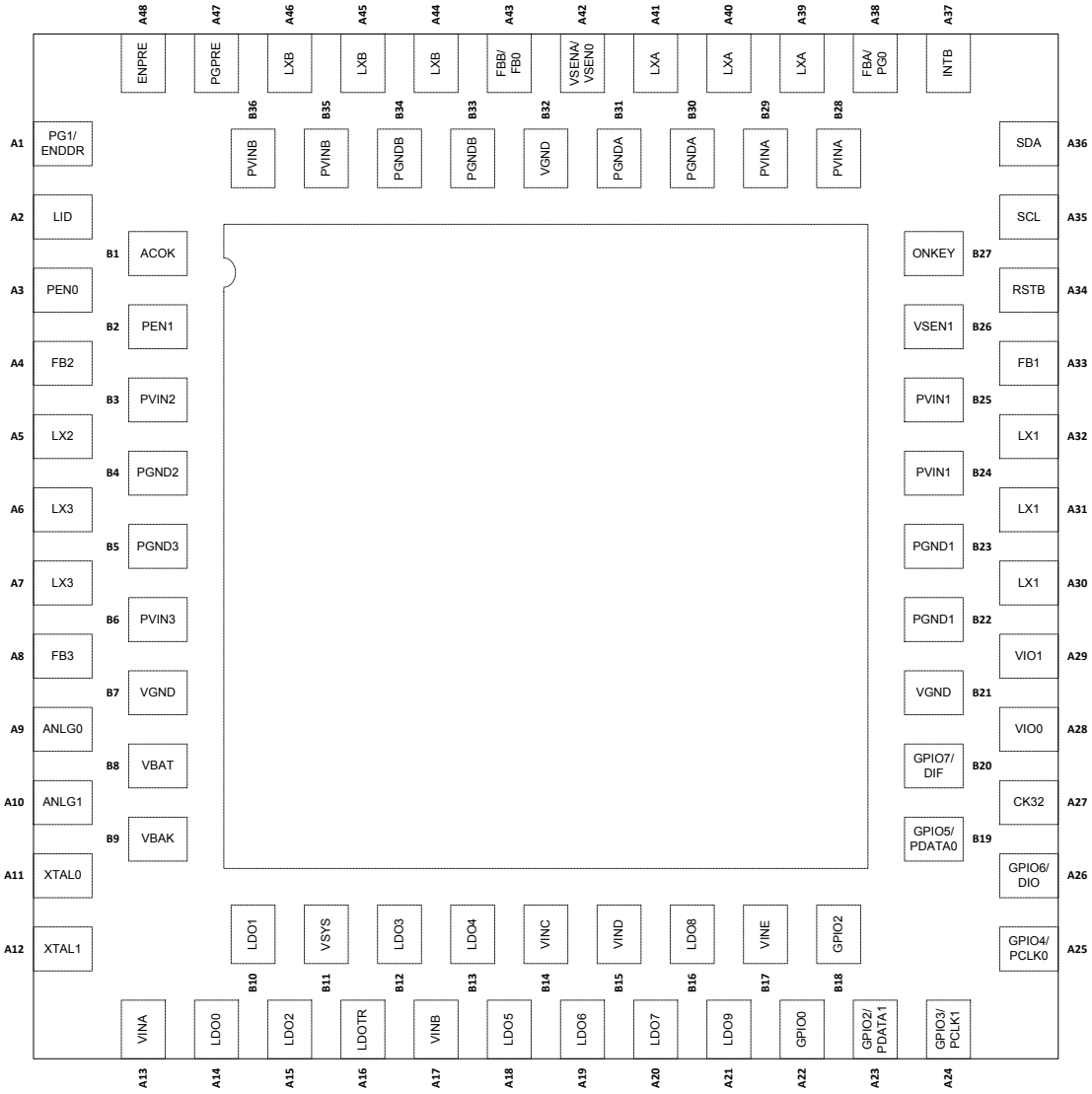


Figure 18 – IDTP9165 Pinout (all possible pin functions shown)

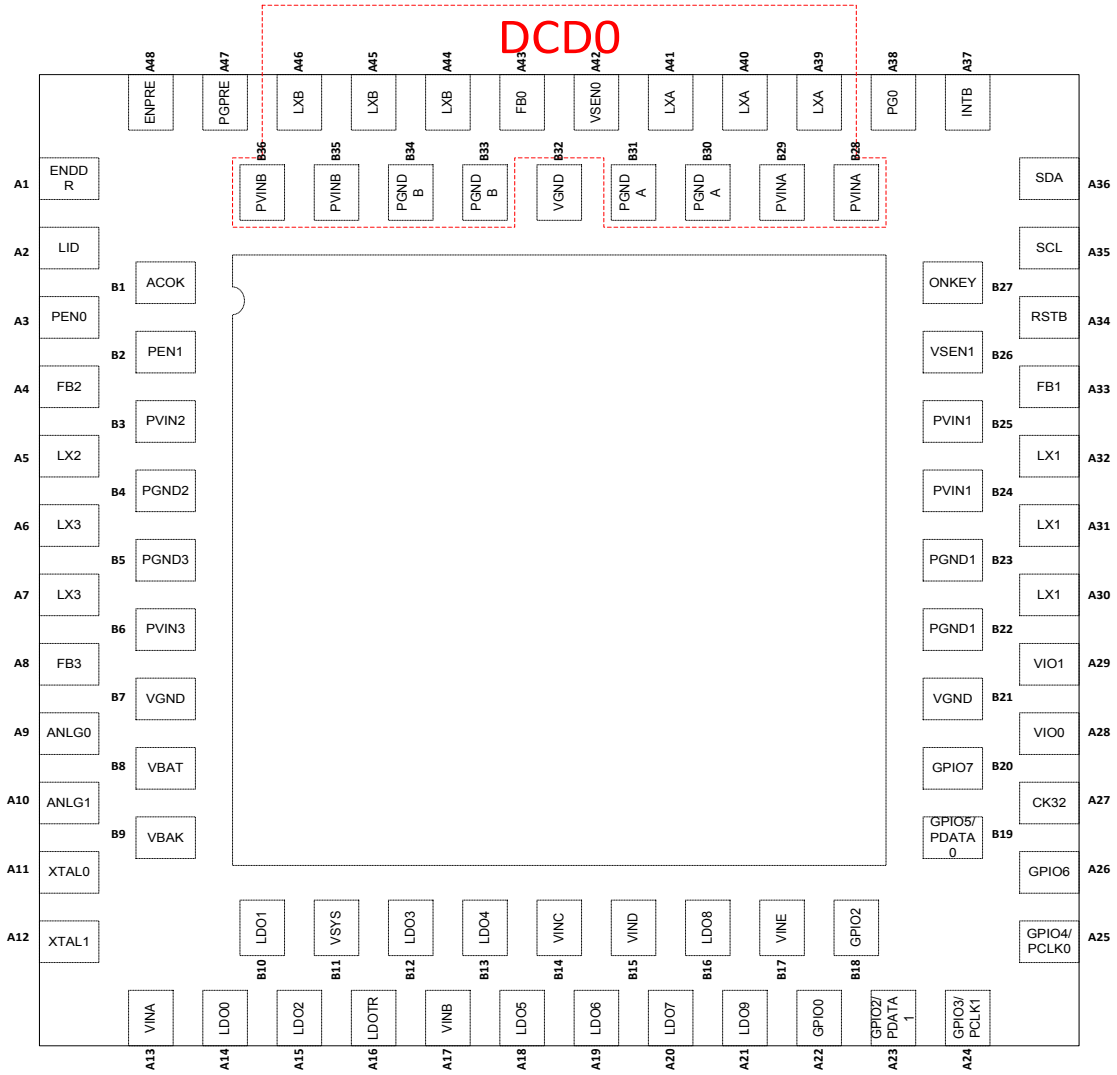


Figure 19 – IDTP9165 Pinout, Trim Option 1 (top view)

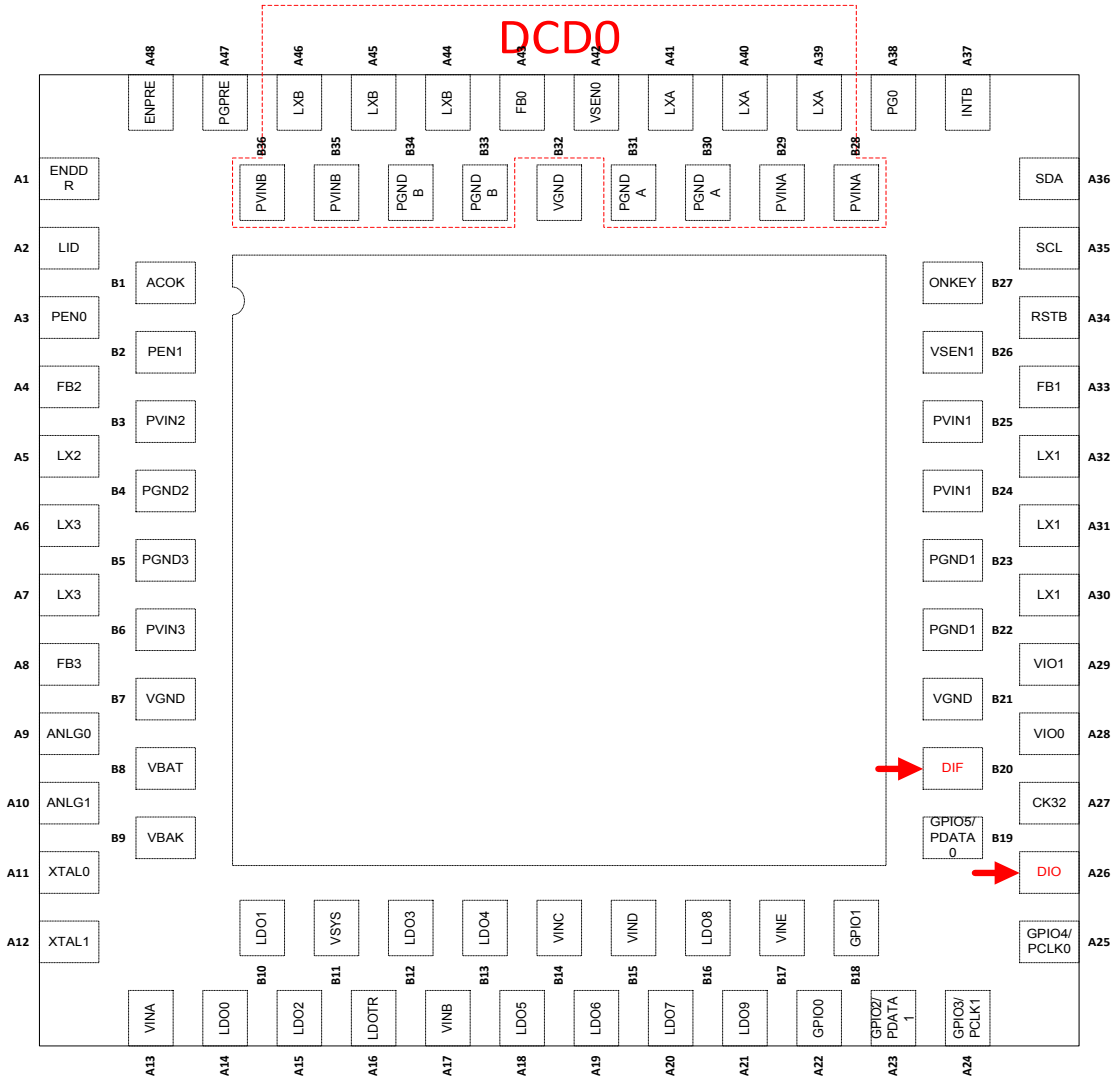


Figure 20 – IDTP9165 Pinout, Trim Option 2 (top view)

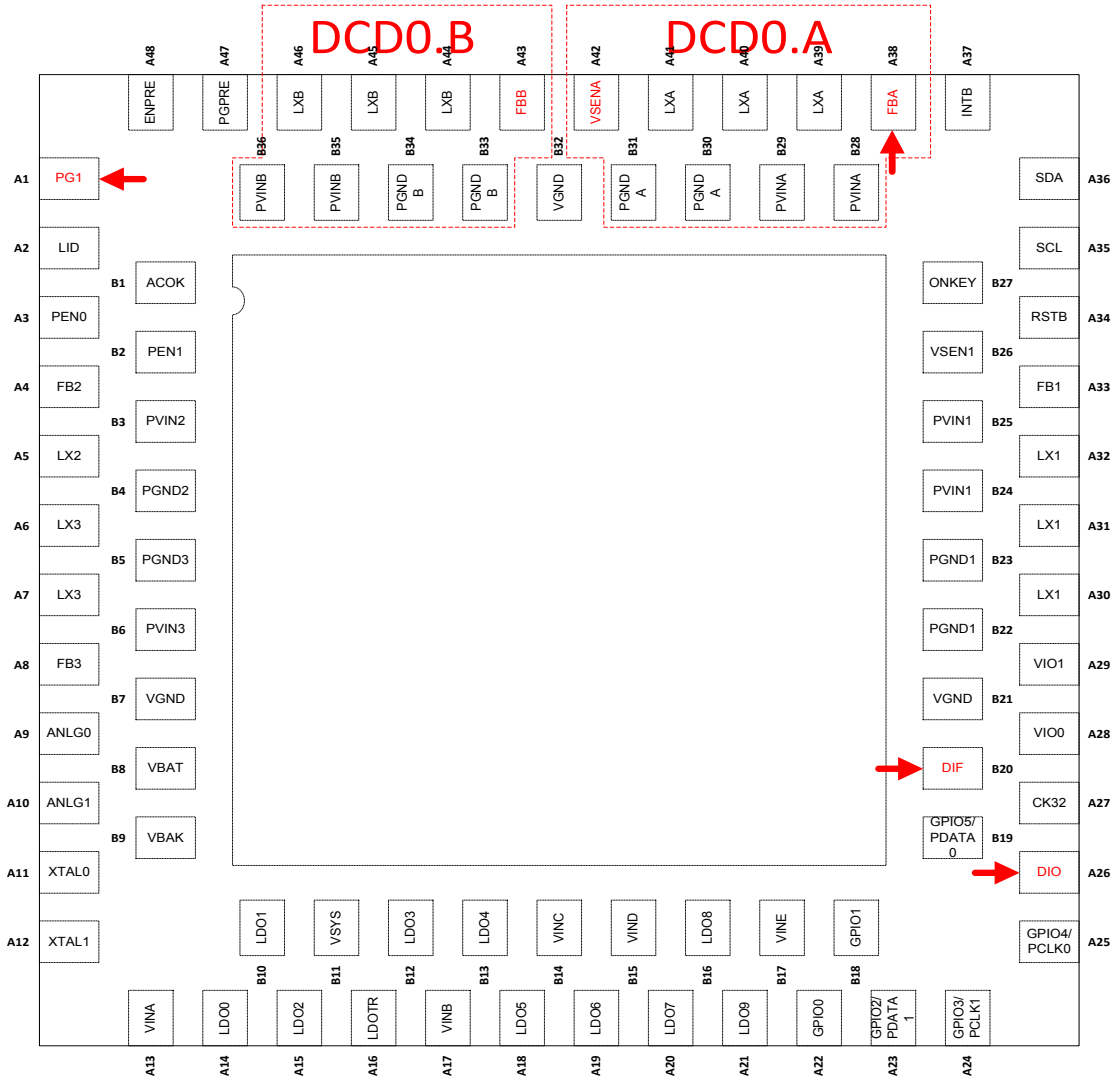


Figure 21 – IDTP9165 Pinout, Trim Option 3 (top view)

DETAILED PIN CONFIGURATION

Table 21 – NQG84 Pin Functions by Pin Number

NUMBER	LABEL	TYPE	DESCRIPTION
A1	ENDDR/ PG1	DO	Enable pin to external power supply/Power Good Pin when DCD0 is split into DCD0a,DCD0b. (The original power good pin – PG0 - becomes DCD0a feedback)
A2	LID	DI	Open/closed LID indication
A3	PEN0	DI	Power Enable control input 0
A4	FB2	A	DCD2 regulator feedback connection
A5	LX2	A	Inductor connection to the DCD2 converter
A6	LX3	A	Inductor connection to the DCD3 converter
A7	LX3	A	Inductor connection to the DCD3 converter
A8	FB3	A	DCD3 regulator feedback connection
A9	ANLG0	A	ADC input 1
A10	ANLG1	A	ADC input 2/ Thermal event input (thermal shutdown from application processor)
A11	XTAL0	A	Oscillator connection 1
A12	XTAL1	A	Oscillator connection 2
A13	VINA	A	LDO1, 2 input
A14	LDO0	A	LDO0 output
A15	LDO2	A	LDO2 output
A16	LDOTR	A	LDOTR output
A17	VINB	A	LDO3, 4 input
A18	LDO5	A	LDO5 output
A19	LDO6	A	LDO6 output
A20	LDO7	A	LDO7 output
A21	LDO9	A	LDO9 output
A22	GPIO0	DIO	General purpose I/O 0 pin
A23	GPIO2/PDATA1	DIO	General purpose I/O 2 pin / DCD1 DVS data
A24	GPIO3/PCLK1	DIO	General purpose I/O 3 pin / DCD1 DVS clock
A25	GPIO4/PCLK0	DIO	General purpose I/O 4 pin / DCD0 or DCD0a DVS clock
A26	GPIO6/DIO	DIO	General purpose I/O 6 pin / Serial Clock communication with External DC/DC Regulator (DIO/DIF is a 1.8V max communication protocol)
A27	CK32	DIO	32.768kHz digital clock output. Only available in ACTIVE state and when VIOx is on.
A28	VIO0	A	*GPIO supply voltage input 0* *Note: The IDTP9167 external DC/DC regulator I/O communication is a 1.8V interface only. VIO0 Supplies this I/O as well as the I²C. It must be set to 1.8V to operate the IDTP9167.If not using the IDTP9167 the voltage can be increased to operate the I²C at higher voltages but the I²C speed maximum communication speed will be decreased.*
A29	VIO1	A	GPIO supply voltage input 1 Individual GPIO supplies can be programmed to VIO0 or VIO1 throiugh registers

NUMBER	LABEL	TYPE	DESCRIPTION
			GPIOxC GPIO Configuration and Status
A30	LX1	A	Inductor connection to the DCD1 converter
A31	LX1	A	Inductor connection to the DCD1 converter
A32	LX1	A	Inductor connection to the DCD1 converter
A33	FB1	A	DCD1 regulator feedback connection
A34	RSTB	DO	Active-low reset output to host controller, biased from VIO1
A35	SCL	DI	I²C bus clock input – Chip address: 0x4F
A36	SDA	DIO	I²C bus data IO– Chip address: 0x4F
A37	INTB	DO	Active-low interrupt request to host
A38	FBA/PG0	A/DO	DCD0a regulator feedback connection / DCD0 power-good and over-current signal
A39	LXA	A	Inductor connection to the DCD0 converter, phase A
A40	LXA	A	Inductor connection to the DCD0 converter, phase A
A41	LXA	A	Inductor connection to the DCD0 converter, phase A
A42	VSENA/VSEN0	A	DCD0a / DCD0 ground remote sense
A43	FBB/FB0	A	DCD0b / DCD0 regulator feedback connection
A44	LXB	A	Inductor connection to the DCD0 converter, phase B
A45	LXB	A	Inductor connection to the DCD0 converter, phase B
A46	LXB	A	Inductor connection to the DCD0 converter, phase B
A47	PGPRE	DI	Power-good signal from pre-regulator
A48	ENPRE	DO	Enable pin for VSYS pre-regulator, connect to EN pin of VSYS pre-regulator
B1	ACOK	DI	AC plugged-in indication
B2	PEN1	DI	Power Enable control input 1
B3	PVIN2	A	DCD2 supply input
B4	PGND2	A	DCD2 power ground
B5	PGND3	A	DCD3 power ground
B6	PVIN3	A	DCD3 supply input
B7	VGND	A	GND connection
B8	VBAT	A	PMIC supply input
B9	VBAK	A	PMIC Coin cell/SuperCap connection
B10	LDO1	A	LDO1 output
B11	VSYS	A	LDO0, LDOTR input, and Bias input for fuse and DCD blocks
B12	LDO3	A	LDO3 output
B13	LDO4	A	LDO4 output
B14	VINC	A	LDO5 input

NUMBER	LABEL	TYPE	DESCRIPTION
B15	VIND	A	LDO6, 7 input
B16	LDO8	A	LDO8 output
B17	VINE	A	LDO8, 9 input
B18	GPIO1	DIO	General purpose I/O 2 pin
B19	GPIO5/PDATA0	DIO	General purpose I/O 5 pin / DCD0 or DCD0a DVS data
B20	GPIO7/DIF	DIO	General purpose I/O 7 pin / Serial Clock communication with External DC/DC Regulator (DIO/DIF is a 1.8V max communication protocol)
B21	VGND	A	GND connection
B22	PGND1	A	DCD1 power ground
B23	PGND1	A	DCD1 power ground
B24	PVIN1	A	DCD1 supply input
B25	PVIN1	A	DCD1 supply input
B26	VSEN1	A	DCD1 ground remote sense
B27	ONKEY	DI	ONKEY input
B28	PVINA	A	DCD0 supply input, phase A
B29	PVINA	A	DCD0 supply input, phase A
B30	PGNDA	A	DCD0 power ground, phase A
B31	PGNDA	A	DCD0 power ground, phase A
B32	VGND	A	Ground connection
B33	PGNDB	A	DCD0 power ground, phase B
B34	PGNDB	A	DCD0 power ground, phase B
B35	PVINB	A	DCD0 supply input, phase B
B36	PVINB	A	DCD0 supply input, phase B
EP	EPAD	A	Exposed pad. Must be electrically connected to ground

PRODUCT OVERVIEW

The IDTP9165 is an integrated device that combines power management, backup battery/SuperCap charging, pre-regulator control, system monitoring, a Real Time Clock (RTC) and external regulator enable control. All of these subsystems are configured, monitored and controlled by on-chip programmable registers over an I²C interface. It includes 4 integrated, synchronous, step-down DC/DC regulators (5 regulators when using Device Option 3, which splits the dual phase DCD0 into two separate single phase switching regulators), 11 LDOs, a 10-bit ADC, 8 GPIOs, and a high speed I²C interface. The IDTP9165 also contains all the necessary interface connections required by state-of-the-art quad-core application processor.

There are three device options available: Option 1, 2, 3:
Device option 1: DCD0 is a 10A Buck with DVS capability. There is no ability to control external power ICs.

Device option 2: The same as option 1 with the exception that GPIO6 becomes DIO and GPIO7 becomes DIF. These are the data (DIO) and clock (DIF) serial communication lines which enable IDTP9165 to control external IDTP9167 type power ICs.

Device option 3: The same as option 2 except that DCD0 is split into two 5A Bucks – DCD0a and DCD0b. Only DCD0a is capable of DVS control. DCD0b is controlled only through the I²C interface. (DCD0a can also be controlled through the usual I²C interface)

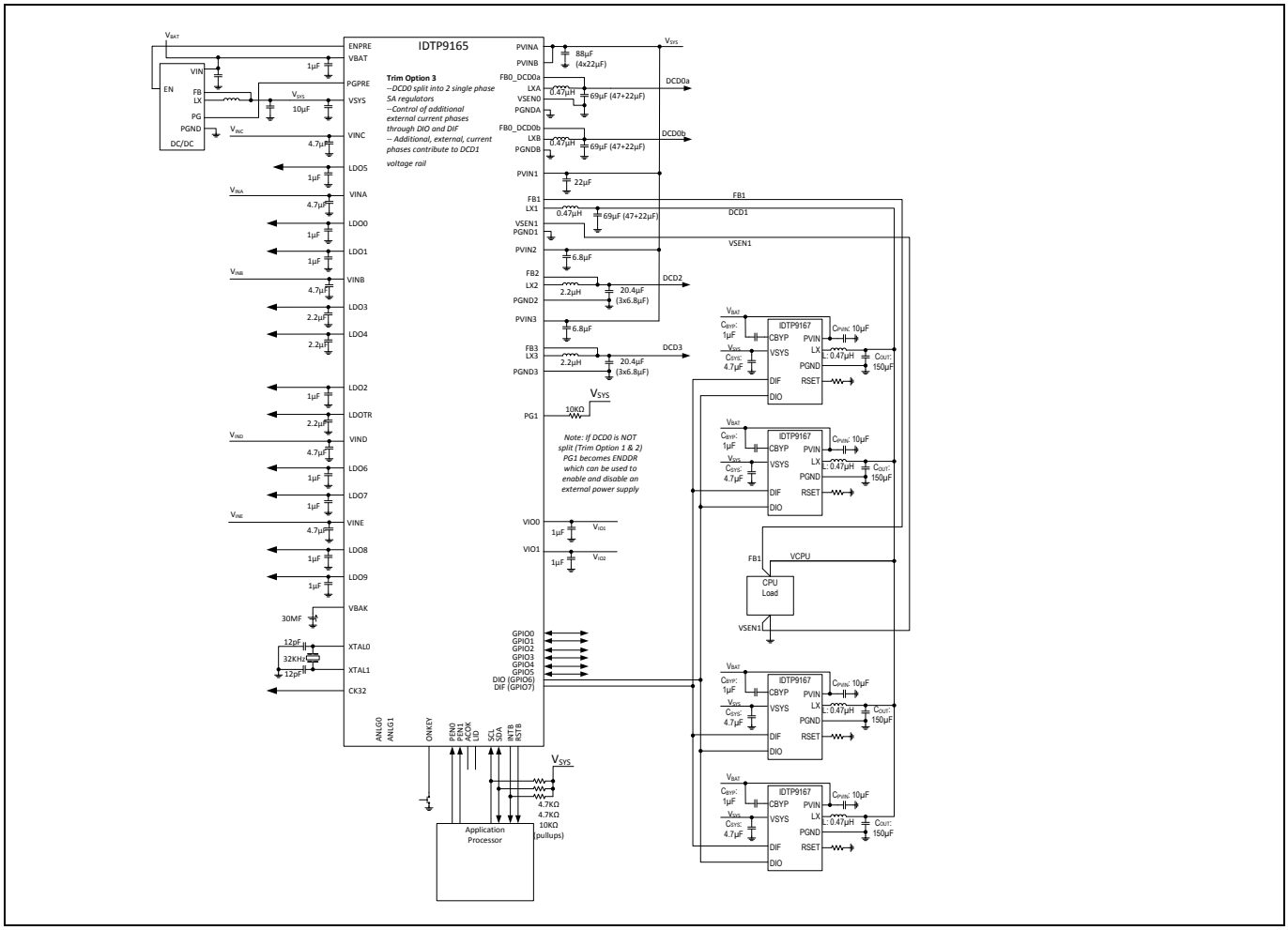


Figure 22. External Component Connections

Dual-Phase Step-Down Regulator DCD0 (Trim option 1, 2)

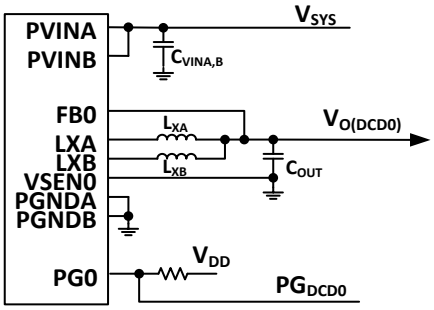


Figure 23. DCD0 External component connections

Table 22– DCD0 Module Pin Definitions

PIN #	Label	Type	DESCRIPTION
A39 A40 A41	LXA	A	Inductor connection to the DCD0 converter, phase A
A44 A45 A46	LXB	A	Inductor connection to the DCD0 converter, phase B
B28 B29	PVINA	A	DCD0 supply input, phase A
B30 B31	PGNDA	A	DCD0 power ground, phase A
B33 B34	PGNDB	A	DCD0 power ground, phase B
B35 B36	PVINB	A	DCD0 supply input, phase B
A42	VSEN0	A	DCD0 ground remote sense
A43	FB0	A	DCD0 regulator feedback connection
A38	PG0	DO	DCD0 power-good and over-current signal

Dual-Phase Step-Down Regulator DCD0a (Trim option 3)

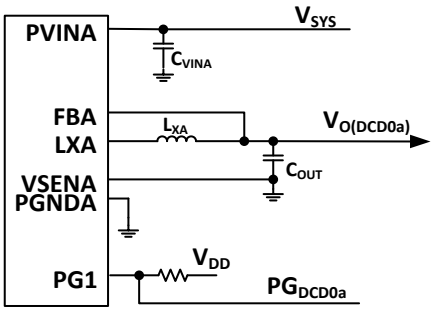


Figure 24. DCD0a External component connections

Table 23– DCD0a Module Pin Definitions

PIN #	Label	Type	DESCRIPTION
A39	LXA	A	Inductor connection to the DCD0 converter, phase A
A40			
A41			
B28	PVINA	A	DCD0 supply input, phase A
B29			
B30	PGNDA	A	DCD0 power ground, phase A
B31			
A42	VSENA	A	DCD0 ground remote sense
A38	FBA	A	DCD0 regulator feedback connection
A1	PG1	DO	DCD0a power-good and over-current signal

Dual-Phase Step-Down Regulator DCD0b (Trim option 3)

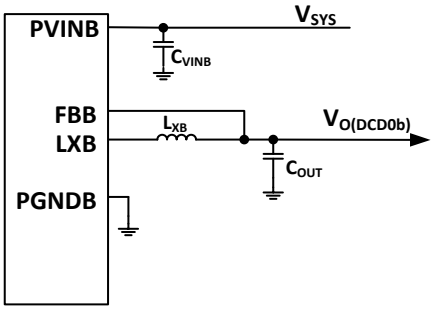


Figure 25. DCD0b External component connections

Table 24– DCD0b Module Pin Definitions

PIN #	Label	Type	DESCRIPTION
A44	LXB	A	Inductor connection to the DCD0 converter, phase B
A45			
A46			
B33	PGNDB	A	DCD0 power ground, phase B
B34			
B35	PVINB	A	DCD0 supply input, phase B
B36			
A43	FBB	A	DCD0 regulator feedback connection

Step-Down Regulator DCD1

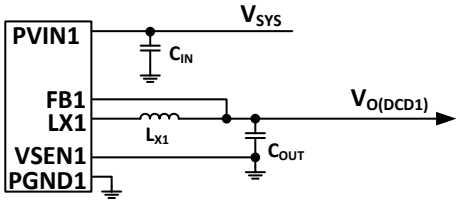


Figure 26. DCD1 External component connections

Table 25– DCD1 Module Pin Definitions

PIN #	Label	Type	DESCRIPTION
A30 A31 A32	LX1	A	Inductor connection to the DCD1 converter
B22 B23	PGND1	A	DCD1 supply input
B24 B25	PVIN1	A	DCD1 power ground
B26	VSEN1	A	DCD1 ground remote sense
A33	FB1	A	DCD1 regulator feedback connection

Step-Down Regulator DCD2

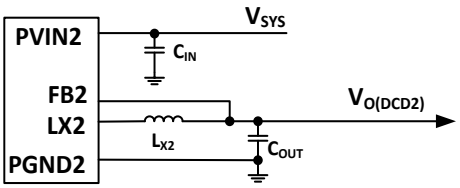


Figure 27. DCD2 External component connections

Table 26– DCD2 Module Pin Definitions

PIN #	Label	Type	DESCRIPTION
A5	LX2	A	Inductor connection to the DCD2 converter
B3	PVIN2	A	DCD2 supply input
B4	PGND2	A	DCD2 power ground
A4	FB2	A	DCD2 regulator feedback connection

Step-Down Regulator DCD3

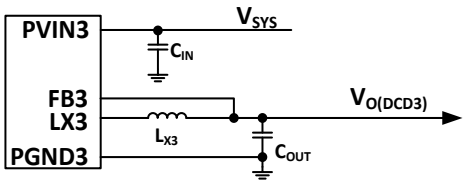


Figure 28. DCD3 External component connections

Table 27– DCD3 Module Pin Definitions

PIN #	Label	Type	DESCRIPTION
A6 A7	LX3	A	Inductor connection to the DCD3 converter
B5	PGND3	A	DCD3 power ground
B6	PVIN3	A	DCD3 supply input
A8	FB3	A	DCD3 regulator feedback connection

LDO Regulators – Electrical Characteristics

LDO0, 1, 2, 5

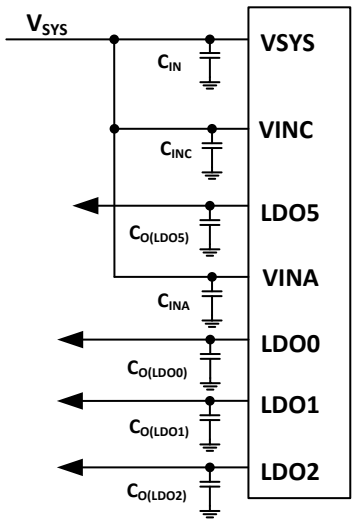


Figure 29. LDO0,1,2,5 External component connections

Table 28– LDO0, 1, 2, 5 Module Pin Definitions

PIN #	Label	Type	DESCRIPTION
B11	VSYS	A	LDO0 input
A13	VINA	A	LDO1, 2 input
B14	VINC	A	LDO5 input
A14	LDO0	A	LDO0 output
B10	LDO1	A	LDO1 output
A15	LDO2	A	LDO2 output
A18	LDO5	A	LDO5 output

LDOTR Tracking LDO

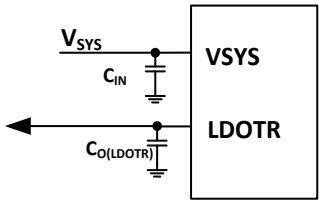


Figure 30. LDOTR External component connections

Table 29– Tracking LDO Module Pin Definitions

PIN #	Label	Type	DESCRIPTION
B11	VSYS	A	LDOTR input
A16	LDOTR	A	LDOTR output

LDO3, 4

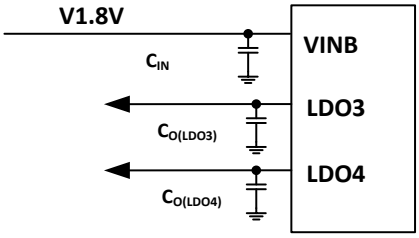


Figure 31. LDO3,4 External component connections

Table 30– LDO3, 4 Module Pin Definitions

PIN #	Label	Type	DESCRIPTION
A17	VINB	A	LDO3, 4 input
B12	LDO3	A	LDO3 output
B13	LDO4	A	LDO4 output

LDO6, 7, 8, 9

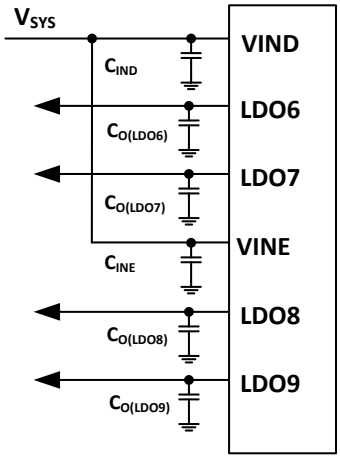


Figure 32. LDO6,7,8,9 External component connections

Table 31– LDO6, 7, 8, 9 Module Pin Definitions

PIN #	Label	Type	DESCRIPTION
B15	VIND	A	LDO6, 7 input
B17	VINE	A	LDO8, 9 input
A19	LDO6	A	LDO6 output
A20	LDO7	A	LDO7 output
B16	LDO8	A	LDO8 output
A21	LDO9	A	LDO9 output

RTC LDO, Coin Cell/SuperCap Charger

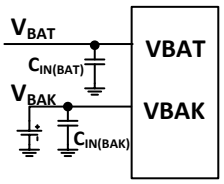


Figure 33. RTC LDO and Coin Cell Charger external component connections

Table 32– Charger Module Pin Definitions

PIN #	Label	Type	DESCRIPTION
B8	VBAT	A	PMIC supply input
B9	VBAK	A	PMIC Coin cell/SuperCap connection/3Cell Lithium

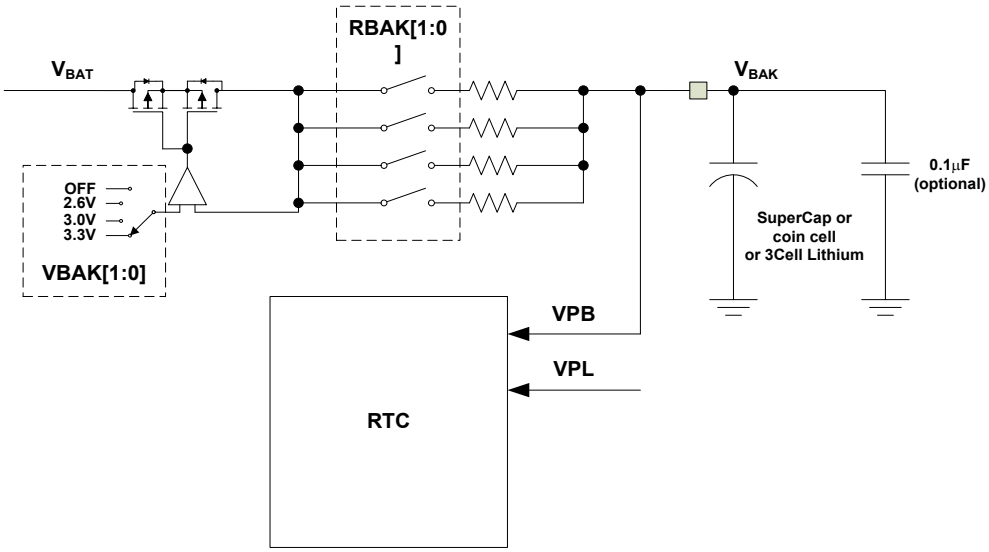


Figure 34. RTC LDO and Coin Cell Charger internal connections

GPIO Interface

Table 33– GPIO Module Pin Definitions

Number	Label	Type	Description
A22	GPIO0	DIO	General purpose I/O 0 pin
A23	GPIO2/PDATA1	DIO	General purpose I/O 2 pin / DCD1 DVS data
A24	GPIO3/PCLK1	DIO	General purpose I/O 3 pin / DCD1 DVS clock
A25	GPIO4/PCLK0	DIO	General purpose I/O 4 pin / DCD0 or DCD0a DVS clock
A26	GPIO6/DIO	DIO	General purpose I/O 6 pin / Serial Clock communication with External DC/DC Regulator
B18	GPIO1	DIO	General purpose I/O 2 pin
B19	GPIO5/PDATA0	DIO	General purpose I/O 5 pin / / DCD0 or DCD0a DVS data
B20	GPIO7/DIF	DIO	General purpose I/O 7 pin / Serial Clock communication with External DC/DC Regulator

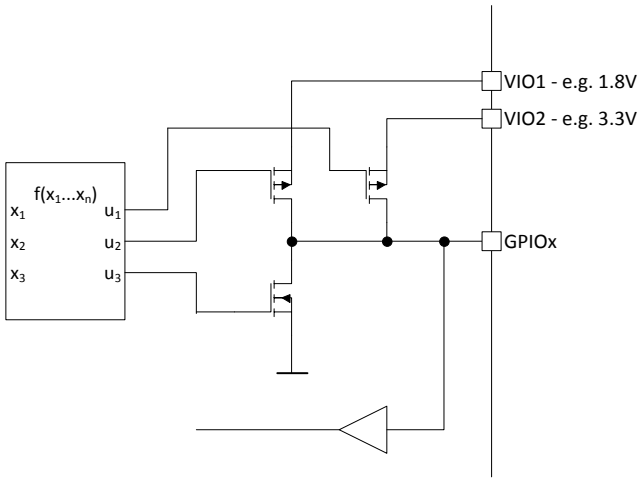


Figure 35. GPIO interface internal connections

IMPORTANT:

The IDTP9167 external DC/DC regulator I/O communication is a 1.8V interface only. VIO0 Supplies this I/O as well as the I²C. It must be set to 1.8V to operate the IDTP9157.If not using the IDTP9157 the voltage can be increased to operate the I²C at higher voltages but the I²C speed maximum communication speed will be decreased.

ADC

Table 34– ADC Module Pin Definitions

PIN #	Label	Type	DESCRIPTION
A9	ANLG0	A	ADC input 0
A10	ANLG1	A	ADC input 1

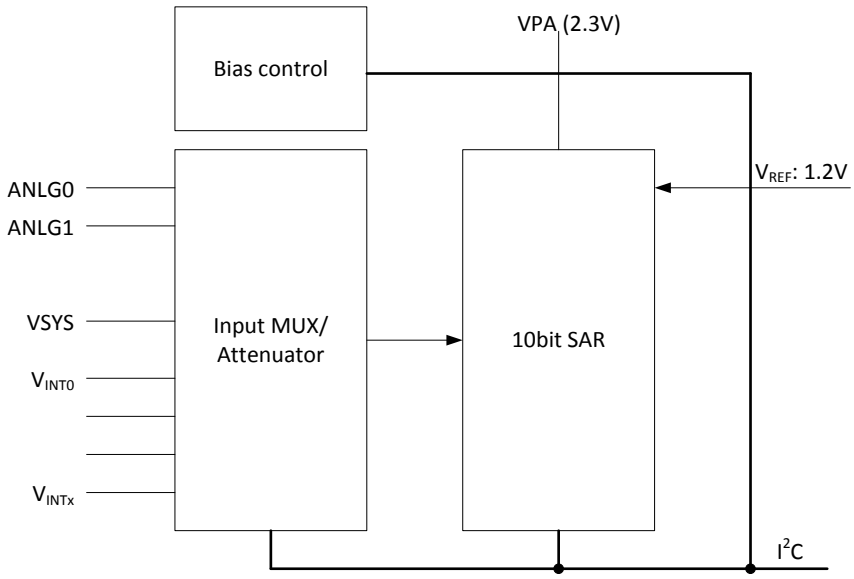


Figure 36. ADC internal connections

RTC

Table 35– RTC Module Pin Definitions

PIN #	Label	Type	DESCRIPTION
A11	XTAL0	A	Oscillator connection 0
A12	XTAL1	A	Oscillator connection 1
A27	CK32	DO	32.768kHz digital clock output. Only available in ACTIVE state and when VIOx is on.

I²C

Description

The IDTP9165 is a slave device only. It is designed to operate with wide frequency range of 400KHz – 3.4MHz. The PMIC is accessed using a 7-bit addressing scheme. The PMIC I²C slave is not allowed to stretch the clock, and must be capable of being multi-mastered in a debug environment. The I²C bus is only used for non-latency critical register accesses and communication between the SoC and PMIC.

The PMIC supports the standard I²C read and write functions. The configuration register space is covered into one 256-byte partitions. The PMIC supports four 7-bit device addresses are configurable through One Time Programming (OTP) at the factory. The address can be configured as 0x4F (1001111), 0x60 (1100000), 0x74 (1110100), and 0x77 (1110111) to allow for cases where multiple IDTP9165s are used on the same board or other I2C address conflicts arise.

The default address is 0x4F.

Note that in 8-bit format, these addresses correspond to 0x9E, 0xC0, 0xE8, and 0xEE for writes, and 0x9F, 0xC1, 0xE9, and 0xEF for reads.

	7-bit	8-bit (Write)	8-bit (Read)
Device 1 (default address)	0x4F	0x9E	0x9F
Device 2	0x60	0xC0	0xC1
Device 3	0x74	0xE8	0xE9
Device 4	0x77	0xEE	0xEF

Table 36: I²C Addresses

Reading data back from PMIC registers follow the "combined protocol" as described in the I²C specification, in which the first byte written is the register offset to be read, and the first byte read (after a repeat START condition) is the data from that register offset. See the figures below for details.

The following diagrams captures the different high-speed and fast-speed transaction format/protocol.

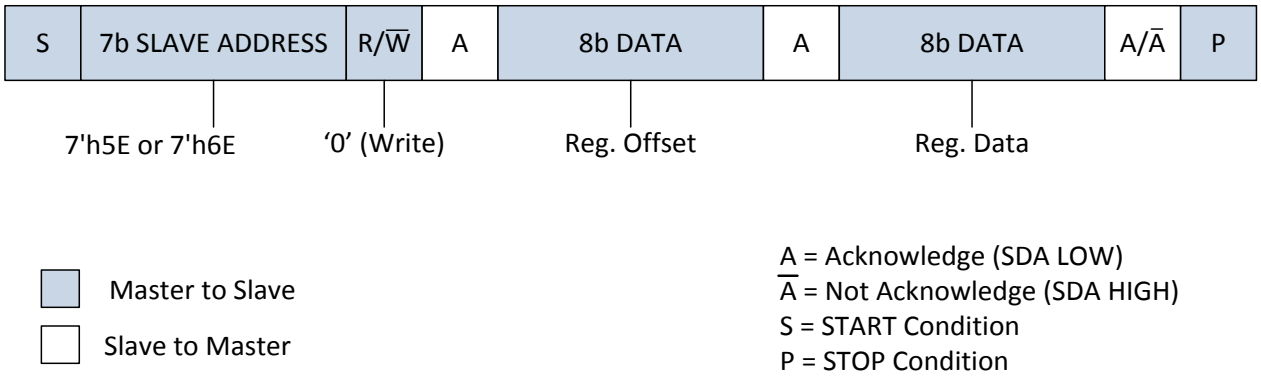


Figure* 37: *I²C Fast Speed Write

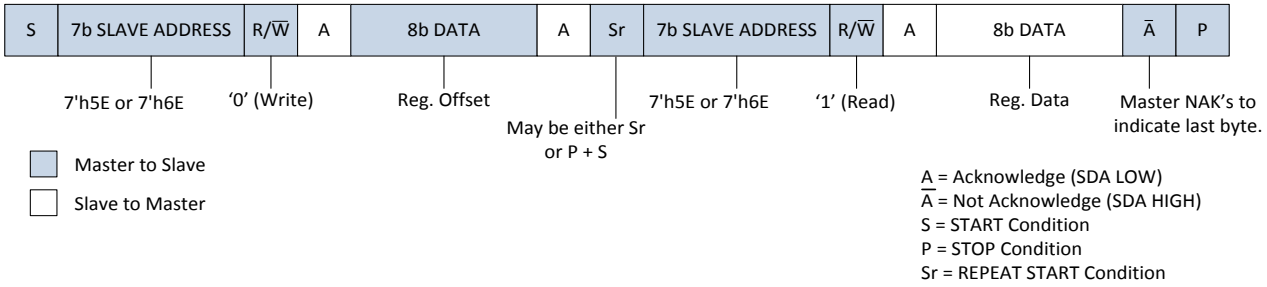


Figure 38: I²C Fast Speed Read

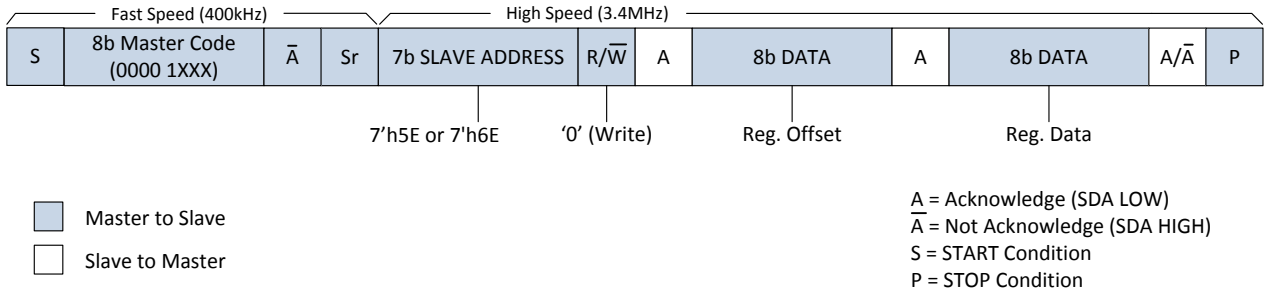


Figure 39: I²C High Speed Write

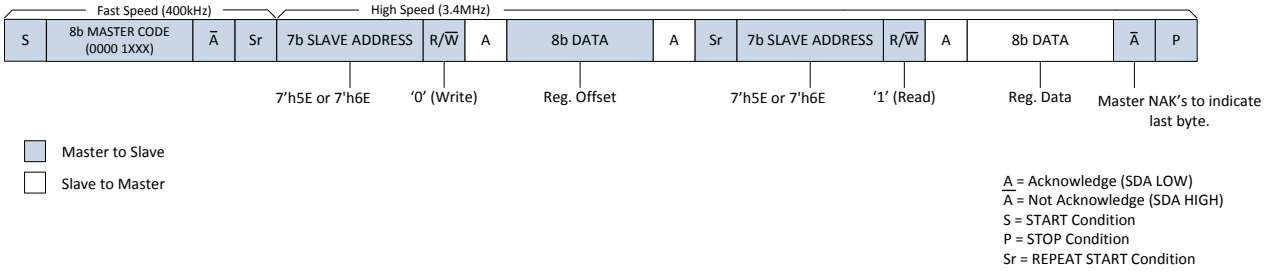


Figure 40: I²C High Speed Read

Sequential offset accesses within a single transaction ("burst" reads and writes) are supported by IDTP9165's I²C module.

The IDTP9165's I²C port conforms to the 3.4 MHz High-speed mode (Hs-mode) I²C bus protocol and supports 7-bit device/page addressing.

The IDTP9165's I²C port follows I²C bus protocol during register reads or writes that are initiated by an external I²C Master (typically the application processor).

I²C Pin Definitions

Table 37– I²C Pin Definitions

PIN #	PIN_ID	TYPE	DESCRIPTION
A35	SCL	DI	I²C bus clock input
A36	SDA	DIO	I²C bus data IO
IDTP9165 I²C Default Address : 0x4F (Optional: 60h, 74h or 77h programmable via OTP)			

I²C Register Map

A yellow field in the table indicates that the bit can be programmed by fuse. After power-on, the bit is set to its pre-programmed value, but it can be changed anytime by an I²C write command.

Byte Ordering and Offset

All registers are defined within one byte width and occupy one byte in the address space. Please refer to the individual register descriptions for information on how that register is stored in address space.

Reserved Bit Fields

Bit fields and Bytes labeled *RESERVED* are reserved for future use. When writing to a register containing some *RESERVED* bits, the user should do a "read-modify-write" such that only the bits, which are intended to be written, are modified.

NOTE: DO NOT WRITE to registers containing all *RESERVED* bits.

Register Access Types

Table 38. Register Access Type Description

TYPE	DESCRIPTION
RW	Readable and Writeable
R	Read only
RW1C	Readable and Write 1 to this bit to clear it (for interrupt status)
RW1A	Readable and Write 1 to this bit to take actions

Regulator Enable

Table 39– Regulator Enable registers

Address Hex/Dec		Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	R/W
1	1	**REG_ON0**	-	-	-	-	DCD3_ON	DCD2_ON	DCD1_ON	DCD0_ON	R/W
		Default	-	-	-	-	0	0	0	0	
2	2	**REG_ON1**	-	-	-	LDOTR_ON	LDO3_ON	LDO2_ON	LDO1_ON	LDO0_ON	R/W
		Default	-	-	-	0	0	0	0	0	
3	3	**REG_ON2**	-	-	LDO9_ON	LDO8_ON	LDO7_ON	LDO6_ON	LDO5_ON	LDO4_ON	R/W
		Default	-	-	0	0	0	0	0	0	
4	4	**REG_ON3**	-	-	-	-	-	-	-	ENDDR	R/W
		Default	-	-	-	-	-	-	-	0	

If regulators are not linked to an enable pin (PEN0, PEN1) nor configured within a sequencing scheme, then bits in REGON0 to REGON3 can be set to turn on/off the regulators. If a regulator is configured by OTP to be part of a power sequence or is pin controlled, the appropriate bit in the register is automatically set to “1” at start-up from OFF state. The user can however disable the regulator at any time by writing a “0” to the enable bit.

It is good practice to read the entire register and modify only the bit that needs to be changed (read-modify-write).

DCD Regulators Configuration

Table 40– DCD Regulators registers

Adress Hex	Adress Dec	Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	R/W
5	5	**DCD0C0**	-	-	DCD0_VOUT[5:0]						R/W
6	6	**DCD0C1**	-	-	DCD0_VDVS[5:0]						R/W
7	7	**DCD0C2**	-	-	-	-	DCD0_SR[1:0]		DCD0_PDVS	DCD0_DVS	R/W
		Default	-	-	-	-	OTP - One Time Prog		0	0	
8	8	**DCD0a**	-	-	DCD0a_VOUT[5:0]						R/W
9	9	**DCD1C0**	-	-	DCD1_VOUT[5:0]						R/W
A	10	**DCD1C1**	-	-	DCD1_VDVS[5:0]						R/W
B	11	**DCD1C2**	-	-	-	-	DCD1_SR[1:0]		DCD1_PDVS	DCD1_DVS	R/W
		Default	-	-	-	-	OTP		0	0	
C	12	**DCD2C**	DCD2_RNG[1:0]		DCD2_VOUT[5:0]						R/W
D	13	**DCD3C**	DCD3_RNG[1:0]		DCD3_VOUT[5:0]						R/W
E	14	**DCD_PEN**	DCD3_PIN	DCD2_PIN	DCD1_PIN	DCD0_PIN	DCD3_PEN	DCD2_PEN	DCD1_PEN	DCD0_PEN	R/W
F	15	**FPWM**	-	-	-	DCD0a_PWM	DCD3_PWM	DCD2_PWM	DCD1_PWM	DCD0_PWM	R/W
		Default	-	-	-	0	0	0	0	0	
10	16	**FPFM**	-	-	-	DCD0a_PFM	DCD3_PFM	DCD2_PFM	DCD1_PFM	DCD0_PFM	R/W
		Default	-	-	-	0	0	0	0	0	
11	17	**DCD_EILIM**	-	-	-	DCD0a_EILIM	DCD3_EILIM	DCD2_EILIM	DCD1_EILIM	DCD0_EILIM	R/W
		Default	-	-	-	0	0	0	0	0	
12	18	**DCD_PG**	-	-	-	DCD0a_PG	DCD3_PG	DCD2_PG	DCD1_PG	DCD0_PG	R
		Default	-	-	-	0	0	0	0	0	
13	19	**DCD_DLY**	-	-	-	-	-	PAR_PHAB	DCD_DLY[1:0]		R/W
		Default	-	-	-	-	-	0	OTP		

Registers 5 to 19 configure and control the 4 switching regulators.

These registers program the regular output voltage (ex. DCD0_VOUT) and the voltage desired during Dynamic Voltage Scaling (ex. DCD0_VDVS). Dynamic Voltage Scaling (DVS) occurs when a different voltage is desired for better performance. At that time the _DVS bits (ex. DCD0_DVS) are set to "1" and the output voltage is changed while the regulator remains on. These registers also control the slew rate of change between the normal output voltage and the DVS voltages through the _SR bits (ex. DCD0_SR). Only DCD0 and DCD1 support dynamic voltage scaling.

A second method of dynamic voltage scaling is available through the use of the DCD0_PDVS (and DCD1_PDVS) bits. PDVS stands for PWM-DVS control. In PDVS control the duty cycle of the PWM signal will add a positive voltage offset to the DCD0_VOUT/DCD1_VOUT command. See "**DCD0/DCD1 PDVS (PWM DVS) Operation**" for more information. This bit is set then the voltage is controlled through a two wire interface (clock and PWM type data). For DCD0, clock and data inputs are GPIO4 and GPIO5 respectively. For DCD1, clock and data inputs are GPIO3 and GPIO2 respectively.

DCD0 and DCD1 support two voltage ranges, a low range from 0.5375V to 1.3250V and a high range from 0.7625V to 1.55V. The default range is set by register bits RANGE_01[5:4] (**Table 57**) to the high range. Important: ALWAYS turn of the regulator before changing ranges.

These registers also control the output voltages of DCD2 and DCD3 (ex. DCD2_VOUT). Four voltage ranges are available depending on the value programmed in the range bits (ex. DCD2_RNG). Using the _RNG and _VOUT bits voltages from 525mV to 3.3375V are possible. As in the case of DCD0 and DCD1, always turn of the regulator before changing ranges..

The power up behavior is programmed through the PIN and PEN bits. PIN are the gate keeper bits, they stand for "Power up Input control". If a PIN bit is set to "1" then the regulator will be turned on by one of the two physical PEN pins that are available to the external world. The PEN bit

determines whether the PMIC reacts to either PEN0 (“0”) or PEN1.The PEN control is available to all four regulators.

Finally, if the PIN bit is not set then power up control defaults to the sequence registers as described later in this document.

All four switching regulators can be forced into constant PFM or PWM mode through the _PWM and _PFM bits (exs. DCD0_PWM, DCD0_PFM). PWM definition: PWM is used for tighter control of the output voltage. Either the high side or the low side power transistor is on at any given time, at no time is the output floating. This allows for very good control of the output voltage and the expense of poor efficiency at light loads. PFM definition: PFM mode is the opposite: good efficiency and more ripple on the output voltage. PFM mode is used for light loads only, typically, when the regulator would be well into the discontinuous conduction mode (DCM) of operation. Due to the light load, the voltage floats up to 20mV above the programmed value. The output stage – both high and low side transistors – then turn off and allow the voltage to decrease to 10mV of the programmed value before turning back on to pump up the output voltage again. This gives an average positive offset of approximately 15mV. If both _PFM and _PWM bits are zero then the regulator automatically transitions between PWM and PFM mode. If both _PFM and _PWM bits are set then the regulator is forced into PFM mode. Do not set both _PFM and _PWM (try to force both PFM and PWM modes) bits at the same time

There are two current limits – a higher one and a lower one - for the DCD0 and DCD1 regulators. They are approximately 7A and 6A. The lower limit over current protection may be turned on or off through the DCDx_EILIM register. The synchronization between DCD0 through DCD3 is configurable through the DCD_DLY register. Also through the DCD_DLY register phase A and B can be programmed to switch at the same time instead of 180° out of phase.

Register bits description

<table>
<tr><td>DCD0_VOUT
DCD1_VOUT</td><td>Output voltage setting for DCD0 and DCD1, see
Table 41 for valid voltage settings.
Output voltage setting also depends on the selected voltage range (Table 57).
<table>
<tr><th colspan="2">Address</th><th>Name</th><th>Bit[7]</th><th>Bit[6]</th><th>Bit[5]</th><th>Bit[4]</th><th>Bit[3]</th><th>Bit[2]</th><th>Bit[1]</th><th>Bit[0]</th><th>R/W</th></tr>
<tr><td rowspan="2">7E</td><td rowspan="2">126</td><td>DCD_RANGE</td><td>-</td><td>-</td><td>DCD1_LS</td><td>DCD0_LS</td><td>-</td><td>-</td><td>-</td><td>-</td><td>R/W</td></tr>
<tr><td>Default</td><td>-</td><td>-</td><td>1</td><td>1</td><td>-</td><td>-</td><td>-</td><td>-</td><td></td></tr>
</table></td></tr>
<tr><td>DCD0_VDVS
DCD1_VDVS</td><td>DVS voltage setting for DCD0 and DCD1, see
Table 41 for valid voltage settings.
Output voltage setting also depends on the selected voltage range (Table 57).
<table>
<tr><th colspan="2">Address</th><th>Name</th><th>Bit[7]</th><th>Bit[6]</th><th>Bit[5]</th><th>Bit[4]</th><th>Bit[3]</th><th>Bit[2]</th><th>Bit[1]</th><th>Bit[0]</th><th>R/W</th></tr>
<tr><td rowspan="2">7E</td><td rowspan="2">126</td><td>DCD_RANGE</td><td>-</td><td>-</td><td>DCD1_LS</td><td>DCD0_LS</td><td>-</td><td>-</td><td>-</td><td>-</td><td>R/W</td></tr>
<tr><td>Default</td><td>-</td><td>-</td><td>1</td><td>1</td><td>-</td><td>-</td><td>-</td><td>-</td><td></td></tr>
</table>
DVS stands for Dynamic Voltage Scaling. The output voltage can be changed while active between its _VOUT voltage and its _VDVS voltage through programming of the _DVS bit.</td></tr>
<tr><td>DCD0_DVS
DCD1_DVS</td><td>Toggle between the normal DCD0/1_VOUT voltage (DCD0/1_DVS = “0”)
And its Dynamically Scaled DCD0/1_VDVS voltage (DCD0/1_DVS = “1”).
If DVDx_DVS = “0” then DVS will be disabled when DCD0 is disabled. and the DVDx_DVS bit is reset to “0”
If DVDx_DVS = “1” the DVS will be disabled when DCDx is disabled. HOWEVER, DVDx_DVS bits remain “1”. When DCDx is again enabled, Vout will charge up to the programmed DCDx_VOUT value, wait for power good, and finally change the Vout to the DCDx_VDVS programmed value.</td></tr>
</table>

<table>
<tr><td>DCD0_PDVS
DCD1_PDVS</td><td>If DCD0_PDVS = “1” the output voltage of DCD0 is controlled by the voltage setting in register DCD0_VOUT plus a voltage offset determined by the PWM_DVS interface. There are two PWM_DVS interfaces. Each interface consists of two pins: a clock and a data.
The physical clock/data pins pairs available are:
1. GPIO4/GPIO5 (PCLK0/PDATA0 – controls DCD0 PWM_DVS interface)
2. GPIO3/GPIO2 (PCLK1/PDATA1 – controls DCD1 PWM_DVS interface).</td></tr>
<tr><td>DCD0_SR
DCD1_SR</td><td>Output slew rate setting. See Table 5 and Table 8 for available slew rates.</td></tr>
<tr><td>DCD2_VOUT
DCD3_VOUT</td><td>Output voltage setting for DCD2 and DCD3, see Table 42 for valid voltage settings. Output voltage setting also depends on the selected voltage range set by DCD2_RNG and DCD3_RNG.</td></tr>
<tr><td>DCD2_RNG
DCD3_RNG</td><td>Output voltage range setting, see Table 40</td></tr>
<tr><td>DCD0_PIN …
DCD3_PIN</td><td>If “1” then regulator enable controlled by external input to either PEN0 or PEN1 as determined by the DCDx_PEN bit.
If “0” then enabled through start up Sequence and Timing registers (see Table 45) or REG_ON1 (see Table 39) register</td></tr>
<tr><td>DCD0_PEN …
DCD3_PEN</td><td>If “0” then DCDx is controlled by pin PEN0. If “1” then DCDx is controlled by pin PEN1.</td></tr>
<tr><td>DCD0_PWM …
DCD3_PWM
DCD0a_PWM</td><td>If DCDx_PWM = “1” the regulator is forced to PWM mode independent of the load.
If DCDx_PWM = “0” and DCDx_PFM = “0” the regulator transitions automatically between PWM and PFM mode, depending on the load.
DCD0_PWM is set to “1” by default.
DCD0a is created (and DCD0 becomes DCD0b) when DCD0 is split into 2 single phase regulators through setting bit DCD0_SPL (Table 58)</td></tr>
<tr><td>DCD0_PFM …
DCD3_PFM
DCD0a_PFM</td><td>If DCDx_PFM = “1” the regulator is forced to PFM mode independent of the load. Forcing it to PFM mode should only be done if the load is known and low enough, otherwise the output voltage will drop down. It is recommended to leave all DCDx_PFM bits at “0”.</td></tr>
<tr><td>DCD0_EILIM …
DCD3_EILIM
DCD0a_EILIM</td><td>If “1” then enable lower current limit
If “0” then disable lower current limit. Still have higher current limit.</td></tr>
<tr><td>DCD0_PG …
DCD3_PG
DCD0a_PG</td><td>When the related voltage comes into the programmed regulation voltage this bit is set to “1”</td></tr>
<tr><td>DCD_DLY</td><td>Introduce delay between each of the four switching regulators (DCD0-DCD3) to avoid beating against each other.
<table>
<tr><th>DCD_DLY</th><th>Functional Description</th></tr>
<tr><td>00</td><td>DCD3 switches first.
Wait 6ns. DCD2 switches.
Wait 6ns. DCD1 switches.
Wait 6ns. DCD0 switches last</td></tr>
<tr><td>01</td><td>DCD0 switches first.
Wait 6ns. DCD1 switches.
Wait 6ns. DCD2 switches.
Wait 6ns. DCD3 switches last</td></tr>
<tr><td>10</td><td>No delays.
DCD0 through DCD3 all switch at same time.</td></tr>
<tr><td>11</td><td>DCD2 and DCD3 both switch at the same time.
Wait 12ns. DCD1 switches.
Wait 6ns. DCD0 switches last</td></tr>
</table></td></tr>
<tr><td>PAR_PHAB</td><td>If set to “1” the parallel phase A and B of DCD0 such that both switch at same time</td></tr>
</table>

Table 41– DCD0/1 Regulator Output Voltage Ranges

LS =	0	DCD0/1		LS =	1	DCD0/1	
VOUT [V]	Code			VOUT [V]	Code		
	dec	hex	bin		dec	hex	bin
0.5375	0	00	000000	0.7625	0	00	000000
0.5500	1	01	000001	0.7750	1	01	000001
0.5625	2	02	000010	0.7875	2	02	000010
0.5750	3	03	000011	0.8000	3	03	000011
0.5875	4	04	000100	0.8125	4	04	000100
0.6000	5	05	000101	0.8250	5	05	000101
0.6125	6	06	000110	0.8375	6	06	000110
0.6250	7	07	000111	0.8500	7	07	000111
0.6375	8	08	001000	0.8625	8	08	001000
0.6500	9	09	001001	0.8750	9	09	001001
0.6625	10	0A	001010	0.8875	10	0A	001010
0.6750	11	0B	001011	0.9000	11	0B	001011
0.6875	12	0C	001100	0.9125	12	0C	001100
0.7000	13	0D	001101	0.9250	13	0D	001101
0.7125	14	0E	001110	0.9375	14	0E	001110
0.7250	15	0F	001111	0.9500	15	0F	001111
0.7375	16	10	010000	0.9625	16	10	010000
0.7500	17	11	010001	0.9750	17	11	010001
0.7625	18	12	010010	0.9875	18	12	010010
0.7750	19	13	010011	1.0000	19	13	010011
0.7875	20	14	010100	1.0125	20	14	010100
0.8000	21	15	010101	1.0250	21	15	010101
0.8125	22	16	010110	1.0375	22	16	010110
0.8250	23	17	010111	1.0500	23	17	010111
0.8375	24	18	011000	1.0625	24	18	011000
0.8500	25	19	011001	1.0750	25	19	011001
0.8625	26	1A	011010	1.0875	26	1A	011010
0.8750	27	1B	011011	1.1000	27	1B	011011
0.8875	28	1C	011100	1.1125	28	1C	011100
0.9000	29	1D	011101	1.1250	29	1D	011101
0.9125	30	1E	011110	1.1375	30	1E	011110
0.9250	31	1F	011111	1.1500	31	1F	011111
0.9375	32	20	100000	1.1625	32	20	100000
0.9500	33	21	100001	1.1750	33	21	100001
0.9625	34	22	100010	1.1875	34	22	100010
0.9750	35	23	100011	1.2000	35	23	100011
0.9875	36	24	100100	1.2125	36	24	100100
1.0000	37	25	100101	1.2250	37	25	100101
1.0125	38	26	100110	1.2375	38	26	100110
1.0250	39	27	100111	1.2500	39	27	100111
1.0375	40	28	101000	1.2625	40	28	101000
1.0500	41	29	101001	1.2750	41	29	101001
1.0625	42	2A	101010	1.2875	42	2A	101010
1.0750	43	2B	101011	1.3000	43	2B	101011
1.0875	44	2C	101100	1.3125	44	2C	101100
1.1000	45	2D	101101	1.3250	45	2D	101101
1.1125	46	2E	101110	1.3375	46	2E	101110
1.1250	47	2F	101111	1.3500	47	2F	101111
1.1375	48	30	110000	1.3625	48	30	110000
1.1500	49	31	110001	1.3750	49	31	110001
1.1625	50	32	110010	1.3875	50	32	110010
1.1750	51	33	110011	1.4000	51	33	110011
1.1875	52	34	110100	1.4125	52	34	110100
1.2000	53	35	110101	1.4250	53	35	110101
1.2125	54	36	110110	1.4375	54	36	110110
1.2250	55	37	110111	1.4500	55	37	110111
1.2375	56	38	111000	1.4625	56	38	111000
1.2500	57	39	111001	1.4750	57	39	111001
1.2625	58	3A	111010	1.4875	58	3A	111010
1.2750	59	3B	111011	1.5000	59	3B	111011
1.2875	60	3C	111100	1.5125	60	3C	111100
1.3000	61	3D	111101	1.5250	61	3D	111101
1.3125	62	3E	111110	1.5375	62	3E	111110
1.3250	63	3F	111111	1.5500	63	3F	111111

Table 42– DCD2/3 Regulator Output Voltage Ranges

RANGE =	0	DCD2/3		RANGE =	1	DCD2/3		RANGE =	2	DCD2/3		RANGE =	3	DCD2/3	
VOUT [V]	Code			VOUT [V]	Code			VOUT [V]	\			VOUT [V]	Code		
	dec	hex	bin		dec	hex	bin		dec	hex	bin		dec	hex	bin
0.5250	0	00	000000	1.2000	0	00	000000	1.8750	0	00	000000	2.5500	0	00	000000
0.5375	1	01	000001	1.2125	1	01	000001	1.8875	1	01	000001	2.5625	1	01	000001
0.5500	2	02	000010	1.2250	2	02	000010	1.9000	2	02	000010	2.5750	2	02	000010
0.5625	3	03	000011	1.2375	3	03	000011	1.9125	3	03	000011	2.5875	3	03	000011
0.5750	4	04	000100	1.2500	4	04	000100	1.9250	4	04	000100	2.6000	4	04	000100
0.5875	5	05	000101	1.2625	5	05	000101	1.9375	5	05	000101	2.6125	5	05	000101
0.6000	6	06	000110	1.2750	6	06	000110	1.9500	6	06	000110	2.6250	6	06	000110
0.6125	7	07	000111	1.2875	7	07	000111	1.9625	7	07	000111	2.6375	7	07	000111
0.6250	8	08	001000	1.3000	8	08	001000	1.9750	8	08	001000	2.6500	8	08	001000
0.6375	9	09	001001	1.3125	9	09	001001	1.9875	9	09	001001	2.6625	9	09	001001
0.6500	10	0A	001010	1.3250	10	0A	001010	2.0000	10	0A	001010	2.6750	10	0A	001010
0.6625	11	0B	001011	1.3375	11	0B	001011	2.0125	11	0B	001011	2.6875	11	0B	001011
0.6750	12	0C	001100	1.3500	12	0C	001100	2.0250	12	0C	001100	2.7000	12	0C	001100
0.6875	13	0D	001101	1.3625	13	0D	001101	2.0375	13	0D	001101	2.7125	13	0D	001101
0.7000	14	0E	001110	1.3750	14	0E	001110	2.0500	14	0E	001110	2.7250	14	0E	001110
0.7125	15	0F	001111	1.3875	15	0F	001111	2.0625	15	0F	001111	2.7375	15	0F	001111
0.7250	16	10	010000	1.4000	16	10	010000	2.0750	16	10	010000	2.7500	16	10	010000
0.7375	17	11	010001	1.4125	17	11	010001	2.0875	17	11	010001	2.7625	17	11	010001
0.7500	18	12	010010	1.4250	18	12	010010	2.1000	18	12	010010	2.7750	18	12	010010
0.7625	19	13	010011	1.4375	19	13	010011	2.1125	19	13	010011	2.7875	19	13	010011
0.7750	20	14	010100	1.4500	20	14	010100	2.1250	20	14	010100	2.8000	20	14	010100
0.7875	21	15	010101	1.4625	21	15	010101	2.1375	21	15	010101	2.8125	21	15	010101
0.8000	22	16	010110	1.4750	22	16	010110	2.1500	22	16	010110	2.8250	22	16	010110
0.8125	23	17	010111	1.4875	23	17	010111	2.1625	23	17	010111	2.8375	23	17	010111
0.8250	24	18	011000	1.5000	24	18	011000	2.1750	24	18	011000	2.8500	24	18	011000
0.8375	25	19	011001	1.5125	25	19	011001	2.1875	25	19	011001	2.8625	25	19	011001
0.8500	26	1A	011010	1.5250	26	1A	011010	2.2000	26	1A	011010	2.8750	26	1A	011010
0.8625	27	1B	011011	1.5375	27	1B	011011	2.2125	27	1B	011011	2.8875	27	1B	011011
0.8750	28	1C	011100	1.5500	28	1C	011100	2.2250	28	1C	011100	2.9000	28	1C	011100
0.8875	29	1D	011101	1.5625	29	1D	011101	2.2375	29	1D	011101	2.9125	29	1D	011101
0.9000	30	1E	011110	1.5750	30	1E	011110	2.2500	30	1E	011110	2.9250	30	1E	011110
0.9125	31	1F	011111	1.5875	31	1F	011111	2.2625	31	1F	011111	2.9375	31	1F	011111
0.9250	32	20	100000	1.6000	32	20	100000	2.2750	32	20	100000	2.9500	32	20	100000
0.9375	33	21	100001	1.6125	33	21	100001	2.2875	33	21	100001	2.9625	33	21	100001
0.9500	34	22	100010	1.6250	34	22	100010	2.3000	34	22	100010	2.9750	34	22	100010
0.9625	35	23	100011	1.6375	35	23	100011	2.3125	35	23	100011	2.9875	35	23	100011
0.9750	36	24	100100	1.6500	36	24	100100	2.3250	36	24	100100	3.0000	36	24	100100
0.9875	37	25	100101	1.6625	37	25	100101	2.3375	37	25	100101	3.0125	37	25	100101
1.0000	38	26	100110	1.6750	38	26	100110	2.3500	38	26	100110	3.0250	38	26	100110
1.0125	39	27	100111	1.6875	39	27	100111	2.3625	39	27	100111	3.0375	39	27	100111
1.0250	40	28	101000	1.7000	40	28	101000	2.3750	40	28	101000	3.0500	40	28	101000
1.0375	41	29	101001	1.7125	41	29	101001	2.3875	41	29	101001	3.0625	41	29	101001
1.0500	42	2A	101010	1.7250	42	2A	101010	2.4000	42	2A	101010	3.0750	42	2A	101010
1.0625	43	2B	101011	1.7375	43	2B	101011	2.4125	43	2B	101011	3.0875	43	2B	101011
1.0750	44	2C	101100	1.7500	44	2C	101100	2.4250	44	2C	101100	3.1000	44	2C	101100
1.0875	45	2D	101101	1.7625	45	2D	101101	2.4375	45	2D	101101	3.1125	45	2D	101101
1.1000	46	2E	101110	1.7750	46	2E	101110	2.4500	46	2E	101110	3.1250	46	2E	101110
1.1125	47	2F	101111	1.7875	47	2F	101111	2.4625	47	2F	101111	3.1375	47	2F	101111
1.1250	48	30	110000	1.8000	48	30	110000	2.4750	48	30	110000	3.1500	48	30	110000
1.1375	49	31	110001	1.8125	49	31	110001	2.4875	49	31	110001	3.1625	49	31	110001
1.1500	50	32	110010	1.8250	50	32	110010	2.5000	50	32	110010	3.1750	50	32	110010
1.1625	51	33	110011	1.8375	51	33	110011	2.5125	51	33	110011	3.1875	51	33	110011
1.1750	52	34	110100	1.8500	52	34	110100	2.5250	52	34	110100	3.2000	52	34	110100
1.1875	53	35	110101	1.8625	53	35	110101	2.5375	53	35	110101	3.2125	53	35	110101
1.2000	54	36	110110	1.8750	54	36	110110	2.5500	54	36	110110	3.2250	54	36	110110
1.2125	55	37	110111	1.8875	55	37	110111	2.5625	55	37	110111	3.2375	55	37	110111
1.2250	56	38	111000	1.9000	56	38	111000	2.5750	56	38	111000	3.2500	56	38	111000
1.2375	57	39	111001	1.9125	57	39	111001	2.5875	57	39	111001	3.2625	57	39	111001
1.2500	58	3A	111010	1.9250	58	3A	111010	2.6000	58	3A	111010	3.2750	58	3A	111010
1.2625	59	3B	111011	1.9375	59	3B	111011	2.6125	59	3B	111011	3.2875	59	3B	111011
1.2750	60	3C	111100	1.9500	60	3C	111100	2.6250	60	3C	111100	3.3000	60	3C	111100
1.2875	61	3D	111101	1.9625	61	3D	111101	2.6375	61	3D	111101	3.3125	61	3D	111101
1.3000	62	3E	111110	1.9750	62	3E	111110	2.6500	62	3E	111110	3.3250	62	3E	111110
1.3125	63	3F	111111	1.9875	63	3F	111111	2.6625	63	3F	111111	3.3375	63	3F	111111

LDOs Voltage Setting and Configuration

Table 43– LDO configuration registers

Address Hex	Address Dec	Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	R/W
14	20	**LDO0C**	LDO0_PIN	LDO0_PEN	LDO0_VOUT[5:0]						R/W
15	21	**LDO1C**	LDO1_PIN	LDO1_PEN	LDO1_VOUT[5:0]						R/W
16	22	**LDO2C**	LDO2_PIN	LDO2_PEN	LDO2_VOUT[5:0]						R/W
17	23	**LDO3C**	LDO3_PIN	LDO3_PEN	LDO3_VOUT[5:0]						R/W
18	24	**LDOTRC0**	-	LDOTR_VOUT[6:0]							R/W
19	25	**LDOTRC1**	-	-	-	-	-	LDOTR_PIN	LDOTR_PEN	LDOTR_TRC	R/W
1A	26	**LDO4C**	LDO4_PIN	LDO4_PEN	LDO4_VOUT[5:0]						R/W
1B	27	**LDO5C**	LDO5_PIN	LDO5_PEN	LDO5_VOUT[5:0]						R/W
1C	28	**LDO6C**	LDO6_PIN	LDO6_PEN	LDO6_VOUT[5:0]						R/W
1D	29	**LDO7C**	LDO7_PIN	LDO7_PEN	LDO7_VOUT[5:0]						R/W
1E	30	**LDO8C**	LDO8_PIN	LDO8_PEN	LDO8_VOUT[5:0]						R/W
1F	31	**LDO9C**	-	-	LDO9_VOUT[5:0]						R/W
20	32	**RESERVED**	-	-	-	-	-	-	-	-	R/W
21	33	**LDOF0**				LDO3_SC	LDOTR_SC	LDO2_SC	LDO1_SC	LDO0_SC	R
		Default				R	R	R	R	R	

Registers 20 to 34 configure the output voltages of the 11 LDOs,

The LDO voltages are programmed through the LDOx_VOUT registers. LDO is controlled by either PEN0 or PEN1 through the LDOx_PIN bits. For example, suppose the user wants LDO5 to output 1.5V only when PEN1 goes high. To program 1.5V write “001010” (see Table 44) into LDO5_VOUT. To activate the PEN mode write “1” to LDO5_PIN. To respond to PEN1 (instead of PEN0) write “1” to LDO5_PEN.

After start-up from OFF state, the output voltage of LDO9 is the same as LDO8. If another voltage setting for LDO9 is required, the user needs to configure the setting via I^2C before turning on the LDO.

The tracking LDO (LDOTR) tracks either DCD0 or DCD1 voltage (depending on the **LDOTR_SEL** bit) if LDOTR_TRC = “1”. Since the output voltage range for LDOTR is 0.6V to 1.4875V the DCD1 output voltage must stay within those range when tracking is enabled.

LDOx_SC are real time short circuit status bits. They are set to “1” when an over current is detected, and set to “0” when the over current ceases.

Register bits description

LDO0_VOUT … LDO8_VOUT	Programs the output voltage. LDO0-2,5-9 have a range of 1V to 3.35V. LDO3,4 have a range of 1V to 1.475V
LDO0_PEN … LDO8_PEN LDOTR_PEN	If associated LDOx_PIN = 1 then these bits assign the enable signal to either PEN0 or PEN1 physical PMIC pins. If “0” then regulator enable controlled by external signal to PEN0. If “1” then regulator enable controlled by external signal to PEN1
LDO0_PIN … LDO8_PIN LDOTR_PIN	The LDOx_PIN bit determines if the regulator will be activated by one of the two physical PEN pins of the PMIC. If “1” the regulator is turned on by a signal applied either the PEN0 or PEN1 pins depending on the LDOx_PEN bit. If “0” then enabled through start up Sequence and Timing registers (see **Table 45**) or REG_ONx (see **Table 39**) register.
LDOTR_VOUT	Programs the output voltage of the tracking LDO. If LDOTR_TRC=”1” then LDOTR_VOUT is over ridden and LDOTR tracks DCD0 or DCD1 (depending on the **LDOTR_SEL** bit) exactly with no offset.
LDOTR_TRC	Enables LDOTR to track the output of the DCD0/1 regulator (depending on the **LDOTR_SEL** bit) when set to “1” and DCD0/1 power-good signal is also “1”
LDO9_VOUT	Programs the output voltage of LDO9. After start-up from OFF state the output voltage setting for LDO9 is controlled by the setting of LDO8. If another voltage setting for LDO9 is required, the user needs to configure the setting via an I^2C write to these bits before turning on the LDO.
LDO0_SC … LDO9_SC LDOTR_SC	LDOx_SC are set to “1” when an over current is detected. They are automatically set to “0” once the over current condition ceases.

Table 44– LDO Output Voltage Ranges

LDOTR			
VOUT [V]	Code		
	dec	hex	bin
0.6000	0	00	0000000
0.6125	1	01	0000001
0.6250	2	02	0000010
0.6375	3	03	0000011
0.6500	4	04	0000100
0.6625	5	05	0000101
0.6750	6	06	0000110
0.6875	7	07	0000111
0.7000	8	08	0001000
0.7125	9	09	0001001
0.7250	10	0A	0001010
0.7375	11	0B	0001011
0.7500	12	0C	0001100
0.7625	13	0D	0001101
0.7750	14	0E	0001110
0.7875	15	0F	0001111
0.8000	16	10	0010000
0.8125	17	11	0010001
0.8250	18	12	0010010
0.8375	19	13	0010011
0.8500	20	14	0010100
0.8625	21	15	0010101
0.8750	22	16	0010110
0.8875	23	17	0010111
0.9000	24	18	0011000
0.9125	25	19	0011001
0.9250	26	1A	0011010
0.9375	27	1B	0011011
0.9500	28	1C	0011100
0.9625	29	1D	0011101
0.9750	30	1E	0011110
0.9875	31	1F	0011111
1.0000	32	20	0100000
1.0125	33	21	0100001
1.0250	34	22	0100010
1.0375	35	23	0100011
1.0500	36	24	0100100
1.0625	37	25	0100101
1.0750	38	26	0100110
1.0875	39	27	0100111
1.1000	40	28	0101000
1.1125	41	29	0101001
1.1250	42	2A	0101010
1.1375	43	2B	0101011
1.1500	44	2C	0101100
1.1625	45	2D	0101101
1.1750	46	2E	0101110
1.1875	47	2F	0101111
1.2000	48	30	0110000
1.2125	49	31	0110001
1.2250	50	32	0110010
1.2375	51	33	0110011
1.2500	52	34	0110100
1.2625	53	35	0110101
1.2750	54	36	0110110
1.2875	55	37	0110111
1.3000	56	38	0111000
1.3125	57	39	0111001
1.3250	58	3A	0111010
1.3375	59	3B	0111011
1.3500	60	3C	0111100
1.3625	61	3D	0111101
1.3750	62	3E	0111110
1.3875	63	3F	0111111
1.4000	64	40	1000000
1.4125	65	41	1000001
1.4250	66	42	1000010
1.4375	67	43	1000011
1.4500	68	44	1000100
1.4625	69	45	1000101
1.4750	70	46	1000110
1.4875	71	47	1000111

LDO0, 1, 2, 5, 6, 7, 8, 9			
VOUT [V]	Code		
	dec	hex	bin
1.0000	0	00	000000
1.0500	1	01	000001
1.1000	2	02	000010
1.1500	3	03	000011
1.2000	4	04	000100
1.2500	5	05	000101
1.3000	6	06	000110
1.3500	7	07	000111
1.4000	8	08	001000
1.4500	9	09	001001
1.5000	10	0A	001010
1.5500	11	0B	001011
1.6000	12	0C	001100
1.6500	13	0D	001101
1.7000	14	0E	001110
1.7500	15	0F	001111
1.8000	16	10	010000
1.8500	17	11	010001
1.9000	18	12	010010
1.9500	19	13	010011
2.0000	20	14	010100
2.0500	21	15	010101
2.1000	22	16	010110
2.1500	23	17	010111
2.2000	24	18	011000
2.2500	25	19	011001
2.3000	26	1A	011010
2.3500	27	1B	011011
2.4000	28	1C	011100
2.4500	29	1D	011101
2.5000	30	1E	011110
2.5500	31	1F	011111
2.6000	32	20	100000
2.6500	33	21	100001
2.7000	34	22	100010
2.7500	35	23	100011
2.8000	36	24	100100
2.8500	37	25	100101
2.9000	38	26	100110
2.9500	39	27	100111
3.0000	40	28	101000
3.0500	41	29	101001
3.1000	42	2A	101010
3.1500	43	2B	101011
3.2000	44	2C	101100
3.2500	45	2D	101101
3.3000	46	2E	101110
3.3500	47	2F	101111

LDO3, 4			
VOUT [V]	Code		
	dec	hex	bin
1.0000	0	00	00000
1.0250	1	01	00001
1.0500	2	02	00010
1.0750	3	03	00011
1.1000	4	04	00100
1.1250	5	05	00101
1.1500	6	06	00110
1.1750	7	07	00111
1.2000	8	08	01000
1.2250	9	09	01001
1.2500	10	0A	01010
1.2750	11	0B	01011
1.3000	12	0C	01100
1.3250	13	0D	01101
1.3500	14	0E	01110
1.3750	15	0F	01111
1.4000	16	10	10000
1.4250	17	11	10001
1.4500	18	12	10010
1.4750	19	13	10011

Sequencing and Timing Configuration

Table 45– Sequencing configuration registers for regulators, GPIOs, and ENEXT pin

Address		Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	R/W
23	35	DCD0_GRP (DCD0a_GRP)	DCD0_SSEQ (DCD0a_SSEQ)	DCD0_OSEQ (DCD0a_OSEQ)	DCD0_GRP_SLEEP[2:0] (DCD0a_GRP_SLEEP[2:0])			DCD0_GRP_ON[2:0] DCD0a_GRP_ON[2:0]			R/W
		Default	0	OTP	Equals Bits[2:0], OTP'd value			OTP - One Time Programmable			
24	36	DCD1_GRP	DCD1_SSEQ	DCD1_OSEQ	DCD1_GRP_SLEEP[2:0]			DCD1_GRP_ON[2:0]			R/W
		Default	0	OTP	Equals Bits[2:0], OTP'd value			OTP			
25	37	DCD2_GRP	DCD2_SSEQ	DCD2_OSEQ	DCD2_GRP_SLEEP[2:0]			DCD2_GRP_ON[2:0]			R/W
		Default	0	OTP	Equals Bits[2:0], OTP'd value			OTP			
26	38	DCD3_GRP	DCD3_SSEQ	DCD3_OSEQ	DCD3_GRP_SLEEP[2:0]			DCD3_GRP_ON[2:0]			R/W
		Default	0	OTP	Equals Bits[2:0], OTP'd value			OTP			
27	39	LDO0_GRP	LDO0_SSEQ	LDO0_OSEQ	LDO0_GRP_SLEEP[2:0]			LDO0_GRP_ON[2:0]			R/W
		Default	0	OTP	Equals Bits[2:0], OTP'd value			OTP			
28	40	LDO1_GRP	LDO1_SSEQ	LDO1_OSEQ	LDO1_GRP_SLEEP[2:0]			LDO1_GRP_ON[2:0]			R/W
		Default	0	OTP	Equals Bits[2:0], OTP'd value			OTP			
29	41	LDO2_GRP	LDO2_SSEQ	LDO2_OSEQ	LDO2_GRP_SLEEP[2:0]			LDO2_GRP_ON[2:0]			R/W
		Default	0	OTP	Equals Bits[2:0], OTP'd value			OTP			
2A	42	LDO3_GRP	LDO3_SSEQ	LDO3_OSEQ	LDO3_GRP_SLEEP[2:0]			LDO3_GRP_ON[2:0]			R/W
		Default	0	OTP	Equals Bits[2:0], OTP'd value			OTP			
2B	43	LDOTR_GRP	LDOTR_SSEQ	LDOTR_OSEQ	LDOTR_GRP_SLEEP[2:0]			LDOTR_GRP_ON[2:0]			R/W
		Default	0	OTP	Equals Bits[2:0], OTP'd value			OTP			
2C	44	LDO4_GRP	LDO4_SSEQ	LDO4_OSEQ	LDO4_GRP_SLEEP[2:0]			LDO4_GRP_ON[2:0]			R/W
		Default	0	OTP	Equals Bits[2:0], OTP'd value			OTP			
2D	45	LDO5_GRP	LDO5_SSEQ	LDO5_OSEQ	LDO5_GRP_SLEEP[2:0]			LDO5_GRP_ON[2:0]			R/W
		Default	0	OTP	Equals Bits[2:0], OTP'd value			OTP			
2E	46	LDO6_GRP	LDO6_SSEQ	LDO6_OSEQ	LDO6_GRP_SLEEP[2:0]			LDO6_GRP_ON[2:0]			R/W
		Default	0	OTP	Equals Bits[2:0], OTP'd value			OTP			
2F	47	LDO7_GRP	LDO7_SSEQ	LDO7_OSEQ	LDO7_GRP_SLEEP[2:0]			LDO7_GRP_ON[2:0]			R/W
		Default	0	OTP	Equals Bits[2:0], OTP'd value			OTP			
30	48	LDO8_GRP	LDO8_SSEQ	LDO8_OSEQ	LDO8_GRP_SLEEP[2:0]			LDO8_GRP_ON[2:0]			R/W
		Default	0	OTP	Equals Bits[2:0], OTP'd value			OTP			
31	49	SEQ_TIM1	-	DLY_ON6	DLY_ON5	DLY_ON4	DLY_ON3	DLY_ON2	DLY_ON1	DLY_ON0	R/W
		Default	-	OTP	OTP	OTP	OTP	OTP	OTP	OTP	
32	50	SEQ_TIM2	DLY_GRP3[1:0]		DLY_GRP2[1:0]		DLY_GRP1[1:0]		DLY_GRP0[1:0]		R/W
		Default	OTP		OTP		OTP		OTP		
33	51	SEQ_TIM3	-	-	DLY_GRP6[1:0]		DLY_GRP5[1:0]		DLY_GRP4[1:0]		R/W
		Default	-	-	OTP		OTP		OTP		
34	52	ENDDR_GRP (DCD0b_GRP)	ENDDR_SSEQ (DCD0b_SSEQ)	ENDDR_OSEQ (DCD0b_OSEQ)	ENDDR_GRP_SLEEP[2:0] (DCD0b_GRP_SLEEP[2:0])			ENDDR_GRP_ON[2:0] (DCD0b_GRP_ON[2:0])			R/W
		Default	0	OTP	Equals Bits[2:0], OTP'd value			OTP			
35	53	ENDDR_PEN (DCD0b_PEN)	-	-	-	-	-	-	ENDDR_PIN (DCD0b_PIN)	ENDDR_PEN (DCD0b_PEN)	R/W
		Default	-	-	-	-	-	-	OTP	OTP	
36	54	GPIO0_GRP	GPIO0_SSEQ	GPIO0_OSEQ	GPIO0_GRP_SLEEP[2:0]			GPIO0_GRP_ON[2:0]			R/W
		Default	0	OTP	Equals Bits[2:0], OTP'd value			OTP			
37	55	GPIO1_GRP	GPIO1_SSEQ	GPIO1_OSEQ	GPIO1_GRP_SLEEP[2:0]			GPIO1_GRP_ON[2:0]			R/W
		Default	0	OTP	Equals Bits[2:0], OTP'd value			OTP			
38	56	GPIO2_GRP	GPIO2_SSEQ	GPIO2_OSEQ	GPIO2_GRP_SLEEP[2:0]			GPIO2_GRP_ON[2:0]			R/W
		Default	0	OTP	Equals Bits[2:0], OTP'd value			OTP			
39	57	GPIO_PEN	-	-	GPIO2_PIN	GPIO1_PIN	GPIO0_PIN	GPIO2_PEN	GPIO1_PEN	GPIO0_PEN	R/W
		Default	-	-	OTP	OTP	OTP	OTP	OTP	OTP	

Registers 35 to 57 configure the regulators' behavior when the IC transitions between OFF/ON states

Only the ON-OFF sequencing can be hard coded; therefore, the desired behavior for SLEEP state entrance and exit needs to be configured before going into SLEEP state the first time. By default the ON-SLEEP-ON transition is identical to the ON-OFF-ON transition.

In order to have a regulator controlled by these sequencing registers the x_OSEQ must first be set to "1".

After that the order in which the regulator comes up is controlled by the x_GRP_ON bits. Group 0 comes up first, followed by group 1, group 2, …, and lastly group 7. The order is reversed for turning off: group 7 first and group 0 last.

The delay time between groups turning-on or off can be set individually from 1ms to 10ms.

To turn on the delay between groups set the appropriate DLY_ON bits to “1”. DLY_ON0 turns on the delay between group 0 and group 1. DLY_ON1 turns on the delay between group 1 and group 2, etc.

The DLY_GRP0 setting defines the delay time between group 0 and group 1, DLY_GRP1 sets the delay time between group 1 and group 2, etc.

For example, if the user wants DCD2 to come up first, wait 1ms, then DCD3, wait 4ms,then DCD1 and LDO0 together then the user must program the registers thus:

Include in sequencing:	DCD2_OSEQ=”1” DCD3_OSEQ=”1” DCD1_OSEQ=”1” LDO0_OSEQ=”1”
First group to turn on:	DCD2_GRP_ON=”000”
Second group to turn on:	DCD3_GRP_ON=”001”
Third group to turn on:	DCD1_GRP_ON=”010” LDO0_GRP_ON=”010”
Turn on the delays between groups:	DLY_ON0=”1” DLY_ON1=”1”
Delay between DCD2 and DCD3: 1ms:	DLY_GRP0=”00”
Delay between DCD3 and DCD1,LDO0: 4ms:	DLY_GRP1=”10”

Three of the GPIOs can be used as enable signals for external regulators and can be part of a sequence. If configured as an enable signal the GPIO is automatically configured as an output.

If DCD0 is split into DCD0a and DCD0b, then DCD0 registers control DCD0a and ENDDR registers control DCD0b.

NOTE: If a regulator is part of a sequence and at the same time assigned to an enable pin (PEN0 or PEN1), the regulator follows the programmed sequence until RSTB is asserted “1”. Once RSTB is asserted “1” the PENx pin controls the regulator.

Register bits description

DCDx_GRP_ON LDOx_GRP_ON ENDDR_GRP_ON GPIOx_GRP_ON	Group assignment for the OFF/ON state transitions. The lower numbered groups turn on first. Group 0 first, followed by group 1 etc. When turning off the lower number groups turn off later. Group 7, then 6, then 5 etc. (When DCD0 is split into DCD0a and DCD0b, then DCD0 registers control DCD0a and ENDDR registers control DCD0b)
DCDx_GRP_SLEEP LDOx_GRP_SLEEP ENDDR_GRP_SLEEP GPIOx_GRP_SLEEP	Group assignment for the ON/SLEEP state transitions. After start-up from OFF state the sleep setting is identical to the group assignment for the OFF/ON state transitions (e.g. DCD2_GRP_SLEEP = DCD2_GRP_ON). If a different behavior is required for SLEEP state entrance and exit, the bits need to be programmed after the IC starts up and before going into the SLEEP state.
DCDx_OSEQ LDOx_OSEQ ENDDR_OSEQ GPIOx_OSEQ	On Sequence. Regulators are assigned to sequencing scheme. Must be set to “1” to participate in the power up sequencing. *Note: if regulator’s x_PIN bit (DCD0_PIN or LDO2_PIN for example) in the previous registers is set to “1” then after RSTB is asserted high the regulator will no longer be part of the sequencing but will follow the assigned PEN physical pin signal.*
DCDx_SSEQ LDOx_SSEQ	Sleep Sequence. Regulator stays on in SLEEP mode if bit is set to “1”.

ENDDR_SSEQ GPIOx_SSEQ	If SSEQ = “0” the regulator follows its configured group assignment and turns-off or on when transitioning to SLEEP or ON state, respectively.
DLY_ON0 … DLY_ON6	Enable delay between groups. For example, DLY_ON0 enables the delay between groups 0 and 1. DLYON1 enables the group 1 to 2 delay, etc.
DLY_GRP0 … DLY_GRP6	Delay time between groups DLY_GRPx[1:0] = 00: 1ms DLY_GRPx[1:0] = 01: 2ms DLY_GRPx[1:0] = 10: 4ms DLY_GRPx[1:0] = 11: 10ms
GPIO0_PIN … GPIO2_PIN ENDDR_PIN	The PIN bit commands the PMIC to use either the PEN0 (“0”) or PEN1 (“1”) pin to enable regulator. If “0” then the sequencer will control the on/off timing of these digital pins If “1” then PEN0 or PEN1 physical pin will control the on/off state of these digital pins after RSTB is asserted “1”. *(Note: the first time RSTB transitions to the logic high state the sequencer will control the digital pins. Immediately after that the control will transfer to the assigned pin (either PEN0 or PEN1) and the pin will transition to the commanded logic state – high if the controlling PEN is high and low if the controlling PEN is low)*
GPIO0_PEN … GPIO2_PEN ENDDR_PEN	Assign regulator enable to PENx pin (masked when RSTB is low) If “0” then PEN0 physical pin will turn on/off the regulator after RSTB is asserted “1” If “1” then PEN1 controls instead

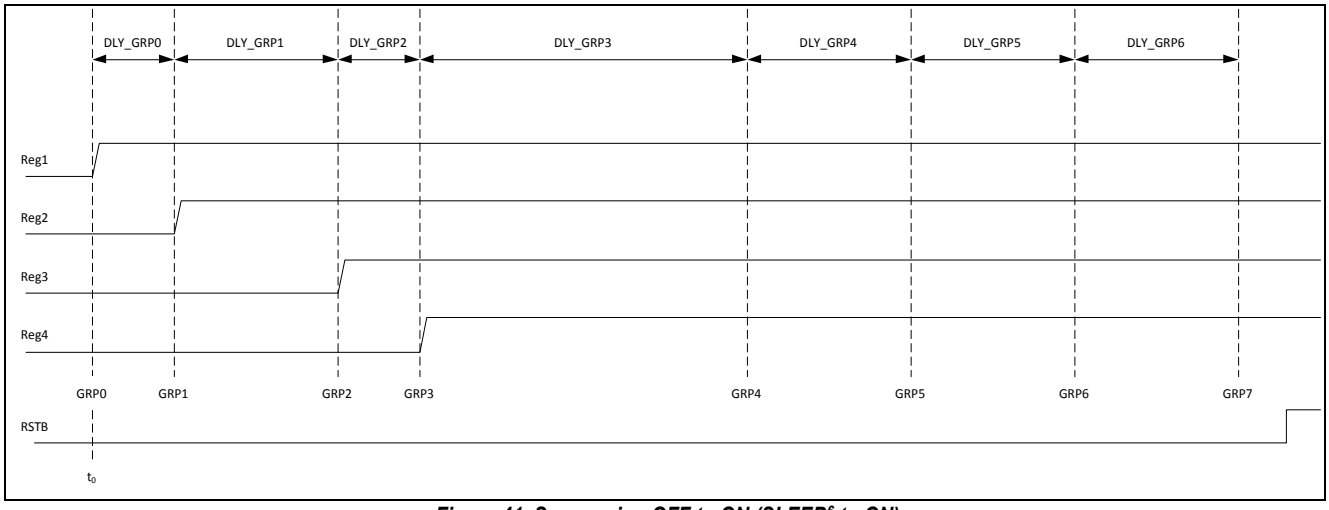


Figure 41. Sequencing OFF to ON (SLEEP[6] to ON)

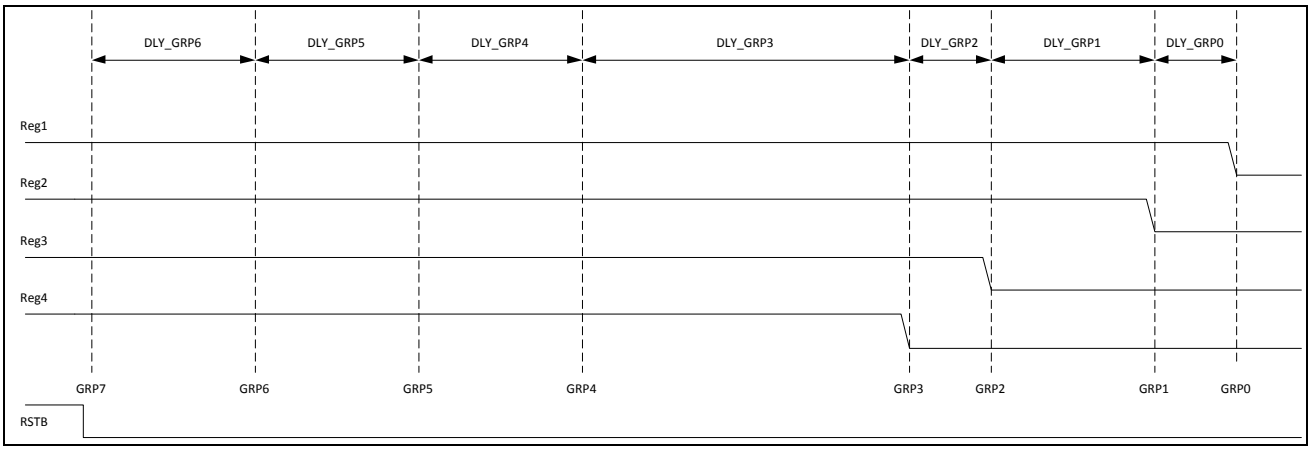


Figure 42. Sequencing ON to OFF (ON to SLEEP[6])

RTC Configuration

Table 46– RTC configuration registers

Address		Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	R/W
3A	58	**RTC_CTRL**	-	-	-	-	-	ALRM_EN	ALRM_INT	RTC_EN	R/W
		Default	-	-	-	-	-				
3B	59	**RTC_SEC**	-	RTC_TS[2:0]			RTC_S[3:0]				R/W
		Default	-	0			0				
3C	60	**RTC_MIN**	-	RTC_TMI[2:0]			RTC_MI[3:0]				R/W
		Default	-	0			0				
3D	61	**RTC_HR**	-	-	RTC_TH[1:0]		RTC_H[3:0]				R/W
		Default	-	-	0		0				
3E	62	**RTC_DOW**	-	-	-	-	-	RTC_DOW[2:0]			R/W
		Default	-	-	-	-	-	0			
3F	63	**RTC_DAY**	-	-	RTC_TD[1:0]		RTC_D[3:0]				R/W
		Default	-	-	0		0				
40	64	**RTC_MON**	-	-	-	RTC_TMO	RTC_MO[3:0]				R/W
		Default	-	-	-	0	0				
41	65	**RTC_YEAR**	RTC_TY[3:0]				RTC_Y[3:0]				R/W
		Default	0				0				
42	66	**ALRM_SEC**	-	ALRM_TS[2:0]			ALRM_S[3:0]				R/W
		Default	-	0			0				
43	67	**ALRM_MIN**	-	ALRM_TMI[2:0]			ALRM_MI[3:0]				R/W
		Default	-	0			0				
44	68	**ALRM_HR**	-	-	ALRM_TH[1:0]		ALRM_H[3:0]				R/W
		Default	-	-	0		0				
45	69	**ALRM_DOW**	-	-	-	-	-	ALRM_DOW[2:0]			R/W
		Default	-	-	-	-	-	0			
46	70	**ALRM_DAY**	-	-	ALRM_TD[1:0]		ALRM_D[3:0]				R/W
		Default	-	-	0		0				
47	71	**ALRM_MON**	-	-	-	ALRM_TMO	ALRM_MO[3:0]				R/W
		Default	-	-	-	0	0				
48	72	**ALRM_YEAR**	ALRM_TY[3:0]				ALRM_Y[3:0]				R/W
		Default	0				0				
49	73	**ALRM_CTRL**	ALARM	ALRM_Y	ALRM_MO	ALRM_D	ALRM_DOW	ALRM_H	ALRM_MI	ALRM_S	R/W
		Default	0	0	0	0	0	0	0	0	
4A	74	**RESERVED**	-	-	-	-	-	-	-	-	R/W
4B	75	**RESERVED**	-	-	-	-	-	-	-	-	R/W

Registers 58 to 73 configure the real-time clock (RTC) and the alarm setting.

If the RTC alarm is enabled and the IC is in ON or SLEEP state the RTC generates an interrupt to the microprocessor through the INTB pin. If the IC is in OFF state the RTC generates a wake-up event and starts-up the system.

The time and alarm is BCD coded and time and date is separated into seconds, minutes, hours, etc. The RTC assumes the clock operating from year 2000 until 2099 with automatic leap year correction. Reading the RTC_xxxx registers returns real time counter content.

Units are conveniently set into multiple of 1's and 10's. For example: RTC_H = real time hours, and RTC_TH = real time counter in units of 10 hours per count. Important note:

IMPORTANT: Even if the bits will allow it, do not program larger values than the ranges defined in the register bits description.

Register bits description

RTC_EN	RTC_EN = “1” enables the RTC. Before changing any bit in registers 54 to 60, the RTC needs to be disabled by setting. RTC_EN = “0”. After configuration of time and date the RTC can be re-enabled
ALRM_INT	ALRM_INT = “0” – Alarm is masked and no interrupt is generated ALRM_INT = “1” – Alarm generates an interrupt in register INT0 (see **Table 47**)
ALRM_EN	ALRM_EN = “0” – Alarm disabled, ALRM_EN = “1” – Alarm enabled. If the RTC alarm is enabled and the IC is in ON or SLEEP state, the RTC generates an interrupt to the microprocessor through the INTB pin. If the PMIC is in the OFF state, the RTC generates a wake-up event and starts-up the system.
RTC_S RTC_TS	Seconds and Ten seconds setting. RTC_S range is 0 to 9[1] RTC_TS range is 0 to 5[1],
RTC_MI RTC_TMI	Minutes and Ten minutes setting. RTC_M range is 0 to 9[1] RTC_TMI range is 0 to 5[1]
RTC_H RTC_TH	Hours and Ten hours setting. RTC_H range is 0 to 9[1] RTC_TH range is 0 to 2[1]
RTC_DOW	Day of week setting. RTC_DOW range is 1 to 7[1]
RTC_D RTC_TD	Days and Ten days setting. RTC_D range is 0 to 9[1] RTC_TD range is 0 to 3[1]
RTC_MO RTC_TMO	Months and Ten months setting. RTC_M range is 0 to 9[1] RTC_TM range is 0 to 1[1]
RTC_Y RTC_TY	Years and Ten years setting. RTC_Y range is 0 to 9[1] RTC_TY range is 0 to 9[1] The hundred years and thousand years bit are internally preset to 0 and 2, respectively. The RTC assumes operation between year 2000 and 2099
ALRM_S ALRM_TS	Seconds and Ten seconds setting. ALRM_S range is 0 to 9[1] ALRM_TS range is 0 to 5[1]
ALRM_MI ALRM_TMI	Minutes and Ten minutes setting. ALRM_M range is 0 to 9[1] ALRM_TMI range is 0 to 5[1]
ALRM_H ALRM_TH	Hours and Ten hours setting. ALRM_TH range is 0 to 2[1] ALRM_H range is 0 to 9[1]
ALRM_DOW	Day of week setting. ALRM_DOW range is 1 to 7[1]
ALRM_D ALRM_TD	Days and Ten days setting. ALRM_TD range is 0 to 3[1] ALRM _D range is 0 to 9[1]
ALRM_MO ALRM_TMO	Months and Ten months setting. ALRM _TM range is 0 to 1[1]

Note [1] Important note: Even if the bits will allow it, do not program larger values than the ranges defined in the register bits description.

	ALRM _M range is 0 to 9[1]
ALRM_Y ALRM_TY	Years and Ten years setting. ALRM_TY range is 0 to 9[1] ALRM_Y range is 0 to 9[1]
ALRM_S ALRM_MI ALRM_H ALRM_DOW ALRM_D ALRM_MO ALRM_Y	If the RTC time and date counter matches the setting in the ALRM registers and the enable bits are set in ALRM_CTRL register, an alarm is generated in the RTC bit of the INTO register (see **Table 47**). Example: For an alarm every day at the same time, bits ALRM_H, ALRM_MI, ALRM_S need to be set to “1”. The other bits (ALRM_Y, ALRM_MO, ALRM_D, ALRM_DOW) must be set to “0”
ALARM	ALARM = “0” – No alarm, ALARM = “1” – Alarm occurred. The ALARM bit stores an alarm event in OFF state and can be read once the PMIC has started-up and is in ON state. A write operation to the ALRM_CTRL register clears the bit.

Interrupt and Interrupt Enable

Table 47– Interrupt configuration registers

Address		Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	R/W
4C	76	**INT0**	OC	LID	ACOK	GPIO	VBAT	-	RTC	OT	RW1C *Read Status Write to Clear*
		Default	0	0	0	0	0	0	0	0	
4D	77	**INT1**	-	-	-	-	-	PEN	ONKEY_LP	ONKEY	RW1C *Read Status Write to Clear*
		Default	-	-	-	-	-	0	0	0	
4E	78	**INT_CTRL**	-	-	-	-	SLID (R only)	SACOK (R only)	PLID	PACOK	R/W
		Default	-	-	-	-	R	R	1	1	
4F	79	**INT1_EN**	OC	LID	ACOK	GPIO	VBAT	-	RTC	OT	R/W
		Default	0	0	0	0	0	0	0	0	
50	80	**INT2_EN**	-	-	-	-	-	PEN	ONKEY_LP	ONKEY	R/W
		Default	-	-	-	-	-	0	1	1	

Registers 76 to 80 configure the interrupt behavior of the PMIC and whether or not specific events will generate an interrupt to the microprocessor.

After reading the interrupt, each event can be individually cleared by writing a "1" to the corresponding bit. All enable bits are set to "0" by default, except bits ONKEY and ONKEY_LP in INT2_EN register. All interrupt events can be enabled/disabled by setting the corresponding bits to "0" in the INT1_EN and INT2_EN registers. Setting the EN bit to "1" generates an interrupt on the INTB pin when an event occurs.

Register bits description

OT	Over-temperature event. If the die temperature (MON_TEMP) is above SET_HTEMP (see **Table 48**) the OT bit of register INT0 is set.
RTC	RTC alarm. If the RTC alarm is enabled and an alarm occurred, the RTC bit of register INT0 is set.
VBAT	VBAT over-or-under voltage event. If the VBAT voltage (MON_VBAT) is above SET_VBATH or below VBATL (see **Table 48**) the VBAT bit of register INT0 is set.
GPIO	GPIO event. If a GPIO pin changed status, the GPIO bit of register INT0 is set. See **Table 49** how to configure GPIO events.
ACOK	ACOK event (power on default: "1"). If PACOK ="1", and the ACOK pin changes from low to high, then the ACOK bit of register INT0 is set. If PACOK="0", and the ACOK pin changes from high to low, then the ACOK bit of register INT0 is set.
LID	LID event (power on default: "0"). If PLID="1", and the LID pin changes from low to high, then the LID bit of register INT0 is set. If PLID="0", and the LID pin changes from high to low, then the LID bit of register INT0 is set.
OC	Over-current event. If any of the regulators DCD0,1,2,3, or DCD0a tripped the over-current threshold set in registers MON_DCDx (see **Table 48**), the OC bit of register INT0 is set.
ONKEY	ONKEY event (power on default: "0"). If the ONKEY pin has been pressed for > 20ms, the ONKEY bit of register INT1 is set.
ONKEY_LP	ONKEY long press event. If the ONKEY has been pressed for > 2s, the ONKEY_LP bit of register INT1 is set. If the ONKEY_LP interrupt is not cleared within 2s, the PMIC resets (RSTB = "0"), will shutdown all regulators and transition into OFF state.
PEN	PEN event. If PENx is used to initiate state transitions between ON and SLEEP state, the PEN bit of register INT1 is set.
PACOK	Polarity of ACOK event: If bit is set to "1" – active high transition, an event is generated when pin state changes from "0" to "1". If bit is set to "0" – active low transition, an event is generated when pin state changes from "1" to "0". PACOK default : "1".

PLID	Polarity of LID event: If bit is set to “1” – active high transition, an event is generated when pin state changes from “0” to “1”. If bit is set to “0” – active low transition, an event is generated when pin state changes from “1” to “0”. PLID default: INT_CTRL register [PLID bit] = “1” *Note: PLID default is opposite in INWAKE1 register [PLID bit]: (INWAKE1 register [PLID bit] = “0”)*
SACOK SLID	Real time status of ACOK and LID pin.
INT1_EN INT2_EN Registers	All interrupt events can be masked by setting the corresponding bits in the INT1_EN and INT2_EN registers to “0” Setting the EN bit to “1” enables an interrupt when an event occurs. Example: INT1_EN[RTC]=”1”, INT2_EN[ONKEY]=”0”: The real time clock (RTC) can generate an interrupt. The ONKEY input will never generate an interrupt.

Voltage, Current, and Temperature Monitoring

Table 48– Monitoring configuration registers

Address		Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	R/W
51	81	MON_TEMP	DIE_TEMP[7:0]								R
		Default	0	0	0	0	0	0	0	0	
52	82	MON_VSYS	VSYS[7:0]								R
		Default	0	0	0	0	0	0	0	0	
53	83	MON_VBAT	VBAT[7:0]								R
		Default	0	0	0	0	0	0	0	0	
54	84	MON_DCD0	IDCDCD0[7:0]								R
		Default	0	0	0	0	0	0	0	0	
55	85	MON_DCD1	IDCDCD1[7:0]								R
		Default	0	0	0	0	0	0	0	0	
56	86	MON_DCD2	IDCDCD2[7:0]								R
		Default	0	0	0	0	0	0	0	0	
57	87	MON_DCD3	IDCDCD3[7:0]								R
		Default	0	0	0	0	0	0	0	0	
58	88	MON_DCD0a	IDCDCD0a[7:0]								R
		Default	0	0	0	0	0	0	0	0	
59	89	SET_VBATL	SET_VBATL[7:0]								R/W
		Default	0	0	0	0	0	0	0	0	
5A	90	SET_VBATH	SET_VBATH[7:0]								R/W
		Default	1	1	1	1	1	1	1	1	
5B	91	SET_HTEMP	SET_HTEMP[7:0]								R/W
		Default	1	1	1	1	1	1	1	1	
5C	92	SET_DCD0	SET_IDCDCD0[7:0]								R/W
		Default	1	1	1	1	1	1	1	1	
5D	93	SET_DCD1	SET_IDCDCD1[7:0]								R/W
		Default	`	1	1	1	1	1	1	1	

Registers 81 to 93 are settings for voltage, current, and temperature limits. Once those limits are exceeded, an interrupt can be generated.

Register bits description

DIE_TEMP	Die temperature. T_J [in °C] = (1.1916 * DIE_TEMP[7:0]) – 136.77.
VSYS	VSYS voltage: V_{SYS} [in V] = VSYS[7:0] * 1.2V/256 * 14/3. The range of V_{SYS}(V) measureable is 0 to 5.58V
VBAT	Battery voltage. V_{BAT} [in V] = VBAT[7:0] * 1.2V/256 * 11/3 The range of V_{BAT}(V) measurable is 0 to 4.38V
IDCD0 … IDCD3 IDCD0a	DCDx current level: I_{DCDx} [in A] = (IDCDx[7:0]*1.2/256 – 0.29 – (270K/2M)*(VOUT/VIN)) /.08 The range of IDCDx(A) measurable is -5.7A to 10.9A
SET_VBATL … SET_VBATH	VBAT low voltage threshold setting, generates event if voltage is below. SET_VBATL[7:0] = lower 7 Binary bits of the equation: V_{SYS} [in V] * 256/1.2 * 3/11 SET_VBATH[7:0]: VBAT high voltage threshold setting, generates event if voltage is above. SET_VBATH[7:0] = upper 7 Binary bits of the equation: V_{SYS} [in V] * 256/1.2 * 3/11 SET_VBATL and VBATH covers the whole range of allowed V_{SYS}
SET_HTEMP	Set die temperature threshold, generates event if temperature is above. SET_HTEMP[7:0] = (T_J [in °C]+154.55°C) * 143/180
SET_IDCDO SET_IDCD1	**IMPORTANT: Don't change default setting for either SET_IDCD0 or SET_IDCD1**

GPIO Configuration and Status

Table 49– GPIO, CK32, and RSTB configuration registers

Address		Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	R/W
5E	94	**GPIO0C**	-	-	GPIO0_INT	GPIO0_POL	GPIO0_OD	GPIO0_VIO	GPIO0_IO	GPIO0_TDB	R/W
			-	-	0	1	0	0	0	0	
5F	95	**GPIO1C**	-	-	GPIO1_INT	GPIO1_POL	GPIO1_OD	GPIO1_VIO	GPIO1_IO	GPIO1_TDB	R/W
			-	-	0	1	0	0	0	0	
60	96	**GPIO2C**	-	-	GPIO2_INT	GPIO2_POL	GPIO2_OD	GPIO2_VIO	GPIO2_IO	GPIO2_TDB	R/W
			-	-	0	1	0	0	0	0	
61	97	**GPIO3C**	-	-	GPIO3_INT	GPIO3_POL	GPIO3_OD	GPIO3_VIO	GPIO3_IO	GPIO3_TDB	R/W
			-	-	0	1	0	0	0	0	
62	98	**GPIO4C**	-	-	GPIO4_INT	GPIO4_POL	GPIO4_OD	GPIO4_VIO	GPIO4_IO	GPIO4_TDB	R/W
			-	-	0	1	0	0	0	0	
63	99	**GPIO5C**	-	-	GPIO5_INT	GPIO5_POL	GPIO5_OD	GPIO5_VIO	GPIO5_IO	GPIO5_TDB	R/W
			-	-	0	1	0	0	0	0	
64	100	**GPIO6C**	-	-	GPIO6_INT	GPIO6_POL	GPIO6_OD	GPIO6_VIO	GPIO6_IO	GPIO6_TDB	R/W
			-	-	0	1	0	0	0	0	
65	101	**GPIO7C**	-	-	GPIO7_INT	GPIO7_POL	GPIO7_OD	GPIO7_VIO	GPIO7_IO	GPIO7_TDB	R/W
			-	-	0	1	0	0	0	0	
66	102	**GPIO_TDB**	-	-	-	-	-	-	GPIO_TDB[1:0]		R/W
			-	-	-	-	-	-	0	0	
67	103	**GPIO**	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0	R/W
			0	0	0	0	0	0	0	0	
68	104	**CK32**	-	-	-	-	-	-	CK32_OD	CK32_VIO	R/W
			-	-	-	-	-	-	0	0	
69	105	**RESETB**	-	-	-	-	-	-	-	RSTB_OD	R/W
			-	-	-	-	-	-	-	0	

Registers 94 to 105 configure the GPIO ports.

Each GPIO can be individually configured as input or output. If configured as an input, one can use the input directly or with a debounce filter. The debounce filter time is the same for all inputs and can be selected between 100µs and 30ms.

If GPIO[0:2] pin is configured as a sequencing output, the GPIOx is set to an output automatically.

Register bits description

GPIO0_TDB … GPIO7_TDB	GPIO global de-bounce time enable (120µs, 1ms, 15ms, 30ms). GPIOx_TDB = "0": GPIO input is used without debounce filter, GPIOx_TDB = "1": GPIO input is used with debounce filter selected in GPIO_TDB register.
GPIO0_IO … GPIO7_IO	GPIOx_IO = "0": GPIOx is input GPIOx_IO = "1": GPIO is output
GPIO0_VIO … GPIO7_VIO	GPIOx_VIO = "0": Use VIO0 as supply rail for GPIOx GPIOx_VIO = "1": Use VIO1 as supply rail for GPIOx
GPIO0_OD … GPIO7_OD	GPIOx_OD = "0": Enable push pull output GPIOx_OD = "1": Enable open-drain output
GPIO0_POL … GPIO7_POL	GPIOx_POL = "0": GPIOx is low level sensitive GPIOx_POL = "1": GPIOx is high level sensitive. If the GPIO is configured to generate an interrupt, the interrupt will only be generated on a low to high transition

	when GPIOx_POL="1", and only on a high to low transition when GPIOx_POL="0"
GPIO0_INT … GPIO7_INT	GPIOx_INT = "0": No interrupt will be generated when GPIOx toggles GPIOx_INT = "1": Interrupt will be generated in register INTO, GPIO bit (see **Table 47**) when GPIOx toggles state
GPIO_TDB	GPIO global de-bounce time (120µs, 1ms, 15ms, 30ms). Values: "00" = 120µs, "01" = 1ms, "10" = 15ms, "11" = 30ms
GPIO0 … GPIO7	Read returns input value of GPIO after de-bounce time (GPIO configured as input) Write sets GPIO value (if GPIO is configured as an output)
CK32_VIO	CK32_VIO = "0": Use VIO0 as supply rail for CK32 CK32_VIO = "1": Use VIO1 as supply rail for CK32
CK32_OD	GP32_OD = "0": Enable push pull output GP32_OD = "1": Enable open-drain output
RSTB_OD	RSTB_OD = "0" RSTB output is a push-pull output RSTB_OD = "1" RSTB output is an open-drain output

ADC Inputs Configuration

Table 50– ADC configuration registers

Address		Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	R/W
6A	106	**ADC_CTRL0**	IDCD2	IDCD1	IDCD0	VSYS	VBAT	DIETEMP	ANLG1	ANLG0	R/W
			0	0	0	0	0	0	0	0	
6B	107	**ADC_CTRL1**	-	-	-	-	-	READ_SEL	IDCD0a	IDCD3	R/W
			-	-	-	-	-	0	0	0	
6C	108	**ADC_CTRL2**	-	-	ENBIAS	ENABLE	ADC_TS[2:0]			MODE	R/W
			-	-	1	0	0	0	0	0	
6D	109	**ADC_CTRL3**	-	-	-	-	-	-	THERM_POL	ANLG1_CFG	R/W
			-	-	-	-	-	-	1	0	
6E	110	**ADC_INL**	ADC0[7:0]								R
			-	-	-	-	-	-	-	-	
6F	111	**ADC_INH**	-	-	-	-	-	-	ADC0[9:8]		R
			-	-	-	-	-	-	-	-	

Registers 106 to 111 configure the ADC operation.

The user can select the sources, which need to be measured as well as the repetition time of the measurements.

Register bits description

ANLG0	Enable analog input ANLG0 measurement. ANLG0 is stored in ADC_INH and ADC_INL
ANLG1	Enable analog input ANLG1 measurement. ANLG1 is stored in ADC_INH and ADC_INL
DIETEMP	Enable die temperature measurement. Result is stored in MON_TEMP, see **Table 48**
VBAT	Enable VBAT measurement. Result is stored in MON_VBAT, see **Table 48**
VSYS	Enable VSYS measurement. Result is stored in MON_VSYS, see **Table 48**
IDCD0 … IDCD3 IDCD0a	Enable DCDx output current measurement. Result is stored in MON_DCDx Enable DCD0a output current measurement. Result is stored in MON_DCD0a, see **Table 48**
READ_SEL	READ_SEL="0": Read ANLG0 READ_SEL="1": Read ANLG1
MODE	MODE = "0": Run ADC only once MODE = "1": Run ADC continuously.
ADC_TS	ADC_TS configures the repetition rate of the ADC measurements. All selected sources will be measured one by one. After the last source has been measured, the next round of measurements commence after a delay defined in ADC_TC.

ADC_TS	000	Continuous
	001	1ms
	010	2ms
	011	4ms
	100	8ms
	101	16ms
	110	32ms
	111	64ms

ENABLE	Enables the ADC. If the MODE bit is set to "0", the ENABLE bit is automatically reset after one round of measurements.
ENBIAS	Enables ADC clock. If "0" then ADC is disabled, and the quiescent current is reduced by ~60µA. If "1" then ADC is enabled. Default is "1"
ANLG1_CFG	ANLG1_CFG = "0": ANLG1 input is used as analog input, ANLG1_CFG = "1": ANLG1 input is used as a THERMAL flag input from microprocessor and shuts down the PMIC immediately if asserted.

THERM_POL	Polarity of the THERMAL input (ANLG1_CFG="1") POL = "0": Low active, POL = "1": High active.
ADC0	ADC output for ANLG0 and ANLG1, 10bit width.

ONKEY and Power Event Pins Configuration

Table 51– ONKEY, PEN1, and PEN2 configuration registers

Address		Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	R/W
70	112	**INPCFG0**	-	-	-	ENPINWAKE	PENSLEEP	PONKEY	PPEN1	PPEN0	R/W
		Default	-	-	-	1	0	1	OTP - One Time Prog		
71	113	**INPCFG1**	-	-	-	-	-	-	ONKYDLY[1:0]		
		Default	-	-	-	-	-	-	OTP - One Time Prog		
72	114	**INPCFG2**	ONKYTIM[7:0]								R

Register bits description

PPEN0	PPEN0 = “0”: Low active PEN0. The PMIC reacts to PEN0 high to low transition only PPEN0 = “1”: High active PEN0 The PMIC reacts to PEN0 low to high transition only
PPEN1	PPEN1 = “0”: Low active PEN1 PPEN1 = “1”: High active PEN1
PONKEY	PONKEY = ”0”: Low active ONKEY PONKEY = “1”: High active ONKEY
PENSLEEP	PENSLEEP = “0”: Use PEN0 for SLEEP mode entry and exit PENSLEEP = “1”: Use PEN1 for SLEEP mode entry and exit
EPINWAKE	EPINWAKE = “0” disables state transition from ON to SLEEP state initiated by PENx EPINWAKE = “1” enables the function. EPINWAKE is set to “1” by default *To enable PENx controlled ON/SLEEP state transition:* *First set EPINWAKE=”1”, then use PENSLEEP to choose either PEN0 (“0”) or PEN1 (“1”) as the control.*
ONKYDLY	ONKEY Long Press delay (“00”=2s, “01”=4s, “10”=6s, “11”=8s)
ONKYTIM	ONKEY long press timer countdown. Time = ONKYTIM[7:0]*250ms. Example: If ONKYTIM is programmed to 6 then the countdown time is 6*250ms = 1.5s

Wake-up from Sleep State, Reset, Turn-off of the Device

Table 52– Wake-up from SLEEP state and PMIC reset configuration registers

Address		Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	R/W
73	115	**MODE**	-	-	-	RTCWAKE	LIDWAKE	ACOKWAKE	TURNOFF	Z0	R/W
			-	-	-	0	0	0	0	0	
74	116	**RESET**	-	-	-	-	-	-	-	RESET	R/W
			-	-	-	-	-	-	-	0	

Register bits description

Z0	Must remain 0 at all times
TURNOFF	If the TURNOFF bit is set to “1”, then: the PMIC pulls RSTB low and shuts down all rails and transitions into OFF state
ACOKWAKE	If the ACOKWAKE bit is set to “1”, the PMIC wakes-up from SLEEP state when ACOK toggles either high or low depending on the PACOK bit (see **Table 47**). ACOK is high active by default.
LIDWAKE	If the LIDWAKE bit is set to “1”, the PMIC wakes-up from SLEEP state when LID toggles either high or low depending on the PLID bit (see **Table 54**). LID is low active by default.
RTCWAKE	If the RTCWAKE bit is set to “1”, then: the PMIC wakes-up from SLEEP state when a RTC alarm is set and the alarm triggers
RESET	If RESET is set to “1”then the PMIC will shutdown, the RESET bit will clear to “0”, then it will automatically start up again.

VSYS UVLO Configuration

Table 53– VSYS UVLO configuration registers

Address		Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	R/W
75	117	**UVLO**	-	-	-	-	-	UVLO[2:0]			R/W
		Default	-	-	-	-	-	Factory Trimmed			
76	118	**UVLOHYS**	-	-	-	-	-	-	UVLOHYS[1:0]		R/W
		Default	-	-	-	-	-	-	0	0	

Register bits description

UVLO

Sets UVLO threshold. See **Table 4** for details.

UVLO	Threshold (V)
000	2.8V
001	2.9V
010	3.0V
011	3.1V
100	3.2V
101	3.3V
110	3.4V
111	3.5V

UVLOHYS

Sets hysteresis of UVLO threshold. See **Table 4** for details.

UVLOHYS	Hysteresis (V)
00	0mV
01	100mV
10	200mV
11	300mV

Wake-up source and ACOK, LID

Table 54– Wake-up source and ACOK, LID configuration register

Address		Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	R/W
77	119	**INWAKE1**	-	-	-	-	DISRESLID	PLID	LID	ACOK	R/W
		Default	-	-	-	-	0	0	1	1	
78	120	**INWAKE2**	-	-	-	-	THERMAL	ONKEY	LID_STAT	ACOK_STAT	RW1C *Read Status* *Write to Clear*
		Default	-	-	-	-	R	R	R	R	

Register bits description

ACOK	ACOK bit set to "1": the PMIC wakes-up from OFF state when ACOK toggles from low to high (high active). The polarity is active high by default and can be changed to active low by through the PACOK bit (see **Table 47**)
LID	LID bit set to "1": the PMIC wakes-up from OFF state when LID toggles from high to low (low active). The polarity is active low by default and can be changed to active high by through the PLID bit
PLID	Polarity of LID pin. PLID = "0" sets LID to high active PLID = "1" sets LID to low active *(Note: There is another PLID bit in the INT_CTRL register that controls the polarity of the PLID bit for the purpose of interrupts only. PLID of register INT_CTRL (address 78) is opposite polarity of PLID of the INWAKE1 register (="0"): INT_CTRL[PLID]="1"=LID is high active)*
DISRESLID	RESERVED
ACOK_STAT	This status bit is set to "1" when an ACOK event woke-up the PMIC from OFF state. It can be cleared by writing a "1" to the bit
LID_STAT	This status bit is set to "1" when a LID event wakes-up the PMIC from OFF state. It can be cleared by writing a "1" to the bit
ONKEY	This status bit is set to "1" when an ONKEY event wakes-up the PMIC from OFF state. It can be cleared by writing a "1" to the bit
THERMAL	This status bit is set to "1" when thermal event (internal or external via THERMAL bit) shuts-down the PMIC. It can be cleared by writing a "1" to the bit

Power-good Pin (PG0)

Table 55– Power-good pin (PG0) configuration register

Address		Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	R/W
79	121	**PGCFG**	-	PWRGOOD0	OVRCUR0	OVRCUR	OTEMP	GPIO	LID	ACOK	R/W
		Default		1	1	0	0	0	0	0	

Register bits description

ACOK	If bit is set to “1”, PG0 flags ACOK events depending on the setting of PACOK. PACOK=”0”: PG0 goes low when ACOK goes low PACOK=”1”: PG0 goes low when ACOK goes high
LID	If bit is set to “1”, PG0 flags LID events depending on the setting of PLID bit of register INT_CNTRL (register 78) PLID=”0”: PG0 goes low when LID goes low PLID=”1”: PG0 goes low when LID goes high
GPIO	If bit is set to “1”, PG0 flags GPIOx events If the GPIOx_INT = “1” and GPIOx_POL = “0”: PG0 flags a high to low transition by transitioning to logic low If the GPIOx_INT = “1” and GPIOx_POL = “1”: PG0 flags a low to high transition by transitioning to logic low
OTEMP	If bit is set to “1”, PG0 flags over-temperature events. The temperature threshold can be set in register MON_TEMP (see **Table 48**)
OVRCUR	If bit is set to “1”, PG0 flags DCD1, DCD2, and DCD3 over-current events by going low.
OVRCUR0	If bit is set to “1”, PG0 flags DCD0 over-current events by going low.
PWRGOOD0	PWRGOOD0 = “0”: PG0 is simply a power good indicator. Allows PG0 pin to transition to logic high after all activated rails charge to their programmed voltages PWRGOOD0 = “1”: PG0 will remain logic low upon a power up, even after the regulators are active with the correct voltages. After ~100µs the PG0 becomes a event flag. At that time PWRGOOD0 no longer has any control over PG0

Charger and RTC crystal capacitor adjustment

Table 56 – RTC crystal capacitor adjustment and charger configuration registers

Address		Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	R/W
7A	122	**CADJ**	-	-	-	-	CINT	CADJ[2:0]			R/W
		Default					0	0	0	0	

CINT and CADJ can be set to fine-tune the crystal oscillator. Normally there are no changes necessary if a crystal with 12.5pF load capacitance is used.

Register bits description

CADJ	Adds 1pF/LSB load capacitance per pin (XTAL0, XTAL1) to ground. Default capacitance is 5pF (CADJ[2:0] = “101”)
CINT	If CINT is set to “1”, it adds a 14.8pF internal capacitance per pin (XTAL0, XTAL1) to ground
VBAK_RCHG	VBAK_RCHG adjusts the internal series resistance. See **Table 15** for details
VBAK_VCHG	VBAK_VCHG adjust the charger output voltage. The setting “00” turns-of the charger. See **Table 15** for all available settings
CHG_ON	Status bit that is set to “1” when the charger is active and charging

ILIM Increase Time and DCD0,1 VOUT Range

Table 57– Increase time of higher current limit for regulators, Determine DCD0,1 VOUT range

Address		Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	R/W
7C	124	**RESERVED**	-	-	-	-	-	-	-	-	R/W
7D	125	**ILIM**	-	-	-	-	-	ILIM100US	-	-	R/W
		Default	-	-	-	-	-	0	-	-	
7E	126	**DCD_RANGE**	-	-	DCD1_LS	DCD0_LS	-	-	-	-	R/W
		Default	-	-	1	1	-	-	-	-	
Address		**Name**	**Bit[7]**	**Bit[6]**	**Bit[5]**	**Bit[4]**	**Bit[3]**	**Bit[2]**	**Bit[1]**	**Bit[0]**	**R/W**

Registers 125 controls the current limits of DCD0 and DCD1, and register 126 controls the range of DCD0 and DCD1

Register bits description

ILIM100US	"Increased current limit " duration is increased to 100µs (vs. default 10µs). Note: "Increased current limit" = Current limit is temporarily increased by ~15%. This increase is used for faster response to large current load steps.
DCD0_LS	If ="0" then DCD0_VOUT range is 0.5375V to 1.325V If ="1" then DCD0_VOUT range is 0.7625V to 1.55V Default value ="1". See **Table 41**
DCD1_LS	If ="0" then DCD1_VOUT range is 0.5375V to 1.325V If ="1" then DCD1_VOUT range is 0.7625V to 1.55V Default value ="1". See **Table 41**

Configuration Registers for Dynamic Power System

Table 58– DCD0 split, LDOTR select, Dynamic Power Scaling control

Address		Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	R/W
7F	127	CONFIG0	-	-	-	-	-	-	LDOTR_SEL	DCD0_SPL	R/W
		Default	-	-	-	-	-	-	0	1	
80	128	CONFIG1	-	-	-	DIS_DISCHG	-	OFF_DLY_SEL[1:0]		USE_DPS	R/W
		Default	-	-	-	0	-	0	0	1	
81	129	CONFIG2	-	-	OVR	GM4	-	-	-	-	R/W
		Default	-	-	0	0	-	-	-	-	

Registers 127 to 129 The main job of these registers is to configure the control of the additional, external current sourcing switching regulators, which add extra phases and current sourcing ability to DCD1.

DCD0_SPO	Split DCD0. If set to “0” then DCD0 is a single 2-phase 10A switching voltage regulator If set to “1” then DCD0 is split into two 1-phase 5A switching voltage regulators – DCD0a and DCD0b
LDOTR_SEL	Select source for LDOTR to track LDOTR_SEL = “0”: Track DCD1 LDOTR_SEL = “1”: Track DCD0
USE_DPS	Enable the “Distributed Power System” USE_DPS = “0”: Disable control of IDTP9167 type external ICs USE_DPS = “1”: Enable DCD1 to control up to 4 IDTP9167 type external ICs through the DIF and DIO communication lines. Each IDTP9167 adds another phase of up to 3.5A of additional DC current to be supplied to the DCD1 output voltage. *Note: In order to set USE_DPS to “1”, OVR (overwrite) must also be set to “1”.* *Note: Insure that DCD1 is off before writing a “1” to USE_DPS.*
OFF_DLY_SEL	Phase shedding timing When the load decreases the external phases need to be shed. The delay between one phase shedding and the next is programmed through these two bits: 00 10µs 01 20µs 10 60µs 11 120µs
DIS_DISCHG	Disable IDTP9167 Discharge Pulse. When USE_DPS=”1” and DCD1 is suddenly turned off the external IDTP9157s will administer discharge pulses for about 1ms. The pulse duty cycle is controlled to produce an average discharge current of approximately 300mA. This helps discharge the large output capacitance that one normally has when using the Distributed Power System (DPU) and external IDTP9157s. DIS_DISCHG = “0”: Disable discharge pulses DIS_DISCHG = “1”:Enable discharge pulses
GM4	Fractional Gain Control GM4 = “0”: Full GM4 gain for maximum bandwidth GM4 = “1”: Gain = GM/4 for more stability
OVR	Over Write Safety Control This bit must be “1” in order to write any other bit in CONFIGx register. OVR = “0”: Cannot program any other bits in CONFIGx OVR = “1”: Can program any bit in CONFIGx

Configuration Registers for Dynamic Power System

Table 59– DCD0 split, LDOTR select, Dynamic Power Scaling control

Address		Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	R/W
82	130	**PMSTATUS**	-	-	-	-	-	-	-	-	R
83	131	**DEVSTATUS**	-	-	-	-	-	-	-	-	R

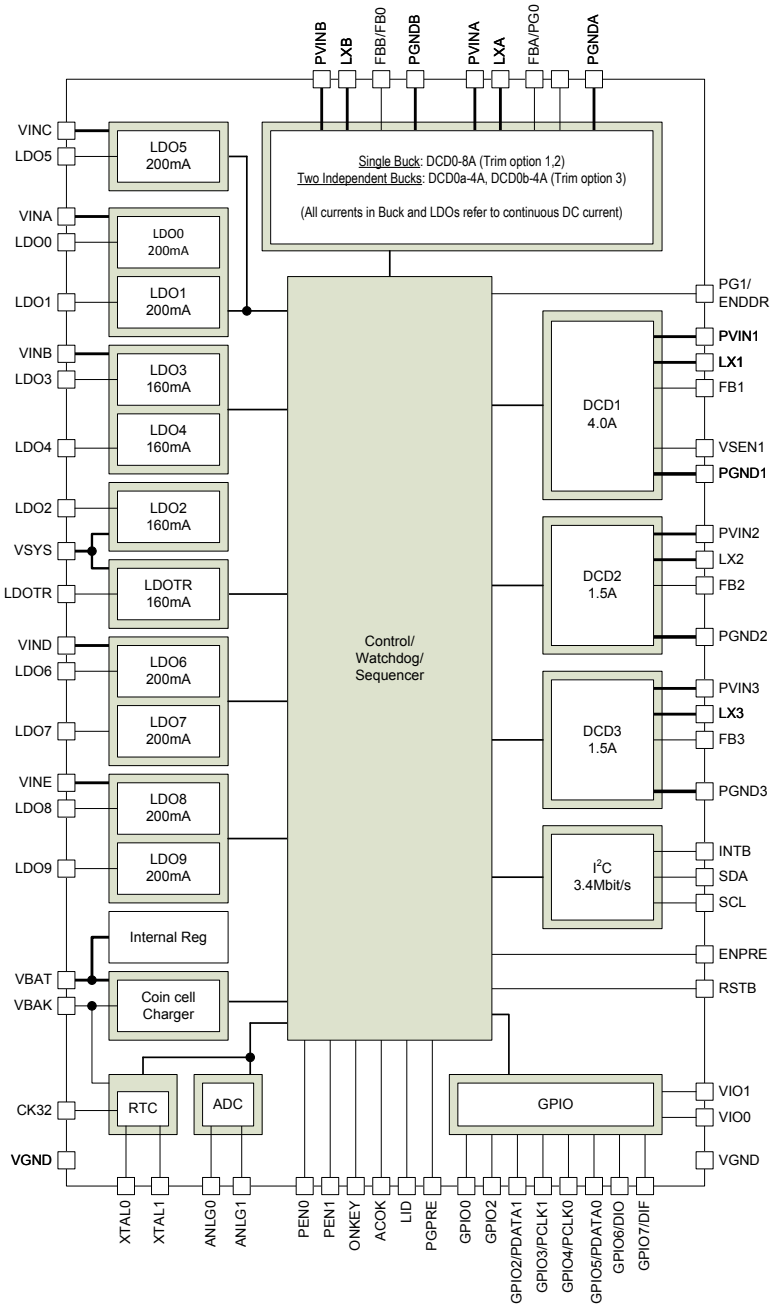
PMSTATUS	Phase Mode Status - Reports how many IDTP9167s are present in DPS mode

Bit Value	Number of IDTP9167s present
0000	0
0001	1
0011	2
0111	3
1111	4

DEVSTATUS	Development Status “2”: Normal / On mode “20”: Sleep mode

THEORY OF OPERATION

Block Diagram



43 – Simplified Block Diagram

OVERVIEW

The IDTP9165 is a high efficiency power management IC with four switching regulators and eleven low drop out regulators. It is designed to supply power to products such as laptop computers, tablet PCs, and other portable devices. It has push button wakeup, power up sequencing, I2C controlled programming, built in ADC, controls for enabling external power supplies, as well as other features.

Power Up

Power up considerations

The IDTP9165 is powered on by pulling ONKEY or LID momentarily low after V_{SYS} is applied.

There is a delay from ONKEY going low to the IDTP9165 turning on (RSTB going low) of approximately 30ms.

The IDTP9165 is powered off by pulling pin ONKEY low for approximately four seconds. This time is programmable from 0 to 64 seconds (see **Table 51**).

ACOK Power up

After proper programming (permanently programming INWAKE register, ACOK bit to one), one may have automatic power up upon detection of V_{IN} through the ACOK pin. However, there is a 600 ms blanking time that must be “waited out” before the IDTP9165 will respond to a high voltage on ACOK. This means a large filter (R=200kΩ, C=10µF) is required to keep ACOK below the logic high threshold for that 600 ms after the V_{IN} is initially applied to the PMIC. In order to bypass this large filter for the next power down, once powered up use a GPIO to drive a 2N7002 to pull ACOK to GND. This will prepare it to detect the next power cycle

Sequence Programming

Only the ON-OFF sequencing can be hard coded; therefore the desired behavior for SLEEP state entrance and exit needs to be configured before going into SLEEP state the first time. By default the ON-SLEEP-ON transition is identical to the ON-OFF-ON transition.

In order to have a regulator controlled by these sequencing registers the x_OSEQ must first be set to “1”. After that the order in which the regulator comes up is controlled by the x_GRP_ON bits. Group 0 comes up first, followed by group 1, group 2, …, and lastly group 7. The order is reversed for turning off: group 7 first and group 0 last (see **Table 45**).

The delay time between groups turning-on or off can be set individually from 1ms to 10ms. The DLY_GRP1 setting defines the delay time between group 0 and group 1, DLY_GRP2 sets the delay time between group 1 and group 2, etc.

For example, if one wants DCD2 to come up first, wait 1ms, then DCD3, wait 4ms,then DCD1 and LDO0 together the one must program the register thus:

Include in sequencing:	DCD2_OSEQ=DCD3_OSEQ=DCD1_OSEQ=LDO0_OSEQ=1
First group to turn on:	DCD2_GRP_ON=0
Second group to turn on:	DCD3_GRP_ON=1
Third group to turn on:	DCD1_GRP_ON=LDO0_GRP_ON=1
Turn on the delays between groups:	DLY_ON0=DLY_ON1=1
Delay between DCD2 and DCD3: 1ms:	DLY_GRP0=0
Delay between DCD3 and DCD1,LDO0: 4ms:	DLY_GRP1=2

Sequencing vs. PENx control

Three of the GPIOs can also be used as enable signals for external regulators and can be part of a sequence. If configured as an enable signal the GPIO is automatically configured as an output.

If a regulator is part of a sequence and at the same time assigned to an enable pin (PEN0 or PEN1), the regulator follows the programmed sequence until RSTB is asserted

"1". Once RSTB is asserted "1" the PENx pin controls the regulator.

ENPRE, PGPRE

There is a regulator before the IDTP9165 that supplies it with its input voltage. The battery voltage is the input to this "pre-regulator". A logic high voltage on the PGPRE pin from the pre-regulator signals the IDTP9165 to power up.

When the IDTP9165 goes into the OFF state it will signal the pre-regulator through a logic low on the ENPRE pin. This signals the pre-regulator to stop supplying the IDTP9165's input voltage. Note that the battery voltage must be supplied to both the pre-regulator and the IDTP9165 for this to work. Otherwise once the pre-regulator shuts off the IDTP9165 is completely off and it has no way to signal the pre-regulator to begin supplying the input voltage to the IDTP9165 again

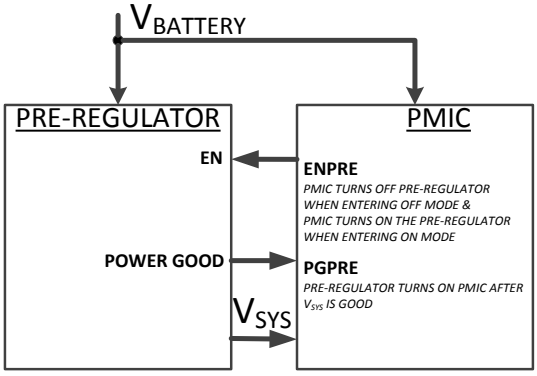


Figure 44 – ENPRE PGPRE block diagram

PG0 Pin Function

If PWRGOOD0 (see **Table 55**) is set to "1" then the PG0 will remain low upon a power up, even after the regulators are up with the correct voltages. After ~100µs the PG0 becomes a event flag. At that time PWRGOOD0 no longer has any control over PG0

ADC Considerations

The IDTP9165 includes an analog to digital converter (ADC). The ADC can measure die temperature, input voltages, and buck currents. Furthermore, warning levels can be programmed to alert the user when a specific ADC value has been reached (see **Table 48**).

The pins that are connected to the ADC (ANLG0, ANLG1) have limited input range so attention should be given to the maximum applied voltage. Decoupling capacitors can be added to minimize noise.

Basic power states

IDTP9165 is controlled by a state machine. Enabling and disabling of power rails or any other device function depends on the power state of the device as well as enable signals or wake-up events. The device has three basic power states:

1. ON state definition: This is the fully powered state for the device. All rails are turned on (if programmed to be on). The I²C interface is active to control supply rails or other functions (ADC, GPIOs). See the – **Simplified State Diagram** for entrance and exit signals

2. SLEEP state definition: In the SLEEP state some rails are turned-off, whereas other rails are still on. The status of each rail in SLEEP state can be programmed by I²C. The I²C interface is active to control supply rails or other functions (ADC, GPIOs). See the **– Simplified State Diagram** for entrance and exit signals

3. OFF state definition: This is the powered off state of the device. All rails are turned off. The I²C interface is inactive. The RTC is operational if VBAT is present and above the UVLO threshold. RTC is also operational if VBAK is supplied by a coin cell battery or supercap and above the UVLO threshold. See the **– Simplified State Diagram** for entrance and exit signals

There are some intermediate states between ON, SLEEP, and OFF state, which control sequencing between the basic power states or simply add delays before or after state changes. For example, after leaving OFF state a 4ms delay is added to allow the pre-regulator to ramp-up to its nominal value before sequencing of regulators is starting.

State transitions are initiated by external events (e.g. ONKEY press, THERMAL flag), internal events, or I²C commands. Figure 45 shows the state diagram with events triggering a state change.

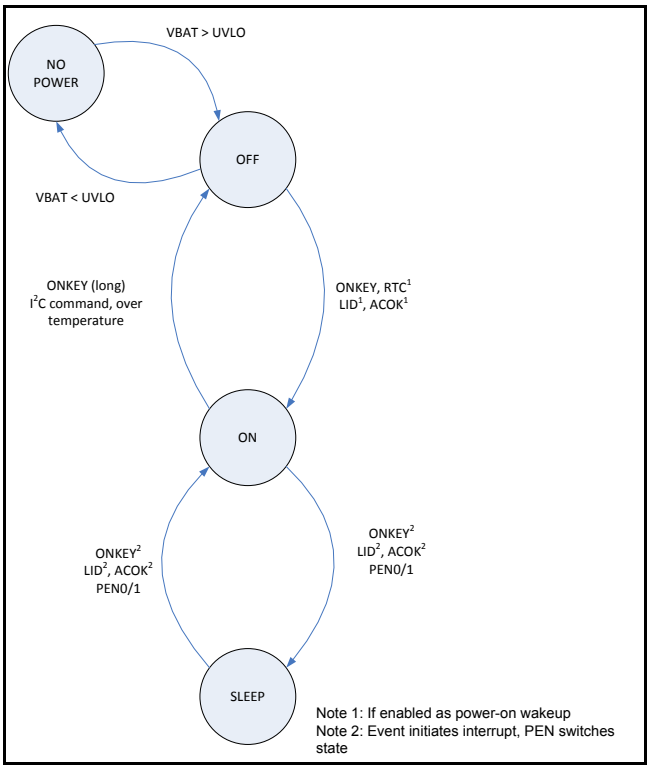


Figure 45 – Simplified State Diagram

Power Event Inputs

PEN0 and PEN1 are “Power Enable” pins 0 and 1. These can be programmed to turn on/off multiple voltage rails (e.g. DCD0, DCD1 + other LDOs). They are programmable to active high or low as desired. PEN0,1 are used to transition between the ON and SLEEP states. The voltage rails return to their programmed values when turned back on with the PENx pin. PEN0,1 pins are masked during reset.

The ONKEY pin transitions the system into and out of SLEEP or full OFF state. Its polarity is a programmable input (de-bounce time 20ms).The ONKEY pin will initiate power up sequencing after de-bounce time, if VBAT and VSYS voltage is above minimum. The ONKEY status register (see **Table 54**) indicates that power-on occurred.

An unmaskable forced power down occurs with ~4 sec power-on hold (ONKEY Long Press). This power-on hold time is programmable within a range of 2-8 seconds. Force power down cannot be disabled other than by clearing the interrupts. The status register is updated for this occurrence.

DCD0/DCD1 DVS Operation

The DCD0 and DCD1 regulators support Dynamic Voltage Scalling using the DVS register setting (DCD0_VDVS / DCD1_DVS) and the DVS enable bit (DCD0_DVS / DCD1_DVS) to adjust the output voltage of the DCD0 regulator. Once the regulator has: (1) been enabled, (2) the power-good signal has turned “1”, and (3) the enable bit for DCD0_DVS has been set to “1”, the regulator will change from the voltage set in register DCDx_VOUT to the DVS voltage set in register DCDx_VDVS. The output voltage ramp rate can be configured in register DCD0_SR.

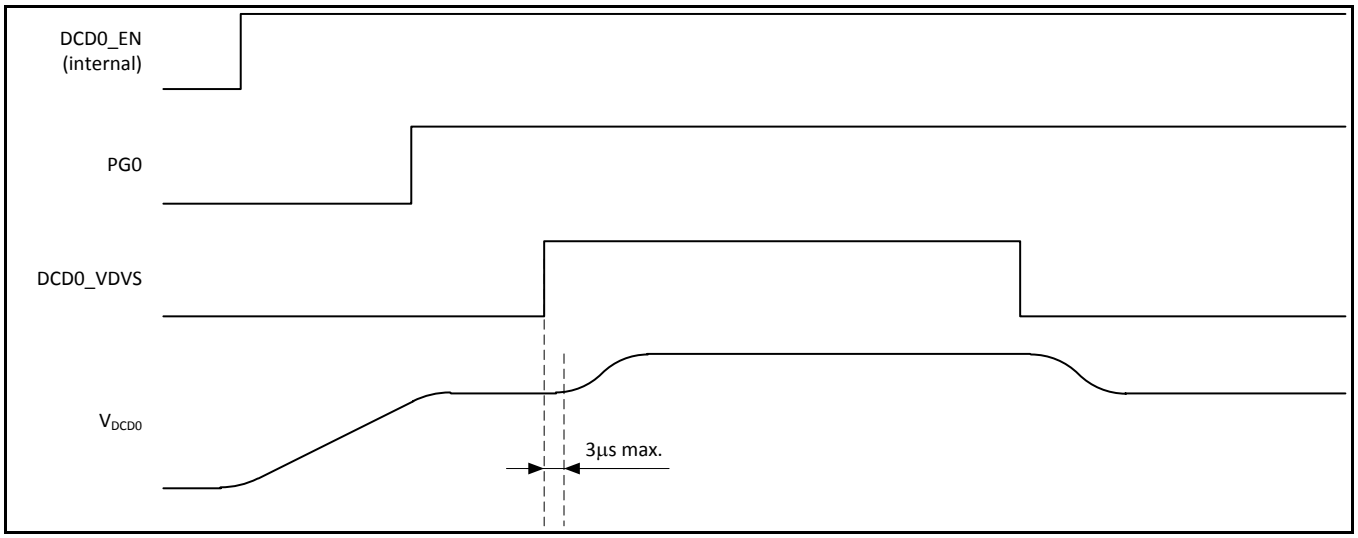


Figure 46. DVS Timing Diagram

DCD0/DCD1 PDVS (PWM DVS) Operation

There is a second way to control the output voltage of DCD0 and DCD1 during DVS, through use of the PWM-DVS interface. Set bits DCD0_PDVS/DCD1_PDVS to activate the PWM DVS function of DCD0 and DCD1 respectively (note: DCD2 and DCD3 are not PWM DVS capable). Through the use of the clock/data pin pairs shown below:

PIN	PWM-DVS FUNCTION	DCDx CONTROLLED
GPIO3	PCLK1	DCD1
GPIO2	PDATA1	
GPIO4	PCLK0	DCD0
GPIO5	PDATA0	

the PWM-DVS interface uses a clock and a data signal to encode up to 32 offset steps of 12.5mV each that are added to the DCD0/DCD1 base voltage. The DCD0/DCD1 base voltage is set in register DCD0_VOUT/ DCD1_VOUT, similar to the I²C controlled DVS operation described before.

The PWM clock can run from 3MHz to 33MHz. The PWM data is sampled during 32 consecutive clock periods. There is no explicit frame start or synchronization signal. A new frame starts with a rising edge of PWMDATA. The interface does not rely on a constant frequency or duty cycle as long as minimum clock low and high times are met. Figure 47 shows the data decoding of the PWM-DVS interface.

If the regulator is turned off during while the PWM-DVS is active, the DCD0_PDVS/DCD1_PDVS bit will be automatically cleared. This makes sure the regulator always starts-up with DVS disabled.

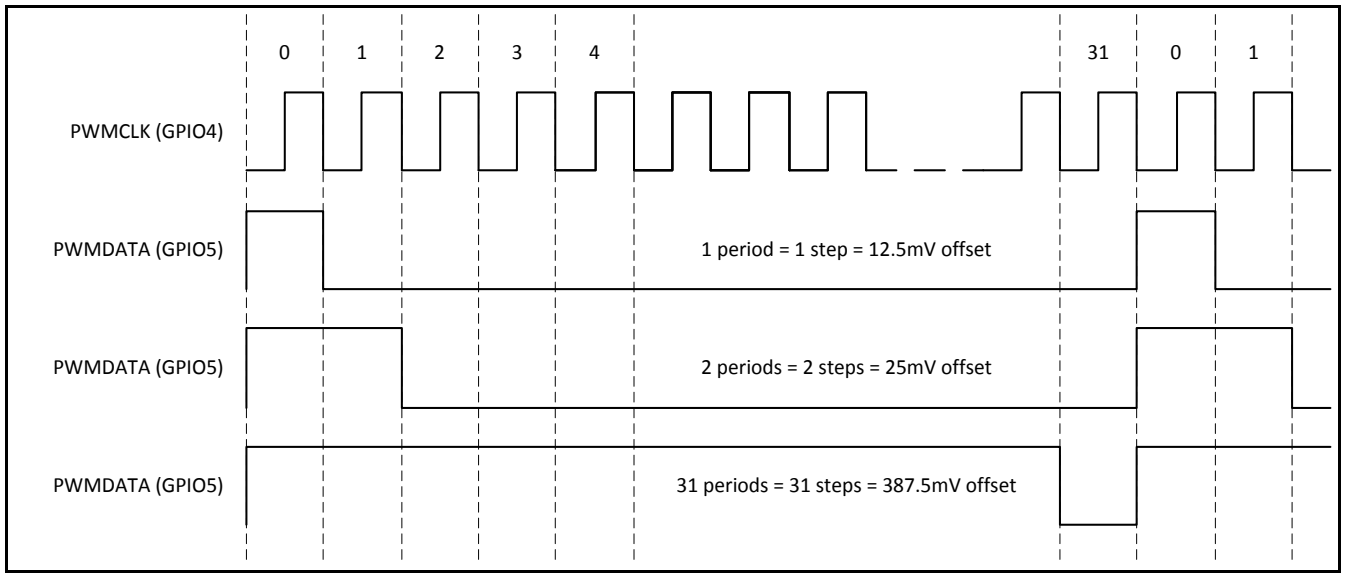


Figure 47 – PWM DVS Operation

DCD0 vs DCD0a & DCD0b

DCD0 can be configured as one 10A current switch mode current controlled regulator or two 5A switch mode regulators – DCD0a (associated with LXA pins), and DCD0b (associated with LXB pins). Set register CONFIG0, bit DCD0_SPL to “1” to split the DCD0 into DCD0a and DCD0b regulators. When this is done pin A38 changes from PG0 to the DCD0a feedback pin. It must be attached to the DCD0a output for proper functionality. In this case, pin A1 changes from a pin for enabling external voltage regulators (ENDDR) to the new PG0 (actually called PG1 to avoid confusion). With regards to DVS control: the DCD0 (unsplit, 2 phase) regulator is capable of both methods of DVS control. When split into DCD0a&b only DCD0a is DVS capable. DCD0b is not DVS capable. DCD0b functions in the same way as DCD1 - control is only through I^2C.

APPLICATIONS INFORMATION

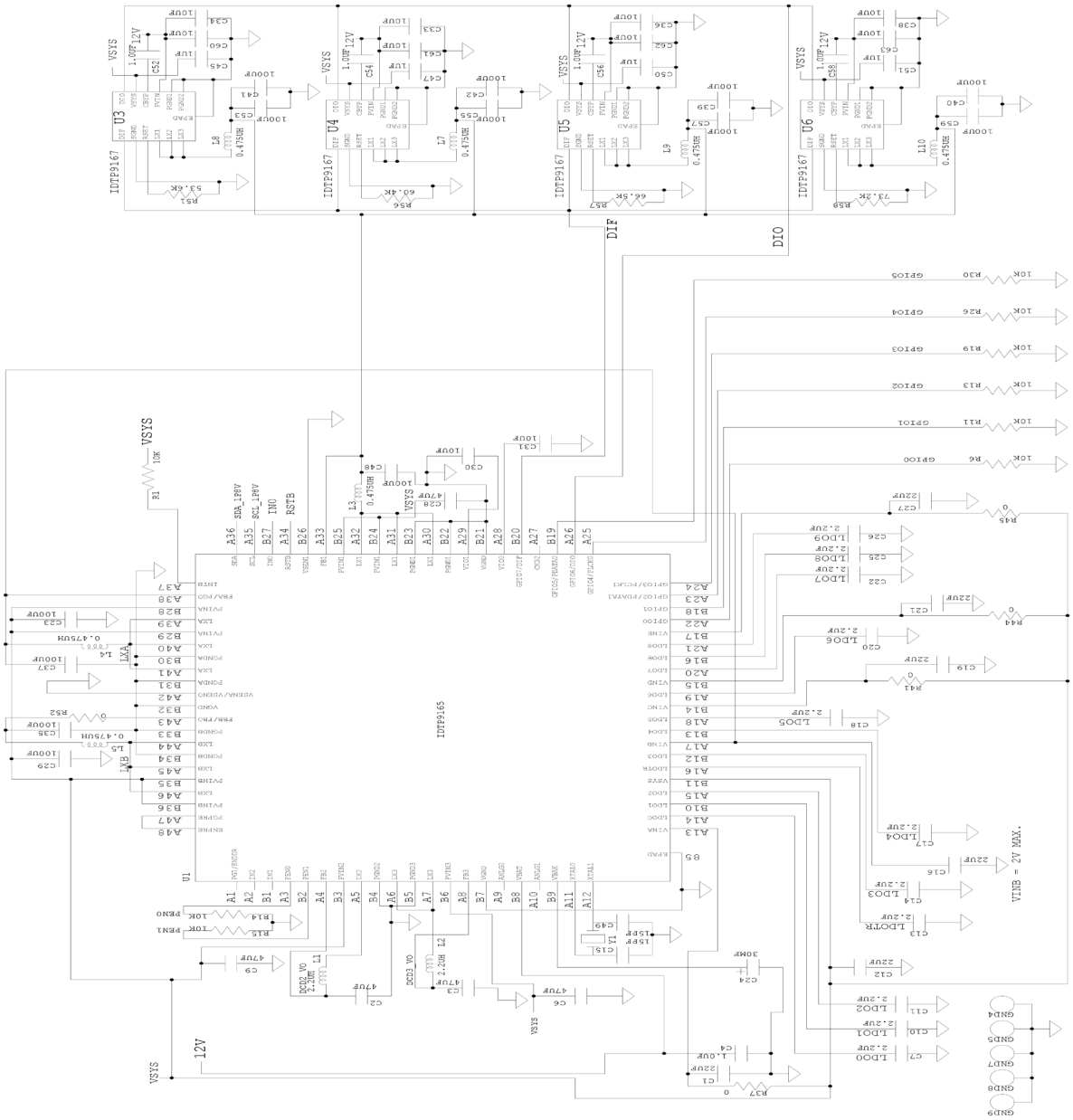


Figure 48 –IDTP9165 Schematic

Item Number	Qty	Description	Ref Design	Part Number
0	4	CAP-1.0UF,0402,10%,X5R,25V	C52,C54,C56,C58	C1005X5R1E105K050BC
1	1	CAP-1.0UF,0603,10%,X7R,25V	C4	CGA3E1X7R1E105K
2	13	CAP-100UF,1206,19.9%,X5R,6.30V	C23,C29,C35,C37, C39-C42,C48,C53,C55,C57,C59	C3216X5R0J107M
3	2	CAP-10UF,0402,19.9%,X5R,6.3V	C30,C31	GRM155R61A106M
4	8	CAP-10UF,0805,10%,X5R,25V	C33,C34,C36,C38,C60-C63	GRM21BR61E106KA73L
5	2	CAP-15PF,0402,5%,NPO,50V	C15,C49	GRM1555C1H150JZ01D
6	4	CAP-1UF,0402,10%,X5R,10V	C45,C47,C50,C51	C1005X5R1A105K
7	11	CAP-2.2UF,0201,19.9%,X5R,6.3V	C7,C10,C11,C13,C14,C17,C18,C20,C22,C25, C26	GRM033R60J225M
8	6	CAP-22UF,0603,19.9%,X5R,6.3V	C1,C12,C16,C19,C21,C27	GRM188R60J226MEA0D
9	5	CAP-47UF,0805,19.9%,X5R,6.3V	C2,C3,C6,C9,C28	GRM21BR60J476ME15L
10	1	CAP_POLARIZED-30MF,SUPERCAP,TBD,3.3V	C24	PAS311HR-VG1
11	1	CRYS_SMD-32.768KHZ,2LD-SMD,20PPM,ECS-.327-12.5-34B	Y1	ECS-.327-12.5-34B
12	1	IDTP9165_SAMELX	U1	IDTP9165-00NQGI
13	4	IDTP9167	U3-U6	IDTP9167
14	7	INDUCTOR-0.475UH,4.0MM by 4.0MM,10.4A,20%,XAL4020-601MEC	L3-L5,L7-L10	XAL4020-601MEC
15	2	INDUCTOR-2.2UH,3.2MM by 2.5MM,3.2(A),30%,DFE322512C	L1,L2	DFE322512C
16	1	RES-0,0201,1%,1/20W,250PPM	R52	ERJ-1GE0R00C
17	4	RES-0,0402,1%,1/10W,-100/+600PPM	R37,R41,R44,R45	ERJ-2GE0R00X
18	3	RES-10K,0402,1%,1/10W,100	R1,R14,R15	RC0402FR-0710KL
19	6	RES-10K,0603,1%,1/10W,100	R6,R11,R13,R19,R26,R30	ERJ-3EKF1002V
20	1	RES-53.6K,0201,1%,1/20W,200PPM	R51	ERJ-1GEF5362C
21	1	RES-60.4K,0201,1%,1/20W,200PPM	R56	ERJ-1GEF6042C
22	1	RES-66.5K,0201,1%,1/20W,200PPM	R57	ERJ-1GEF6652C
23	1	RES-73.2K,0201,1%,1/20W,200PPM	R58	ERJ-1GEF7322C
24	5	TP-PAD70CIR42D,5010	GND4,GND5, GND7-GND9	5010

Figure 49 –IDTP9165 Bill of Materials

Design of components

Recommended values

The IDTP9165 is designed for specific minimum component values as seen in the electrical characteristic tables. These values are chosen to optimize footprint size and performance; furthermore, loop compensation is internal for optimal performance. Use the recommended values for optimal performance. See the electrical charateristic tables for these values (see Table 5 and following, as well as Table 20). The following equations can be used to evaluate the voltages and currents that result.

Inductor – L

L is the inductor connected to the switch node of the IDTP9165. This along with the output capacitor filters the pulsed input voltages and currents to create a constant output voltage. The inductor must be able to handle the maximum current without saturating. It must also limit the current ripple to an amount that will not cause the output voltage ripple to be too large. The inductor ripple current can be calculated from the following equation:

$$\Delta I_L = \frac{V_{IN} - V_{OUT}}{L} \times \frac{V_{OUT}}{V_{IN} \times F_{SW}}$$

Where:

- L (H): Inductor value
- V_{IN} (V): Input voltage
- V_{OUT} (V): Output voltage
- ΔI_L (A): Inductor current ripple
- F_{SW} (Hz): The switching frequency

Power input capacitor - C_{PVIN}

C_{PVIN} is the power input filter capacitor. This capacitor supplies all the power to the output of its respective IDTP9165.As with any buck type switching regulator this capacitor sees very large ac currents. The ripple current and ripple voltage must be calculated and the appropriate capacitor chosen. The capacitor input ripple current can be calculated with the following equation:

$$I_{RMS} = I_{OUT} \times \sqrt{D} \times \sqrt{1 + \left(\frac{1}{3}\right) \times \left(\frac{\frac{\Delta I_L}{2}}{I_{OUT}}\right)^2}$$

The peak to peak voltage ripple of the input capacitor is:

$$V_{PP} = D \times I_{OUT} \times \left(R_{ESR} + \frac{1 - D}{C_{PVIN} \times F_{SW}}\right)$$

This can be rearranged to find the desired C_{PVIN} given the designed for V_{PP}.

$$C_{PVIN} = \left(\frac{1 - D}{F_{SW}}\right) \times \left(\frac{1}{\frac{V_{PP}}{D \times I_{OUT}} - R_{ESR}}\right)$$

From V_{PP} the V_{RMS} of the input voltage ripple can be found from:

$$V_{RMS} = \frac{\frac{V_{PP}}{2}}{\sqrt{3}}$$

Where:

- I_{RMS} (A): Current ripple seen by the input capacitor
- D: Duty cycle. The proportion of switching period when the high side switch is on and the IC is charging up its inductor with current.
- I_{OUT} (A): The maximum output load current
- ΔI_L (A): Inductor current ripple, peak to peak
- C_{PVIN} (F): Input power capacitor
- V_{RMS} (V): Root mean square value of C_{PVIN} ripple
- V_{IN} (V): Input voltage
- V_{PP} (V): Peak to peak ripple voltage at the input capacitor
- F_{SW} (Hz): The switching frequency

Output capacitor – C_{OUT}

The output capacitor combines with the inductor to filter the currents and voltages in order to provide a constant output voltage. This capacitor will have a voltage ripple associated with it. This ripple must be much smaller than the output voltage. Typical values are in the range of 0.1% of V_{OUT}. The voltage rating of this capacitor should be at least double of maximum output voltage. This helps to reduce the value of C_{OUT} desired. Given the desired C_{OUT}, the desired ripple can be calculated from the formula:

$$\Delta V_{OUT} = \frac{\Delta I_L}{8 \times C_{OUT} \times F_{SW}}$$

Where:

- C_{OUT} (F): Output capacitor
- ΔI_L (A): Inductor current ripple
- ΔV_{OUT} (V): Output voltage ripple (typically 0.1% x V_{OUT})
- F_{SW} (Hz): Switching frequency

The input capacitor (C_{IN}) should be connected directly between the power VIN and power PGND pins.
The output capacitor (C_{OUT}) and power ground should be connected together to minimize any DC regulation errors caused by ground potential differences.

The output-sense connection to the feedback pins should be separated from any switching node. Route the output-sense trace as close as possible to the load point to avoid additional load regulation errors. Sensing through a high-current load trace will degrade DC load regulation.

LDOs

Input Capacitor LDOs

The input capacitors should be located as physically close as possible to the power pin and power ground (GND). Use ceramic capacitors for their higher current operation and small profile. Ceramic capacitors are inherently more capable than are tantalum capacitors to withstand input current surges from low impedance sources such as batteries used in portable devices. Typically, 10V rated capacitors are required (roughly double the input voltage). The recommended external components are shown in Table 11and following.(see also Table 20)

Output Capacitor - LDOs

For proper load voltage regulation and operational stability, a capacitor is required on the output of each LDO. The output capacitor connection to the ground pin (PGND) should be made as close as practically possible to the IDTP9165 for maximum device performance. Since the LDOs have been designed to function with very low ESR capacitors, a ceramic capacitor is recommended for best performance.

Tracking LDO - LDOTR

LDOTR can be programmed to an independent voltage through the register LDOTRC0 (address 24). LDOTR can also track either DCD0 or DCD1. To enable tracking set LDOTR_TRC in register LDOTRC1 to “1”. Choose between tracking DCD0 or DCD1 through programming of the LDOTR_SEL bit in the CONFIG0 register (address 127). LDOTR_SEL=”0”= track DCD1, “1” = track DCD0.

Charger

The IDTP9165 has the ability to charge a cell battery / super cap. The output voltage and series resistance are programmable within the range specified in Table 15

I²C DESCRIPTION

The IDTP9165’s I²C port conforms to the 3.4 MHz High-speed mode (Hs-mode) I²C bus protocol and supports 7-bit device / page addressing. The IDTP9165’s I²C port follows I²C bus protocol during register reads or writes that are initiated by an external I²C Master (typically the application processor). PCB Layout Considerations

PCB Layout Considerations

C_{OUT} placement

All C_{OUT} capacitors should be placed as close to the load as possible. The voltage and ground sense lines that feed back to the host IC to control the output voltage should be placed as close to the load as possible. Be careful to shield the feedback lines from noise as these are high impedance lines and therefore sensitive to noise.

For optimum device performance and lowest output phase noise, the following guidelines must be observed. Please contact IDT for Gerber files that contain the recommended board layout.

- As for all switching power supplies, especially those providing high current and using high switching frequencies, layout is an important design step. If layout is not carefully done, the regulator could show instability as well as EMI problems. Therefore, use wide and short traces for high current paths.
- The C_{IN} decoupling capacitor must be mounted on the component side of the board as close to their respective pins as possible. Do not use vias between the decoupling capacitors and their pins. Keep PCB traces to each pin and to ground vias as short as possible. The C_{IN} is the most important to keep close to the IDTP9165 with the shortest power and ground traces possible because C_{IN} carries, filters and delivers the power from the battery to the IDTP9165. If it is not possible to have the input voltage plane and the ground plane on the top layers then make use at

least 1 via for every 500mA of current that C_{IN} will handle.

- To optimize board layout, place all components on the same side of the board and limit the use of vias. Route other signal traces away from the IDTP9165. For example, use keep outs for signal traces routing on inner and bottom layers underneath the device.
- The NQG QFN-84 package has an inner thermal pad which requires blind assembly. It is recommended that a more active flux solder paste be used such as Alpha OM-350 solder paste from Cookson Electronics (http://www.cooksonsemi.com). Please contact IDT for Gerber files that contain recommended solder stencil design.
- The package center exposed pad (EP) must be reliably soldered directly to the PCB. The center land pad on the PCB (set 1:1 with EP) must also be tied to the board ground plane, primarily to maximize thermal performance in the application. The ground connection is best achieved using a matrix of plated-through-hole (PTH) vias embedded in the PCB center land pad for the NQG QFN-84. The PTH vias perform as thermal conduits to the ground plane (thermally, a heat spreader) as well as to the solder side of the board. There, these thermal vias embed in a copper fill having the same dimensions as the center land pad on the component side. Recommendations for the via finished hole-size and array pitch are .012" and .037", respectively. A symmetrical array of 5x5 vias is recommended.
- Layout and PCB design have a significant influence on the power dissipation capabilities of power management ICs. This is due to the fact that the surface mount packages used with these devices rely heavily on thermally conductive traces or pads to transfer heat away from the package. Appropriate PC layout techniques must then be used to remove the heat due to device power dissipation. The following general guidelines will be helpful in designing a board layout for lowest thermal resistance:
    1. PC board traces with large cross sectional areas remove more heat. For optimum results, use large area PCB patterns with wide and heavy (2 oz.) copper traces, placed on the top layer of the PCB.
    2. In cases where maximum heat dissipation is required, use double-sided copper planes connected with multiple vias.
    3. Thermal vias are needed to provide a thermal path to the inner and/or bottom layers of the PCB to remove the heat generated by device power dissipation.
    4. Where possible, increase the thermally conducting surface area(s) openly exposed to moving air, so that heat can be removed by convection (or forced air flow, if available).
    5. Do not use solder mask or place silkscreen on the heat-dissipating traces/pads, as they increase the net thermal resistance of the mounted IC package.

Power Dissipation/Thermal Requirements

The IDTP9165 is offered in a NQG QFN-84 package. The maximum power dissipation capability is limited by the die's specified maximum operating junction temperature, T_J, of 125°C. The junction temperature rises with the device power dissipation based on the package thermal resistance. The package offers a typical thermal resistance, junction to ambient (θ_{JA}), of 30.6°C/W (see **Table 2**) when the PCB layout and surrounding devices are optimized as described in the PCB Layout Considerations section. The techniques as noted in the PCB Layout section need to be followed when designing the printed circuit board layout, as well as the placement of the IDTP9165 IC package in proximity to other heat generating devices in a given application design. The ambient temperature around the power IC will also have an effect on the thermal limits of an application. The main factors influencing θ_{JA} (in the order of decreasing influence) are PCB characteristics, die/package attach thermal pad size, and internal package construction. Board designers should keep in mind that the package thermal metric θ_{JA} is impacted by the characteristics of the PCB itself upon which the NQG QFN-84 is mounted. For example, in a still air environment, as is often the case, a significant amount of the heat that is generated (60 - 85%) sinks into the PCB. Changing the design or configuration of the PCB changes impacts the overall thermal resistivity and, thus, the board's heat sinking efficiency.

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system

dependent issues such as thermal coupling, airflow, added heat sinks, and convection surfaces, and the presence of other heat-generating components, affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below:

1. Improve the power dissipation capability of the PCB design
2. Improve the thermal coupling of the component to the PCB
3. Introduce airflow into the system

Maximum Power Calculation

First, the maximum power dissipation for a given situation must be calculated:

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

Where:

- $P_{D(MAX)}$ = Maximum Power Dissipation (W)
- θ_{JA} = Package Thermal Resistance (°C/W)
- $T_{J(MAX)}$ = Maximum Device Junction Temperature (°C)
- T_A = Ambient Temperature (°C)

The maximum recommended junction temperature ($T_{J(MAX)}$) for the IDTP9165 device is 150°C. The thermal resistance of the NQG QFN-84 is optimally θ_{JA}=30°C/W. Operation is specified to a maximum steady-state ambient temperature (T_A) of 85°C. Therefore, the maximum recommended power dissipation is 2.1W:

Thermal Overload Protection

The IDTP9165 integrates thermal overload shutdown circuitry to prevent damage resulting from excessive thermal stress that may be encountered under fault conditions. This circuitry will shut down or reset the device if the die temperature exceeds 130°C. To allow the maximum load current on each regulator, and to prevent thermal overload, it is important to ensure that the heat generated by the IDTP9165 is dissipated into the PCB. The package exposed paddle must be soldered to the PCB, with multiple vias evenly distributed under the exposed paddle and exiting the bottom side of the PCB. This improves heat flow away from the package and minimizes package thermal gradients.

Special Notes

NQG QFN-84 Package Assembly

Note 1: Unopened Dry Packaged Parts have a one year shelf life.

Note 2: Newly opened Dry Packaged Parts HIC indicator card should be checked, if there is any moisture content, the parts need to be baked for minimum of 8 hours at 125˚ C within 24 hours of the assembly reflow process.

Note 3: Opened Dry Packaged parts that are not assembled within 168 hours of opening must be baked for minimum of 8 hours at 125˚C within 24 hours of the assembly reflow process.

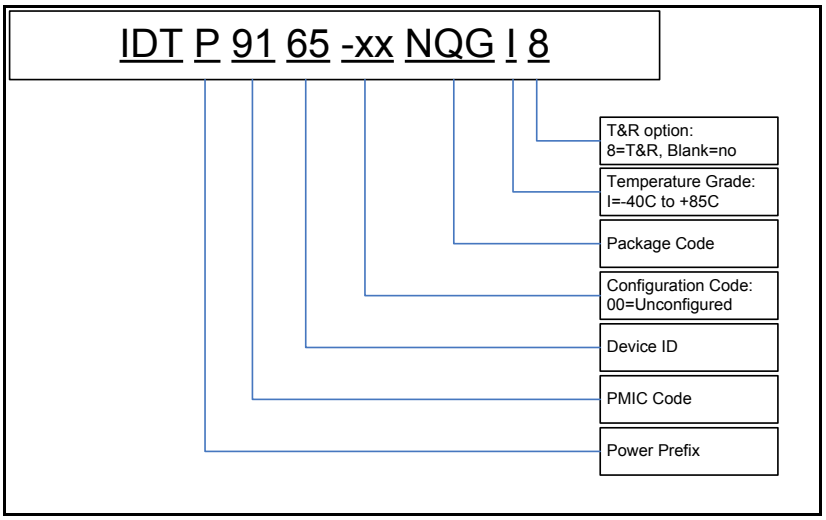
ORDERING GUIDE

Table 60 – Ordering Summary

PART NUMBER	MARKING	PACKAGE	AMBIENT TEMP. RANGE	SHIPPING CARRIER	QUANTITY
P9165-xxNQGI	P9165-xxNQGI	84ld-7x7 DR-QFN	-40°C to +85°C	Tape or Canister	25
P9165-xxNQGI8	P9165-xxNQGI	84ld-7x7 DR-QFN T&R	-40°C to +85°C	Tape and Reel	2,500

The **–xx** part number suffix identifies the device OTP (fuse) configuration. Please contact IDT for additional information.

NQG84: 84ld-7x7 DR-QFN, Please refer to http://www.idt.com/package/ngg84 for package information.



Note [1] Loop BW Limited
Note [2] Output current can approach 10A if the combined output current of all supplies does not cause the T_J to exceed the thermal shutdown limit of 132°C
Note [3] Output current can approach 5A if the combined output current of all supplies does not cause the T_J to exceed the thermal shutdown limit of 132°C
Note [4] Trim option 1 and 2: DCD0 is dual phase 10A step down converter.
Note [5] Trim option 3: DCD0 is split into two independent 5A step down converter – DCD0a and DCD0b
Note [6] In SLEEP state RSTB remains high

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.