

ISL12022

Low Power RTC with Battery-Backed SRAM and Embedded Temp Compensation $\pm 5\text{ppm}$ with Auto Daylight Saving

Description

The **ISL12022** device is a low power real time clock with an embedded Temp sensor for oscillator compensation, clock/calendar, power fail, low battery monitor, brownout indicator, single periodic or polled alarms, intelligent battery-backup switching, Battery Reseal™ function, and 128 bytes of battery-backed user SRAM.

The oscillator uses an external, low-cost 32.768kHz crystal. The real time clock tracks time with separate registers for hours, minutes, and seconds. The device has calendar registers for date, month, year, and day of the week. The calendar is accurate through 2099, with automatic leap year correction.

Daylight Savings time adjustment is done automatically, using parameters entered by the user. Power fail and battery monitors offer user-selectable trip levels. A time stamp function records the time and date of switchover from V_{DD} to V_{BAT} power, and also from V_{BAT} to V_{DD} power.

Applications

- Utility Meters
- POS Equipment
- Medical Devices
- Security Systems
- Vending Machines
- White Goods
- Printers and Copiers

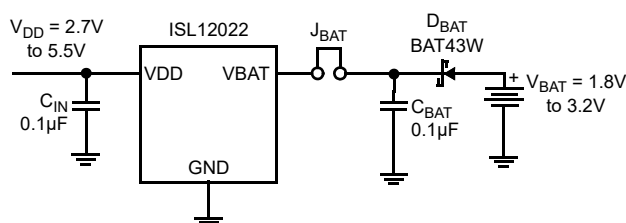


Figure 1. Typical Application Circuit

Features

- Real Time Clock/Calendar
 - Tracks Time in Hours, Minutes and Seconds
 - Day of the Week, Day, Month, and Year
- On-chip Oscillator Compensation Over the Operating Temperature Range
 - $\pm 5\text{ppm}$ Over -40°C to $+85^{\circ}\text{C}$
- 10-bit Digital Temperature Sensor Output
 - $\pm 2^{\circ}\text{C}$ Accuracy
- Customer Programmable Day Light Saving Time
- 15 Selectable Frequency Outputs
- 1 Alarm
 - Settable to the Second, Minute, Hour, Day of the Week, Day, or Month
 - Single Event or Pulse Interrupt Mode
- Battery Reseal™ Function to Extend Battery Shelf Life
- Automatic Backup to Battery or Super Capacitor
 - Operation to $V_{BAT} = 1.8\text{V}$
 - $1.0\mu\text{A}$ Battery Supply Current
- Battery Status Monitor
 - 2 User Programmable Levels
 - Seven Selectable Voltages for Each Level
- Power Status Brownout Monitor
 - Six Selectable Trip Levels, from 2.295V to 4.675V
- Oscillator Failure Detection
- Time Stamp for First V_{DD} to V_{BAT} , and Last V_{BAT} to V_{DD}
- 128 Bytes Battery-Backed User SRAM
- I²C Bus™
 - 400kHz Clock Frequency
- $1\mu\text{A}$ Typical Battery Current
- Pb-Free (RoHS Compliant)

Contents

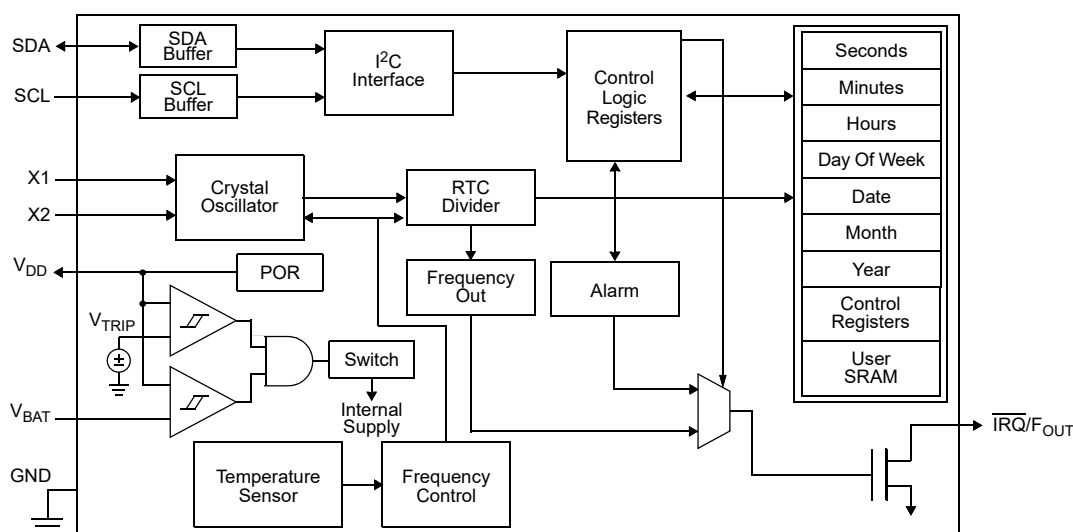
1. Overview	5
1.1 Block Diagram	5
2. Pin Information	5
2.1 Pin Configuration	5
2.2 Pin Descriptions	5
3. Specifications	6
3.1 Absolute Maximum Ratings	6
3.2 Thermal Specifications	6
3.3 DC Operating Characteristics - RTC	6
3.4 Power-Down Timing	7
3.5 I ² C Interface Specifications	7
4. Typical Performance Curves	10
5. General Description	11
6. Pin Descriptions	12
6.1 X1, X2	12
6.2 V _{BAT}	12
6.3 IRQ/F _{OUT} (Interrupt Output/Frequency Output)	12
6.4 Serial Clock (SCL)	12
6.5 Serial Data (SDA)	12
6.6 V _{DD} , GND	13
7. Functional Description	13
7.1 Power Control Operation	13
7.2 Normal Mode (V _{DD}) to Battery-Backup Mode (V _{BAT})	13
7.3 Battery-Backup Mode (V _{BAT}) to Normal Mode (V _{DD})	13
7.4 Power Failure Detection	14
7.5 Brownout Detection	14
7.6 Battery Level Monitor	14
8. Real Time Clock Operation	14
8.1 Single Event and Interrupt	14
8.2 Frequency Output Mode	15
8.3 General Purpose User SRAM	15
8.4 I ² C Serial Interface	15
8.5 Oscillator Compensation	15
9. Register Descriptions	15
9.0.1 Register Access	17
10. Real Time Clock Registers	18
10.1 Addresses [00h to 06h]	18
10.1.1 RTC Registers (SC, MN, HR, DT, MO, YR, DW)	18
10.1.2 24 Hour Time	18
10.1.3 Leap Years	18
11. Control and Status Registers (CSR)	18
11.1 Addresses [07h to 0Fh]	18
11.2 Status Register (SR)	18
11.2.1 Busy Bit (BUSY)	18
11.2.2 Oscillator Fail Bit (OSCF)	18
11.2.3 Daylight Savings Time Change Bit (DSTADJ)	18
11.2.4 Alarm Bit (ALM)	19
11.2.5 Low V _{DD} Indicator Bit (LV _{DD})	19
11.2.6 Low Battery Indicator 85% Bit (LBAT85)	19
11.2.7 Low Battery Indicator 75% Bit (LBAT75)	19

11.2.8	Real Time Clock Fail Bit (RTCF)	20
11.3	Interrupt Control Register (INT)	20
11.3.1	Automatic Reset bit (ARST)	20
11.3.2	Write RTC Enable Bit (WRTC)	20
11.3.3	Interrupt/Alarm Mode Bit (IM)	20
11.3.4	Frequency Output and Interrupt Bit (FOBATB)	20
11.3.5	Frequency Out Control Bits (FO[3:0])	21
11.3.6	Power Supply Control Register (PWR_VDD)	21
11.4	V _{DD} Brownout Trip Voltage BITS (V _{DD} Trip[2:0])	21
11.5	Battery Voltage Trip Voltage Register (PWR_VBAT)	22
11.5.1	Reseal Bit (RESEALB)	22
11.5.2	Battery Level Monitor Trip Bits (VB85TP[2:0])	22
11.5.3	Battery Level Monitor Trip Bits (VB75TP[2:0])	22
11.6	Initial AT and DT Setting Register (ITRO)	23
11.6.1	Aging and Initial Trim Digital Trimming Bits (IDTRO[1:0])	23
11.6.2	Aging and Initial Analog Trimming Bits (IATRO [5:0])	23
11.6.3	ALPHA Register (ALPHA)	25
11.6.4	BETA Register (BETA)	25
11.6.5	Temperature Sensor Enabled Bit (TSE)	25
11.6.6	Temp Sensor Conversion in Battery Mode Bit (BTSE)	25
11.6.7	Frequency of Temperature Sensing and Correction Bit (BTSR)	26
11.6.8	Gain Factor of AT BIT (BETA[4:0])	26
11.7	Final Analog Trimming Register (FATR)	27
11.8	Final Digital Trimming Register (FDTR)	27
11.9	ALARM Registers (10h to 15h)	28
11.9.1	Example 1	29
11.9.2	Example 2	29
11.10	Time Stamp VDD to Battery Registers (TSV2B)	30
11.11	Time Stamp Battery to VDD Registers (TSB2V)	30
11.12	DST Control Registers (DSTCR)	30
11.12.1	DST Forward Registers (20h to 23h)	30
11.12.2	DST Reverse Registers (24h to 27h)	31
11.13	TEMP Registers (TEMP)	32
11.14	NPPM Registers (NPPM)	32
11.15	XT0 Registers (XT0)	33
11.15.1	Turnover temperature (XT[4:0])	33
11.16	ALPHA Hot Register (ALPHAH)	34
12.	User Registers (Accessed by Using Slave Address 1010111x)	34
12.1	Addresses [00h to 7Fh]	34
13.	I²C Serial Interface	34
13.1	Protocol Conventions	34
14.	Device Addressing	35
15.	Write Operation	36
16.	Read Operation	36
17.	Applications Information	37
17.1	Power Supply Considerations	37
17.2	Battery-Backup Details	37
17.3	Oscillator Crystal Requirements	38
17.4	Layout Considerations	38
17.5	Crystal Oscillator Frequency Compensation	39
17.5.1	Crystal Characteristics	39
17.5.2	RTC Clock Control	39

17.5.3	Active Temperature Compensation	40
17.6	Measuring Oscillator Accuracy	40
17.7	Temperature Compensation Operation	40
17.8	Daylight Savings Time (DST) Example	41
18.	Package Outline Drawing	41
19.	Ordering Information	42
20.	Revision History	42

1. Overview

1.1 Block Diagram



2. Pin Information

2.1 Pin Configuration

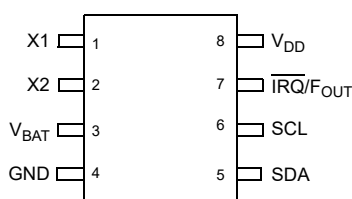


Figure 2. Pin Configuration - Top View

2.2 Pin Descriptions

Pin #	Symbol	Description
1	X1	Crystal Input. The X1 pin is the input of an inverting amplifier and is intended to be connected to one pin of an external 32.768kHz quartz crystal. X1 can also be driven directly from a 32.768kHz source.
2	X2	Crystal Output. The X2 pin is the output of an inverting amplifier and is intended to be connected to one pin of an external 32.768kHz quartz crystal. X2 should be left open when X1 is driven from external source.
3	V _{BAT}	Backup Supply. This input provides a backup supply voltage to the device. V _{BAT} supplies power to the device in the event that the V _{DD} supply fails. This pin should be tied to ground if not used.
4	GND	Ground.
5	SDA	Serial Data. SDA is a bi-directional pin used to transfer serial data into and out of the device. It has an open drain output and may be wire OR'ed with other open drain or open collector outputs.
6	SCL	Serial Clock. The SCL input is used to clock all serial data into and out of the device.
7	IRQ/F _{OUT}	Interrupt Output/Frequency Output. Multi-functional pin that can be used as interrupt or frequency output pin. The function is set via the configuration register. It is an open-drain output.
8	V _{DD}	Power Supply.

3. Specifications

3.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
Voltage on VDD, VBAT and $\overline{\text{IRQ}}/\text{F}_{\text{OUT}}$ Pins (Respect to Ground)	-0.3	6.0	V
Voltage on SCL and SDA Pins (Respect to Ground)	-0.3	0.3	V
Voltage on X1 and X2 pins (respect to ground)	-0.3	2.5	V
Maximum Storage Temperature Range	-65	150	°C
Human Body Model (Tested per Per MIL-STD-883 Method 3014)	-	3000	V
Machine Model	-	300	V

3.2 Thermal Specifications

Parameter	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance	8 Lead SOIC	$\theta_{\text{JA}}^{[1]}$	Junction to ambient	102	°C/W
		$\theta_{\text{JC}}^{[2]}$	Junction to case	46	°C/W

1. θ_{JA} is measured with the component mounted on a high-effective thermal conductivity test board in free air. See [TB379](#) for details.
2. For θ_{JC} , the case temperature location is taken at the package top center.

3.3 DC Operating Characteristics - RTC

Test Conditions: $V_{\text{DD}} = +2.7$ to $+5.5\text{V}$, $T_{\text{A}} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, unless otherwise stated. **Boldface limits apply across the operating temperature range, -40°C to $+85^{\circ}\text{C}$**

Parameter	Symbol	Conditions	Min ^[1]	Typ ^[2]	Max ^[1]	Unit
Main Power Supply ^[3]	V_{DD}	-	2.7	-	5.5	V
Battery Supply Voltage ^{[3][4]}	V_{BAT}	-	1.8	-	5.5	V
Supply Current. (I ² C not Active, Temperature Conversion not Active, F_{OUT} not Active) ^{[5][6]}	I_{DD1}	$V_{\text{DD}} = 5\text{V}$	-	4.1	15	μA
		$V_{\text{DD}} = 3\text{V}$	-	3.5	14	μA
Supply Current. (I ² C Active, Temperature Conversion not Active, F_{OUT} not Active) ^{[5][6]}	I_{DD2}	$V_{\text{DD}} = 5\text{V}$	-	200	500	μA
Supply Current. (I ² C not Active, Temperature Conversion Active, F_{OUT} not Active) ^{[5][6]}	I_{DD3}	$V_{\text{DD}} = 5\text{V}$	-	120	400	μA
Battery Supply Current ^[5]	I_{BAT}	$V_{\text{DD}} = 0\text{V}$, $V_{\text{BAT}} = 3\text{V}$, $T_{\text{A}} = +25^{\circ}\text{C}$	-	1.0	1.6	μA
		$V_{\text{DD}} = 0\text{V}$, $V_{\text{BAT}} = 3\text{V}$	-	1.0	5.0	μA
Battery Input Leakage	I_{BATLKG}	$V_{\text{DD}} = 5.5\text{V}$, $V_{\text{BAT}} = 1.8\text{V}$	-		100	nA
Input Leakage Current on SCL	I_{LI}	$V_{\text{IL}} = 0\text{V}$, $V_{\text{IH}} = 5.5\text{V}$	-1.0	±0.1	1.0	μA
I/O Leakage Current on SDA	I_{LO}	$V_{\text{IL}} = 0\text{V}$, $V_{\text{IH}} = 5.5\text{V}$	-1.0	±0.1	1.0	μA
Battery Level Monitor Threshold	V_{BATM}	-	-100		+100	mV
Brownout Level Monitor Threshold	V_{PBM}	-	-100		+100	mV
V_{BAT} Mode Threshold ^[3]	V_{TRIP}	-	2.0	2.2	2.4	V
V_{TRIP} Hysteresis ^[7]	V_{TRIPHYS}	-	-	30	-	mV
V_{BAT} Hysteresis ^[7]	V_{BATHYS}	-	-	50	-	mV
Oscillator Stability vs Temperature ^[8]	ΔFout_T	$V_{\text{DD}} = 3.3\text{V}$	-5	-	+5	ppm

Test Conditions: $V_{DD} = +2.7$ to $+5.5V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise stated. **Boldface limits apply across the operating temperature range, $-40^{\circ}C$ to $+85^{\circ}C$** (Cont.)

Parameter	Symbol	Conditions	Min ^[1]	Typ ^[2]	Max ^[1]	Unit
Oscillator Stability vs Voltage ^[8]	ΔF_{out_V}	$2.7V \leq V_{DD} \leq 5.5V$	-3	-	+3	ppm
AT Sensitivity per LSB ^[8]	ΔAT_{LSB}	BETA (4:0) = 10000	0.5	1	2	ppm
Temperature Sensor Accuracy ^[7]	Temp	$V_{DD} = V_{BAT} = 3.3V$	-	± 2		$^{\circ}C$
IRQ/F_{OUT} (Open-Drain Output)						
Output Low Voltage	V_{OL}	$V_{DD} = 5.5V, I_{OL} = 3mA$	-	-	0.4	V
		$V_{DD} = 2.7V, I_{OL} = 1mA$	-	-	0.4	V

- Parameters with MIN and/or MAX limits are 100% tested at $+25^{\circ}C$, unless otherwise specified. Temperature limits established by characterization and are not production tested.
- Specified at $+25^{\circ}C$.
- Minimum V_{DD} and/or V_{BAT} of 1V to sustain the SRAM. The value is based on characterization and it is not tested.
- Temperature Conversion is inactive below $V_{BAT} = 2.7V$. Device operation is not guaranteed at $V_{BAT} < 1.8V$.
- IRQ/F_{OUT} inactive.
- $V_{DD} > V_{BAT} + V_{BATHYS}$.
- Limits should be considered typical and are not production tested.
- Specifications are typical and require using a recommended crystal (see [Applications Information](#)).

3.4 Power-Down Timing

Test Conditions: $V_{DD} = +2.7$ to $+5.5V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise stated. **Boldface limits apply across the operating temperature range, $-40^{\circ}C$ to $+85^{\circ}C$** .

Parameter	Symbol	Conditions	Min ^[1]	Typ ^[2]	Max ^[1]	Unit
V_{DD} Negative Slew Rate ^[3]	$V_{DD} \text{ SR-}$	-	-	-	10	V/ms
V_{DD} Positive Slew Rate, Minimum ^[4]	V_{DDSR+}	-	-	0.05	-	V/ms

- Parameters with MIN and/or MAX limits are 100% tested at $+25^{\circ}C$, unless otherwise specified. Temperature limits established by characterization and are not production tested.
- Specified at $+25^{\circ}C$.
- To ensure proper timekeeping, the $V_{DD} \text{ SR-}$ specification must be followed.
- To avoid EEPROM recall issues, it is advised to use this minimum power up slew rate. Not tested, shown as typical only.

3.5 I²C Interface Specifications

Test Conditions: $V_{DD} = +2.7$ to $+5.5V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise specified. **Boldface limits apply across the operating temperature range, $-40^{\circ}C$ to $+85^{\circ}C$**

Parameter	Symbol	Test Conditions	Min ^[1]	Typ ^[2]	Max ^[1]	Unit
SDA and SCL Input Buffer LOW Voltage	V_{IL}	-	-0.3	-	$0.3 \times V_{DD}$	V
SDA and SCL Input Buffer HIGH Voltage	V_{IH}	-	$0.7 \times V_{DD}$	-	$V_{DD} + 0.3$	V
SDA and SCL Input Buffer Hysteresis ^{[3][4]}	Hysteresis	-	$0.05 \times V_{DD}$	-	-	V
SDA Output Buffer LOW Voltage, Sinking 3mA	V_{OL}	$V_{DD} = 5V, I_{OL} = 3mA$	0	0.02	0.4	V
SDA and SCL Pin Capacitance ^{[3][4]}	C_{PIN}	$T_A = +25^{\circ}C, f = 1MHz, V_{DD} = 5V, V_{IN} = 0V, V_{OUT} = 0V$	-	-	10	pF
SCL Frequency	f_{SCL}	-	-	-	400	kHz
Pulse Width Suppression Time at SDA and SCL Inputs	t_{IN}	Any pulse narrower than the max spec is suppressed.	-	-	50	ns
SCL Falling Edge To SDA Output Data Valid	t_{AA}	SCL falling edge crossing 30% of V_{DD} , until SDA exits the 30% to 70% of V_{DD} window.	-	-	900	ns

Test Conditions: $V_{DD} = +2.7$ to $+5.5V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise specified. **Boldface limits apply across the operating temperature range, $-40^{\circ}C$ to $+85^{\circ}C$** (Cont.)

Parameter	Symbol	Test Conditions	Min ^[1]	Typ ^[2]	Max ^[1]	Unit
Time the Bus Must be Free Before the Start of a New Transmission	t_{BUF}	SDA crossing 70% of V_{DD} during a STOP condition, to SDA crossing 70% of V_{DD} during the following START condition.	1300	-	-	ns
Clock LOW Time	t_{LOW}	Measured at the 30% of V_{DD} crossing.	1300	-	-	ns
Clock HIGH Time	t_{HIGH}	Measured at the 70% of V_{DD} crossing.	600	-	-	ns
START Condition Setup Time	$t_{SU:STA}$	SCL rising edge to SDA falling edge. Both crossing 70% of V_{DD} .	600	-	-	ns
START Condition Hold Time	$t_{HD:STA}$	From SDA falling edge crossing 30% of V_{DD} to SCL falling edge crossing 70% of V_{DD} .	600	-	-	ns
Input Data Setup Time	$t_{SU:DAT}$	From SDA exiting the 30% to 70% of V_{DD} window, to SCL rising edge crossing 30% of V_{DD} .	100	-	-	ns
Input Data Hold Time	$t_{HD:DAT}$	From SCL falling edge crossing 30% of V_{DD} to SDA entering the 30% to 70% of V_{DD} window.	0	-	900	ns
STOP Condition Setup Time	$t_{SU:STO}$	From SCL rising edge crossing 70% of V_{DD} , to SDA rising edge crossing 30% of V_{DD} .	600	-	-	ns
STOP Condition Hold Time	$t_{HD:STO}$	From SDA rising edge to SCL falling edge. Both crossing 70% of V_{DD} .	600	-	-	ns
Output Data Hold Time	t_{DH}	From SCL falling edge crossing 30% of V_{DD} , until SDA enters the 30% to 70% of V_{DD} window.	0	-	-	ns
SDA and SCL Rise Time ^[4]	t_R	From 30% to 70% of V_{DD} .	$20 + 0.1 \times C_b$	-	300	ns
SDA and SCL Fall Time ^[4]	t_F	From 70% to 30% of V_{DD} .	$20 + 0.1 \times C_b$	-	300	ns
Capacitive Loading of SDA or SCL ^[4]	C_b	Total on-chip and off-chip	10	-	400	pF
SDA and SCL Bus Pull-up Resistor Off-chip ^[4]	R_{PU}	Maximum is determined by t_R and t_F . For $C_b = 400pF$, max is about $2k\Omega \sim 2.5k\Omega$. For $C_b = 40pF$, max is about $15k\Omega \sim 20k\Omega$	1	-	-	$k\Omega$

- Parameters with MIN and/or MAX limits are 100% tested at $+25^{\circ}C$, unless otherwise specified. Temperature limits established by characterization and are not production tested.
- Specified at $+25^{\circ}C$.
- Limits should be considered typical and are not production tested.
- These are I^2C specific parameters and are not tested, however, they are used to set conditions for testing devices to validate specification.

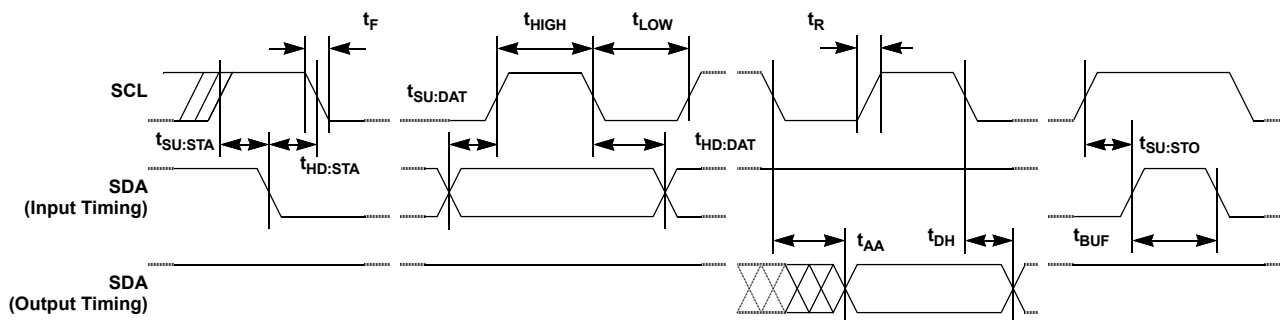
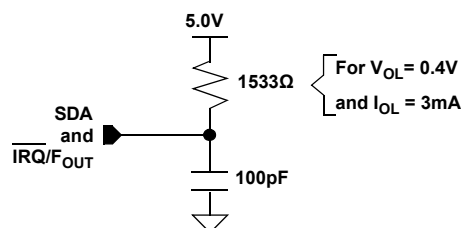


Figure 3. SDA vs SCL Timing

Waveform	Inputs	Outputs
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Figure 4. Symbol Table

Equivalent AC Output Load Circuit for $V_{DD} = 5V$ Figure 5. Standard Output Load for Testing the Device with $V_{DD} = 5.0V$

4. Typical Performance Curves

Temperature is +25°C unless otherwise specified.

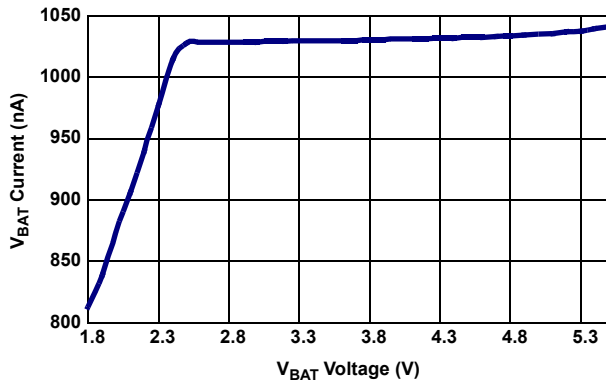


Figure 6. I_{BAT} vs V_{BAT}

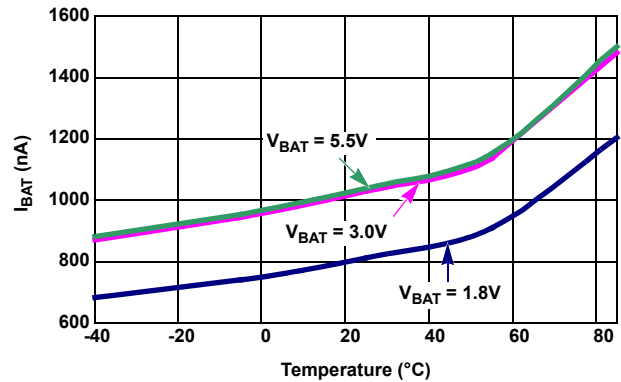


Figure 7. I_{BAT} vs Temperature

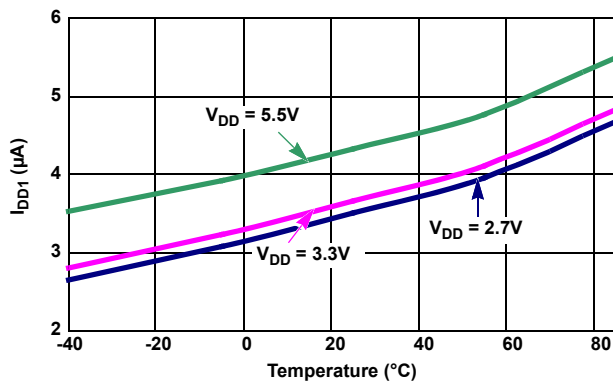


Figure 8. I_{DD1} vs Temperature

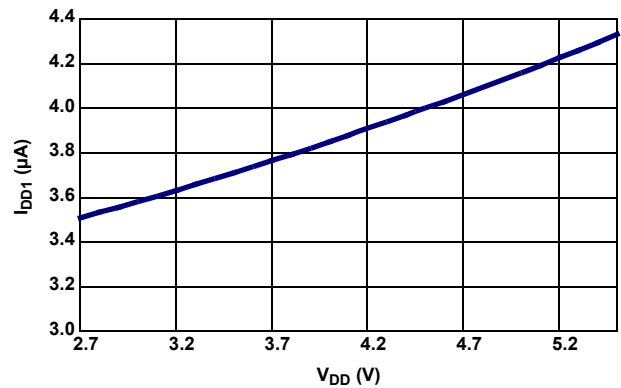


Figure 9. I_{DD1} vs V_{DD}

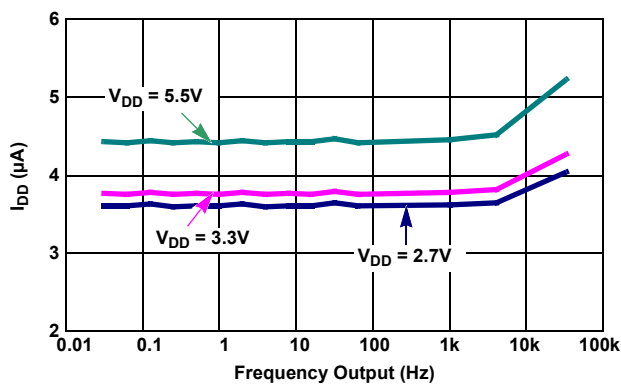


Figure 10. F_{OUT} vs I_{DD}

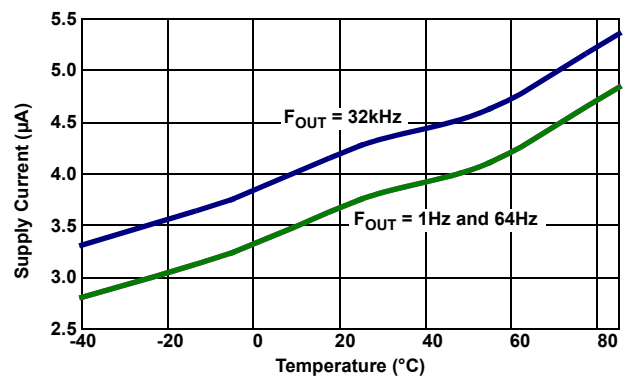


Figure 11. I_{DD} vs Temperature, 3 Different F_{OUT}

Temperature is +25°C unless otherwise specified. (Cont.)

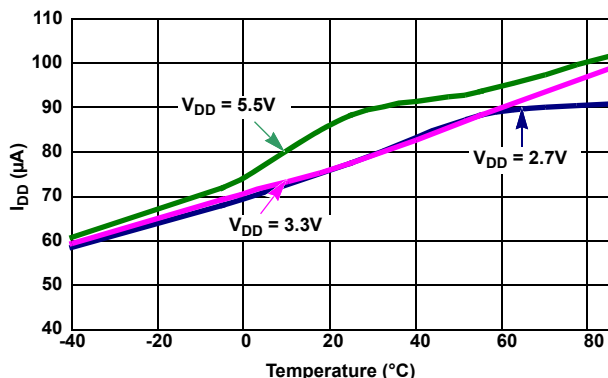


Figure 12. I_{DD} with TSE = 1 vs Temperature

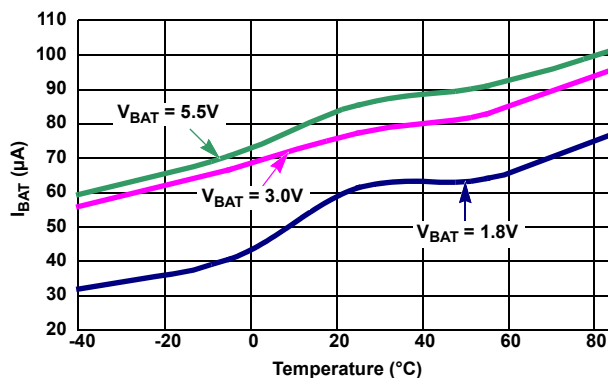


Figure 13. I_{BAT} with TSE = 1, BTSE = 1 vs Temperature

5. General Description

The ISL12022 device is a low power real time clock (RTCs) with embedded temperature sensors. It contains crystal frequency compensation circuitry over the operating temperature range, clock/calendar, power fail and low battery monitors, brownout indicator, 1 periodic or polled alarm, intelligent battery-backup switching and 128 Bytes of battery-backed user SRAM.

The oscillator uses an external, low cost 32.768kHz crystal. The real time clock tracks time with separate registers for hours, minutes and seconds. The device has calendar registers for date, month, year and day of the week. The calendar is accurate through 2099, with automatic leap year correction. In addition, the ISL12022 can be programmed for automatic Daylight Savings Time (DST) adjustment by entering local DST information.

The ISL12022's alarm can be set to any clock/calendar value for a match, for example, every minute, every Tuesday or at 5:23 AM on March 21. The alarm status is available by checking the Status Register, or the device can be configured to provide a hardware interrupt via the $\overline{IRQ}/F_{OUT}$ pin. There is a repeat mode for the alarm allowing a periodic interrupt every minute, every hour, every day, etc.

The device also offers a backup power input pin. This V_{BAT} pin allows the device to be backed up by battery or super capacitor with automatic switchover from V_{DD} to V_{BAT} . The ISL12022 device is specified for $V_{DD} = 2.7V$ to 5.5V and the clock/calendar portion of the device remains fully operational in battery-backup mode down to 1.8V (Standby Mode). The V_{BAT} level is monitored and reported against preselected levels. The first report is registered when the V_{BAT} level falls below 85% of nominal level, the second level is set for 75%. Battery levels are stored in PWR_VBAT registers.

The ISL12022 offers a Brownout alarm once the V_{DD} falls below a pre-selected trip level. This allows system Micro to save vital information to memory before complete power loss. There are six V_{DD} levels that could be selected for initiation of the Brownout alarm.

6. Pin Descriptions

6.1 X1, X2

The X1 and X2 pins are the input and output, respectively, of an inverting amplifier. An external 32.768kHz quartz crystal is used with the device to supply a timebase for the real time clock. Internal compensation circuitry with internal temperature sensor provides frequency corrections for selected popular crystals to ± 5 ppm over the operating temperature range from -40°C to $+85^{\circ}\text{C}$. (See [Applications Information](#) for recommended crystal). The ISL12022 allows the user to input via I²C serial bus the temperature variation profile of an individual crystal. The oscillator compensation network can also be used to calibrate the initial crystal timing accuracy to less than 1ppm error at room temperature. The device can also be driven directly from a 32.768kHz source at pin X1.

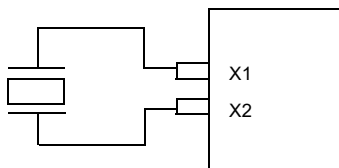


Figure 14. Recommended Crystal Connection

6.2 V_{BAT}

This input provides a backup supply voltage to the device. V_{BAT} supplies power to the device in the event that the V_{DD} supply fails. Device power will automatically switch to the V_{BAT} input when V_{DD} drops below the switchover trip level (V_{TRIP}). This pin can be connected to a battery, a super capacitor or tied to ground if not used.

6.3 $\overline{\text{IRQ}}/\text{F}_{\text{OUT}}$ (Interrupt Output/Frequency Output)

This dual function pin can be used as an interrupt or frequency output pin. The $\overline{\text{IRQ}}/\text{F}_{\text{OUT}}$ mode is selected via the frequency out control bits of the control/status register. It is an open-drain output.

- **Interrupt Mode.** The pin provides an interrupt signal output. This signal notifies a host processor that an alarm has occurred and requests action. It is an active low output.
- **Frequency Output Mode.** The pin outputs a clock signal, which is related to the crystal frequency. The frequency is user selectable and enabled via the I²C bus.

6.4 Serial Clock (SCL)

The SCL input is used to clock all serial data into and out of the device. The input buffer on this pin is always active (not gated). It is disabled when the backup power supply on the V_{BAT} pin is activated to minimize power consumption.

6.5 Serial Data (SDA)

SDA is a bi-directional pin used to transfer data into and out of the device. It has an open drain output and may be ORed with other open drain or open collector outputs. The input buffer is always active (not gated) in normal mode.

An open drain output requires the use of a pull-up resistor. The output circuitry controls the fall time of the output signal with the use of a slope controlled pull-down. The circuit is designed for 400kHz I²C interface speeds. It is disabled when the backup power supply on the V_{BAT} pin is activated.

6.6 V_{DD} , GND

Chip power supply and ground pins. The device will operate with a power supply from $V_{DD} = 2.7V$ to $5.5VDC$. A $0.1\mu F$ capacitor is recommended on the V_{DD} pin to ground. The V_{DD} Negative and V_{DD} Positive Slew Rate specifications have to be observed.

7. Functional Description

7.1 Power Control Operation

The power control circuit accepts a V_{DD} and a V_{BAT} input. Many types of batteries can be used with Renesas RTC products. For example, 3.0V or 3.6V Lithium batteries are appropriate, and battery sizes are available that can power the ISL12022 for up to 10 years. Another option is to use a super capacitor for applications where V_{DD} is interrupted for up to a month. See the [Applications Information](#) for more information.

7.2 Normal Mode (V_{DD}) to Battery-Backup Mode (V_{BAT})

To transition from the V_{DD} to V_{BAT} mode, both of the following conditions must be met:

- Condition 1: $V_{DD} < V_{BAT} - V_{BATHYS}$ where $V_{BATHYS} \approx 50mV$
- Condition 2: $V_{DD} < V_{TRIP}$ where $V_{TRIP} \approx 2.2V$

7.3 Battery-Backup Mode (V_{BAT}) to Normal Mode (V_{DD})

The ISL12022 device will switch from the V_{BAT} to V_{DD} mode when one of the following conditions occurs:

- Condition 1: $V_{DD} > V_{BAT} + V_{BATHYS}$ where $V_{BATHYS} \approx 50mV$
- Condition 2: $V_{DD} > V_{TRIP} + V_{TRIPHS}$ where $V_{TRIPHS} \approx 30mV$

These power control situations are illustrated in [Figure 15](#) and [Figure 16](#).

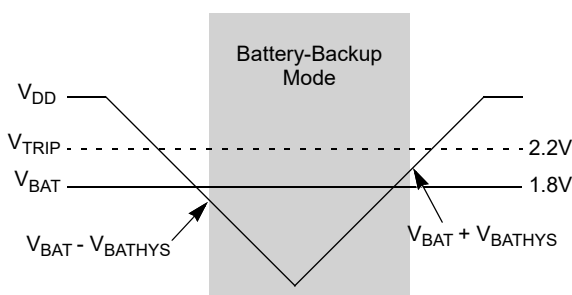


Figure 15. Battery Switchover when $V_{BAT} < V_{TRIP}$

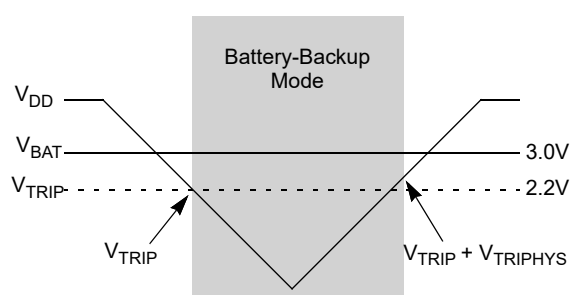


Figure 16. Battery Switchover when $V_{BAT} > V_{TRIP}$

The I²C bus is deactivated in battery-backup mode to reduce power consumption. Aside from this, all RTC functions are operational during battery-backup mode. Except for SCL and SDA, all the inputs and outputs of the ISL12022 are active during battery-backup mode unless disabled via the control register.

The device Time Stamps the switchover from V_{DD} to V_{BAT} and V_{BAT} to V_{DD} , and the time is stored in t_{SV2B} and t_{SB2V} registers respectively. If multiple V_{DD} power-down sequences occur before status is read, the earliest V_{DD} to V_{BAT} power-down time is stored and the most recent V_{BAT} to V_{DD} time is stored.

Temperature conversion and compensation can be enabled in battery-backup mode. Bit BTSE in the BETA register controls this operation, as described in [BETA Register \(BETA\)](#).

7.4 Power Failure Detection

The ISL12022 provides a Real Time Clock Failure Bit (RTCF) to detect total power failure. It allows users to determine if the device has powered up after having lost all power to the device (both V_{DD} and V_{BAT}).

7.5 Brownout Detection

The ISL12022 monitors the V_{DD} level continuously and provides warning if the V_{DD} level drops below prescribed levels. There are six (6) levels that can be selected for the trip level. For the values refer to [Table 6](#). Trips are 85% of nominal values. The LVDD bit in the Status Register is set to "1" when brownout is detected. Note that the I²C serial bus remains active unless the Battery V_{TRIP} levels are reached.

7.6 Battery Level Monitor

The ISL12022 has a built in warning feature once the Back-up battery level drops first to 85% and then to 75% of the battery's nominal V_{BAT} level. When the battery voltage drops to between 85% and 75%, the LBAT85 bit is set in the status register. When the level drops below 75%, both LBAT85 and LBAT75 bits are set in the status register.

The battery level monitor is not functional in battery backup mode. In order to read the monitor bits after powering up V_{DD} , instigate a battery level measurement by setting the TSE bit to "1" (BETA register), and then read the bits.

There is a Battery Time Stamp Function available. Once the V_{DD} is low enough to enable switchover to the battery, the RTC time/date are written into the TSV2B register. This information can be read from the TSV2B registers to discover the point in time of the V_{DD} power-down. If there are multiple power-down cycles before reading these registers, the first values stored in these registers will be retained. These registers will hold the original power-down value until they are cleared by setting CLRTS = 1 to clear the registers.

The normal power switching of the ISL12022 is designed to switch into battery-backup mode only if the V_{DD} power is lost. This will ensure that the device can accept a wide range of backup voltages from many types of sources while reliably switching into backup mode.

Note that the ISL12022 is not guaranteed to operate with $V_{BAT} < 1.8V$. If the battery voltage is expected to drop lower than this minimum, correct operation of the device, especially after a V_{DD} power-down cycle, is not guaranteed.

The minimum V_{BAT} to insure SRAM is stable is 1.0V. Below that, the SRAM may be corrupted when V_{DD} power resumes.

8. Real Time Clock Operation

The Real Time Clock (RTC) uses an external 32.768kHz quartz crystal to maintain an accurate internal representation of second, minute, hour, day of week, date, month, and year. The RTC also has leap-year correction. The clock also corrects for months having fewer than 31 days and has a bit that controls 24-hour or AM/PM format. When the ISL12022 powers up after the loss of both V_{DD} and V_{BAT} , the clock will not begin incrementing until at least one byte is written to the clock register.

8.1 Single Event and Interrupt

The alarm mode is enabled via the MSB bit. Choosing single event or interrupt alarm mode is selected via the IM bit. Note that when the frequency output function is enabled, the alarm function is disabled.

The standard alarm allows for alarms of time, date, day of the week, month, and year. When a time alarm occurs in single event mode, the $\overline{IRQ}/F_{OUT}$ pin will be pulled low and the alarm status bit (ALM) will be set to "1".

The pulsed interrupt mode allows for repetitive or recurring alarm functionality. Hence, once the alarm is set, the device will continue to alarm for each occurring match of the alarm and present time. Thus, it will alarm as often as

every minute (if only the nth second is set) or as infrequently as once a year (if at least the nth month is set). During pulsed interrupt mode, the $\overline{\text{IRQ}}/\text{F}_{\text{OUT}}$ pin will be pulled low for 250ms and the alarm status bit (ALM) will be set to “1”.

The ALM bit can be reset by the user or cleared automatically using the auto reset mode (see ARST bit). The alarm function can be enabled/disabled during battery-backup mode using the FOBATB bit. For more information on the alarm, please see [ALARM Registers \(10h to 15h\)](#).

8.2 Frequency Output Mode

The ISL12022 has the option to provide a clock output signal using the $\overline{\text{IRQ}}/\text{F}_{\text{OUT}}$ open drain output pin. The frequency output mode is set by using the FO bits to select 15 possible output frequency values from 1/32Hz to 32kHz. The frequency output can be enabled/disabled during battery-backup mode using the FOBATB bit.

8.3 General Purpose User SRAM

The ISL12022 provides 128 bytes of user SRAM. The SRAM will continue to operate in battery-backup mode. However, it should be noted that the I²C bus is disabled in battery-backup mode.

8.4 I²C Serial Interface

The ISL12022 has an I²C serial bus interface that provides access to the control and status registers and the user SRAM. The I²C serial interface is compatible with other industry I²C serial bus protocols using a bi-directional data signal (SDA) and a clock signal (SCL).

8.5 Oscillator Compensation

The ISL12022 provides both initial timing correction and temperature correction due to variation of the crystal oscillator. Analog and digital trimming control is provided for initial adjustment, and a temperature compensation function is provided to automatically correct for temperature drift of the crystal. Initial values are preset and recalled on initial power-up for the Initial AT and DT settings (IATR, IDTR), temperature coefficient (ALPHA), crystal capacitance (BETA), and the crystal turn-over temperature (XTO). These initial values are typical of units available on the market, although the user may program specific values after testing for best accuracy. The function can be enabled/disabled at any time and can be used in battery mode as well.

9. Register Descriptions

The battery-backed registers are accessible following a slave byte of “1101111x” and reads or writes to addresses [00h:2Fh]. The defined addresses and default values are described in the [Table 1](#). The battery backed general purpose SRAM has a different slave address (1010111x), so it is not possible to read/write that section of memory while accessing the registers.

Table 1. Register Memory Map

Addr.	Section	Reg Name	Bit								Range	Default
			7	6	5	4	3	2	1	0		
00h	RTC	SC	0	SC22	SC21	SC20	SC13	SC12	SC11	SC10	0 to 59	00h
01h		MN	0	MN22	MN21	MN20	MN13	MN12	MN11	MN10	0 to 59	00h
02h		HR	MIL	0	HR21	HR20	HR13	HR12	HR11	HR10	0 to 23	00h
03h		DT	0	0	DT21	DT20	DT13	DT12	DT11	DT10	1 to 31	01h
04h		MO	0	0	0	MO20	MO13	MO12	MO11	MO10	1 to 12	01h
05h		YR	YR23	YR22	YR21	YR20	YR13	YR12	YR11	YR10	0 to 99	00h
06h		DW	0	0	0	0	0	DW2	DW1	DW0	0 to 6	00h

Table 1. Register Memory Map (Cont.)

Addr.	Section	Reg Name	Bit								Range	Default
			7	6	5	4	3	2	1	0		
07h	CSR	SR	BUSY	OSCF	DSTADJ	ALM	LVDD	LBAT85	LBAT75	RTCF	N/A	01h
08h		INT	ARST	WRTC	IM	FOBATB	FO3	FO2	FO1	FO0	N/A	01h
09h		PWR_VD D	CLRTS	D	D	D	D	V _{DD} Trip2	V _{DD} Trip1	V _{DD} Trip0	N/A	00h
0Ah		PWR_VB AT		RESEAL B	VB85Tp2	VB85Tp1	VB85Tp0	VB75Tp2	VB75Tp1	VB75Tp0	N/A	00h
0Bh		ITRO	IDTR01	IDTR00	IATR05	IATR04	IATR03	IATR02	IATR01	IATR00	N/A	20h
0Ch		ALPHA	D	ALPHA6	ALPHA5	ALPHA4	ALPHA3	ALPHA2	ALPHA1	ALPHA0	N/A	46h
0Dh		BETA	TSE	BTSE	BTSR	BETA4	BETA3	BETA2	BETA1	BETA0	N/A	00h
0Eh		FATR	0	0	FFATR5	FATR4	FATR3	FATR2	FATR1	FATR0	N/A	00h
0Fh		FDTR	0	0	0	FDTR4	FDTR3	FDTR2	FDTR1	FDTR0	N/A	00h
10h	ALARM	SCA0	ESCA0	SCA022	SCA021	SCA020	SCA013	SCA012	SCA011	SCA010	00 to 59	00h
11h		MNA0	EMNA0	MNA022	MNA021	MNA020	MNA013	MNA012	MNA011	MNA010	00 to 59	00h
12h		HRA0	EHRA0	D	HRA021	HRA020	HRA013	HRA012	HRA011	HRA010	0 to 23	00h
13h		DTA0	EDTA0	D	DTA021	DTA020	DTA013	DTA012	DTA011	DTA010	01 to 31	00h
14h		MOA0	EMOA0 0	D	D	MOA020	MOA013	MOA012	MOA011	MOA010	01 to 12	00h
15h		DWA0	EDWA 0	D	D	D	D	DWA02	DWA01	DWA00	0 to 6	00h
16h	TSV2B	VSC	0	VSC22	VSC21	VSC20	VSC13	VSC12	VSC11	VSC10	0 to 59	00h
17h		VMN	0	VMN22	VMN21	VMN20	VMN13	VMN12	VMN11	VMN10	0 to 59	00h
18h		VHR	VMIL	0	VHR21	VHR20	VHR13	VHR12	VHR11	VHR10	0 to 23	00h
19h		VDT	0	0	VDT21	VDT20	VDT13	VDT12	VDT11	VDT10	1 to 31	00h
1Ah		VMO	0	0	0	VMO20	VMO13	VMO12	VMO11	VMO10	1 to 12	00h
1Bh	TSB2V	BSC	0	BSC22	BSC21	BSC20	BSC13	BSC12	BSC11	BSC10	0 to 59	00h
1Ch		BMN	0	BMN22	BMN21	BMN20	BMN13	BMN12	BMN11	BMN10	0 to 59	00h
1Dh		BHR	BMIL	0	BHR21	BHR20	BHR13	BHR12	BHR11	BHR10	0 to 23	00h
1Eh		BDT	0	0	BDT21	BDT20	BDT13	BDT12	BDT11	BDT10	1 to 31	00h
1Fh		BMO	0	0	0	BMO20	BMO13	BMO12	BMO11	BMO10	1 to 12	00h
20h	DSTCR	DstMoFd	DSTE	D	D	DstMoFd20	DstMoFd1 3	DstMoFd1 2	DstMoFd1 1	DstMoFd1 0	1 to 12	00h
21h		DstDwFd	D	DstDwFd E	DstWkFd1 2	DstWkFd11	DstWkFd1 0	DstDwFd1 2	DstDwFd1 1	DstDwFd1 0	0 to 6	00h
22h		DstDtFd	D	D	DstDtFd2 1	DstDtFd20	DstDtFd13	DstDtFd12	DstDtFd11	DstDtFd10	1 to 31	00h
23h		DstHrFd	D	D	DstHrFd2 1	DstHrFd20	DstHrFd13	DstHrFd12	DstHrFd11	DstHrFd10	0 to 23	00h
24h		DstMoRv	D	D	D	XDstMoRv2 0	DstMoRv1 3	DstMoR12 v	DstMoRv1 1	DstMoRv1 0	01 to 12	00h
25h		DstDwRv	D	DstDwRv E	DstWkRv1 2	DstWkRv11	DstWkRv1 0	DstDwRv1 2	DstDwRv1 1	DstDwRv1 0	0 to 6	00h
26h		DstDtRv	D	D	DstDtRv2 1	DstDtRv20	DstDtRv13	DstDtRv12	DstDtRv11	DstDtRv10	01 to 31	00h
27h		DstHrRv	D	D	DstHrRv2 1	DstHrRv20	DstHrRv13	DstHrRv12	DstHrRv11	DstHrRv10	0 to 23	00h
28h	TEMP	TK0L	TK07	TK06	TK05	TK04	TK03	TK02	TK01	TK00	00 to FF	00h
29h		TK0M	0	0	0	0	0	0	TK09	TK08	00 to 03	00h

Table 1. Register Memory Map (Cont.)

Addr.	Section	Reg Name	Bit								Range	Default
			7	6	5	4	3	2	1	0		
2Ah	NPPM	NPPML	NPPM7	NPPM6	NPPM5	NPPM4	NPPM3	NPPM2	NPPM1	NPPM0	00 to FF	00h
2Bh		NPPMH	0	0	0	0	0	NPPM10	NPPM9	NPPM8	00 to 07	00h
2Ch	XT0	XT0	D	D	D	XT4	XT3	XT2	XT1	XT0	00 to FF	00h
2Dh	ALPHA_H	ALPHAH	D	ALP_H6	ALP_H5	ALP_H4	ALP_H3	ALP_H2	ALP_H1	ALP_H0	00 to 7F	46h
2Eh	GPM	GPM1	GPM17	GPM16	GPM15	GPM14	GPM13	GPM12	GPM11	GPM10	00 to FF	00h
2Fh		GPM2	GPM27	GPM26	GPM25	GPM24	GPM23	GPM22	GPM21	GPM20	00 to FF	00h

9.0.1 Register Access

The contents of the registers can be modified by performing a byte or a page write operation directly to any register address.

The registers are divided into 11 sections. They are:

- Real Time Clock (7 bytes): Address 00h to 06h.
- Control and Status (9 bytes): Address 07h to 0Fh.
- Alarm (6 bytes): Address 10h to 15h.
- Time Stamp for Battery Status (5 bytes): Address 16h to 1Ah.
- Time Stamp for V_{DD} Status (5 bytes): Address 1Bh to 1Fh.
- Daylight Savings Time (8 bytes): 20h to 27h.
- TEMP (2 bytes): 28h to 29h
- Crystal Net PPM Correction, NPPM (2 bytes): 2Ah, 2Bh
- Crystal Turnover Temperature, XT0 (1 byte): 2Ch
- Crystal ALPHA at high temperature, ALPHA_H (1 byte): 2Dh
- Scratch Pad (2 bytes): Address 2Eh and 2Fh

Write capability is allowable into the RTC registers (00h to 06h) only when the WRTC bit (Bit[6] of address 08h) is set to "1". A multi-byte read or write operation should be limited to one section per operation for best RTC time keeping performance.

A register can be read by performing a random read at any address at any time. This returns the contents of that register location. Additional registers are read by performing a sequential read. For the RTC and Alarm registers, the read instruction latches all clock registers into a buffer, so an update of the clock does not change the time being read. At the end of a read, the master supplies a stop condition to end the operation and free the bus. After a read, the address remains at the previous address +1 so the user can execute a current address read and continue reading the next register. When the previous address is 2Fh, the next address will wrap around to 00h.

It is not necessary to set the WRTC bit prior to writing into the control and status, alarm, and user SRAM registers.

10. Real Time Clock Registers

10.1 Addresses [00h to 06h]

10.1.1 RTC Registers (SC, MN, HR, DT, MO, YR, DW)

These registers depict BCD representations of the time. As such, SC (Seconds) and MN (Minutes) range from 0 to 59, HR (Hour) can either be a 12-hour or 24-hour mode, DT (Date) is 1 to 31, MO (Month) is 1 to 12, YR (Year) is 0 to 99, and DW (Day of the Week) is 0 to 6.

The DW register provides a Day of the Week status and uses three bits DW2 to DW0 to represent the seven days of the week. The counter advances in the cycle 0-1-2-3-4-5-6-0-1-2-... The assignment of a numerical value to a specific day of the week is arbitrary and may be decided by the system software designer. The default value is defined as "0".

10.1.2 24 Hour Time

If the MIL bit of the HR register is "1", the RTC uses a 24-hour format. If the MIL bit is "0", the RTC uses a 12-hour format and HR21 bit functions as an AM/PM indicator with a "1" representing PM. The clock defaults to 12-hour format time with HR21 = "0".

10.1.3 Leap Years

Leap years add the day February 29 and are defined as those years that are divisible by 4. Years divisible by 100 are not leap years, unless they are also divisible by 400. This means that the year 2000 is a leap year and the year 2100 is not. The ISL12022 does not correct for the leap year in the year 2100.

11. Control and Status Registers (CSR)

11.1 Addresses [07h to 0Fh]

The Control and Status Registers consist of the Status Register, Interrupt and Alarm Register, Analog Trimming and Digital Trimming Registers.

11.2 Status Register (SR)

The Status Register is located in the memory map at address 07h. This is a volatile register that provides either control or status of RTC failure (RTCF), Battery Level Monitor (LBAT85, LBAT75), alarm trigger, Daylight Savings Time, crystal oscillator enable and temperature conversion in progress bit.

Table 2. Status Register (SR)

ADDR	7	6	5	4	3	2	1	0
07h	BUSY	OSCF	DSTADJ	ALM	LVDD	LBAT85	LBAT75	RTCF

11.2.1 Busy Bit (BUSY)

Busy Bit indicates temperature sensing is in progress. In this mode, Alpha, Beta and ITRO registers are disabled and cannot be accessed.

11.2.2 Oscillator Fail Bit (OSCF)

Oscillator Fail Bit indicates that the oscillator has failed. The oscillator frequency is either zero or very far from the desired 32.768kHz due to failure, PC board contamination or mechanical issues.

11.2.3 Daylight Savings Time Change Bit (DSTADJ)

DSTADJ is the Daylight Savings Time Adjusted Bit. It indicates the daylight saving time forward adjustment has happened. If a DST Forward event happens, DSTADJ will be set to "1". The DSTADJ bit will stay high after the

DSTFD event happens, and will be reset to “0” when the DST Reverse event happens. It is read-only and cannot be written. Setting time during a DST forward period will not set this bit to “1”.

The DSTE bit must be enabled when the RTC time is more than one hour before the DST Forward or DST Reverse event time setting, or the DST event correction will not happen.

DSTADJ is reset to “0” upon power-up. It will reset to “0” when the DSTE bit in Register 15h is set to “0” (DST disabled), but no time adjustment will happen.

11.2.4 Alarm Bit (ALM)

This bit announces if the alarm matches the real time clock. If there is a match, the respective bit is set to “1”. This bit can be manually reset to “0” by the user or automatically reset by enabling the auto-reset bit (see ARST bit). A write to this bit in the SR can only set it to “0”, not “1”. An alarm bit that is set by an alarm occurring during an SR read operation will remain set after the read operation is complete.

11.2.5 Low V_{DD} Indicator Bit (LVDD)

This bit indicates when V_{DD} has dropped below the pre-selected trip level (Brownout Mode). The trip points for the brownout levels are selected by three bits: VDD Trip2, VDD Trip1 and VDD Trip0 in PWR_ VDD registers. The LVDD detection is only enabled in VDD mode and the detection happens in real time. The LVDD bit is set whenever the V_{DD} has dropped below the pre-selected trip level, and self clears whenever the V_{DD} is above the pre-selected trip level.

11.2.6 Low Battery Indicator 85% Bit (LBAT85)

In Normal Mode (V_{DD}), this bit indicates when the battery level has dropped below the pre-selected trip levels. The trip points are selected by three bits: VB85Tp2, VB85Tp1 and VB85Tp0 in the PWR_VBAT registers. The LBAT85 detection happens automatically once every minute when seconds register reaches 59. The detection can also be manually triggered by setting the TSE bit in BETA register to “1”. The LBAT85 bit is set when the V_{BAT} has dropped below the pre-selected trip level, and will self clear when the V_{BAT} is above the pre-selected trip level at the next detection cycle either by manual or automatic trigger.

In Battery Mode (V_{BAT}), this bit indicates the device has entered into battery mode by polling once every 10 minutes. The LBAT85 detection happens automatically once when the minute register reaches x9h or x0h minutes.

11.2.6.1 Example - LBAT85 is Set To “1” In Battery Mode:

The minute the register changes to 19h when the device is in battery mode, the LBAT85 is set to “1” the next time the device switches back to Normal Mode.

11.2.6.2 Example - LBAT85 Remains at “0” In Battery Mode:

If the device enters into battery mode after the minute register reaches 20h and switches back to Normal Mode before the minute register reaches 29h, then the LBAT85 bit will remain at “0” the next time the device switches back to Normal Mode.

11.2.7 Low Battery Indicator 75% Bit (LBAT75)

In Normal Mode (V_{DD}), this bit indicates when the battery level has dropped below the pre-selected trip levels. The trip points are selected by three bits: VB75Tp2, VB75Tp1, and VB75Tp0 in the PWR_VBAT registers. The LBAT75 detection happens automatically once every minute when seconds register reaches 59. The detection can also be manually triggered by setting the TSE bit in BETA register to “1”. The LBAT75 bit is set when the V_{BAT} has dropped below the pre-selected trip level, and will self clear when the V_{BAT} is above the pre-selected trip level at the next detection cycle either by manual or automatic trigger.

In Battery Mode (V_{BAT}), this bit indicates the device has entered into battery mode by polling once every 10 minutes. The LBAT75 detection happens automatically once when the minute register reaches x9h or x0h minutes.

11.2.7.1 Example - LBAT75 is Set to “1” in Battery Mode:

The minute register changes to 30h when the device is in battery mode, the LBAT75 is set to “1” the next time the device switches back to Normal Mode.

11.2.7.2 Example - LBAT75 Remains at “0” in Battery Mode:

If the device enters into battery mode after the minute register reaches 49h and switches back to Normal Mode before minute register reaches 50h, then the LBAT75 bit will remain at “0” the next time the device switches back to Normal Mode.

11.2.8 Real Time Clock Fail Bit (RTCF)

This bit is set to a “1” after a total power failure. This is a read only bit that is set by hardware (ISL12022 internally) when the device powers up after having lost all power (defined as $V_{DD} = 0V$ and $V_{BAT} = 0V$). The bit is set regardless of whether V_{DD} or V_{BAT} is applied first. The loss of only one of the supplies does not set the RTCF bit to “1”. The first valid write to the RTC section after a complete power failure resets the RTCF bit to “0” (writing one byte is sufficient).

11.3 Interrupt Control Register (INT)

Table 3. Interrupt Control Register (INT)

ADDR	7	6	5	4	3	2	1	0
08h	ARST	WRTC	IM	FOBATB	FO3	FO2	FO1	FO0

11.3.1 Automatic Reset bit (ARST)

This bit enables/disables the automatic reset of the ALM, LVDD, LBAT85, and LBAT75 status bits only. When ARST bit is set to “1”, these status bits are reset to “0” after a valid read of the respective status register (with a valid STOP condition). When the ARST is cleared to “0”, the user must manually reset the ALM, LVDD, LBAT85, and LBAT75 bits.

11.3.2 Write RTC Enable Bit (WRTC)

The WRTC bit enables or disables write capability into the RTC Timing Registers. The factory default setting of this bit is “0”. Upon initialization or power-up, the WRTC must be set to “1” to enable the RTC. Upon the completion of a valid write (STOP), the RTC starts counting. The RTC internal 1Hz signal is synchronized to the STOP condition during a valid write cycle.

11.3.3 Interrupt/Alarm Mode Bit (IM)

This bit enables/disables the interrupt mode of the alarm function. When the IM bit is set to “1”, the alarm operates in the interrupt mode, where an active low pulse width of 250ms appears at the $\overline{IRQ}/F_{OUT}$ pin when the RTC is triggered by the alarm, as defined by the alarm registers (10h to 15h). When the IM bit is cleared to “0”, the alarm operates in standard mode, where the $\overline{IRQ}/F_{OUT}$ pin is set low until the ALM status bit is cleared to “0”.

IM Bit	Interrupt/Alarm FREQUENCY
0	Single Time Event Set By Alarm
1	Repetitive/Recurring Time Event Set By Alarm

11.3.4 Frequency Output and Interrupt Bit (FOBATB)

This bit enables/disables the $\overline{IRQ}/F_{OUT}$ pin during battery-backup mode (i.e., V_{BAT} power source active). When the FOBATB is set to “1”, the $\overline{IRQ}/F_{OUT}$ pin is disabled during battery-backup mode. This means that both the frequency output and alarm output functions are disabled. When the FOBATB is cleared to “0”, the $\overline{IRQ}/F_{OUT}$ pin is enabled during battery-backup mode. Note that the open drain $\overline{IRQ}/F_{OUT}$ pin will need a pull-up to the battery voltage to operate in battery-backup mode.

11.3.5 Frequency Out Control Bits (FO[3:0])

These bits enable/disable the frequency output function and select the output frequency at the $\overline{\text{IRQ}}/\text{F}_{\text{OUT}}$ pin. See [Table 4](#) for frequency selection. Default for the ISL12022 is FO[3:0] = 1h, or 32.768kHz output. When the frequency mode is enabled, it will override the alarm mode at the $\overline{\text{IRQ}}/\text{F}_{\text{OUT}}$ pin.

Table 4. Frequency Selection of $\overline{\text{IRQ}}/\text{F}_{\text{OUT}}$ Pin

Frequency, F_{OUT}	Units	FO3	FO2	FO1	FO0
0	Hz	0	0	0	0
32768	Hz	0	0	0	1
4096	Hz	0	0	1	0
1024	Hz	0	0	1	1
64	Hz	0	1	0	0
32	Hz	0	1	0	1
16	Hz	0	1	1	0
8	Hz	0	1	1	1
4	Hz	1	0	0	0
2	Hz	1	0	0	1
1	Hz	1	0	1	0
1/2	Hz	1	0	1	1
1/4	Hz	1	1	0	0
1/8	Hz	1	1	0	1
1/16	Hz	1	1	1	0
1/32	Hz	1	1	1	1

11.3.6 Power Supply Control Register (PWR_VDD)

TABLE 5. Clear Time Stamp Bit (CLRTS)

ADDR	7	6	5	4	3	2	1	0
09h	CLRTS	0	0	0	0	$\text{V}_{\text{DD}}\text{Trip2}$	$\text{V}_{\text{DD}}\text{Trip1}$	$\text{V}_{\text{DD}}\text{Trip0}$

This bit clears Time Stamp V_{DD} to Battery (TSV2B) and Time Stamp Battery to V_{DD} Registers (TSB2V). The default setting is 0 (CLRTS = 0) and the Enabled setting is 1 (CLRTS = 1).

11.4 V_{DD} Brownout Trip Voltage BITS ($\text{V}_{\text{DD}}\text{Trip}[2:0]$)

These bits set the six trip levels for the V_{DD} alarm, indicating that V_{DD} has dropped below a preset level. In this event, the LVDD bit in the Status Register is set to "1". See [Table 6](#).

Table 6. V_{DD} Trip Levels

$\text{V}_{\text{DD}}\text{Trip2}$	$\text{V}_{\text{DD}}\text{Trip1}$	$\text{V}_{\text{DD}}\text{Trip0}$	Trip Voltage (V)
0	0	0	2.295
0	0	1	2.550
0	1	0	2.805
0	1	1	3.060
1	0	0	4.250
1	0	1	4.675

11.5 Battery Voltage Trip Voltage Register (PWR_VBAT)

This register controls the trip points for the two V_{BAT} alarms, with levels set to approximately 85% and 75% of the nominal battery level.

ADDR	7	6	5	4	3	2	1	0
0Ah	D	RESEALB	VB85Tp2	VB85Tp1	VB85Tp0	VB75Tp2	VB75Tp1	VB75Tp0

11.5.1 Reseal Bit (RESEALB)

This is the Reseal bit for actively disconnecting V_{BAT} pin from the internal circuitry. Setting this bit allows the device to disconnect the battery and eliminate standby current drain while the device is unused. Once V_{DD} is powered up, this bit is reset and the V_{BAT} pin is then connected to the internal circuitry.

The application for this bit involves placing the chip on a board with a battery and testing the board. Once the board is tested and ready to ship, it is desirable to disconnect the battery to keep it fresh until the board or unit is placed into final use. Setting RESEALB = “1” initiates the battery disconnect, and after V_{DD} power is cycled down and up again, the RESEAL bit is cleared to “0”.

11.5.2 Battery Level Monitor Trip Bits (VB85TP[2:0])

Three bits select the first alarm (85% of Nominal V_{BAT}) level for the battery voltage monitor. There are total of 7 levels that could be selected for the first alarm. Any of the of levels could be selected as the first alarm with no reference as to nominal Battery voltage level. See [Table 7](#).

Table 7. VB85T Alarm Level

VB85Tp2	VB85Tp1	VB85Tp0	Battery Alarm Trip Level (V)
0	0	0	2.125
0	0	1	2.295
0	1	0	2.550
0	1	1	2.805
1	0	0	3.060
1	0	1	4.250
1	1	0	4.675

11.5.3 Battery Level Monitor Trip Bits (VB75TP[2:0])

Three bits select the second alarm (75% of Nominal V_{BAT}) level for the battery voltage monitor. There are total of 7 levels that could be selected for the second alarm. Any of the of levels could be selected as the second alarm with no reference as to nominal Battery voltage level. See [Table 8](#).

Table 8. Battery Level Monitor Trip Bits (VB75TP[2:0])

VB75Tp2	VB75Tp1	VB75Tp0	Battery Alarm Trip Level (V)
0	0	0	1.875
0	0	1	2.025
0	1	0	2.250
0	1	1	2.475
1	0	0	2.700
1	0	1	3.750
1	1	0	4.125

11.6 Initial AT and DT Setting Register (ITRO)

These bits are used to trim the initial error (at room temperature) of the crystal. Both Digital Trimming (DT) and Analog Trimming (AT) methods are available. The digital trimming uses clock pulse skipping and insertion for frequency adjustment. Analog trimming uses load capacitance adjustment to pull the oscillator frequency. A range of +62.5ppm to -61.5ppm is possible with combined digital and analog trimming.

11.6.1 Aging and Initial Trim Digital Trimming Bits (IDTR0[1:0])

These bits allow ± 30.5 ppm initial trimming range for the crystal frequency. This is meant to be a coarse adjustment if the range needed is outside that of the IATR control. See [Table 9](#). The IDTR0 register should only be changed while the TSE (Temp Sense Enable) bit is "0".

Table 9. IDTR0 Trimming Range

IDTR01	IDTR00	Trimming Range
0	0	Default/Disabled
0	1	+30.5ppm
1	0	0ppm
1	1	-30.5ppm

11.6.2 Aging and Initial Analog Trimming Bits (IATR0 [5:0])

The analog trimming register allows +32ppm to -31ppm adjustment in 1ppm/bit increments. This enables fine frequency adjustment for trimming initial crystal accuracy error or to correct for aging drift. The IATR0 register should only be changed while the TSE (Temp Sense Enable) bit is "0".

Table 10. Initial AT and DT Setting Register

ADDR	7	6	5	4	3	2	1	0
0Bh	IDTR01	IDTR00	IATR05	IATR04	IATR03	IATR02	IATR01	IATR00

Aging adjustment is normally a few ppm and can be handled by writing to the IATR section.

Table 11. IATR0 Trimming Range

IATR05	IATR04	IATR03	IATR02	IATR01	IATR00	Trimming Range
0	0	0	0	0	0	+32
0	0	0	0	0	1	+31
0	0	0	0	1	0	+30
0	0	0	0	1	1	+29
0	0	0	1	0	0	+28
0	0	0	1	0	1	+27
0	0	0	1	1	0	+26
0	0	0	1	1	1	+25
0	0	1	0	0	0	+24
0	0	1	0	0	1	+23
0	0	1	0	1	0	+22
0	0	1	0	1	1	+21
0	0	1	1	0	0	+20
0	0	1	1	0	1	+19
0	0	1	1	1	0	+18
0	0	1	1	1	1	+17
0	1	0	0	0	0	+16

Table 11. IATR0 Trimming Range (Cont.)

IATR05	IATR04	IATR03	IATR02	IATR01	IATR00	Trimming Range
0	1	0	0	0	1	+15
0	1	0	0	1	0	+14
0	1	0	0	1	1	+13
0	1	0	1	0	0	+12
0	1	0	1	0	1	+11
0	1	0	1	1	0	+10
0	1	0	1	1	1	+9
0	1	1	0	0	0	+8
0	1	1	0	0	1	+7
0	1	1	0	1	0	+6
0	1	1	0	1	1	+5
0	1	1	1	0	0	+4
0	1	1	1	0	1	+3
0	1	1	1	1	0	+2
0	1	1	1	1	1	+1
1	0	0	0	0	0	0
1	0	0	0	0	1	-1
1	0	0	0	1	0	-2
1	0	0	0	1	1	-3
1	0	0	1	0	0	-4
1	0	0	1	0	1	-5
1	0	0	1	1	0	-6
1	0	0	1	1	1	-7
1	0	1	0	0	0	-8
1	0	1	0	0	1	-9
1	0	1	0	1	0	-10
1	0	1	0	1	1	-11
1	0	1	1	0	0	-12
1	0	1	1	0	1	-13
1	0	1	1	1	0	-14
1	0	1	1	1	1	-15
1	1	0	0	0	0	-16
1	1	0	0	0	1	-17
1	1	0	0	1	0	-18
1	1	0	0	1	1	-19
1	1	0	1	0	0	-20
1	1	0	1	0	1	-21
1	1	0	1	1	0	-22
1	1	0	1	1	1	-23
1	1	1	0	0	0	-24
1	1	1	0	0	1	-25
1	1	1	0	1	0	-26
1	1	1	0	1	1	-27
1	1	1	1	0	0	-28

Table 11. IATR0 Trimming Range (Cont.)

IATR05	IATR04	IATR03	IATR02	IATR01	IATR00	Trimming Range
1	1	1	1	0	1	-29
1	1	1	1	1	0	-30
1	1	1	1	1	1	-31

Note that setting the IATR to the lowest settings (-31ppm) with the default 32kHz output can cause the oscillator frequency to become unstable on power-up. The lowest settings for IATR should be avoided to insure oscillator frequency integrity. If the lowest IATR settings are needed, then the user is advised to disable the F_{OUT} and enable again to insure placing the oscillator in a stable condition.

11.6.3 ALPHA Register (ALPHA)

Table 12. ALPHA Register

ADDR	7	6	5	4	3	2	1	0
0Ch	D	ALPHA6	ALPHA5	ALPHA4	ALPHA3	ALPHA2	ALPHA1	ALPHA0

The Alpha variable is 8 bits and is defined as the temperature coefficient of Crystal from -40°C to T₀, or the Alpha Cold (There is an Alpha Hot register that must be programmed as well). It is normally given in units of ppm/°C², with a typical value of -0.034. The ISL12022 device uses a scaled version of the absolute value of this coefficient in order to get an integer value. Therefore, Alpha[7:0] is defined as the (|Actual Alpha Value| x 2048) and converted to binary. For example, a crystal with Alpha of -0.034ppm/°C² is first scaled (|2048×(-0.034)| = 70d) and then converted to a binary number of 01000110b.

The practical range of Actual Alpha values is from -0.020 to -0.060.

The ALPHA register should only be changed while the TSE (Temp Sense Enable) bit is "0". Note that both the ALPHA and the ALPHA Hot registers need to be programmed with values for full range temperature compensation.

11.6.4 BETA Register (BETA)

Table 13. BETA Register

ADDR	7	6	5	4	3	2	1	0
0Dh	TSE	BTSE	BTSR	BETA4	BETA3	BETA2	BETA1	BETA0

11.6.5 Temperature Sensor Enabled Bit (TSE)

This bit enables the Temperature Sensing operation, including the temperature sensor, A/D converter and AT/DT register adjustment. The default mode after power-up is disabled (TSE = 0). To enable the operation, TSE should be set to 1 (TSE = 1). When the temperature sensor is disabled, the initial values for IATR and IDTR registers are used for frequency control.

All changes to the IDTR, IATR, ALPHA and BETA registers must be made with TSE = 0. After loading the new values, TSE can be enabled and the new values are used. When TSE is set to 1, the temperature conversion cycle begins and will end when two temperature conversions are completed. The average of the two conversions is in the TEMP registers. The total time for temperature sense and conversion is approximately 22ms from the time TSE = 1 write is completed.

11.6.6 Temp Sensor Conversion in Battery Mode Bit (BTSE)

This bit enables the Temperature Sensing and Correction in battery mode. BTSE = 0 (default) no conversion, Temp Sensing or Compensation in battery mode. BTSE = 1 indicates Temp Sensing and Compensation enabled in battery mode. The BTSE is disabled when the battery voltage is lower than 2.7V. No temperature compensation will take place with $V_{BAT} < 2.7V$.

11.6.7 Frequency of Temperature Sensing and Correction Bit (BTSR)

This bit controls the frequency of Temperature Sensing and Correction. BTSR = 0 default mode is every 10 minutes, BTSR = 1 is every 1.0 minute. Note that BTSE has to be enabled in both cases. See [Table 14](#).

Table 14. Frequency of Temperature Sensing and Correction Bit

BTSE	BTSR	TC Period in Battery Mode
0	0	OFF
0	1	OFF
1	0	10 Minutes
1	1	1 Minute

The temperature measurement conversion time is the same for battery mode as for V_{DD} mode, approximately 22ms. The battery mode current will increase during this conversion time to typically 68μA. The average increase in battery current is much lower than this due to the small duty cycle of the ON-time versus OFF-time for the conversion.

To figure the average increase in battery current, we take the change in current times the duty cycle. For the 1 minute temperature period the average current is shown in [Equation 1](#).

$$(EQ. 1) \quad \Delta I_{BAT} = \frac{0.022s}{60s} \times 68\mu A = 25nA$$

For the 10 minute temperature period the average current is shown in [Equation 2](#):

$$(EQ. 2) \quad \Delta I_{BAT} = \frac{0.022s}{600s} \times 68\mu A = 2.5nA$$

If the application has a stable temperature environment that doesn't change quickly, the 10 minute option will work well and the backup battery lifetime impact is minimized. If quick temperature variations are expected (multiple cycles of more than 10° within an hour), then the 1 minute option should be considered and the slightly higher battery current figured into overall battery life.

11.6.8 Gain Factor of AT BIT (BETA[4:0])

Beta is specified to take care of the C_m variations of the crystal. Most crystals specify C_m around 2.2fF. For example, if $C_m > 2.2fF$, the actual AT steps may reduce from 1ppm/step to approximately 0.80ppm/step. Beta is then used to adjust for this variation and restore the step size to 1ppm/step.

BETA values are limited in the range from 01000 to 11111 as shown in [Table 15](#). To use [Table 15](#), the device is tested at two AT settings as shown in [Equation 3](#):

$$(EQ. 3) \quad BETAVALUES = (AT(max) - AT(min))/63$$

where:

- AT(max) = F_{OUT} in ppm (at AT = 00H)
- AT(min) = F_{OUT} in ppm (at AT = 3FH)

The BETA VALUES result is indexed in the right hand column and the resulting Beta factor (for the register) is in the same row in the left column.

The value for BETA should only be changed while the TSE (Temperature Sense Enable) bit is "0". The procedure for writing the BETA register involves two steps. First, write the new value of BETA with TSE = 0. Then write the same value of BETA with TSE = 1. This will insure the next temperature sense cycle will use the new BETA value.

Table 15. BETA Values

BETA[4:0]	At Step Adjustment
01000	0.5000
00111	0.5625

Table 15. BETA Values (Cont.)

BETA[4:0]	At Step Adjustment
00110	0.6250
00101	0.6875
00100	0.7500
00011	0.8125
00010	0.8750
00001	0.9375
00000	1.0000
10000	1.0625
10001	1.1250
10010	1.1875
10011	1.2500
10100	1.3125
10101	1.3750
10110	1.4375
10111	1.5000
11000	1.5625
11001	1.6250
11010	1.6875
11011	1.7500
11100	1.8125
11101	1.8750
11110	1.9375
11111	2.0000

11.7 Final Analog Trimming Register (FATR)

This register shows the final setting of AT after temperature correction. It is read-only; the user cannot overwrite a value to this register. This value is accessible as a means of monitoring the temperature compensation function. See [Table 16](#).

Table 16. Final Analog Trimming Register

ADDR	7	6	5	4	3	2	1	0
0Eh	0	0	FATR5	FATR4	FATR3	FATR2	FATR1	FATR0

11.8 Final Digital Trimming Register (FDTR)

This Register shows the final setting of DT after temperature correction. It is read-only; the user cannot overwrite a value to this register. The value is accessible as a means of monitoring the temperature compensation function. The corresponding clock adjustment values are shown in [Table 18](#). The DT setting has both positive and negative settings to adjust for any offset in the crystal.

Table 17. Final Digital Trimming Register

ADDR	7	6	5	4	3	2	1	0
0Fh	0	0	0	FDTR4	FDTR3	FDTR2	FDTR1	FDTR0

Table 18. Clock Adjustment Values for Final Digital Trimming Register

FDTR[4:0]	Decimal	ppm Adjustment
00000	0	0
00001	1	30.5
00010	2	61
00011	3	91.5
00100	4	122
00101	5	152.5
00110	6	183
00111	7	213.5
01000	8	244
01001	9	274.5
01010	10	305
10000	0	0
10001	-1	-30.5
10010	-2	-61
10011	-3	-91.5
10100	-4	-122
10101	-5	-152.5
10110	-6	-183
10111	-7	-213.5
11000	-8	-244
11001	-9	-274.5
11010	-10	-305

11.9 ALARM Registers (10h to 15h)

The alarm register bytes are set up identical to the RTC register bytes, except that the MSB of each byte functions as an enable bit (enable = "1"). These enable bits specify which alarm registers (seconds, minutes, and so on) are used to make the comparison. *Note:* There is no alarm byte for year.

The alarm function works as a comparison between the alarm registers and the RTC registers. As the RTC advances, the alarm will be triggered once a match occurs between the alarm registers and the RTC registers. Any one alarm register, multiple registers, or all registers can be enabled for a match.

There are two alarm operation modes: Single Event and periodic Interrupt Mode:

- **Single Event Mode** is enabled by setting the Bit[7] on any of the Alarm registers (ESCA0... EDWA0) to "1", the IM bit to "0", and disabling the frequency output. This mode permits a one-time match between the Alarm registers and the RTC registers. When this match occurs, the ALM bit is set to "1" and the $\overline{\text{IRQ}}/\text{F}_{\text{OUT}}$ output is pulled low and remains low until the ALM bit is reset. This can be done manually or by using the auto-reset feature.
- **Interrupt Mode** is enabled by setting the Bit[7] on any of the Alarm registers (ESCA0... EDWA0) to "1", the IM bit to "1", and disabling the frequency output. The $\overline{\text{IRQ}}/\text{F}_{\text{OUT}}$ output is pulsed each time an alarm occurs. This means that when the interrupt mode alarm is set, it continues to alarm for each occurring match of the alarm and present time. This mode is convenient for hourly or daily hardware interrupts in microcontroller applications such as security cameras or utility meter reading.

To clear a single event alarm, the ALM bit in the status register must be set to "0" with a write. *Note:* If the ARST bit is set to 1 (address 08h, Bit[7]), the ALM bit automatically clears when the status register is read.

Following are examples of both Single Event and periodic Interrupt Mode alarms.

11.9.1 Example 1

- Alarm set with single interrupt (IM = "0")
- A single alarm occurs on January 1 at 11:30 a.m.
- Set Alarm registers as follows:

Alarm Register	Bit									Description
	7	6	5	4	3	2	1	0	Hex	
SCA0	0	0	0	0	0	0	0	0	00h	Seconds disabled
MNA0	1	0	1	1	0	0	0	0	B0h	Minutes set to 30, enabled
HRA0	1	0	0	1	0	0	0	1	91h	Hours set to 11, enabled
DTA0	1	0	0	0	0	0	0	1	81h	Date set to 1, enabled
MOA0	1	0	0	0	0	0	0	1	81h	Month set to 1, enabled
DWA0	0	0	0	0	0	0	0	0	00h	Day of week disabled

After these registers are set, an alarm is generated when the RTC advances to exactly 11:30 a.m. on January 1 (after seconds changes from 59 to 00) by setting the ALM bit in the status register to "1" and also bringing the $\overline{\text{IRQ}}/\text{F}_{\text{OUT}}$ output low.

11.9.2 Example 2

- Pulsed interrupt once per minute (IM = "1")
- Interrupts at one minute intervals when the seconds register is at 30s.
- Set Alarm registers as follows:

Alarm Register	Bit									Description
	7	6	5	4	3	2	1	0	Hex	
SCA0	1	0	1	1	0	0	0	0	B0h	Seconds set to 30, enabled
MNA0	0	0	0	0	0	0	0	0	00h	Minutes disabled
HRA0	0	0	0	0	0	0	0	0	00h	Hours disabled
DTA0	0	0	0	0	0	0	0	0	00h	Date disabled
MOA0	0	0	0	0	0	0	0	0	00h	Month disabled
DWA0	0	0	0	0	0	0	0	0	00h	Day of week disabled

When the registers are set, the following waveform is seen at $\overline{\text{IRQ}}/\text{F}_{\text{OUT}}$:

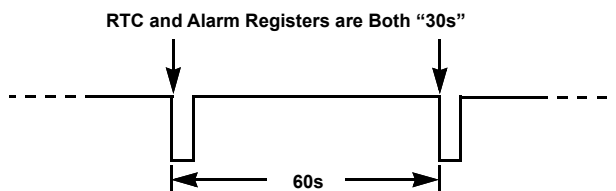


Figure 17. $\overline{\text{IRQ}}/\text{F}_{\text{OUT}}$ Waveform

Note: The status register ALM bit is set each time the alarm is triggered, but does not need to be read or cleared.

11.10 Time Stamp V_{DD} to Battery Registers (TSV2B)

The TSV2B Register bytes are identical to the RTC register bytes, except they do not extend beyond the Month. The Time Stamp captures the FIRST V_{DD} to Battery Voltage transition time, and will not update upon subsequent events, until cleared (only the first event is captured before clearing). Set CLRTS = 1 to clear this register (Add 09h, PWR_ V_{DD} register).

Note: The time stamp registers are cleared to all “0”, including the month and day, which is different from the RTC and alarm registers (those registers default to 01h). This is the indicator that no time stamping has occurred since the last clear or initial power-up. Once a time stamp occurs, there will be a non-zero time stamp.

11.11 Time Stamp Battery to V_{DD} Registers (TSB2V)

The Time Stamp Battery to V_{DD} Register bytes are identical to the RTC register bytes, except they do not extend beyond Month. The Time Stamp captures the LAST transition of V_{BAT} to V_D (only the last event of a series of power-up/down events is retained). Set CLRTS = 1 to clear this register (Add 09h, PWR_ V_{DD} register).

11.12 DST Control Registers (DSTCR)

8 bytes of control registers have been assigned for the Daylight Savings Time (DST) functions. DST beginning (set Forward) time is controlled by the registers DstMoFd, DstDwFd, DstDtFd, and DstHrFd. DST ending time (set Backward or Reverse) is controlled by DstMoRv, DstDwRv, DstDtRv and DstHrRv.

Table 19 and Table 20 describe the structure and functions of the DSTCR.

11.12.1 DST Forward Registers (20h to 23h)

DST forward is controlled by the following DST Registers:

Table 19. DST Forward Registers

Address	Function	7	6	5	4	3	2	1	0
20h	Month Forward	DSTE	0	0	MoFd20	MoFd13	MoFd12	MoFd11	MoFd10
21h	Day Forward	0	DwFdE	WkFd12	WkFd11	WkFd10	DwFd12	DwFd11	DwFd10
22h	Date Forward	0	0	DtFd21	DtFd20	DtFd13	DtFd12	DtFd11	DtFd10
23h	Hour Forward	0	0	HrFd21	HrFd20	HrFd13	HrFd12	HrFd11	HrFd10

11.12.1.1 DST Enable

DSTE is the DST Enabling Bit located in Bit[7] of register 20h (DstMoFdxx). Set DSTE = 1 will enable the DSTE function. Upon powering up for the first time (including battery), the DSTE bit defaults to “0”. When DSTE is set to “1” the RTC time must be at least one hour before the scheduled DST time change for the correction to take place. When DSTE is set to “0”, the DSTADJ bit in the Status Register automatically resets to “0”.

11.12.1.2 DST Month Forward

DstMoFd sets the Month that DST starts. The format is the same as for the RTC register month, from 1 to 12. The default value for the DST begin month is 00h.

11.12.1.3 DST Day/Week Forward

DstDwFd contains both the Day of the Week and the Week of the Month data for DST Forward control. DST can be controlled either by actual date or by setting both the Week of the month and the Day of the Week. DstDwFdE sets the priority of the Day/Week over the Date. For DstDwFdE = 1, Day/Week is the priority. You must have the correct Day of Week entered in the RTC registers for the Day/Week correction to work properly.

- Bits[0:2] contain the Day of the week information which sets the Day of the Week that DST starts. Note that Day of the week counts from 0 to 6, like the RTC registers. The default for the DST Forward Day of the Week is 00h (normally Sunday).
- Bits[3:5] contain the Week of the Month information that sets the week that DST starts. The range is from 1 to 5, and Week 7 is used to indicate the last week of the month. The default for the DST Forward Week of the Month is 00h.

11.12.1.4 DST Date Forward

DstDtFd controls which Date DST begins. The format for the Date is the same as for the RTC register, from 1 to 31. The default value for DST forward date is 00h. DstDtFd is only effective if DstDwFdE = 0.

11.12.1.5 DST Hour Forward

DstHrFd controls the hour that DST begins. The RTC hour and DstHrFd registers have the same formats except there is no Military bit for DST hour. The user sets the DST hour with the same format as used for the RTC hour (AM/PM or MIL) but without the MIL bit, and the DST will still advance as if the MIL bit were there. The default value for DST hour Forward is 00h.

11.12.2 DST Reverse Registers (24h to 27h)

DST end (reverse) is controlled by the following DST Registers:

Table 20. DST Reverse Registers

Address	Function	7	6	5	4	3	2	1	0
24h	Month Reverse	0	0	0	MoRv20	MoRv13	MoRv12	MoRv11	MoRv10
25h	Day Reverse	0	DwRvE	WkRv12	WkRv11	WkRv10	DwRv12	DwRv11	DwRv10
26h	Date Reverse	0	0	DtRv21	DtRv20	DtRv13	DtRv12	DtRv11	DtRv10
27h	Hour Reverse	0	0	HrRv21	HrRv20	HrRv13	HrRv12	HrRv11	HrRv10

11.12.2.1 DST Month Reverse

DstMoRv sets the Month that DST ends. The format is the same as for the RTC register month, from 1 to 12. The default value for the DST begin month is 00h.

11.12.2.2 DST Day/Week Reverse

DstDwRv contains both the Day of the Week and the Week of the Month data for DST Reverse control. DST can be controlled either by actual date or by setting both the Week of the month and the Day of the Week. DstDwRvE sets the priority of the Day/Week over the Date. For DstDwRvE = 1, Day/Week is the priority. You must have the correct Day of Week entered in the RTC registers for the Day/Week correction to work properly.

- Bits[0:2] contain the Day of the week information which sets the Day of the Week that DST ends. *Note:* Day of the week counts from 0 to 6, like the RTC registers. The default for the DST Reverse Day of the Week is 00h (normally Sunday).
- Bits[3:5] contain the Week of the Month information that sets the week that DST ends. The range is from 1 to 5, and Week 7 is used to indicate the last week of the month. The default for the DST Reverse Week of the Month is 00h.

11.12.2.3 DST Date Reverse

DstDtRv controls which Date DST ends. The format for the Date is the same as for the RTC register, from 1 to 31. The default value for DST Date Reverse is 00h. The DstDtRv is only effective if the DwRvE = 0.

11.12.2.4 DST Hour Reverse

DstHrRv controls the hour that DST ends. The RTC hour and DstHrRv registers have the same formats except there is no Military bit for DST hour. The user sets the DST hour with the same format as used for the RTC hour

(AM/PM or MIL) but without the MIL bit, and the DST will still advance as if the MIL bit were there. The default value for DST hour Reverse is 00h.

11.13 TEMP Registers (TEMP)

The temperature sensor produces an analog voltage output which is input to an A/D converter and produces a 10-bit temperature value in degrees Kelvin. TK07:00 are the LSBs of the code, and TK09:08 are the MSBs of the code. The temperature result is actually the average of two successive temperature measurements to produce greater resolution for the temperature control. The output code can be converted to degrees Centigrade (°C) by first converting from binary to decimal, dividing by 2, and then subtracting 273d, as shown in [Equation 4](#):

(EQ. 4) Temperature in °C = [(TK <9:0>)/2] - 273

The practical range for the temp sensor register output is from 446d to 726d, or -50°C to +90°C. The temperature compensation function is only guaranteed over -40°C to +85°C. The TSE bit must be set to "1" to enable temperature sensing.

TEMP	7	6	5	4	3	2	1	0
TK0L	TK07	TK06	TK05	TK04	TK03	TK02	TK01	TK00
TK0M	0	0	0	0	0	0	TK09	TK08

11.14 NPPM Registers (NPPM)

The NPPM value is exactly 2x the net correction required to bring the oscillator to 0ppm error. The value is the combination of oscillator Initial Correction (IPPM) and crystal temperature dependent correction (CPPM).

IPPM is used to compensate the oscillator offset at room temperature and is controlled by the ITR0 and BETA registers, which are fixed during factor test.

The CPPM compensates the oscillator frequency fluctuation over temperature. It is determined by the temperature (T), crystal curvature parameter (ALPHA), and crystal turnover temperature (XT0). T is the result of the temp sensor/ADC conversion, whose decimal result is 2x the actual temperature in Kelvin. ALPHA is from either the ALPHA (cold) or ALPHAH (hot) register depending on T, and XT0 is from the XT0 register.

NPPM is governed by [Equation 5](#):

$$\begin{aligned} \text{NPPM} &= \text{IPPM}(\text{ITR0}, \text{BETA}) + \text{ALPHA} \times (\text{T} - \text{T0})^2 \\ \text{(EQ. 5)} \quad \text{NPPM} &= \text{IPPM} + \text{CPPM} \\ \text{PPM} &= \text{IPPM} + \frac{\text{ALPHA} \times (\text{T} - \text{T0})^2}{4096} \end{aligned}$$

where:

$$\text{ALPHA} = \alpha \bullet 2048$$

T is the reading of the ADC, result is 2 x temperature in degrees Kelvin.

$$\begin{aligned} \text{(EQ. 6)} \quad \text{T} &= (2 \times 298) + \text{XT0} \\ \text{or } \text{T} &= 596 + \text{XT0} \end{aligned}$$

Note: NPPM can also be predicted from the FATR and FDTR register by the relationship (all values in decimal):

$$\text{NPPM} = 2 \times (\text{BETA} \times \text{FATR} - (\text{FDTR} - 16))$$

11.15 XT0 Registers (XT0)

11.15.1 Turnover temperature (XT[4:0])

The apex of the Alpha curve occurs at a point called the turnover temperature, or XT0. Crystals normally have a turnover temperature between +20°C and +30°C, with most occurring near +25°C.

Table 21. Turnover Temperature

ADDR	7	6	5	4	3	2	1	0
2Ch	0	0	0	XT4	XT3	XT2	XT1	XT0

The ISL12022 allows setting the turnover temperature so that temperature compensation can more exactly fit the curve of a crystal. [Table 22](#) shows the values available, with a range from +17.5°C to +32.5°C in +0.5°C increments. The default value is 00000b or +25°C.

Table 22. XT0 Values

XT[4:0]	Turnover Temperature
01111	32.5
01110	32.0
01101	31.5
01100	31
01011	30.5
01010	30
01001	29.5
01000	29.0
00111	28.5
00110	28.0
00101	27.5
00100	27.0
00011	26.5
00010	26.0
00001	25.5
00000	25.0
10000	25.0
10001	24.5
10010	24.0
10011	23.5
10100	23.0
10101	22.5
10110	22.0
10111	21.5
11000	21.0
11001	20.5
11010	20.0
11011	19.5
11100	19.0
11101	18.5
11110	18.0
11111	17.5

11.16 ALPHA Hot Register (ALPHAH)

The Alpha Hot variable is 7 bits and is defined as the temperature coefficient of Crystal from the T0 value to +85°C (both Alpha Hot and Alpha Cold must be programmed to provide full temperature compensation). It is normally given in units of ppm/°C², with a typical value of -0.034. Like the Alpha Cold version, a scaled version of the absolute value of this coefficient is used in order to get an integer value. Therefore, ALPHAH[7:0] is defined as the $(|Actual\ Alpha\ Hot\ Value| \times 2048)$ and converted to binary. For example, a crystal with Alpha Hot of -0.034ppm/°C² is first scaled $(|2048 \times (-0.034)| = 70d)$ and then converted to a binary number of 0100110b.

The practical range of Actual AlphaH values is from -0.020 to -0.060.

The ALPHAH register should only be changed while the TSE (Temp Sense Enable) bit is "0".

Table 23. ALPHAH Register

ADDR	7	6	5	4	3	2	1	0
2Dh	D	ALP_H6	ALP_H5	ALP_H4	ALP_H3	ALP_H2	ALP_H1	ALP_H0

12. User Registers (Accessed by Using Slave Address 1010111x)

12.1 Addresses [00h to 7Fh]

These registers are 128 bytes of battery-backed user SRAM.

13. I²C Serial Interface

The ISL12022 supports a bi-directional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is the master and the device being controlled is the slave. The master always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the ISL12022 operates as a slave device in all applications.

All communication over the I²C interface is conducted by sending the MSB of each byte of data first.

13.1 Protocol Conventions

Data states on the SDA line can change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (see Figure 18). On power-up of the ISL12022, the SDA pin is in the input mode.

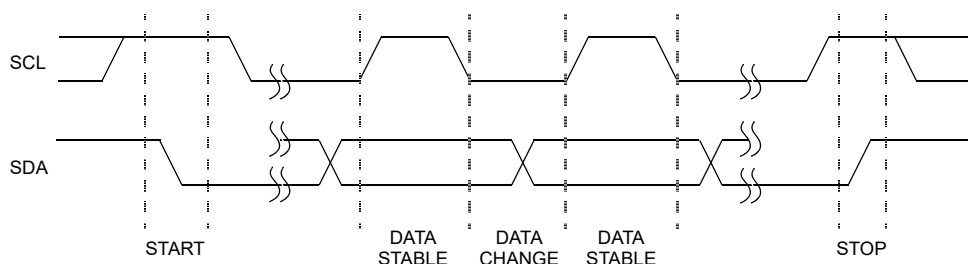


Figure 18. Valid Data Changes, Start and Stop Conditions

All I²C interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The ISL12022 continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (see Figure 18). A START condition is ignored during the power-up sequence.

All I²C interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH (see Figure 18). A STOP condition at the end of a read operation or at the end of a write operation to memory only places the device in its standby mode.

An acknowledge (ACK) is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the 8 bits of data (see Figure 19).

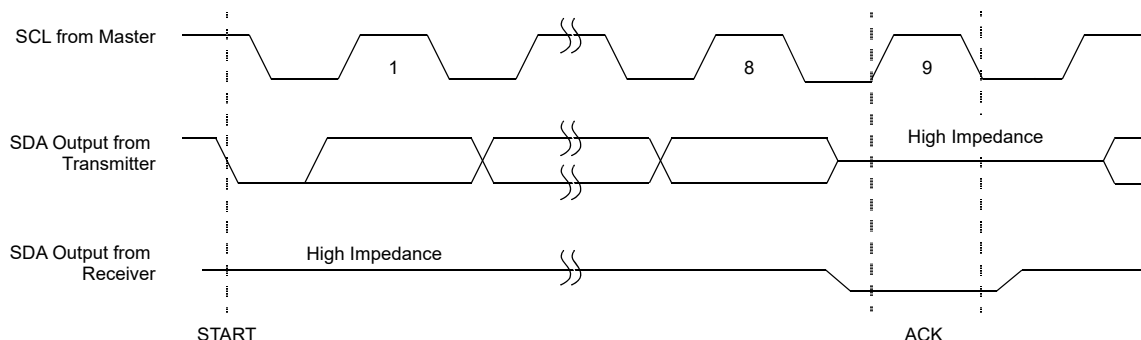


Figure 19. Acknowledge Response From Receiver

The ISL12022 responds with an ACK after recognition of a START condition followed by a valid Identification Byte, and once again, after successful receipt of an Address Byte. The ISL12022 also responds with an ACK after receiving a Data Byte of a write operation. The master must respond with an ACK after receiving a Data Byte of a read operation.

14. Device Addressing

Following a start condition, the master must output a Slave Address Byte. The 7 MSBs are the device identifiers. These bits are “1101111” for the RTC registers and “1010111” for the User SRAM.

The last bit of the Slave Address Byte defines a read or write operation to be performed. When this $\overline{R/\overline{W}}$ bit is a “1”, a read operation is selected. A “0” selects a write operation (refer to Figure 20).

After loading the entire Slave Address Byte from the SDA bus, the ISL12022 compares the device identifier and device select bits with “1101111” or “1010111”. Upon a correct compare, the device outputs an acknowledge on the SDA line.

Following the Slave Byte is a one byte word address. The word address is either supplied by the master device or obtained from an internal counter. On power-up, the internal address counter is set to address 00h, so a current address read starts at address 00h. When required, as part of a random read, the master must supply the 1 Word Address Bytes, as shown in Figure 22.

In a random read operation, the slave byte in the “dummy write” portion must match the slave byte in the “read” section. For a random read of the Control/Status Registers, the slave byte must be “1101111x” in both places.

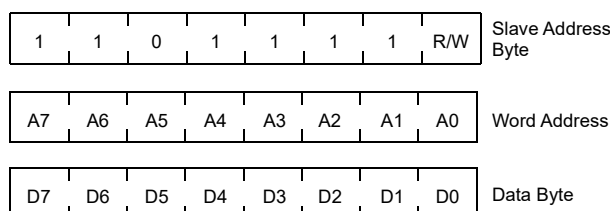


Figure 20. Slave Address, Word Address, and Data Bytes

15. Write Operation

A Write operation requires a START condition, followed by a valid Identification Byte, a valid Address Byte, a Data Byte, and a STOP condition. After each of the three bytes, the ISL12022 responds with an ACK. At this time, the I²C interface enters a standby state.

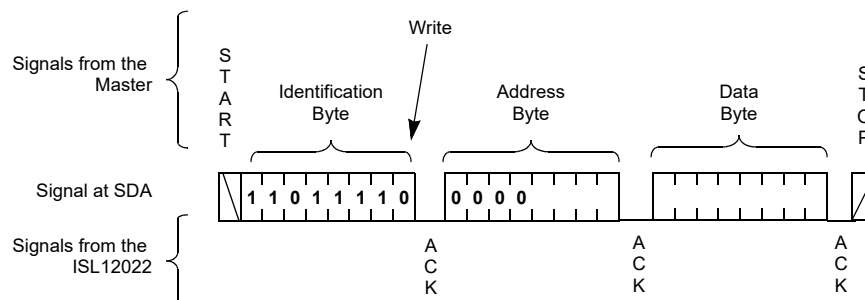


Figure 21. Byte Write Sequence (Slave Address for CSR Shown)

16. Read Operation

A Read operation consists of a three byte instruction, followed by one or more Data Bytes (see Figure 22). The master initiates the operation issuing the following sequence: a START, the Identification byte with the R/W bit set to "0", an Address Byte, a second START, and a second Identification byte with the R/W bit set to "1". After each of the three bytes, the ISL12022 responds with an ACK. Then the ISL12022 transmits Data Bytes as long as the master responds with an ACK during the SCL cycle following the eighth bit of each byte. The master terminates the read operation (issuing a STOP condition) following the last bit of the last Data Byte (see Figure 22).

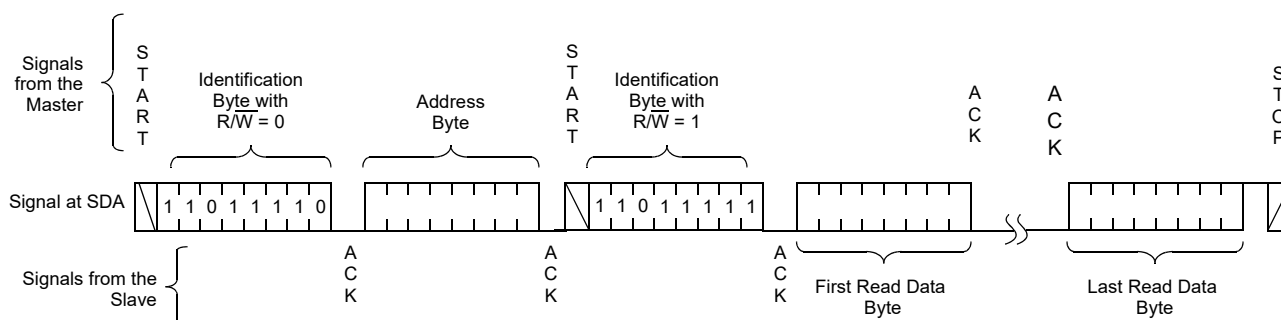


Figure 22. Read Sequence (CSR Slave Address Shown)

The Data Bytes are from the memory location indicated by an internal pointer. This pointer's initial value is determined by the Address Byte in the Read operation instruction, and increments by one during transmission of each Data Byte. After reaching the memory location 2Fh, the pointer "rolls over" to 00h, and the device continues to output data for each ACK received.

17. Applications Information

17.1 Power Supply Considerations

The ISL12022M contains programmed EEPROM registers which are recalled to volatile RAM registers during initial power-up. These registers contain DC voltage, frequency and temperature calibration settings. Initial power-up can be either application of V_{BAT} or V_{DD} power, whichever is first. It is important that the initial power-up meet the power supply slew rate specification to avoid faulty EEPROM power-up recall. Also, any glitches or low voltage DC pauses should be avoided, as these may activate recall at a low voltage and load erroneous data into the calibration registers. Note that a very slow V_{DD} ramp rate (outside data sheet limits) will almost always trigger erroneous recall and should be avoided entirely.

17.2 Battery-Backup Details

The ISL12022 has automatic switchover to battery-backup when the V_{DD} drops below the V_{BAT} mode threshold. A wide variety of backup sources can be used, including standard and rechargeable lithium, super capacitors, or regulated secondary sources. The serial interface is disabled in battery-backup, while the oscillator and RTC registers are operational. The SRAM register contents are powered to preserve their contents as well.

The input voltage range for V_{BAT} is 1.8V to 5.5V, but keep in mind the temperature compensation only operates for $V_{BAT} > 2.7V$. Note that the device is not guaranteed to operate with a $V_{BAT} < 1.8V$, so the battery should be changed before discharging to that level. It is strongly advised to monitor the low battery indicators in the status registers and take action to replace discharged batteries.

If a supercapacitor is used, it is possible that it may discharge to below 1.8V during prolonged power-down. Once powered up, the device may lose serial bus communications until both V_{DD} and V_{BAT} are powered down together. To avoid that situation, including situations where a battery may discharge deeply, the circuit in [Figure 23](#) can be used.

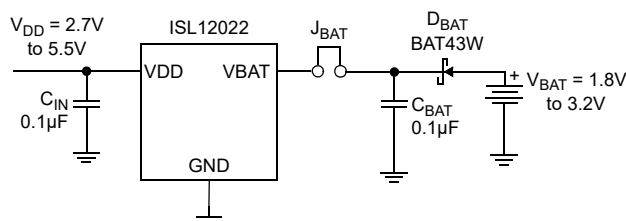


Figure 23. Suggested Battery-Backup Circuit

The diode, D_{BAT} adds a small drop to the battery voltage but protects the circuit should battery voltage drop below 1.8V. The jumper is added as a safeguard should the battery ever need to be disconnect from the circuit.

The V_{DD} negative slew rate should be limited to below the data sheet spec (10V/ms) otherwise battery switchover can be delayed, resulting in SRAM contents corruption and oscillator operation interruption.

Some applications will require separate supplies for the RTC V_{DD} and the I^2C pull-ups. This is not advised, as it may compromise the operation of the I^2C bus. For applications that do require serial bus communication with the RTC V_{DD} powered down, the SDA pin must be pulled low during the time the RTC V_{DD} ramps down to 0V. Otherwise, the device may lose serial bus communications once V_{DD} is powered up, and will return to normal operation ONLY once V_{DD} and V_{BAT} are both powered down together.

17.3 Oscillator Crystal Requirements

The ISL12022 uses a standard 32.768kHz crystal. Either through hole or surface mount crystals can be used. Table 24 lists some recommended surface mount crystals and the parameters of each. This list is not exhaustive and other surface mount devices can be used with the ISL12022 if their specifications are very similar to the devices listed. The crystal should have a required parallel load capacitance of 12.5pF and an equivalent series resistance of less than 50k. The crystal's temperature range specification should match the application. Many crystals are rated for -10°C to +60°C (especially through-hole and tuning fork types), so an appropriate crystal should be selected if extended temperature range is required.

Table 24. Suggested Surface Mount Crystals

Manufacturer	Part Number
Citizen	CM200S
Epson	MC-405, MC-406
Raltron	RSM-200S
SaRonix	32S12
Ecliptek	ECPSM29T-32.768K
ECS	ECX-306
Fox	FSM-327

17.4 Layout Considerations

The crystal input at X1 has a very high impedance, and oscillator circuits operating at low frequencies (such as 32.768kHz) are known to pick up noise very easily if layout precautions are not followed. Most instances of erratic clocking or large accuracy errors can be traced to the susceptibility of the oscillator circuit to interference from adjacent high speed clock or data lines. Careful layout of the RTC circuit will avoid noise pickup and insure accurate clocking.

Figure 24 shows a suggested layout for the ISL12022 device using a surface mount crystal. Two main precautions should be followed:

- Do not run the serial bus lines or any high speed logic lines in the vicinity of the crystal. These logic level lines can induce noise in the oscillator circuit, causing mislocking.
- Add a ground trace around the crystal with one end terminated at the chip ground. This will provide termination for emitted noise in the vicinity of the RTC device.

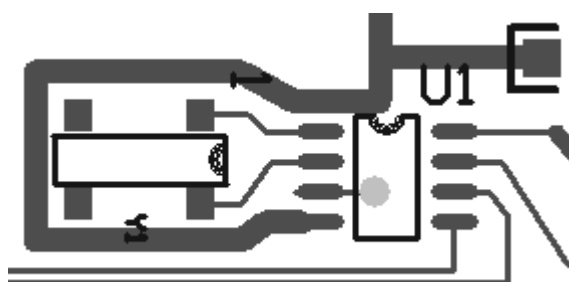


Figure 24. Suggested Layout for ISL12022 and Crystal

In addition, it is a good idea to avoid a ground plane under the X1 and X2 pins and the crystal, as this will affect the load capacitance and therefore the oscillator accuracy of the circuit. If the $\sim\overline{\text{IRQ}}/\text{F}_{\text{OUT}}$ pin is used as a clock, it should be routed away from the RTC device as well. The traces for the V_{BAT} and V_{DD} pins can be treated as a ground, and should be routed around the crystal.

17.5 Crystal Oscillator Frequency Compensation

17.5.1 Crystal Characteristics

The ISL12022 device contains a complete system for adjusting the frequency of the crystal oscillator to compensate for temperature variation. A typical 32.768kHz crystal used with RTC devices has a temperature versus frequency curve, as shown in Figure 25.

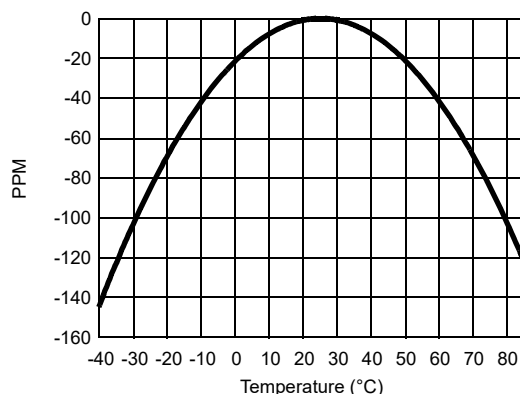


Figure 25. RTC Crystal Temperature Drift

The curve in Figure 25 follows Equation 7:

$$(EQ. 7) \quad \Delta f = \alpha \times (T - T_0)^2$$

where α is the temperature constant, with a typical value of 0.034 ppm/°C.

T_0 is the turnover temperature of the crystal, which is the apex of the parabolic curve. If the two factors α and T_0 are known, it is possible to correct for crystal temperature error to very high accuracy.

The crystal has an initial accuracy error at room temperature, typically specified at $\pm 20^\circ\text{C}$. The other important characteristic is the capacitances associated with the crystal. The load capacitance is normally specified at 12.5pF, although it can be lower in some cases. There is also a motional capacitance which affects the ability of the load capacitance to pull the oscillation frequency, and it is usually in the range of 2.2fF to 4.0fF.

17.5.2 RTC Clock Control

The ISL12022 uses two mechanisms to adjust the RTC clock and correct for the temperature error of the external crystal.

The Analog Trimming (AT) adjusts the load capacitance seen by the crystal. Analog switches connect the appropriate capacitance to change the frequency in increments of 1ppm. The adjustment range for the ISL12022 is +32/-31ppm.

The AT can be further refined using the BETA register. the BETA register function is to allow for changes in C_M (motional capacitance) which will affect the incremental frequency change of the AT adjustment. A simple test procedure uses the BETA register to bring the step size back to 1ppm.

Normally, the crystal frequency is adjusted at room temperature to zero out the frequency error using the IATRxx register bits (initial Analog Trimming). In addition, the IATRxx setting is varied up and down to record the variation in oscillator frequency compared to the step change in IATRxx. When that value is known then the BETA register is used to adjust the step size to be as close to 1ppm per IATRxx step as possible. After that adjustment is made, any ISL12022 temperature compensation adjustments use a 1ppm change for each bit change in the internal AT adjustment.

The Digital Trimming (DT) uses clock pulse add/subtract logic to change the RTC timing during temperature compensation. The DT steps are much coarser than the AT steps and are therefore used for large adjustments.

The DT steps are 30.5ppm, and the range is from -305ppm to +305ppm. The Frequency Output function will show the clock variation with DT settings, except for the 32,768Hz setting which only shows the AT control.

17.5.3 Active Temperature Compensation

The ISL12022 contains an intelligent logic circuit which takes the temperature sensor digital value as the only input variable. It then uses the register values for the crystal variables α and T_0 , and combines those with calibration from the BETA and ITR0 registers to produce “Final” values for the AT and DT, known as FATR (Final AT Register) and FDTR (Final DT Register). Those AT and DT values combine to directly compensate for the temperature error shown in [Figure 25](#).

The temperature sensor produces a new value every 60s (or up to 10 minutes in battery mode), which triggers the logic to calculate a new AT/DT value set. For every temperature calculation result, there can only be one corresponding AT/DT correction value.

17.6 Measuring Oscillator Accuracy

The best way to analyze the ISL12022 frequency accuracy is to set the $\overline{\text{IRQ}}/\text{F}_{\text{OUT}}$ pin for a specific frequency, and look at the output of that pin on a high accuracy frequency counter (at least 7 digits accuracy). Note that the $\overline{\text{IRQ}}/\text{F}_{\text{OUT}}$ is a drain output and will require a pull-up resistor.

Using the 1.0Hz output frequency is the most convenient as the ppm error is as expressed in [Equation 8](#):

$$\text{(EQ. 8)} \quad \text{ppm error} = (F_{\text{OUT}} - 1) \times 1\text{e}6$$

Other frequencies may be used for measurement but the error calculation becomes more complex.

When the proper layout guidelines are observed, the oscillator should start up in most circuits in less than 1s. When testing RTC circuits, a common impulse is to apply a scope probe to the circuit at the X2 pin (oscillator output) and observe the waveform. DO NOT DO THIS! Although in some cases you may see a usable waveform, due to the parasitics (usually 10pF to ground) applied with the scope probe, there will be no useful information in that waveform other than the fact that the circuit is oscillating. The X2 output is sensitive to capacitive impedance so the voltage levels and the frequency will be affected by the parasitic elements in the scope probe. Use the F_{OUT} output and a frequency counter for the most accurate results.

17.7 Temperature Compensation Operation

The ISL12022 temperature compensation feature needs to be enabled by the user. This must be done in a specific order as follows.

1. Read register 0Dh, the BETA register. This register contains the 5-bit BETA trimmed value which is automatically loaded on initial power-up. Mask off the 5LSB's of the value just read.
2. Bit[7] of the BETA register is the master enable control for temperature sense operation. Set this to “1” to allow continuous temperature frequency correction. Frequency correction will then happen every 60s with V_{DD} applied.
3. Bits[5:6] of the BETA register control temperature compensation in battery-backup mode (see [Table 14](#)). Set the values for the operation desired.
4. Write back to register 0Dh making sure not to change the 5 LSB values, and include the desired compensation control bits.

Note: Every time the BETA register is written with the TSE bit = 1, a temperature compensation cycle is instigated and a new correction value will be loaded into the FATR/FDTR registers (if the temperature changed since the last conversion).

Also note that registers 0Bh and 0Ch, the ITR0 and ALPHA registers, should not be changed. If they must be written be sure to write the same values that are recalled from initial power-up. The ITR0 register may be written if the user wishes to re-calibrate the oscillator frequency at room temperature for aging or board mounting. The original recalled value can be re-written if desired after testing.

For further information on the operation of the ISL12022 and temperature compensated RTC's, see Application Note [AN1389](#), *Using Intersil's High Accuracy Real Time Clock Module*.

17.8 Daylight Savings Time (DST) Example

DST involves setting the forward and back times and allowing the RTC device to automatically advance the time or set the time back. This can be done for current year, and future years. Many regions have DST rules that use standard months, weeks and time of the day which permit a pre-programmed, permanent setting.

[Table 25](#) shows the example setup for the ISL12022.

Table 25. DST Example

Variable	Value	Register	Value
Month Forward and DST Enable	April	20h	84h
Week and Day Forward and select Day/Week, not Date	1st Week and Sunday	21h	48h
Date Forward	not used	22h	00h
Hour Forward	2am	23h	02h
Month Reverse	October	24h	10h
Week and Day Reverse and select Day/Week, not Date	Last Week and Sunday	25h	78h
Date Reverse	not used	26h	00h
Hour Reverse	2am	27h	02h

The Enable bit (DSTE) is in the Month forward register, so the BCD value for that register is altered with the additional bit. The Week and Day values along with Week/Day vs Date select bit is in the Week/Day register, so that value is also not straight BCD. Hour and Month are normal BCD, but the Hour doesn't use the MIL bit since Military time PM values are already discretely different from AM/PM time PM values. The DST reverse setting utilizes the option to select the last week of the month for October, which could have 4 or 5 weeks but needs to have the time change on the last Sunday.

Note that the DSTADJ bit in the status register monitors whether the DST forward adjustment has happened. When it is "1", DST forward has taken place. When it is "0", then either DST reverse has happened, or it has been reset either by initial power-up or if the DSTE bit has been set to "0".

18. Package Outline Drawing

The package outline drawing is located at the end of this document and is accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

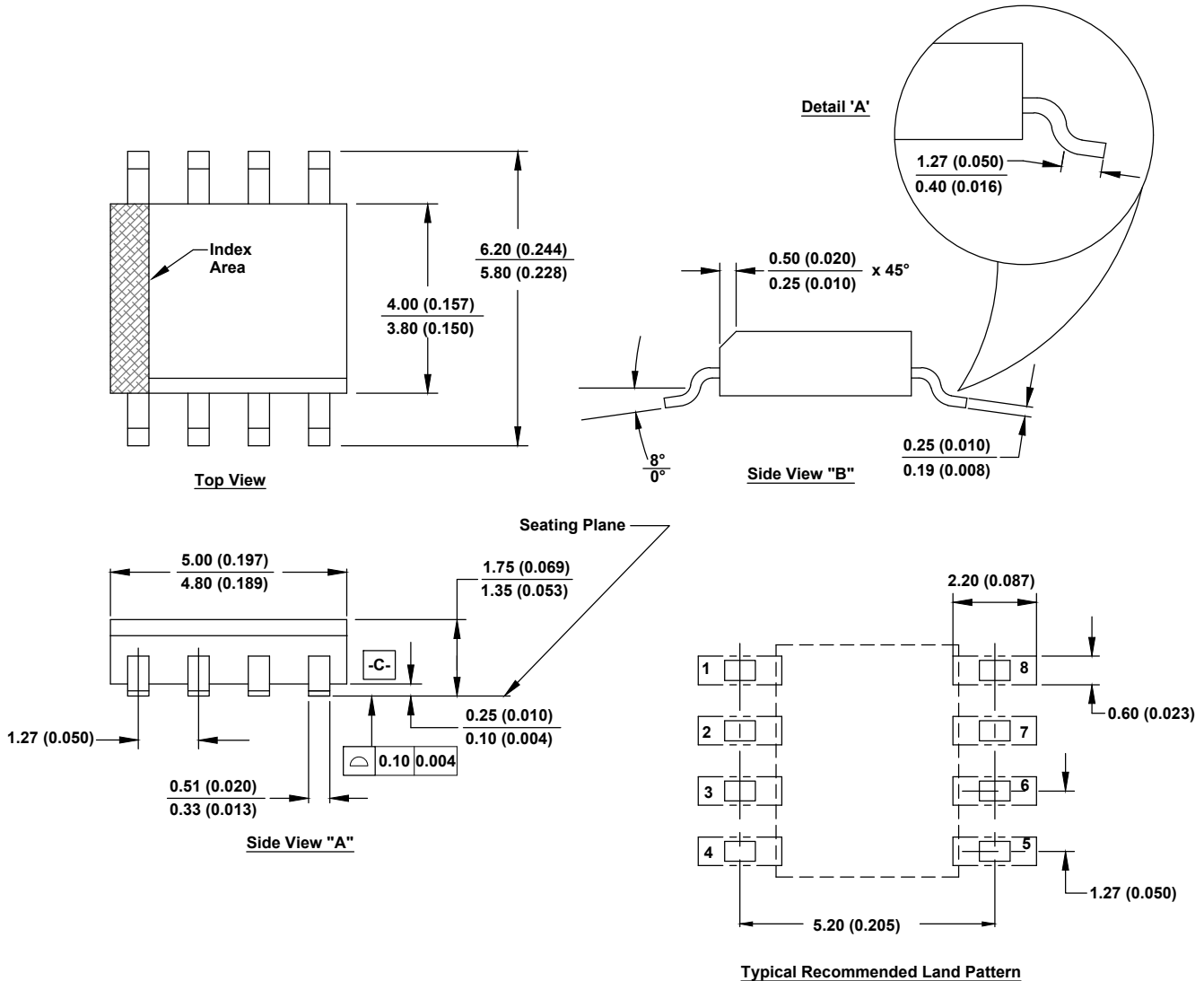
19. Ordering Information

Part Number ^{[1][2]}	Part Marking	V _{DD} Range (V)	Package Description ^[3] (RoHS Compliant)	Pkg. Dwg. #	Carrier Type ^[4]	Temp Range
ISL12022IBZ	12022 IBZ	2.7 to 5.5	8 Ld SOIC	M8.15	Tube	-40 to +85°C
ISL12022IBZ-T	12022 IBZ	2.7 to 5.5	8 Ld SOIC	M8.15	Reel, 2.5k	-40 to +85°C
ISL12022IBZ-T7A	12022 IBZ	2.7 to 5.5	8 Ld SOIC	M8.15	Reel, 250	-40 to +85°C

1. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. For Moisture Sensitivity Level (MSL), see the [ISL12022](#) device page. For more information about MSL, see [TB363](#).
3. For the Pb-Free Reflow Profile, see [TB493](#).
4. See [TB347](#) for details about reel specifications.

20. Revision History

Revision	Date	Description
4.00	Sep 10, 2026	▪ Applied latest template. ▪ Updated POD to the latest version.
3.01	Oct 24, 2019	▪ Updated links throughout. ▪ Added Related Literature section. ▪ Updated Ordering information by adding tape and reel information and updating notes. ▪ Updated labels on Figures 5 and 9. ▪ Added Revision History ▪ Updated POD M8.15 to latest revision changes are as follows: • Updated Note 1 changed 1982 to 1994. ▪ Updated Disclaimer.



Notes:

1. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
2. Package length does not include mold flash, protrusion or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.

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