ISL1591

Fixed Gain, Dual Port, VDSL2 Line Driver

FN7625
Rev 1.00
October 31, 2012

The ISL1591 provides 4 internal wideband op amps intended to be used as two pairs of fixed gain differential line drivers. The ISL1591's high bandwidth, and ultra low distortion enables the support of VDSL2 8b, 17a, and 30a in central office modem applications. This highly versatile line driver allows for operation from +14V to +24V nominal power supplies, while delivering exceptional MTPR distortion performance.

Using a single +24V supply, the ISL1591 MBPR distortion is below -62dBc in VDSL2 8b, -63dBc in VDSL2 17a, and -60dBc in VDSL2 30a profiles. Using a single +14V supply, ISL1591 supports 14.5dBm VDSL2 17a and 30a profiles at only a power consumption of 425mW. This capability is ideal for short loop, high bit rate VDSL2 applications where 14.5dBm transmit power is all that is required. For full power VDSL2 8b profile with 20dBm of transmit power, the line driver will require +24V single supply.

Each of the 4 internal op amps is a wideband current feedback amplifier offering very high slew rate intrinsic to that design using low quiescent current levels. Each of the two pair of amplifiers (ports) can also be power optimized to the application using two external quiescent control logic pins. Full power is nominally 14mA/port with options of medium power cutback to 9.7mA/port, a low power condition at 7.4mA/port, and an off state at <0.5mA/port.

High power push/pull line driver applications are best supported using a low headroom, high output current device. On +24V supplies, the ISL1591 offers a 1.6V headroom with >360mA peak output current. Driving differentially, this gives >42.4V_{P-P} swing to as low as 58Ω differential load. The four amplifiers in ISL1591 are intended to be used as differential pairs and not as individual amplifiers.

Features

- Internal Fixed Gain of 11.6V/V at R_{LOAD}
- ±360mA Output Drive Capability
- 42.4V_{P-P} Differential Output Drive into 82.6Ω
- -62dBc MBPR (VDSL 8b Profile)
- -65dBc US1, -63dBc US2 MBPR (VDSL2 17a Profile)
- -64dBc US1, -62dBc US2, -60dBc US3 MBPR (VDSL 30a Profile)
- High Slew Rate of 2000V/µs Differential
- Bandwidth (170MHz)
- Supply Current Control Pins
- K.20, GR-1089 Surge Robustness Validated
- Pb-Free (RoHS Compliant)

Applications

- ADSL2+
- VDSL2 Profiles: 8MHz, 17MHz, and 30MHz

Related Literature

- AN1325 "Choosing and Using Bypass Capacitors"

TABLE 1. ALTERNATE SOLUTIONS

PART #	NOMINAL ±V_{CC} (V)	BANDWIDTH (MHz)	APPLICATIONS
ISL1557	±6,+12	200	VDSL2
ISL1536	±12,+24	50	ADSL2+
ISL1539A	±12,+24	240	VDSL2

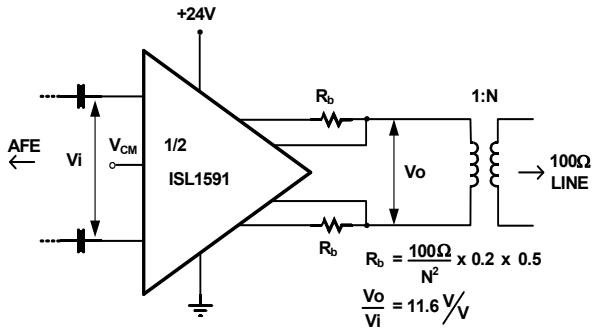


FIGURE 1. FIXED GAIN LINE DRIVER CIRCUIT

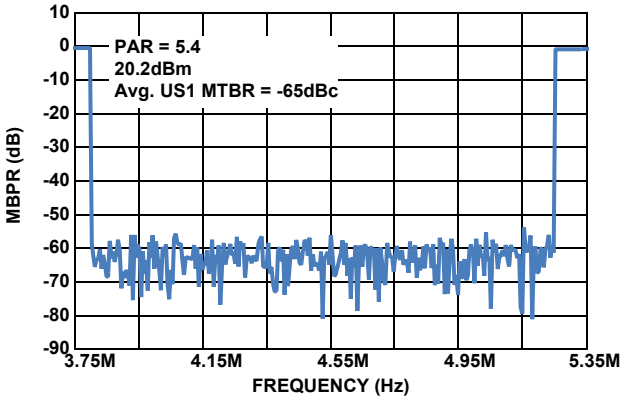


FIGURE 2. MBPR VDSL2 8b PERFORMANCE

Connection Diagram

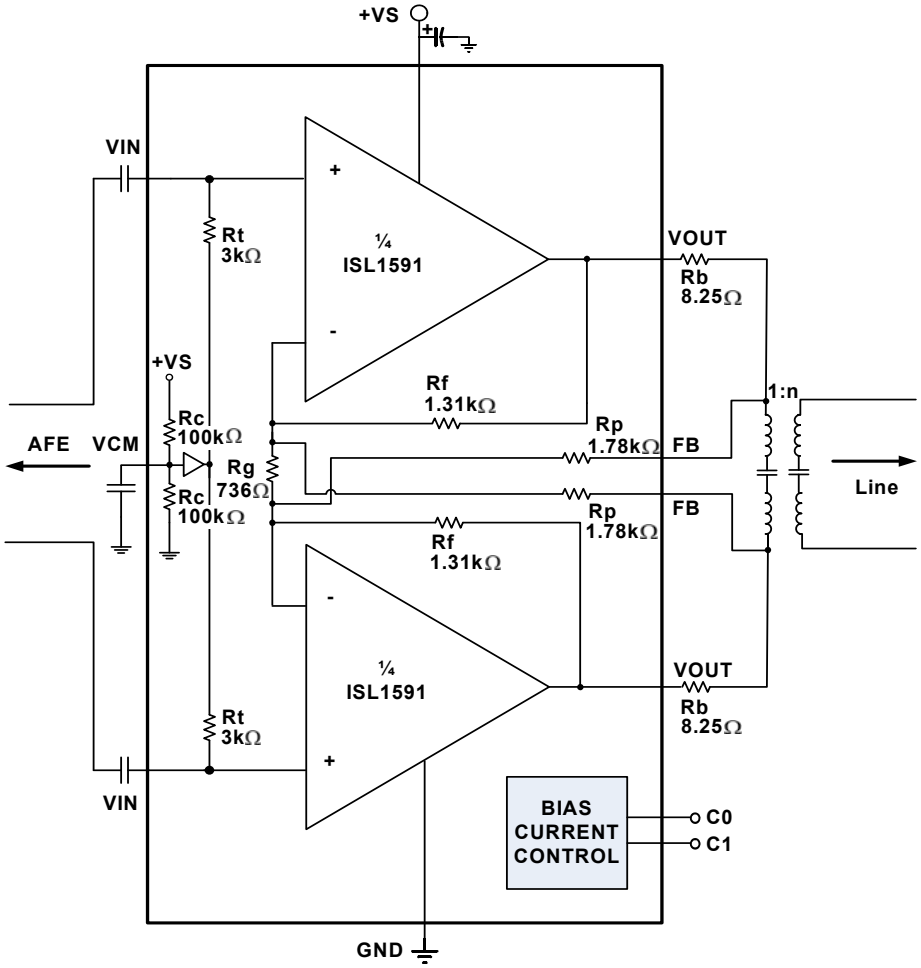
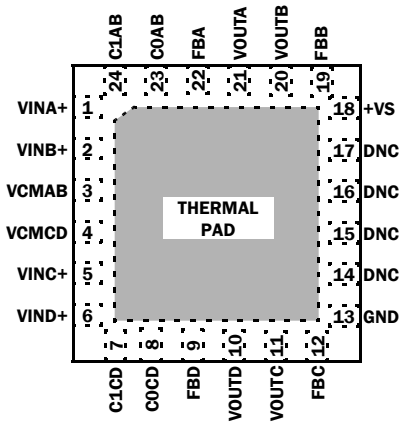


FIGURE 3. TYPICAL DIFFERENTIAL I/O LINE DRIVER (1 OF 2 PORTS)

Pin Configuration

ISL1591
(24 LD TQFN)
TOP VIEW



THERMAL PAD CONNECTS TO GND

Pin Descriptions

PIN NUMBER	PIN NAME	FUNCTION
1	VINA+	Amplifier A non-inverting input
2	VINB+	Amplifier B non-inverting input
3	VCMAB	Input common mode bias for port AB(#1)
4	VCMCD	Input common mode bias for port CD(#2)
5	VINC+	Amplifier C non-inverting input
6	VIND+	Amplifier D non-inverting input
7	C1CD	DSL Port #2 current control pin
8	C0CD	DSL Port #2 current control pin
9	FBD	Feedback pin for amplifier D
10	VOUTD	Amplifier D output
11	VOUTC	Amplifier C output
12	FBC	Feedback pin for amplifier C
13	GND	Ground
14, 15, 16, 17	DNC	Do not connect
18	+VS	Positive supply voltage
19	FBB	Feedback pin for amplifier B
20	VOUTB	Amplifier B output
21	VOUTA	Amplifier A output
22	FBA	Feedback pin for amplifier A
23	C0AB	DSL Port #1 current control pin
24	C1AB	DSL Port #1 current control pin
-	THERMAL PAD	Connects to GND

Ordering Information

PART NUMBER (Notes 2, 3)	PART MARKING	TEMP RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL1591IRTZ	15 91IRTZ	-40 to +85	24 Ld TQFN	L24.4x4F
ISL1591IRTZ-T7 (Note 1)	15 91IRTZ	-40 to +85	24 Ld TQFN	L24.4x4F
ISL1591IRTZ-T13 (Note 1)	15 91IRTZ	-40 to +85	24 Ld TQFN	L24.4x4F
ISL1591IRTZ-EVALZ	Evaluation Board			

NOTES:

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL1591. For more information on MSL please see tech brief TB363.

Absolute Maximum Ratings (T_A = +25°C)

V_S+ Voltage to GND ..... -0.3V to +26.4V
Driver V_{IN}+ Voltage ..... GND to V_S+
C_0, C_1 Voltage to GND ..... -0.3V to +6V
V_{CM} Voltage to GND ..... GND to V_S+
Current into any Input 8mA
Continuous Output Current for Long Term Reliability 50mA
ESD Rating
Human Body Model (Tested per JESD22-A114F) 3kV
Machine Model (Tested per JESD22-A115C) 300V
Charge Device Model (Tested per JESD22-C101E) 1.5kV

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
24 Ld TQFN Package (Notes 4, 5)	43	5.5

Maximum Junction Temperature (Plastic Package) ..... +150°C
Power Dissipation ..... See Figure 47
Storage Temperature Range ..... -40°C to +150°C
Pb-Free Reflow Profile ..... see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Ambient Temperature Range ..... -40°C to +85°C
Junction Temperature Range ..... -40°C to +150°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_S = +24V, R_L = 82.6Ω differential, $C_0 = C_1$ = 0V, T_A = +25°C. Amplifier pairs tested separately, unless otherwise indicated.

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
AC PERFORMANCE						
Av	Internal Gain Across R_{LOAD}	R_B = 8.25Ω	11.1	11.6	12.1	V/V
BW	-3dB Small Signal Bandwidth	$V_O < 2V_{P-P-DIFF}$		170		MHz
	-3dB Large Signal Bandwidth	$V_O = 10V_{P-P-DIFF}$		60		MHz
SR	20% to 80%	$V_O = 32V_{P-P-DIFF}$	1800	2000		V/µs
200kHz Harmonic Distortion	2nd Harmonic	$V_{OUT} = 2V_{P-P-DIFF}$		-90	-80	dBc
		$V_{OUT} = 10V_{P-P-DIFF}$		-87	-78	dBc
	3rd Harmonic	$V_{OUT} = 2V_{P-P-DIFF}$		-90	-78	dBc
		$V_{OUT} = 10V_{P-P-DIFF}$		-87	-80	dBc
	THD	$V_{OUT} = 2V_{P-P-DIFF}$		-87	-76	dBc
		$V_{OUT} = 10V_{P-P-DIFF}$		-84	-76	dBc
4MHz Harmonic Distortion	2nd Harmonic	$V_{OUT} = 10V_{P-P-DIFF}$		-83		dBc
	3rd Harmonic	$V_{OUT} = 10V_{P-P-DIFF}$		-75		dBc
	THD	$V_{OUT} = 10V_{P-P-DIFF}$		-74		dBc
8MHz Harmonic Distortion	2nd Harmonic	$V_{OUT} = 2V_{P-P-DIFF}$		-73		dBc
	3rd Harmonic	$V_{OUT} = 2V_{P-P-DIFF}$		-65		dBc
	THD	$V_{OUT} = 2V_{P-P-DIFF}$		-65		dBc
MBPR	Missing-Band Power Ratio: US1 Band	26kHz to 8MHz, 4kHz Tone Spacing, P_{LINE} = 19dBm, VDSL2+ 8b		-65	-62	dBc
e_O	Output Voltage Noise	f = 1MHZ		90		nV/√Hz
e_{N-CM}	Common Mode Output Noise at each Port Pair	f = 1MHZ		90		nV/√Hz
POWER CONTROL FEATURES						
V_{IH}	Logic High Voltage	C_0 and C_1 inputs	2.0			V

Electrical Specifications V_S = +24V, R_L= 82.6Ω differential, C_0 = C_1 = 0V, T_A = +25°C. Amplifier pairs tested separately, unless otherwise indicated. **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
V_{IL}	Logic Low Voltage	C_0 and C_1 inputs			0.8	V
I_{IH0} , I_{IH1}	Logic High Current for C_0, C_1	C_0 = 3.3V, C_1 = 3.3V	-7.5	1	+7.5	µA
I_{IL0}, I_{IL1}	Logic Low Current for C_0, C_1	C_0 = 0V, C_1 = 0V	-17	-13	-10	µA
SUPPLY CHARACTERISTICS						
	Maximum Operating Supply Voltage			+25.2		V
	Minimum Operating Supply Voltage			+14		V
I_S+ (Full Power)	Positive Supply Current per Port	All outputs at V_{CM}, C_0 = C_1 = 0V, $+V_S$ = 24V	13	14	14.9	mA
		$+V_S$ = 14V	9.7	10.8	12	mA
I_S+ (Medium)	Positive Supply Current per Port	All outputs at V_{CM}, C_0 = 3.3V, C_1 = 0V, $+V_S$ = 24V	9.1	9.7	10.5	mA
		$+V_S$ = 14V	6.7	7.2	8.0	mA
I_S+ (Low)	Positive Supply Current per Port	All outputs at V_{CM}, C_0 = 0V, C_1 = 3.3V, $+V_S$ = 24V	6.8	7.4	8.1	mA
		$+V_S$ = 14V	5.0	5.4	6.1	mA
I_S+ (Power-down)	Positive Supply Current per Port	All outputs at V_{CM}, C_0 = C_1 = 3.3V, $+V_S$ = 24V	0.4	0.5	0.65	mA
		$+V_S$ = 14V	0.3	0.4	0.5	mA
OUTPUT CHARACTERISTICS						
V_{OUT}	Output Swing	R_{L-DIFF} = No Load	+22	+22.4		V
	Lightly Loaded Output Swing	R_{L-DIFF} = 100Ω	+20.2	+21.2		V
I_{OL}	Linear Output Current	R_L = 25Ω, f = 100kHz, THD = -60dBc		±360		mA
I_{OUT}	Peak Output Current	V_{OUT} = ±1V, R_L = 1Ω		±600		mA
V_{OS-OUT}	Differential Output Offset Voltage		-150	25	+150	mV
V_{OS-CM}	Common Mode Output Offset Voltage		-50	-20	+50	mV
INPUT CHARACTERISTICS						
CMIR	Common Mode Input Range at each of the 4 Non-Inverting Input Pins		+4.5		+19.5	V
CMRR	Common Mode Rejections for each Port. V_{CM} = +4.5V to +19.5V	V_{CM} to Differential Mode Output (Input Referred), DC		66		dB
		V_{CM} to Commonl Mode Output (Output Referred), DC		55		dB
PSRR	Power Supply Rejections for each Port to Differential Output (Input Referred)	$+V_S$ = +15V to +24V, GND = 0V, DC		66		dB
	Power Supply Rejections for each Port to Common Mode Output (Output Referred)	$+V_S$ = +15V to +24V, GND = 0V, DC		58		dB
R_{IN}	Input Resistance	Differential		6.0		kΩ

NOTE:

6. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Typical Performance Curves

V_{CC} = +24V, R_b = 8.25Ω, GND at the Load = 11.6V/V (differential), R_{LOAD} = 82.5Ω, T_A +25°C, C0 = C1 = 0V (full power) unless otherwise noted.

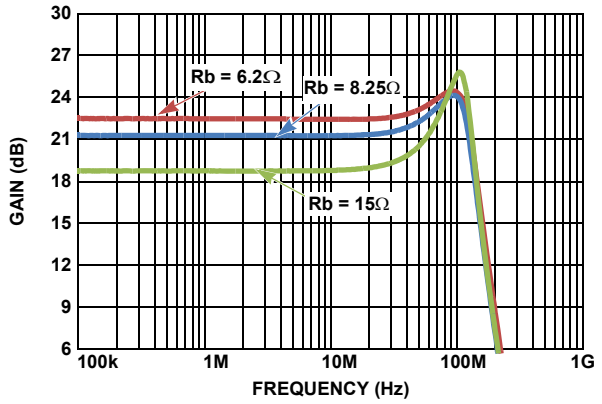


FIGURE 4. SMALL SIGNAL FREQUENCY RESPONSE vs GAIN AT THE LOAD

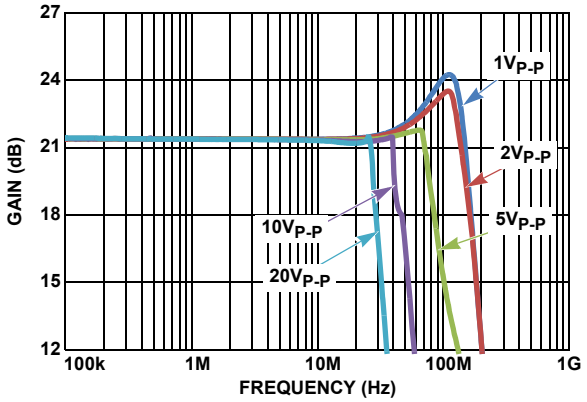


FIGURE 5. LARGE SIGNAL FREQUENCY RESPONSE

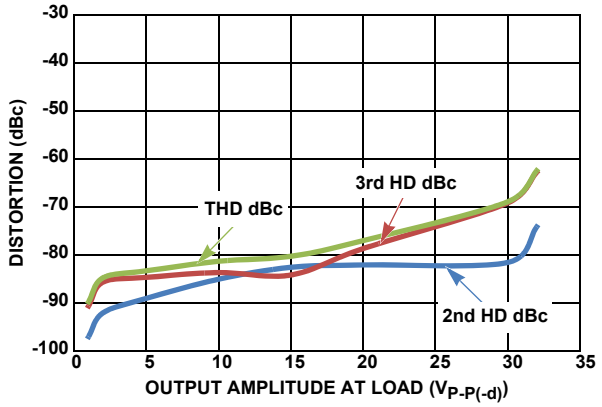


FIGURE 6. 1MHz HARMONIC DISTORTION vs OUTPUT AMPLITUDE

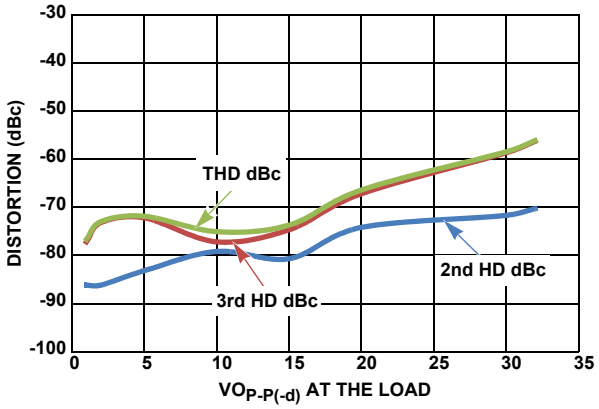


FIGURE 7. 4MHz HARMONIC DISTORTION vs OUTPUT AMPLITUDE

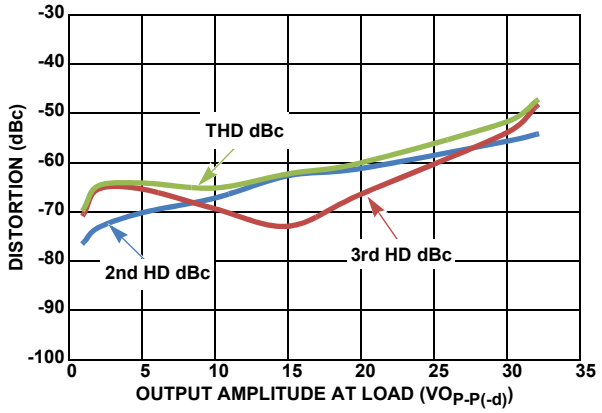


FIGURE 8. 8MHz HARMONIC DISTORTION vs OUTPUT AMPLITUDE

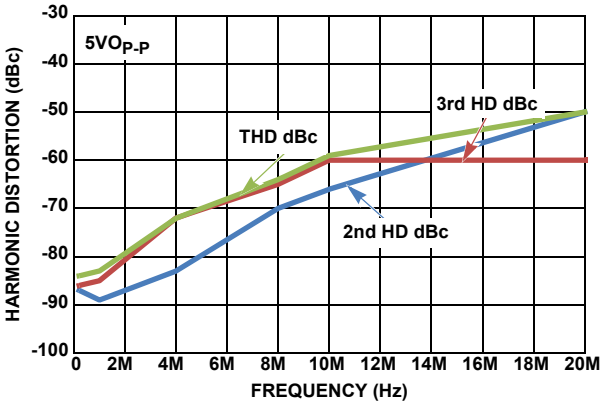


FIGURE 9. HARMONIC DISTORTION vs FREQUENCY

Typical Performance Curves

V_{CC} = +24V, R_b = 8.25Ω, GND at the Load = 11.6V/V (differential), R_{LOAD} = 82.5Ω, T_A +25°C, C0 = 3.3V, C1 = 0V (85% power) unless otherwise noted.

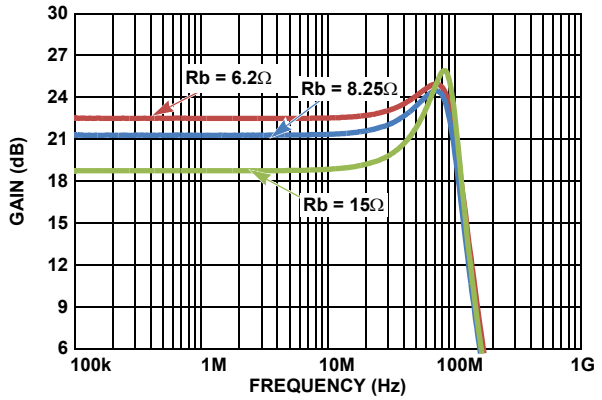


FIGURE 10. SMALL SIGNAL FREQUENCY RESPONSE vs GAIN AT THE LOAD

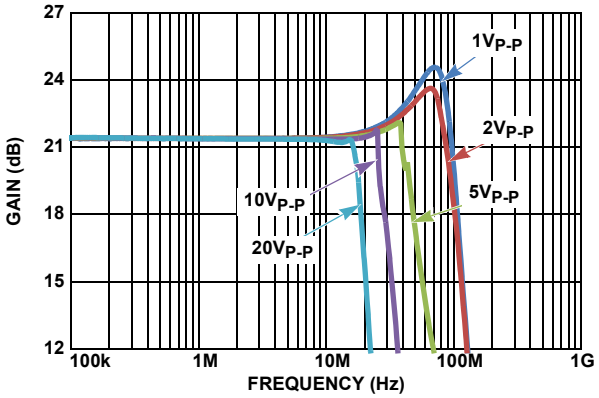


FIGURE 11. LARGE SIGNAL FREQUENCY RESPONSE

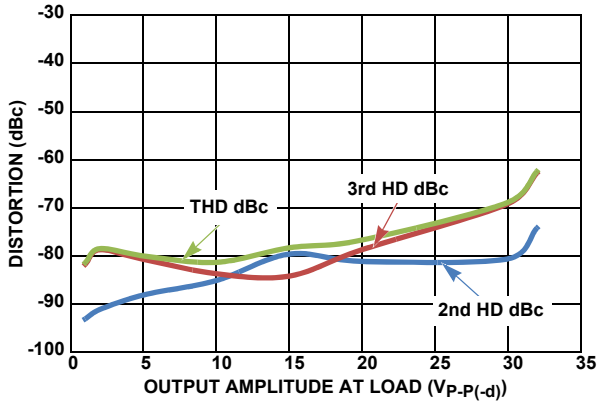


FIGURE 12. 1MHz HARMONIC DISTORTION vs OUTPUT AMPLITUDE

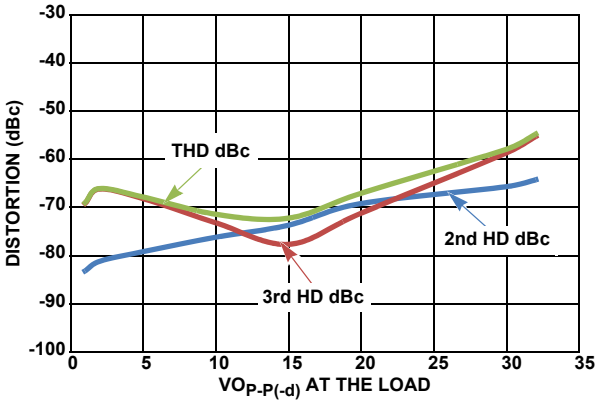


FIGURE 13. 4MHz HARMONIC DISTORTION vs OUTPUT AMPLITUDE

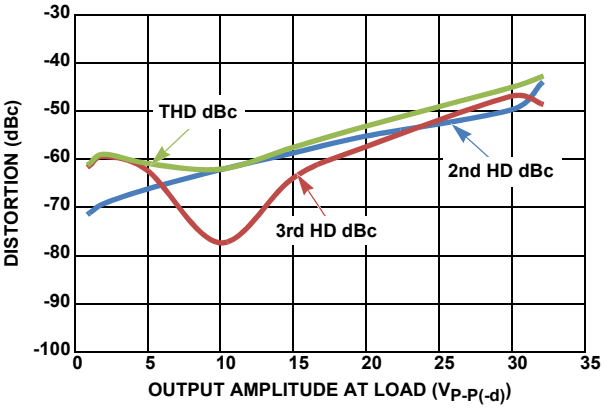


FIGURE 14. 8MHz HARMONIC DISTORTION vs OUTPUT AMPLITUDE

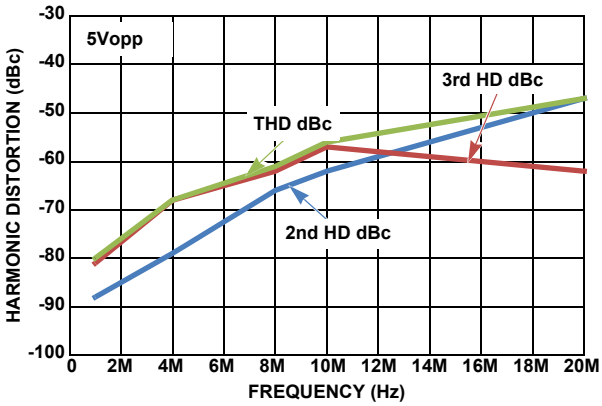


FIGURE 15. HARMONIC DISTORTION vs FREQUENCY

Typical Performance Curves

V_{CC} = +24V, R_b = 8.25Ω, GND at the Load = 11.6V/V (differential), R_{LOAD} = 82.5Ω, T_A +25°C, C1 = 3.3V, C0 = 0V (50% power) unless otherwise noted.

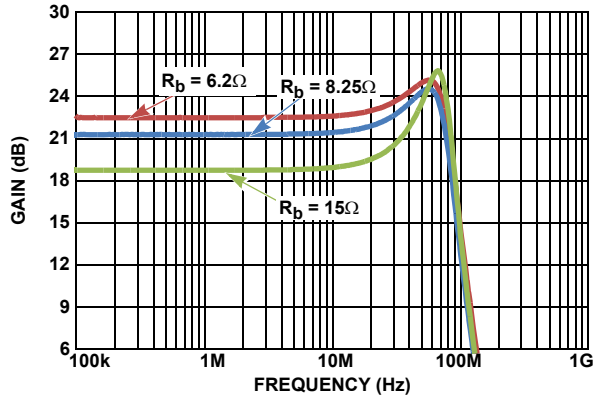


FIGURE 16. SMALL SIGNAL FREQUENCY RESPONSE vs GAIN AT THE LOAD

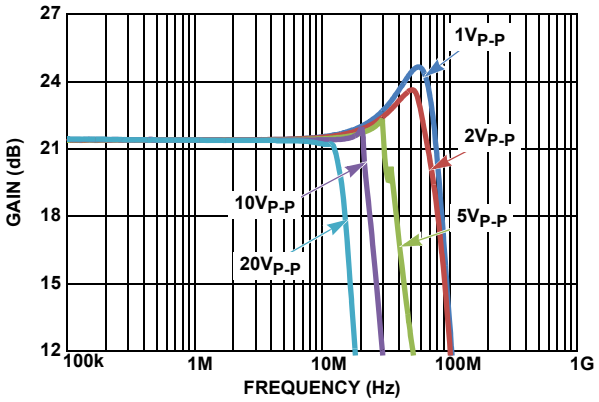


FIGURE 17. LARGE SIGNAL FREQUENCY RESPONSE

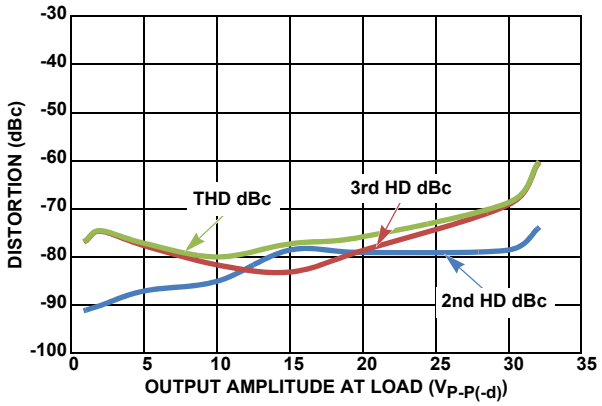


FIGURE 18. 1MHz HARMONIC DISTORTION vs OUTPUT AMPLITUDE

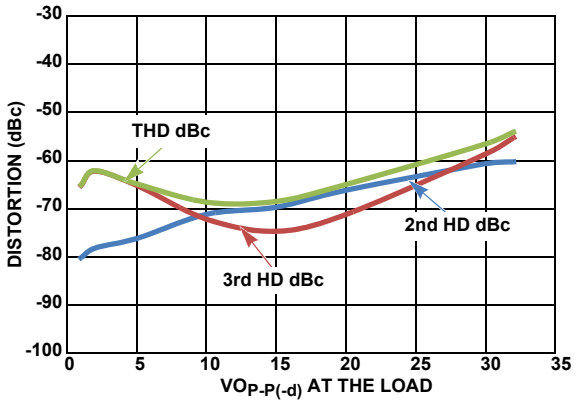


FIGURE 19. 4MHz HARMONIC DISTORTION vs OUTPUT AMPLITUDE

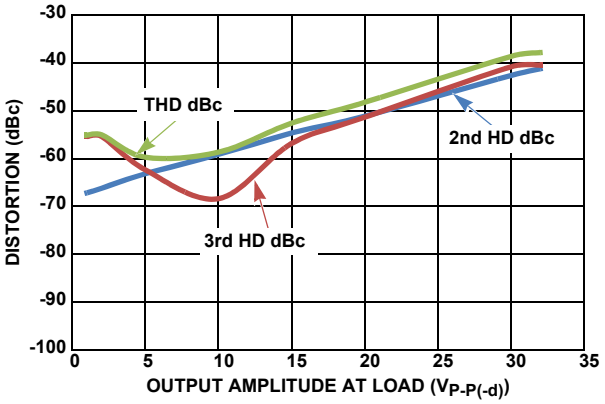


FIGURE 20. 8MHz HARMONIC DISTORTION vs OUTPUT AMPLITUDE

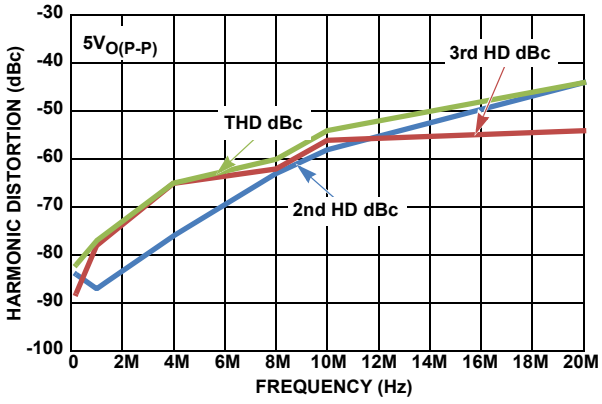


FIGURE 21. HARMONIC DISTORTION vs FREQUENCY

Typical Performance Curves

V_{CC} = +24V, R_b = 8.25Ω, GND at the Load = 11.6V/V (differential), R_{LOAD} = 82.5Ω, T_A +25°C, C0 = C1, C0 = 0V (Full power) unless otherwise noted.

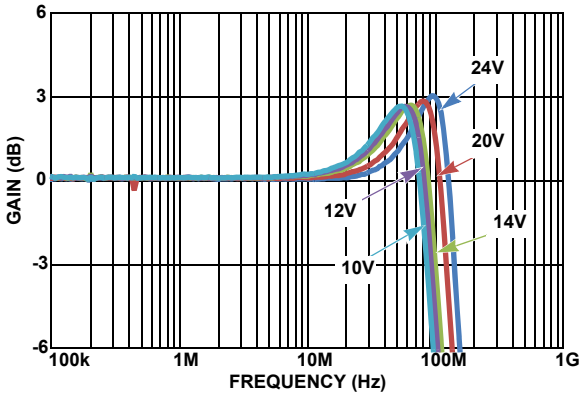


FIGURE 22. SMALL SIGNAL BW vs SUPPLY VOLTAGE

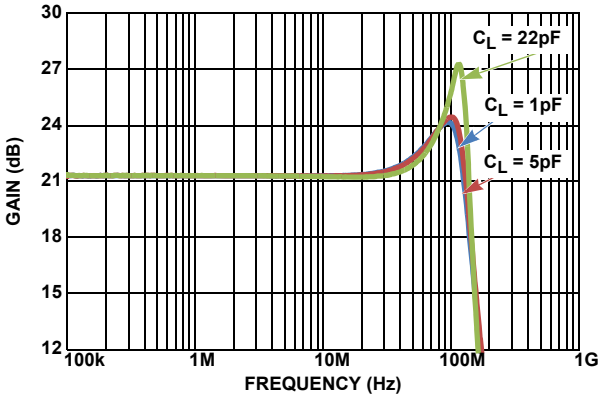


FIGURE 23. SMALL SIGNAL FREQUENCY RESPONSE vs C_{LOAD} (AFTER RB)

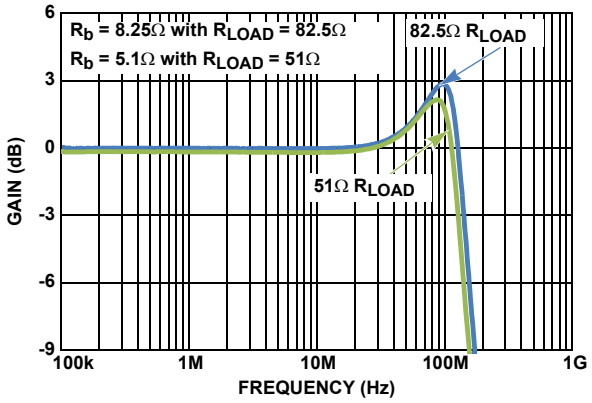


FIGURE 24. SMALL SIGNAL FREQUENCY RESPONSE vs R_{LOAD}

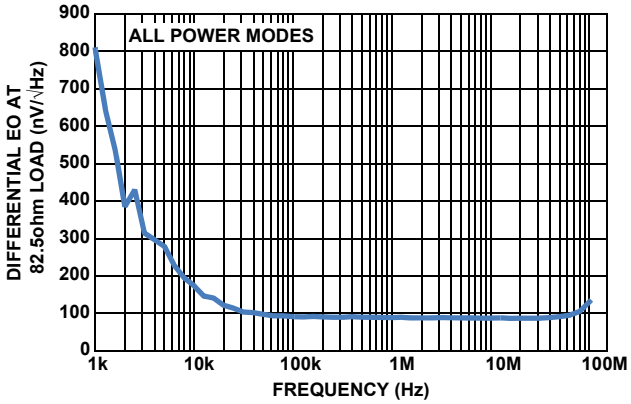


FIGURE 25. OUTPUT VOLTAGE NOISE

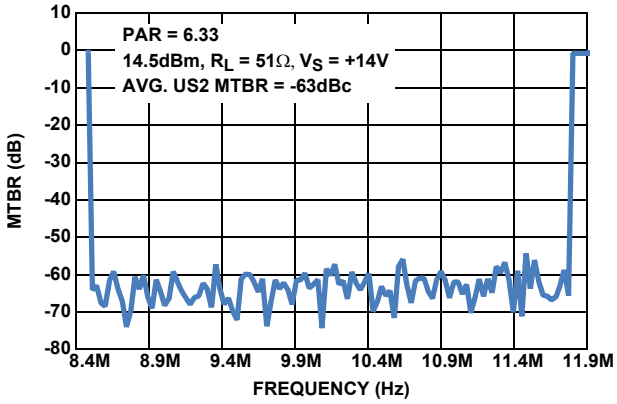


FIGURE 26. VDSL2 17a PROFILE MTBR US2

Typical Performance Curves

V_{CC} = +24V, R_b = 8.25Ω, GND at the Load = 11.6V/V (differential), R_{LOAD} = 82.5Ω, T_A +25°C, C0 = 3.3V, C1 = 0V (85%power) unless otherwise noted.

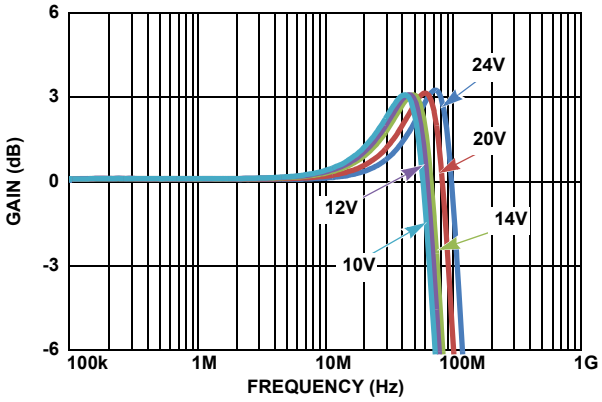


FIGURE 27. SMALL SIGNAL BW vs SUPPLY VOLTAGE

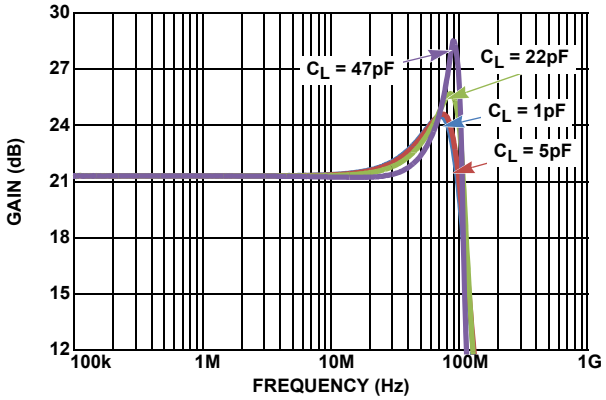


FIGURE 28. SMALL SIGNAL FREQUENCY RESPONSE vs C_{LOAD} (AFTER RB)

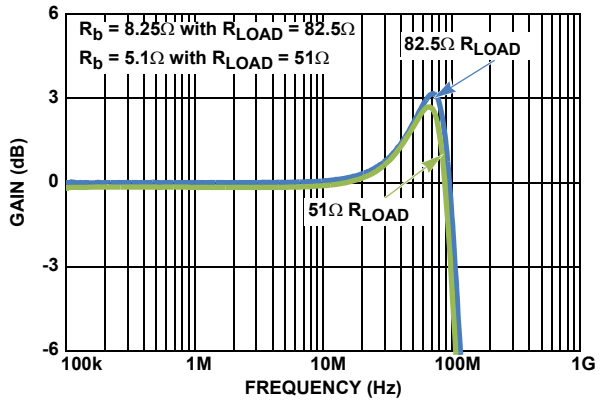


FIGURE 29. SMALL SIGNAL FREQUENCY RESPONSE vs R_{LOAD}

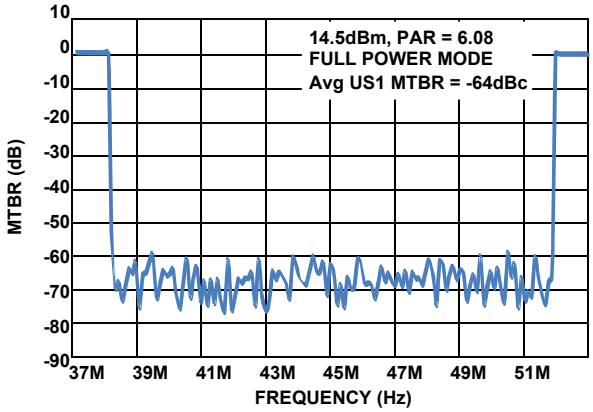


FIGURE 30. VDSL2 30a PROFILE MTBR US1

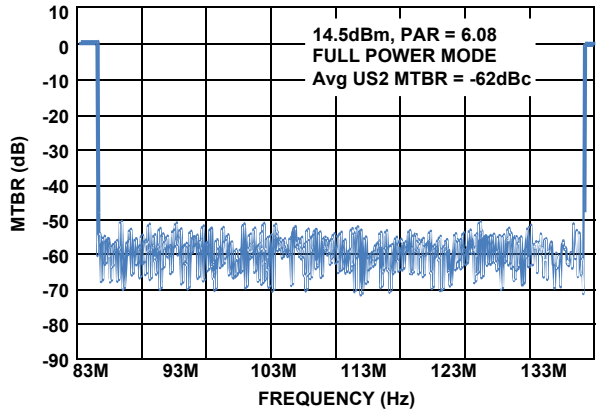


FIGURE 31. VDSL2 30a PROFILE MTBR US2

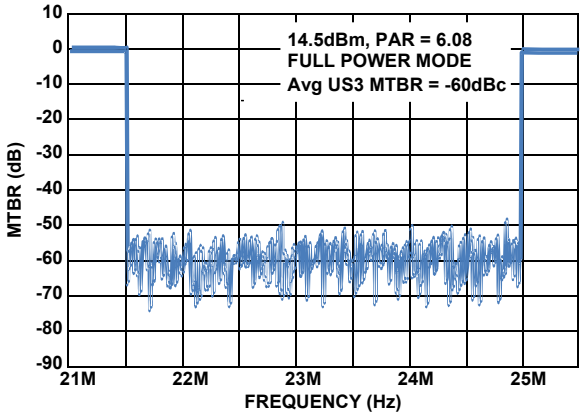


FIGURE 32. VDSL2 30a PROFILE MTBR US3

Typical Performance Curves

V_{CC} = +24V, R_b = 8.25Ω, GND at the Load = 11.6V/V (differential), R_{LOAD} = 82.5Ω, T_A +25°C, C1 = 3.3V, C0 = 0V (50%power) unless otherwise noted.

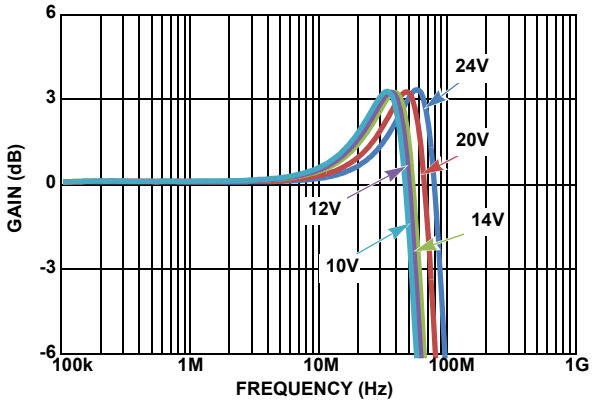


FIGURE 33. SMALL SIGNAL BW vs SUPPLY VOLTAGE

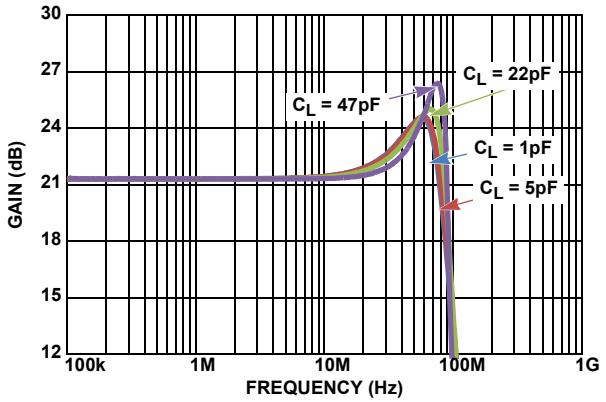


FIGURE 34. SMALL SIGNAL FREQUENCY RESPONSE vs C_{LOAD}

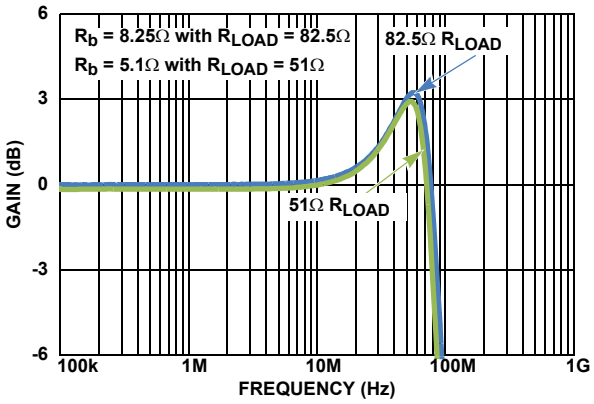


FIGURE 35. SMALL SIGNAL FREQUENCY RESPONSE vs R_{LOAD}

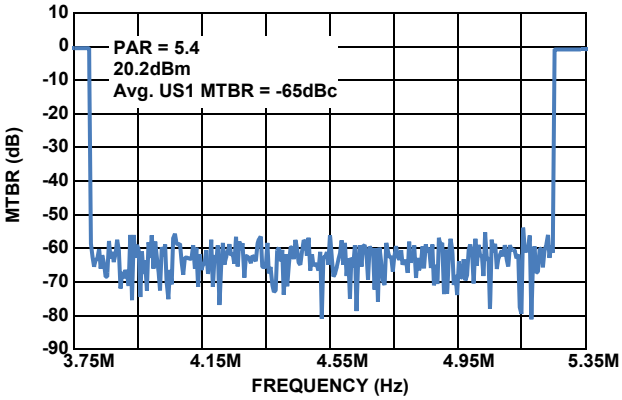


FIGURE 36. VDSL2+ 8b PROFILE MTBR

Typical Performance Curves

V_{CC} = +24V, R_b = 8.25Ω, GND at the Load = 11.6V/V (differential), R_{LOAD} = 82.5Ω, T_A +25°C, C0 and C1 Parametric unless otherwise noted.

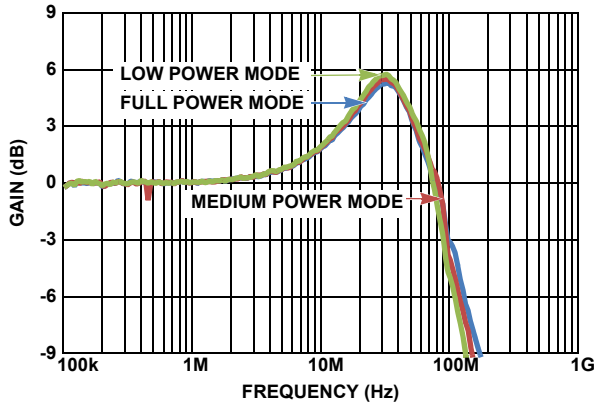


FIGURE 37. COMMON MODE SMALL SIGNAL FREQUENCY RESPONSE

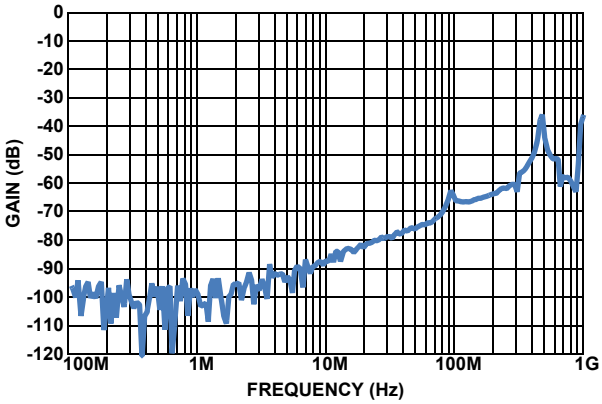


FIGURE 38. CHANNEL-TO-CHANNEL X-TALK

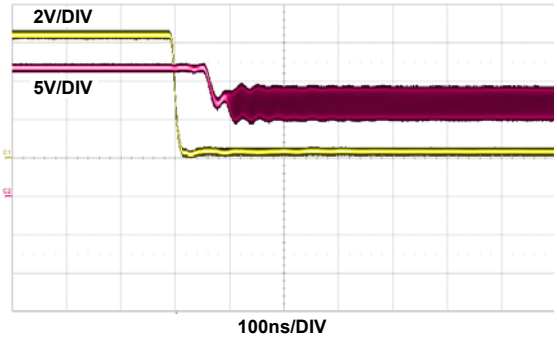


FIGURE 39. POWER-UP TIME

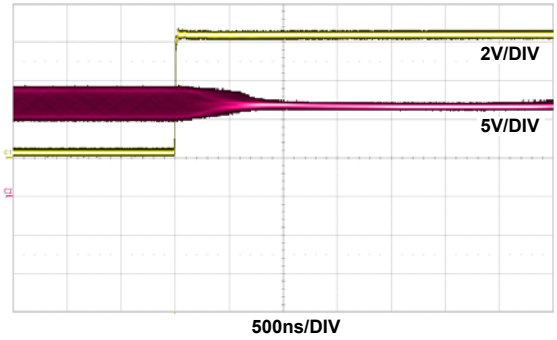


FIGURE 40. POWER-DOWN TIME

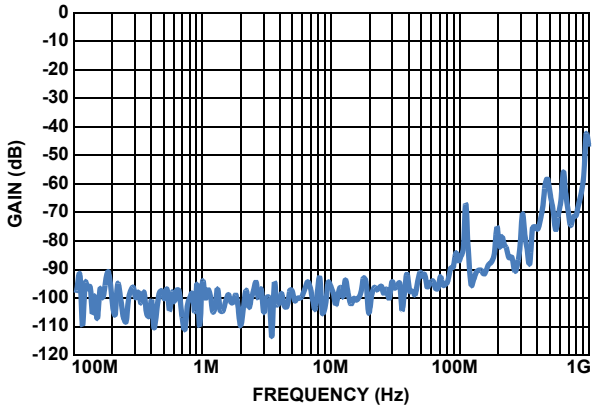


FIGURE 41. OFF-ISOLATION

Typical Performance Curves

V_{CC} = +24V, R_b = 8.25Ω, GND at the Load = 11.6V/V (differential), R_{LOAD} = 82.5Ω, T_A +25°C, C0 and C1 Varied unless otherwise noted.

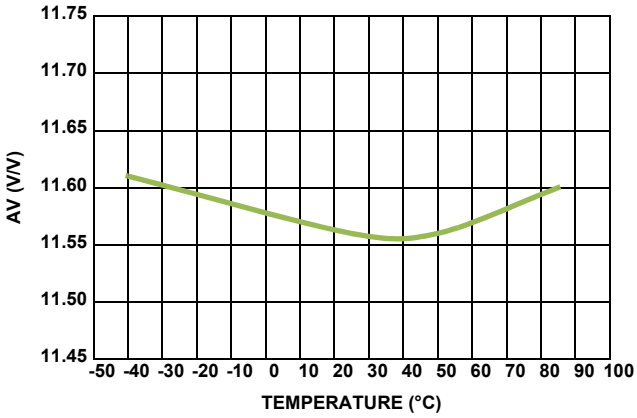


FIGURE 42. GAIN AT THE LOAD vs TEMPERATURE

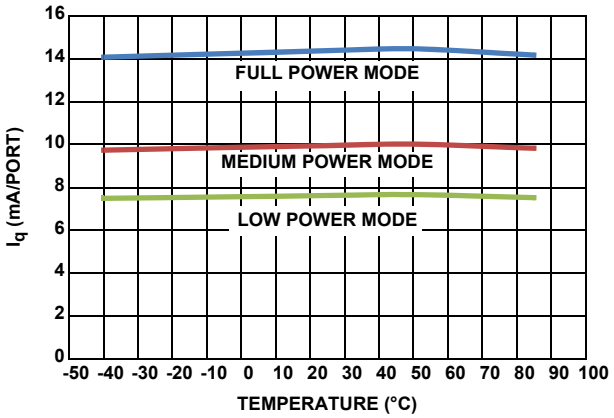


FIGURE 43. QUIESCENT CURRENT vs TEMPERATURE

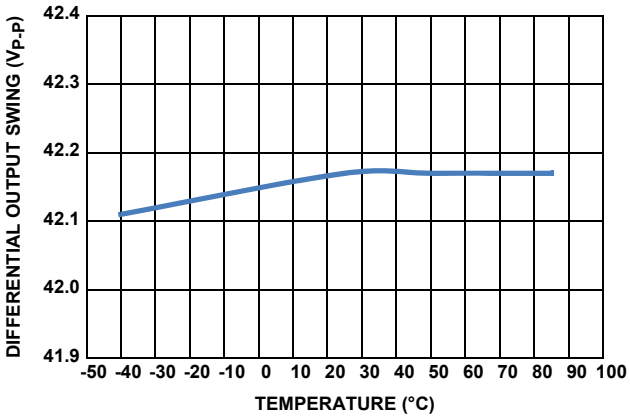


FIGURE 44. DIFFERENTIAL OUTPUT SWING vs TEMPERATURE

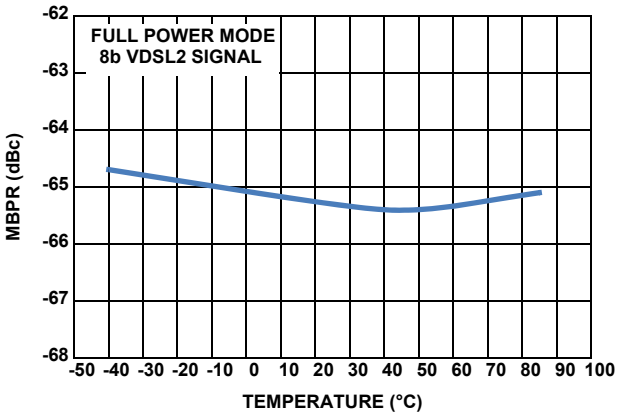


FIGURE 45. 8b MBPR vs TEMPERATURE

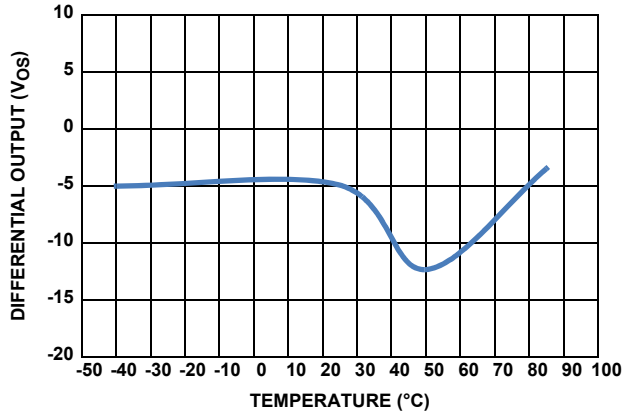


FIGURE 46. OUTPUT OFFSET vs TEMPERATURE

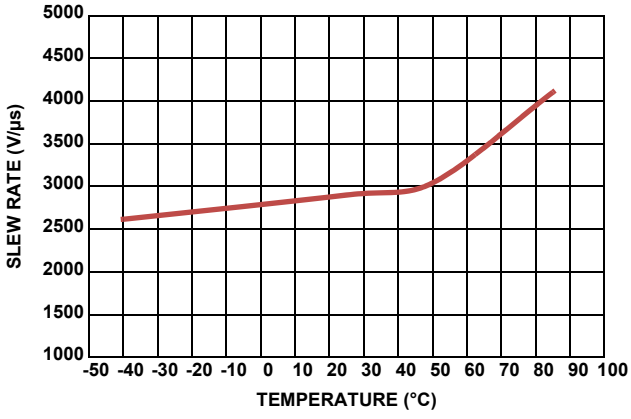


FIGURE 47. SLEW RATE vs TEMPERATURE

Test Circuit

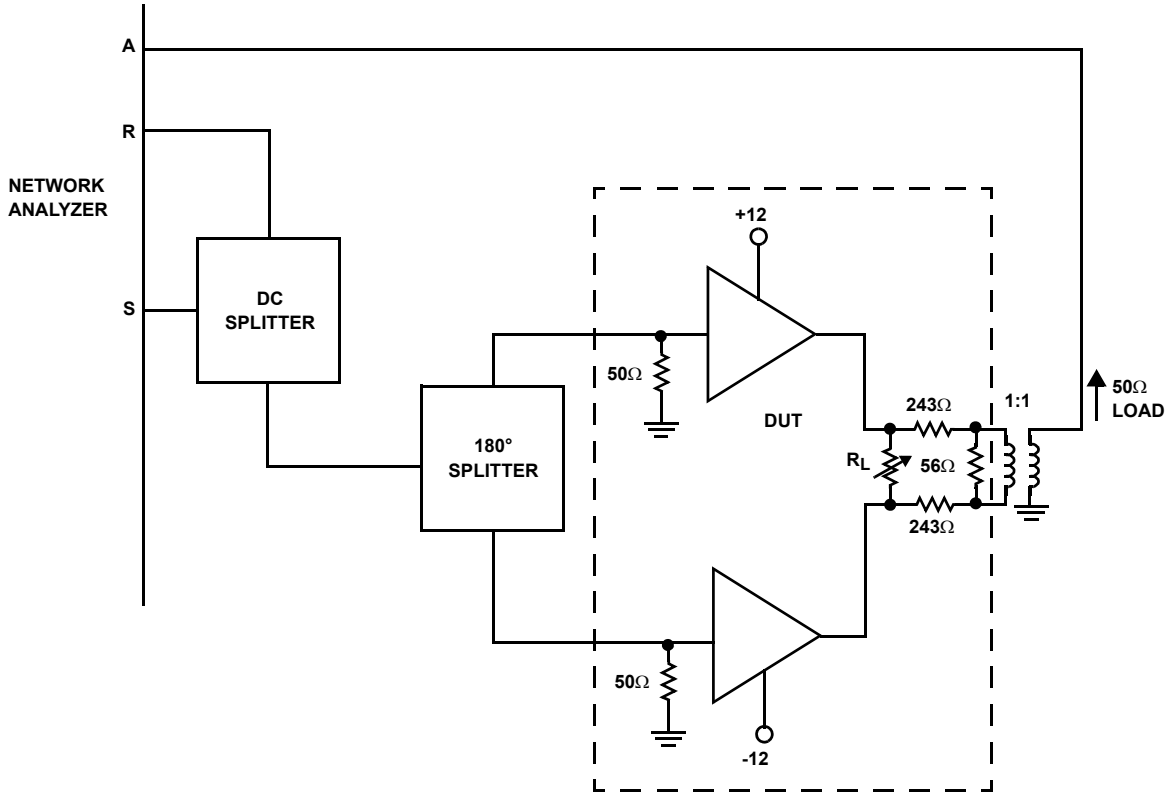


FIGURE 48. FREQUENCY RESPONSE CHARACTERIZATION CIRCUIT

Applications Information

Applying Wideband Current Feedback Op Amps as Differential Drivers

A current feedback amplifier (CFA) like the ISL1591 is particularly suited to the requirements of high output power, full power bandwidth, differential drivers. This topology offers a very high slew rate on low quiescent power. The ISL1591 is a fixed gain amplifier set to an optimized gain of 11.6V/V given R_L = 82.6 and R_b = 8.25, as shown in Figure 49.

The ISL1591 provides 4 very power efficient, high output current, CFA's. These are intended to be connected as two pairs of differential drivers. The “Connection Diagram” on page 2 shows that Channels A and B are intended to operate as a pair while Channels C and D comprise the other pair. Power control is also provided through two pairs of control pins, which separately set the power for Channels A and B together and then the other pair controls Channels C and D together.

Very low output distortion can be provided by the differential configuration. The high slew rate intrinsic to the CFA topology also contributes to the exceptional performance shown in Figures 9, 15 and 21. These swept frequency distortion plots show extremely low distortion at 200kHz holding to very low levels up through 20MHz. At the full operating power, (Figure 9, 7mA per amplifier or 14mA/port) we still see < -70dBc through 5MHz for a $5V_{P-P}$ differential output swing.

Advanced Configurations - Active Termination

Where the best power efficiency is required in a full duplex DSL line interface application, it is common to apply the circuit shown in Figure 49 to reduce the power loss in the matching loads, R_b, while retaining a higher impedance for the upstream signal coming into this output stage. This circuit acts to provide a higher apparent output impedance (through its cross-coupled positive feedback through the R_p resistors integrated internally) while physically taking a smaller I_R drop through the R_b resistors for the output signal.

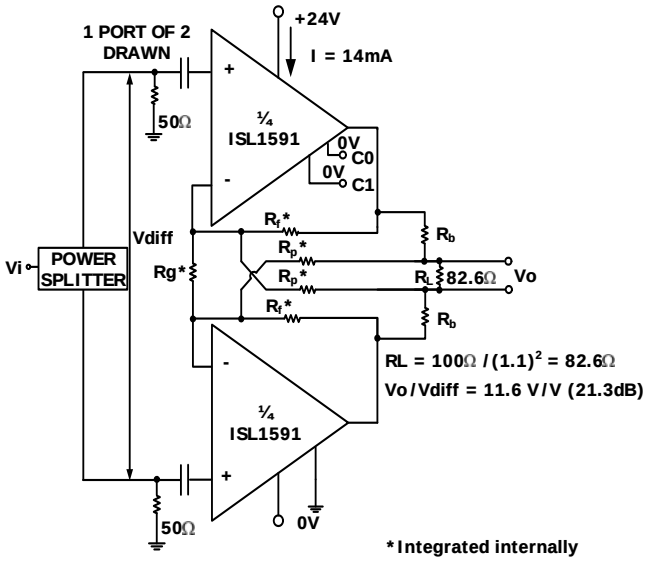


FIGURE 49. ACTIVE TERMINATION TEST CIRCUIT

Figure 49 shows one of two ports configured in an active termination circuit used for all characterization tests. This is showing the device operating in the full power mode, but data has been shown at the other power settings as well.

The 82.6Ω differential load is intended to emulate a 100Ω line load reflected through a 1:1.1 turns ratio transformer ($100\Omega/(1.1^2) = 82.6\Omega$ load). The gain and output impedance for this circuit can be described by the following equations.

The ideal transfer function is set by the open circuit gain (R_L = infinite) and an equivalent output impedance Z_O.

$$\frac{V_o}{V_i} = A_{oc}\frac{R_L}{R_L + Z_o} \quad \text{(EQ. 1)}$$

The goal of the positive feedback resistor, R_p, is to provide some "gain" in the apparent output impedance over just the $2*R_b$. It also will act to increase the A_{OC} over the simple differential gain equation if a synthesis factor (SF) is defined, as shown in Equation 2:

$$SF = \frac{1}{1 - \frac{R_f - R_b}{R_p}} \quad \text{(EQ. 2)}$$

We can see this "gain" is achieved by letting R_P be > R_F. The closer R_p is to R_f - R_b, the more "gain" is achieved but at the risk of instability. Keeping a synthesis factor of < 4 is desirable. With SF defined in Equation 2, the exact A_{OC} and Z_O will be as shown in Equations 3 and 4:

$$A_{oc} = SF\left(1 + 2\frac{R_f}{R_g} + \frac{R_f - R_m}{R_p}\right) \quad \text{(EQ. 3)}$$

$$Z_o = SF(2R_b) \quad \text{(EQ. 4)}$$

The internal resistors and external R_b resistors shown in Figure 49 were configured to achieve the following results.

SF = 3.93

A_{OC} = 20.9V/V

$Z_O = 66\Omega$

Putting these together into the gain to an 82.6Ω load gives the following test condition as shown by Equation 5.

$$\frac{V_o}{V_i} = A_{oc}\frac{R_L}{R_L + Z_o} = 20.9\frac{82.6\Omega}{82.6\Omega + 66\Omega} = 11.6\left(\frac{V}{V}\right) \quad \text{(EQ. 5)}$$

The advantage offered by this technique is that for any swing desired at the load, there is less voltage drop through the physical output matching resistor than if we simply inserted two 33Ω R_b resistors to achieve the 66Ω output impedance achieved in this test circuit. Any load current required in R_L will rise to the output pins through $2*R_b$. The voltage rise from the load swing to the output pin swing is given by Equation 6:

$$\frac{R_L + 2R_b}{R_L} \quad \text{(EQ. 6)}$$

This was a factor of 1.36 for the test circuit shown in Figure 49. Hence a ±10V swing at each output in Figure 49 will produce a $40V_{P-P}$ differential swing which will drop to the load divided by 1.36 or a $29.41V_{P-P}$ differential swing at the load.

Distortion and MTPR/MBPR

The ISL1591 is intended to provide very low distortion levels under the demanding conditions required by the discrete multi-tone (DMT) characteristic of modern DSL modulations. The standard test for linearity is the Multi-Tone Power Ratio (MTPR) test where a specified PSD profile is loaded up with discrete carriers over the specified frequencies in such a way as to produce the maximum rated line power and Peak to Average Ratio (PAR) with some tones missing. The measure of linearity is the delta between the active tones vs a missing tone. To the extent that the amplifier is slightly non-linear, it will fold a small amount of power into the missing tones through intermodulation products for the active tones. Missing band power ratio (MBPR) is a similar measurement test comparing the added non-linearity in the missing frequency bands to the nearest tone. Any non-linearity in the missing band will affect the receive path performance in a DSL system. Figure 36 shows the circuit operating at the low power setting used to test 8b VDSL2 frequency plan and power. For this test, the carriers are spaced at 5kHz.

This -62dBc average MBPR is exceptional for the very low 7mA total quiescent current used in this configuration. Operating at reduced power targets on the line will improve MBPR.

When operating in full power mode of 14mA of total quiescent current, ISL1591 can deliver better than -60dBc average MBPR for 30a VDSL2 upstream band (US3), as shown in Figure 32.

Power Control Function

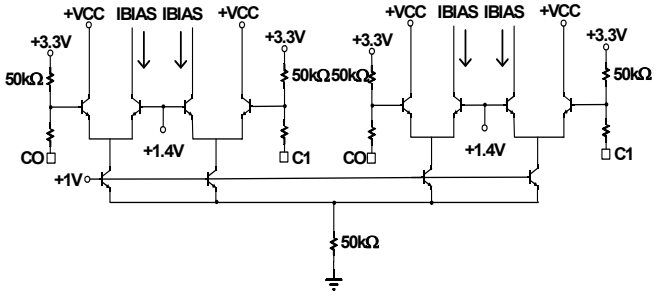


FIGURE 50. BIAS CONTROL CIRCUIT

CO_{AB} and $C1_{AB}$ control the quiescent current for the port constructed from amplifiers A and B. If both control lines are unconnected externally, the internal 50kΩ pull-up will switch the differential pairs to divert the 100µA tail currents into the supply turning off the amplifiers. Taking both control pins low will pass both I_{BIAS} lines on into scaling current sources. When C_0 and C_1 are low, the typical 14mA total quiescent current for a port is shown in the "Electrical Specification" tables on page 4. Taking C_0 high (>2V) while leaving C_1 low (<0.8V) will reduce the current into a port to a typical 9.7mA. Taking C_1 high, while leaving C_0 low will reduce the current in a port to a typical 7.4mA supply current. Table 2 summarizes the operation modes for ISL1591 for each port.

TABLE 2. POWER MODES OF THE ISL1591

C_1	C_0	OPERATION
0	0	I_S Full Power Mode
0	1	I_S Medium Power Mode
1	0	I_S Low Power Mode
1	1	Power-Down

Performance Considerations

Driving Capacitive Loads

All closed loop op amps are susceptible to reduced phase margin when driving capacitive loads. This shows up as peaking in the frequency response that can, in extreme situations, lead to oscillations. The ISL1591 is designed to operate successfully with small capacitive loads such as layout parasitics. As the parasitic capacitance increases, it is best consider a small resistor in series with the output to isolate the phase margin effects of the capacitor. Figure 23 on page 9 shows the effect of capacitive load. With 22pF on each output, we see about 6dB peaking. This will increase quickly at higher C_{LOADS}.

Output Headroom Model

Driving high voltages into heavy loads will require a careful consideration of the available output swing vs. load. Figure 51 shows a useful model for predicting the available output swing. If the output is modeled as ideal NPN and PNP transistors, the output swing limits can be described as no load headrooms (V_P and V_N) and an equivalent impedance to the supplies (R_P and R_N).

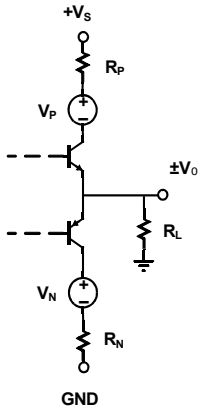


FIGURE 51. HEADROOM MODEL

The no load headrooms can be found in the "Electrical Specifications" table on page 5 as 24V - 22.4V = 1.6V giving 0.8V to each supply.

The equivalent impedances for this model can be extracted from the reduced swings shown in the specification table for the 100Ω load. Looking at the typical 100Ω load swings, we see a +21.2V swing. Solving for the two resistors in the Headroom model shown in Figure 51 gives Equation 7:

$$R_p = 2.8\Omega \text{ and } R_n = 2.8\Omega \quad \text{(EQ. 7)}$$

For the differential configuration, Figure 52 shows the Headroom model that can be used to predict the maximum available swing for a given supply voltage and load resistor, R_L.

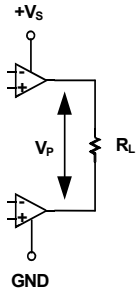


FIGURE 52. HEADROOM MODEL

For equal bipolar supplies, the available peak output swing will be given by Equation 8:

$$V_p = \frac{2(V_s - V_p - V_n)}{1 + \frac{R_p + R_n}{R_L}} \quad \text{(EQ. 8)}$$

For example, to worst case the design using +24V supplies with ±5% supply tolerance and a minimum expected load of 50Ω, a maximum V_P can be calculated as shown in Equation 9:

$$V_{peak} = \frac{(V_s - V_p - V_n)}{1 + \frac{R_p + R_n}{R_L}} = \frac{(22.8 - 1.6)}{1 + \frac{2.8\Omega + 2.8\Omega}{50\Omega}} = 19.1V_{peak} \quad \text{(EQ. 9)}$$

The minimum V_{P-P} would be twice as much, or 38.2V_{P-P}. While this extreme condition would normally not be encountered, it does show the importance of knowing your minimum expected load for high output swing conditions.

Board Design Recommendations

Close placement of the supply decoupling capacitors will minimize parasitic inductance in the supply path. High frequency load currents are typically pulled through these capacitors so close placement of 0.01µF capacitors on each of the supply pins will improve dynamic performance. Higher valued capacitors, 6.8µF typically, can be placed further from the package as they are providing more of the low frequency decoupling.

The thermal pad for the ISL1591 should be connected to either ground or the -V_S power plane. The choice of which plane depends on which one would have the more accessible thermal area.

While the ISL1591 is relatively robust in driving parasitic capacitive loads, it is always preferred to get any series output resistor needed in the design as physically close as possible to the output pins. Then trace capacitance on the other side of that resistor will have a much smaller effect on loop phase margin.

Protection devices that are intended to steer large load transients away from the ISL1591 output stage and into the power supplies or ground should have a short trace from their supply connections into the nearest supply capacitor - or should include their own supply capacitors to provide a low impedance path under fast transient conditions.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
10/30/2012	FN7625.1	page 2 , Figure 3 schematic: added resistor values and added buffer between Rc and Rt.
08/18/2011	FN7625.0	Initial Release

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

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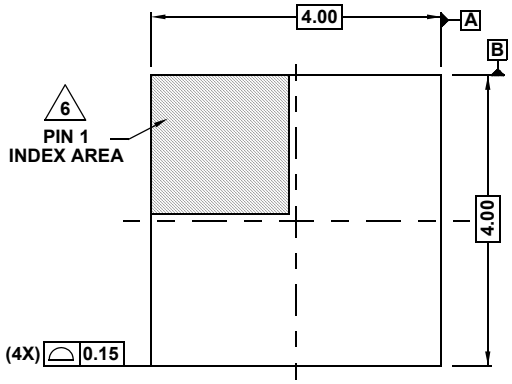
Package Outline Drawing

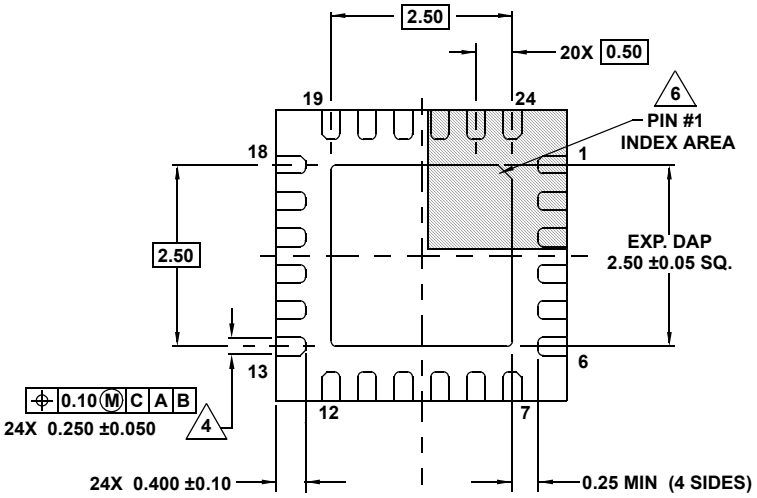
L24.4X4F

24 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE

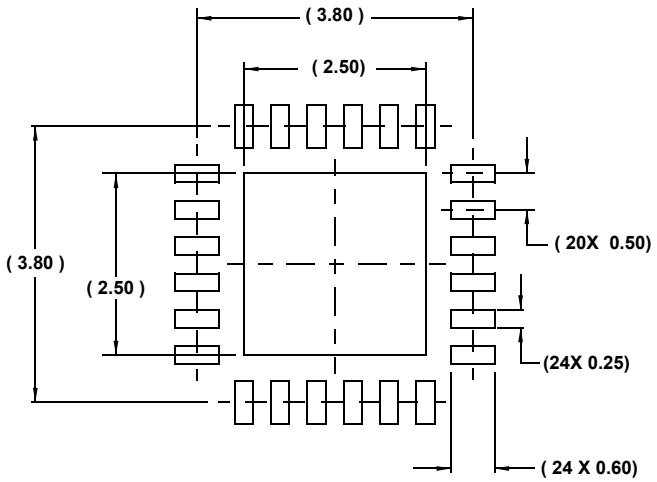
Rev 2, 1/11



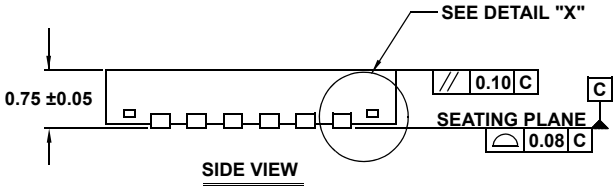
TOP VIEW



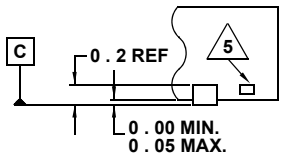
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Compliant to JEDEC MO-220 VGGD-8.