ISL28133A

Single Micro-Power, High-Precision, RRIO, CMOS Operational Amplifier

Description

The ISL28133A is a single micropower, chopper-stabilized operational amplifier designed for precision and efficiency in compact spaces. With a quiescent current of just 22µA and rail-to-rail input/output, it delivers exceptional performance across a wide supply range of 1.8V to 5.5V. Its ultra-low input offset voltage (10µV max) and minimal noise make it ideal for high-accuracy applications like medical instrumentation, temperature sensing, and electronic weigh scales.

The low supply current of 22µA and wide input range enable this device to be an excellent high-precision op amp for a wide range of application where low power is paramount.

The device operates across the temperature range of -40°C to +125°C and is available in a wide variety of packages.

Part Number	Package Description	Body Size (nom)
ISL28133A	SC70-5	1.25mm×2.00mm
	SOT-23-5	1.60mm×2.90mm

Features

- Single-Supply Operation: 1.8V to 5.5V
- Rail-To-Rail Input and Output
- Low Input Offset Voltage: ±10µV (Maximum)
- Low Offset Drift: ±0.075µV/°C (Maximum)
- 0.01Hz to 10Hz Noise: 1.1μV_{PP}
- Low Supply Current: 22µA
- Gain Bandwidth Product: 340kHz
- Unity-Gain Stable
- Temperature Range: -40°C to 125°C

Applications

- Low-Ohmic Current Sensing
- Temperature Measurement
- Precision/Strain Gauge Sensors
- High-Gain Amplifiers
- Smoke Detectors
- Appliances
- Medical Equipment
- Motor Control

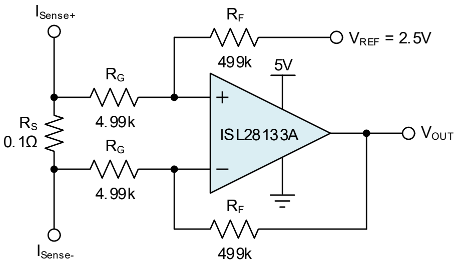


Figure 1. Typical Application Circuit - Bidirectional Current Sense Amplifier

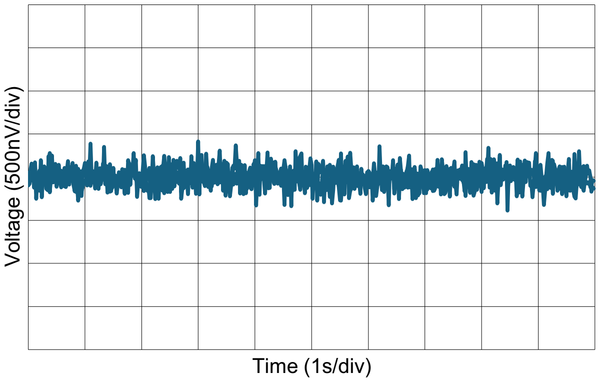


Figure 2. 0.1Hz to 10Hz Noise

Contents

1. Pin Information

1.1 Pin Assignments

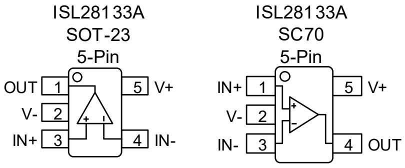


Figure 3. Pin Assignments – Top View

1.2 Pin Descriptions

Pin Name	ISL28133A	ISL28133A	Function
	SOT-23	SC70	
IN+	3	1	Non-inverting Signal Input
IN1+	–	–	
IN2+	–	–	
IN3+	–	–	
IN4+	–	–	
IN-	4	3	Inverting Signal Input
IN1-	–	–	
IN2-	–	–	
IN3-	–	–	
IN4-	–	–	
OUT	1	4	Signal Output
OUT1	–	–	
OUT2	–	–	
OUT3	–	–	
OUT4	–	–	
V+	5	5	Positive Supply Voltage
V-	2	2	Negative Supply Voltage

2. Specifications

2.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
Supply Voltage, V+ to V-	-	6.0	V
Input Voltage, IN± to GND	-0.5	6.0	V
Input Voltage, IN+ to IN-	-	6.0	V
Input Current	-	20	mA
Output Short-Circuit	Continuous		mA
Ambient Temperature, T_A	-40	125	°C
Junction Temperature, T_J	-	150	°C
Storage Temperature, T_{stg}	-65	150	°C
ESD Ratings			
Human-Body Model (HBM), per ANSI/ESDA/JEDEC JS-001	-	±2	kV
Charged-Device Model (CDM), per JEDEC specification JESD22-C101	-	±2	kV
Latch-Up (Tested per JESD78B), T_A = 125°C	-	±100	mA

2.2 Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Supply Voltage [(V+) – (V-)]	V_S	1.8	5.5	V
Input Voltage Range	V_I	(V-) – 0.1	(V+) + 0.1	V
Output Voltage range	V_O	V-	V+	V
Ambient Temperature	T_A	-40	125	°C

2.3 Thermal Specifications

Parameter	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance	5 Ld SOT-23 Package	θ_{JA}[1]	Junction to ambient	188	°C/W
		θ_{JC}[2]	Junction to case	137	°C/W
Thermal Resistance	5 Ld SC-70 Package	θ_{JA}[1]	Junction to ambient	227	°C/W
		θ_{JC}[2]	Junction to case	141	°C/W

1. θ_{JA} is measured with the component mounted on a high-effective thermal conductivity test board in free air. See TB379 for details.
2. For θ_{JC}, the case temperature location is taken at the package top center.

2.4 Electrical Specifications

V_S = (V+) – (V-) = 5V at T_A = 25°C, R_L = 10kΩ connected to $V_S/2$, V_{CM} = $V_S/2$ (unless otherwise noted)

Parameter	Symbol	Test Condition	Min[1]	Typ	Max[1]	Unit
DC Parameters						
Input Offset Voltage	V_{OS}	V_S = 5V, V_{CM} = 2.5V	-	±2	±10	µV
		T_A = -40°C to 125°C	-	-	±17	µV

V_S = (V+) – (V-) = 5V at T_A = 25°C, R_L = 10kΩ connected to V_S/2, V_{CM} = V_S/2 (unless otherwise noted)

Parameter	Symbol	Test Condition	Min[1]	Typ	Max[1]	Unit
Input Offset Voltage Temperature Coefficient	TCV_{OS}	T_A = -40°C to 125°C	-	0.02	0.075	µV/°C
Input Bias Current	I_B	T_A = -40°C to 125°C	-	±37	±600	pA
Input Offset Current	I_{OS}	T_A = -40°C to 125°C	-	±73	±400	pA
Common-Mode Input Range	V_{ICM}	V_S = 1.8V to 5.5V	(V_S-) - 0.1	-	(V_S+) + 0.1	V
Common-Mode Rejection Ratio	CMRR	V_S = 1.8V to 5.5V, T_A = -40°C to 125°C (V-) - 0.1V < VCM < (V+) + 0.1V	106	127	-	dB
Power Supply Rejection Ratio	PSRR	V_S = 1.8V to 5.5V, T_A = -40°C to 125°C	106	124	-	dB
Open-Loop Gain	A_{OL}	(V-) + 100mV < V_O < (V+) – 100mV, R_L = 10kΩ, T_A = -40°C to 125°C	106	143	-	dB
Output Voltage Swing from Rails	V_{OFR+}	R_L = 10kΩ, T_A = -40°C to 125°C	-	28	70	mV
	V_{OFR-}	R_L = 10kΩ, T_A = -40°C to 125°C	-	24	70	mV
Sourcing Short-Circuit Current	I_{SC+}	V_{OUT} connected to V-	-	19	30	mA
Sinking Short-Circuit Current	I_{SC-}	V_{OUT} connected to V+	-35	-14	-	mA
Supply Current per Amplifier	I_Q	R_L = ∞, T_A = -40°C to 125°C	-	22	35	µA
AC Parameters						
Input Noise Voltage	E_n	f = 0.01 to 1Hz	-	0.9	-	$µV_{pp}$
		f = 0.1 to 10Hz	-	1.1	-	$µV_{pp}$
Voltage Noise Density	e_n	f = 1kHz	-	43.5	-	nV/√Hz
Current Noise Density	i_n	f = 10Hz	-	76	-	fA/√Hz
Gain Bandwidth Product	GBW	G = 100, R_L = 10kΩ	-	340	-	kHz
Transient Response						
Positive Slew Rate	SR+	V_{OUT} = 1V to 4V, R_L = 10kΩ, G = 1	-	0.2	-	V/µs
Negative Slew Rate	SR-	V_{OUT} = 1V to 4V, R_L = 10kΩ, G = 1	-	0.2	-	V/µs
Settling Time to 0.1% V_O	t_S	V_S = ±2.5V, G =1, 2V-Step, C_L = 1.2pF	-	22.5	-	µs

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.

3. Typical Performance Graphs

V_S = 5V (±2.5V) at T_A = 25°C, RL = 10kΩ connected to $V_S/2$, V_{CM} = $V_S/2$ (unless otherwise noted)

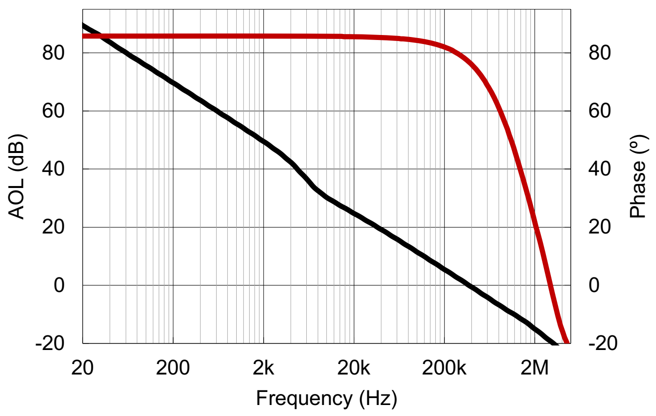


Figure 4. Open-Loop Gain and Phase vs Frequency

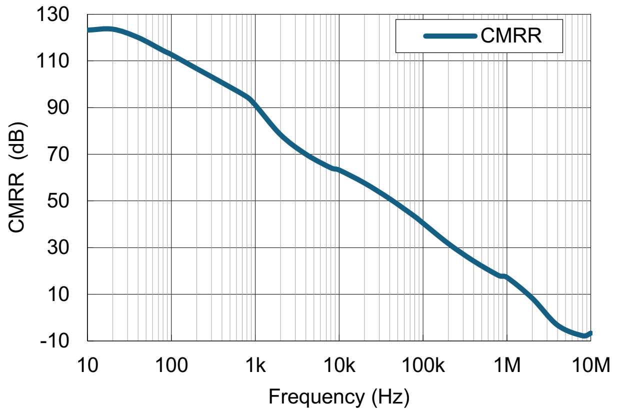


Figure 5. CMRR vs Frequency

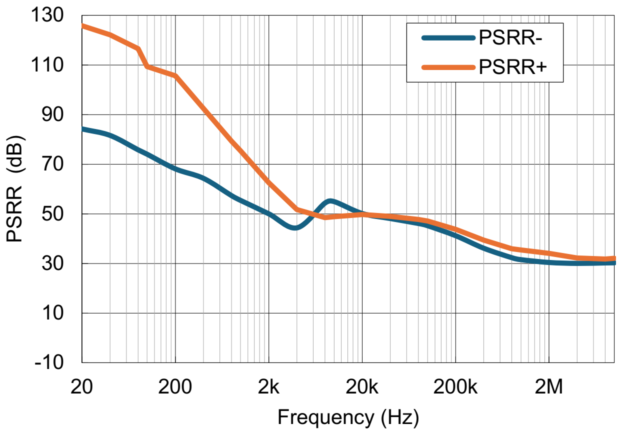


Figure 6. PSRR vs Frequency

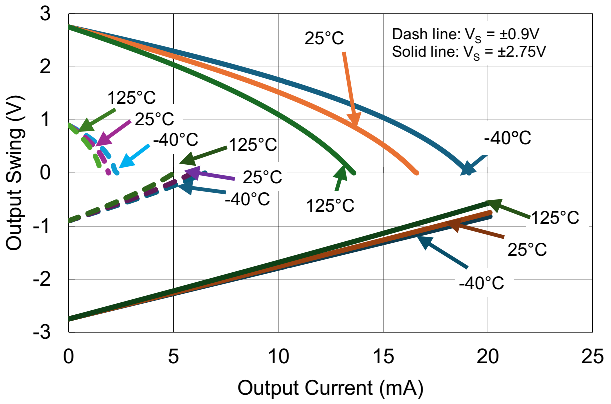


Figure 7. Output Voltage Swing vs Output Current

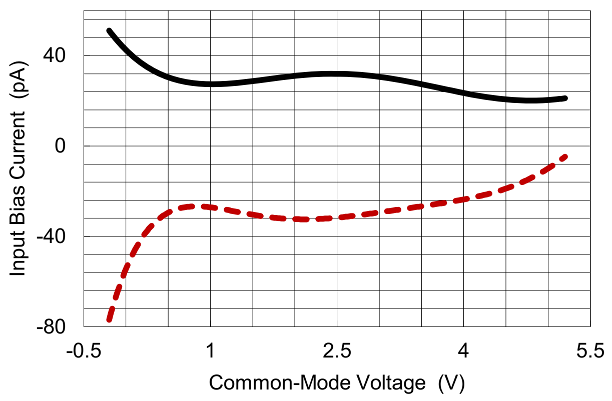


Figure 8. Input Bias Current vs Common-Mode Voltage

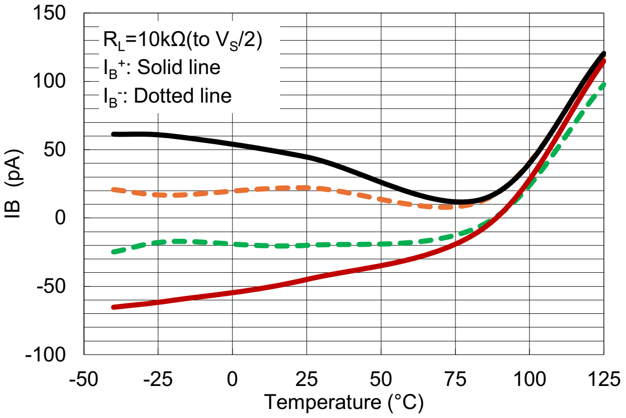


Figure 9. Input Bias Current vs Temperature

V_S = 5V (±2.5V) at T_A = 25°C, RL = 10kΩ connected to $V_S/2$, V_{CM} = $V_S/2$ (unless otherwise noted) (Cont.)

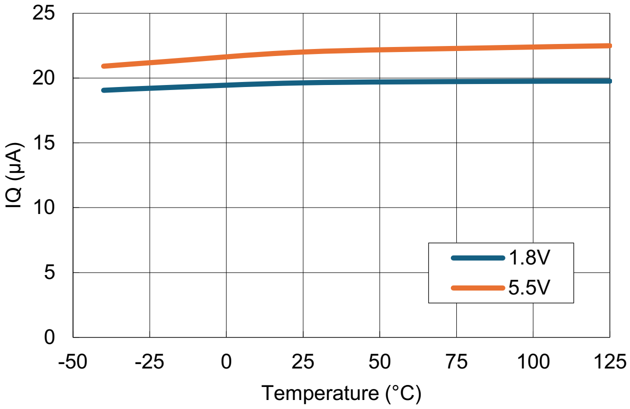


Figure 10. Quiescent Current vs Temperature

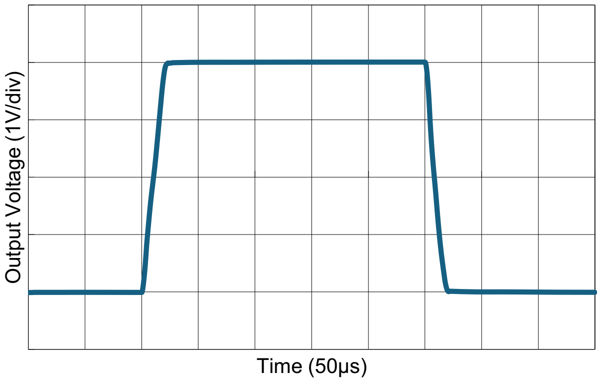


Figure 11. Large Signal Step Response

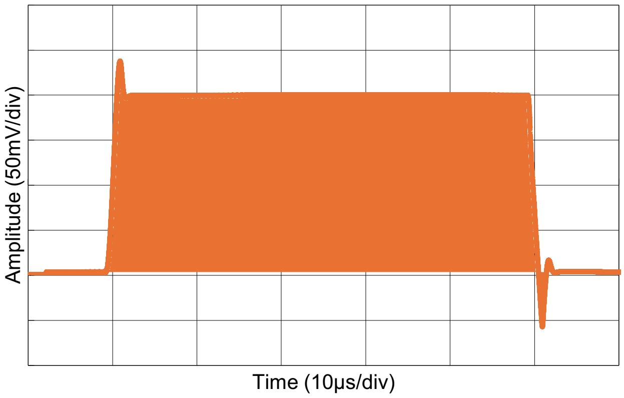


Figure 12. Small Signal Step Response

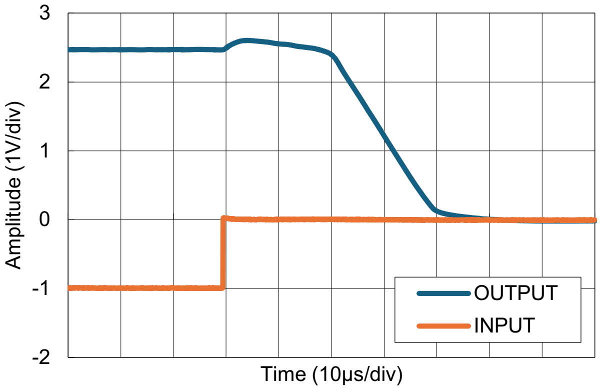


Figure 13. Positive Overvoltage Recovery

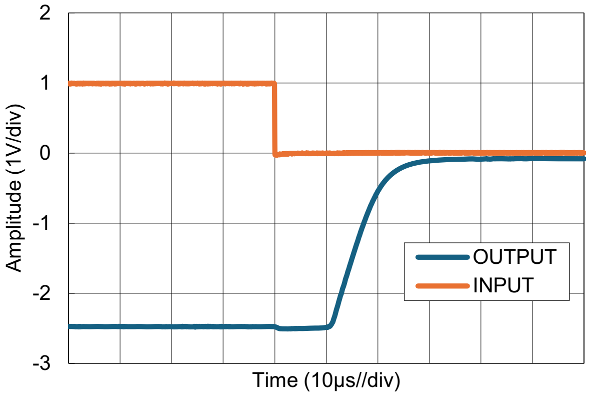


Figure 14. Negative Overvoltage Recovery

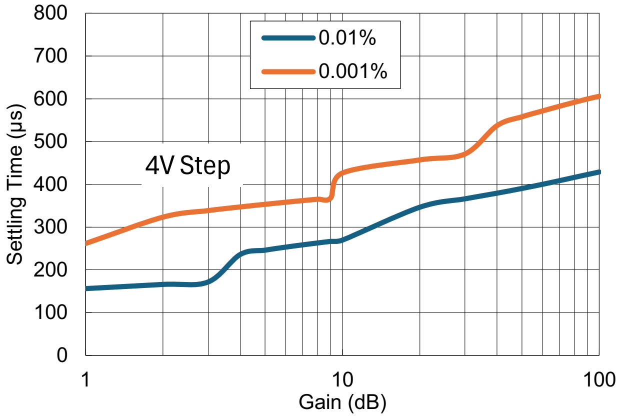


Figure 15. Settling Time vs Closed-Loop Gain

V_S = 5V (±2.5V) at T_A = 25°C, RL = 10kΩ connected to $V_S/2$, V_{CM} = $V_S/2$ (unless otherwise noted) (Cont.)

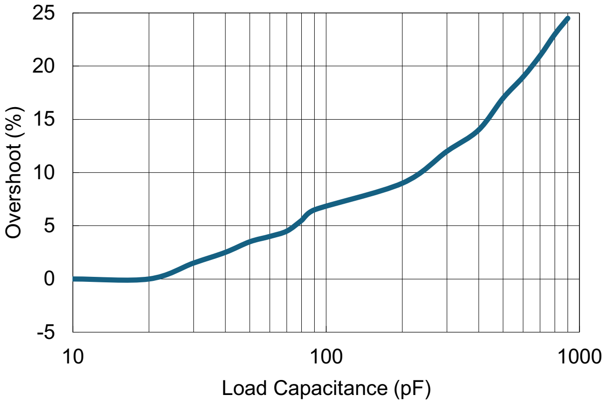


Figure 16. Small Signal Overshoot vs Load Capacitance

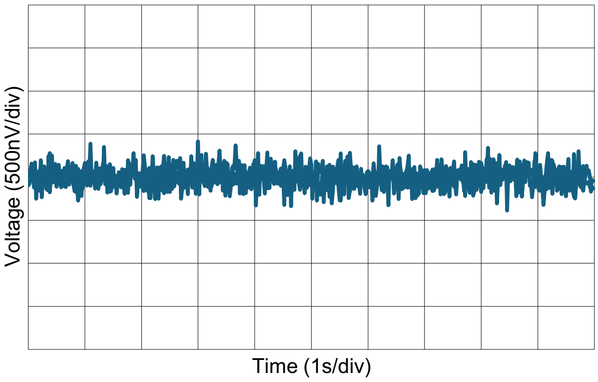


Figure 17. 0.1Hz to 10Hz Noise

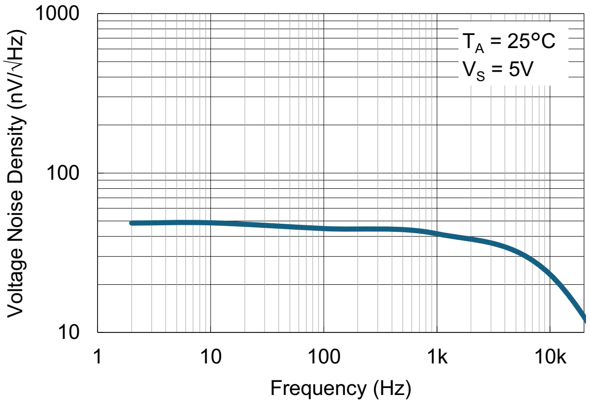


Figure 18. Voltage Noise Spectral Density

4. Detailed Description

4.1 Overview

The ISL28133A auto-zero operational amplifier (op amp) is a low-power device with rail-to-rail input and outputs. This op amp operates from supply voltages as low as 1.8V up to 5.5V. The device is unity-gain stable and designed for a wide range of precision and general-purpose applications.

Its input common-mode voltage range extends 100mV above and below the power supply voltage rails, allowing this op amp to be used in virtually any single-supply application. The rail-to-rail input and output swing capability increases the signal dynamic range and therefore, signal-to-noise ratio, a performance feature highly necessary in low-supply applications. The combination of low-offset voltage and low drift over temperature and time makes this device ideal for the use in high-gain amplifiers and precision sensor signal conditioners.

4.2 Functional Block Diagram

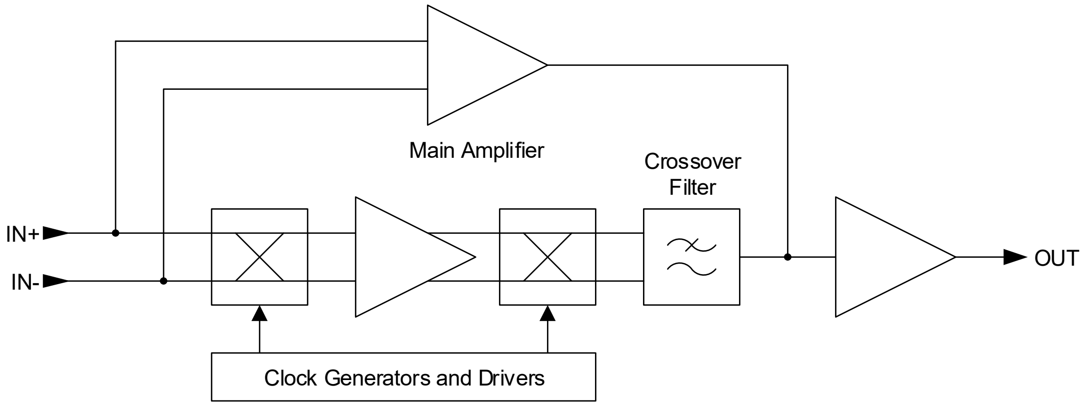


Figure 19. Block Diagram of a Single Amplifier Stage

4.3 Feature Description

4.3.1 Low Offset and Drift

The ISL28133A device uses a proprietary chopper-stabilized technique that combines a 340kHz main amplifier with a high open-loop gain chopper amplifier to achieve low offset voltage and drift, while consuming only 22µA of supply current per channel.

This multi-path amplifier architecture contains a time continuous main amplifier whose DC offset input is corrected by a parallel connected, high gain chopper stabilized DC correction amplifier operating at 100kHz. From DC to about 5kHz, both amplifiers are active with DC offset correction and most of the low frequency gain is provided by the chopper amplifier. A 5kHz crossover filter cuts off the low frequency amplifier path, leaving the main amplifier active out to the 340kHz gain-bandwidth product of the device.

The key benefits of this architecture for precision applications are very high open-loop gain, very low DC offset, and low 1/f noise. The noise is virtually flat across the frequency range from a few millihertz out to 100kHz, except for the narrow noise peak at the amplifier crossover frequency.

4.3.2 Rail-To-Rail Input and Output (RRIO)

The RRIO CMOS amplifier uses parallel input PMOS and NMOS that enable the inputs to swing 100mV beyond either supply rail. The inverting and non-inverting inputs do not have back-to-back input clamp diodes and can maintain high input impedance at high differential input voltages. This is effective in eliminating output distortion caused by high slew-rate input signals.

The output stage uses common source connected PMOS and NMOS devices to achieve rail-to-rail output drive capability within 17mA current limit and the capability to swing to within 25mV of either rail while driving a 10kΩ load.

4.3.3 Layout Guidelines for High Impedance Inputs

To achieve the maximum performance of the high input impedance and low offset voltage of the ISL28133A amplifier, care should be taken in the circuit board layout. The surface of the printed circuit board must remain clean and free of moisture to avoid leakage-currents between adjacent traces. Surface coating of the circuit board reduces surface moisture and provides a humidity barrier, reducing parasitic resistance on the board.

4.3.4 Input and Output ESD Protection

ISL28133A incorporates internal ESD protection circuits on all pins. For the input and output pins, this protection primarily consists of current-steering diodes that are connected between the input and output pins and the power-supply pins. If the input voltage is expected to exceed the specified value in the Absolute Maximum Ratings, insert a series resistor (R_S) to limit the input current to about 20mA (Figure 20).

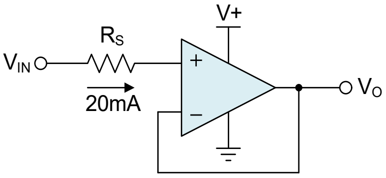


Figure 20. Input Current Protection

5. Application Information

The ISL28133A features 340kHz gain-bandwidth and 0.2V/µs slew rate with only 22µA of supply current per channel. Its low input offset of 2µV enables the design of DC-coupled high-gain amplifiers. However, care must be applied when designing for maximum dynamic output range to prevent signal distortions due to the low slew rate. Also, PCB layout considerations are different to that of a standard op amp.

5.1 Typical Applications

5.1.1 High Gain, Precision DC-Coupled Amplifier

The circuit in Figure 21 implements a single-stage DC-coupled amplifier with an input DC sensitivity of under 100nV that is only possible using a low V_{OS} amplifier with high open-loop gain. High gain DC amplifiers operating from low voltage supplies are not practical using typical low offset precision op amps. For example, a typical precision amplifier in a gain of 10kV/V with a ±100µV V_{OS} and an offset drift of 0.5µV/°C of a low offset op amp would produce a DC error of >1V with an additional 5mV/°C of temperature dependent error, making it difficult to resolve DC input voltage changes in the mV range.

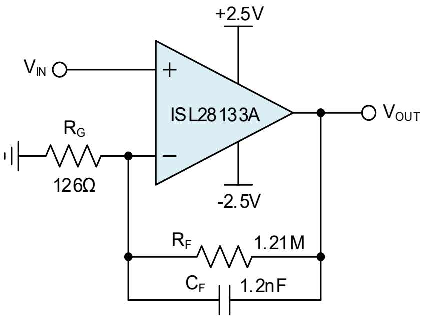


Figure 21. High-Gain, Precision DC-Coupled Amplifier with ISL28133A

The ±10µV max V_{OS} and 0.075µV/°C maximum temperature drift of the ISL28133A produces a temperature stable maximum DC output error of only ±100mV with a maximum output temperature drift of 0.75mV/°C. The additional benefit of a low 1/f noise corner frequency and some feedback filtering enables DC voltages and voltage fluctuations well below 100nV to be easily detected with a simple single stage amplifier.

5.1.2 Design Procedure

The following are design requirements for this design:

- Input voltage and frequency range: V_{IN} = 0 to 500µV_{P-P}, f_{IN} = 0 to 10Hz
- Required Signal output range: V_O = 0 to 4.8V_{P-P}
- Low-pass filter cut-off frequency: f_C = 100Hz

The signal gain of the amplifier is:

(EQ. 1)
$$G = \frac{V_O}{V_{IN}} = \frac{4.8V_{P\text{-}P}}{500\mu V_{P\text{-}P}} = 9600\text{V/V or }96.65\text{dB}$$

This gain is defined by the feedback and gain resistors, R_F and R_G, with G = 1+ R_F/R_G. Solving for the resistor ratio gives:

(EQ. 2)
$$R_F / R_G = G - 1 = 9599$$

Making R_F = 1.21MΩ and R_G = 126Ω yields a gain of 9604 and therefore, a gain error of 0.04%.
The cut-off frequency of the low-pass filter is defined by $f_C = 1/(2\pi \times C_F \times R_F)$. Solving for C_F gives:

(EQ. 3)
$$C_F = \frac{1}{2\pi \times f_C \times R_F} = \frac{1}{2\pi \times 100\text{Hz} \times 1.21\text{M}\Omega} = 13.15\text{nF}$$

Selecting the closest standard value makes C_F = 12nF, resulting in a cut-off frequency of f_C = 109Hz.

Figure 22 shows the gain response of the high-gain amplifier using ISL28133A in comparison with the gain response of an ideal op amp. *Note*: The output impedance of low-power CMOS op amps increases significantly at high frequencies. This causes the gain response to divert from theoretical response, which assumes an op amp output impedance of Z_O = 0Ω.

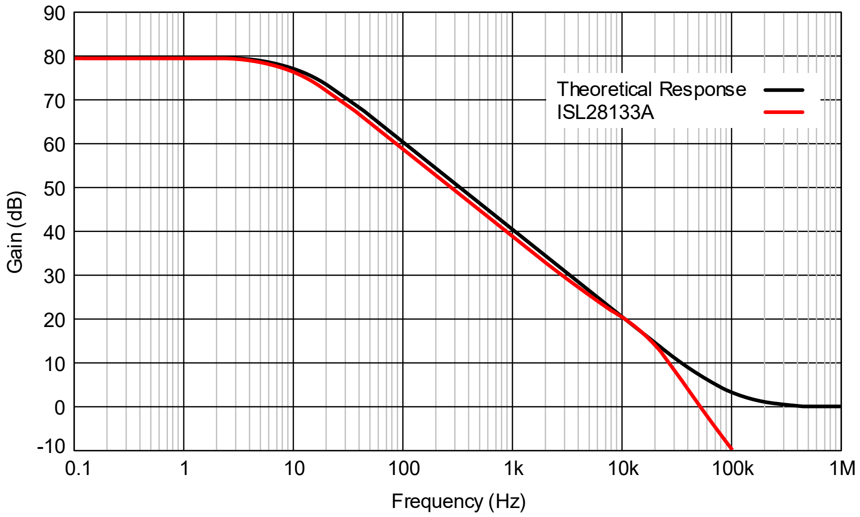


Figure 22. High-Gain Amplifier Frequency Response

5.2 Layout Considerations

When using the highest-precision amplifier available, the overall accuracy of your application might still fall short of expectations. Specifically, employing an auto-zero amplifier often shifts the precision limitation from the amplifier itself to the design and layout of the printed circuit board (PCB).

One significant contributor to offset voltage errors on a PCB is thermoelectric voltage, commonly referred to as thermocouple or Seebeck voltage. This voltage is generated at the junction between two dissimilar metals and is directly proportional to the junction temperature. The magnitude of Seebeck voltage varies considerably depending on the specific metals involved, typically ranging from microvolts up to millivolts. Additionally, temperature-induced variations in these voltages can span from several microvolts to tens of microvolts per degree Celsius.

Typical metallic junctions found on PCBs include solder-to-trace interfaces and solder-to-component lead connections. If a temperature gradient exists across the PCB, resulting in different temperatures at each end of a component, the resulting Seebeck voltages differs, thereby producing a thermal voltage error. Figure 23 illustrates this scenario.

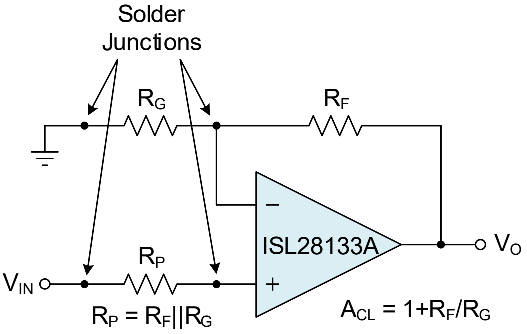


Figure 23. Using Dummy Resistor minimizes Offset Errors due to Seebeck Voltages and Bias Currents

In a high-gain configuration, where feedback resistor (R_F) is significantly larger than gain resistor (R_G), any difference in Seebeck voltages appearing across R_G manifests as an offset voltage directly at the amplifier's inverting input. This initial offset voltage is subsequently amplified by the closed-loop gain, therefore causing a substantially larger output voltage error.

Thermocouple errors can be mitigated by using a dummy component to match the thermoelectric error source. For instance, adding a resistor (R_P) in series with the non-inverting input does not impact the amplifier's AC performance but, when placed physically close to R_G, ensures that their Seebeck potentials are closely matched, thereby minimizing thermocouple-induced errors. Matching R_P to the parallel combination of R_G and R_F further reduces offset errors caused by input bias currents.

The Seebeck voltage difference across the feedback resistor (R_F) is less critical because this error appears directly at the output and is not amplified by the closed-loop gain.

Another effective approach for reducing offset errors due to Seebeck voltages is maintaining a uniform ambient temperature across the PCB. Implementing a ground plane helps distribute heat evenly throughout the PCB and provides additional benefits, such as reducing susceptibility to electromagnetic interference (EMI).

The PCB surface should be clean and moisture-free to prevent leakage currents between adjacent traces. Applying a surface coating creates a humidity barrier, reducing surface moisture and thereby minimizing parasitic resistance on the board.

Further reduction of leakage currents can be achieved by using guard rings around the amplifier inputs. While the guard rings do not require a specific width, each guard ring should form a continuous loop around the inverting and non-inverting inputs of the amplifier. By setting the guard ring voltage equal to the voltage at the non-inverting input, both parasitic resistance and capacitance are effectively reduced.

6. Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

7. Ordering Information

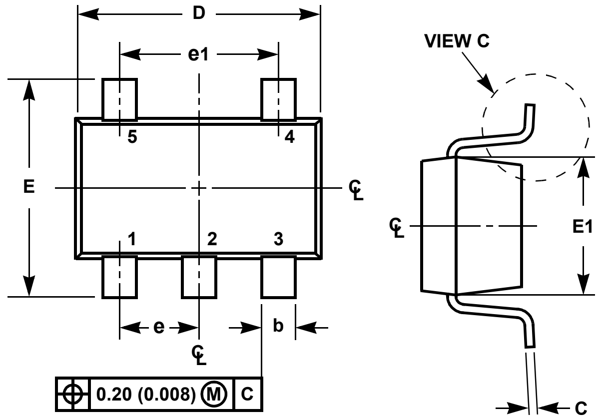
Part Number[1]	# Channels	Part Marking	Package Description[2] (RoHS Compliant)	Pkg. Dwg. #	Carrier Type[3]	MSL Rating[4]	Temp. Range
ISL28133AFEZ-T7	1	133[5]	SC70-5	P5.049	Reel, 3k	1	-40 to 125°C
ISL28133AFHZ-T7	1	133A[5]	SOT-23-5	P5.064	Reel, 3k	1	-40 to 125°C

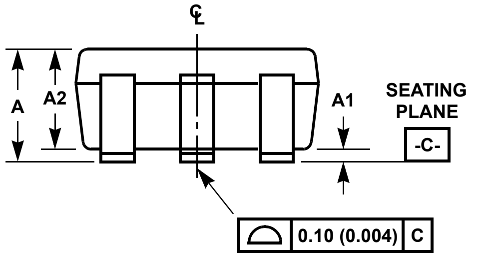
1. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. For the Pb-Free Reflow Profile, see TB493.
3. See TB347 for details about reel specifications.
4. Moisture Sensitivity Level (MSL) tested per JEDEC J-STD-020. For more information about MSL, see TB363.
5. The part marking is located on the bottom of the part.

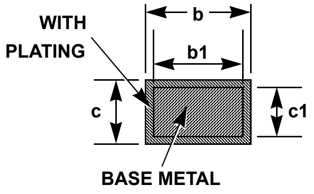
8. Revision History

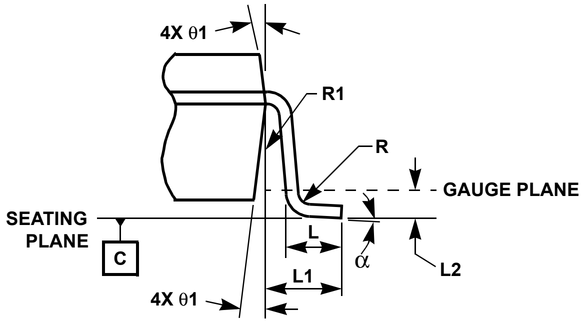
Revision	Date	Description
1.00	Jul 8, 2025	Initial release.

Small Outline Transistor Plastic Packages (SC70-5)

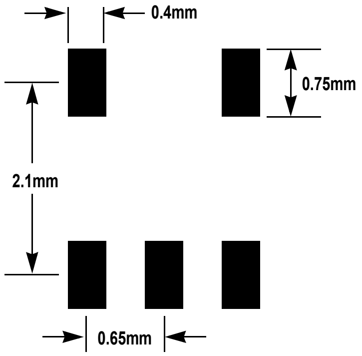








VIEW C



TYPICAL RECOMMENDED LAND PATTERN

P5.049

5 LEAD SMALL OUTLINE TRANSISTOR PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.031	0.043	0.80	1.10	-
A1	0.000	0.004	0.00	0.10	-
A2	0.031	0.039	0.80	1.00	-
b	0.006	0.012	0.15	0.30	-
b1	0.006	0.010	0.15	0.25	
c	0.003	0.009	0.08	0.22	6
c1	0.003	0.009	0.08	0.20	6
D	0.073	0.085	1.85	2.15	3
E	0.071	0.094	1.80	2.40	-
E1	0.045	0.053	1.15	1.35	3
e	0.0256 Ref		0.65 Ref		-
e1	0.0512 Ref		1.30 Ref		-
L	0.010	0.018	0.26	0.46	4
L1	0.017 Ref.		0.420 Ref.		-
L2	0.006 BSC		0.15 BSC		
α	0^o	8^o	0^o	8^o	-
N	5		5		5
R	0.004	-	0.10	-	
R1	0.004	0.010	0.15	0.25	

Rev. 3 7/07

NOTES:

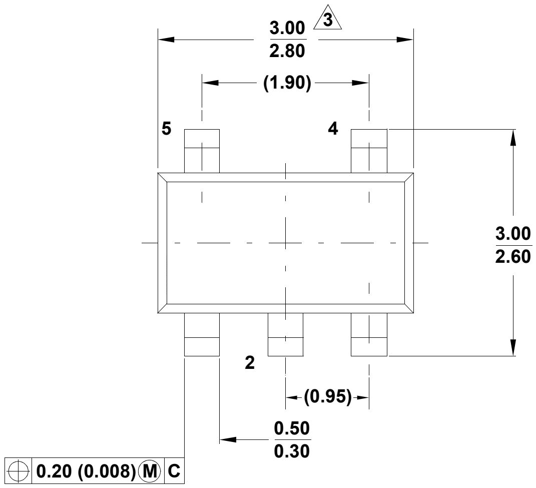
1. Dimensioning and tolerances per ASME Y14.5M-1994.
2. Package conforms to EIAJ SC70 and JEDEC MO-203AA.
3. Dimensions D and E1 are exclusive of mold flash, protrusions, or gate burrs.
4. Footlength L measured at reference to gauge plane.
5. “N” is the number of terminal positions.
6. These Dimensions apply to the flat section of the lead between 0.08mm and 0.15mm from the lead tip.
7. Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only.

Package Outline Drawing

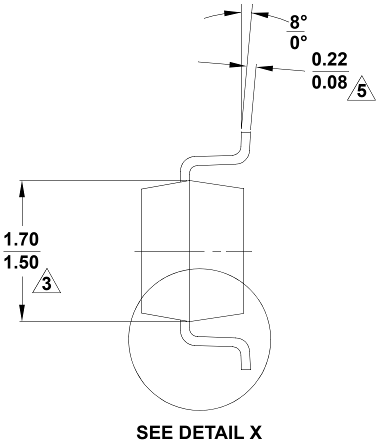
P5.064

5 LEAD SMALL OUTLINE TRANSISTOR PLASTIC PACKAGE

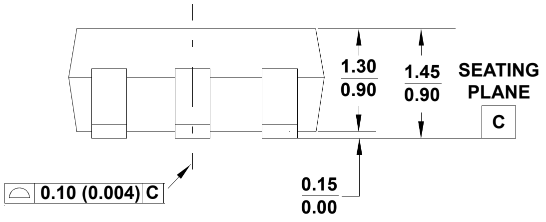
Rev 3, 4/11



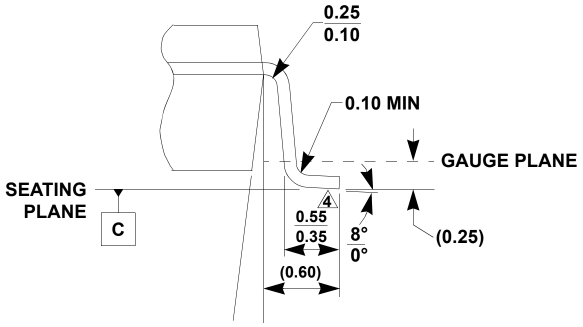
TOP VIEW



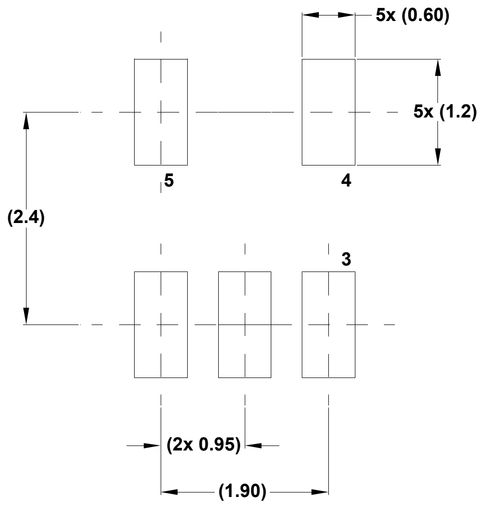
END VIEW



SIDE VIEW



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensioning and tolerance per ASME Y14.5M-1994.
2. Package conforms to EIAJ SC-74 and JEDEC MO178AA.
3. Package length and width are exclusive of mold flash, protrusions, or gate burrs.
4. Footlength measured at reference to gauge plane.
5. Lead thickness applies to the flat section of the lead between 0.08mm and 0.15mm from the lead tip.
6. Controlling dimension: MILLIMETER.
   Dimensions in ( ) for reference only.

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