ISL28133A, ISL28233A, ISL28433A

Single/Dual/Quad Micro-Power, High-Precision, RRIO, CMOS Operational Amplifiers

Description

The ISL28133A, ISL28233A, and ISL28433A are single, dual and quad micropower, chopper-stabilized operational amplifiers designed for precision and efficiency in compact spaces. With a quiescent current of just 22µA and rail-to-rail input/output, they deliver exceptional performance across a wide supply range of 1.8V to 5.5V. Their ultra-low input offset voltage (10µV max) and minimal noise make them ideal for high-accuracy applications like medical instrumentation, temperature sensing, and electronic weigh scales.

The low supply current of 22µA and wide input range enable these devices to be an excellent high-precision op amps for a wide range of application where low power is paramount.

All devices operate across the temperature range of -40°C to +125°C and are available in a wide variety of packages.

Part Number	Package Description	Body Size (nom)
ISL28133A	5-SC70	1.25mm×2.00mm
	5-SOT23	1.60mm×2.90mm
ISL28233A	8-MSOP	3.00mm×3.00mm
	8-SOICN	3.91mm×4.90mm
	8-DFN	2.00mm×2.00mm
ISL28433A	14-SOICN	3.90mm×8.65mm
	14-TSSOP	4.40mm×5.00mm

Features

- Single-supply operation: 1.8V to 5.5V
- Rail-to-rail input and output
- Low input offset voltage: ±10µV (Maximum)
- Low offset drift: ±0.075µV/°C (Maximum)
- 0.01Hz to 10Hz noise: 1.1μV_{PP}
- Low supply current: 22µA
- Gain bandwidth: 340kHz
- Unity-gain stable
- Temperature range: -40°C to 125°C

Applications

- Low-ohmic current sensing
- Temperature measurement
- Precision/strain gauge sensors
- High-gain amplifiers
- Smoke detectors
- Appliances
- Medical equipment
- Motor control

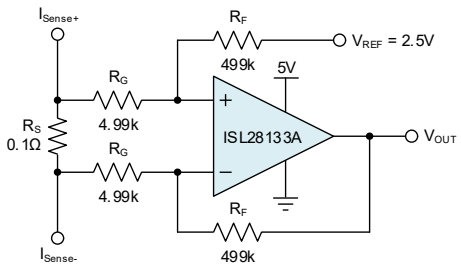


Figure 1. Typical Application Circuit - Bidirectional Current Sense Amplifier

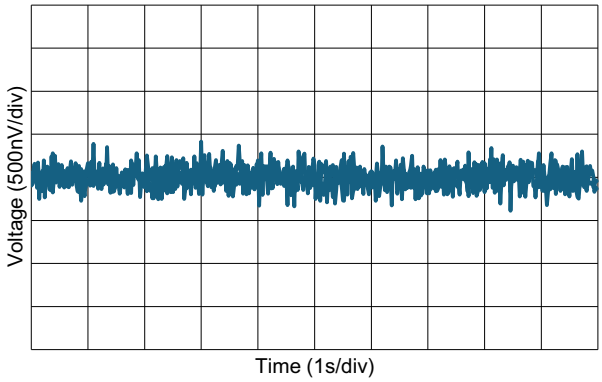


Figure 2. 0.1Hz to 10Hz Noise

Contents

1. Pin Information

1.1 5-Pin SC70

1.1.1 Pin Assignments

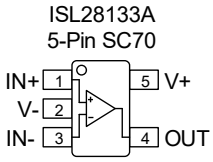


Figure 3. Pin Assignments – Top View

1.1.2 Pin Descriptions

Pin Number	Pin Name	Function
1	IN+	Non-inverting Signal Input
3	IN-	Inverting Signal Input
4	OUT	Signal Output
5	V+	Positive Supply Voltage
2	V-	Negative Supply Voltage

1.2 5-Pin SOT23

1.2.1 Pin Assignments

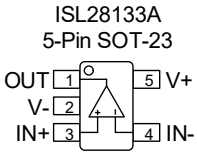


Figure 4. Pin Assignments – Top View

1.2.2 Pin Descriptions

Pin Name	Pin Name	Function
1	OUT	Signal Output
2	V-	Negative Supply Voltage
3	IN+	Non-inverting Signal Input
4	IN-	Inverting Signal Input
5	V+	Positive Supply Voltage

1.3 8-Pin DFN

1.3.1 Pin Assignments

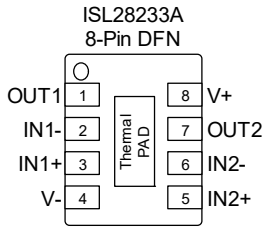


Figure 5. Pin Assignments – Top View

1.3.2 Pin Descriptions

Pin Number	Pin Name	Function
1	OUT1	Signal Output
2	IN1-	Inverting Signal Input
3	IN1+	Non-inverting Signal Input
4	V-	Negative Supply Voltage
5	IN2+	Non-inverting Signal Input
6	IN2-	Inverting Signal Input
7	OUT2	Signal Output
8	V+	Positive Supply Voltage
EPAD	V-	Connect the EPAD to V- or left floating for temperature dissipation. (DFN package only)

1.4 8-Pin SOIC, MSOP

1.4.1 Pin Assignments

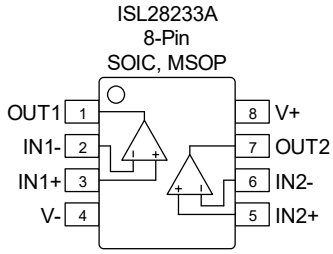


Figure 6. Pin Assignments – Top View

1.4.2 Pin Descriptions

Pin Number	Pin Name	Function
1	OUT1	Signal Output
2	IN1-	Inverting Signal Input
3	IN1+	Non-inverting Signal Input
4	V-	Negative Supply Voltage
5	IN2+	Non-inverting Signal Input
6	IN2-	Inverting Signal Input

Pin Number	Pin Name	Function
7	OUT2	Signal Output
8	V+	Positive Supply Voltage

1.5 14-Pin SOIC, TSSOP

1.5.1 Pin Assignments

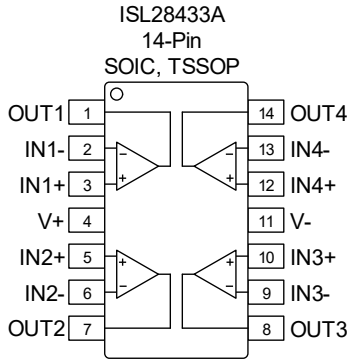


Figure 7. Pin Assignments – Top View

1.5.2 Pin Descriptions

Pin Number	Pin Name	Function
1	OUT1	Signal Output
2	IN1-	Inverting Signal Input
3	IN1+	Non-inverting Signal Input
4	V+	Positive Supply Voltage
5	IN2+	Non-inverting Signal Input
6	IN2-	Inverting Signal Input
7	OUT2	Signal Output
8	OUT3	Signal Output
9	IN3-	Inverting Signal Input
10	IN3+	Non-inverting Signal Input
11	V-	Negative Supply Voltage
12	IN4+	Non-inverting Signal Input
13	IN4-	Inverting Signal Input
14	OUT4	Signal Output

2. Specifications

2.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
Supply Voltage, V+ to V-	-	6.0	V
Input Voltage, IN± to GND	-0.5	6.0	V
Input Voltage, IN+ to IN-	-	6.0	V
Input Current	-	20	mA
Output Short-Circuit	Continuous		mA
Ambient Temperature, T_A	-40	125	°C
Junction Temperature, T_J	-	150	°C
Storage Temperature, T_{stg}	-65	150	°C
ISL28133A ESD Ratings			
Human-Body Model (HBM), per ANSI/ESDA/JEDEC JS-001	-	±2	kV
Charged-Device Model (CDM), per JEDEC specification JS-002	-	±2	kV
Latch-Up (Tested per JESD78), T_A = 125°C	-	±100	mA
ISL28233A, ISL28433A ESD Ratings			
Human-Body Model (HBM), per ANSI/ESDA/JEDEC JS-001	-	±6	kV
Charged-Device Model (CDM), per JEDEC specification JS-002	-	±1.5	kV
Latch-Up (Tested per JESD78), T_A = 125°C	-	±100	mA

2.2 Thermal Specifications

Parameter	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance	5-Pin SOT23 Package	θ_{JA}[1]	Junction to ambient	188	°C/W
		θ_{JC}[2]	Junction to case	137	°C/W
Thermal Resistance	5-Pin SC70 Package	θ_{JA}[1]	Junction to ambient	227	°C/W
		θ_{JC}[2]	Junction to case	141	°C/W
Thermal Resistance	8-Pin SOIC Package	θ_{JA}[1]	Junction to ambient	135	°C/W
		θ_{JC}[2]	Junction to case	75	°C/W
Thermal Resistance	8-Pin MSOP Package	θ_{JA}[1]	Junction to ambient	162	°C/W
		θ_{JC}[2]	Junction to case	86	°C/W
Thermal Resistance	8-Pin 2x2 DFN Package	θ_{JA}[3]	Junction to ambient	77	°C/W
		θ_{JC}[4]	Junction to case	17	°C/W
Thermal Resistance	14-Pin SOIC Package	θ_{JA}[1]	Junction to ambient	86	°C/W
		θ_{JC}[2]	Junction to case	50	°C/W
Thermal Resistance	14-Pin TSSOP Package	θ_{JA}[1]	Junction to ambient	115	°C/W
		θ_{JC}[2]	Junction to case	45	°C/W

1. θ_{JA} is measured with the component mounted on a high-effective thermal conductivity test board in free air. See TB379 for details.
2. For θ_{JC}, the case temperature location is taken at the package top center.
3. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.
4. For θ_{JC}, the case temperature is measured at the center of the exposed metal pad on the package underside.

2.3 Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Supply Voltage [(V+) – (V-)]	V_S	1.8	5.5	V
Input Voltage Range	V_I	(V-) – 0.1	(V+) + 0.1	V
Output Voltage range	V_O	V-	V+	V
Ambient Temperature	T_A	-40	125	°C

2.4 Electrical Specifications

V_S = (V+) – (V-) = 5V at T_A = 25°C, R_L = 10kΩ connected to V_S/2, V_{CM} = V_S/2 (unless otherwise noted)

Parameter	Symbol	Test Condition	Min[1]	Typ	Max[1]	Unit
DC Parameters						
Input Offset Voltage	V_{OS}	V_S = 5V, V_{CM} = 2.5V	-	±2	±10	µV
		T_A = -40°C to 125°C	-	-	±17	µV
Input Offset Voltage Temperature Coefficient	TCV_{OS}	T_A = -40°C to 125°C	-	0.02	0.075	µV/°C
Input Bias Current	I_B	T_A = -40°C to 125°C	-	±37	±600	pA
Input Offset Current	I_{OS}	T_A = -40°C to 125°C	-	±73	±400	pA
Common-Mode Input Range	V_{ICM}	V_S = 1.8V to 5.5V	(V_S-) - 0.1	-	(V_S+) + 0.1	V
Common-Mode Rejection Ratio	CMRR	V_S = 1.8V to 5.5V, T_A = -40°C to 125°C (V-) - 0.1V < VCM < (V+) + 0.1V	106	127	-	dB
Power Supply Rejection Ratio	PSRR	V_S = 1.8V to 5.5V, T_A = -40°C to 125°C	106	124	-	dB
Open-Loop Gain	A_{OL}	(V-) + 100mV < V_O < (V+) – 100mV, R_L = 10kΩ, T_A = -40°C to 125°C	106	143	-	dB
Output Voltage Swing from Rails	V_{OFR+}	R_L = 10kΩ, T_A = -40°C to 125°C	-	28	70	mV
	V_{OFR-}	R_L = 10kΩ, T_A = -40°C to 125°C	-	24	70	mV
Sourcing Short-Circuit Current	I_{SC+}	V_{OUT} connected to V-	-	19	30	mA
Sinking Short-Circuit Current	I_{SC-}	V_{OUT} connected to V+	-35	-14	-	mA
Supply Current per Amplifier	I_Q	R_L = ∞, T_A = -40°C to 125°C	-	22	35	µA
AC Parameters						
Input Noise Voltage	E_n	f = 0.01 to 1Hz	-	0.9	-	$µV_{pp}$
		f = 0.1 to 10Hz	-	1.1	-	$µV_{pp}$
Voltage Noise Density	e_n	f = 1kHz	-	43.5	-	nV/√Hz
Current Noise Density	i_n	f = 10Hz	-	76	-	fA/√Hz
Gain Bandwidth Product	GBW	G = 100, R_L = 10kΩ	-	340	-	kHz
Transient Response						
Positive Slew Rate	SR+	V_{OUT} = 1V to 4V, R_L = 10kΩ, G = 1	-	0.2	-	V/µs
Negative Slew Rate	SR-	V_{OUT} = 1V to 4V, R_L = 10kΩ, G = 1	-	0.2	-	V/µs
Settling Time to 0.1% V_O	t_S	V_S = ±2.5V, G =1, 2V-Step, C_L = 1.2pF	-	22.5	-	µs

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.

3. Typical Performance Graphs

V_S = 5V (±2.5V) at T_A = 25°C, RL = 10kΩ connected to V_S/2, V_{CM} = V_S/2 (unless otherwise noted)

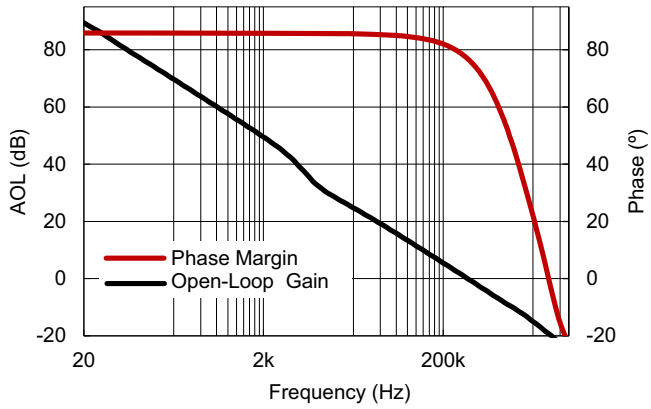


Figure 8. Open-Loop Gain and Phase vs Frequency

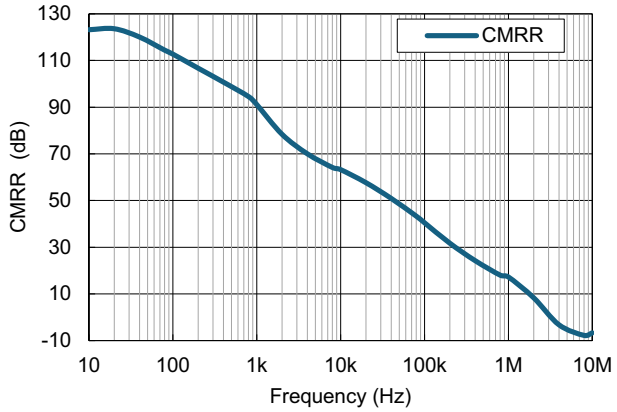


Figure 9. CMRR vs Frequency

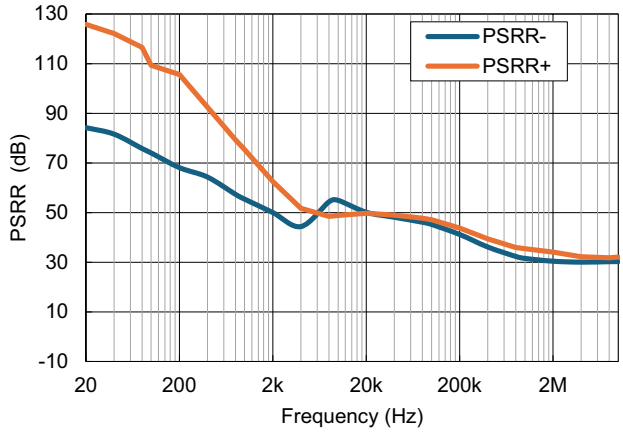


Figure 10. PSRR vs Frequency

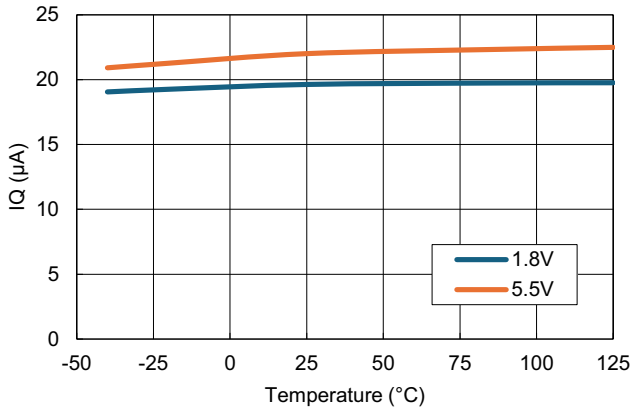


Figure 11. Quiescent Current vs Temperature

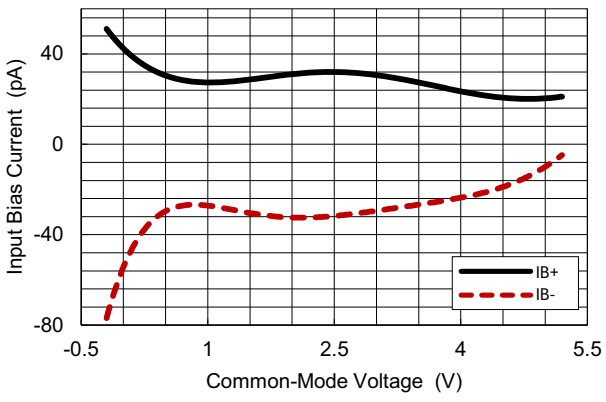


Figure 12. Input Bias Current vs Common-Mode Voltage

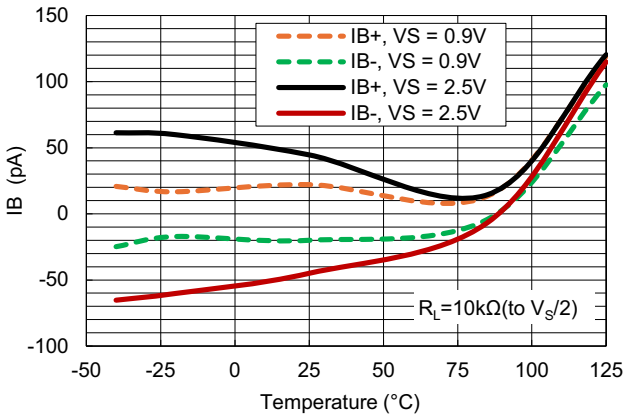


Figure 13. Input Bias Current vs Temperature

V_S = 5V (±2.5V) at T_A = 25°C, RL = 10kΩ connected to V_S/2, V_{CM} = V_S/2 (unless otherwise noted) (Cont.)

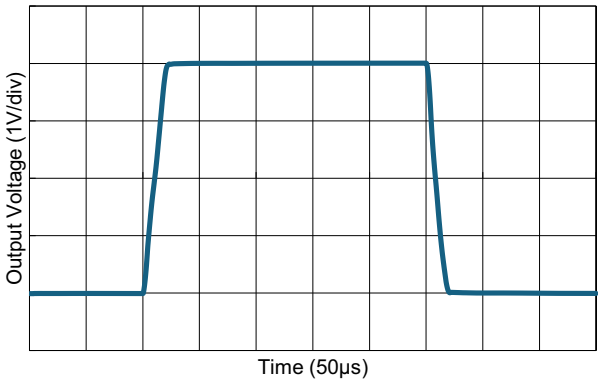


Figure 14. Large Signal Step Response

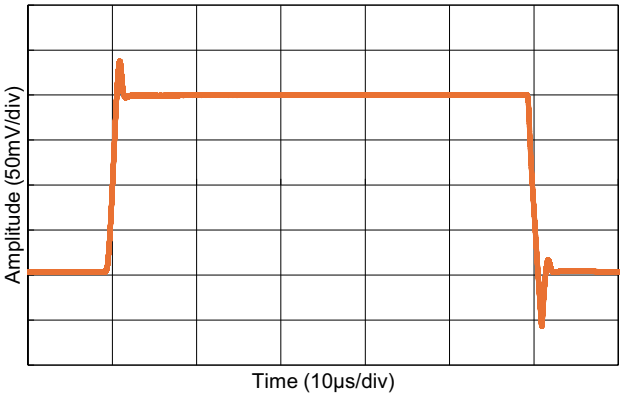


Figure 15. Small Signal Step Response

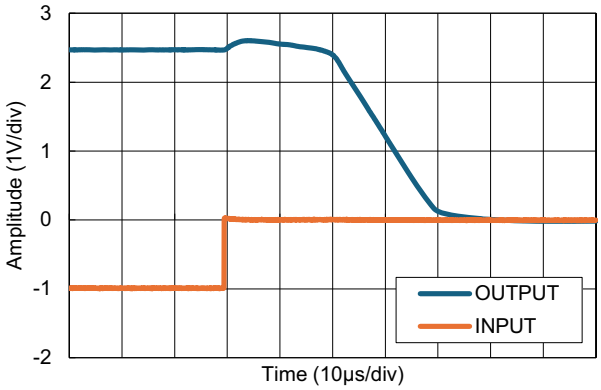


Figure 16. Positive Overvoltage Recovery

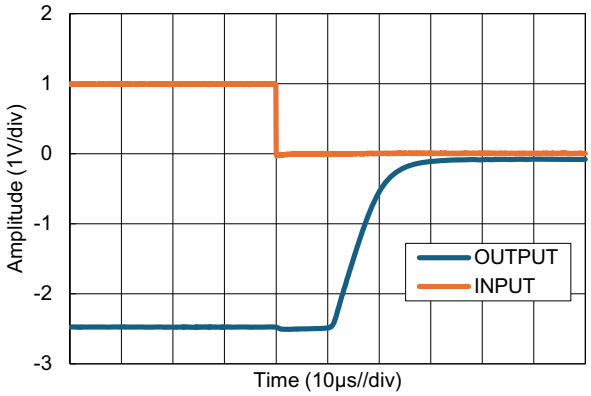


Figure 17. Negative Overvoltage Recovery

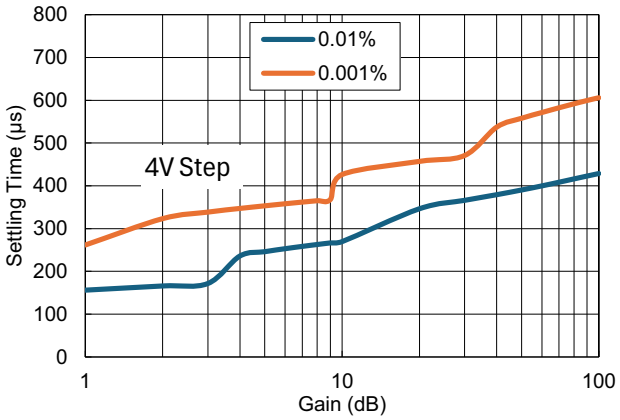


Figure 18. Settling Time vs Closed-Loop Gain

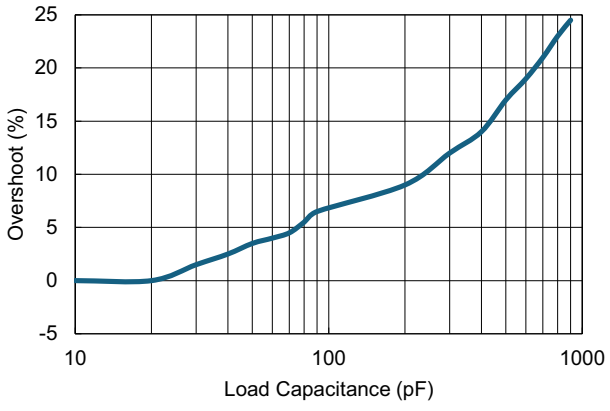


Figure 19. Small Signal Overshoot vs Load Capacitance

V_S = 5V (±2.5V) at T_A = 25°C, RL = 10kΩ connected to V_S/2, V_{CM} = V_S/2 (unless otherwise noted) (Cont.)

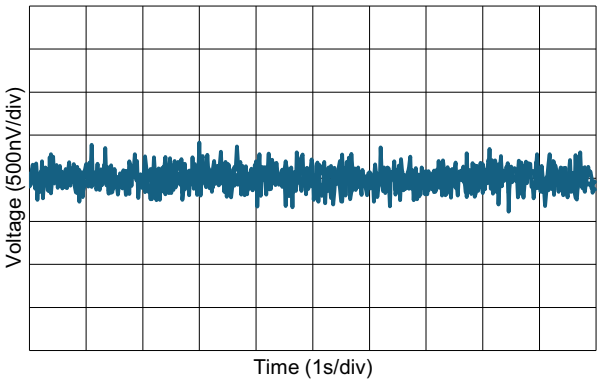


Figure 20. 0.1Hz to 10Hz Noise

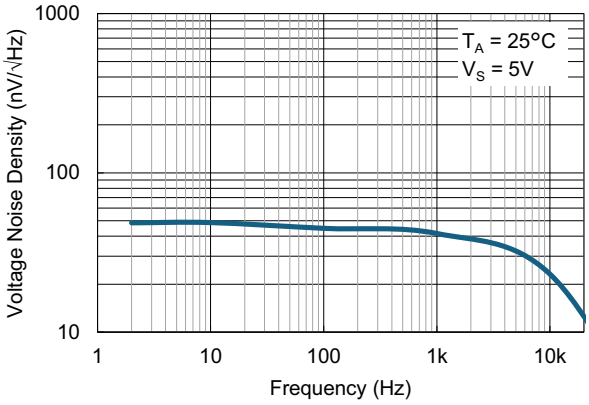


Figure 21. Voltage Noise Spectral Density

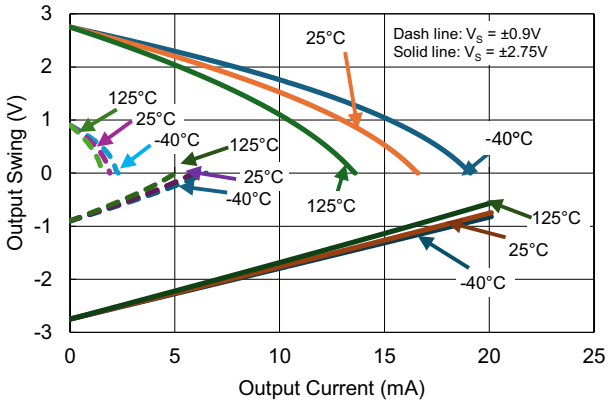


Figure 22. Output Voltage Swing vs Output Current

4. Detailed Description

4.1 Overview

The ISL28x33A family of auto-zero operational amplifiers (op amps) are low-power devices with rail-to-rail input and outputs. These op amps operate from supply voltages as low as 1.8V up to 5.5V. The devices are unity-gain stable and designed for a wide range of precision and general-purpose applications.

Their input common-mode voltage range extends 100mV above and below the power supply voltage rails, allowing these op amps to be used in virtually any single-supply application. The rail-to-rail input and output swing capability increases the signal dynamic range and therefore, signal-to-noise ratio, a performance feature highly necessary in low-supply applications. The combination of low-offset voltage and low drift over temperature and time makes these devices ideal for the use in high-gain amplifiers and precision sensor signal conditioners.

4.2 Functional Block Diagram

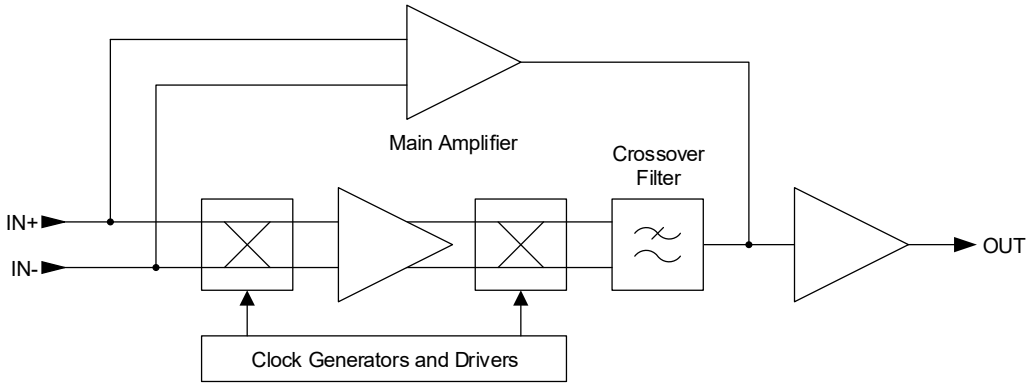


Figure 23. Block Diagram of a Single Amplifier Stage

4.3 Feature Description

4.3.1 Low Offset and Drift

The ISL28x33A devices use a proprietary chopper-stabilized technique that combines a 340kHz main amplifier with a high open-loop gain chopper amplifier to achieve low offset voltage and drift, while consuming only 22µA of supply current per channel.

This multi-path amplifier architecture contains a time continuous main amplifier whose DC offset input is corrected by a parallel connected, high gain chopper stabilized DC correction amplifier operating at 100kHz. From DC to about 5kHz, both amplifiers are active with DC offset correction and most of the low frequency gain is provided by the chopper amplifier. A 5kHz crossover filter cuts off the low frequency amplifier path, leaving the main amplifier active out to the 340kHz gain-bandwidth product of the device.

The key benefits of this architecture for precision applications are very high open-loop gain, very low DC offset, and low 1/f noise. The noise is virtually flat across the frequency range from a few millihertz out to 100kHz, except for the narrow noise peak at the amplifier crossover frequency.

4.3.2 Rail-To-Rail Input and Output (RRIO)

The RRIO CMOS amplifier uses parallel input PMOS and NMOS that enable the inputs to swing 100mV beyond either supply rail. The inverting and non-inverting inputs do not have back-to-back input clamp diodes and can maintain high input impedance at high differential input voltages. This is effective in eliminating output distortion caused by high slew-rate input signals.

The output stage uses common source connected PMOS and NMOS devices to achieve rail-to-rail output drive capability with 17mA current limit and the capability to swing to within 70mV of either rail while driving a 10kΩ load.

4.3.3 Layout Guidelines for High Impedance Inputs

To achieve the maximum performance of the high input impedance and low offset voltage of the ISL28x33A amplifiers, care should be taken in the circuit board layout. The surface of the printed circuit board must remain clean and free of moisture to avoid leakage-currents between adjacent traces. Surface coating of the circuit board reduces surface moisture and provides a humidity barrier, reducing parasitic resistance on the board.

4.3.4 Input and Output ESD Protection

ISL28x33A incorporates internal ESD protection circuits on all pins. For the input and output pins, this protection primarily consists of current-steering diodes that are connected between the input and output pins and the power-supply pins. If the input voltage is expected to exceed the specified value in the Absolute Maximum Ratings, insert a series resistor (R_S) to limit the input current to about 20mA (Figure 24).

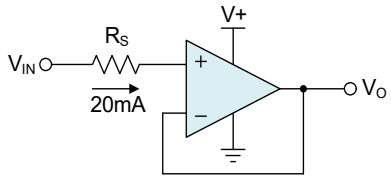


Figure 24. Input Current Protection

5. Application Information

The ISL28x33A family features 340kHz gain-bandwidth and 0.2V/µs slew rate with only 22µA of supply current per channel. Its low input offset of 2µV enables the design of DC-coupled high-gain amplifiers. However, care must be applied when designing for maximum dynamic output range to prevent signal distortions due to the low slew rate. Also, PCB layout considerations are different to that of a standard op amp.

5.1 Typical Applications

5.1.1 High Gain, Precision DC-Coupled Amplifier

The circuit in Figure 25 implements a single-stage DC-coupled amplifier with an input DC sensitivity of under 100nV that is only possible using a low V_{OS} amplifier with high open-loop gain. High gain DC amplifiers operating from low voltage supplies are not practical using typical low offset precision op amps. For example, a typical precision amplifier in a gain of 10kV/V with a ±100µV V_{OS} and an offset drift of 0.5µV/°C of a low offset op amp would produce a DC error of >1V with an additional 5mV/°C of temperature dependent error, making it difficult to resolve DC input voltage changes in the mV range.

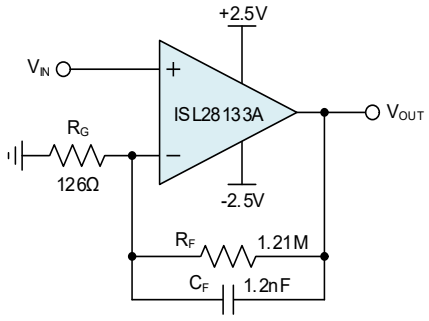


Figure 25. High-Gain, Precision DC-Coupled Amplifier with ISL28133A

The ±10µV max V_{OS} and 0.075µV/°C maximum temperature drift of the ISL28x33A produces a temperature stable maximum DC output error of only ±100mV with a maximum output temperature drift of 0.75mV/°C. The

additional benefit of a low 1/f noise corner frequency and some feedback filtering enables DC voltages and voltage fluctuations well below 100nV to be easily detected with a simple single stage amplifier.

5.1.2 Design Procedure

The following are design requirements for this design:

- Input voltage and frequency range: V_{IN} = 0 to 500µV_{P-P}, f_{IN} = 0 to 10Hz
- Required Signal output range: V_O = 0 to 4.8V_{P-P}
- Low-pass filter cut-off frequency: f_C = 100Hz

The signal gain of the amplifier is:

(EQ. 1) $$G = \frac{V_O}{V_{IN}} = \frac{4.8V_{P-P}}{500\mu V_{P-P}} = 9600V/V \text{ or } 96.65dB$$

This gain is defined by the feedback and gain resistors, R_F and R_G, with G = 1+ R_F/R_G. Solving for the resistor ratio gives:

(EQ. 2) $$R_F/R_G = G - 1 = 9599$$

Making R_F = 1.21MΩ and R_G = 126Ω yields a gain of 9604 and therefore, a gain error of 0.04%.
The cut-off frequency of the low-pass filter is defined by $f_C = 1/(2\pi \times C_F \times R_F)$. Solving for C_F gives:

(EQ. 3) $$C_F = \frac{1}{2\pi \times f_C \times R_F} = \frac{1}{2\pi \times 100Hz \times 1.21M\Omega} = 13.15nF$$

Selecting the closest standard value makes C_F = 12nF, resulting in a cut-off frequency of f_C = 109Hz.

Figure 26 shows the gain response of the high-gain amplifier using ISL28133A in comparison with the gain response of an ideal op amp. *Note*: The output impedance of low-power CMOS op amps increases significantly at high frequencies. This causes the gain response to divert from theoretical response, which assumes an op amp output impedance of Z_O = 0Ω.

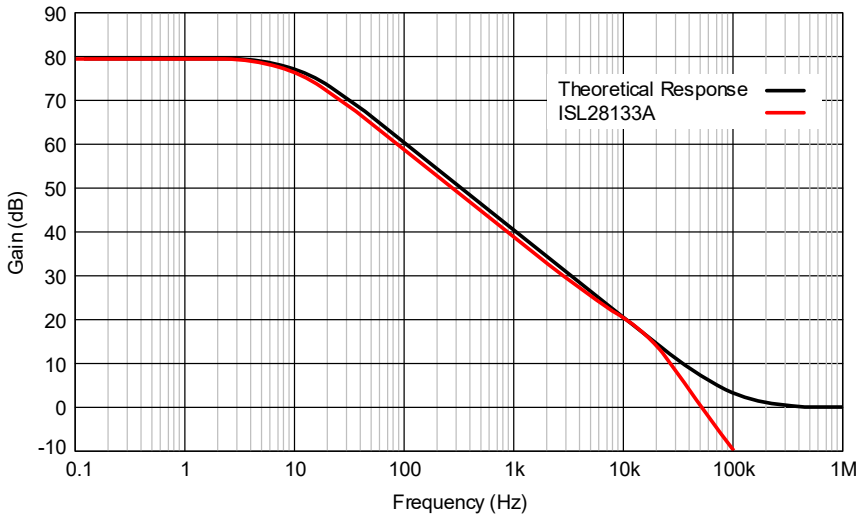


Figure 26. High-Gain Amplifier Frequency Response

5.2 Layout Considerations

When using the highest-precision amplifier available, the overall accuracy of your application might still fall short of expectations. Specifically, employing an auto-zero amplifier often shifts the precision limitation from the amplifier itself to the design and layout of the printed circuit board (PCB).

One significant contributor to offset voltage errors on a PCB is thermoelectric voltage, commonly referred to as thermocouple or Seebeck voltage. This voltage is generated at the junction between two dissimilar metals and is directly proportional to the junction temperature. The magnitude of Seebeck voltage varies considerably depending on the specific metals involved, typically ranging from microvolts up to millivolts. Additionally, temperature-induced variations in these voltages can span from several microvolts to tens of microvolts per degree Celsius.

Typical metallic junctions found on PCBs include solder-to-trace interfaces and solder-to-component lead connections. If a temperature gradient exists across the PCB, resulting in different temperatures at each end of a component, the resulting Seebeck voltages differs, thereby producing a thermal voltage error. Figure 27 illustrates this scenario.

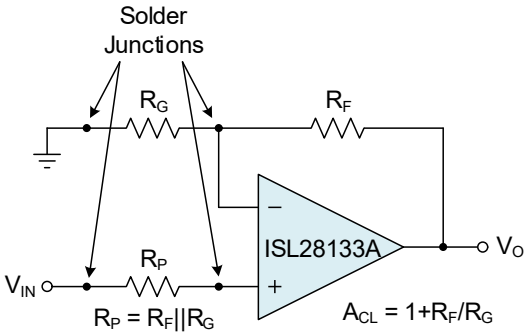


Figure 27. Using Dummy Resistor minimizes Offset Errors due to Seebeck Voltages and Bias Currents

In a high-gain configuration, where feedback resistor (R_F) is significantly larger than gain resistor (R_G), any difference in Seebeck voltages appearing across R_G manifests as an offset voltage directly at the amplifier's inverting input. This initial offset voltage is subsequently amplified by the closed-loop gain, therefore causing a substantially larger output voltage error.

Thermocouple errors can be mitigated by using a dummy component to match the thermoelectric error source. For instance, adding a resistor (R_P) in series with the non-inverting input does not impact the amplifier's AC performance but, when placed physically close to R_G, ensures that their Seebeck potentials are closely matched, thereby minimizing thermocouple-induced errors. Matching R_P to the parallel combination of R_G and R_F further reduces offset errors caused by input bias currents.

The Seebeck voltage difference across the feedback resistor (R_F) is less critical because this error appears directly at the output and is not amplified by the closed-loop gain.

Another effective approach for reducing offset errors due to Seebeck voltages is maintaining a uniform ambient temperature across the PCB. Implementing a ground plane helps distribute heat evenly throughout the PCB and provides additional benefits, such as reducing susceptibility to electromagnetic interference (EMI).

The PCB surface should be clean and moisture-free to prevent leakage currents between adjacent traces. Applying a surface coating creates a humidity barrier, reducing surface moisture and thereby minimizing parasitic resistance on the board.

Further reduction of leakage currents can be achieved by using guard rings around the amplifier inputs. While the guard rings do not require a specific width, each guard ring should form a continuous loop around the inverting and non-inverting inputs of the amplifier. By setting the guard ring voltage equal to the voltage at the non-inverting input, both parasitic resistance and capacitance are effectively reduced.

Figure 28 provides an example of such a layout employing the surface-mount dual amplifier ISL28233A.

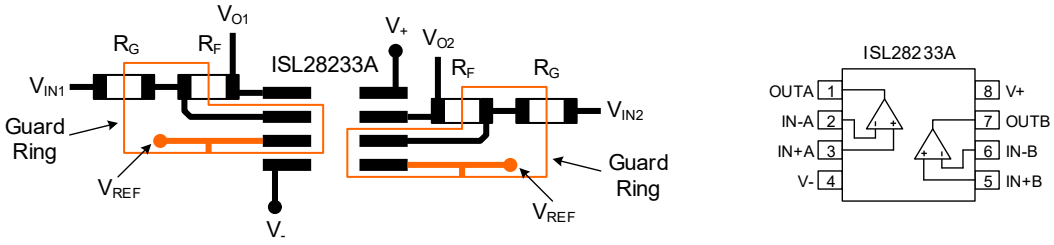


Figure 28. Using Guard Rings minimizes Leakage Current

6. Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

7. Ordering Information

Part Number[1]	# Channels	Part Marking	Package Description[2] (RoHS Compliant)	Pkg. Dwg. #	Carrier Type[3]	MSL Rating[4]	Temp. Range
ISL28133AFEZ-T7	1	133[5]	5-Pin SC70	P5.049	Reel, 3k Units	1	-40 to 125°C
ISL28133AFHZ-T7	1	133A[5]	5-Pin SOT23	P5.064	Reel, 3k Units	1	-40 to 125°C
ISL28233AFUZ-T	2	233AU	8-Pin MSOP	M8.118D	Reel, 2.5k Units	1	-40 to 125°C
ISL28233AFBZ-T	2	28233 AFBZ	8-Pin SOICN	M8.15	Reel, 2.5k Units	3	-40 to 125°C
ISL28233AFRZ-T7	2	33A	8-Pin DFN	L8.2x2F	Reel, 1k Units	1	-40 to 125°C
ISL28433AFBZ-T	4	28433 AFBZ	14-Pin SOICN	M14.15	Reel, 2.5k Units	3	-40 to 125°C
ISL28433AFVZ-T	4	28433 AFVZ	14-Pin TSSOP	M14.173	Reel, 2.5k Units	1	-40 to 125°C

1. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. For the Pb-Free Reflow Profile, see TB493.
3. See TB347 for details about reel specifications.
4. Moisture Sensitivity Level (MSL) tested per JEDEC J-STD-020. For more information about MSL, see TB363.
5. The part marking is located on the bottom of the part.

8. Revision History

Revision	Date	Description
1.02	Jan 15, 2026	Added ISL28233A and ISL28433A product information throughout.
1.01	Sep 10, 2025	Updated PODs to the latest format. Added ECAD Information.
1.00	Jul 8, 2025	Initial release.

A. ECAD Design Information

This information supports the development of the PCB ECAD model for this device. It is intended to be used by PCB designers.

A.1 Part Number Indexing

Orderable Part Number	Number of Pins	Package Type	Package Code/POD Number
ISL28133AFEZ-T7	5	SC70	P5.049
ISL28133AFHZ-T7	5	SOT23	P5.064
ISL28233AFUZ-T	8	MSOP	M8.118D
ISL28233AFBZ-T	8	SOIC	M8.15
ISL28233AFRZ-T7	8	DFN	L8.2x2F
ISL28433AFBZ-T	14	SOIC	M14.15
ISL28433AFVZ-T	14	TSSOP	M14.173

A.2 Symbol Pin Information

A.2.1 5-SC70

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
1	IN+	Input	-
2	V-	Power	-
3	IN-	Input	-
4	OUT	Output	-
5	V+	Power	-

A.2.2 5-SOT23

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
1	OUT	Output	-
2	V-	Power	-
3	IN+	Input	-
4	IN-	Input	-
5	V+	Power	-

A.2.3 8-MSOP

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
1	OUT1	Ouput	-
2	IN1-	Input	-
3	IN1+	Input	-
4	V-	Power	-
5	IN2+	Input	-
6	IN2-	Input	-
7	OUT2	Ouput	-
8	V+	Power	-

A.2.4 8-SOIC

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
1	OUT1	Ouput	-
2	IN1-	Input	-
3	IN1+	Input	-
4	V-	Power	-
5	IN2+	Input	-
6	IN2-	Input	-
7	OUT2	Ouput	-
8	V+	Power	-

A.2.5 8-DFN

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
1	OUT1	Ouput	-
2	IN1-	Input	-
3	IN1+	Input	-
4	V-	Power	-
5	IN2+	Input	-
6	IN2-	Input	-
7	OUT2	Ouput	-
8	V+	Power	-
EPAD9	V-	Power	

A.2.6 14-SOIC/TSSOP

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
1	OUT1	Output	-
2	IN1-	Input	-
3	IN1+	Input	-
4	V+	Power	-
5	IN2+	Input	-
6	IN2-	Input	-
7	OUT2	Output	-
8	OUT3	Output	-
9	IN3-	Input	-
10	IN3+	Input	-
11	V-	Power	-
12	IN4+	Input	-
13	IN4-	Input	-
14	OUT4	Output	-

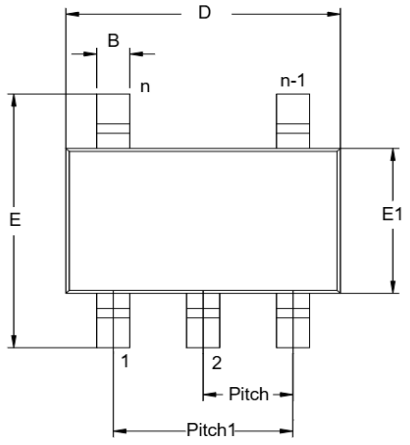
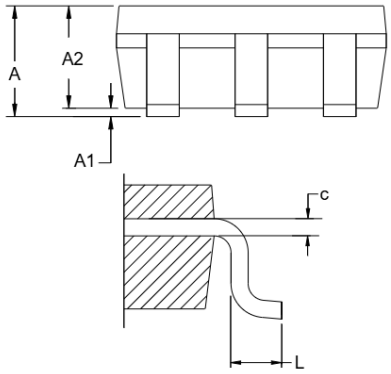
A.3 Symbol Parameters

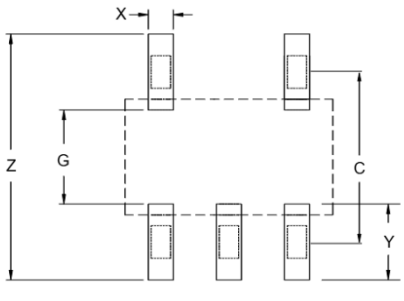
Orderable Part Number	Qualification	Mounting Type	RoHS	Min Operating Temperature	Max Operating Temperature	Min Supply Voltage	Max Supply Voltage	Number of Channels	Supply Current	Max Input Offset Voltage
ISL28133AFEZ-T7	Commercial	SMD	Compliant	-40 °C	+125 °C	1.8 V	5.5 V	1	22 µA	±10 µV
ISL28133AFHZ-T7	Commercial	SMD	Compliant	-40 °C	+125 °C	1.8 V	5.5 V	1	22 µA	±10 µV
ISL28233AFUZ-T	Commercial	SMD	Compliant	-40 °C	+125 °C	1.8 V	5.5 V	2	22 µA	±10 µV
ISL28233AFBZ-T	Commercial	SMD	Compliant	-40 °C	+125 °C	1.8 V	5.5 V	2	22 µA	±10 µV
ISL28233AFRZ-T7	Commercial	SMD	Compliant	-40 °C	+125 °C	1.8 V	5.5 V	2	22 µA	±10 µV
ISL28433AFBZ-T	Commercial	SMD	Compliant	-40 °C	+125 °C	1.8 V	5.5 V	4	22 µA	±10 µV
ISL28433AFVZ-T	Commercial	SMD	Compliant	-40 °C	+125 °C	1.8 V	5.5 V	4	22 µA	±10 µV

A.4 Footprint Design Information

A.4.1 5-SC70

IPC Footprint Type	Package Code/ POD Number	Number of Pins
SC70	P5.049/KA0005AA	5

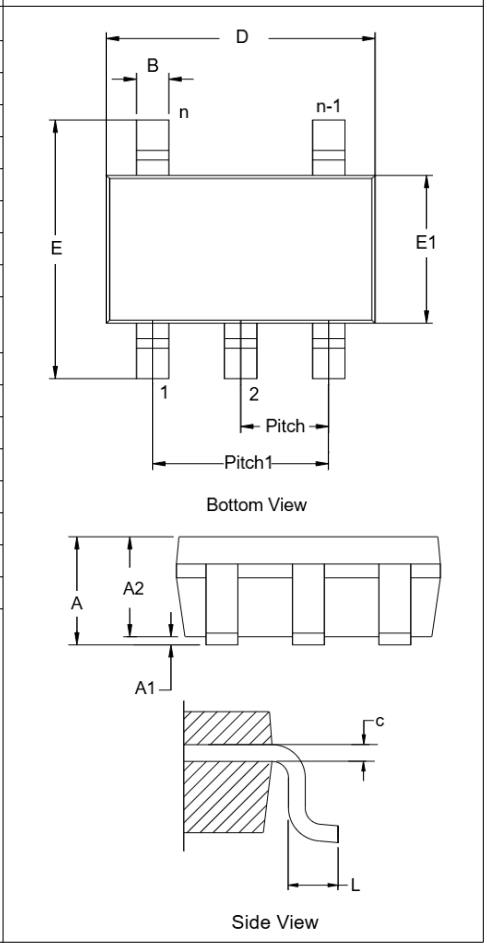
Description	Dimension	Value (mm)	Reference Diagram[1]
Minimum body span (vertical side)	Dmin	1.85	 Bottom View
Maximum body span (vertical side)	Dmax	2.15	
Minimum lead span (horizontal side)	Emin	1.80	
Maximum lead span (horizontal side)	Emax	2.40	
Minimum lead width	Bmin	0.15	
Maximum lead width	Bmax	0.30	
Minimum body width (horizontal side)	E1min	1.15	
Maximum body width (horizontal side)	E1max	1.35	
Number of leads: 3, 4, 5 or 6	PinCount	5	
Comma separated list showing pin sequence (Na,Nb,...). Example: 1,2,3 or 1,2,3,4,5,6 or 5,4,1,3,2	PinOrder	1,2,3,4,5	
Distance between the center of any two adjacent pins	Pitch	0.65	
Overall pitch (e1)	Pitch1	1.30	
Maximum Height	Amax	1.10	
Minimum standoff height	A1min	0.00	
Maximum body height	A2max	1.00	
Minimum Lead Thickness	cmin	0.08	
Maximum Lead Thickness	cmax	0.22	
Minimum Lead Length	Lmin	0.26	
Maximum Lead Length	Lmax	0.46	 Side View

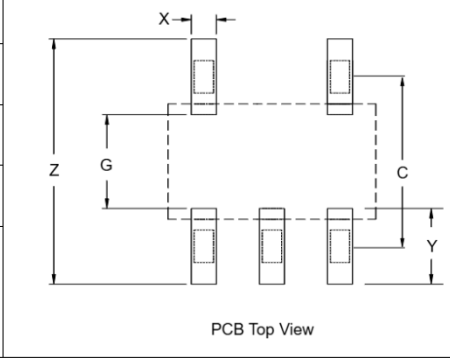
Recommended Land Pattern			
Description	**Dimension**	**Value (mm)**	**Reference Diagram[1]**
Distance between pads. Measured from outside edges	Z	2.85	 PCB Top View
Distance between pads. Measured from inside edges	G	1.35	
Pad width	X	0.40	
Pad length	Y	0.75	
Row spacing. Distance between pad centers	C	2.10	

1. The diagrams show table attribute referencing. For the exact diagrams, see the package outline drawing.

A.4.2 5-SOT23

IPC Footprint Type	Package Code/ POD Number	Number of Pins
SOT23	P5.064/KA0005AB	5

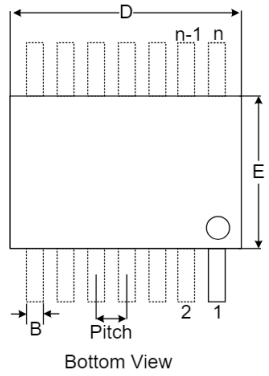
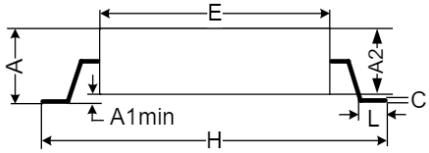
Description	Dimension	Value (mm)	Reference Diagram[1]
Minimum body span (vertical side)	Dmin	2.80	
Maximum body span (vertical side)	Dmax	3.00	
Minimum lead span (horizontal side)	Emin	2.60	
Maximum lead span (horizontal side)	Emax	3.00	
Minimum lead width	Bmin	0.30	
Maximum lead width	Bmax	0.50	
Minimum body width (horizontal side)	E1min	1.50	
Maximum body width (horizontal side)	E1max	1.70	
Number of leads: 3, 4, 5 or 6	PinCount	5	
Comma separated list showing pin sequence (Na,Nb,...). Example: 1,2,3 or 1,2,3,4,5,6 or 5,4,1,3,2	PinOrder	1,2,3,4,5	
Distance between the center of any two adjacent pins	Pitch	0.95	
Overall pitch (e1)	Pitch1	1.90	
Maximum Height	Amax	1.45	
Minimum standoff height	A1min	0.00	
Maximum body height	A2max	1.30	
Minimum Lead Thickness	cmin	0.08	
Maximum Lead Thickness	cmax	022	
Minimum Lead Length	Lmin	0.35	
Maximum Lead Length	Lmax	0.55	

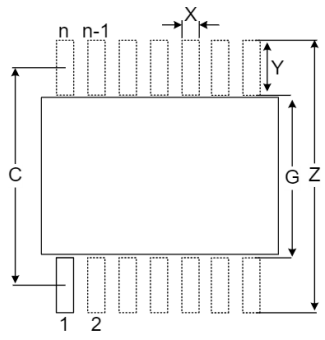
Recommended Land Pattern			
Description	**Dimension**	**Value (mm)**	**Reference Diagram[1]**
Distance between pads. Measured from outside edges	Z	3.60	
Distance between pads. Measured from inside edges	G	1.20	
Pad width	X	0.60	
Pad length	Y	1.20	
Row spacing. Distance between pad centers	C	2.40	

1. The diagrams show table attribute referencing. For the exact diagrams, see the package outline drawing.

A.4.3 8-MSOP

IPC Footprint Type	Package Code/ POD Number	Number of Pins
SOP	M8.118D/HV0008AC	8

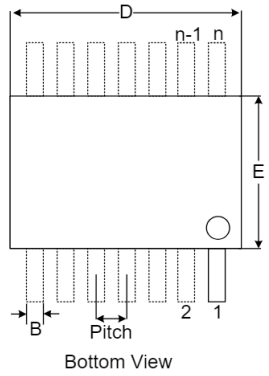
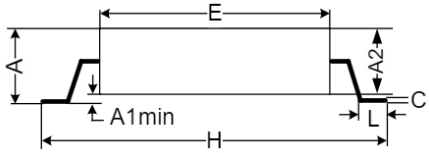
Description	Dimension	Value (mm)	Reference Diagram[1]
Minimum lead span (horizontal side)	Hmin	4.70	 Bottom View
Maximum lead span (horizontal side)	Hmax	5.10	
Minimum body span (horizontal side)	Dmin	2.90	
Maximum body span (horizontal side)	Dmax	3.10	
Minimum body span (vertical side)	Emin	2.90	
Maximum body span (vertical side)	Emax	3.10	
Minimum Lead Width	Bmin	0.22	
Maximum Lead Width	Bmax	0.40	
Minimum Lead Length	Lmin	0.40	 Side View
Maximum Lead Length	Lmax	0.80	
Maximum Height	Amax	1.10	
Minimum Standoff Height	A1min	0.00	
Minimum Lead Thickness	cmin	0.08	
Maximum Lead Thickness	cmax	0.23	
Total number of pin positions (including absent pins)	PinCount	8	
Distance between the center of any two adjacent pins	Pitch	0.65	

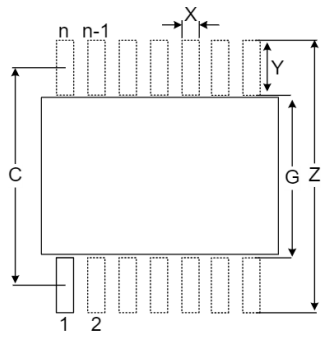
Recommended Land Pattern			
Description	**Dimension**	**Value (mm)**	**Reference Diagram[1]**
Distance between left pad toe to right pad toe.	Z	5.50	 PCB Top View
Distance between left pad heel to right pad heel.	G	3.10	
Row spacing. Distance between pad centers	C	4.30	
Pad Width	X	0.32	
Pad Length	Y	1.20	

1. The diagrams show table attribute referencing. For the exact diagrams, see the package outline drawing.

A.4.4 8-SOICN

IPC Footprint Type	Package Code/ POD Number	Number of Pins
SOIC	M8.15/GS0008AC	8

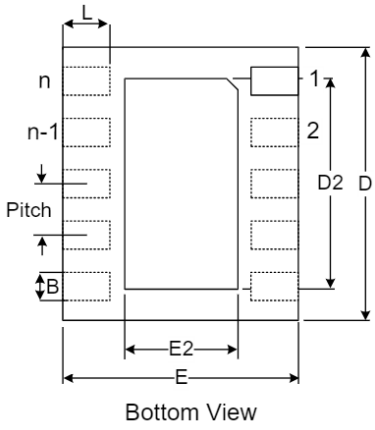
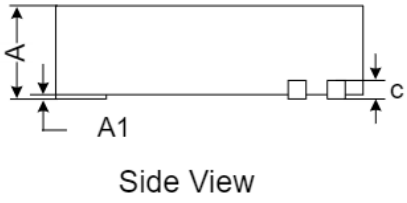
Description	Dimension	Value (mm)	Reference Diagram[1]
Minimum lead span (horizontal side)	Hmin	5.80	 Bottom View
Maximum lead span (horizontal side)	Hmax	6.20	
Minimum body span (horizontal side)	Dmin	4.80	
Maximum body span (horizontal side)	Dmax	5.00	
Minimum body span (vertical side)	Emin	3.80	
Maximum body span (vertical side)	Emax	4.00	
Minimum Lead Width	Bmin	0.33	
Maximum Lead Width	Bmax	0.51	
Minimum Lead Length	Lmin	0.40	 Side View
Maximum Lead Length	Lmax	1.27	
Maximum Height	Amax	1.75	
Minimum Standoff Height	A1min	0.10	
Minimum Lead Thickness	cmin	0.19	
Maximum Lead Thickness	cmax	0.25	
Total number of pin positions (including absent pins)	PinCount	8	
Distance between the center of any two adjacent pins	Pitch	1.27	

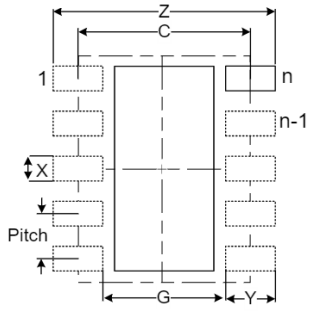
Recommended Land Pattern			
Description	**Dimension**	**Value (mm)**	**Reference Diagram[1]**
Distance between left pad toe to right pad toe.	Z	7.40	 PCB Top View
Distance between left pad heel to right pad heel.	G	3.00	
Row spacing. Distance between pad centers	C	5.20	
Pad Width	X	0.60	
Pad Length	Y	2.20	

1. The diagrams show table attribute referencing. For the exact diagrams, see the package outline drawing.

A.4.5 8-DFN

IPC Footprint Type	Package Code/ POD Number	Number of Pins
DFN	L8.2x2F/DW0008AA	8

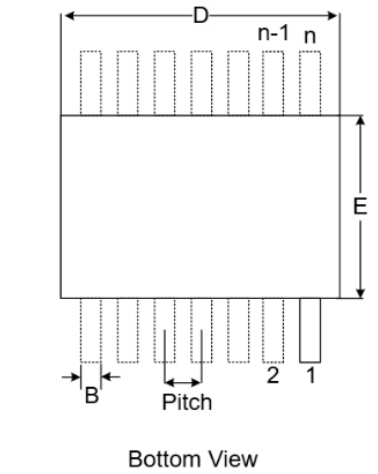
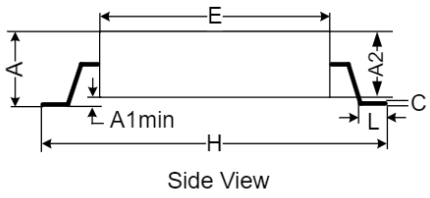
Description	Dimension	Value (mm)	Reference Diagram[1]
Minimum body span (vertical side)	Dmin	1.90	
Maximum body span (vertical side)	Dmax	2.10	
Minimum body span (horizontal side)	Emin	1.90	
Maximum body span (horizontal side)	Emax	2.10	
Minimum Lead Width	Bmin	0.20	
Maximum Lead Width	Bmax	0.30	
Minimum Lead Length	Lmin	0.25	
Maximum Lead Length	Lmax	0.35	
Maximum Height	Amax	0.80	
Minimum Standoff Height	A1min	0.00	
Minimum Lead Thickness	cmin	0.15	
Maximum Lead Thickness	cmax	0.25	
Number of pins	PinCount	8	
Distance between the center of any two adjacent pins	Pitch	0.50	
Minimum thermal pad size (vertical side)	D2min	1.50	
Maximum thermal pad size (vertical side)	D2max	1.70	
Minimum thermal pad size (horizontal side)	E2min	0.80	
Maximum thermal pad size (horizontal side)	E2max	1.00	

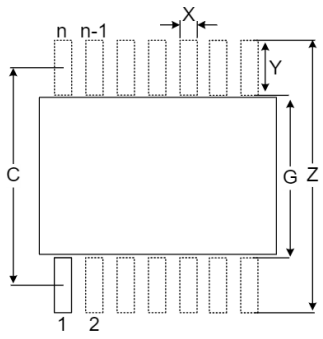
Recommended Land Pattern			
Description	**Dimension**	**Value (mm)**	**Reference Diagram[1]**
Row spacing. Distance between pad centres	C	1.85	
Distance between pads. Measured from outside edges	Z	2.30	
Distance between pads. Measured from inside edges	G	1.40	
Pad Width	X	0.25	
Pad Length	Y	0.45	

1. The diagrams show table attribute referencing. For the exact diagrams, see the package outline drawing.

A.4.6 14-SOICN

IPC Footprint Type	Package Code/ POD Number	Number of Pins
SOIC	M14.15/GS0014AB	14

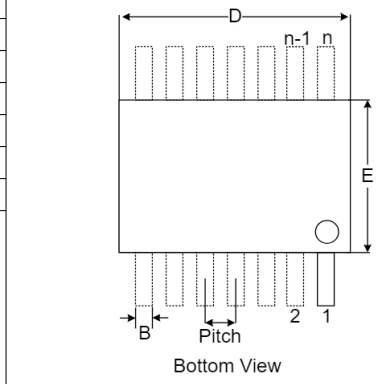
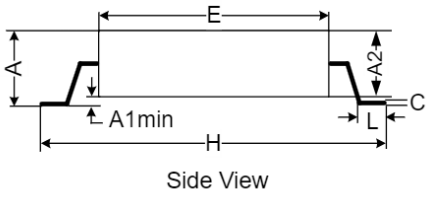
Description	Dimension	Value (mm)	Reference Diagram[1]
Minimum lead span (horizontal side)	Hmin	5.95	
Maximum lead span (horizontal side)	Hmax	6.05	
Minimum body span (pin1 side)	Dmin	8.55	
Maximum body span (pin1 side)	Dmax	8.75	
Minimum body span	Emin	3.80	
Maximum body span	Emax	4.00	
Minimum Lead Width	Bmin	0.31	
Maximum Lead Width	Bmax	0.51	
Minimum Lead Length	Lmin	0.40	
Maximum Lead Length	Lmax	1.27	
Maximum Height	Amax	1.75	
Minimum Standoff Height	A1min	0.10	
Minimum Lead Thickness	cmin	0.19	
Maximum Lead Thickness	cmax	0.25	
Total number of pin positions (including absent pins)	PinCount	14	
Distance between the center of any two adjacent pins	Pitch	1.27	

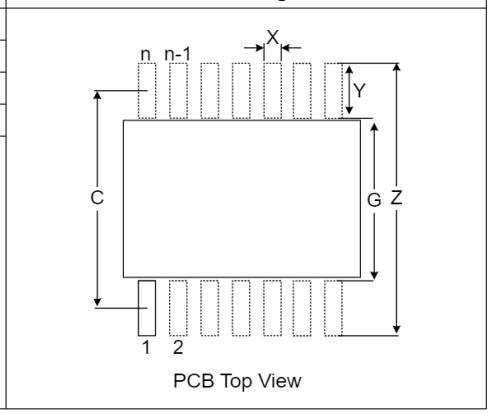
Recommended Land Pattern			
Description	**Dimension**	**Value (mm)**	**Reference Diagram[1]**
Distance between left pad toe to right pad toe.	Z	6.60	
Distance between left pad heel to right pad heel.	G	4.20	
Row spacing. Distance between pad centers	C	5.40	
Pad Width	X	0.41	
Pad Length	Y	1.20	

1. The diagrams show table attribute referencing. For the exact diagrams, see the package outline drawing.

A.4.7 14-TSSOP

IPC Footprint Type	Package Code/ POD Number	Number of Pins
SOP	M14.173/HV0014AA	14

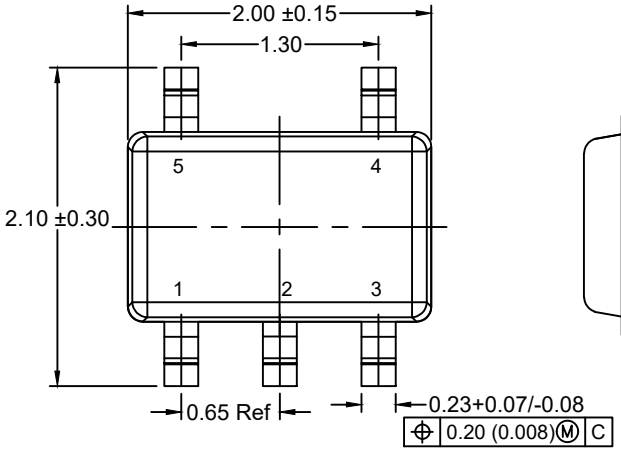
Description	Dimension	Value (mm)	Reference Diagram[1]
Minimum lead span (horizontal side)	Hmin	6.30	
Maximum lead span (horizontal side)	Hmax	6.50	
Minimum body span (horizontal side)	Dmin	4.90	
Maximum body span (horizontal side)	Dmax	5.10	
Minimum body span (vertical side)	Emin	4.30	
Maximum body span (vertical side)	Emax	4.50	
Minimum Lead Width	Bmin	0.20	
Maximum Lead Width	Bmax	0.30	
Minimum Lead Length	Lmin	0.45	
Maximum Lead Length	Lmax	0.75	
Maximum Height	Amax	1.20	
Minimum Standoff Height	A1min	0.05	
Minimum Lead Thickness	cmin	0.09	
Maximum Lead Thickness	cmax	0.20	
Total number of pin positions (including absent pins)	PinCount	14	
Distance between the center of any two adjacent pins	Pitch	0.65	

Recommended Land Pattern			
Description	**Dimension**	**Value (mm)**	**Reference Diagram[1]**
Distance between left pad toe to right pad toe.	Z	7.0	
Distance between left pad heel to right pad heel.	G	4.60	
Row spacing. Distance between pad centers	C	5.80	
Pad Width	X	0.25	
Pad Length	Y	1.20	

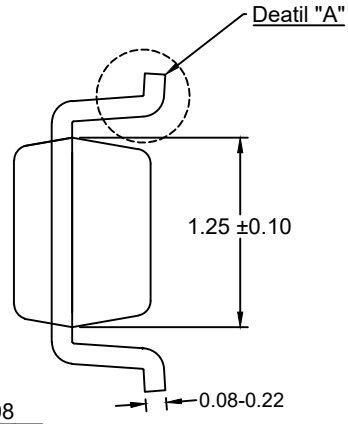
1. The diagrams show table attribute referencing. For the exact diagrams, see the package outline drawing.

Package Outline Drawing

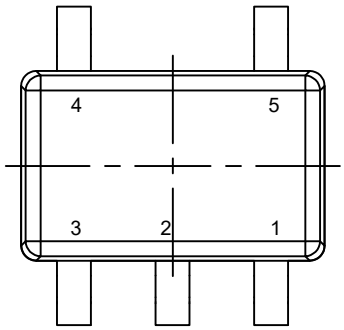
P5.049
KA0005AA
5-SC70 2.0 x 1.25 x 0.95 mm Body, 0.65mm Pitch Lead Small Outlibe Transistor Plastic Package
Rev04, Jul 16, 2025



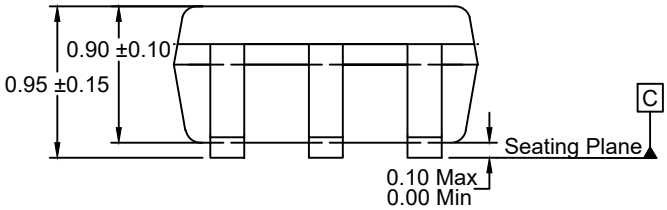
Top View



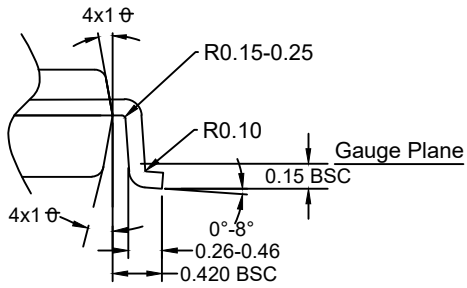
Side View



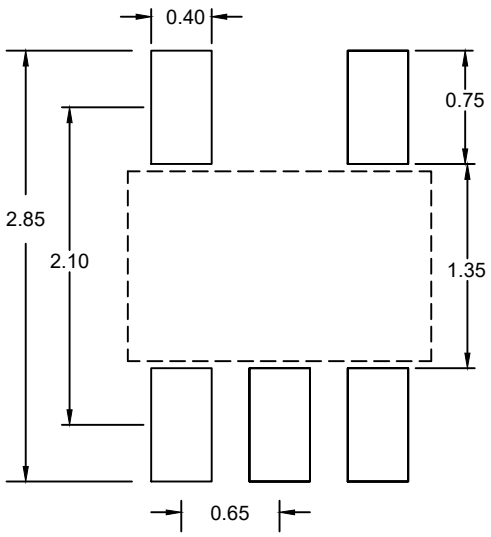
Bottom View



Side View



Detail"A"

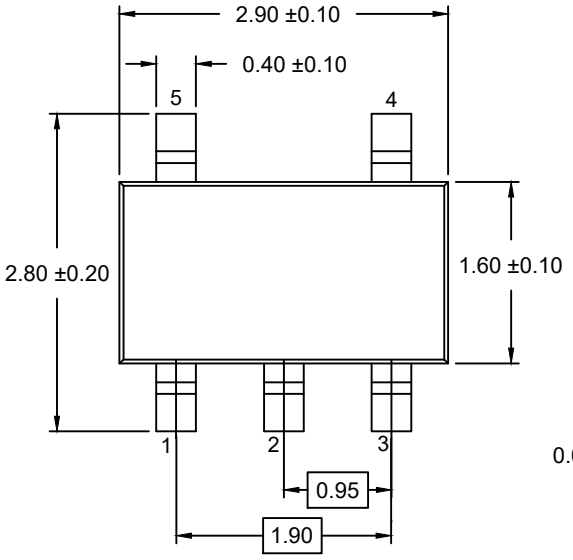


Recommended Land Pattern

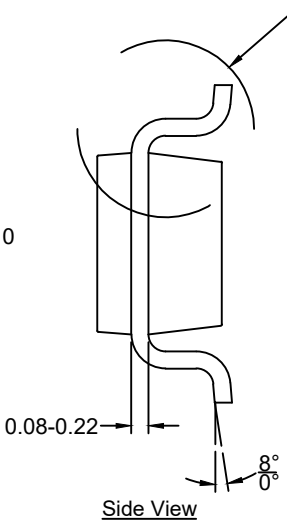
Notes:
1. Dimensioning and tolerances per ASME Y14.5M-1994.
2. Package conforms to EIAJ SC70 and JEDEC MO-203AA.
3. Dimensions body x and y are exclusive of mold flash, protrusions, or gate burrs.
4. Footlength L measured at reference to gauge plane.
5. 0.08mm and 0.15mm from the lead tip.
6. Controlling dimension: MILLIMETER. Converted inch dimen

Package Outline Drawing

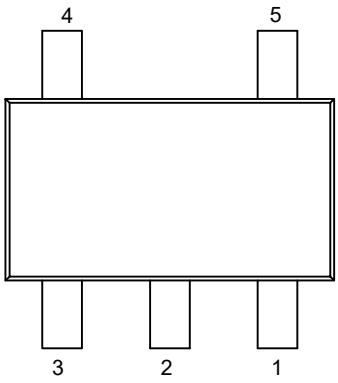
P5.064
KA0005AB
5-SOT 2.90 x 1.60 x 1.45 mm Body, 0.95mm Pitch Lead Small Outline Transistor Plastic Package
Rev04, Jul 22, 2025



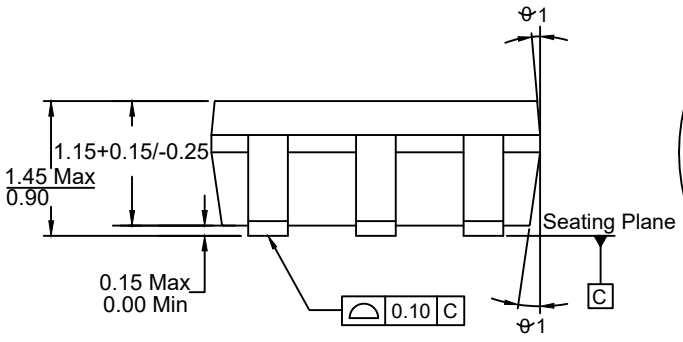
Top View



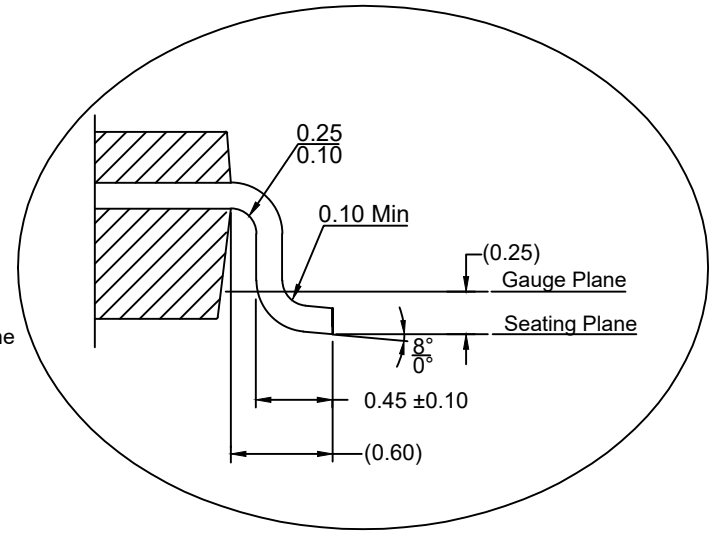
Side View



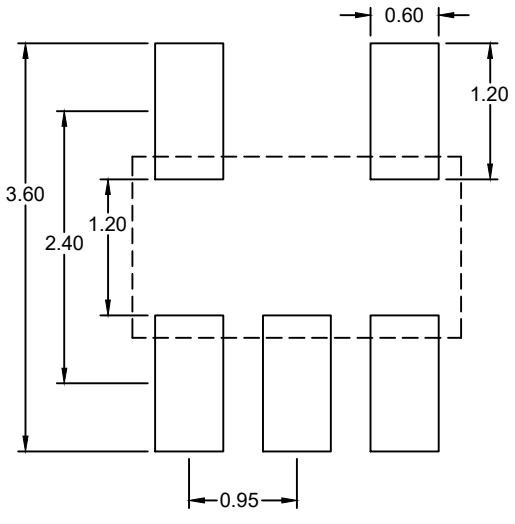
Bottom View



Side View



Detail "A"



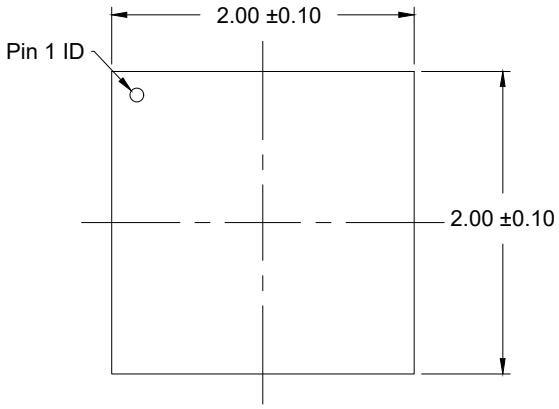
Recommended Land Pattern

Notes:

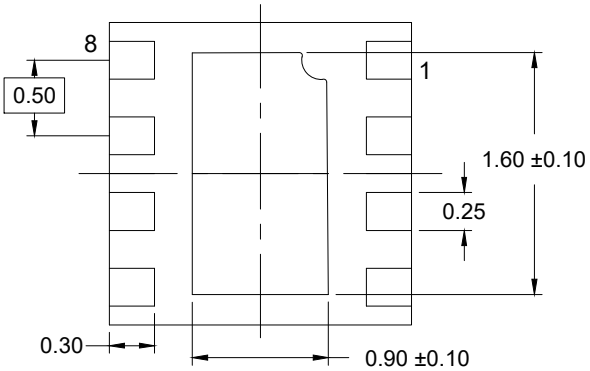
1. Dimensioning and tolerance per ASME Y14.5M-1994.
2. Package conforms to EIAJ SC-74 and JEDEC MO178AA
3. Package length and width are exclusive of mold flash, protrusions or gate burrs.
4. Footlength measured at reference to gauge plane.
5. Lead thickness applies to the flat section of the lead between 0.08mm and 0.15mm from the lead tip.
6. Controlling dimension: Millimeter.

Package Outline Drawing

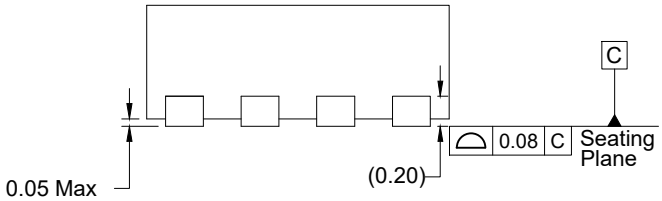
L8.2x2F
DW0008AA
8-DFN 2.0 x2.0 x 0.8 mm Body, 0.50mm Pitch
Rev 00, Jan 21, 2025



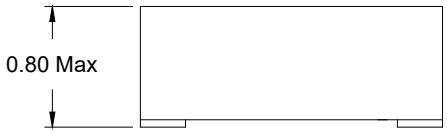
Top View



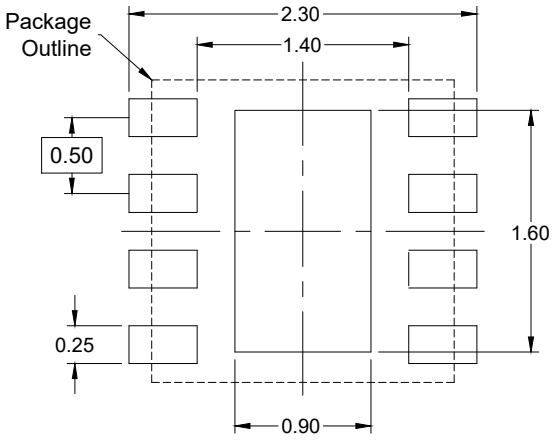
Bottom View



Side View (Rotated 90°)



Side View



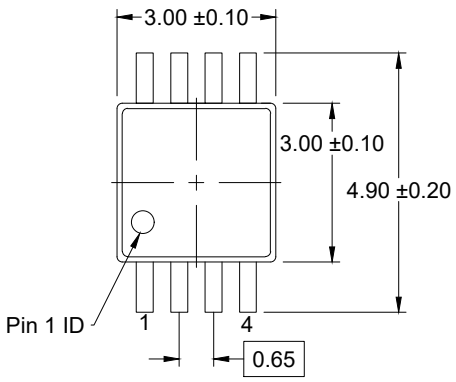
Recommende Land Pattern

Notes:

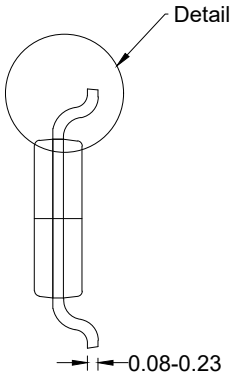
1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

Package Outline Drawing

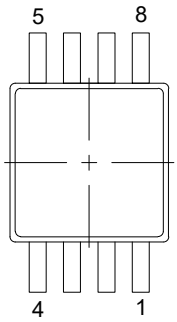
M8.118D
HV0008AC
8-MSOP 3.00 x4.90 x 1.10 mm Body, 0.65 mm Pitch
Rev03, Jul 11, 2025



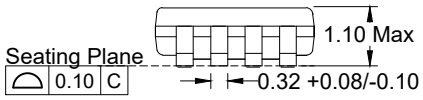
Top View



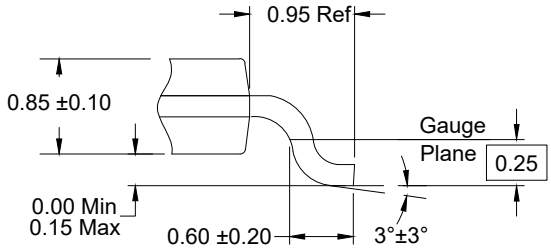
Side View



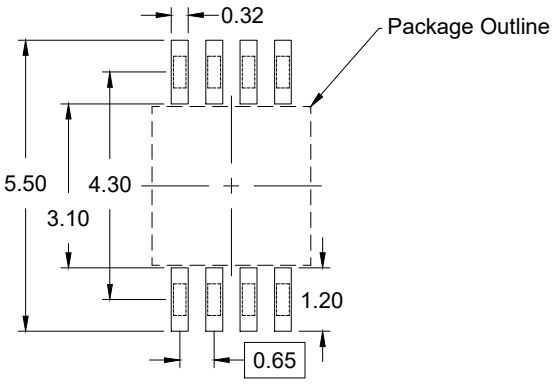
Bottom View



Side View



Detail "X"



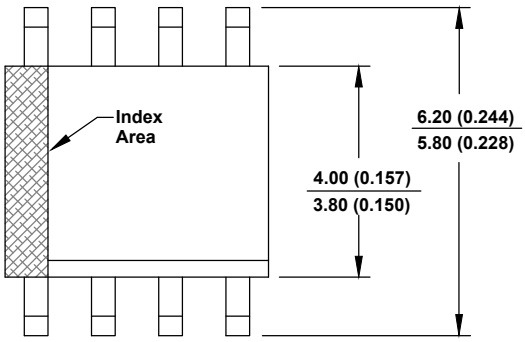
Typical Recommended Land Pattern

Notes:

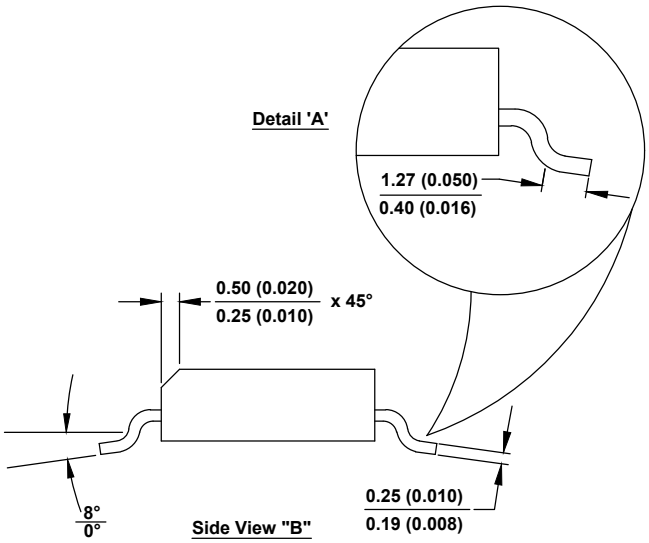
1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Foot length is measured at gauge plane 0.25 mm above seating plane.

Package Outline Drawing

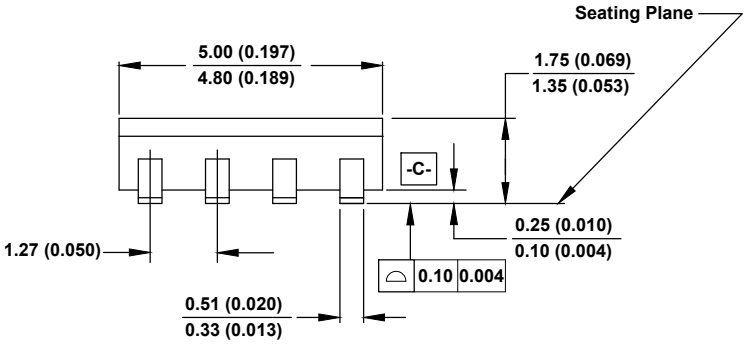
M8.15
GS0008AC
8-Lead Narrow Body Small Outline Plastic Package 4.90 x 3.90 x 1.43 mm Body, 1.27 mm Pitch
Rev08, Jul 7, 2025



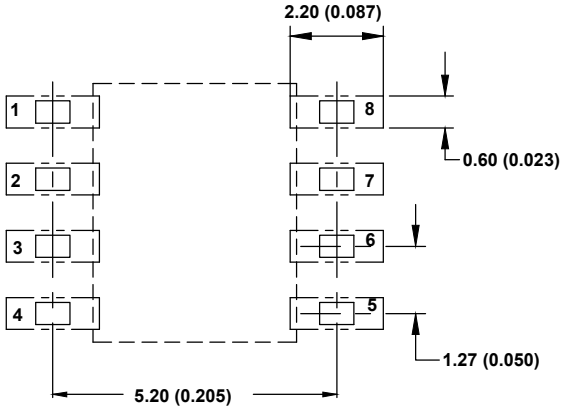
Top View



Side View "B"



Side View "A"



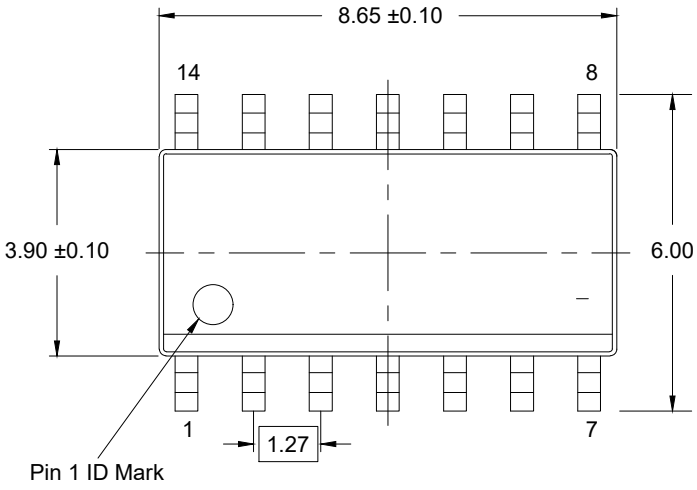
Typical Recommended Land Pattern

Notes:

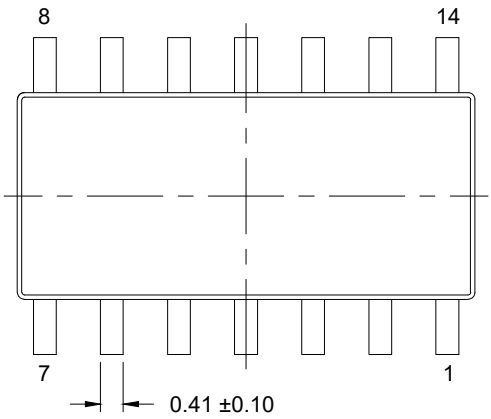
1. Dimensioniong and tolerancing conform to ASME Y14.5M-1994.
2. Package length does not include mold flash, protrusion or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
7. Controlling dimension: MILLIMETER. Converted inch dimension are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.

Package Outline Drawing

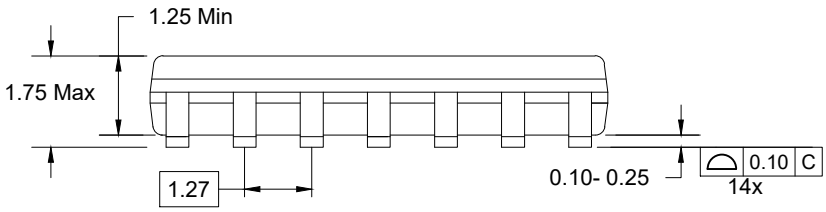
M14.15
GS0014AB
14-SOICN 8.65 x 3.90 x 1.75 mm Body, 1.27 mm Pitch
Rev03, Jun 26, 2025



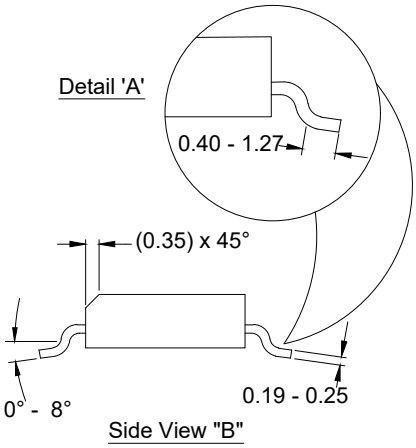
Top View



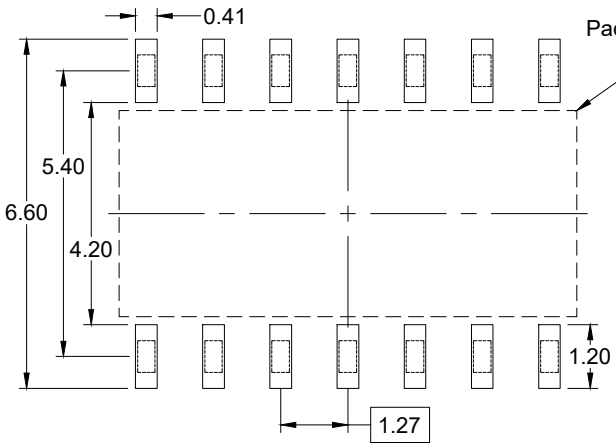
Bottom View



Side View



Side View "B"



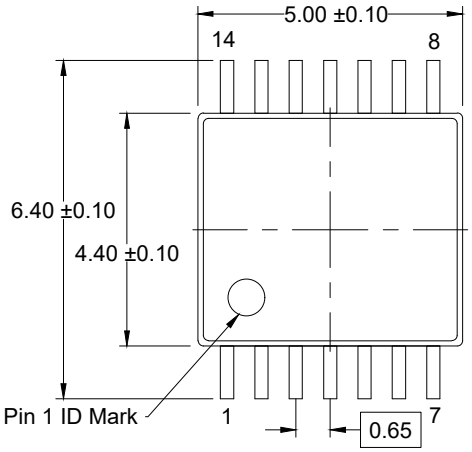
Typical Recommended Land Pattern

Notes:

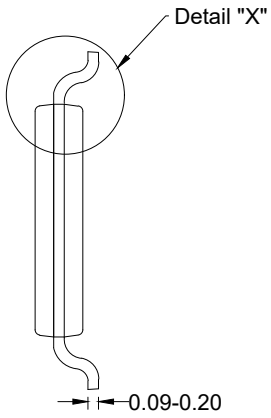
1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Foot length is measured at gauge plane 0.25 mm above seating plane.

Package Outline Drawing

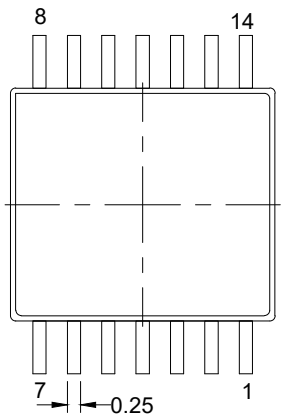
M14.173
HV0014AA
14-Lead Thin Shrink Small Outline package (TSSOP) 5.00 x 4.40 x 1.20 mm Body, 0.65 mm Pitch
Rev04, Jun 26, 2025



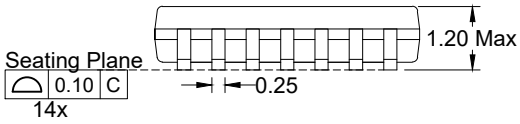
Top View



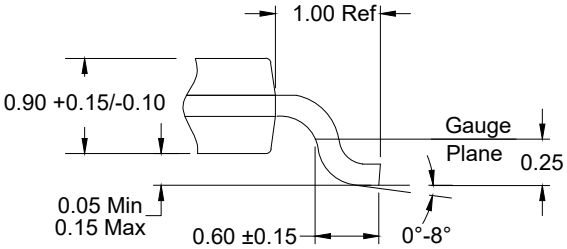
Side View



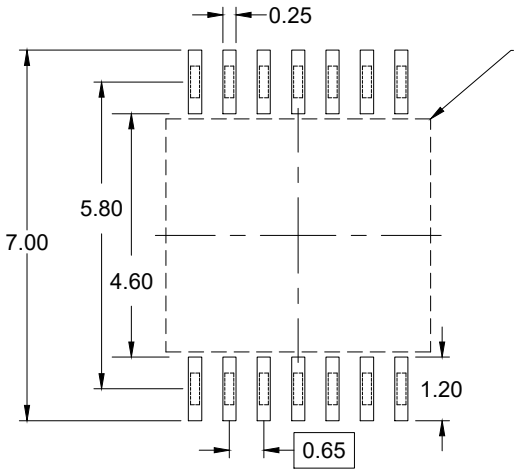
Bottom View



Side View



Detail "X"



Typical Recommended Land Pattern

Notes:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Foot length is measured at gauge plane 0.25 mm above seating plane.

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