ISL29044A

Low Power Ambient Light and Proximity Sensor with Internal IR-LED and Digital Output

FN8419
Rev 3.00
April 28, 2016

The ISL29044A is an integrated ambient and infrared light-to-digital converter with a built-in IR LED and I^2C Interface (SMBus Compatible). This device uses two independent ADCs for concurrently measuring ambient light and proximity in parallel. The flexible interrupt scheme is designed for minimal micro-controller utilization.

For ambient light sensor (ALS) data conversions, an ADC converts photodiode current (with a light sensitivity range up to 3200Lux) in 100ms per sample. The ADC rejects 50Hz/60Hz flicker noise caused by artificial light sources.

For proximity sensor (Prox) data conversions, the built-in driver turns on an internal infrared LED and the proximity sensor ADC converts the reflected IR intensity to digital. This ADC rejects ambient IR noise (such as sunlight) and has a 547µs conversion time.

The ISL29044A provides low power operation of ALS and proximity sensing with a typical 133µA normal operation current (108µA for sensors and internal circuitry, ~25µA for LED) with 220mA current pulses for a net 100µs, repeating every 800ms (or under).

The ISL29044A uses both a hardware pin and software bits to indicate an interrupt event has occurred. An ALS interrupt is defined as a measurement that is outside a set window. A proximity interrupt is defined as a measurement over a threshold limit. The user may also require that both ALS/Prox interrupts occur at once, up to 16 times in a row before activating the interrupt pin.

The ISL29044A is designed to operate from 2.25V to 3.63V over the -40°C to +85°C ambient temperature range. It is packaged in a clear, lead-free 8 Ld ODFN package.

Features

- Internal LED + Sensor = complete solution
- Works under all light sources including sunlight
- Dual ADCs measure ALS/Prox concurrently
- <1.0µA Supply current when powered down
- Temperature compensated
- Pb-Free (RoHS compliant)

Intelligent and Flexible Interrupts

- Independent ALS/Prox interrupt thresholds
- Adjustable interrupt persistency
  - 1/4/8/16 consecutive triggers required before interrupt

Applications

- Display and keypad dimming adjustment and proximity sensing for:
  - Mobile devices: Smart phone, PDA, GPS
  - Computing devices: Laptop PC, Netbook, Tablet PC
  - Consumer devices: LCD-TV, digital picture frame, digital camera
  - Industrial and medical light and proximity sensing

Related Literature

- See AN1436, “Proximity Sensors”

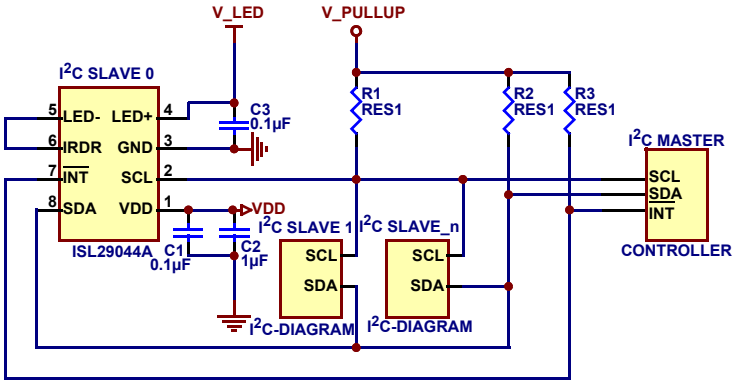


FIGURE 1. TYPICAL APPLICATION

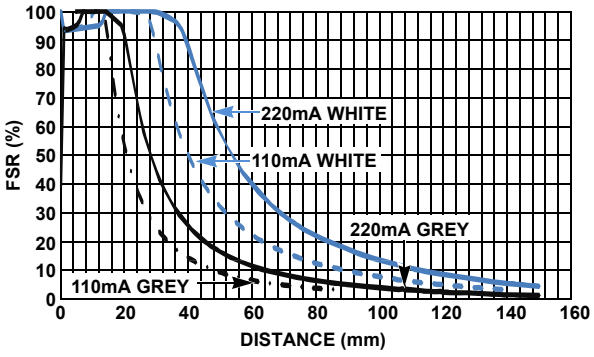
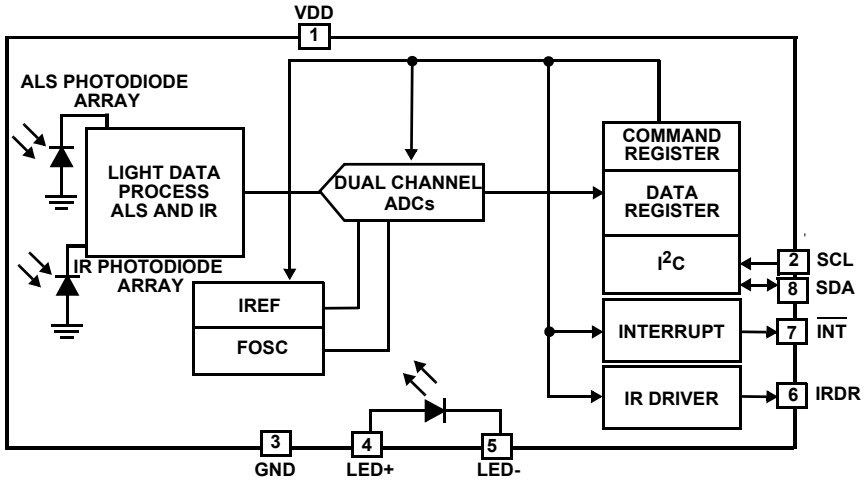


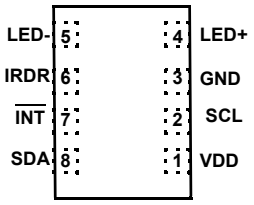
FIGURE 2. PROXIMITY RESPONSE vs DISTANCE

ISL29044A Block Diagram



Pin Configuration

ISL29044A
(8 LD 2.36x3.94 (mm) OPTICAL CO-PACKAGE)
TOP VIEW



Pin Descriptions

PIN#	PIN NAME	DESCRIPTIONS
1	VDD	Voltage supply 2.25V to 3.63V.
2	SCL	I^2C clock line can be pulled from 1.7V to above V_{DD}, 3.63V max.
3	GND	Ground
4	LED+	Anode of IR LED
5	LED-	Cathode of IR LED
6	IRDR	IR-LED driver pin - current flows into ISL29044A from LED cathode.
7	$\overline{INT}$	$\overline{Interrupt}$ pin; Logic output (open-drain) for interrupt.
8	SDA	I^2C data line can be pulled from 1.7V to above V_{DD}, 3.63V max.

Ordering Information

PART NUMBER (Notes 1, 2, 3)	TEMP. RANGE (°C)	PACKAGE Tape & Reel (Pb-free)	PKG. DWG. #
ISL29044AIROMZ-T7	-40 to +85	8 Ld Optical Co-package	L8.2.36x3.94
ISL29044AIROMZ-EVALZ	Evaluation Board		

NOTES:

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets: molding compounds, die attach materials, NiPdAu plate (e4 termination finish), which are all RoHS compliant. The ISL29044A is compatible with limited SnPb and Pb-free soldering operations. The ISL29044A is MSL classified. See Tech Brief TB487 (*Surface Mount Assembly Guidelines for Optical Co-Package Sensor and LED*) for reflow profile and more information.
3. For more information on MSL please see tech brief TB477.

Absolute Maximum Ratings (T_A = +25°C)

V_{DD} Supply Voltage between V_{DD} and GND 4.0V
I^2C Bus Pin Voltage (SCL, SDA) . . . . . -0.5V to 4.0V
I^2C Bus Pin Current (SCL, SDA) . . . . . <10mA
IRDR, LED+Pin Voltage 5.5V
INT Pin Voltage . . . . . -0.5V to 4.0V
INT Pin Current . . . . . <10mA
ESD Rating
Human Body Model 2kV

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Ld Optical Module Package (Notes 4, 5)	113	58

Maximum Die Temperature . . . . . +90°C
Storage Temperature . . . . . -40°C to +85°C
Operating Temperature . . . . . -40°C to +85°C
Pb-Free Reflow Profile . . . . . see TB487
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications V_{DD} = 3.0V, T_A = +25°C.

PARAMETER	DESCRIPTION	CONDITION	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
V_{DD}	Power Supply Range		2.25	3.0	3.63	V
SR_V_{DD}	Power Supply Slew Rate	V_{DD} Rising Edge between 0.4V and 2.25V	0.5			V/ms
VLED+	Voltage Supply for IR LED				5	V
I_{DD_OFF}	Supply Current when Powered Down	ALS_EN = 0; PROX_EN = 0		0.05	0.8	µA
I_{DD_NORM}	Supply Current for ALS+Prox in Sleep Time	ALS_EN = 1; PROX_EN = 1		108	135	µA
$I_{DD\_PRX\_SLP}$	Supply Current for Prox in Sleep Time	ALS_EN = 0; PROX_EN = 1		79		µA
I_{DD_ALS}	Supply Current for ALS	ALS_EN = 1; PROX_EN = 0		94		µA
t_{INTGR_ALS}	12-bit ALS Integration/Conversion Time		80	100	112	ms
t_{INTGR_PROX}	8-bit Prox Integration/Conversion Time			0.51		ms
$DATA_{ALS\_0}$	ALS Result when Dark	$E_{AMBIENT}$ = 0 Lux, 2k Range		1	3	Counts
$DATA_{ALS\_F}$	Full Scale ALS ADC Code	$E_{AMBIENT}$ > Selected Range Maximum Lux			4095	Counts
$\frac{\Delta DATA}{DATA}$	Count Output Variation Over Three Light Sources: Fluorescent, Incandescent and Sunlight	Ambient Light Sensing		±10		%
$DATA_{ALS\_1}$	Light Count Output with LSB of 0.0488 Lux/count	E = 48.8 Lux, Fluorescent (Notes 7), ALS_RANGE = 0		1000		Counts
$DATA_{ALS\_2}$	Light Count Output With LSB of 0.7814 Lux/count	E = 288 Lux, Fluorescent (Note 7), ALS_RANGE = 1	265	370	463	Counts
$DATA_{PROX\_0}$	Prox Measurement w/o Object in Path			1		Counts
$DATA_{PROX\_F}$	Full Scale Prox ADC Code				255	Counts
t_r	Rise Time for IRDR Sink Current	R_{LOAD} = 15Ω at IRDR pin, 20% to 80%		500		ns
t_f	Fall Time for IRDR Sink Current	R_{LOAD} = 15Ω at IRDR pin, 80% to 20%		400		ns
I_{IRDR_0}	IRDR Sink Current	PROX_DR = 0; V_{IRDR} = 0.5V	85	109	135	mA
I_{IRDR_1}	IRDR Sink Current	PROX_DR = 1; V_{IRDR} = 0.5V		208		mA
I_{IRDR_LEAK}	IRDR Leakage Current	PROX_EN = 0; V_{DD} = 3.63V (Note 8)		0.001	1	µA
V_{IRDR}	Acceptable Voltage Range on IRDR Pin	Register bit PROX_DR = 0	0.5		4.3	V
t_{PULSE}	Net I_{IRDR} On Time Per PROX Reading			100		µs
F_{I^2C}	I^2C Clock Rate Range				400	kHz
V_{I^2C}	Supply Voltage Range for I^2C Interface		1.7		3.63	V

Electrical Specifications V_{DD} = 3.0V, T_A = +25°C. (Continued)

PARAMETER	DESCRIPTION	CONDITION	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
V_{IL}	SCL and SDA Input Low Voltage				0.55	V
V_{IH}	SCL and SDA Input High Voltage		1.25			V
I_{SDA}	SDA Current Sinking Capability	V_{OL} = 0.4V	3	5		mA
$I_{\overline{INT}}$	$\overline{INT}$ Current Sinking Capability	V_{OL} = 0.4V	3	5		mA
$PSRR_{IRDR}$	$\overline{(\Delta I_{\overline{IRDR}})}/\overline{(\Delta V_{\overline{IRDR}})}$	PROX_DR = 0; V_{IRDR} = 0.5V to 4.3V		5.8		mA/V

NOTES:

6. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
7. An 530nm Green LED is used in production test. The LED irradiance is calibrated to produce the same DATA count against a fluorescent light source of the same lux level.
8. Ability to guarantee I_{IRDR} leakage of ~1nA is limited by test hardware.

IR-LED Specifications T_A = +25°C

PARAMETER	DESCRIPTION	CONDITION	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
V_F	IR-LED Forward Voltage Drop	I_F = 200mA		2.0		V
		I_F = 100mA		1.8		V
I_R	IR-LED Reverse-Bias Current	V_R = 5.5V		0.061	5	µA
λ_P	IR-LED Peak Output Wavelength	I_F = 110mA		858		nm
Δ_λ	IR-LED Spectral Half-Width	I_F = 110mA		39		nm
Φ_E	IR-LED Radiant Power	I_F = 110mA		30		mW
I	$\overline{\text{IR-LED Radiant Intensity (in 0.01sr) at 0°}}$	I_F = 110mA		128		mW/sr

I^2C Electrical Specifications For SCL and SDA unless otherwise noted, V_{DD} = 3V, T_A = +25°C (Note 9).

PARAMETER	DESCRIPTION	CONDITION	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
V_{I^2C}	Supply Voltage Range for I^2C Interface		1.7		3.63	V
f_{SCL}	SCL Clock Frequency				400	kHz
V_{IL}	SCL and SDA Input Low Voltage				0.55	V
V_{IH}	SCL and SDA Input High Voltage		1.25			V
V_{hys}	Hysteresis of Schmitt Trigger Input		$0.05V_{DD}$			V
V_{OL}	Low-level Output Voltage (Open-drain) at 4mA Sink Current				0.4	V
I_i	Input Leakage for each SDA, SCL Pin		-10		10	µA
t_{SP}	Pulse Width of Spikes that must be Suppressed by the Input Filter				50	ns
t_{AA}	SCL Falling Edge to SDA Output Data Valid				900	ns
C_i	Capacitance for each SDA and SCL Pin				1	pF
$t_{HD:STA}$	Hold Time (Repeated) START Condition	After this period, the first clock pulse is generated.	600			ns
t_{LOW}	LOW Period of the SCL Clock	Measured at the 30% of VDD crossing.	1300			ns
t_{HIGH}	HIGH Period of the SCL Clock		600			ns

I²C Electrical Specifications

For SCL and SDA unless otherwise noted, V_{DD} = 3V, T_A = +25°C (Note 9). **(Continued)**

PARAMETER	DESCRIPTION	CONDITION	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
$t_{SU:STA}$	Set-up Time for a Repeated START Condition		600			ns
$t_{HD:DAT}$	Data Hold Time		30			ns
$t_{SU:DAT}$	Data Set-up Time		100			ns
t_R	Rise Time of both SDA and SCL Signals	(Note 10)	20 + 0.1xC_b			ns
t_F	Fall Time of both SDA and SCL Signals	(Note 10)	20 + 0.1xC_b			ns
$t_{SU:STO}$	Set-up Time for STOP Condition		600			ns
t_{BUF}	Bus Free Time Between a STOP and START Condition		1300			ns
C_b	Capacitive Load for Each Bus Line				400	pF
$R_{pull-up}$	SDA and SCL System Bus Pull-up Resistor	Maximum is determined by t_R and t_F	1			kΩ
$t_{VD;DAT}$	Data Valid Time				0.9	µs
$t_{VD:ACK}$	Data Valid Acknowledge Time				0.9	µs
V_{nL}	Noise Margin at the Low Level		0.1V_{DD}			V
V_{nH}	Noise Margin at the High Level		0.2V_{DD}			V

NOTES:

9. All parameters in I²C Electrical Specifications table are guaranteed by design and simulation.
10. C_b is the capacitance of the bus in pF.

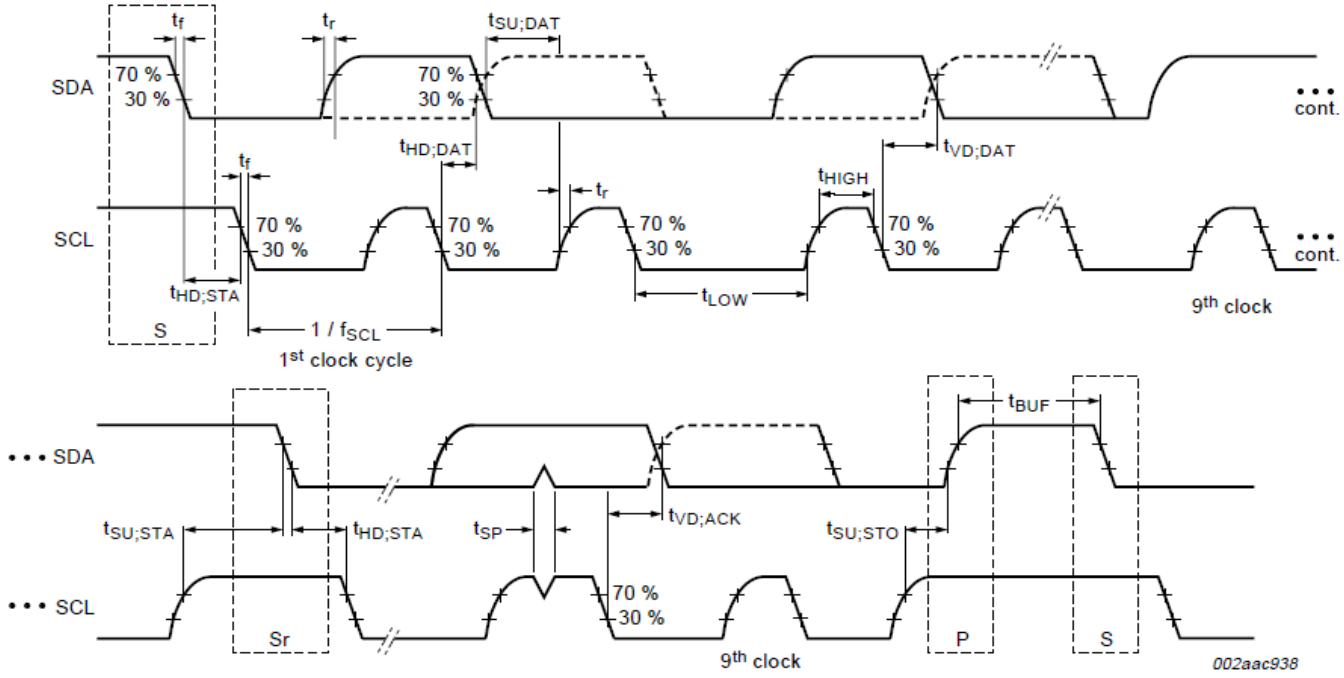


FIGURE 3. I²C TIMING DIAGRAM

Typical Performance Curves V_{DD} = 3.0V

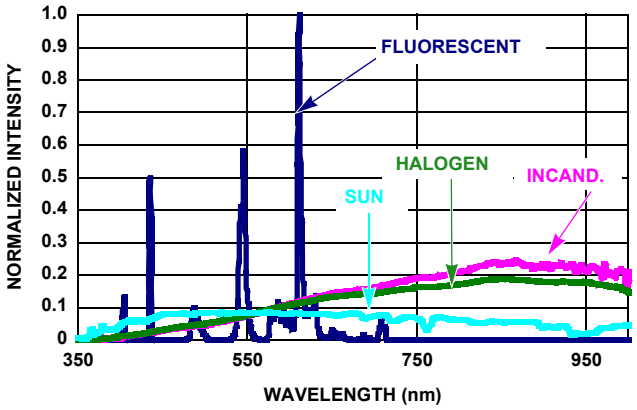


FIGURE 4. SPECTRUM OF FOUR LIGHT SOURCES NORMALIZED BY LUMINOUS INTENSITY (LUX)

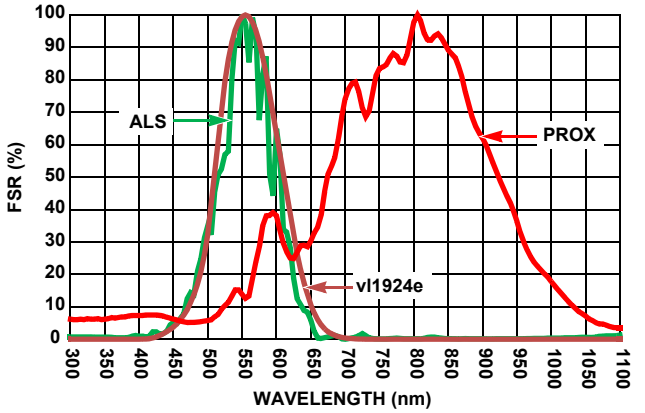


FIGURE 5. ISL29044A SENSITIVITY TO DIFFERENT WAVELENGTHS

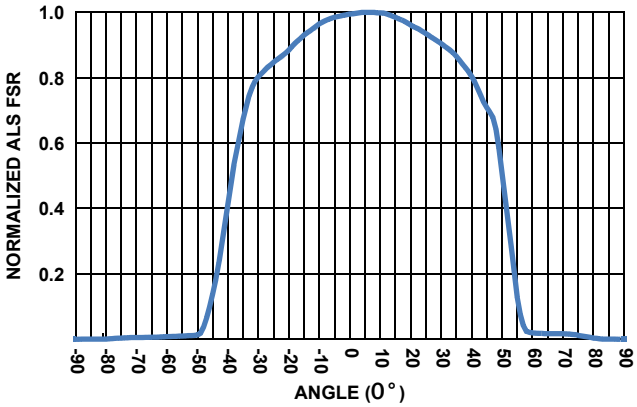


FIGURE 6. ANGULAR SENSITIVITY OF ALS

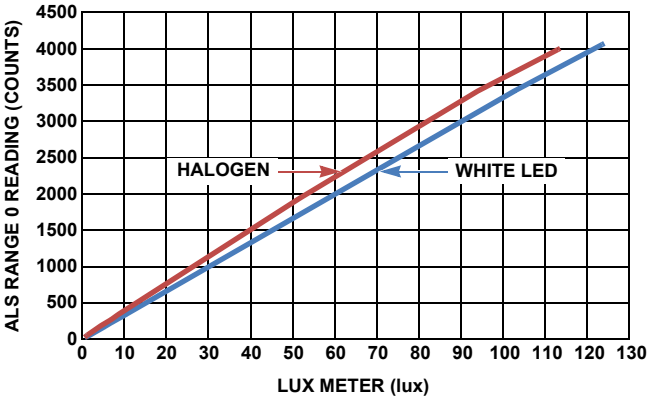


FIGURE 7. ALS TRANFER FUNCTION 2 LIGHT SOURCES (RANGE0)

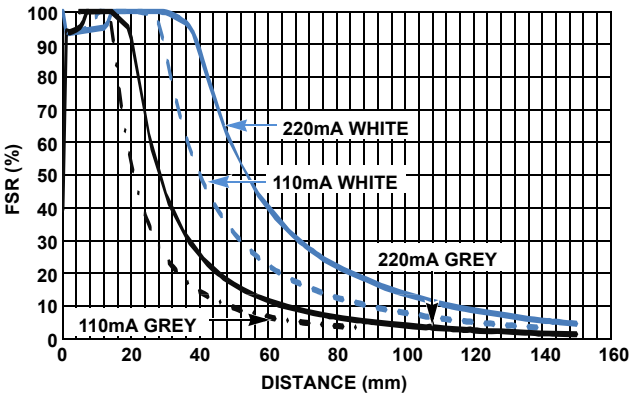


FIGURE 8. PROX COUNTS vs DISTANCE WITH 10cmx10cm REFLECTORS

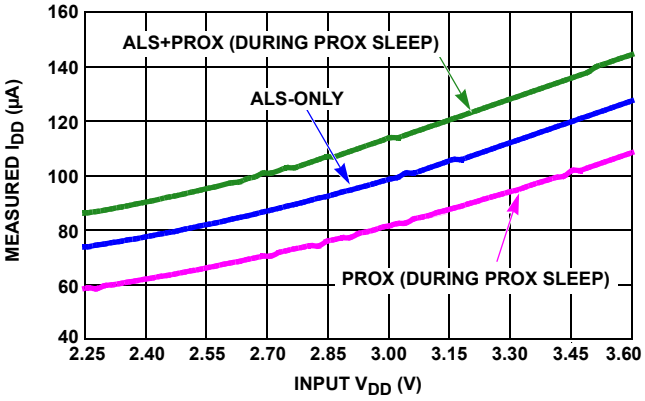


FIGURE 9. V_{DD} vs I_{DD} FOR VARIOUS MODES OF OPERATION

Typical Performance Curves V_{DD} = 3.0V (Continued)

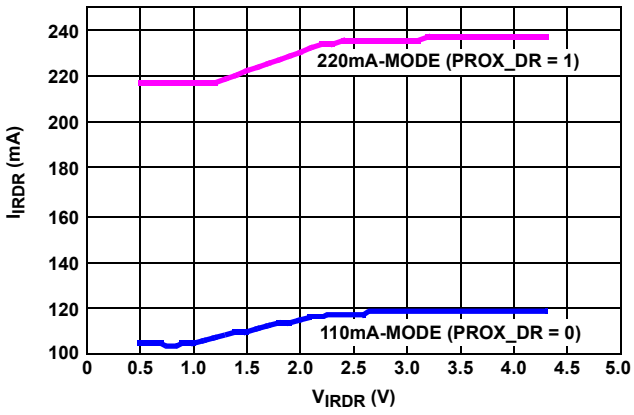


FIGURE 10. IRDR PULSE AMPLITUDE vs V_{IRDR}

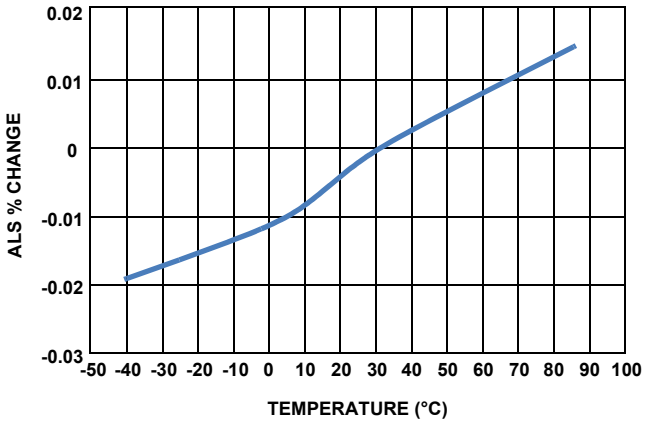


FIGURE 11. ALS RANGE1 OVER-TEMPERATURE AT 75 LUX WHITE LED

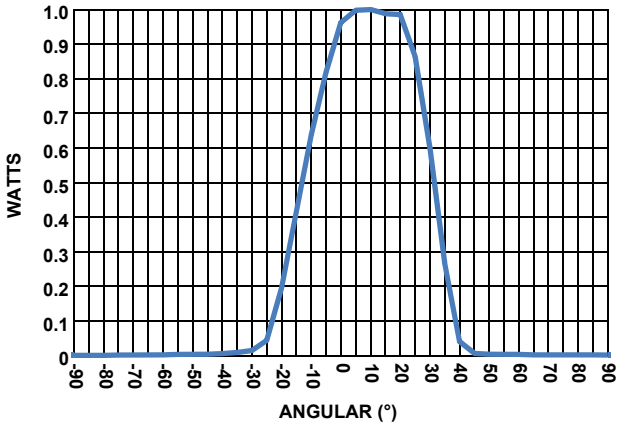


FIGURE 12. RADIATION EMISSION PATTERN IRLED TRANSVERSE

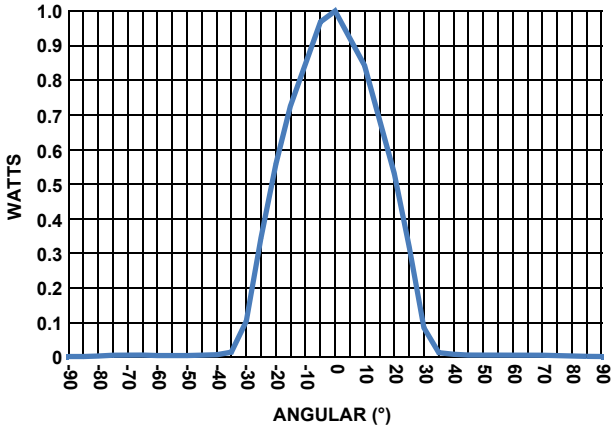


FIGURE 13. IR-LED LATERAL EMISSION PATTERN (NORMALIZED INTENSITY vs Θ_{TRANS})

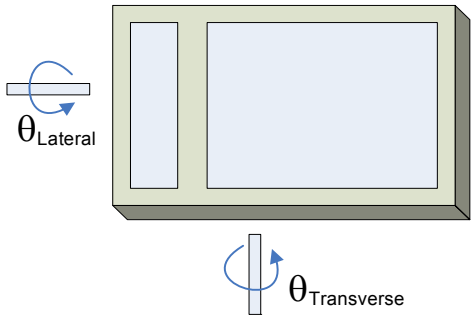


FIGURE 14. DEFINITION OF LATERAL AND TRANSVERSE AXES

Principles of Operation

Photodiodes and ADCs

The ISL29044A contains two photodiode arrays, which convert photons (light) into current. The ALS photodiodes are constructed to mimic the human eye's wavelength response curve to visible light (see Figure 5). The ALS photodiodes' current output is digitized by a 12-bit ADC in 100ms. These 12 bits can be accessed by reading from I^2C registers 0x9 and 0xA when the ADC conversion is completed.

The ALS converter is a charge-balancing, integrating 12-bit ADC. Charge-balancing is best for converting small current signals in the presence of periodic AC noise. Integrating over 100ms highly rejects both 50Hz and 60Hz light flicker by picking the lowest integer number of cycles for both 50Hz/60Hz frequencies.

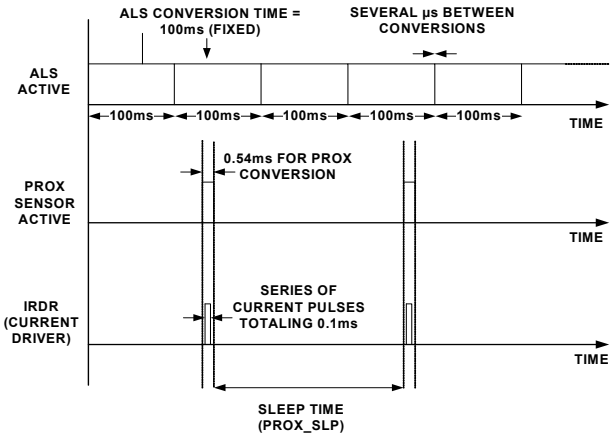


FIGURE 15. TIMING DIAGRAM FOR PROX/ALS EVENTS - NOT TO SCALE

The proximity sensor is an 8-bit ADC that operates in a similar fashion. When proximity sensing is enabled, the IRDR pin will drive the internal infrared LED, the emitted IR reflects off an object (e.g., a human head) back into the ISL29044A, and a sensor converts the reflected IR wave to a current signal in 0.54ms. The ADC subtracts the IR reading before and after the LED is driven (to remove ambient IR such as sunlight), and converts this value to a digital count stored in Register 0x8.

The ISL29044A is designed to run two conversions concurrently: a proximity conversion and an ALS (or IR) conversion. Please note that because of the conversion times, the user must let the ADCs perform one full conversion first before reading from I^2C Registers PROX_DATA (wait 0.54ms) or ALSIR_DT1/2 (wait 100ms). The timing between ALS and Prox conversions is arbitrary, as shown in Figure 15. The ALS runs continuously with new data available every 100ms. The proximity sensor runs continuously with a time between conversions decided by PROX_SLP (Register 1 Bits [6:4]).

Ambient Light and IR Sensing

The ISL29044A is set for ambient light sensing when Register bit ALSIR_MODE = 0 and ALR_EN = 1. The light-wavelength response of the ALS appears, as shown in Figure 5. ALS measuring mode (as opposed to IR measuring mode) is set by default.

When the part is programmed for infrared (IR) sensing (ALSIR_MODE = 1; ALS_EN = 1), infrared light is converted into a current and digitized by the same ALS ADC. The result of an IR conversion is *strongly related* to the amount of IR energy incident on our sensor, but is unitless and is referred to in digital counts.

Proximity Sensing

When proximity sensing is enabled (PROX_EN = 1), the internal IR LED is driven for 0.1ms by the built-in IR LED driver through the IRDR pin. The amplitude of the IR LED current depends on Register 1 bit 3: PROX_DR. If this bit is low, the load will see a fixed 110mA current pulse. If this bit is high, the load on IRDR will see a fixed 220mA current pulse, as seen in Figure 16.

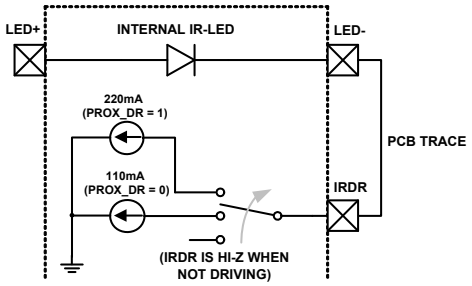


FIGURE 16. CURRENT DRIVE MODE OPTIONS

When the IR from the LED reaches an object and gets reflected back into the ISL29044A, the reflected IR light is converted into current as per the IR spectral response shown in Figure 5. One entire proximity measurement takes 0.54ms for one conversion (which includes 0.1ms spent driving the LED), and the period *between* proximity measurements is decided by PROX_SLP (sleep time) in Register 1 Bits 6:4.

Average LED driving current consumption is given by Equation 1.

$$I_{IRDR;AVG} = \frac{I_{IRDR;PEAK} \times 100\mu s}{540\mu s + t_{SLEEP}} \quad \text{(EQ. 1)}$$

A typical IRDR scheme is 220mA amplitude pulses every 800ms, which yields 28µA DC.

Total Current Consumption

Total current consumption is the sum of I_{DD} and I_{IRDR}. The IRDR pin sinks current (see Figure 16) and the average IRDR current can be calculated using Equation 1. I_{DD} depends on voltage and the mode-of-operation, as seen in Figure 9.

Interrupt Function

The ISL29044A has an intelligent interrupt scheme designed to shift some logic processing away from the intensive microcontroller I^2C polling routines (which consume power) and towards a more independent light sensor, which can instruct a system to "wake up" or "go to sleep".

An ALS interrupt event (ALS_FLAG) is governed by Registers 5 through 7. The user writes a high and low threshold value to these registers and the ISL29044A will issue an ALS interrupt flag if the actual count stored in Registers 0x9 and 0xA are outside the user's programmed window. The user must write 0 to clear the ALS_FLAG.

A proximity interrupt event (PROX_FLAG) is governed by the high and low thresholds in registers 3 and 4 (PROX_LT and PROX_HT). PROX_FLAG is set when the measured proximity data is more than the higher threshold X-times-in-a-row (X is set by user; see following paragraph). The proximity interrupt flag is cleared when the prox data is lower than the low proximity threshold X-times-in-a-row, or when the user writes “0” to PROX_FLAG.

Interrupt persistency is another useful option available for both ALS and proximity measurements. Persistency requires X-in-a-row interrupt flags before the $\overline{INT}$ pin is driven low. Both ALS and Prox have their own independent interrupt persistency options. See ALS_PRST and PROX_PRST bits in Register 2.

The final interrupt option is the ability to AND or OR the two interrupt flags using Register 2 Bit 0 (INT_CTRL). If the user wants both ALS/Prox interrupts to happen at the same time before changing the state of the interrupt pin, set this bit high. If the user wants the interrupt pin to change state when *either* the ALS or the Proximity interrupt flag goes high, leave this bit to its default of 0.

V_{DD} Power-up and Power Supply Considerations

Upon power-up, please ensure a V_{DD} slew rate of 0.5V/ms or greater. After power-up, or if the user’s power supply temporarily deviates from our specification (2.25V to 3.63V), Intersil recommends the user write the following: write 0x00 to register 0x01, write 0x29 to register 0x0F, write 0x00 to register 0x0E, and write 0x00 to register 0x0F. The user should then wait ~1ms or more and then rewrite all registers to the desired values. If the user prefers a hardware reset method instead of writing to test registers: set V_{DD} = 0V for 1 second or more, power back up at the required slew rate, and write registers to the desired values.

Power-Down

To put the ISL29044A into a power-down state, the user can set both PROX_EN and ALS_EN bits to 0 in Register 1 or more; simply set all of Register 1 to 0x00.

Serial Interface

The ISL29044A supports the Inter-Integrated Circuit (I^2C) bus data transmission protocol. The I^2C bus is a two wire serial bidirectional interface consisting of SCL (clock) and SDA (data). Both the wires are connected to the device supply via pull-up resistors. The I^2C protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The transmitting device pulls down the SDA line to transmit a “0” and releases it to transmit a “1”. The master always initiates the data transfer, only when the bus is not busy, and provides the clock for both transmit and receive operations. The ISL29044A operates as a slave device in all applications. The serial communication over the I^2C interface is conducted by sending the most significant bit (MSB) of each byte of data first.

Start Condition

During data transfer, the SDA line must remain stable, while the SCL line is HIGH. All I^2C interface operations must begin with a START condition, which is a HIGH-to-LOW transition of SDA while SCL is HIGH (refer to Figure 17). The ISL29044A continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (refer to Figure 17). A START condition is ignored during the power-up sequence.

Stop Condition

All I^2C interface operations must be terminated by a STOP condition, which is a LOW-to-HIGH transition of SDA, while SCL is HIGH (refer to Figure 17). A STOP condition at the end of a read/write operation places the device in its standby mode. If a stop is issued in the middle of a Data byte, or before 1 full Data byte + ACK is sent, then the serial communication of ISL29044A resets itself without performing the read/write. The contents of the array are not affected.

Acknowledge

An acknowledge (ACK) is a software convention used to indicate a successful data transfer. The transmitting device releases the SDA bus after transmitting 8-bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data (refer to Figure 17). The ISL29044A responds with an ACK after recognition of a START condition followed by a valid Identification Byte, and once again, after successful receipt of an Address Byte. The ISL29044A also responds with an ACK after receiving a Data byte of a write operation. The master must respond with an ACK after receiving a Data byte of a read operation.

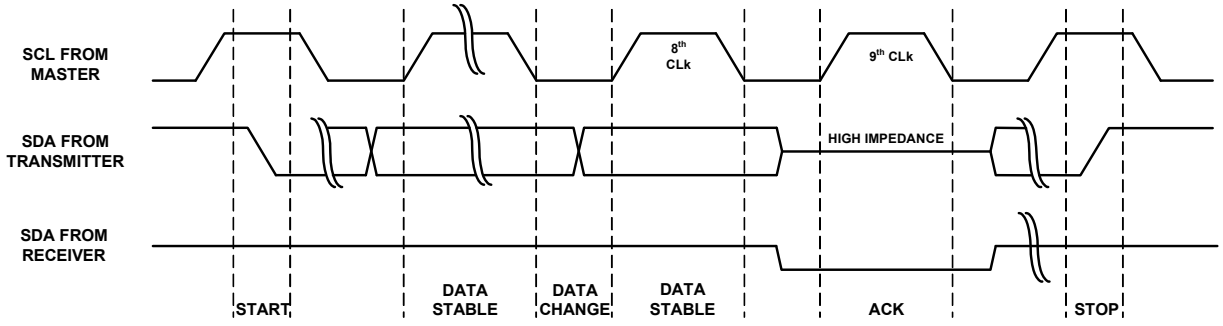


FIGURE 17. START, DATA STABLE, ACKNOWLEDGE, AND STOP CONDITION

Device Addressing

Following a START condition, the master must output a Device Address byte. The 7 MSBs of the Device Address byte are known as the device identifier. The device identifier bits of ISL29044A are internally hard-wired as “1000100”. The LSB of the Device Address byte is defined as read or write (R/$\overline{W}$) bit. When this R/$\overline{W}$ bit is a “1”, a read operation is selected and when “0”, a write operation is selected (refer to Figure 18). The master generates a START condition followed by a Device Address byte 1000100x (x as R/$\overline{W}$) and the ISL29044A compares it with the internal device identifier. Upon a correct comparison, the device outputs an acknowledge (LOW) on the SDA line (refer to Figure 17).

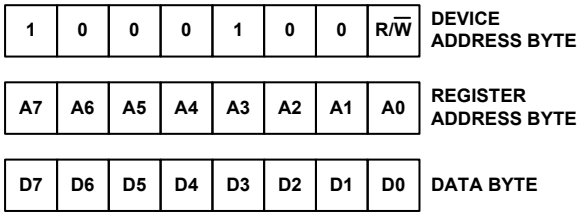


FIGURE 18. DEVICE ADDDRESS, REGISTER ADDRESS, and DATA BYTE

Write Operation

BYTE WRITE

In a byte write operation, the ISL29044A requires the Device Address byte, Register Address byte, and the Data byte. The master starts the communication with a START condition. Upon receipt of the Device Address byte, Register Address byte, and the Data byte, the ISL29044A responds with an acknowledge (ACK). Following the ISL29044A data acknowledge response, the master terminates the transfer by generating a STOP condition. The ISL29044A then begins an internal write cycle of the data to the volatile memory. During the internal write cycle, the device inputs are disabled and the SDA line is in a high impedance state, so the device will not respond to any requests from the master (refer to Figure 19).

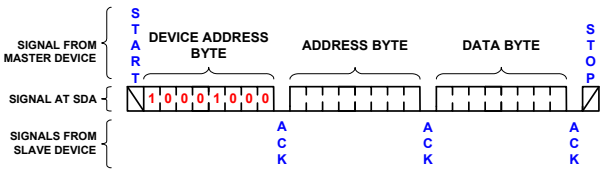


FIGURE 19. BYTE WRITE SEQUENCE

BURST WRITE

The ISL29044A has a burst write operation, which allows the master to write multiple consecutive bytes from a specific address location. It is initiated in the same manner as the byte write operation, but instead of terminating the write cycle after the first Data byte is transferred, the master can write to the whole register array. After the receipt of each byte, the ISL29044A responds with an acknowledge, and the address is internally incremented by one. The address pointer remains at the last address byte written. When the counter reaches the end of the register address list, it “rolls over” and goes back to the first Register Address.

Read Operation

The ISL29044A has two basic read operations: Byte Read and Burst Read.

BYTE READ

Byte read operations allow the master to access any register location in the ISL29044A. The Byte read operation is a two step process. The master issues the START condition and the Device Address byte with the R/$\overline{W}$ bit set to “0”, receives an acknowledge, then issues the Register Address byte. After acknowledging receipt of the register address byte, the master immediately issues another START condition and the Device Address byte with the R/$\overline{W}$ bit set to “1”. This is followed by an acknowledge from the device and then by the 8-bit data word. The master terminates the read operation by not responding with an acknowledge and then issuing a stop condition (refer to Figure 20).

BURST READ

Burst read operation is identical to the Byte Read operation. After the first Data byte is transmitted, the master responds with an acknowledge, indicating it requires additional data. The device continues to output data for each acknowledge received.

The master terminates the read operation by not responding with an acknowledge but issuing a STOP condition (refer to Figure 21).

For more information about the I^2C standard, please consult the Philips™ I^2C specification documents.

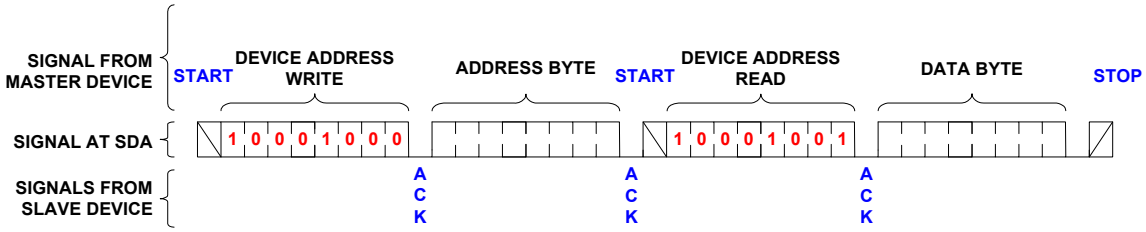


FIGURE 20. BYTE ADDRESS READ SEQUENCE

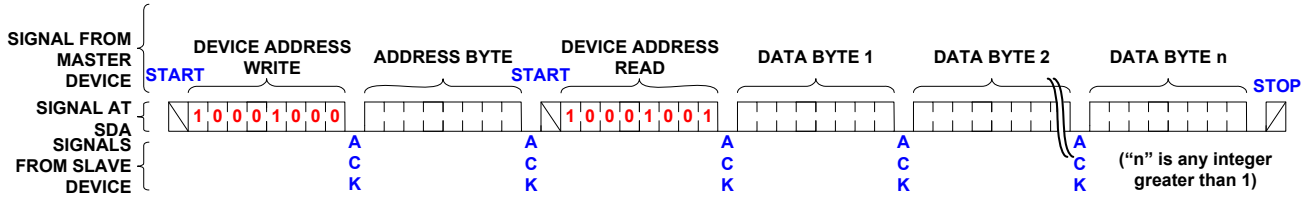


FIGURE 21. BURST READ SEQUENCE

Register Map

Following are detailed descriptions of the control registers related to the operation of the ISL29044A ambient light sensor device. These registers are accessed by the I^2C serial interface. For details on the I^2C interface, refer to “Serial Interface” on page 9.

All the functionalities of the device are controlled by the registers. The ADC data can also be read. The following sections explain the details of each register bit. All RESERVED bits must be set to zero, unless otherwise specified.

Register Descriptions

TABLE 1. ISL29044A REGISTERS AND REGISTER BITS

ADDR	REG NAME	BIT								
		7	6	5	4	3	2	1	0	DEFAULT
0x00	ChipID	1	0	1	1	1	0	Reserved	Reserved	0x2E
0x01	CONFIGURE	PROX EN	PROX_SLP[2:0]			PROX_DR	ALS_EN	ALS_RANGE	ALSIR_MODE	0x00
0x02	INTERRUPT	PROX_FLAG	PROX_PRST[1:0]		(Write 0)	ALS_FLAG	ALS_PRST[1:0]		INT_CTRL	0x00
0x03	PROX_LT	PROX_LT[7:0]								0x00
0x04	PROX_HT	PROX_HT[7:0]								0xFF
0x05	ALSIR_TH1	ALSIR_LT[7:0]								0x00
0x06	ALSIR_TH2	ALSIR_HT[3:0]				ALSIR_LT[11:8]				0xF0
0x07	ALSIR_TH3	ALSIR_HT[11:4]								0xFF
0x08	PROX_DATA	PROX_DATA[7:0]								0x00
0x09	ALSIR_DT1	ALSIR_DATA[7:0]								0x00
0x0A	ALSIR_DT2	(Unused)				ALSIR_DATA[11:8]				0x00

Register (Address: 0x00)

TABLE 2. ChipID REGISTER ADDRESS

NAME	Access	Reg. Addr (Hex)	Register Bits								DFLT (Hex)
			B7	B6	B5	B4	B3	B2	B1	B0	
ChipID	RO	0x00	1	0	1	1	1	0	Reserved	Reserved	0x2E

This is a reserved register. Do not write or read.

Configure Register (Address: 0x01)

TABLE 3. CONFIGURE REGISTER ADDRESS

NAME	Access	Reg. Addr (Hex)	Register Bits								DFLT (Hex)
			B7	B6	B5	B4	B3	B2	B1	B0	
Configure	RW	0x01	PROX_EN	PROX_S2	PROX_S1	PROX_X0	PROX_DR	ALS/IR_EN	ALS_RANGE	ALS/IR data	0x00

The Configure register consists all of control bits for both ALS Sensing and Proximity Sensing. This register determines operation mode. The register has one Enable Prox sensing bit, three Proximity Sleep mode bits, one proximity current driver bit, one Enable ALS/IR sensing bit, one ALS/IR range bit, and one ALS/IR sensing data bits. The default register value is 0x00 at power on.

ALS/IR DATA BIT [B0]

The ALS/IR data mode bit is a select mode for fetching data from the data register (reg 0x09 and reg 0x0A). If B0 is set to 0, the ALS/IR data register will contain visible spectrum ALS sensing data. If B0 is set to 1, the ALS/IR data register will contain IR spectrum sensing data.

TABLE 4. ALS/IR DATA BIT

BIT 0	OPERATION
0	Visible Spectrum ALS sensing data
1	IR Spectrum sensing data

FULL SCALE RANGE [B1]

The Full Scale Range (FSR) has two selectable ranges. Each range has a maximum allowable lux value. The higher the range value, the better the resolution and the wider the ALS lux value.

TABLE 5. RANGE REGISTER BITS

BIT1	RANGE(k)	FSR (LUX) @ VISIBLE ALS SENSING
0	Range1	200
1	Range2	3200

ALS/IR_EN [B2]

The ALS/IR_EN bit[B2] is the enable bit for both ALS sensing and IR sensing. If [B2] is 0, ALS sensing an IR sensing is disabled. If [B2] is 1, ALS sensing and IR sensing is enabled.

TABLE 6. RANGE REGISTER BITS

BIT 0	OPERATION
0	Disable ALS sensing and IR sensing
1	Enable ALS sensing and IR sensing

PROX_DR[B3]

PROX_DR bit[B3] selects the IR driver current strength. The IR driver sinks current through the LDR pin. The drive capability can be programmed through [B3] either a pulse 110mA current sink or 220mA pulse current sink. The higher the amplitude, the better the range of detection.

TABLE 7. CURRENT DRIVER REGISTER BITS

BIT 0	OPERATION
0	110mA current sink
1	220mA current sink

PROX SLEEP MODE [B6,B5,B4]

ISL29044A is equipped with multiple sleep modes in proximity sensing. It is a good power saving feature. The different sleep modes can be selected by setting [B6-B4] bits on register 0x01. When proximity sensing is enabled, the ADC converts for 0.54ms and sleeps for 800ms by default.

Table 8 lists the possible operating sleep modes.

TABLE 8. SLEEP MODES BITS

B6	B5	B4	SLEEP TIME OPERATION (ms)
0	0	0	800 (Default)
0	0	1	400
0	1	0	200
0	1	1	100
1	0	0	75
1	0	1	50
1	1	0	12.5
1	1	1	0.0 (Sleep Mode Disabled)

PROX_EN[B7].

Proximity is enabled when PROX_EN[B7] is set to high.

TABLE 9. EN_PROXIMITY REGISTER BITS

BIT 0	CURRENT DRIVER OPERATION
0	Disable proximity sensing (Default)
1	Enable proximity sensing

Interrupt Register (Address: 0x02)

TABLE 10. INTERRUP REGISTER ADDRESS

NAME	Access	Reg. Addr (Hex)	REGISTER BITS								DFLT (Hex)
			B7	B6	B5	B4	B3	B2	B1	B0	
INTERRUPT	RW	0x02	PROX_ FLAG	PROX_ PRST1	PROX_ PRST0	0	ALS/IR _FLAG	ALS/IR _PRST 1	ALS/IR _PRSST 0	INT_CTRL	0x00

The Interrupt register consists of all status bits. The ISL29044A has an interrupt scheme designed for both ALS/IR sensing and Proximity logic detection sensing. The register has one proximity sensing flag bit, two proximity sensing persistent bits, one ALS/IR sensing flag bit and two ALS/IR persistent bits. The default register value is 0x00.

INT_CTRL[B0]

INT_CTRL [B0] can be programmed to cause an interrupt when either ALS_FLAG or PROX_FLAG go high or when both go high. Writing ‘0’ will do a logical OR and a one will do a logical AND. The $\overline{INT}$ pin is open-drain therefore, in this INT_CTRL bit, there are two options to make the $\overline{INT}$ pin go low. Once the interrupt is triggered, the $\overline{INT}$ pin goes low if the PROX_FLAG bit or ALS_FLAG goes high in logic OR option. Otherwise, the interrupt is triggered and the $\overline{INT}$ pin goes low if the PROX_FLAG bit and ALS_FLAG go high in logic AND option. Both the $\overline{INT}$ pin and these interrupt status bits are automatically cleared when writing ‘0’ to those flag bits. Table 11 shows interrupt control bits.

TABLE 11. INTERRUPT CONTROL REGISTER BITS

BIT 0	OPERATION
0	Logical OR
1	Logical AND

ALS/IR INTERRUPT PERSIST BITS [B2,B1]

The interrupt persist bits[B2LOL, B1] provide control when interrupts occur. There are four different selections for this feature. A value of *N* (where *N* is 1, 4, 8, and 16) results in an interrupt only if the value remains outside the threshold window for *N* consecutive integration cycles. For example, if *N* is equal to 8 and the integration time is 100ms. An interrupt is generated whenever the last conversion results in a value outside of the programmed threshold window. Table 12 lists the possible interrupt persist bits.

TABLE 12. INTERRUPT PERSIST BITS

B2	B1	NUMBER OF INTEGRATION CYCLES (n)
0	0	1
0	1	4
1	0	8
1	1	16

ALS_FLAG BIT [B3]

The ALS_FLAG[B3] bit is a status bit for light intensity detection. The bit is set to logic HIGH when the light intensity results at (reg 0x09, 0x0A), crosses the interrupt threshold's window (register address 0x05 - 0x07), and is set to logic LOW when it is within the interrupt threshold's window. Once the interrupt is triggered, the ALS_FLAG bit goes HIGH. The ALS/IR_FLAG bit is cleared by writing '0' to [B3]. Table 13 shows the interrupt flag states.

TABLE 13. INTERRUPT FLAG BIT

BIT 3	OPERATION
0	Interrupt is cleared or not triggered yet
1	Interrupt is triggered

PROXIMITY INTERRUPT PERSIST BITS [B6,B5]

The interrupt persist bits provide control over when interrupts occur. There are four different selections for this feature. A value of N (where N is 1, 4, 8, and 16) results in an interrupt only if the value remains above the PROX_HT (reg0x04) threshold for N consecutive integration. At that moment, the PROX_FLAG is high and remains asserted until cleared by writing the '0' to PROX_FLAG bit or if the value is below PROX_LT (reg0x03) threshold for N consecutive integration, it will also clear the PROX_FLAG.

For example, if N is equal to 8, then an interrupt is generated whenever the last conversion results in a value above the PROX_HT threshold, then PROX_FLAG = 1. There are two ways of clearing the PROX_FLAG. You can write a 0h to Reg0x02 to manually clear the flag, or if the conversion results are less than the PROX_LT value, upon completion of the measurement, the Reg0x02 will be set to 0h and thus, the PROX_FLAG will be automatically cleared.

TABLE 14. PROXIMITY LOGIC PERSIST BITS

B2	B1	NUMBER OF INTEGRATION CYCLES (n)
0	0	1
0	1	4
1	0	8
1	1	16

PROX_FLAG BIT [B7]

PROX_FLAG bit [B7] is a status bit for IR light intensity detection. [B7] is set to logic HIGH when the IR light intensity reflected from the object to the sensor (reg 0x08) crosses the PROX_HT (register address 0x04), and if [B7] is set to logic LOW when the IR light intensity goes lower than PROX_LT (register address 0x03) or to clear by writing '0' to PROX_FLAG. Table 15 shows the interrupt flag states.

TABLE 15. INTERRUPT FLAG BIT

BIT 3	OPERATION
0	Logic Low (Far)
1	Logic High (Near)

PROX_TL Registers (Address: 0x03)

TABLE 16. PROX_TL REGISTER BITS

NAME	Access	Reg. Addr (Hex)	REGISTER BITS								DFLT (Hex)
			B7	B6	B5	B4	B3	B2	B1	B0	
PROX_TL	RW	0x03	TL7	TL6	TL5	TL4	TL3	TL2	TL1	TL0	0x00

The lower interrupt threshold registers are used to set the lower trigger point for interrupt generation. If the Prox value crosses below or is equal to the lower threshold, it will clear the last state of Interrupt. For example, if PROX_FLAG is high at the last state, then the proximity value is below the PROX_LT threshold and the PROX_FLAG will go low at this moment. The register defaults to 0x00 on power-up.

PROX_TH Registers (Address: 0x04)

TABLE 17. PROX_TH REGISTER BITS

NAME	Access	Reg. Addr (Hex)	REGISTER BITS								DFLT (Hex)
			B7	B6	B5	B4	B3	B2	B1	B0	
PROX_TH	RW	0x04	TH7	TH6	TH5	TH4	TH3	TH2	TH1	TH0	0xFF

The upper proximity threshold registers are used to set the upper trigger point for Logic HIGH (Near). If the Prox value crosses above or is equal to the upper threshold, a Logic HIGH (Far) is asserted on the interrupt flag. Registers PROX_HT(0x04) are set to upper threshold. 0x04 register is defaulted to 0xFF on power-up.

ALS_TH1 and ALS_TH2 Registers (Address: 0x05 and 0x06[B3,B2,B1,B0])

TABLE 18. INTERRUPT THRESHOLD LOW REGISTER BITS

NAME	Access	Reg. Addr (Hex)	REGISTER BITS								DFLT (Hex)
			B7	B6	B5	B4	B3	B2	B1	B0	
ALS_TH2_MSB	RW	0x06					TL3	TL2	TL1	TL0	0x00
ALS_TH1_LSB	RW	0x05	TL7	TL6	TL5	TL4	TL3	TL2	TL1	TL0	0x00

The lower interrupt threshold registers are used to set the lower trigger point for interrupt generation. If the ALS value crosses below or is equal to the lower threshold, an interrupt is asserted on the interrupt flag. An 8-bit RW Register ALS_TH1(0x05) and a nibble ALS_TH2(0x06[B3,B2,B1,B0]) provides the low and high bytes, respectively, of the lower interrupt threshold. The high and low bytes from each set of registers are combined to form a 12-bit threshold value. The interrupt threshold registers default to 0x00 on power-up.

ALS_TH2 and ALS_TH3 Registers (Address: 0x06[B7,B6,B5,B4] and 0X07)

TABLE 19. INTERRUPT THRESHOLD HIGH REGISTER BITS

NAME	Access	Reg. Addr (Hex)	REGISTER BITS								DFLT (Hex)
			B7	B6	B5	B4	B3	B2	B1	B0	
ALS_TH2_LSB	RW	0x06	TH7	TH6	TH5	TH4					0xF0
ALS_TH3_MSB	RW	0x07	TH7	TH6	TH5	TH4	TH3	TH2	TH1	TH0	0xFF

The upper interrupt threshold registers are used to set the upper trigger point for interrupt generation. If the ALS value crosses above or is equal to the upper threshold, an interrupt is asserted on the interrupt pin and the interrupt flag. A nibble RW Register ALS_TH(0x06[B7,B6,B5,B4]) and an 8-bit RW ALS_TH3(0x07) provides the low and high bytes, respectively, of the upper interrupt threshold. The high and low bytes from each set of registers are combined to form a 12-bit threshold value. The interrupt threshold registers default to 0xFF on power-up.

Data Registers (Addresses: 0x08)

TABLE 20. ADC REGISTER BITS

NAME	ACCESS	REG. ADDR (HEX)	Register Bits								DFLT (Hex)
			B7	B6	B5	B4	B3	B2	B1	B0	
DATA	RO	0x08	D7	D6	D5	D4	D3	D2	D1	D0	0x00

The ISL29044A has 8-bit read-only registers to hold the ADC value. The registers are refreshed after every conversion cycle. The default register value is 0x00 at power on.

Data Registers (Addresses: 0x09 and 0x0A)

TABLE 21. ADC REGISTER BITS

NAME	Access	Reg. Addr (Hex)	Register Bits								DFLT (Hex)
			B7	B6	B5	B4	B3	B2	B1	B0	
$DATA_{LSB}$	RO	0x09	D7	D6	D5	D4	D3	D2	D1	D0	0x00
$DATA_{MSB}$	RO	0x0A					D11	D10	D9	D8	0x00

The ISL29044A has one 8-bit read-only register to hold the lower, and one nibble (4-bit read only) to hold the upper of the ADC value. The nibble (4-bit read only) is accessed at address 0x0A and the lower byte is accessed at address 0x09. For a 12-bit resolution, the data is from D0 to D11. The registers are refreshed after every conversion cycle. The default register value is 0x00 at power on.

Applications Information

Calculating Lux

The ISL29044A's ADC output codes are directly proportional to lux when in ALS mode (see ALSIR_MODE bit).

$$E_{calc} = \alpha_{RANGE} \times OUT_{ADC} \quad \text{(EQ. 2)}$$

In Equation 2, E_{calc} is the calculated lux reading and *OUT* represents the ADC code. The constant α to plug in is determined by the range bit ALS_RANGE (register 0x1 bit 1) and is independent of the light source type.

TABLE 22. ALS SENSITIVITY AT DIFFERENT RANGES

ALS_RANGE	α_{RANGE} (Lux/Count)
0	0.0488
1	0.7814

Table 22 shows two different scale factors: one for the low range (ALS_RANGE = 0) and the other for the high range (ALS_RANGE = 1).

Noise Rejection

Charge balancing ADC's have excellent noise-rejection characteristics for periodic noise sources whose frequency is an integer multiple of the conversion rate. For instance, a 60Hz AC unwanted signal's sum from 0ms to k*16.66ms (k = 1,2...ki) is zero. Similarly, setting the device's integration time to be an integer multiple of the periodic noise signal greatly improves the light sensor output signal in the presence of noise. Since wall sockets may output at 60Hz or 50Hz, our integration time is 100ms: the lowest common integer number of cycles for both frequencies.

Proximity Detection of Various Objects

Proximity sensing relies on the amount of IR reflected back from objects. A perfectly black object would absorb all light and reflect no photons. The ISL29044A is sensitive enough to detect black ESD foam, which reflects only 1% of IR. For biological objects, blonde hair reflects more than brown hair and customers may notice that skin tissue is much more reflective than hair. IR penetrates into the skin and is reflected or scattered back from within. As a result, the proximity count peaks at contact and monotonically decreases as skin moves away. The reflective characteristics of skin are very different from that of paper.

Soldering Considerations

Convection heating is recommended for reflow soldering; direct-infrared heating is not recommended. The plastic ODFN package requires a custom reflow soldering profile pursuant to Figure 4 in TB487 (*Surface Mount Assembly Guidelines for Optical Co-Package Sensor and LED*).

Suggested PCB Footprint

It is important that users check the “Surface Mount Assembly Guidelines for Optical Dual FlatPack No Lead (ODFN) Package” before starting ODFN product board mounting. However, this device requires a special solder reflow profile as mentioned in Figure 4 in TB487 (*Surface Mount Assembly Guidelines for Optical Co-Package Sensor and LED*).

Layout Considerations

The ISL29044A is relatively insensitive to layout. Like other I^2C devices, it is intended to provide excellent performance even in significantly noisy environments. There are only a few considerations that will ensure best performance.

Route the supply and I^2C traces as far as possible from all sources of noise. 0.1µF and 1µF power supply decoupling capacitors need to be placed close to the device.

Typical Circuit

A typical application for the ISL29044A is shown in Figure 22. The ISL29044A's I^2C address is internally hardwired as 0b1000100. The device can be tied onto a system's I^2C bus together with other I^2C compliant devices.

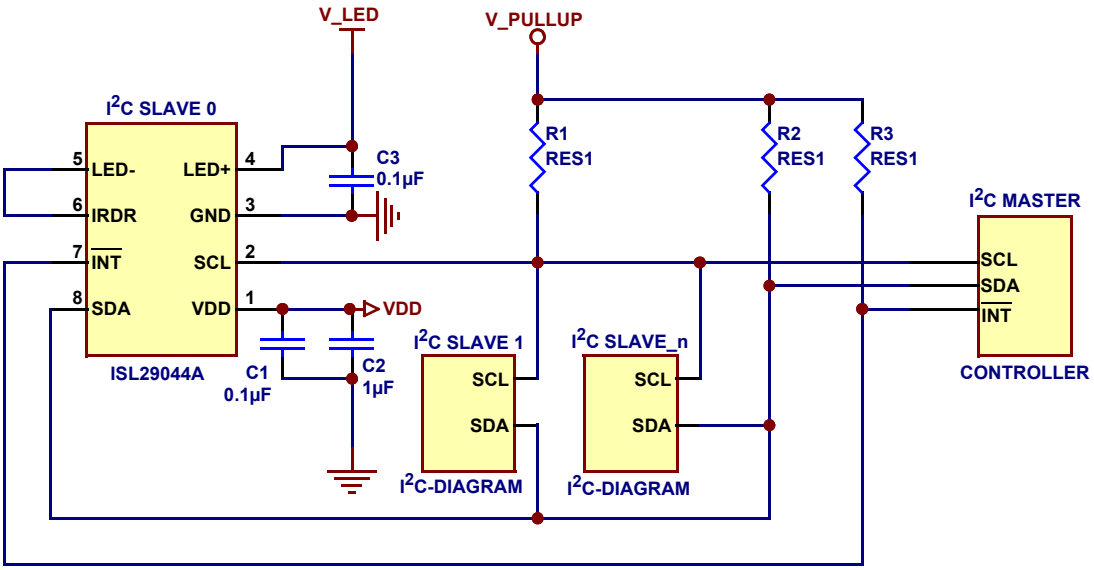


FIGURE 22. ISL29044A TYPICAL CIRCUIT

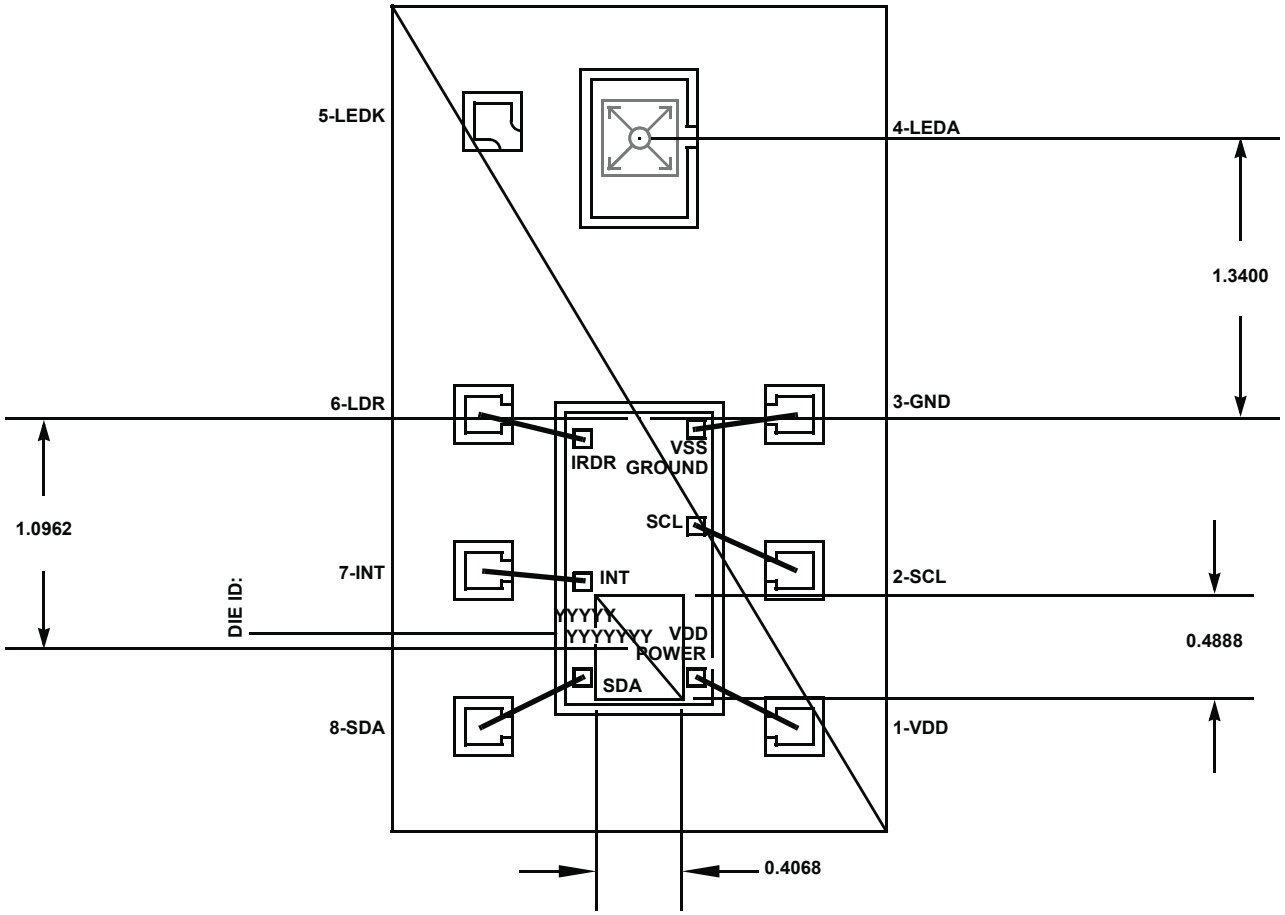


FIGURE 23. OPTICAL SENSOR LOCATION

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
April 28, 2016	FN8419.3	Added Related Literature section.
April 21, 2016	FN8419.2	Removed Related Literature section.
April 19, 2013	FN8419.1	Initial release.

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

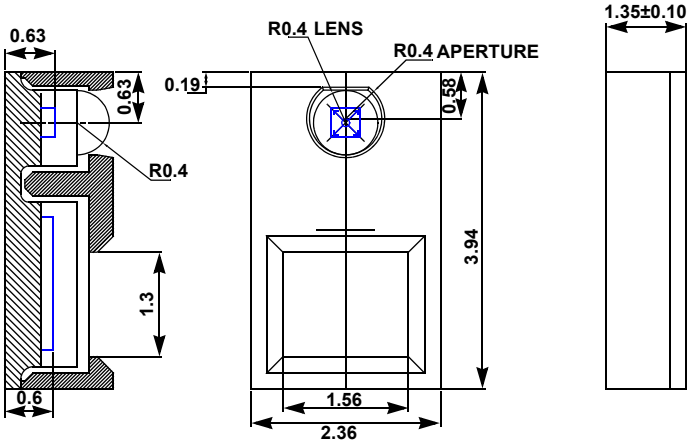
Reliability reports are also available from our website at www.intersil.com/support.

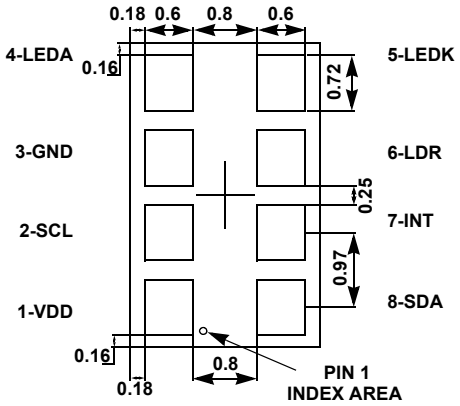
Package Outline Drawing

L8.2.36x3.94

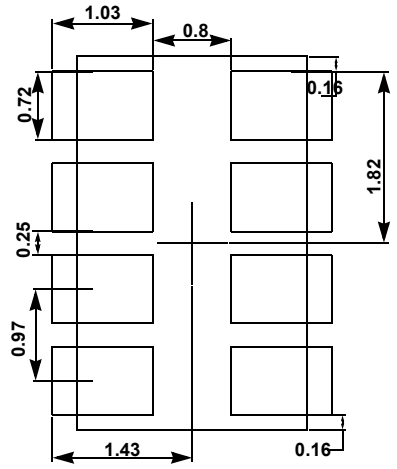
8 LEAD OPTICAL CO-PACKAGE

Rev 1, 4/13

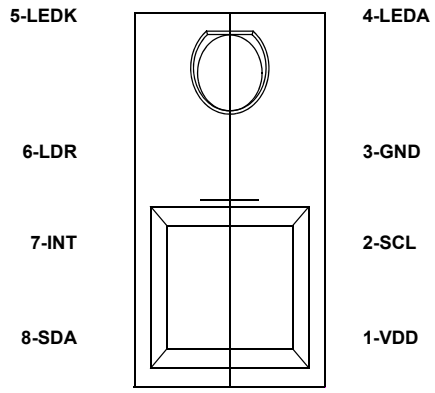




BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



TOP VIEW

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ± 0.05
4. Pin #1 identifier is a laser-etched dot on bottom surface.