ISL45041

TFT-LCD I2C Programmable VCOM Calibrator

FN6189
Rev 6.00
Apr 22, 2016

The V_{COM} voltage of an LCD panel needs to be adjusted to remove flicker. The ISL45041 part provides a digital interface to control the sink current output that attaches to an external voltage divider. The increase in output sink current lowers the voltage on the external divider, which is applied to an external V_{COM} buffer amplifier. The desired V_{COM} setting is loaded from an external source via a standard 2-wire I^2C serial interface. At power-up, the part automatically comes up at the last programmed EEPROM setting.

An external resistor attaches to the SET pin and sets the full-scale sink current that determines the lowest voltage of the external voltage divider.

The ISL45041 is available in an 8 Ld 3mmx3mm TDFN package with a maximum thickness of 0.8mm for ultra thin LCD panel design.

An evaluation kit complete with software to control the DCP from a computer is available. Reference Application Note AN1275 and "Ordering Information" on page 2.

Features

- 128-step adjustable sink current output
- 2.25V to 3.6V logic supply voltage operating range (2.6V minimum programming voltage)
- 4.5V to 18V analog supply voltage operating range (10.8V minimum programming voltage)
- I^2C interface with addresses 100111x and 100110x
- On-chip 7-Bit EEPROM
- Output adjustment SET pin
- Output guaranteed monotonic over-temperature
- Thin 8 Ld 3mmx3mm DFN (0.8mm max)
- Pb-free (RoHS compliant)

Applications

- LCD panels

Related Literature

- AN1208 "LCD screens don't flicker - or do they?"
- AN1275, "ISL45041EVAL1Z User's Manual"

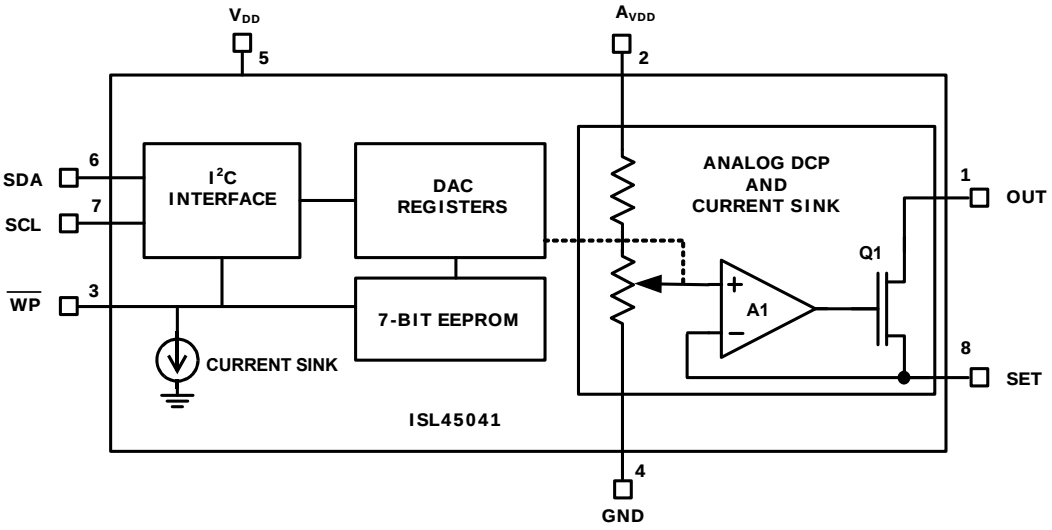
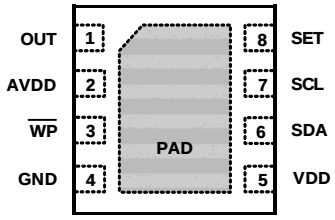


FIGURE 1. BLOCK DIAGRAM

Pin Configuration

ISL45041
(8 LD TDFN)
TOP VIEW



Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	PULL U/D	FUNCTION
1	OUT	Output		Adjustable Sink Current Output Pin. The current that sinks into the OUT pin is equal to the DAC setting times the maximum adjustable sink current divided by 128. See SET pin function description for the maximum adjustable sink current setting.
2	AVDD	Supply		High-Voltage Analog Supply. Bypass to GND with 0.1µF capacitor.
3	$\overline{WP}$	Input	Pull-Down	Write Protect. Active Low. To enable programming, connect to 0.7*V_{DD} supply or greater. The $\overline{WP}$ pin is designed for static control. It has an internal pull-down current sink. To avoid the possibly overwriting the EEPROM contents, no frequency above 1Hz should be applied to this input. Care should be taken to avoid any glitches on the input. When removing or applying mechanical jumpers, always ensure the V_{DD} power is off. A high to low transition on the $\overline{WP}$ pin results in the register contents being loaded with EEPROM data.
4	GND	Supply		Ground connection
5	VDD	Supply		Digital power supply input. Bypass to GND with 0.1µF capacitor.
6	SDA	In/Out		I^2C Serial Data Input and Output
7	SCL	Input		I^2C Clock Input
8	SET	Analog		Maximum Sink Current Adjustment Point. Connect a resistor from SET to GND to set the maximum adjustable sink current of the OUT pin. The maximum adjustable sink current is equal to (AV_{DD}/20) divided by RSET.
	Pad	Power		Thermal pad. Electrically connected to GND. Connect to ground plane on PCB to maximize thermal performance.

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL45041IRZ	041Z	0 to +85	8 Ld 3x3 TDFN	L8.3x3A
ISL45041EVAL1Z	Evaluation Board			

NOTES:

1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL45041. For more information on MSL, please see Technical Brief TB363.

Absolute Maximum Ratings

VDD to GND . . . . . +4V
Input Voltages to GND
SET . . . . . -0.3V to +4V
AVDD . . . . . -0.3V to +20V
Output Voltages to GND
OUT . . . . . -0.3V to +A_{VDD}
ESD Rating
Human Body Model
Device (Tested per JESD22-A114E) 2kV
Input Pins (SCL, SDA) (Tested per JESD22-A114E) 4kV

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Ld TDFN Package (Notes 4, 5)	53	11

Moisture Sensitivity (see Technical Brief TB363)
All Packages . . . . . Level 2
Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-free reflow profile . . . . . see TB493

Operating Conditions

Temperature Range . . . . . 0°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Test Conditions: V_{DD} = 3.3V, AV_{DD} = 18V, R_{SET} = 5kΩ, R1 = 10kΩ, R2 = 10kΩ; (See Figure 2) Unless otherwise specified. Typicals are at T_A = +25°C. **Boldface limits apply across the operating temperature range, 0°C to +85°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
POWER SUPPLY CHARACTERISTICS						
V_{DD} Supply Range Supporting EEPROM Programming	V_{DD}		**2.6**		**3.6**	V
AV_{DD} Supply Range Supporting EEPROM Programming	AV_{DD}		**10.8**		**18**	V
V_{DD} Supply Range for Wide-supply Operation (not supporting EEPROM programming)	V_{DD}		**2.25**		**3.6**	V
AV_{DD} Supply Range for Wide-supply Operation (not supporting EEPROM programming)	AV_{DD}	2.6V < V_{DD} < 3.6V	**4.5**		**18**	V
		2.25V < V_{DD} < 2.6V	**4.5**		**13**	V
V_{DD} Supply Current	I_{DD}	(Note 7)			**65**	µA
AV_{DD} Supply Current	I_{AVDD}	(Note 8)			**38**	µA
DC CHARACTERISTICS						
SET Voltage Resolution	SET_{VR}		**7**	7	**7**	Bits
SET Differential Nonlinearity	SET_{DN}	Monotonic Over-temperature			±**1**	LSB
SET Zero-scale Error	SET_{ZSE}				±**3**	LSB
SET Full-scale Error	SET_{FSE}				±**8**	LSB
SET Current (R_{SET} = 24.9kΩ and AV_{DD} = 10V)	ISET	Through R_{SET} (Note 11)		20		µA
SET External Resistance	SET_{ER}	To GND, AV_{DD} = 18V	**5**		**200**	kΩ
		To GND, AV_{DD} = 4.5V	**2.25**		**45**	kΩ
		To GND, AV_{DD} = 15V, V_{DD} = 3V V_{OUT} > 2.5V (Note 12)	**1.0**		**200**	kΩ
AV_{DD} to SET Voltage Attenuation	AVDD to SET	(Note 9)		1:20		V/V
OUT Settling Time	OUT_{ST}	To ±0.5 LSB Error Band (Note 9)		8		µs
OUT Voltage Range	V_{OUT}		**V_{SET} + 0.5V**		**13**	V
SET Voltage Drift	SET_{VD}	25°C < T_A < 55°C (Note 9)		<10		mV

Electrical Specifications Test Conditions: V_{DD} = 3.3V, AV_{DD} = 18V, R_{SET} = 5kΩ, R1 = 10kΩ, R2 = 10kΩ; (See Figure 2) Unless otherwise specified. Typicals are at T_A = +25°C. **Boldface limits apply across the operating temperature range, 0°C to +85°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
SDA, SCL Input Logic High	I^2CV_{IH}		**0.7*V_{DD}**			V
SDA, SCL Input Logic Low	I^2CV_{IL}				**0.55**	V
SDA, SCL Hysteresis		(Note 9)		260		mV
SDA Output Logic High	VOH_S		**V_{DD} - 0.4**			V
SDA Output Logic Low	VOL_S	at 3mA			**0.4**	V
$\overline{WP}$ Input Logic High	V_{IH}		**0.7*V_{DD}**			V
$\overline{WP}$ Input Logic Low	V_{IL}				**0.3*V_{DD}**	V
$\overline{WP}$ Hysteresis		(Note 9)		0.14V_{DD}		V
$\overline{WP}$ Input Current	IL_{WPN}		**0.20**		**35**	µA
I^2C Timing						
SCL Clock Frequency	f_{SCL}		**0**		**400**	kHz
I^2C Clock High Time	t_{SCH}		**0.6**			µs
I^2C Clock Low Time	t_{SCL}		**1.3**			µs
I^2C Spike Rejection Filter Pulse Width	t_{DSP}		**0**		**50**	ns
I^2C Data Set Up Time	t_{SDS}		**100**			ns
I^2C Data Hold Time	t_{SDH}		**900**			ns
I^2C SDA, SCL Input Rise Time	t_{ICR}	Dependent on Load (Note 10)		20 + 0.1*Cb	**1000**	ns
I^2C SDA, SCL Input Fall Time	t_{ICF}	(Note 10)		20 + 0.1*Cb	**300**	ns
I^2C Bus Free Time Between Stop and Start	t_{BUF}		**200**			µs
I^2C Repeated Start Condition Set-up	t_{STS}		**0.6**			µs
I^2C Repeated Start Condition Hold	t_{STH}		**0.6**			µs
I^2C Stop Condition Set-up	t_{SPS}		**0.6**			µs
I^2C Bus Capacitive Load	Cb				**400**	pF
SDA Pin Capacitance	C_{SDA}				**10**	pF
SCL Pin Capacitance	C_S				**10**	pF
EEPROM Write Cycle Time	t_W				**100**	ms

NOTES:

6. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
7. I_{DD} current may increase to 2mA for 45ms or less during each EEPROM programming operation.
8. I_{AVDD} current may increase to 1mA for 30ms or less during each EEPROM programming operation.
9. Simulated and Determined via Design and NOT Directly Tested.
10. Simulated and Designed According to I^2C Specifications.
11. A typical Current of 20µA is Calculated using AV_{DD} = 10V and R_{SET} = 24.9kΩ. Reference "R_{SET} Resistor" in Figure 3.
12. Minimum value of R_{SET} resistor guaranteed when: AV_{DD} = 15V, V_{DD} = 3.0V and when voltage on the VOUT pin is greater than 2.5V. Reference Equation 2 on page 5 with Setting = 128.

Application Information

This device provides the ability to reduce the flicker of an LCD panel by adjustment of the V_{COM} voltage during production test and alignment. A 128-step resolution is provided under digital control, which adjusts the sink current of the output. The output is connected to an external voltage divider, so that the device will have the capability to reduce the voltage on the output by increasing the output sink current.

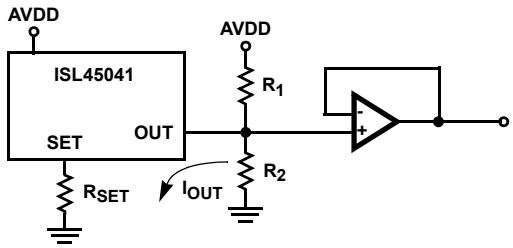


FIGURE 2. OUTPUT CONNECTION CIRCUIT EXAMPLE

The adjustment of the output is provided by the 2-wire I^2C serial interface.

Expected Output Voltage

The ISL45041 provides an output sink current, which lowers the voltage on the external voltage divider (V_{COM} output voltage). Equations 1 and 2 can be used to calculate the output current (I_{OUT}) and output voltage (V_{OUT}) values. The setting is the register value +1 with a value between 1 and 128.

$$I_{OUT} = \frac{Setting}{128} x \frac{AV_{DD}}{20(R_{SET})} \quad \text{(EQ. 1)}$$

$$V_{OUT} = \left(\frac{R_2}{R_1 + R_2}\right) AV_{DD}\left(1 - \frac{Setting}{128} x \frac{R_1}{20(R_{SET})}\right) \quad \text{(EQ. 2)}$$

Table 1 gives the calculated value of V_{OUT} using the resistor values of: R_{SET} = 24.9kΩ, R_1 = 200kΩ, R_2 = 243kΩ and AV_{DD} = 10V.

TABLE 1.

SETTING VALUE	V_{OUT} (V)
1	5.468
10	5.313
20	5.141
30	4.969
40	4.797
50	4.625
60	4.453
70	4.281
80	4.109
90	3.936
100	3.764
110	3.592
128	3.282

R_{SET} Resistor

The external R_{SET} resistor sets the full-scale sink current, I_{SET} maximum, that determines the lowest voltage of the external voltage divider R_1 and R_2 (Figure 2). The voltage difference between the OUT pin and SET pin (Figure 3), which are also the drain and source of the output transistor, must be greater than 1.75V. This will keep the output transistor in its saturation region to maintain linear operation over the full range of register values. Expected current settings and 7-bit accuracy occurs when the output MOS transistor is operating in the saturation region. Figure 3 shows the internal connection for the output MOS transistor. The value of the AV_{DD} supply sets the voltage at the source of the output transistor. This voltage is equal to (Setting/128) x (AV_{DD}/20). The I_{SET} current is therefore equal to (Setting/128) x (AV_{DD}/20 x R_{SET}). The drain voltage is calculated using Equation 2. The values of R_1 and R_2 (Equation 2) should be determined using I_{OUT} maximum (setting equal to 128) so the minimum value of V_{OUT} is greater than 1.75V + AV_{DD}/20.

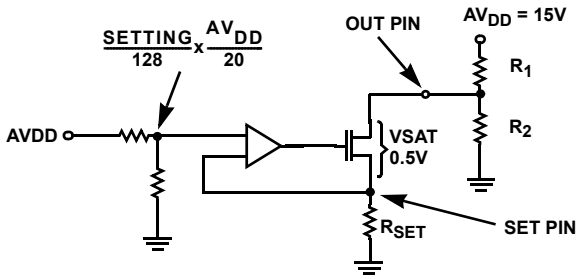


FIGURE 3. OUTPUT CONNECTION CIRCUIT EXAMPLE

Ramp-Up of the VDD Power Supply

The ramp-up from 10% V_{DD} to 90% V_{DD} level must be achieved in 10ms or less to ensure that the EEPROM and power-on-reset circuits are synchronized and the correct value is read from the EEPROM Memory.

Power Supply Sequence

The recommended power supply sequencing is shown in Figure 3. When applying power, VDD should be applied before or at the same time as AVDD. The minimum time for t_{VS} is 0µs. When removing power, the sequence of VDD and AVDD is not important.

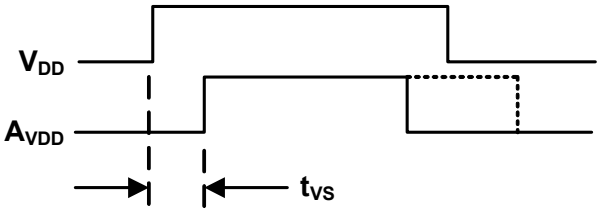


FIGURE 3. POWER SUPPLY SEQUENCE

Do not remove VDD or AVDD within 100ms of the start of the EEPROM programming cycle. Removing power before the EEPROM programming cycle is completed may result in corrupted data in the EEPROM.

I²C Bus Format

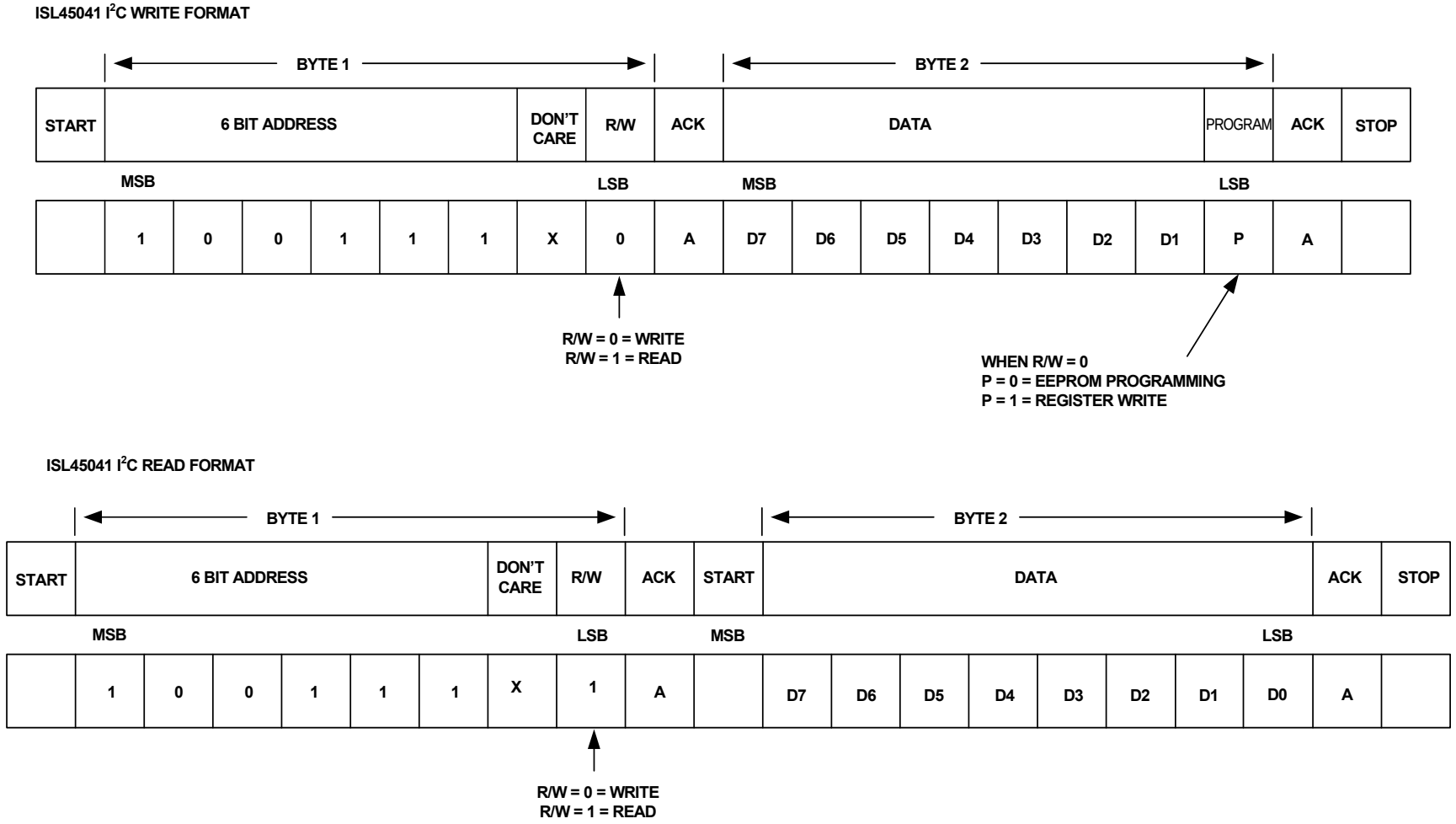


FIGURE 4. ISL45041 I²C READ AND WRITE FORMAT

I²C Addressing

The ISL45041 will respond identically to either of two I²C address: 1001110x and 1001111x. 100111x is the preferred address. To prevent bus conflicts, ensure that there are no other devices on the I²C bus with either of the above addresses.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
April 22, 2016	FN6189.6	Removed AN1244 from related literature section.
October 30, 2014	FN6189.5	Updated datasheet to Intersil's new standards. Added related Literature on page 1. Moved Block Diagram to page 1. Moved the Pin Configurations and Ordering Information to page 2. Added Pad to "Pin Descriptions" on page 2. In Table 1 on page 5, updated typo in first row (VOUT value) from "5.486" to "5.468" and added (V) units to header. Added revision history and About Intersil sections.

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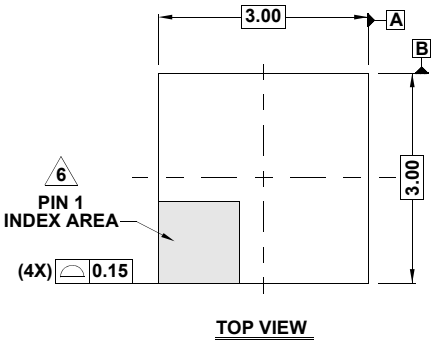
Package Outline Drawing

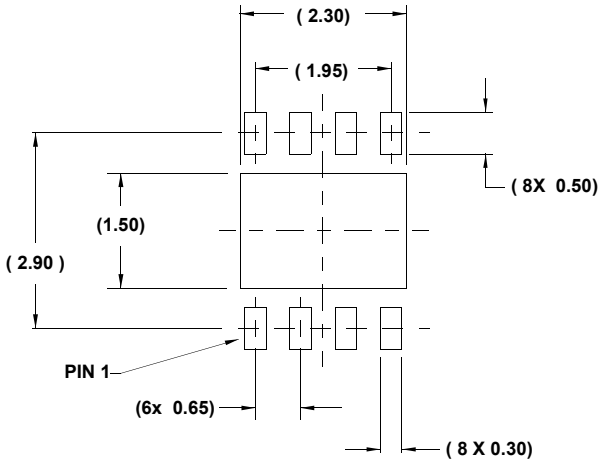
L8.3x3A

8 LEAD THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE

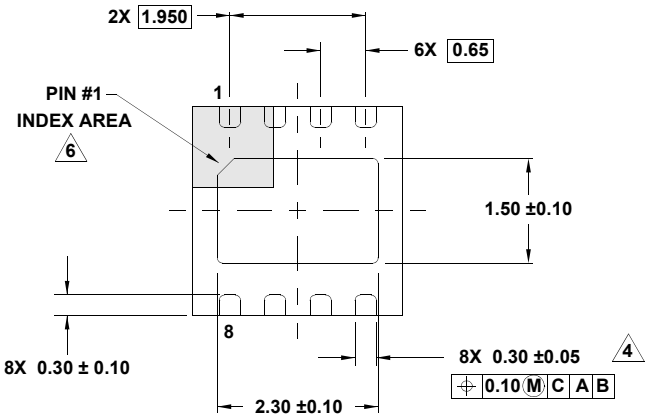
Rev 4, 2/10



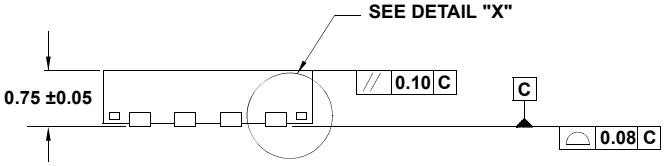
TOP VIEW



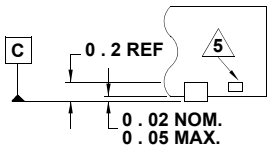
TYPICAL RECOMMENDED LAND PATTERN



BOTTOM VIEW



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.20mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Compliant to JEDEC MO-229 WEEC-2 except for the foot length.