ISL58781

Laser Diode Driver with Serial Control and Write Current DAC

FN6909
Rev 3.00
December 3, 2015

The ISL58781 is a highly integrated laser diode driver designed to support multi-standard writable optical drives in CD, DVD, and Blu-Ray at various speeds. It is a ‘hybrid’ part having an interface compatible with a conventional LDD, but an internal architecture similar to a write strategy LDD. This combination adds versatility to the conventional interface.

The rise and fall times and overshoot of the blue output are adjustable to compensate for high and low resistance lasers.

There are two banks of write currents with a bank select line, BSEL. This eliminates the need to synchronize the serial port to the media.

The oscillator can be controlled by external LVDS lines, or internally activated through program assignment to any WEN state.

The WEN lines have internal 100Ω terminators. There is a skew detector on the WEN receiver outputs.

The ISL58781 requires a single 5V supply.

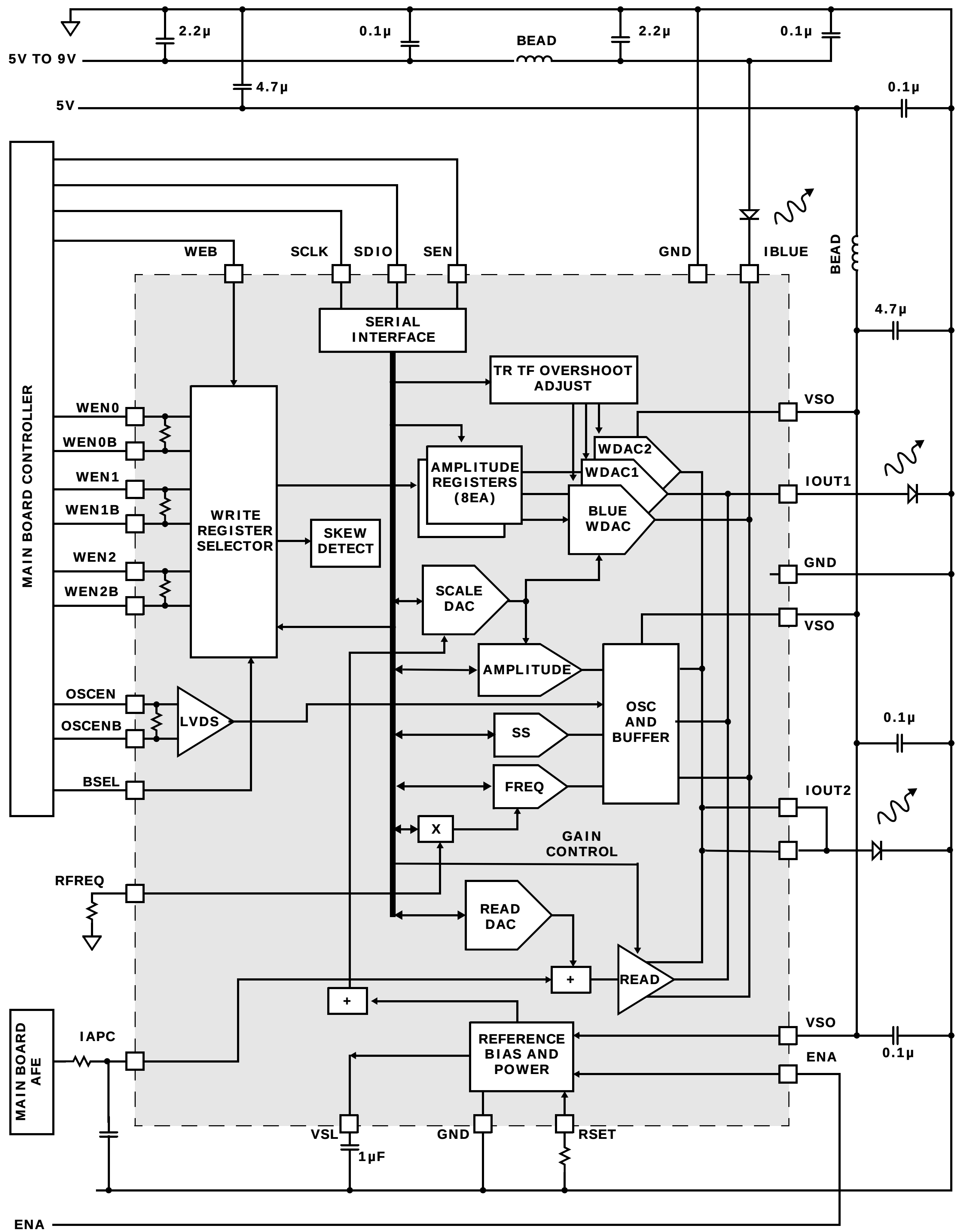
Features

- Compatible with all Conventional Controllers Having a Serial Port, with Some Programming
- Programmable Snubber on all Outputs
- Compatible with Future Controllers Having Gray Coded WEN Lines for Glitchless High-Speed Operation
- WEN Line Skew Detection
- 1000mA Maximum Total Output
- 10-bit x 10-bit Multiplying DAC Output Provides 10-bit Full Scale Adjustment and 10-bit Resolution at any Full Scale Output
- Three Laser Outputs Allow Read/Write DVD, CD, and Blue Combinations
- Analog Inputs Supports Read APC
- HFM Oscillator Programmable to $100mA_{P-P}$ and Range from 100MHz to >1GHz
- Programmable HFM On, Off and Cooling Levels
- Programmable Spread Spectrum for Low EMI
- Built-in ADC to Sample Laser Voltage Allows Power Reduction by Optimizing Headroom
- Built-in Thermal Sensor Aids in Thermal Design
- Serial Input Works up to 50MHz
- Pb-Free (RoHS Compliant)

Applications

- Combination DVD, CD, and Blue Writable Drives
- BD Camcorders
- BD Video Recorders

Application Block Diagram



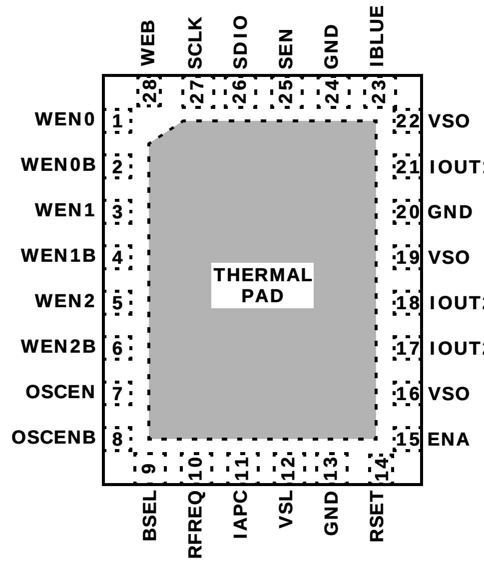
Ordering Information

PART NUMBER	PART MARKING	TEMP RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG.#
ISL58781CRZ-T13 (Notes 1, 2, 3)	58781 CRZ	-10 to +85	28 Ld QFN	L28.4x5A

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL58781. For more information on MSL please see techbrief TB363.

Pin Configuration

ISL58781
(28 LD QFN)
TOP VIEW



Pin Descriptions

PIN NAME	PIN NUMBER	I/O	PIN TYPE	PIN DESCRIPTION
WEN0, WEN0B	1, 2	I	LVDS	Write Enable 0. When WEN0 > WEN0B, the result is a logic 1 in the write current selection. Otherwise it is logic 0.
WEN1, WEN1B	3, 4	I	LVDS	Write Enable 1. When WEN1 > WEN1B, the result is a logic 1 in the write current selection. Otherwise it is logic 0.
WEN2, WEN2B	5, 6	I	LVDS	Write Enable 2. When WEN2 > WEN2B, the result is a logic 1 in the write current selection. Otherwise it is logic 0.
OSCEN, OSCENB	7, 8	I	LVDS	Oscillator Enable. When OSCEN > OSCENB, the result is a logic 1, which may be used to turn on the oscillator. When 0, the oscillator will output a DC current that is programmable.
BSEL	9	I	Digital	Bank Select input selects the write current register banks.
RFREQ	10	I/O	Analog	A resistor from RFREQ to GND sets the range of the HFM frequency.
IAPC	11	I	Analog	A 1kΩ impedance current input; 100*IAPC flow to the output. This controls the read current, which may also include a current from an internal DAC.
VSL	12	O	Power	The internal 2.5V regulator needs a 1µF capacitor from VSL to GND. Do not use VSL for other loads.
GND	13, 20		Ground	Ground
RSET	14	I/O	Analog	A resistor from RSET to analog ground calibrates the DAC full-scales
ENA	15	I	Digital	Chip enable input (H = enable, L = disable)
VSO	16, 19, 22		Power	Supply voltage for the output drivers only (connect all pins)
IOUT2	17, 18	O	Analog	Laser diode output #2
IOUT1	21	O	Analog	Laser diode output #1
IBLUE	23	O	Analog	Blue laser diode output
SEN	25	I	Digital	Serial control enable (H = enable, L = disable)
SDIO	26	I/O	Digital	Serial data for parameters and control; in/out
SCLK	27	I	Digital	Serial control clock
WEB	28	I	Digital	Write enable Bar. When low, write current is enabled.
PD			Thermal	The Thermal pad should be grounded and connected to a heat sink.

NOTE: Pins with the same name are internally connected together; however, LDD pins must not be used for connecting together external components or features.

Absolute Maximum Ratings (T_A = +25°C)

V_{SO}, Supply Voltages 6V
I_{BLUE}, Voltage at I_{BLUE} 7V
$I_{OUT1,2}$, Output Current 1000mApk
I_{BLUE}, Output Current. 600mApk
V_{IN}, Logic Input Voltages . . . . -0.5V to V_{SO} +0.5V
I_{IN}, Current into R_{SET}, R_{FREQ}, I_{APC}. 5mA
ESD Rating
Human Body Model 2500V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
28 Lead QFN (Notes 4, 5)	37	2.9

P_D, Maximum Power Dissipation . . . . .see curves on page 12
T_S, Storage Temperature Range . . . . -60°C to +150°C
Pb-Free Reflow Profile . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

T_A, Ambient Temperature Range. . . . . -10°C to +85°C
T_J, Junction Temperature Range . . . . -10°C to +150°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

Unless otherwise indicated, all of the following tables are: $V_{SO} = V_{HI}$ = 5V, R_{SET} = 620Ω, R_{FREQ} = 4.7kΩ, $R_{LOAD-IOUT1/2}$ = 8Ω to GND, $R_{LOAD-BLUE}$ = 10Ω to V_{HI}, PMAX = 0x3FF, Reg 1 21 = 88h, Reg x-00 bit6 = 0b, T_A = +25°C.

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
DC ELECTRICAL SPECIFICATIONS					
V_{SO}	(Notes 6, 7)	4.5		5.7	V
V_{IBLUE}	IBLUE pin; R_{LOAD} = 10Ω			7.0	V
I_{VSO}	Supply Current (No Current Output)		25	35	mA
I_S, $dis_{(nom)}$	Supply Current, Disable Mode		3.5	6	mA
I_S, $dis_{(high)}$	Supply Current; VSO = 5.5V, Disable Mode		3.9	7	mA
V_{SO}, good	V_{SO} Voltage above which STATUS: VDDOK = 1	2.9		3.5	V
$I_{BLUE-LEAK(SEL)}$	V_{IBLUE} = 7.0V; I_{BLUE} is selected		150	400	µA
$I_{BLUE-LEAK(DE-SEL)}$	V_{IBLUE} = 7.0V; I_{BLUE} is not selected		1.1	1.6	mA
V_{IH}	Input Logic High Level	2.0			V
V_{IL}	Input Logic Low Level			0.8	V
V_{OH}	SDIO High Level, I_L = -5mA	2.4			V
V_{OL}	SDIO Low Level, I_L = 5mA			0.4	V
I_{INH}	Logic Input Current High Level	-15		+10	µA
I_{INL}	Logic Input Current Low Level	-15		+10	µA

NOTES:

6. Required voltage at the device pins. Allowance must be made for any voltage drop between the power supply and the device.
7. Required voltage also depends on laser diode manufacturer and pickup optical efficiency. Also, see R_{OUT} spec of WDAC.

PMAX DAC (10-bit) DC Specifications

Standard conditions unless otherwise noted.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
DNL-PMAX	Differential Non-Linearity	(Note 8)	-3.5		+3.5	LSB
INL-PMAX	Integral Non-Linearity	At 200h Resistive Load ~0V to ~3V		+40		LSB
ZS-PMAX	Zero-Scale Error	(Note 9)	-2	0	+2	LSB
V_{RSET}	RSET Pin Voltage		1.03	1.06	1.11	V

NOTES:

8. Differential non-linearity (DNL) is the differential between the measured and ideal 1 LSB change of any two adjacent codes.
9. Zero-scale error (ZS) is the deviation from zero current output when the digital input code is zero.

IOUT1/2 Write Power DAC (10-bit) DC Specifications

Standard conditions unless otherwise noted.

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 14)	TYP	MAX (Note 14)	UNIT
DNL-W	Differential Non-Linearity		-1.7		+1.0	LSB
INL-W	Integral Non-Linearity	At 200h Resistive Load ~0V to ~3V		+21		LSB
FS_{OUT}-W620	Write DAC Full-Scale Output Current R_{SET} = 620Ω	WriteDAC = 0x3FF. Headroom depends on I_{OUT}. Reg 1-21 = 8F	475	500		mA
FS_{OUT}-H1.1	Write DAC Full-Scale Output Current	WriteDAC = 0x3FF, Reg 1-21 = 8F Fixed Headroom = 1.1V	700	773	875	mA
$PSRR_{-FS}$	Power Supply Rejection -Full-Scale Current	vs V_{SO} (Note 10)		-30		dB
$TC_{-FS-IOUT}$	Temperature Coefficient -Full-Scale Current	(Note 11) 0°C to +85°C		-32		ppm/°C
ZS-W	Zero-scale error	(Note 12)	-2	0	+2	LSB
R_{OUT}-WDAC	Write DAC Output Series Resistance	WriteDAC = PMAX = 0x3FF PMAX bias overdriven (Note 13)		1.1	1.4	Ω

NOTES:

10. Full scale output current power supply sensitivity (SFS) is measured by varying the V_{SO} from 4.5V to 5.5V DC and measuring the effect of this signal on the full-scale output current.
11. Full scale output current temperature coefficient (TFS) is given by delta (full scale output current)/Δ(T).
12. Zero-scale error (ZS) is the deviation from zero current output when the digital input code is zero.
13. PMAX bias overdriven via R_{SET}.
14. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

IBLUE Write Power DAC (10-bit) DC Specifications

Standard conditions unless otherwise noted.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
DNL-W	Differential Non-Linearity		-4.9		+2.0	LSB
INL-W	Integral Non-Linearity	At fixed 2.5V headroom		+60		LSB
FS_{OUT}-H2.0	Write DAC Full-Scale Output Current R_{SET} = 620Ω	WriteDAC = 0x3FF; Fixed Headroom = 2.0V; Reg 1-21 = 8F	380	445	575	mA
TR_{RANGE}	Tr Tf adjustment Range	Reg 1-0A from X0h to X7h		1		ns
$PSRR_{-FS}$	Power Supply Rejection -Full -Scale Current	vs V_{SO} (Note 15)		-40		dB
$TC_{FS\text{-}IBLUE}$	Temperature Coefficient -Full-Scale Current	(Note 16)		600		ppm/°C
ZS-W	Zero-Scale Error	V_{IOUT} = 2V (Note 17)	-8	0	+8	LSB
R_{OUT}-WDAC	Write DAC Output Series Resistance	WriteDAC = PMAX = 0x3FF PMAX bias overdriven (Note 18)		2.9	4.5	Ω

NOTES:

15. Full scale output current power supply sensitivity (SFS) is measured by varying the V_{SO} from 4.5V to 5.5V DC and measuring the effect of this signal on the full-scale output current.
16. Full scale output current temperature coefficient (TFS) is given by delta (full scale output current)/Δ(T).
17. Zero-scale error (ZS) is the deviation from zero current output when the digital input code is zero.
18. PMAX bias overdriven via R_{SET}.

IBLUE Read APC Amplifier DC Specifications

Standard conditions unless otherwise noted.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
$IAPC_{MIN\text{-}GAIN}$	Current Gain @Min Gain	Reg1-21h = 1X, I_{APC} = 0µA, 500µA	8	12	22	mA/mA
$IAPC_{MAX\text{-}GAIN}$	Current Gain @ Max Gain	Reg1-21h = FX, I_{APC} = 0µA, 500µA	180	220	280	mA/mA
$IAPC_{GAIN}$	Current Gain	I_{APC} = 0µA, 500µA	80	101	150	mA/mA
$IAPC_{OS}$	Current Offset	I_{APC} = 0µA	-2	1	3	mA
LIN_{APC}	Output Current Linearity	I_{APC} = 0µA, 500µA, 1.0mA	0		6	%
I_{OUT}-R-APC	Blue Read Output Current, Using I_{APC} Input	I_{APC} = 1.5mA	150			mA
R_{IN}	I_{APC} Input Impedance to GND		800		1300	Ω
$PSRR_{APC}$	I_{APC} Current Power Supply Rejection	$I_{OUT\text{-}average}$ = 100mA, varying V_{SO}		-46		dB

OUT1/2 Read APC Amplifier DC Specifications

Standard condition unless otherwise noted.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
$IAPC_{MIN\text{-}GAIN}$	Current Gain @ Min Gain	Reg1-21h = 1X, I_{APC} = 0µA, 500µA	10.5	14	17.5	mA/mA
$IAPC_{MAX\text{-}GAIN}$	Current Gain @ Max Gain	Reg1-21h = FX, I_{APC} = 0µA, 500µA	145	163	185	mA/mA
$IAPC_{GAIN}$	Current Gain	I_{APC} = 0µA, 500µA	82	92	108	mA/mA
$IAPC_{OS}$	Current Offset	I_{APC} = 0µA	-2	1	3	mA
LIN_{APC}	Output Current Linearity	I_{APC} = 0µA, 500µA, 1.0mA	0		6	%
I_{OUT}-R-APC	Read Output Current, Using I_{APC} Input	I_{APC} = 1.5mA	120			mA
R_{IN}	I_{APC} Input Impedance to GND		800		1300	Ω
$PSRR_{APC}$	I_{APC} Current Power Supply Rejection	$I_{APC\text{-}IN}$ = 0.45mA, varying V_{SO}		-48		dB

Read DAC (12-bit) DC Specifications

Standard conditions unless otherwise noted.

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 22)	TYP	MAX (Note 22)	UNIT
DNL-R	Read DAC Differential Non-Linearity	PREAD: Reg 0-19 + Reg 1-09	-2		+2	LSB
INL-R	Read DAC Integral Non-Linearity	@ 900h on Resistive Load. 0V to ~3V		+90		LSB
I_{OUT}-R-DAC-RED	Read Output Current, Read DAC at Full-Scale, I_{OUT1} or I_{OUT2}	PREAD = 0xFFF, I_{APC} = 0, Reg 1-21 = 8F	110	130	170	mA
$PSRR_{-FS}$	Power Supply Rejection - Ful-Scale Current	varying the V_{SO} (Note 14)		-42		dB
$TC_{-FS-IOUT}$	Temperature Coefficient - Full-Scale Current	Not including the R_{SET} tempco (Note 20) 0°C to +85°C		-48		ppm/°C
ZS-R	Zero-Scale Error	V_{IOUT} = 2V (Note 16)	-80	0	80	LSB

NOTES:

19. Full scale output current power supply sensitivity (SFS) is measured by varying the V_{SO} from 4.5V to 5.5V DC and measuring the effect of this signal on the full-scale output current.
20. Full scale output current temperature coefficient (TFS) is given by delta (full scale output current)/Δ(T).
21. Zero-scale error (ZS) is the deviation from zero current output when the digital input code is zero.
22. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

HFM (High Frequency Modulator)

Standard conditions unless otherwise noted.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
$I_{MAX-RED-OFF-LINK}$	Max HFM Off DC Output, I_{OUT1} or I_{OUT2} in Link Mode	HFMOFF = 0xFFF	90	120	160	mA
$I_{MAX-RED-OFF-UNLINK}$	Max HFM Off DC Output, I_{OUT1} or I_{OUT2} in Unlink mode	HFMOFF = 0xFFF	80	115	150	mA
$I_{MAX-BLUE-OFF}$	Max HFM Off DC Output, IBLUE	HFMOFF = 0xFFF	50	62	80	mA
$I_{MIN-RED-OFF}$	Min HFM Off DC Output, I_{OUT1} or I_{OUT2}	HFMOFF = 0x000	-3	0	3	mA
$I_{MIN-BLUE-OFF}$	Min HFM Off DC Output, I_{BLUE}	HFMOFF = 0x000	-3	0	3	mA
$I_{MAX-RED-ON-LINK}$	Max HFM Oscillator Output, I_{OUT1} or I_{OUT2} in Link Mode	HFMON = Reg 0-17h = 0xFF		118		mA_{P-P}
$I_{MAX-RED-ON-UNLINK}$	Max HFM Oscillator Output, I_{OUT1} or I_{OUT2} in Unlink Mode	HFMON = Reg 0-17h = 0xFF		114		mA_{P-P}
$I_{MAX-BLUE-ON}$	Max HFM Oscillator Output, I_{BLUE}	HFMON = 0xFF		60		mA_{P-P}
$F_{OSC-HI-MAX}$	Max HFM Frequency, High Range	Reg 0-16 = FFh, Reg X-00 bit 6 = 0	900	1020	1250	MHz
$F_{OSC-HI-MIN}$	Min HFM Frequency, High Range	Reg 0-16 = 01h, Reg X-00 bit 6 = 0	120	175	240	MHz
$F_{OSC-LO-MAX}$	Max HFM Frequency, Low Range	Reg 0-16 = FFh, Reg X-00 bit 6 =1	425	525	625	MHz
$F_{OSC-LO-MIN}$	Min HFM Frequency, Low Range	Reg 0-16 = 01h, Reg X-00 bit 6 = 1	55	78	105	MHz
$PSRR_{OSC-FREQ}$	PSRR -HFM Frequency	VSO from 4.5V to 5.0V		0.5		%/V
$PSRR_{OSC-AMP-IOUT}$	PSRR - HFM Amplitude	350MHz; HFMON = FFh; Link		3		%/V
$PSRR_{OSC-AMP-IBLUE}$	PSRR - HFM Amplitude	700MHz; HFMON = FFh; Link		1.2		%/V
$TF_{OSC400MAX}$	HFM Frequency Temperature Coefficient	Range from 200MHz to 400MHz		0 - 900		ppm/°C
$TF_{OSC900MAX}$	HFM Frequency Temperature Coefficient	Range from 400MHz to 900MHz		±250		ppm/°C
VR_{FREQ}	R_{FREQ} Pin Voltage	R_{FREQ} = 4.7kΩ	0.9	1.11	1.2	V

HFM (High Frequency Modulator) Standard conditions unless otherwise noted. (Continued)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
$SS_{-WIDTH-RANGE}$	Spread Spectrum Spreading Width Adjustment Range	R_{FREQ} = 4.7kΩ, Reg 1-18 = 10h, Reg 0-16 = 26h; Reg X-00 bit 6 = 0	0.1	0.525	1.1	%
SS_Shift	Shift of Center Frequency when SS is Enabled vs when it's Disabled	R_{FREQ} = 4.7kΩ, Reg 1-18-00h to 30h, Reg 0-16 = 26h; Reg X-00 bit 6 = 0		0.7		%
SS_Mod	Spread Spectrum Modulation Frequency	REG 1-18h Bit 7 = 0; Reg X-00 bit 6 = 0	30	53	80	kHz
SS_Mod	Spread Spectrum Modulation Frequency	REG 1-18h Bit 7 = 1; Reg X-00 bit 6 = 0	15	34	55	kHz

Serial Interface AC Performance Standard conditions unless otherwise noted.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
F_{SER}	SCLK Operating Range	Static logic not limited at low frequency			50	MHz
t_{EH}	SEN "H" Time	@ 50MHz	320			ns
t_{EL}	SEN "L" Time	@ 50MHz	160			ns
t_{ERSR}	SEN Rising Edge to the First SCLK Rising Edge	@ 50MHz	10			ns
t_{CDS}	SDIO Set Up Time	@ 50MHz		10		ns
t_{CDH}	SDIO Hold Time	@ 50MHz		10		ns
t_{SREF}	Last SCLK Rising Edge to SEN Falling Edge	@ 50MHz	10			ns
t_{CC}	SCLK Cycle Time1	@ 50MHz	20			ns
Duty	SCLK "H" Duty Cycle	@ 50MHz	40	50	60	%
t_{CDD}	SDIO Output Delay	@ 50MHz			4	ns
t_{EDH}	SDIO Output Hold Time	@ 50MHz	2			ns

LVDS Specifications Standard conditions unless otherwise noted.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IN-HIGH}$	Maximum Single Line Voltage			2.4		V
V_{IN-LOW}	Minimum Single Line Voltage			0		V
C_{IN}	Input Capacitance			2		pF
R_{IN}	Input Resistance		85	100	115	Ω
V_{MIN}	Minimum Differential Voltage	Signal tested with ±240mV differential input	240			mV_{PK}

Laser Driver AC Performance

Demoboard test, 10% duty cycle pulse, load = equivalent circuitry to [laser + flex cable] and/or as noted. V_{SO} = 5V. T_A = +25°C

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
$t_{R\text{-}IOUTx}$	$I_{OUT1/2}$ Write Rise Time (10% to 90%)	300mW Optical ML229U7 (Note 23)		1.3		ns
$t_{F\text{-}IOUTx}$	$I_{OUT1/2}$ Write Fall Time (10% to 90%)	300mW Optical ML229U7 (Note 23)		800		ps
$O/S_{\text{-}IOUTx}$	$I_{OUT1/2}$ Write Pulse Overshoot	300mW Optical ML229U7 (Note 23)		11		%
$t_{D\text{-}IOUTx}$	$I_{OUT1/2}$ Write Pulse Delay From LVDS = Zero crossing to I_{OUT} rise 10%	(Note 23)		5.3		ns
$t_{R\text{-}BLUE}$	I_{BLUE} Write Rise Time (10% to 90%)	250mW Optical (Note 23)		600		ps
$t_{F\text{-}BLUE}$	I_{BLUE} Write Fall Time (10% to 90%)	250mW Optical (Note 23)		450		ps
$O/S_{\text{-}BLUE}$	I_{BLUE} Write Pulse Overshoot	250mW Rising Optical (Note 23)		6		%
$t_{D\text{-}BLUE}$	I_{BLUE} Write Pulse Delay From LVDS = Zero crossing to I_{OUT} rise 10%	(Note 23)		5.2		ns
$I_{NOISE}\text{-}I_{OUTx}$	$I_{OUT1/2}$ Read Output Current Noise	I_{OUT} = 50mA, measured @ 10MHz		0.55		nA/√Hz
$I_{NOISE}\text{-}I_{OUTx}$	$I_{OUT1/2}$ Read & HFM Output Current Noise	I_{OUT} = 50mA+30mA$_{P\text{-}P}$; Measured @ 10MHz		0.96		nA/√Hz
$I_{NOISE\text{-}BLUE}$	I_{BLUE} Read Output Current Noise	I_{OUT} = 50mA, measured @ 10MHz		0.37		nA/√Hz
$I_{NOISE\text{-}BLUE}$	I_{BLUE} Read & HFM Output Current Noise	I_{OUT} = 50mA+10mA$_{P\text{-}P}$; Measured @ 10MHz		0.47		nA/√Hz
BW_{APC}	Read Amplifier 3dB Bandwidth	I_{OUT} = 50mA		0.5		MHz

NOTE:

23. Limits established by characterization and are not production tested

TABLE 1. AMPLITUDE SELECTION REGISTER ACTIVATION

NAME	ENA	WEB	CR0 Bit 2	WEN2	WEN1	WEN0	MSB BSEL = 0	LSB BSEL = 0	MSB BSEL = 1	LSB BSEL = 1
OFF	0	X	x	X	X	X	X	X	X	X
READ	1	1	0	X	X	X	0-19	1-09	0-19	1-09
W0	1	0	1	0	0	0	0-10	2-10	0-11	2-11
W1	1	0	1	0	0	1	0-04	2-04	0-05	2-05
W2	1	0	1	0	1	0	0-06	2-06	0-07	2-07
W3	1	0	1	0	1	1	0-08	2-08	0-09	2-09
W4	1	0	1	1	0	0	0-0A	2-0A	0-0B	2-0B
W5	1	0	1	1	0	1	0-0C	2-0C	0-0D	2-0D
W6	1	0	1	1	1	0	0-0E	2-0E	0-0F	2-0F
W7	1	0	1	1	1	1	0-12	2-12	0-13	2-13

NOTES:

24. There are two sets of write current registers. When BSEL = 1, bank 1 is selected. When BSEL = 0, bank 0 is selected.
25. Read and write are independent. Read is enabled with a control bit.
26. Register terminology is page Number-Register number (hex). Thus 1-09 is page 1, register 09h

Applications Information

I_{OUT}

The data sheet values for oscillator current, and write current are based on an R_{SET} of 620Ω when PMAX and WriteDAC are both set to full scale. The user may choose R_{SET} to match the output current needs of the application.

The PMAX DAC is biased by I_{RSET} (= V_{RSET}/R_{SET}). See the "Typical Performance Curves" on page 10.

The write channel output capability for a typical part is shown in Figure 1. The amount of I_{OUT} will be limited by the available headroom voltage at the I_{OUTx} pins.

A four input DAC (Reg 1-0A bits 3, 2, 1, 0) can be used to control the amount of RC snubbing applied to the outputs.

Read current may be controlled by either the Read DAC or the IAPC input. When set by PREAD, I_{READ} is limited to the data sheet value, whereas the I_{APC} input will allow a significantly higher value to be obtained. The ReadDAC and I_{APC} currents sum together.

Glitches could occur if two or three WEN lines are changed simultaneously, and the propagation delay is different for the two lines between the inner circuits of the controller and the inner circuits of the LDD. Because the WEN lines are encoded, the selected write current will be correct before the change in code, and again after the code changes. But some other output could result momentarily if the propagation delays are not matched. The skew detector detects the first rising edge at the LVDS outputs.

F_{OSC}

Both F_{OSC} and R_{FREQ} may be chosen to accommodate the desired range or operating point of the HFMFREQ DAC. Although F_{OSC} is relatively linear with DAC code, monotonicity is not guaranteed (see Figure 5). Under extreme conditions, where VSO = 4.5V and temperature is +125°C, the HFM frequency is only capable of 900MHz (see Figure 6).

The oscillator may be turned on either by the OSCEN lines or by the WEN code selected. The particular code that selects the oscillator is under program control. The Pcool function is only available through the program control and WEN selection.

The WEB enables write current. Thus WEN code 000 may also select a write current.

Power

The main power consumption is caused by the headroom voltage across the output stage (V_{SO} - V_{IOUT}) xI_{OUT}. For I_{OUT1} and I_{OUT2}, the V_{SO} can be reduced below 5.0V (but above $V_{SO\text{-}GOOD}$), as long as sufficient headroom voltage is available to obtain the desired output current. For the blue outputs, the built in ADC can be used to obtain the output voltage, which is also the headroom voltage. The HFM oscillator power consumption will increase with increasing frequency and amplitude (see Figure 7).

Note that in the QFN package, the die is mounted directly on the thermal pad. This provides a very low thermal resistance Junction to thermal pad of just a few °C/W. The problem is in moving the heat from the thermal pad to some other heat sink.

Figure 10 shows that when mounted well on a 4-layer PCB with 3 ground plane layers, and an area of 10cmx10cm, the θ_{JA} is +37°C/W. The typical application will not afford this good of a heat sink.

Typical Performance Curves

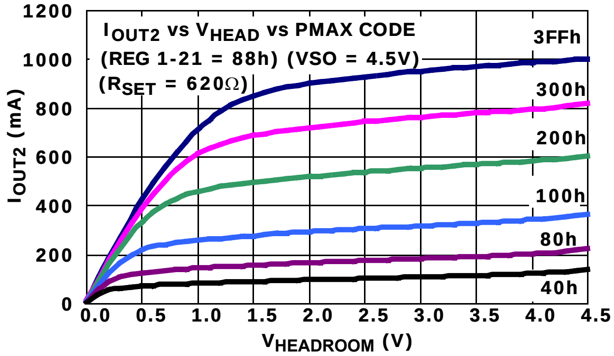


FIGURE 1. I_{OUT} WRITE CURRENT vs V_{SD} vs I_{PMAX_BIAS}

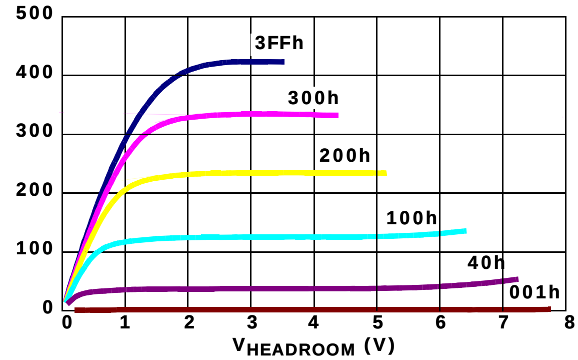


FIGURE 2. I_{BLUE} vs P_{MAX} vs $V_{HEADROOM}$ (V_{SO} = 5.0V) (R_{SET} = 620Ω) (1-21 = FFh), (R_{LOAD} = 10Ω)

Typical Performance Curves (Continued)

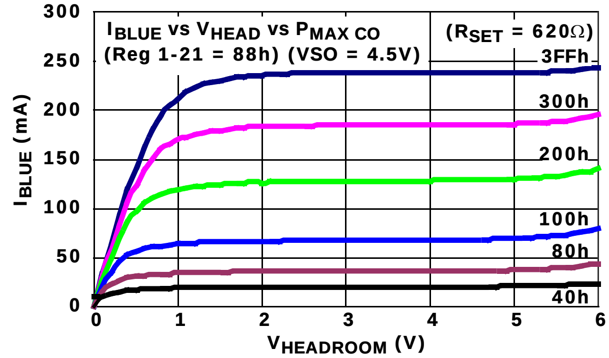


FIGURE 3. I_{BLUE} WRITE CURRENT vs V_{DS} vs I_{PMAX_BIAS}

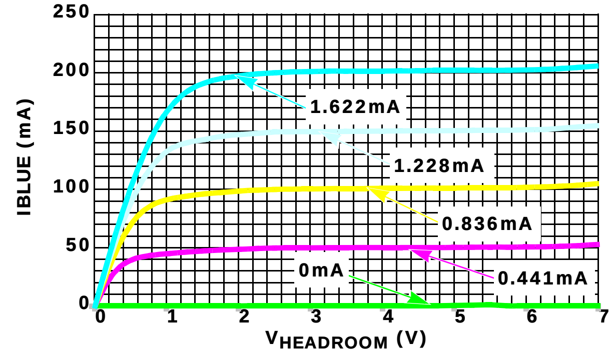


FIGURE 4. I_{BLUE} READ vs $V_{HEADROOM}$ vs I_{APC}, (REG 1-212 = 88h) (V_{SO} = 5.0V) (R_{SET} = 620Ω)

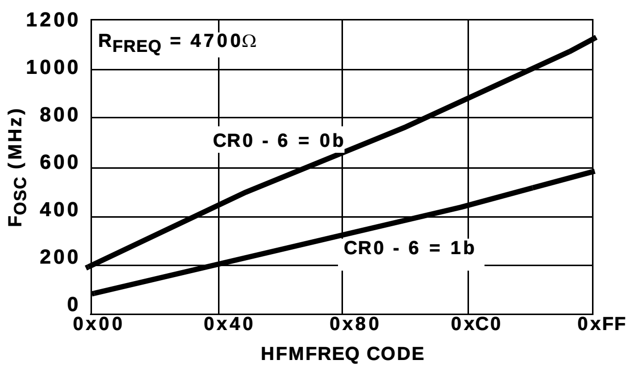


FIGURE 5. HFM CONTROL

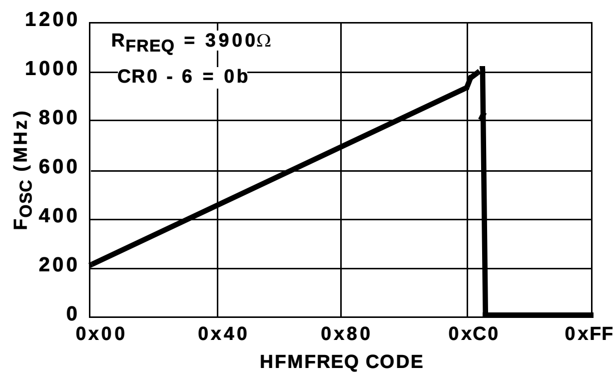


FIGURE 6. HFM CONTROL; VSO = 4.5V; TEMP = +125°C

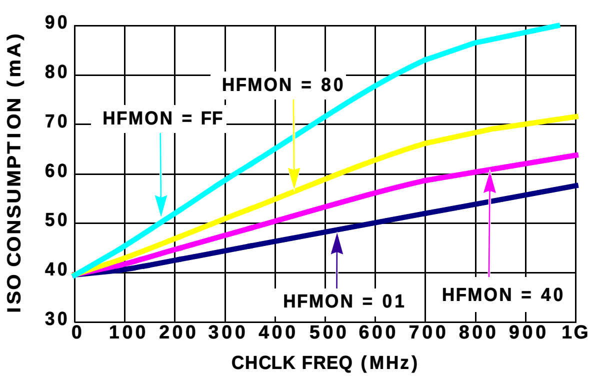


FIGURE 7. HFM OSCILLATOR CURRENT CONSUMPTION

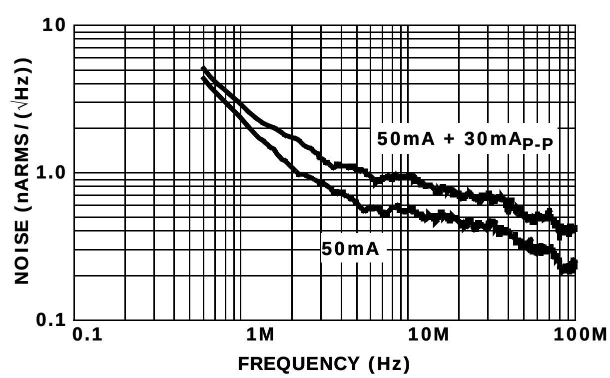


FIGURE 8. I_{OUTX} NOISE vs FREQUENCY

Typical Performance Curves (Continued)

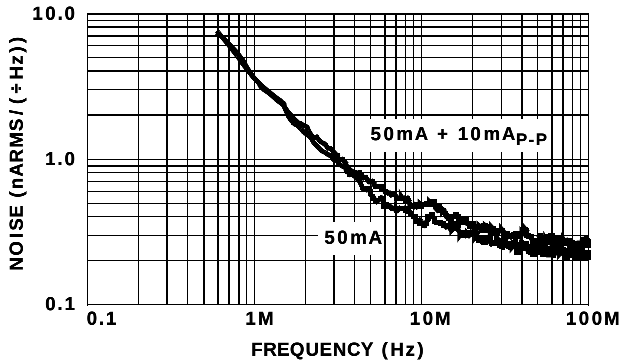


FIGURE 9. I_{BLUE} NOISE vs FREQUENCY

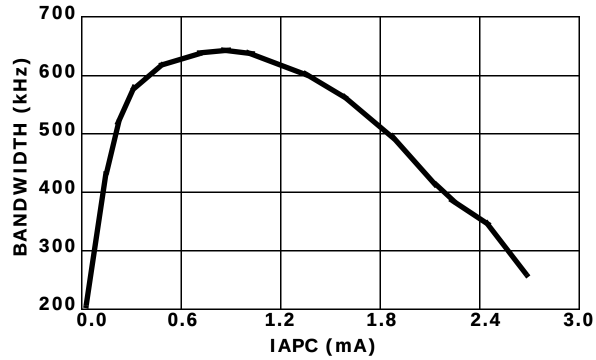


FIGURE 10. I_{OUT}/I_{APC} BANDWIDTH vs I_{APC}

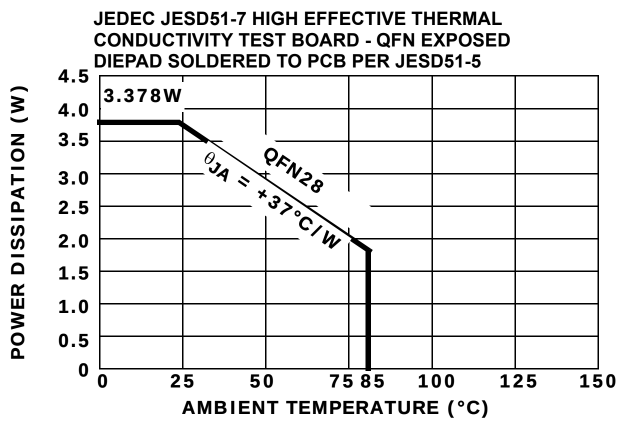


FIGURE 11. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

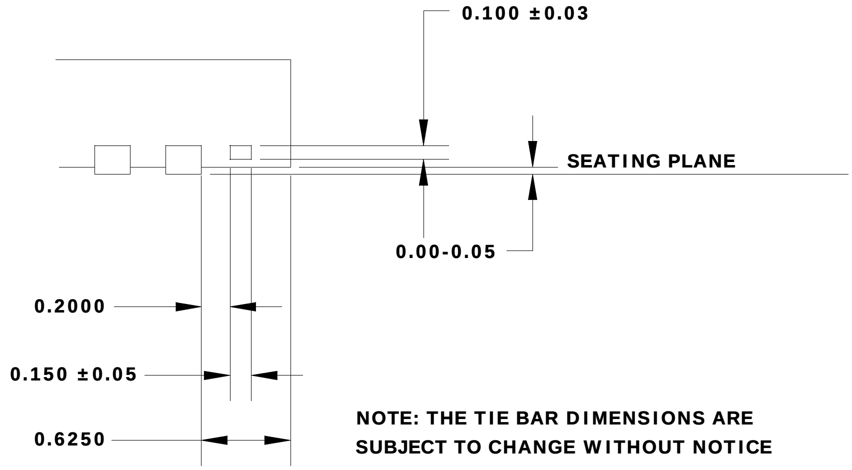


FIGURE 12. TIE BAR LOCATION FOR 4X5 QFN

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
12/3/15	FN6909.3	Removed ISL58781CRZ-EVAL from Ordering Information table.
7/22/13	FN6909.2	Updated datasheet by changing Logo, removed side bar with part number, copyright on page 1 and changed Product Information verbiage to About Intersil verbiage on page 14.
11/12/09	FN6909.1	Added Figure 12 “TIE BAR LOCATION FOR 4X5 QFN” on page 13 Added “Pin Number” column to “Pin Descriptions” on page 3 On page 7: In HFM spec Table, for IMAX-RED-OFF-LINK, IMAX-RED-OFF-UNLINK & IMAX-BLUE-OFF parameters, changed "HFMOFF = 0x7FF" test condition to "HFMOFF = 0xFFF": since HFMOFF DAC is 12 bits now. On page 7: In HFM spec Table, Reg 1-21h=x7h for Imax_Blue_ON: Imax_Blue_On (Blue HFM ON amplitude) does not depend on Reg 1-21h setting. So, deleted "Reg 1-21h=x7h" condition
9/2/09	FN6909.0	Initial release.

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

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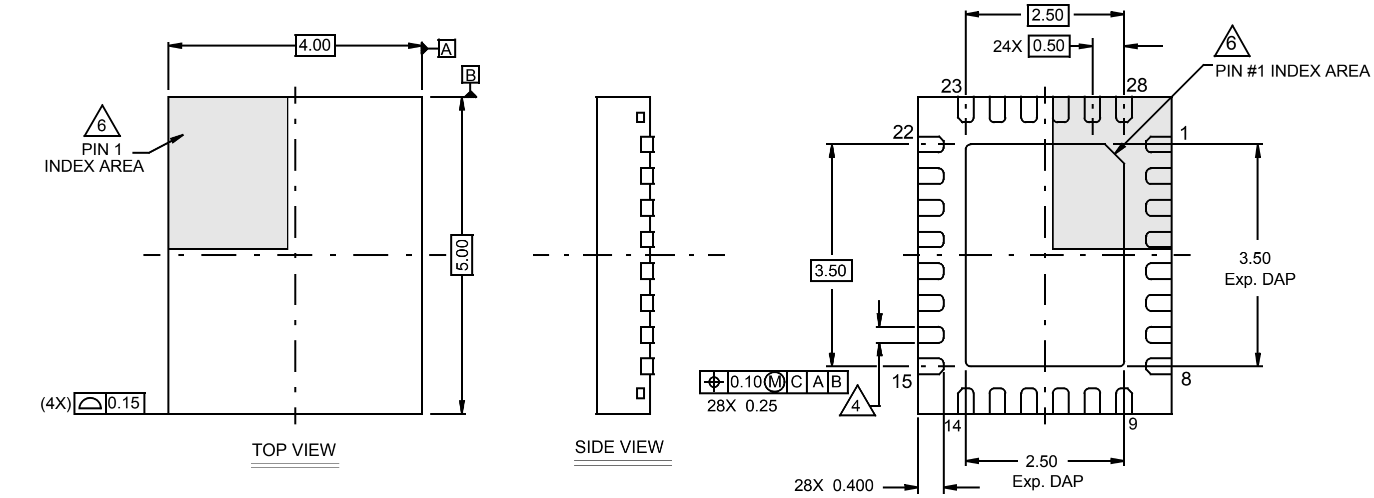
Package Outline Drawing

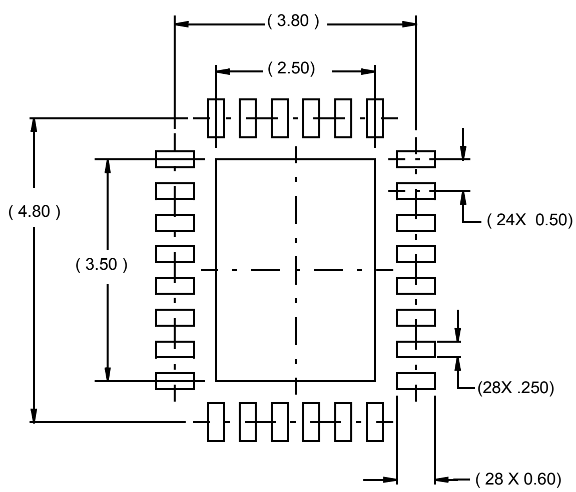
L28.4x5A

28 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE

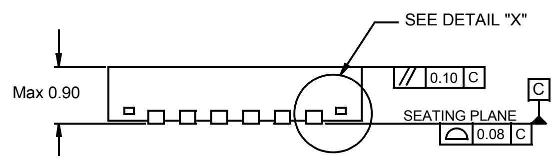
Rev 2, 06/08



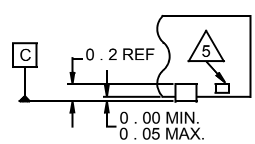
TOP VIEW SIDE VIEW BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.