# ISL62881, ISL62881B

Single-Phase PWM Regulator for IMVP-6.5™ Mobile CPUs and GPUs

The ISL62881 is a single-phase PWM buck regulator for miroprocessor or graphics processor core power supply. It uses an integrated gate driver to provide a complete solution. The PWM modulator of ISL62881 is based on Intersil's Robust Ripple Regulator (R$^3$) technology™. Compared with traditional modulators, the R$^3$™ modulator commands variable switching frequency during load transients, achieving faster transient response. With the same modulator, the switching frequency is reduced at light load, increasing the regulator efficiency.

The ISL62881 can be configured as CPU or graphics Vcore controller and is fully compliant with IMVP-6.5™ specifications. It responds to DPRSLPVR signals by entering/exiting diode emulation mode. It reports the regulator output current through the IMON pin. It senses the current by using either discrete resistor or inductor DCR whose variation over-temperature can be thermally compensated by a single NTC thermistor. It uses differential remote voltage sensing to accurately regulate the processor die voltage. The adaptive body diode conduction time reduction function minimizes the body diode conduction loss in diode emulation mode. User-selectable overshoot reduction function offers an option to aggressively reduce the output capacitors as well as the option to disable it for users concerned about increased system thermal stress.

Maintaining all the ISL62881 functions, the ISL62881B offers VR_TT# function for thermal throttling control. It also offers the split LGATE function to further improve light load efficiency.

## Features

- Precision Core Voltage Regulation
  - 0.5% System Accuracy Over-Temperature
  - Enhanced Load Line Accuracy
- Voltage Identification Input
  - 7-Bit VID Input, 0V to 1.500V in 12.5mV Steps
  - Supports VID Changes On-The-Fly
- Supports Multiple Current Sensing Methods
  - Lossless Inductor DCR Current Sensing
  - Precision Resistor Current Sensing
- Superior Noise Immunity and Transient Response
- Current Monitor
- Differential Remote Voltage Sensing
- High Efficiency Across Entire Load Range
- Integrated Gate Driver
- Split LGATE Driver to Increase Light-Load Efficiency (for ISL62881B)
- Adaptive Body Diode Conduction Time Reduction
- User-selectable Overshoot Reduction Function
- Capable of Disabling the Droop Function
- Audio-filtering for GPU Application
- Small Footprint 28 Ld 4x4 TQFN Package
- Pb-Free (RoHS Compliant)

## Applications

- Notebook Computers

## Ordering Information

| PART NUMBER (Notes 1, 2, 3) | PART MARKING | TEMP. RANGE (°C) | PACKAGE (Pb-Free) | PKG. DWG. # |
|---|---|---|---|---|
| ISL62881HRTZ | 628 81HRTZ | -10 to +100 | 28 Ld 4x4 TQFN | L28.4x4 |
| ISL62881BHRTZ | 62881B HRTZ | -10 to +100 | 32 Ld 5x5 TQFN | L32.5x5E |

NOTES:

1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.

2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

3. For Moisture Sensitivity Level (MSL), please see device information page for ISL62881, ISL62881B. For more information on MSL please see techbrief TB363.

# Pin Configurations

**ISL62881**
**(28 LD TQFN)**
**TOP VIEW**



**ISL62881B**
**(32 LD TQFN)**
**TOP VIEW**
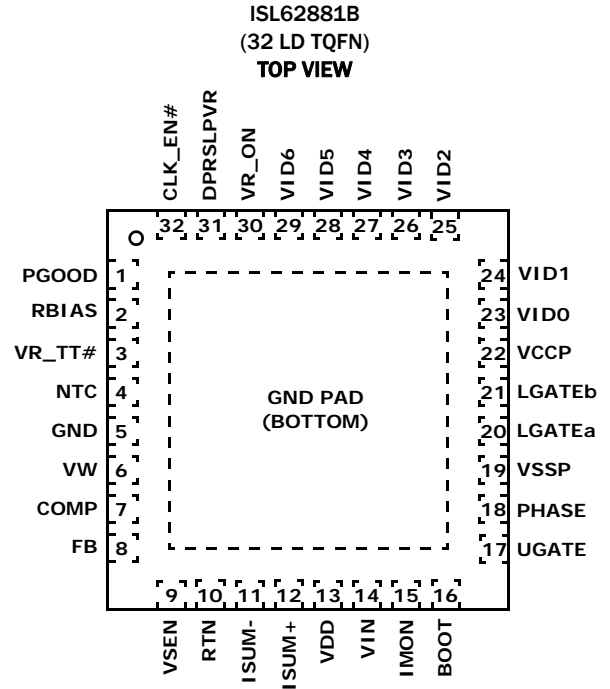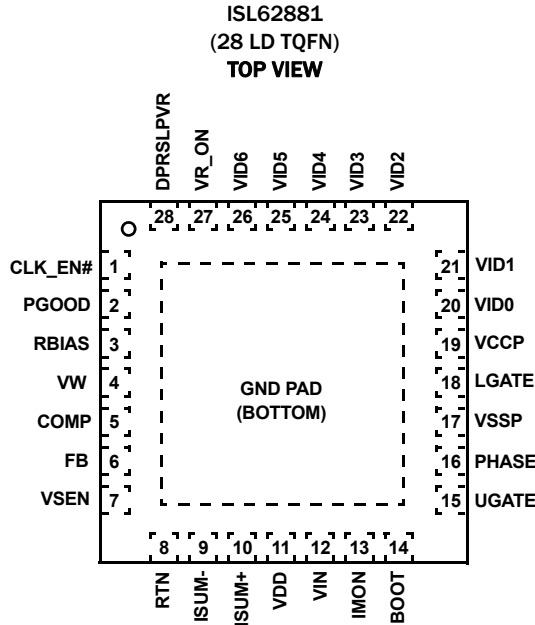


# Pin Function Descriptions

## GND (Bottom Pad)

Signal common of the IC. Unless otherwise stated, signals are referenced to the GND pin.

## CLK_EN#

Open drain output to enable system PLL clock; goes active 13 switching cycles after $V_{core}$ is within 10% of $V_{boot}$.

## PGOOD

Power-Good open-drain output indicating when the regulator is able to supply regulated voltage. Pull-up externally with a 680$\Omega$ resistor to VCCP or 1.9k$\Omega$ to 3.3V.

## RBIAS

A resistor to GND sets internal current reference. A 147k$\Omega$ resistor sets the controller for CPU core application and a 47k$\Omega$ resistor sets the controller for GPU core application.

## VR_TT#

Thermal overload output indicator.

## NTC

Thermistor input to VR_TT# circuit.

## VW

A resistor from this pin to COMP programs the switching frequency (8k$\Omega$ gives approximately 300kHz).

## COMP

This pin is the output of the error amplifier. Also, a resistor across this pin and GND adjusts the overcurrent threshold.

## FB

This pin is the inverting input of the error amplifier.

## VSEN

Remote core voltage sense input. Connect to microprocessor die.

## RTN

Remote voltage sensing return. Connect to ground at microprocessor die.

## ISUM- and ISUM+

Droop current sense input.

## VDD

5V bias power.

## VIN

Battery supply voltage, used for feed-forward.

## IMON

An analog output. IMON outputs a current proportional to the regulator output current.

## BOOT

Connect an MLCC capacitor across the BOOT and the PHASE pins. The boot capacitor is charged through an internal boot

diode connected from the VCCP pin to the BOOT pin, each time the PHASE pin drops below VCCP minus the voltage dropped across the internal boot diode.

## UGATE

Output of the high-side MOSFET gate driver. Connect the UGATE pin to the gate of the high-side MOSFET.

## PHASE

Current return path for the high-side MOSFET gate driver. Connect the PHASE pin to the node consisting of the high-side MOSFET source, the low-side MOSFET drain and the output inductor.

## VSSP

Current return path for the low-side MOSFET gate driver. Connect the VSSP pin to the source of the low-side MOSFET through a low impedance path, preferably in parallel with the trace connecting the LGATE pin to the gate of the low-side MOSFET.

## LGATE (for ISL62881)

Output of the low-side MOSFET gate driver. Connect the LGATE pin to the gate of the low-side MOSFET.

## LGATEa (for ISL62881B)

Output of the low-side MOSFET gate driver that is always active. Connect the LGATEa pin to the gate of the low-side MOSFET that is active all the time.

## LGATEb (For ISL62881B)

Another output of the low-side MOSFET gate driver. This gate driver will be pulled low when the DPRSLPVR pin logic is high. Connect the LGATEb pin to the gate of the low-side MOSFET that is idle in deeper sleep mode.

## VCCP

Input voltage bias for the internal gate drivers. Connect +5V to the VCCP pin. Decouple with at least 1µF of an MLCC capacitor to VSSP1 and VSSP2 pins respectively.

## VID0, VID1, VID2, VID3, VID4, VID5, VID6

VID input with VID0 = LSB and VID6 = MSB.

## VR_ON

Voltage regulator enable input. A high level logic signal on this pin enables the regulator.

## DPRSLPVR

A high level logic signal on this pin puts the ISL62881 in 1-phase diode emulation mode. If $R_{BIAS}$ = 47k$\Omega$ (GPU VR application), this pin also controls $V_{core}$ slew rate. $V_{core}$ slews at 5mV/µs for DPRSLPVR = 0 and 10mV/µs for DPRSLPVR = 1. If $R_{BIAS}$ = 147k$\Omega$ (CPU VR application), this pin doesn't control $V_{core}$ slew rate.

# Block Diagram

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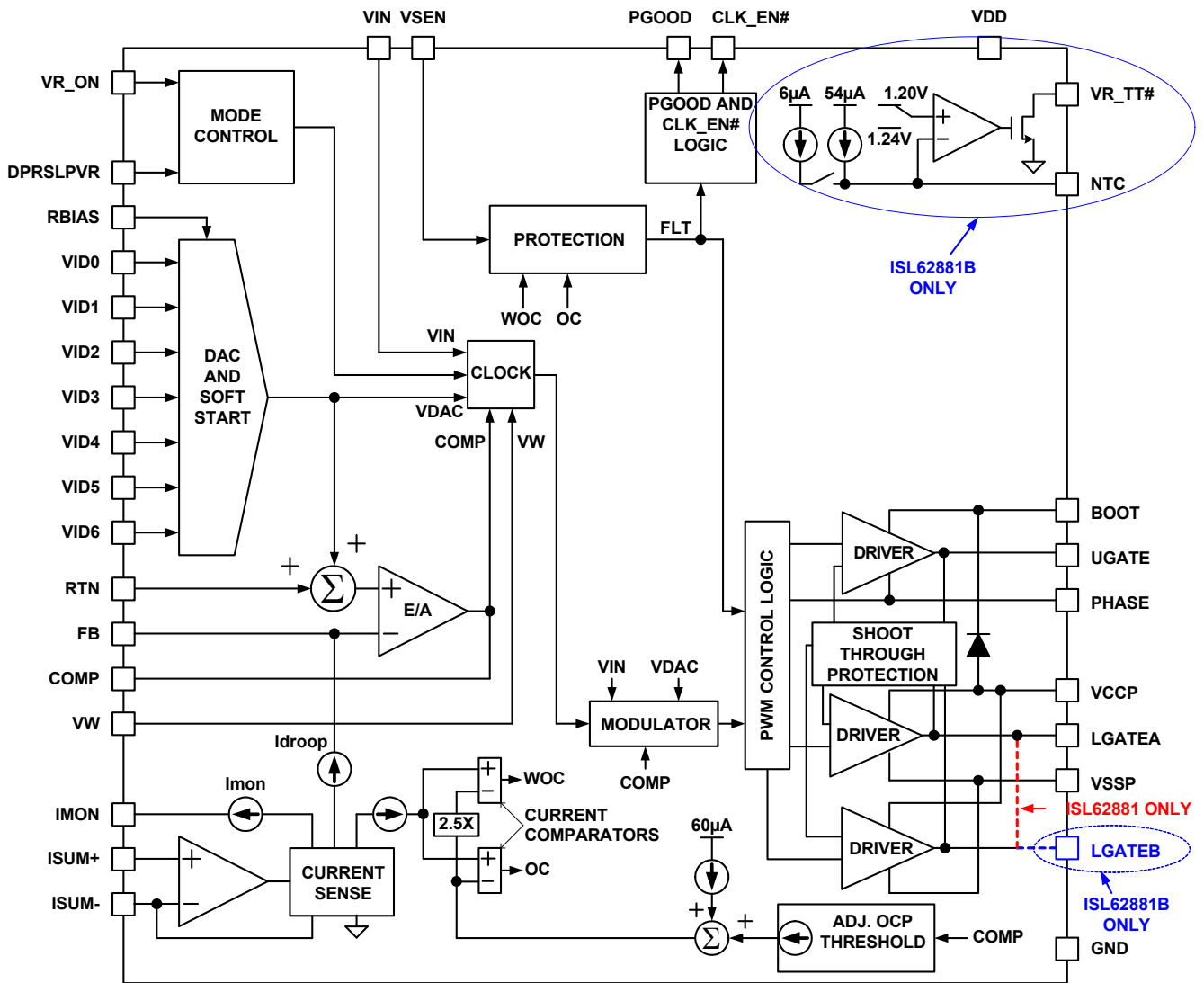
## Absolute Maximum Ratings

Supply Voltage, VDD. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . -0.3V to +7V
Battery Voltage, VIN . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . +28V
Boot Voltage (BOOT). . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . .-0.3V to +33V
Boot to Phase Voltage (BOOT-PHASE) . . . . . . . . . . . . . . . -0.3V to +7V(DC)
. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . -0.3V to +9V(<10ns)
Phase Voltage (PHASE) . . . . . . . . . . . . . . . . -7V (<20ns Pulse Width, 10µJ)
UGATE Voltage (UGATE) . . . . . . . . . . . . . . . . . . . PHASE-0.3V (DC) to BOOT
. . . . . . . . . . . . . . . . . . . . .PHASE-5V (<20ns Pulse Width, 10µJ) to BOOT
LGATE Voltage (LGATE). . . . . . . . . . . . . . . . . . . . . -0.3V (DC) to VDD + 0.3V
. . . . . . . . . . . . . . . . . . . . . -2.5V (<20ns Pulse Width, 5µJ) to VDD + 0.3V
All Other Pins . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . -0.3V to (VDD + 0.3V)
Open Drain Outputs, PGOOD, VR_TT#, CLK_EN# . . . . . . . . . . . . . -0.3V to +7V

## Thermal Information

| Thermal Resistance (Typical, Notes 4, 5) | $\theta_{JA}$ (°C/W) | $\theta_{JC}$ (°C/W) |
|---|---|---|
| 28 Ld TQFN Package . . . . . . . . . . . . . . . . . . | 40 | 3 |
| 32 Ld TQFN Package . . . . . . . . . . . . . . . . . . | 32 | 3 |

Maximum Junction Temperature . . . . . . . . . . . . . . . . . . . . . . . . . . . . .+150°C
Maximum Storage Temperature Range . . . . . . . . . . . . . .-65°C to +150°C
Pb-Free Reflow Profile . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

## Recommended Operating Conditions

Supply Voltage, VDD. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . .+5V ±5%
Battery Voltage, VIN . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . +4.5V to 25V
Ambient Temperature . . . . . . . . . . . . . . . . . . . . . . . . . . . . .-10°C to +100°C
Junction Temperature . . . . . . . . . . . . . . . . . . . . . . . . . . . . .-10°C to +125°C

*CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.*

NOTES:

4. $\theta_{JA}$ is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.

5. For $\theta_{JC}$, the "case temp" location is the center of the exposed metal pad on the package underside.

## Electrical Specifications
Operating Conditions: $V_{DD}$ = 5V, $T_A$ = -10°C to +100°C, $f_{SW}$ = 300kHz, unless otherwise noted. **Boldface limits apply over the operating temperature range, -10°C to +100°C.**

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN (Note 6) | TYP | MAX (Note 6) | UNITS |
|---|---|---|---|---|---|---|
| **INPUT POWER SUPPLY** | | | | | | |
| +5V Supply Current | $I_{VDD}$ | VR_ON = 1V | | 3.2 | **4.0** | mA |
| | | VR_ON = 0V | | | **1** | µA |
| Battery Supply Current | $I_{VIN}$ | VR_ON = 0V | | | **1** | µA |
| $V_{IN}$ Input Resistance | $R_{VIN}$ | VR_ON = 1V | | 900 | | kΩ |
| Power-On-Reset Threshold | $POR_r$ | $V_{DD}$ rising | | 4.35 | **4.5** | V |
| | $POR_f$ | $V_{DD}$ falling | **4.00** | 4.15 | | V |
| **SYSTEM AND REFERENCES** | | | | | | |
| System Accuracy | %Error ($V_{CC\_CORE}$) | No load; closed loop, active mode range VID = 0.75V to 1.50V | **-0.5** | | **+0.5** | % |
| | | VID = 0.5V to 0.7375V | **-8** | | **+8** | mV |
| | | VID = 0.3V to 0.4875V | **-15** | | **+15** | mV |
| $V_{BOOT}$ | | | **1.0945** | 1.100 | **1.1055** | V |
| Maximum Output Voltage | $V_{CC\_CORE(max)}$ | VID = [0000000] | | 1.500 | | V |
| Minimum Output Voltage | $V_{CC\_CORE(min)}$ | VID = [1111111] | | 0 | | V |
| $R_{BIAS}$ Voltage | | $R_{BIAS}$ = 147kΩ | **1.45** | 1.47 | **1.49** | V |
| **CHANNEL FREQUENCY** | | | | | | |
| Nominal Channel Frequency | $f_{SW(nom)}$ | $RF_{SET}$ = 7kΩ, $V_{COMP}$ = 1V | **295** | 310 | **325** | kHz |
| Adjustment Range | | | **200** | | **500** | kHz |
| **AMPLIFIERS** | | | | | | |
| Current-Sense Amplifier Input Offset | | $I_{FB}$ = 0A | **-0.15** | | **+0.15** | mV |
| Error Amp DC Gain | $A_{v0}$ | | | 90 | | dB |
| Error Amp Gain-Bandwidth Product | GBW | $C_L$ = 20pF | | 18 | | MHz |

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## Electrical Specifications
Operating Conditions: $V_{DD}$ = 5V, $T_A$ = -10°C to +100°C, $f_{SW}$ = 300kHz, unless otherwise noted. **Boldface limits apply over the operating temperature range, -10°C to +100°C. (Continued)**

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN (Note 6) | TYP | MAX (Note 6) | UNITS |
|---|---|---|---|---|---|---|
| **POWER GOOD AND PROTECTION MONITORS** | | | | | | |
| PGOOD Low Voltage | $V_{OL}$ | $I_{PGOOD}$ = 4mA | | 0.26 | **0.4** | V |
| PGOOD Leakage Current | $I_{OH}$ | PGOOD = 3.3V | **-1** | | **1** | µA |
| PGOOD Delay | tpgd | CLK_ENABLE# LOW to PGOOD HIGH | **6.3** | 7.6 | **8.9** | ms |
| **UGATE DRIVER** | | | | | | |
| UGATE Pull-Up Resistance | $R_{UGPU}$ | 200mA Source Current | | 1.0 | **1.5** | Ω |
| UGATE Source Current | $I_{UGSRC}$ | BOOT - UGATE = 2.5V | | 2.0 | | A |
| UGATE Sink Resistance | $R_{UGPD}$ | 250mA Sink Current | | 1.0 | **1.5** | Ω |
| UGATE Sink Current | $I_{UGSNK}$ | UGATE - PHASE = 2.5V | | 2.0 | | A |
| **LGATE DRIVER For ISL62881** | | | | | | |
| LGATE Pull-Up Resistance | $R_{LGPU}$ | 250mA Source Current | | 1.0 | **1.5** | Ω |
| LGATE Source Current | $I_{LGSRC}$ | VCCP - LGATE = 2.5V | | 2.0 | | A |
| LGATE Sink Resistance | $R_{LGPD}$ | 250mA Sink Current | | 0.5 | **0.9** | Ω |
| LGATE Sink Current | $I_{LGSNK}$ | LGATE - VSSP = 2.5V | | 4.0 | | A |
| UGATE to LGATE Deadtime | $t_{UGFLGR}$ | UGATE falling to LGATE rising, no load | | 23 | | ns |
| LGATE to UGATE Deadtime | $t_{LGFUGR}$ | LGATE falling to UGATE rising, no load | | 28 | | ns |
| **LGATE DRIVERS For ISL62881B** | | | | | | |
| LGATEa and b Pull-Up Resistance | $R_{LGPU}$ | 250mA Source Current | | 2.0 | **3** | Ω |
| LGATEa and b Source Current | $I_{LGSRC}$ | VCCP - LGATEa and b = 2.5V | | 1.0 | | A |
| LGATEa and b Sink Resistance | $R_{LGPD}$ | 250mA Sink Current | | 1 | **1.8** | Ω |
| LGATEa and b Sink Current | $I_{LGSNK}$ | LGATEa and b - VSSP = 2.5V | | 2.0 | | A |
| UGATE to LGATEa and b Deadtime | $t_{UGFLGR}$ | UGATE falling to LGATEa and b rising, no load | | 23 | | ns |
| LGATEa and b to UGATE Deadtime | $t_{LGFUGR}$ | LGATEa and b falling to UGATE rising, no load | | 28 | | ns |
| **BOOTSTRAP DIODE** | | | | | | |
| Forward Voltage | $V_F$ | PVCC = 5V, $I_F$ = 2mA | | 0.58 | | V |
| Reverse Leakage | $I_R$ | $V_R$ = 25V | | 0.2 | | µA |
| **PROTECTION** | | | | | | |
| Overvoltage Threshold | $OV_H$ | VSEN rising above setpoint for >1ms | **150** | 200 | **240** | mV |
| Severe Overvoltage Threshold | $OV_{HS}$ | VSEN rising for >2µs | **1.525** | 1.55 | **1.575** | V |
| OC Threshold Offset | | ISUM- pin current | **8.2** | 10.1 | **12** | µA |
| Undervoltage Threshold | $UV_f$ | VSEN falling below setpoint for >1.2ms | **-355** | -295 | **-235** | mV |
| **LOGIC THRESHOLDS** | | | | | | |
| VR_ON Input Low | $V_{IL(1.0V)}$ | | | | **0.3** | V |
| VR_ON Input High | $V_{IH(1.0V)}$ | | **0.7** | | | V |
| VID0-VID6 and DPRSLPVR Input Low | $V_{IL(1.0V)}$ | | | | **0.3** | V |
| VID0-VID6 and DPRSLPVR Input High | $V_{IH(1.0V)}$ | | **0.7** | | | V |
| **THERMAL MONITOR (For ISL62881B)** | | | | | | |
| NTC Source Current | | NTC = 1.3V | **53** | 60 | **67** | µA |

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**Electrical Specifications** Operating Conditions: $V_{DD}$ = 5V, $T_A$ = -10°C to +100°C, $f_{SW}$ = 300kHz, unless otherwise noted. **Boldface limits apply over the operating temperature range, -10°C to +100°C.  (Continued)**

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN (Note 6) | TYP | MAX (Note 6) | UNITS |
|---|---|---|---|---|---|---|
| Over-Temperature Threshold | | V (NTC) falling | **1.18** | 1.2 | **1.22** | V |
| VR_TT# Low Output Resistance | $R_{TT}$ | I = 20mA | | 6.5 | **9** | Ω |
| **CLK_EN# OUTPUT LEVELS** | | | | | | |
| CLK_EN# Low Output Voltage | $V_{OL}$ | I = 4mA | | 0.26 | **0.4** | V |
| CLK_EN# Leakage Current | $I_{OH}$ | CLK_EN# = 3.3V | **-1** | | **1** | µA |
| **CURRENT MONITOR** | | | | | | |
| IMON Output Current | $I_{IMON}$ | ISUM- pin current = 20µA | **108** | 120 | **132** | µA |
| | | ISUM- pin current = 10µA | **51** | 60 | **69** | µA |
| | | ISUM- pin current = 5µA | **22** | 30 | **37.5** | µA |
| IMON Clamp Voltage | $V_{IMONCLAMP}$ | | | 1.1 | **1.15** | V |
| Current Sinking Capability | | | | 275 | | µA |
| **INPUTS** | | | | | | |
| VR_ON Leakage Current | $I_{VR\_ON}$ | VR_ON = 0V | **-1** | 0 | | µA |
| | | VR_ON = 1V | | 0 | **1** | µA |
| VIDx Leakage Current | $I_{VIDx}$ | VIDx = 0V | **-1** | 0 | | µA |
| | | VIDx = 1V | | 0.45 | **1** | µA |
| DPRSLPVR Leakage Current | $I_{DPRSLPVR}$ | DPRSLPVR = 0V | **-1** | 0 | | µA |
| | | DPRSLPVR = 1V | | 0.45 | **1** | µA |
| **SLEW RATE** | | | | | | |
| Slew Rate (For VID Change) | SR | | **5** | | **6.5** | mV/µs |

NOTE:

6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

# Gate Driver Timing Diagram
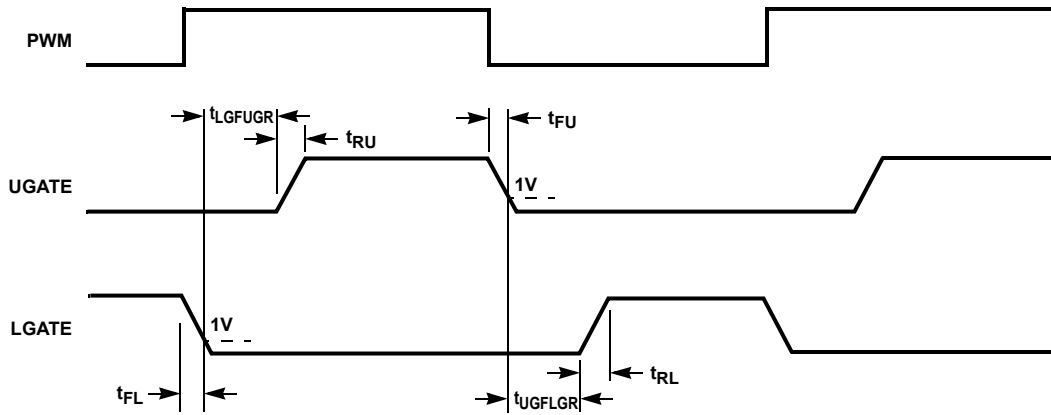


# Simplified Application Circuits
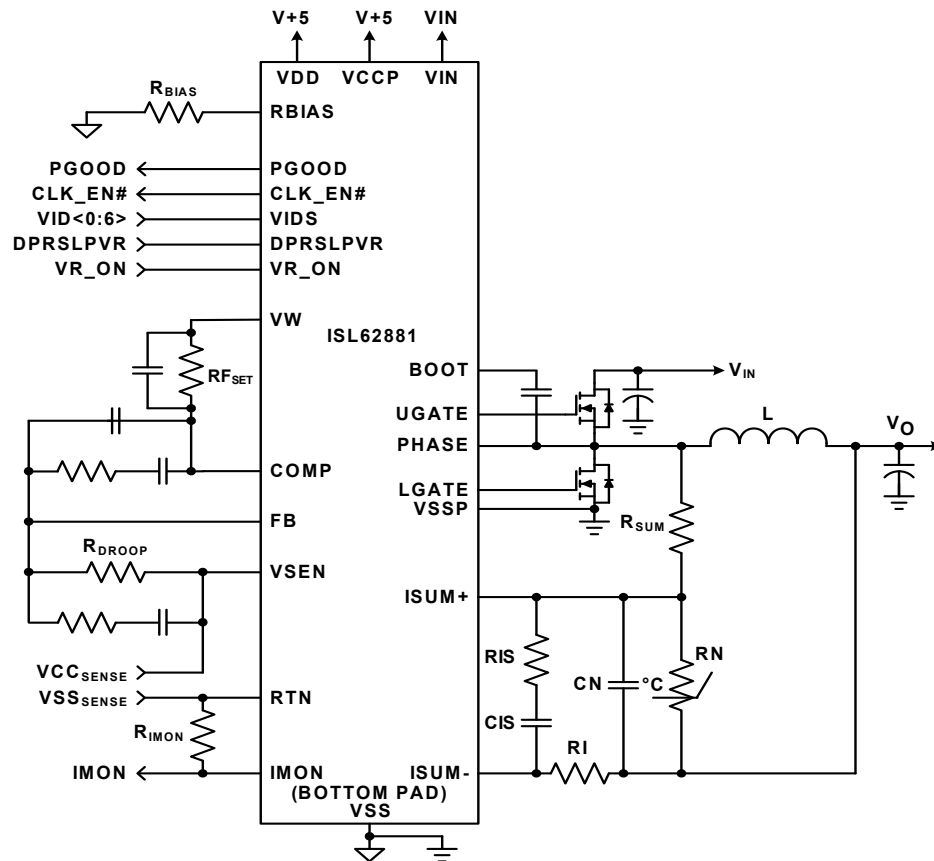


FIGURE 1.  ISL62881 TYPICAL APPLICATION CIRCUIT USING DCR SENSING

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# Simplified Application Circuits (Continued)



**FIGURE 2. ISL62881 TYPICAL APPLICATION CIRCUIT USING RESISTOR SENSING**

# Simplified Application Circuits (Continued)
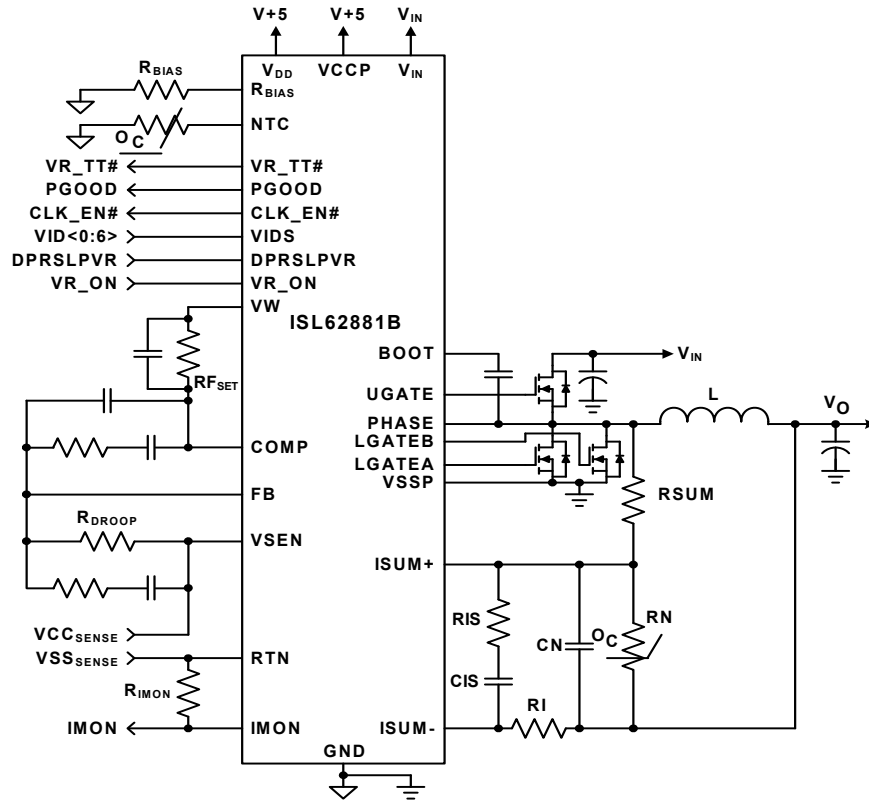


FIGURE 3. ISL62881B TYPICAL APPLICATION CIRCUIT USING DCR SENSING

# Simplified Application Circuits (Continued)
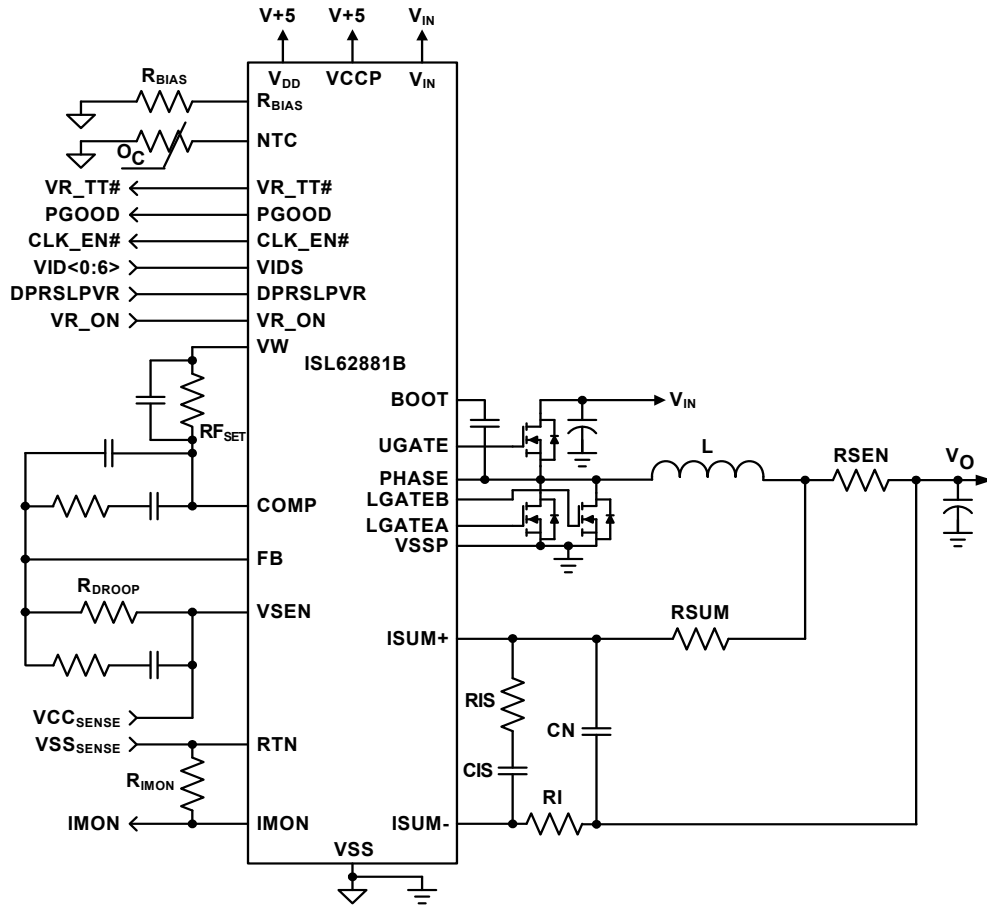


**FIGURE 4. ISL62881B TYPICAL APPLICATION CIRCUIT USING RESISTOR SENSING**

# Theory of Operation

## Multiphase R$^{3™}$ Modulator
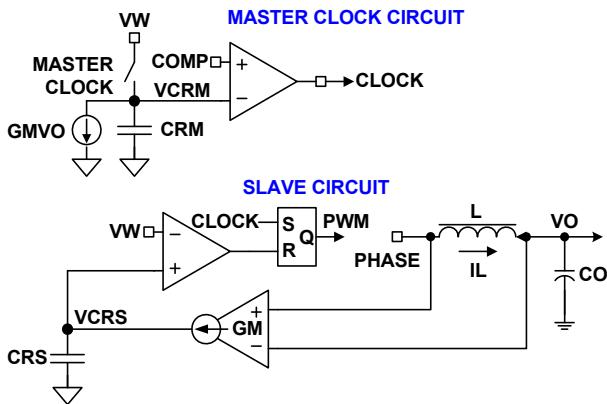


FIGURE 5. R$^{3™}$ MODULATOR CIRCUIT
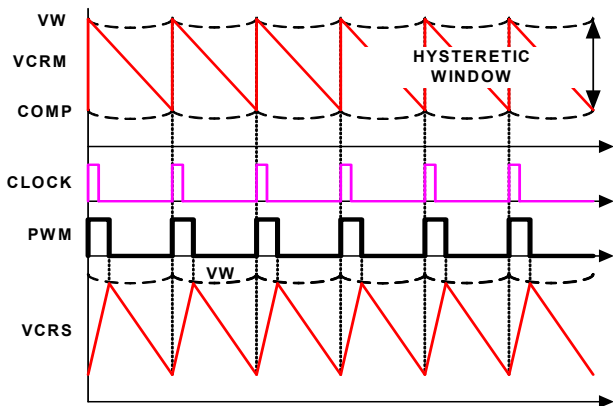


FIGURE 6. R$^{3™}$ MODULATOR OPERATION PRINCIPLES IN STEADY STATE
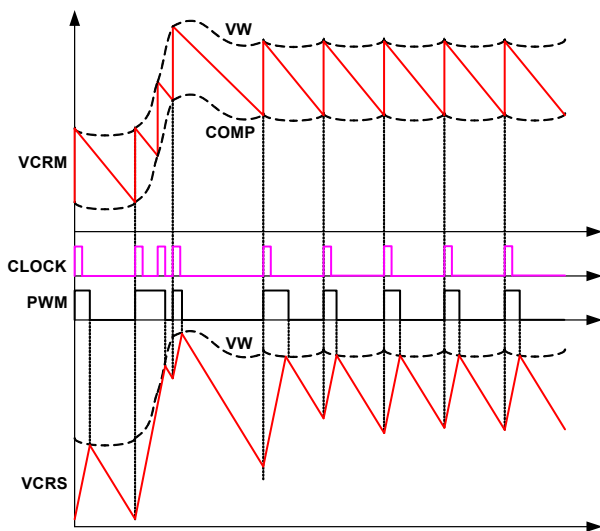


FIGURE 7. R$^{3™}$ MODULATOR OPERATION PRINCIPLES IN LOAD INSERTION RESPONSE

The ISL62881 is a single-phase regulator implementing Intel$^{®}$ IMVP-6.5$^{™}$ protocol. It uses Intersil patented R$^{3™}$(Robust Ripple Regulator$^{™}$) modulator. The R$^{3™}$ modulator combines the best features of fixed frequency PWM and hysteretic PWM while eliminating many of their shortcomings. Figure 5 conceptually shows the ISL62881 R$^{3™}$ modulator circuit, and Figure 6 shows the operation principles.

A current source flows from the VW pin to the COMP pin, creating a voltage window set by the resistor between between the two pins. This voltage window is called VW window in the following discussion.

Inside the IC, the modulator uses the master clock circuit to generate the clocks for the slave circuit. The modulator discharges the ripple capacitor $C_{rm}$ with a current source equal to $g_m V_o$, where $g_m$ is a gain factor. $C_{rm}$ voltage $V_{crm}$ is a sawtooth waveform traversing between the VW and COMP voltages. It resets to VW when it hits COMP, and generates a one-shot clock signal.

The slave circuit has its own ripple capacitor $C_{rs}$, whose voltage mimics the inductor ripple current. A $g_m$ amplifier converts the inductor voltage into a current source to charge and discharge $C_{rs}$. The slave circuit turns on its PWM pulse upon receiving the clock signal, and the current source charges $C_{rs}$. When $C_{rs}$ voltage $V_{Crs}$ hits VW, the slave circuit turns off the PWM pulse, and the current source discharges $C_{rs}$.

Since the ISL62881 works with $V_{crs}$, which is large-amplitude and noise-free synthesized signal, the ISL62881 achieves lower phase jitter than conventional hysteretic mode and fixed PWM mode controllers. Unlike conventional hysteretic mode converters, the ISL62881 has an error amplifier that allows the controller to maintain a 0.5% output voltage accuracy.

Figure 7 shows the operation principles during load insertion response. The COMP voltage rises during load insertion, generating the clock signal more quickly, so the PWM pulse turns on earlier, increasing the effective switching frequency, which allows for higher control loop bandwidth than conventional fixed frequency PWM controllers. The VW voltage rises as the COMP voltage rises, making the PWM pulse wider. During load release response, the COMP voltage falls. It takes the master clock circuit longer to generate the next clock signal so the PWM pulse is held off until needed. The VW voltage falls as the VW voltage falls, reducing the current PWM pulse width. This kind of behavior gives the ISL62881 excellent response speed.

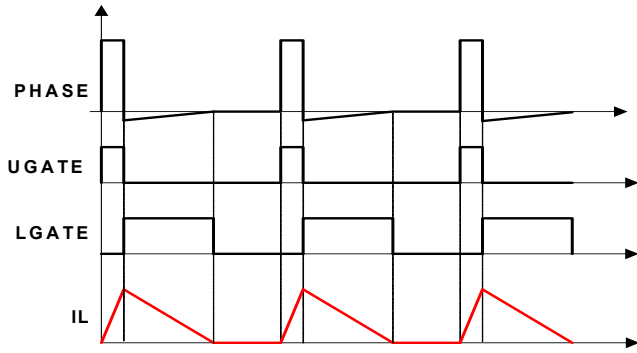## Diode Emulation and Period Stretching



FIGURE 8. DIODE EMULATION

ISL62881 can operate in diode emulation (DE) mode to improve light load efficiency. In DE mode, the low-side MOSFET conducts when the current is flowing from source to drain and doesn't not allow reverse current, emulating a diode. As shown in Figure 8, when LGATE is on, the low-side MOSFET carries current, creating negative voltage on the phase node due to the voltage drop across the ON-resistance. The ISL62881 monitors the current through monitoring the phase node voltage. It turns off LGATE when the phase node voltage reaches zero to prevent the inductor current from reversing the direction and creating unnecessary power loss.

If the load current is light enough, as Figure 9 shows, the inductor current will reach and stay at zero before the next phase node pulse, and the regulator is in discontinuous conduction mode (DCM). If the load current is heavy enough, the inductor current will never reach 0A, and the regulator is in CCM although the controller is in DE mode.
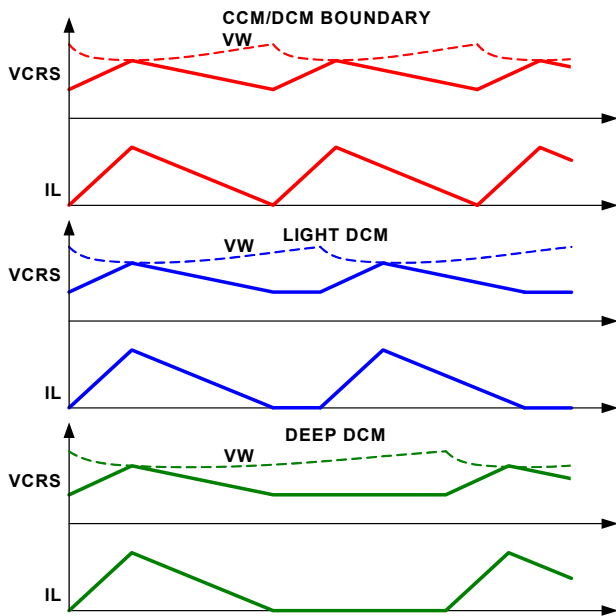


FIGURE 9. PERIOD STRETCHING

Figure 9 shows the operation principle in diode emulation mode at light load. The load gets incrementally lighter in the three cases from top to bottom. The PWM on-time is determined by the VW

window size, therefore is the same, making the inductor current triangle the same in the three cases. The ISL62881 clamps the ripple capacitor voltage $V_{crs}$ in DE mode to make it mimic the inductor current. It takes the COMP voltage longer to hit $V_{crs}$, naturally stretching the switching period. The inductor current triangles move further apart from each other such that the inductor current average value is equal to the load current. The reduced switching frequency helps increase light load efficiency.

## Start-up Timing

With the controller's $V_{DD}$ voltage above the POR threshold, the start-up sequence begins when VR_ON exceeds the 3.3V logic high threshold.

Figure 10 shows the typical start-up timing when the ISL62881 is configured for CPU VR application. The ISL62881 uses digital soft-start to ramp up DAC to the boot voltage of 1.1V at about 2.5mV/μs. Once the output voltage is within 10% of the boot voltage for 13 PWM cycles (43μs for frequency = 300kHz), CLK_EN# is pulled low and DAC slews at 5mV/μs to the voltage set by the VID pins. PGOOD is asserted high in approximately 7ms. Similar results occur if VR_ON is tied to $V_{DD}$, with the soft-start sequence starting 120μs after $V_{DD}$ crosses the POR threshold.

Figure 11 shows the typical start-up timing when the ISL62881 is configured for GPU VR application. The ISL62881 uses digital soft-start to ramp-up DAC to the voltage set by the VID pins at 5mV/μs. Once the output voltage is within 10% of the target voltage for 13 PWM cycles (43μs for frequency = 300kHz), CLK_EN# is pulled low. PGOOD is asserted high in approximately 7ms. Similar results occur if VR_ON is tied to $V_{DD}$, with the soft-start sequence starting 120μs after $V_{DD}$ crosses the POR threshold.
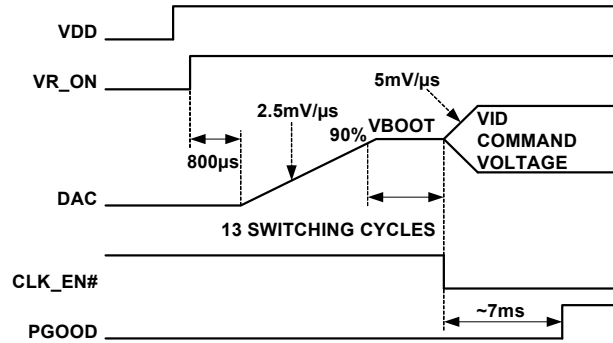


FIGURE 10. SOFT-START WAVEFORMS FOR CPU VR APPLICATION
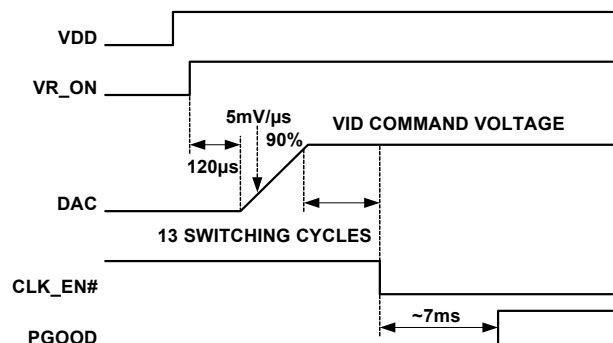


FIGURE 11. SOFT-START WAVEFORMS FOR GPU VR APPLICATION

## Voltage Regulation and Load Line Implementation

After the start sequence, the ISL62881 regulates the output voltage to the value set by the VID inputs per Table 1. The ISL62881 will control the no-load output voltage to an accuracy of ±0.5% over the range of 0.75V to 1.5V. A differential amplifier allows voltage sensing for precise voltage regulation at the microprocessor die.

### TABLE 1.  VID TABLE

| VID6 | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | $V_O$ (V) |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1.5000 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1.4875 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1.4750 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1.4625 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1.4500 |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1.4375 |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1.4250 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1.4125 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1.4000 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1.3875 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1.3750 |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1.3625 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1.3500 |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1.3375 |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1.3250 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1.3125 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1.3000 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1.2875 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1.2750 |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1.2625 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1.2500 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1.2375 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1.2250 |
| 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1.2125 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1.2000 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1.1875 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1.1750 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1.1625 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1.1500 |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1.1375 |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1.1250 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1.1125 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1.1000 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1.0875 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1.0750 |

### TABLE 1.  VID TABLE  (Continued)

| VID6 | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | $V_O$ (V) |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1.0625 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1.0500 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1.0375 |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1.0250 |
| 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1.0125 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1.0000 |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0.9875 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0.9750 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0.9625 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0.9500 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0.9375 |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0.9250 |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0.9125 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0.9000 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0.8875 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0.8750 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0.8625 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0.8500 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0.8375 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0.8250 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0.8125 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0.8000 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0.7875 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0.7750 |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0.7625 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0.7500 |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0.7375 |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0.7250 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0.7125 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0.7000 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0.6875 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0.6750 |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0.6625 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0.6500 |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0.6375 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0.6250 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0.6125 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0.6000 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0.5875 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0.5750 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0.5625 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0.5500 |

TABLE 1. VID TABLE (Continued)

| VID6 | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | $V_O$ (V) |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0.5375 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0.5250 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0.5125 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0.5000 |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0.4875 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0.4750 |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0.4625 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0.4500 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0.4375 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0.4250 |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0.4125 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0.4000 |
| 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0.3875 |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0.3750 |
| 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0.3625 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0.3500 |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0.3375 |
| 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0.3250 |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0.3125 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0.3000 |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0.2875 |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0.2750 |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0.2625 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0.2500 |
| 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0.2375 |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0.2250 |
| 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0.2125 |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0.2000 |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0.1875 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0.1750 |
| 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0.1625 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0.1500 |
| 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0.1375 |
| 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0.1250 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0.1125 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0.1000 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0.0875 |
| 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0.0750 |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0.0625 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0.0500 |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0.0375 |
| 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0.0250 |

TABLE 1. VID TABLE (Continued)

| VID6 | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | $V_O$ (V) |
|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0.0125 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0.0000 |
| 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0.0000 |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0.0000 |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0.0000 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0.0000 |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0.0000 |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0.0000 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0.0000 |
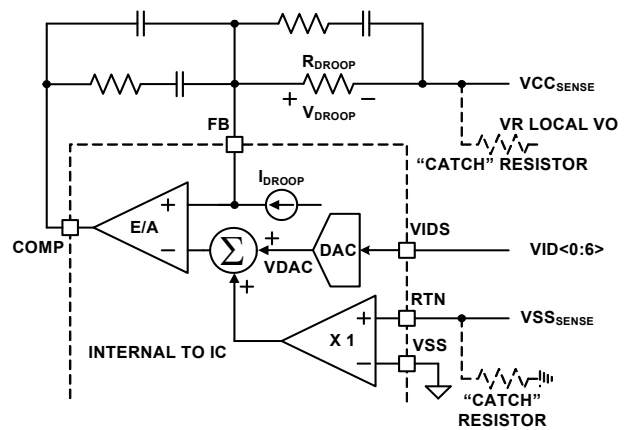


FIGURE 12. DIFFERENTIAL SENSING AND LOAD LINE IMPLEMENTATION

As the load current increases from zero, the output voltage will droop from the VID table value by an amount proportional to the load current to achieve the load line. The ISL62881 can sense the inductor current through the intrinsic DC Resistance (DCR) resistance of the inductors as shown in Figure 1 or through resistors in series with the inductors as shown in Figure 2. In both methods, capacitor $C_n$ voltage represents the inductor total currents. A droop amplifier converts $C_n$ voltage into an internal current source with the gain set by resistor $R_i$. The current source is used for load line implementation, current monitor and overcurrent protection.

Figure 12 shows the load line implementation. The ISL62881 drives a current source $I_{droop}$ out of the FB pin, described by Equation 1.

$$I_{droop} = \frac{2 \times V_{Cn}}{R_i} \tag{EQ. 1}$$

When using inductor DCR current sensing, a single NTC element is used to compensate the positive temperature coefficient of the copper winding thus sustaining the load line accuracy with reduced cost.

$I_{droop}$ flows through resistor $R_{droop}$ and creates a voltage drop, as shown in Equation 2.

$$V_{droop} = R_{droop} \times I_{droop} \tag{EQ. 2}$$

$V_{droop}$ is the droop voltage required to implement load line. Changing $R_{droop}$ or scaling $I_{droop}$ can both change the load line slope. Since $I_{droop}$ also sets the overcurrent protection level, it is recommended to first scale $I_{droop}$ based on OCP requirement, then select an appropriate $R_{droop}$ value to obtain the desired load line slope.

## Differential Sensing

Figure 12 also shows the differential voltage sensing scheme. $VCC_{SENSE}$ and $VSS_{SENSE}$ are the remote voltage sensing signals from the processor die. A unity gain differential amplifier senses the $VSS_{SENSE}$ voltage and adds it to the DAC output. The error amplifier regulates the inverting and the non-inverting input voltages to be equal, therefore:

$$VCC_{SENSE} + V_{droop} = V_{DAC} + VSS_{SENSE} \qquad \text{(EQ. 3)}$$

Rewriting Equation 3 and substituting Equation 2 gives:

$$VCC_{SENSE} - VSS_{SENSE} = V_{DAC} - R_{droop} \times I_{droop} \qquad \text{(EQ. 4)}$$

Equation 4 is the exact equation required for load line implementation.

The $VCC_{SENSE}$ and $VSS_{SENSE}$ signals come from the processor die. The feedback will be open circuit in the absence of the processor. As shown in Figure 12, it is recommended to add a "catch" resistor to feed the VR local output voltage back to the compensator, and add another "catch" resistor to connect the VR local output ground to the RTN pin. These resistors, typically $10\Omega \sim 100\Omega$, will provide voltage feedback if the system is powered up without a processor installed.

## CCM Switching Frequency

The $R_{FSET}$ resistor between the COMP and the VW pins sets the VW windows size, which therefore sets the switching frequency. When the ISL62881 is in continuous conduction mode (CCM), the switching frequency is not absolutely constant due to the nature of the $R3^{TM}$ modulator. As explained in "Multiphase R3™ Modulator" on page 12, the effective switching frequency will increase during load insertion and will decrease during load release to achieve fast response. On the other hand, the switching frequency is relatively constant at steady state. Variation is expected when the power stage condition, such as input voltage, output voltage, load, etc. changes. The variation is usually less than 15% and doesn't have any significant effect on output voltage ripple magnitude. Equation 5 gives an estimate of the frequency-setting resistor $R_{fset}$ value. $8k\Omega$ $R_{FSET}$ gives approximately 300kHz switching frequency. Lower resistance gives higher switching frequency.

$$R_{FSET}(k\Omega) = (Period(\mu s) - 0.29) \times 2.65 \qquad \text{(EQ. 5)}$$

## Modes of Operation

TABLE 2.  ISL62881 MODES OF OPERATION

| CONFIGURATION | DPRSLPVR | OPERATIONAL MODE | VOLTAGE SLEW RATE |
|---|---|---|---|
| CPU VR Application | 0 | 1-phase CCM | 5mV/µs |
| | 1 | 1-phase DE | |
| GPU VR Application | 0 | 1-phase CCM | 5mV/µs |
| | 1 | 1-phase DE | 10mV/µs |

Table 2 shows the ISL62881 operational modes, programmed by the logic status of the DPRSLPVR pin. The ISL62881 enters 1-phase DE mode when there is DPRSLPVR = 1.

When the ISL62881 is configured for GPU VR application, DPRSLPVR logic status also controls the output voltage slew rate. The slew rate is 5mV/µs for DPRSLPVR = 0 and is 10mV/µs for DPRSLPVR = 1.

## Dynamic Operation

When the ISL62881 is configured for CPU VR application, it responds to VID changes by slewing to the new voltage at 5mV/µs slew rate. As the output approaches the VID command voltage, the dv/dt moderates to prevent overshoot. Geyserville-III transitions commands one LSB VID step (12.5mV) every 2.5µs, controlling the effective dv/dt at 5mv/µs. The ISL62881 is capable of 5mV/µs slew rate.

When the ISL62881 is configured for GPU VR application, it responds to VID changes by slewing to the new voltage at a slew rate set by the logic status on the DPRSLPVR pin. The slew rate is 5mV/µs when DPRSLPVR = 0 and is 10mV/µs when DPRSLPVR = 1.

When the ISL62881 is in DE mode, it will actively drive the output voltage up when the VID changes to a higher value. It'll resume DE mode operation after reaching the new voltage level. If the load is light enough to warrant DCM, it will enter DCM after the inductor current has crossed zero for four consecutive cycles. The ISL62881 will remain in DE mode when the VID changes to a lower value. The output voltage will decay to the new value and the load will determine the slew rate.

The $R3^{TM}$ modulator intrinsically has voltage feed forward. The output voltage is insensitive to a fast slew rate input voltage change.

## Protections

The ISL62881 provides overcurrent, undervoltage, and overvoltage protections.

The ISL62881 determines overcurrent protection (OCP) by comparing the average value of the droop current $I_{droop}$ with an internal current source threshold. It declares OCP when $I_{droop}$ is above the threshold for 120µs. A resistor $R_{comp}$ from the COMP pin to GND programs the OCP current source threshold, as well as the overshoot reduction function (to be discussed in later sections), as Table 3 shows. It is recommended to use the nominal $R_{comp}$ value. The ISL62881 detects the $R_{comp}$ value at the beginning of start-up, and sets the internal OCP threshold accordingly. It remembers the $R_{comp}$ value until the VR_ON signal drops below the POR threshold.

### TABLE 3. ISL62881 OCP THRESHOLD AND OVERSHOOT REDUCTION FUNCTION

| $R_{comp}$ | | | OCP THRESHOLD (µA) | OVERSHOOT REDUCTION FUNCTION |
| MIN (k$\Omega$) | NOMINAL (k$\Omega$) | MAX (k$\Omega$) | | |
|---|---|---|---|---|
| | none | none | 20 | Disabled |
| 305 | 400 | 410 | 22.67 | |
| 205 | 235 | 240 | 20.67 | |
| 155 | 165 | 170 | 18 | |
| 104 | 120 | 130 | 20 | Enabled |
| 78 | 85 | 90 | 22.67 | |
| 62 | 66 | 68 | 20.67 | |
| 45 | 50 | 55 | 18 | |

The default OCP threshold is the value when $R_{comp}$ is not populated. It is recommended to scale the droop current $I_{droop}$ such that the default OCP threshold gives approximately the desired OCP level, then use $R_{comp}$ to fine tune the OCP level if necessary.

For overcurrent condition above 2.5x the OCP level, the PWM output will immediately shut off and PGOOD will go low to maximize protection. This protection is also referred to as way-overcurrent protection or fast-overcurrent protection, for short-circuit protections.

The ISL62881 will declare undervoltage (UV) fault and latch-off if the output voltage is less than the VID set value by 300mV or more for 1ms. It'll turn off the PWM output and de-assert PGOOD.

The ISL62881 has two levels of overvoltage protections. The first level of overvoltage protection is referred to as PGOOD overvoltage protection. If the output voltage exceeds the VID set value by +200mV for 1ms, the ISL62881 will declare a fault and de-assert PGOOD.

The ISL62881 takes the same actions for all of the above fault protections: de-assertion of PGOOD and turn-off of the high-side and low-side power MOSFETs. Any residual inductor current will decay through the MOSFET body diodes. These fault conditions can be reset by bringing VR_ON low or by bringing $V_{DD}$ below the POR threshold. When VR_ON and $V_{DD}$ return to their high operating levels, a soft-start will occur.

The second level of overvoltage protection is different. If the output voltage exceeds 1.55V, the ISL62881 will immediately declare an OV fault, de-assert PGOOD, and turn on the low-side power MOSFETs. The low-side power MOSFETs remain on until the output voltage is pulled down below 0.85V when all power MOSFETs are turned off. If the output voltage rises above 1.55V again, the protection process is repeated. This behavior provides the maximum amount of protection against shorted high-side power MOSFETs while preventing output ringing below ground. Resetting VR_ON cannot clear the 1.55V OVP. Only resetting $V_{DD}$ will clear it. The 1.55V OVP is active all the time when the controller is enabled, even if one of the other faults have been declared. This ensures that the processor is protected against high-side power MOSFET leakage while the MOSFETs are commanded off.

Table 4 summarizes the fault protections.

### TABLE 4. FAULT PROTECTION SUMMARY

| FAULT TYPE | FAULT DURATION BEFORE PROTECTION | PROTECTION ACTION | FAULT RESET |
|---|---|---|---|
| Overcurrent | 120µs | PWM tri-state, PGOOD latched low | VR_ON toggle or VDD toggle |
| Way-Overcurrent (2.5xOC) | <2µs | | |
| Overvoltage +200mV | 1ms | | |
| Undervoltage -300mV | | | |
| Overvoltage 1.55V | Immediately | Low-side MOSFET on until $V_{core}$ <0.85V, then PWM tri-state, PGOOD latched low. | VDD toggle |

## Current Monitor

The ISL62881 provides the current monitor function. The IMON pin outputs a high-speed analog current source that is 3 times of the droop current flowing out of the FB pin. Thus as shown by Equation 6.

$$I_{IMON} = 3 \times I_{droop} \qquad \text{(EQ. 6)}$$

As Figures 1 and 2 show, a resistor $R_{imon}$ is connected to the IMON pin to convert the IMON pin current to voltage. A capacitor can be paralleled with $R_{imon}$ to filter the voltage information. The IMVP-6.5™ specification requires that the IMON voltage information be referenced to $VSS_{SENSE}$.

The IMON pin voltage range is 0V to 1.1V. A clamp circuit prevents the IMON pin voltage from going above 1.1V.

## Adaptive Body Diode Conduction Time Reduction

In DCM, the controller turns off the low-side MOSFET when the inductor current approaches zero. During on-time of the low-side MOSFET, phase voltage is negative and the amount is the MOSFET $R_{DS(ON)}$ voltage drop, which is proportional to the inductor current. A phase comparator inside the controller monitors the phase voltage during on-time of the low-side MOSFET and compares it with a threshold to determine the zero-crossing point of the inductor current. If the inductor current has not reached zero when the low-side MOSFET turns off, it'll flow through the low-side MOSFET body diode, causing the phase node to have a larger voltage drop until it decays to zero. If the inductor current has crossed zero and reversed the direction when the low-side MOSFET turns off, it'll flow through the high-side MOSFET body diode, causing the phase node to have a spike until it decays to zero. The controller continues monitoring the phase voltage after turning off the low-side MOSFET and adjusts the phase comparator threshold voltage accordingly in iterative steps such that the low-side MOSFET body diode conducts for approximately 40ns to minimize the body diode-related loss.

## Overshoot Reduction Function

The ISL62881 has an optional overshoot reduction function, enabled or disabled by the resistor from the COMP pin to GND, as shown in Table 3.

When a load release occurs, the energy stored in the inductors will dump to the output capacitor, causing output voltage overshoot. The inductor current freewheels through the low-side MOSFET during this period of time. The overshoot reduction function turns off the low-side MOSFET during the output voltage overshoot, forcing the inductor current to freewheel through the low-side MOSFET body diode. Since the body diode voltage drop is much higher than MOSFET $R_{DS(ON)}$ voltage drop, more energy is dissipated on the low-side MOSFET therefore the output voltage overshoot is lower.

If the overshoot reduction function is enabled, the ISL62881 monitors the COMP pin voltage to determine the output voltage overshoot condition. The COMP voltage will fall and hit the clamp voltage when the output voltage overshoots. The ISL62881 will turn off LGATE when COMP is being clamped. The low-side MOSFET in the power stage will be turned off. When the output voltage has reached its peak and starts to come down, the COMP voltage starts to rise and is no longer clamped. The ISL62881 will resume normal PWM operation.

While the overshoot reduction function reduces the output voltage overshoot, energy is dissipated on the low-side MOSFET, causing additional power loss. The more frequent the transient event, the more power loss is dissipated on the low-side MOSFET. The MOSFET may face severe thermal stress when transient events happen at a high repetitive rate. User discretion is advised when this function is enabled.

# Key Component Selection

## $R_{BIAS}$

The ISL62881 uses a resistor (1% or better tolerance is recommended) from the RBIAS pin to GND to establish highly accurate reference current sources inside the IC. Using $R_{BIAS}$ = 147kΩ sets the controller for CPU core application and using $R_{BIAS}$ = 47kΩ sets the controller for GPU core application. Do not connect any other components to this pin. Do not connect any capacitor to the RBIAS pin as it will create instability.

Care should be taken in layout that the resistor is placed very close to the RBIAS pin and that a good quality signal ground is connected to the opposite side of the $R_{BIAS}$ resistor.

## $R_{is}$ and $C_{is}$

As Figures 1 and 2 show, the ISL62881 needs the $R_{is}$ - $C_{is}$ network across the ISUM+ and the ISUM- pins to stabilize the droop amplifier. The preferred values are $R_{is}$ = 82.5Ω and $C_{is}$ = 0.01μF. Slight deviations from the recommended values are acceptable. Large deviations may result in instability.

## Inductor DCR Current-Sensing Network
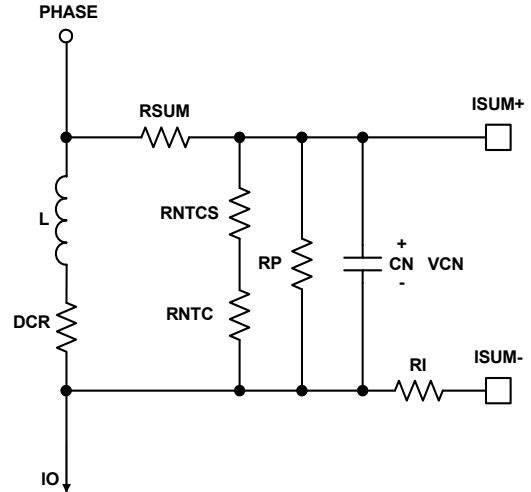


FIGURE 13. DCR CURRENT-SENSING NETWORK

Figure 13 shows the inductor DCR current-sensing network for a 2-phase solution. An inductor current flows through the DCR and creates a voltage drop. The inductor has a resistors in $R_{sum}$ connected to the phase-node-side pad and a PCB trace connected to the output-side pad to accurately sense the inductor current by sensing the DCR voltage drop. The sensed current information is fed to the NTC network (consisting of $R_{ntcs}$, $R_{ntc}$ and $R_p$) and capacitor $C_n$. $R_{ntc}$ is a negative temperature coefficient (NTC) thermistor, used to temperature-compensate the inductor DCR change. The inductor current information is presented to the capacitor $C_n$. Equations 7 through 11 describe the frequency-domain relationship between inductor total current $I_o(s)$ and $C_n$ voltage $V_{Cn}(s)$:

$$V_{Cn}(s) = \left( \frac{R_{ntcnet}}{R_{ntcnet} + R_{sum}} \times DCR \right) \times I_o(s) \times A_{cs}(s) \qquad \text{(EQ. 7)}$$

$$R_{ntcnet} = \frac{(R_{ntcs} + R_{ntc}) \times R_p}{R_{ntcs} + R_{ntc} + R_p} \qquad \text{(EQ. 8)}$$

$$A_{cs}(s) = \frac{1 + \dfrac{s}{\omega_L}}{1 + \dfrac{s}{\omega_{sns}}} \qquad \text{(EQ. 9)}$$

$$\omega_L = \frac{DCR}{L} \qquad \text{(EQ. 10)}$$

$$\omega_{sns} = \frac{1}{\dfrac{R_{ntcnet} \times R_{sum}}{R_{ntcnet} + R_{sum}} \times C_n} \qquad \text{(EQ. 11)}$$

Transfer function $A_{cs}(s)$ always has unity gain at DC. The inductor DCR value increases as the winding temperature increases, giving higher reading of the inductor DC current. The NTC $R_{ntc}$ values decreases as its temperature decreases. Proper selections of $R_{sum}$, $R_{ntcs}$, $R_p$ and $R_{ntc}$ parameters ensure that $V_{Cn}$ represents the inductor total DC current over the temperature range of interest.

There are many sets of parameters that can properly temperature-compensate the DCR change. Since the NTC network and the $R_{sum}$ resistors form a voltage divider, $V_{cn}$ is always a fraction of the inductor DCR voltage. It is recommended to have a higher ratio of $V_{cn}$ to the inductor DCR voltage, so the droop circuit has higher signal level to work with.

A typical set of parameters that provide good temperature compensation are: $R_{sum}$ = 3.65kΩ, $R_p$ = 11kΩ, $R_{ntcs}$ = 2.61kΩ and $R_{ntc}$ = 10kΩ (ERT-J1VR103J). The NTC network parameters may need to be fine tuned on actual boards. One can apply full load DC current and record the output voltage reading immediately; then record the output voltage reading again when the board has reached the thermal steady state. A good NTC network can limit the output voltage drift to within 2mV. It is recommended to follow the Intersil evaluation board layout and current-sensing network parameters to minimize engineering time.

$V_{cn}(s)$ also needs to represent real-time $I_o(s)$ for the controller to achieve good transient response. Transfer function $A_{cs}(s)$ has a pole $\omega_{sns}$ and a zero $\omega_L$. One needs to match $\omega_L$ and $\omega_{sns}$ so $A_{cs}(s)$ is unity gain at all frequencies. By forcing $\omega_L$ equal to $\omega_{sns}$ and solving for the solution, Equation 12 gives $C_n$ value.

$$C_n = \frac{L}{\dfrac{R_{ntcnet} \times R_{sum}}{R_{ntcnet} + R_{sum}} \times DCR} \qquad \text{(EQ. 12)}$$
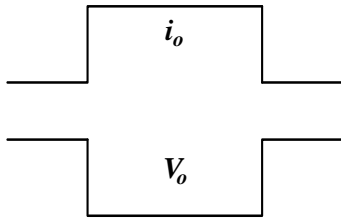


FIGURE 14. DESIRED LOAD TRANSIENT RESPONSE WAVEFORMS
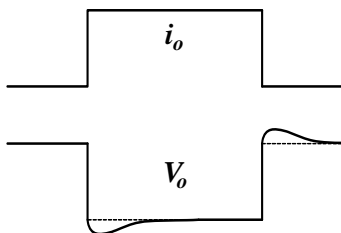


FIGURE 15. LOAD TRANSIENT RESPONSE WHEN $C_n$ IS TOO SMALL
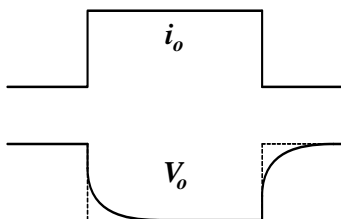


FIGURE 16. LOAD TRANSIENT RESPONSE WHEN $C_n$ IS TOO LARGE

For example, given $R_{sum}$ = 3.65kΩ, $R_p$ = 11kΩ, $R_{ntcs}$ = 2.61kΩ, $R_{ntc}$ = 10kΩ, DCR = 1.1mΩ and L = 0.45µH, Equation 12 gives $C_n$ = 0.18µF.

Assuming the compensator design is correct, Figure 14 shows the expected load transient response waveforms if $C_n$ is correctly selected. When the load current $I_{core}$ has a square change, the output voltage $V_{core}$ also has a square response.

If $C_n$ value is too large or too small, $V_{cn}(s)$ will not accurately represent real-time $I_o(s)$ and will worsen the transient response. Figure 15 shows the load transient response when $C_n$ is too small. $V_{core}$ will sag excessively upon load insertion and may create a system failure. Figure 16 shows the transient response when $C_n$ is too large. $V_{core}$ is sluggish in drooping to its final value. There will be excessive overshoot if load insertion occurs during this time, which may potentially hurt the CPU reliability.
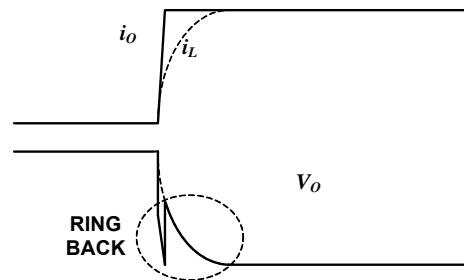


FIGURE 17. OUTPUT VOLTAGE RING BACK PROBLEM
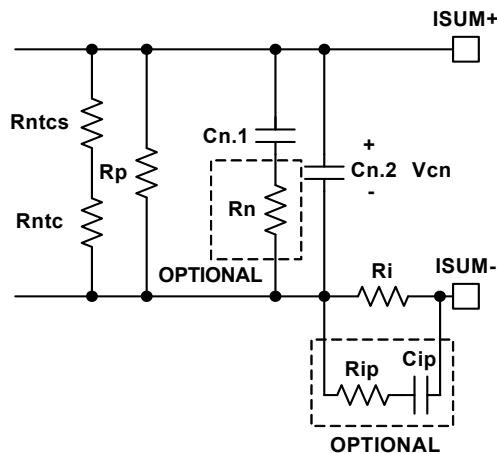


FIGURE 18. OPTIONAL CIRCUITS FOR RING BACK REDUCTION

Figure 17 shows the output voltage ring back problem during load transient response. The load current $i_o$ has a fast step change, but the inductor current $i_L$ cannot accurately follow. Instead, $i_L$ responds in first order system fashion due to the nature of current loop. The ESR and ESL effect of the output capacitors makes the output voltage $V_o$ dip quickly upon load current change. However, the controller regulates $V_o$ according to the droop current $i_{droop}$, which is a real-time representation of $i_L$; therefore it pulls $V_o$ back to the level dictated by $i_L$, causing the ring back problem. This phenomenon is not observed when the output capacitors have very low ESR and ESL, such as all ceramic capacitors.

Figure 18 shows two optional circuits for reduction of the ring back. $R_{ip}$ and $C_{ip}$ form an R-C branch in parallel with $R_i$, providing a lower impedance path than $R_i$ at the beginning of $i_o$ change. $R_{ip}$ and $C_{ip}$ do not have any effect at steady state. Through proper selection of $R_{ip}$ and $C_{ip}$ values, $i_{droop}$ can resemble $i_o$ rather than $i_L$, and $V_O$ will not ring back. The recommended value for $R_{ip}$ is 100W. $C_{ip}$ should be determined through tuning the load transient response waveforms on an actual board. The recommended range for $C_{ip}$ is 100pF~2000pF.

$C_n$ is the capacitor used to match the inductor time constant. It usually takes the parallel of two (or more) capacitors to get the desired value. Figure 18 shows that two capacitors $C_{n.1}$ and $C_{n.2}$ are in parallel. Resistor $R_n$ is an optional component to reduce the $V_O$ ring back. At steady state, $C_{n.1} + C_{n.2}$ provides the desired $C_n$ capacitance. At the beginning of $i_o$ change, the effective capacitance is less because $R_n$ increases the impedance of the $C_{n.1}$ branch. As Figure 15 explains, $V_O$ tends to dip when $C_n$ is too small, and this effect will reduce the $V_O$ ring back. This effect is more pronounced when $C_{n.1}$ is much larger than $C_{n.2}$. It is also more pronounced when $R_n$ is bigger. However, the presence of $R_n$ increases the ripple of the $V_n$ signal if $C_{n.2}$ is too small. It is recommended to keep $C_{n.2}$ greater than 2200pF. $R_n$ value usually is a few ohms. $C_{n.1}$, $C_{n.2}$ and $R_n$ values should be determined through tuning the load transient response waveforms on an actual board.

$R_{ip}$ and $C_{ip}$ form an R-C branch in parallel with $R_i$, providing a lower impedance path than $R_i$ at the beginning of $i_o$ change. $R_{ip}$ and $C_{ip}$ do not have any effect at steady state. Through proper selection of $R_{ip}$ and $C_{ip}$ values, $i_{droop}$ can resemble $i_o$ rather than $i_L$, and $V_O$ will not ring back. The recommended value for $R_{ip}$ is 100$\Omega$. $C_{ip}$ should be determined through tuning the load transient response waveforms on an actual board. The recommended range for $C_{ip}$ is 100pF~2000pF. However, it should be noted that the $R_{ip}$-$C_{ip}$ branch may distort the $i_{droop}$ waveform. Instead of being triangular as the real inductor current, $i_{droop}$ may have sharp spikes, which may adversely affect $i_{droop}$ average value detection and therefore may affect OCP accuracy. User discretion is advised.

## Resistor Current-Sensing Network
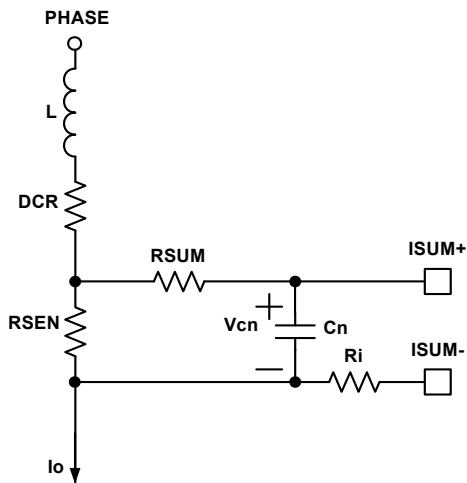


**FIGURE 19.  RESISTOR CURRENT-SENSING NETWORK**

Figure 19 shows the resistor current-sensing network. The inductor has a series current-sensing resistor $R_{sen}$. $R_{sum}$ and is connected to the $R_{sen}$ pad to accurately capture the inductor current information. The $R_{sum}$ feeds the sensed information to capacitor $C_n$. $R_{sum}$ and $C_n$ form a a filter for noise attenuation. Equations 13 through 15 gives $V_{Cn}(s)$ expressions:

$$V_{Cn}(s) = R_{sen} \times I_o(s) \times A_{Rsen}(s) \qquad \text{(EQ. 13)}$$

$$A_{Rsen}(s) = \frac{1}{1+\dfrac{s}{\omega_{sns}}} \qquad \text{(EQ. 14)}$$

$$\omega_{Rsen} = \frac{1}{R_{sum} \times C_n} \qquad \text{(EQ. 15)}$$

Transfer function $A_{Rsen}(s)$ always has unity gain at DC. Current-sensing resistor $R_{sen}$ value will not have significant variation over-temperature, so there is no need for the NTC network.

The recommended values are $R_{sum}$ = 1k$\Omega$ and $C_n$ = 5600pF.

## Overcurrent Protection

Referring to Equation 1 and Figures 12, 13 and 19, resistor $R_i$ sets the droop current $I_{droop}$. Table 3 shows the internal OCP threshold. It is recommended to design $I_{droop}$ without using the $R_{comp}$ resistor.

For example, the OCP threshold is 20µA. We will design $I_{droop}$ to be 14µA at full load, so the OCP trip level is 1.43x of the full load current.

For inductor DCR sensing, Equation 16 gives the DC relationship of $V_{cn}(s)$ and $I_o(s)$.

$$V_{Cn} = \left( \frac{R_{ntcnet}}{R_{ntcnet}+R_{sum}} \times DCR \right) \times I_o \qquad \text{(EQ. 16)}$$

Substitution of Equation 16 into Equation 1 gives:

$$I_{droop} = \frac{2}{R_i} \times \frac{R_{ntcnet}}{R_{ntcnet}+R_{sum}} \times DCR \times I_o \qquad \text{(EQ. 17)}$$

Therefore:

$$R_i = \frac{2R_{ntcnet} \times DCR \times I_o}{(R_{ntcnet}+R_{sum}) \times I_{droop}} \qquad \text{(EQ. 18)}$$

Substitution of Equation 8 and application of the OCP condition in Equation 18 gives:

$$R_i = \frac{2 \times \dfrac{(R_{ntcs}+R_{ntc}) \times R_p}{R_{ntcs}+R_{ntc}+R_p} \times DCR \times I_{omax}}{\left( \dfrac{(R_{ntcs}+R_{ntc}) \times R_p}{R_{ntcs}+R_{ntc}+R_p} + R_{sum} \right) \times I_{droopmax}} \qquad \text{(EQ. 19)}$$

where $I_{omax}$ is the full load current, $I_{droopmax}$ is the corresponding droop current. For example, given $R_{sum}$ = 3.65k$\Omega$, $R_p$ = 11k$\Omega$, $R_{ntcs}$ = 2.61k$\Omega$, $R_{ntc}$ = 10k$\Omega$, DCR = 1.1m$\Omega$, $I_{omax}$ = 14A and $I_{droopmax}$ = 14µA, Equation 19 gives $R_i$ = 1.36k$\Omega$.

For resistor sensing, Equation 20 gives the DC relationship of $V_{cn}(s)$ and $I_o(s)$.

$$V_{Cn} = R_{sen} \times I_o \qquad \text{(EQ. 20)}$$

Substitution of Equation 20 into Equation 1 gives Equation 21:

$$I_{droop} = \frac{2}{R_i} \times R_{sen} \times I_o \qquad \text{(EQ. 21)}$$

Therefore:

$$R_i = \frac{2R_{sen} \times I_o}{I_{droop}} \qquad \text{(EQ. 22)}$$

Substitution of Equation 22 and application of the OCP condition in Equation 18 gives:

$$R_i = \frac{2R_{sen} \times I_{omax}}{I_{droopmax}} \qquad \text{(EQ. 23)}$$

where $I_{omax}$ is the full load current, $I_{droopmax}$ is the corresponding droop current. For example, given $R_{sen} = 1m\Omega$, $I_{omax} = 14A$ and $I_{droopmax} = 14\mu A$, Equation 23 gives $R_i = 2k\Omega$.

A resistor from COMP to GND can adjust the internal OCP threshold, providing another dimension of fine-tune flexibility. Table 3 shows the detail. It is recommended to scale $I_{droop}$ such that the default OCP threshold gives approximately the desired OCP level, then use $R_{comp}$ to fine tune the OCP level if necessary.

## Load Line Slope

Refer to Figure 12.

For inductor DCR sensing, substitution of Equation 17 into Equation 2 gives the load line slope expression in Equation 24.

$$LL = \frac{V_{droop}}{I_o} = \frac{2R_{droop}}{R_i} \times \frac{R_{ntcnet}}{R_{ntcnet} + R_{sum}} \times DCR \qquad \text{(EQ. 24)}$$

For resistor sensing, substitution of Equation 21 into Equation 2 gives the load line slope expression in Equation 25:

$$LL = \frac{V_{droop}}{I_o} = \frac{2R_{sen} \times R_{droop}}{R_i} \qquad \text{(EQ. 25)}$$

Substitution of Equation 18 and rewriting Equation 24, or substitution of Equation 22 and rewriting Equation 25 gives the same result in Equation 26:

$$R_{droop} = \frac{I_o}{I_{droop}} \times LL \qquad \text{(EQ. 26)}$$

One can use the full load condition to calculate $R_{droop}$. For example, given $I_{omax} = 14A$, $I_{droopmax} = 14\mu A$ and $LL = 7m\Omega$, Equation 26 gives $R_{droop} = 7k\Omega$.

It is recommended to start with the $R_{droop}$ value calculated by Equation 26, and fine tune it on the actual board to get accurate load line slope. One should record the output voltage readings at no load and at full load for load line slope calculation. Reading the output voltage at lighter load instead of full load will increase the measurement error.

## Current Monitor

Referring to Equation 6 for the IMON pin current expression.

Refer to Figures 1 and 2, the IMON pin current flows through $R_{imon}$. The voltage across $R_{imon}$ is shown in Equation 27:

$$V_{Rimon} = 3 \times I_{droop} \times R_{imon} \qquad \text{(EQ. 27)}$$

Rewriting Equation 26 gives Equation 28:

$$I_{droop} = \frac{I_o}{R_{droop}} \times LL \qquad \text{(EQ. 28)}$$

Substitution of Equation 28 into Equation 27 gives Equation 29:

$$V_{Rimon} = \frac{3I_o \times LL}{R_{droop}} \times R_{imon} \qquad \text{(EQ. 29)}$$

Rewriting Equation 29 and application of full load condition gives Equation 30:

$$R_{imon} = \frac{V_{Rimon} \times R_{droop}}{3I_o \times LL} \qquad \text{(EQ. 30)}$$

For example, given $LL = 7m\Omega$, $R_{droop} = 7k\Omega$, $V_{Rimon} = 963mV$ at $I_{omax} = 14A$, Equation 30 gives $R_{imon} = 22.9k\Omega$.

A capacitor $C_{imon}$ can be paralleled with $R_{imon}$ to filter the IMON pin voltage. The $R_{imon}C_{imon}$ time constant is the user's choice. It is recommended to have a time constant long enough such that switching frequency ripples are removed.

## Compensator

Figure 14 shows the desired load transient response waveforms. Figure 20 shows the equivalent circuit of a voltage regulator (VR) with the droop function. A VR is equivalent to a voltage source (= VID) and output impedance $Z_{out}(s)$. If $Z_{out}(s)$ is equal to the load line slope LL, i.e. constant output impedance, in the entire frequency range, $V_o$ will have square response when $I_o$ has a square change.
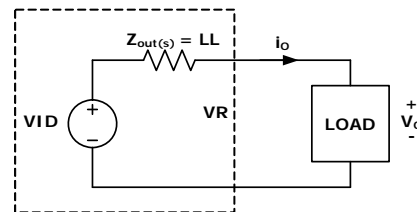


FIGURE 20. VOLTAGE REGULATOR EQUIVALENT CIRCUIT

A VR with active droop function is a dual-loop system consisting of a voltage loop and a droop loop which is a current loop. However, neither loop alone is sufficient to describe the entire system. The spreadsheet shows two loop gain transfer functions, T1(s) and T2(s), that describe the entire system. Figure 21 conceptually shows T1(s) measurement set-up and Figure 22 conceptually shows T2(s) measurement set-up. The VR senses the inductor current, multiplies it by a gain of the load line slope, then adds it on top of the sensed output voltage and feeds it to the compensator. T(1) is measured after the summing node, and T2(s) is measured in the voltage loop before the summing node. The spreadsheet gives both T1(s) and T2(s) plots. However, only T2(s) can be actually measured on an ISL62881 regulator.

T1(s) is the total loop gain of the voltage loop and the droop loop. It always has a higher crossover frequency than T2(s) and has more meaning of system stability.

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T2(s) is the voltage loop gain with closed droop loop. It has more meaning of output voltage response.

Design the compensator to get stable T1(s) and T2(s) with sufficient phase margin, and output impedance equal or smaller than the load line slope.
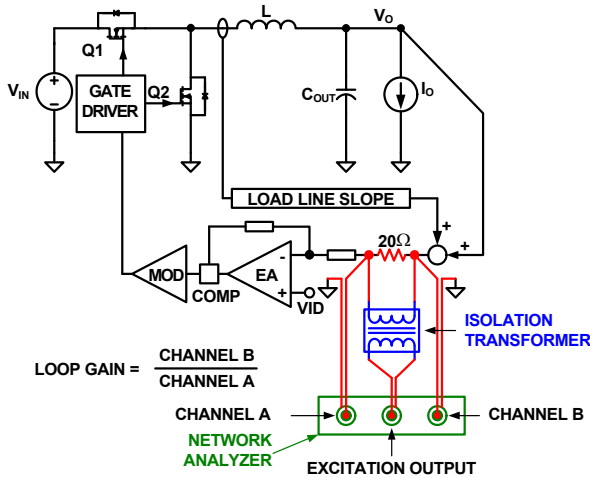


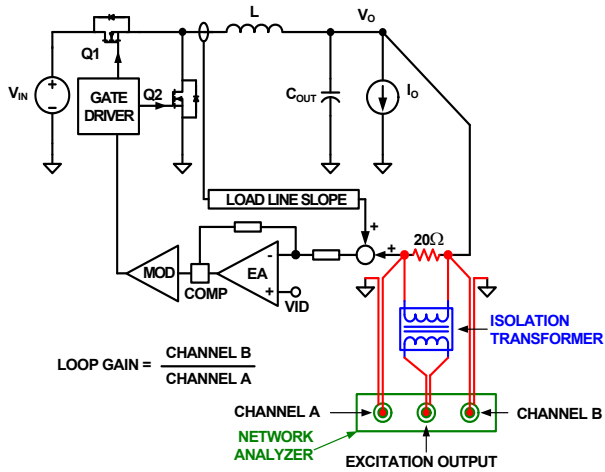FIGURE 21. LOOP GAIN T1(s) MEASUREMENT SET-UP



FIGURE 22. LOOP GAIN T2(s) MEASUREMENT SET-UP

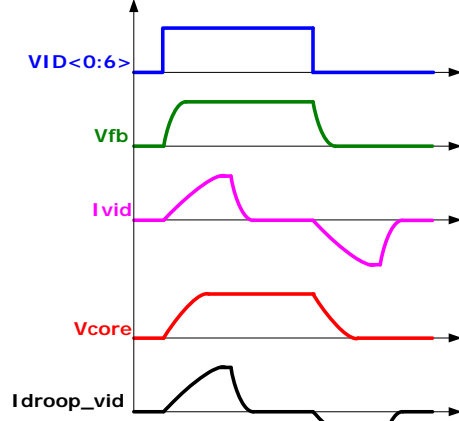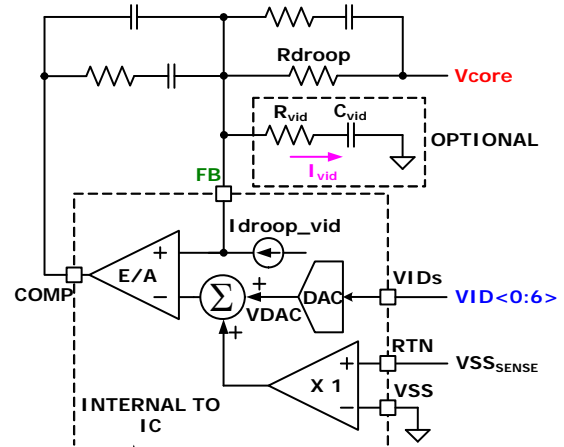## Optional Slew Rate Compensation Circuit For 1-Tick VID Transition



FIGURE 23. OPTIONAL SLEW RATE COMPENSATION CIRCUIT FOR1-TICK VID TRANSITION

During a large VID transition, the DAC steps through the VIDs at a controlled slew rate of 2.5µs or 1.25µs per tick (12.5mV), controlling output voltage $V_{core}$ slew rate at 5mV/µs or 10mV/µs.

Figure 23 shows the waveforms of 1-tick VID transition. During 1-tick VID transition, the DAC output changes at approximately 15mV/µs slew rate, but the DAC cannot step through multiple VIDs to control the slew rate. Instead, the control loop response speed determines $V_{core}$ slew rate. Ideally, $V_{core}$ will follow the FB pin voltage slew rate. However, the controller senses the inductor current increase during the up transition, as the $I_{droop\_vid}$ waveform shows, and will droop the output voltage $V_{core}$ accordingly, making $V_{core}$ slew rate slow. Similar behavior occurs during the down transition.

To control $V_{core}$ slew rate during 1-tick VID transition, one can add the $R_{vid}$-$C_{vid}$ branch, whose current $I_{vid}$ cancels $I_{droop\_vid}$.

When $V_{core}$ increases, the time domain expression of the induced $I_{droop}$ change is as shown in Equation 31:

$$I_{droop}(t) = \frac{C_{out} \times LL}{R_{droop}} \times \frac{dV_{core}}{dt} \times \left(1 - e^{\frac{-t}{C_{out} \times LL}}\right) \qquad \text{(EQ. 31)}$$

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where $C_{out}$ is the total output capacitance.

In the meantime, the $R_{vid}$-$C_{vid}$ branch current $I_{vid}$ time domain expression is as shown in Equation 32:

$$I_{vid}(t) = C_{vid} \times \frac{dV_{fb}}{dt} \times \left( 1 - e^{\frac{-t}{R_{vid} \times C_{vid}}} \right) \qquad \text{(EQ. 32)}$$

It is desired to let $I_{vid}(t)$ cancel $I_{droop\_vid}(t)$. So there are:

$$C_{vid} \times \frac{dV_{fb}}{dt} = \frac{C_{out} \times LL}{R_{droop}} \times \frac{dV_{core}}{dt} \qquad \text{(EQ. 33)}$$

and:

$$R_{vid} \times C_{vid} = C_{out} \times LL \qquad \text{(EQ. 34)}$$

The result is:

$$R_{vid} = R_{droop} \qquad \text{(EQ. 35)}$$

and:

$$C_{vid} = \frac{C_{out} \times LL}{R_{droop}} \times \frac{\frac{dV_{core}}{dt}}{\frac{dV_{fb}}{dt}} \qquad \text{(EQ. 36)}$$

For example: given LL = 3m$\Omega$, $R_{droop}$ = 4.22k$\Omega$, $C_{out}$ = 1320µF, $dV_{core}/dt$ = 5mV/µs and $dV_{fb}/dt$ = 15mV/µs, Equation 35 gives $R_{vid}$ = 4.22k$\Omega$ and Equation 36 gives $C_{vid}$ = 227pF.

It's recommended to select the calculated $R_{vid}$ value and start with the calculated $C_{vid}$ value and tweak it on the actual board to get the best performance.

During normal transient response, the FB pin voltage is held constant, therefore is virtual ground in small signal sense. The $R_{vid}$-$C_{vid}$ network is between the virtual ground and the real ground, and hence has no affect on transient response.

## Voltage Regulator Thermal Throttling

Figure 24 shows the thermal throttling feature with hysteresis. An NTC network is connected between the NTC pin and GND. At low temperature, SW1 is on and SW2 connects to the 1.20V side. The total current flowing out of the NTC pin is 60µA. The voltage on NTC pin is higher than the threshold voltage of 1.20V and the comparator output is low. VR_TT# is pulled up by the external resistor.
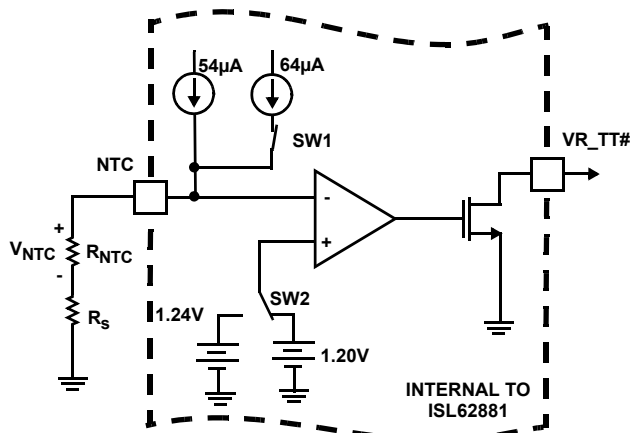


FIGURE 24. CIRCUITRY ASSOCIATED WITH THE THERMAL THROTTLING FEATURE OF THE ISL62881

When temperature increases, the NTC thermistor resistance decreases so the NTC pin voltage drops. When the NTC pin voltage drops below 1.20V, the comparator changes polarity and turns SW1 off and throws SW2 to 1.24V. This pulls VR_TT# low and sends the signal to start thermal throttle. There is a 6µA current reduction on NTC pin and 40mV voltage increase on threshold voltage of the comparator in this state. The VR_TT# signal will be used to change the CPU operation and decrease the power consumption. When the temperature drops down, the NTC thermistor voltage will go up. If NTC voltage increases to above 1.24V, the comparator will flip back. The external resistance difference in these two conditions is shown in Equation 37:

$$\frac{1.24V}{54\mu A} - \frac{1.20V}{60\mu A} = 2.96k \qquad \text{(EQ. 37)}$$

One needs to properly select the NTC thermistor value such that the required temperature hysteresis correlates to 2.96k$\Omega$ resistance change. A regular resistor may need to be in series with the NTC thermistor to meet the threshold voltage values.

For example, given Panasonic NTC thermistor with B = 4700, the resistance will drop to 0.03322 of its nominal at +105°C, and drop to 0.03956 of its nominal at +100°C. If the required temperature hysteresis is +105°C to +100°C, the required resistance of NTC will be as shown in Equation 38:

$$\frac{2.96k\Omega}{(0.03956 - 0.03322)} = 467k\Omega \qquad \text{(EQ. 38)}$$

Therefore, a larger value thermistor such as 470k NTC should be used.

At +105°C, 470k$\Omega$ NTC resistance becomes (0.03322 × 470k$\Omega$) = 15.6k$\Omega$. With 60µA on the NTC pin, the voltage is only (15.6k$\Omega$ × 60µA) = 0.937V. This value is much lower than the threshold voltage of 1.20V. Therefore, a regular resistor needs to be in series with the NTC. The required resistance can be calculated by Equation 39:

$$\frac{1.20V}{60\mu A} - 15.6k\Omega = 4.4k\Omega \qquad \text{(EQ. 39)}$$

4.42k is a standard resistor value. Therefore, the NTC branch should have a 470k NTC and 4.42k resistor in series. The part number for the NTC thermistor is ERTJ0EV474J. It is a 0402 package. NTC thermistor will be placed in the hot spot of the board.

# Layout Guidelines

Table 5 shows the layout considerations. The designators refer to the reference designs shown in Figures 25 and 26.

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**TABLE 5. LAYOUT CONSIDERATIONS**

| NAME | LAYOUT CONSIDERATION |
|---|---|
| GND | Create analog ground plane underneath the controller and the analog signal processing components. Don't let the power ground plane overlap with the analog ground plane. Avoid noisy planes/traces (e.g.: phase node) from crossing over/overlapping with the analog plane. |
| CLK_EN# | No special consideration. |
| PGOOD | No special consideration. |
| RBIAS | Place the $R_{BIAS}$ resistor ($R_{16}$) in general proximity of the controller. Low impedance connection to the analog ground plane. |
| VR_TT# | No special consideration. |
| NTC | The NTC thermistor (R9) needs to be placed close to the thermal source that is monitor to determine thermal throttling. Usually it's placed close to phase-1 high-side MOSFET. |
| VW | Place capacitor (C4) across VW and COMP in close proximity of the controller. |
| COMP | Place compensator components (C3, C5, C6 R7, R11, R10 and C11) in general proximity of the controller. |
| FB | |
| VSEN | Place the VSEN/RTN filter (C12, C13) in close proximity of the controller for good decoupling. |
| RTN | |
| VDD | A capacitor (C16) decouples it to GND. Place it in close proximity of the controller. |
| IMON | Place the filter capacitor (C21) close to the CPU. |
| ISUM- | Place the current sensing circuit in general proximity of the controller. |
| ISUM+ | Place C82 very close to the controller.<br>Place NTC thermistors $R_{42}$ next to inductor (L1) so it senses the inductor temperature correctly.<br>The power stage sends a pair of VSUM+ and VSUM- signals to the controller. Run these two signal traces in parallel fashion with decent width (>20mil).<br>IMPORTANT: Sense the inductor current by routing the sensing circuit to the inductor pads.<br>Route $R_{63}$ to the phase-node side pad of inductor L1. Route the other current sensing trace to the output side pad of inductor L1.<br>If possible, route the traces on a different layer from the inductor pad layer and use vias to connect the traces to the center of the pads. If no via is allowed on the pad, consider routing the traces into the pads from the inside of the inductor. The following drawings show the two preferred ways of routing current sensing traces.<br><br>INDUCTOR VIAS CURRENT-SENSING TRACES / INDUCTOR CURRENT-SENSING TRACES |
| VIN | A capacitor (C17) decouples it to GND. Place it in close proximity of the controller. |
| BOOT | Use decent wide trace (>30mil). Avoid any sensitive analog signal trace from crossing over or getting close. |
| UGATE | Run these two traces in parallel fashion with decent width (>30mil). Avoid any sensitive analog signal trace from crossing over or getting close. Recommend routing PHASE trace to the high-side MOSFET (Q2 and Q8) source pins instead of general phase node copper. |
| PHASE | |
| VSSP | Run these two traces in parallel fashion with decent width (>30mil). Avoid any sensitive analog signal trace from crossing over or getting close. Recommend routing VSSP to the low-side MOSFET (Q3 and Q9) source pins instead of general power ground plane for better performance. |
| LGATE or LGATEa and LGATEb | |
| VCCP | A capacitor (C22) decouples it to GND. Place it in close proximity of the controller. |
| VID0~6 | No special consideration. |
| VR_ON | No special consideration. |
| DPRSLPVR | No special consideration. |
| Phase Node | Minimize phase node copper area. Don't let the phase node copper overlap with/getting close to other sensitive traces. Cut the power ground plane to avoid overlapping with phase node copper. |
| | Minimize the loop consisting of input capacitor, high-side MOSFETs and low-side MOSFETs (e.g.: C27, C33, Q2, Q8, Q3 and Q9). |

**FIGURE 25. GPU APPLICATION REFERENCE DESIGN**
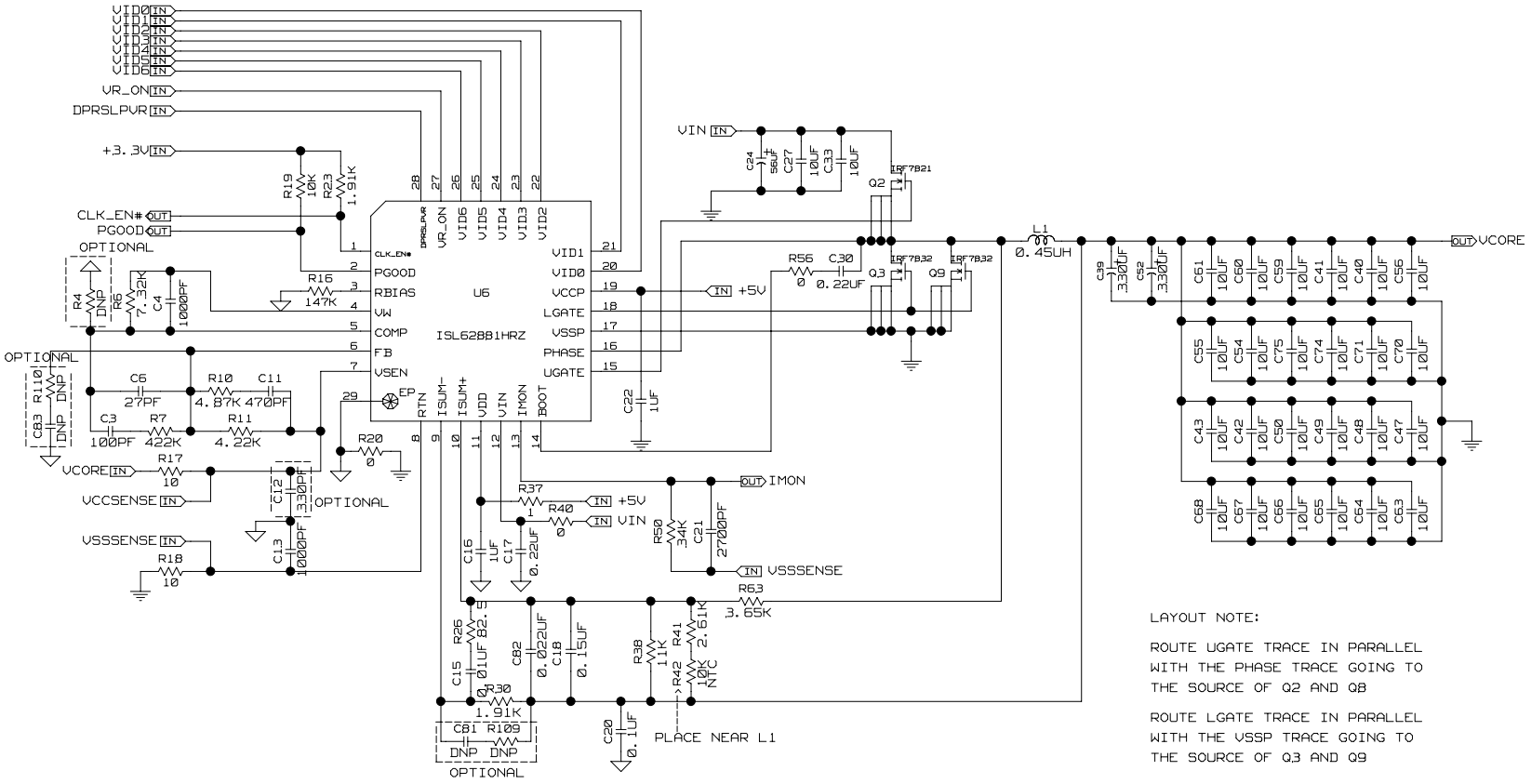
**FIGURE 26. CPU APPLICATION REFERENCE DESIGN**

LAYOUT NOTE:

ROUTE UGATE TRACE IN PARALLEL
WITH THE PHASE TRACE GOING TO
THE SOURCE OF Q2 AND Q8

ROUTE LGATE TRACE IN PARALLEL
WITH THE VSSP TRACE GOING TO
THE SOURCE OF Q3 AND Q9

# CPU Application Reference Design Bill of Materials

| QTY | REFERENCE | VALUE | DESCRIPTION | MANUFACTURER | PART NUMBER | PACKAGE |
|---|---|---|---|---|---|---|
| 1 | C11 | 470pF | Multilayer Cap, 16V, 10% | GENERIC | H1045-00471-16V10 | SM0603 |
| 1 | C12 | 330pF | Multilayer Cap, 16V, 10% | GENERIC | H1045-00331-16V10 | SM0603 |
| 1 | C13 | 1000pF | Multilayer Cap, 16V, 10% | GENERIC | H1045-00102-16V10 | SM0603 |
| 1 | C15 | 0.01µF | Multilayer Cap, 16V, 10% | GENERIC | H1045-00103-16V10 | SM0603 |
| 2 | C16, C22 | 1µF | Multilayer Cap, 16V, 20% | GENERIC | H1045-00105-16V20 | SM0603 |
| 1 | C18 | 0.15µF | Multilayer Cap, 16V, 10% | GENERIC | H1045-00154-16V10 | SM0603 |
| 1 | C20 | 0.1µF | Multilayer Cap, 16V, 10% | GENERIC | H1045-00104-16V10 | SM0603 |
| 1 | C21 | 2700pF | Multilayer Cap, 16V, 10% | GENERIC | H1045-00272-16V10 | SM0603 |
| 2 | C17, C30 | 0.22µF | Multilayer Cap, 25V, 10% | GENERIC | H1045-00224-25V10 | SM0603 |
| 1 | C24 | 56µF | Radial SP Series Cap, 25V, 20% | SANYO | 25SP56M | CASE-CC |
| 2 | C27, C33 | 10µF | Multilayer Cap, 25V, 20% | GENERIC | H1065-00106-25V20 | SM1206 |
| 1 | C3 | 100pF | Multilayer Cap, 16V, 10% | GENERIC | H1045-00101-16V10 | SM0603 |
| 2 | C39, C52 | 330µF | SPCAP, 2V, 4M$\Omega$ | PANASONIC | EEXSX0D331E4 | |
| | | | POLYMER CAP, 2.5V, 4.5M$\Omega$ | KEMET | T520V337M2R5A(1)E4R5-6666 | |
| 1 | C4 | 1000pF | Multilayer Cap, 16V, 10% | GENERIC | H1045-00102-16V10 | SM0603 |
| 30 | C40-C43, C47-C50, C53-C56, C59, C75, C78 | 10µF | Multilayer Cap, 6.3V, 20% | MURATA | GRM21BR61C106KE15L | SM0805 |
| | | | | TDK | C2012X5R0J106K | |
| 1 | C6 | 27pF | Multilayer Cap, 16V, 10% | GENERIC | H1045-00270-16V10 | SM0603 |
| 1 | C82 | 0.022µF | Multilayer Cap, 16V, 10% | GENERIC | H1045-00223-16V10 | SM0603 |
| 0 | C81, C83 | DNP | | | | |
| 1 | L1 | 0.45µH | Inductor, Inductance 20%, DCR 7% | NEC-TOKIN | MPCG1040LR45 | 10mmx10mm |
| 1 | Q2 | | N-Channel Power MOSFET | IR | IRF7821 | PWRPAKSO8 |
| 2 | Q3, Q9 | | N-Channel Power MOSFET | IR | IRF7832 | PWRPAKSO8 |
| 1 | R10 | 4.87k | Thick Film Chip Resistor, 1% | GENERIC | H2511-04871-1/16W1 | SM0603 |
| 1 | R11 | 4.22k | Thick Film Chip Resistor, 1% | GENERIC | H2511-04221-1/16W1 | SM0603 |
| 1 | R16 | 147k | Thick Film Chip Resistor, 1% | GENERIC | H2511-01473-1/16W1 | SM0603 |
| 2 | R17, R18 | 10 | Thick Film Chip Resistor, 1% | GENERIC | H2511-00100-1/16W1 | SM0603 |
| 1 | R19 | 1.91k | Thick Film Chip Resistor, 1% | GENERIC | H2511-01911-1/16W1 | SM0603 |
| 1 | R26 | 82.5 | Thick Film Chip Resistor, 1% | GENERIC | H2511-082R5-1/16W1 | SM0603 |
| 3 | R20, R40, R56 | 0 | Thick Film Chip Resistor, 1% | GENERIC | H2511-00R00-1/16W1 | SM0603 |
| 1 | R30 | 1.91k | Thick Film Chip Resistor, 1% | GENERIC | H2511-01911-1/16W1 | SM0603 |
| 1 | R37 | 1 | Thick Film Chip Resistor, 1% | GENERIC | H2511-01R00-1/16W1 | SM0603 |
| 1 | R38 | 11k | Thick Film Chip Resistor, 1% | GENERIC | H2511-01102-1/16W1 | SM0603 |
| 1 | R41 | 2.61k | Thick Film Chip Resistor, 1% | GENERIC | H2511-02611-1/16W1 | SM0603 |
| 1 | R42 | 10k NTC | Thermistor, 10k NTC | PANASONIC | ERT-J1VR103J | SM0603 |
| 1 | R50 | 34k | Thick Film Chip Resistor, 1% | GENERIC | H2511-03402-1/16W1 | SM0603 |

## CPU Application Reference Design Bill of Materials (Continued)

| QTY | REFERENCE | VALUE | DESCRIPTION | MANUFACTURER | PART NUMBER | PACKAGE |
|---|---|---|---|---|---|---|
| 1 | R6 | 7.32k | Thick Film Chip Resistor, 1% | GENERIC | H2511-07321-1/16W1 | SM0603 |
| 1 | R63 | 3.65k | Thick Film Chip Resistor, 1% | GENERIC | H2511-03651-1/16W1 | SM0805 |
| 1 | R7 | 422k | Thick Film Chip Resistor, 1% | GENERIC | H2511-04223-1/16W1 | SM0603 |
| 0 | R109, R110, R4, R8, R9 | DNP | | | | |
| 1 | U6 | | IMVP-6.5 PWM Controller | INTERSIL | ISL62881HRTZ | QFN-28 |

# GPU Application Reference Design Bill of Materials

| QTY | REFERENCE | VALUE | DESCRIPTION | MANUFACTURER | PART NUMBER | PACKAGE |
|---|---|---|---|---|---|---|
| 1 | C11 | 270pF | Multilayer Cap, 16V, 10% | GENERIC | H1045-00271-16V10 | SM0603 |
| 1 | C12 | 330pF | Multilayer Cap, 16V, 10% | GENERIC | H1045-00331-16V10 | SM0603 |
| 1 | C13 | 1000pF | Multilayer Cap, 16V, 10% | GENERIC | H1045-00102-16V10 | SM0603 |
| 1 | C15 | 0.01µF | Multilayer Cap, 16V, 10% | GENERIC | H1045-00103-16V10 | SM0603 |
| 2 | C16, C22 | 1µF | Multilayer Cap, 16V, 20% | GENERIC | H1045-00105-16V20 | SM0603 |
| 1 | C18 | 0.15µF | Multilayer Cap, 16V, 10% | GENERIC | H1045-00154-16V10 | SM0603 |
| 1 | C20 | 0.1µF | Multilayer Cap, 16V, 10% | GENERIC | H1045-00104-16V10 | SM0603 |
| 2 | C17, C30 | 0.22µF | Multilayer Cap, 25V, 10% | GENERIC | H1045-00224-25V10 | SM0603 |
| 1 | C21 | 3900pF | Multilayer Cap, 16V, 10% | GENERIC | H1045-00392-16V10 | SM0603 |
| 1 | C24 | 56µF | Radial SP Series Cap, 25V, 20% | SANYO | 25SP56M | CASE-CC |
| 2 | C27, C33 | 10µF | Multilayer Cap, 25V, 20% | GENERIC | H1065-00106-25V20 | SM1206 |
| 1 | C3 | 100pF | Multilayer Cap, 16V, 10% | GENERIC | H1045-00101-16V10 | SM0603 |
| 1 | C52 | 470µF | SPCAP, 2V, 4M$\Omega$ | PANASONIC | EEXSX0D471E4 | |
| | | | POLYMER CAP, 2.5V, 4.5M$\Omega$ | KEMET | T520V477M2R5A(1)E4R5-6666 | |
| 1 | C4 | 1000pF | Multilayer Cap, 16V, 10% | GENERIC | H1045-00102-16V10 | SM0603 |
| 8 | C40, C41, C54-C56, C59-C61 | 10µF | Multilayer Cap, 6.3V, 20% | MURATA | GRM21BR61C106KE15L | SM0805 |
| | | | | TDK | C2012X5R0J106K | |
| 1 | C6 | 15pF | Multilayer Cap, 16V, 10% | GENERIC | H1045-00150-16V10 | SM0603 |
| 1 | C82 | 0.056µF | Multilayer Cap, 16V, 10% | GENERIC | H1045-00563-16V10 | SM0603 |
| 0 | C81, C83 | DNP | | | | |
| 1 | L1 | 0.88µH | Inductor, Inductance 20%, DCR 7% | NEC-TOKIN | MPC1040LR88 | 10mmx10mm |
| 1 | Q2 | | N-Channel Power MOSFET | IR | IRF7821 | PWRPAKSO8 |
| 2 | Q3, Q9 | | N-Channel Power MOSFET | IR | IRF7832 | PWRPAKSO8 |
| 1 | R10 | 2.37k | Thick Film Chip Resistor, 1% | GENERIC | H2511-02371-1/16W1 | SM0603 |
| 1 | R11 | 6.98k | Thick Film Chip Resistor, 1% | GENERIC | H2511-06981-1/16W1 | SM0603 |
| 1 | R16 | 47.5k | Thick Film Chip Resistor, 1% | GENERIC | H2511-04752-1/16W1 | SM0603 |
| 2 | R17, R18 | 10 | Thick Film Chip Resistor, 1% | GENERIC | H2511-00100-1/16W1 | SM0603 |
| 1 | R19 | 1.91k | Thick Film Chip Resistor, 1% | GENERIC | H2511-01911-1/16W1 | SM0603 |
| 1 | R26 | 82.5 | Thick Film Chip Resistor, 1% | GENERIC | H2511-082R5-1/16W1 | SM0603 |

## GPU Application Reference Design Bill of Materials (Continued)

| QTY | REFERENCE | VALUE | DESCRIPTION | MANUFACTURER | PART NUMBER | PACKAGE |
|---|---|---|---|---|---|---|
| 3 | R20, R40, R56 | 0 | Thick Film Chip Resistor, 1% | GENERIC | H2511-00R00-1/16W1 | SM0603 |
| 1 | R30 | 3.01k | Thick Film Chip Resistor, 1% | GENERIC | H2511-03011-1/16W1 | SM0603 |
| 1 | R37 | 1 | Thick Film Chip Resistor, 1% | GENERIC | H2511-01R00-1/16W1 | SM0603 |
| 1 | R38 | 11k | Thick Film Chip Resistor, 1% | GENERIC | H2511-01102-1/16W1 | SM0603 |
| 1 | R41 | 2.61k | Thick Film Chip Resistor, 1% | GENERIC | H2511-02611-1/16W1 | SM0603 |
| 1 | R42 | 10k NTC | Thermistor, 10k NTC | PANASONIC | ERT-J1VR103J | SM0603 |
| 1 | R50 | 22.6k | Thick Film Chip Resistor, 1% | GENERIC | H2511-02262-1/16W1 | SM0603 |
| 1 | R6 | 10k | Thick Film Chip Resistor, 1% | GENERIC | H2511-01002-1/16W1 | SM0603 |
| 1 | R63 | 3.65k | Thick Film Chip Resistor, 1% | GENERIC | H2511-03651-1/16W1 | SM0805 |
| 1 | R7 | 412k | Thick Film Chip Resistor, 1% | GENERIC | H2511-04123-1/16W1 | SM0603 |
| 0 | R109, R110, R4, R8, R9 | DNP | | | | |
| 1 | U6 | | IMVP-6.5 PWM Controller | INTERSIL | ISL62881HRTZ | QFN-28 |

# Typical Performance
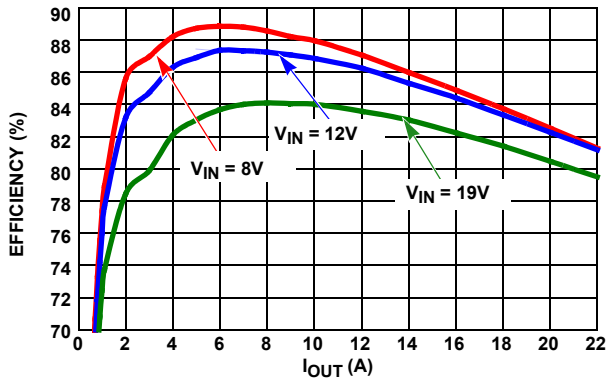


FIGURE 27. CPU APPLICATION CCM EFFICIENCY, VID = 0.9V, $V_{IN1}$ = 8V, $V_{IN2}$ = 12.6V AND $V_{IN3}$ = 19V
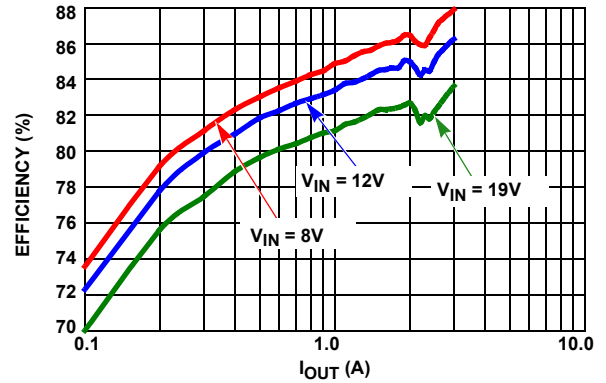


FIGURE 28. CPU APPLICATION DCM EFFICIENCY, VID = 0.9V, $V_{IN1}$ = 8V, $V_{IN2}$ = 12.6V AND $V_{IN3}$ = 19V
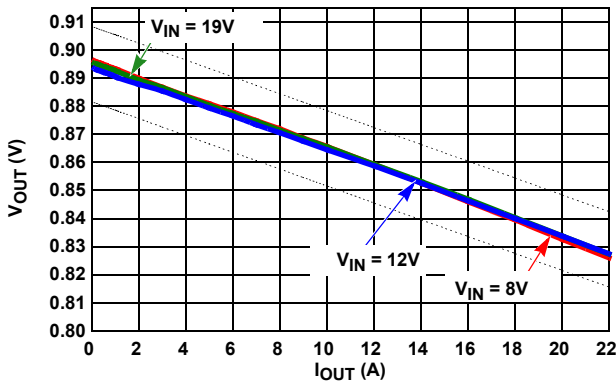


FIGURE 29. CPU APPLICATION CCM LOAD LINE, VID = 0.9V, $V_{IN1}$ = 8V, $V_{IN2}$ = 12.6V AND $V_{IN3}$ = 19V
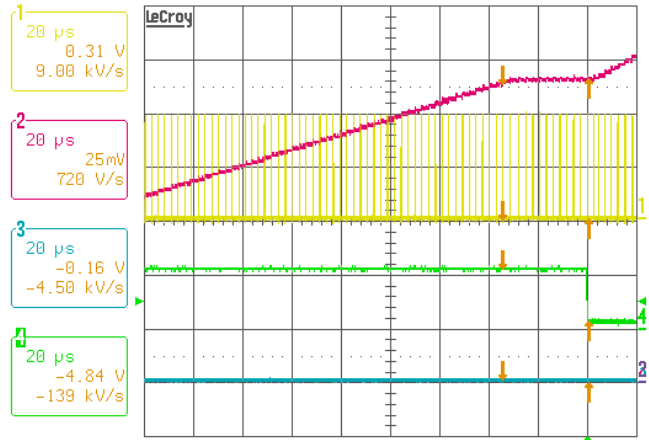


FIGURE 30. CPU MODE CLK_EN# DELAY, $V_{IN}$ = 19V, $I_O$ = 0A, VID = 1.2V, Ch1: PHASE1, Ch2: $V_O$, Ch4: CLK_EN#
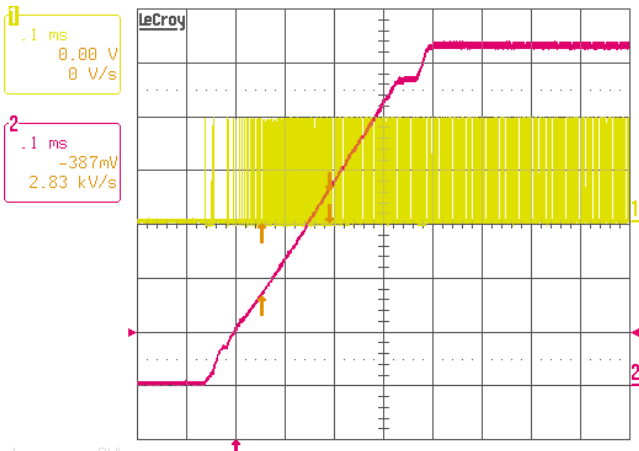


FIGURE 31. CPU MODE SOFT-START, $V_{IN}$ = 19V, $I_O$ = 0A, VID = 1.2V, Ch1: PHASE, Ch2: $V_O$
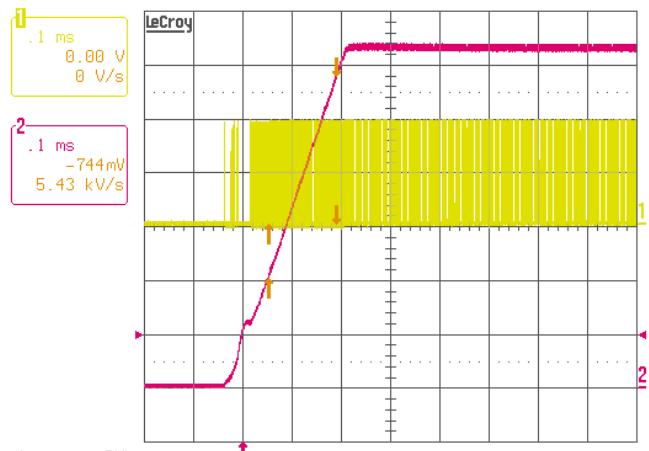


FIGURE 32. GPU MODE SOFT-START, $V_{IN}$ = 19V, $I_O$ = 0A, VID = 1.2V, Ch1: PHASE, Ch2: $V_O$

## Typical Performance (Continued)
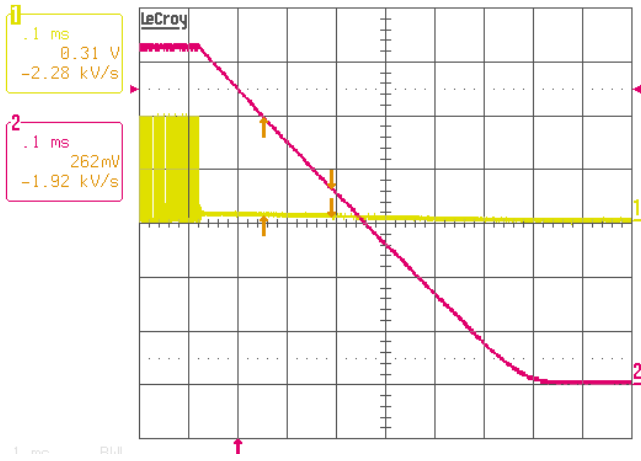


FIGURE 33. CPU MODE SHUT DOWN, $V_{IN}$ = 19V, $I_O$ = 0A, VID = 1.2V, Ch1: PHASE, Ch2: $V_O$
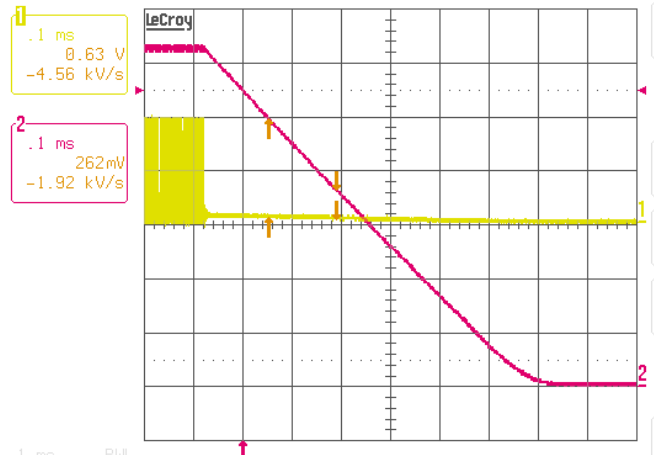


FIGURE 34. GPU MODE SHUT DOWN, $V_{IN}$ = 19V, $I_O$ = 0A, VID = 1.2V, Ch1: PHASE, Ch2: $V_O$
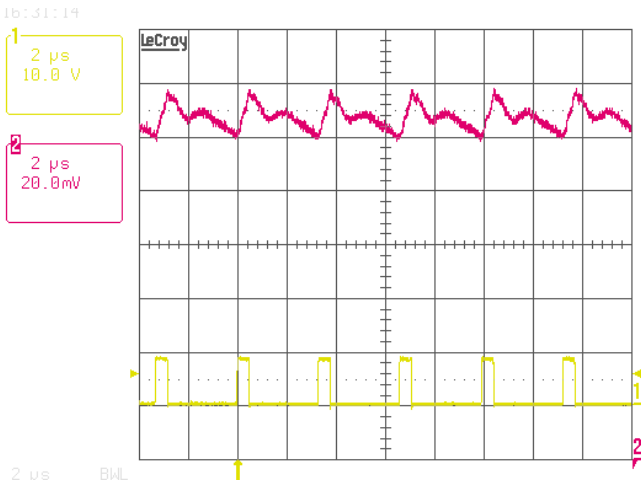


FIGURE 35. CCM STEADY STATE, CPU MODE, $V_{IN}$ = 8V, $I_O$ = 1A, VID = 1.2375V, Ch1: PHASE, Ch2: $V_O$
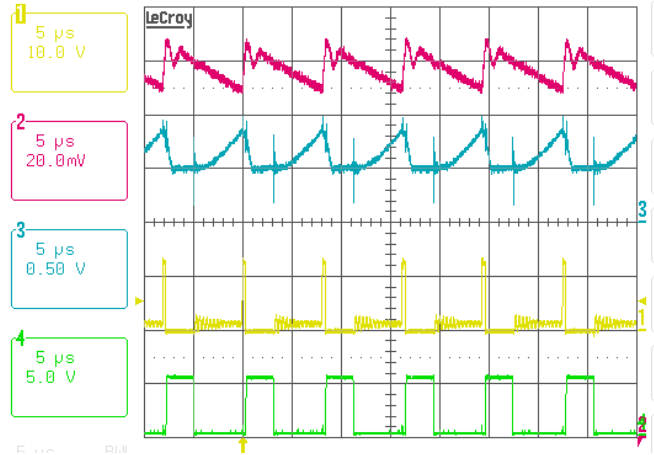


FIGURE 36. DCM STEADY STATE, CPU MODE, $V_{IN}$ = 12V, $I_O$ = 1A, VID = 1.075V, Ch1: PHASE1, Ch2: $V_O$, Ch3: COMP, Ch4: LGATE



FIGURE 37. GPU MODE REFERENCE DESIGN LOOP GAIN T2(s) MEASUREMENT RESULT
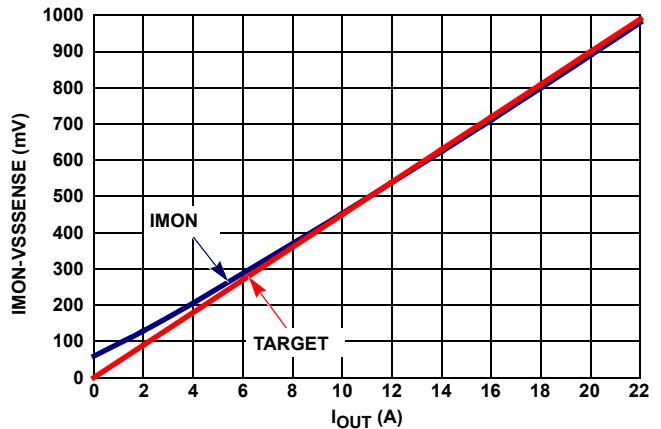


FIGURE 38. IMON, VID = 1.2375

## Typical Performance (Continued)
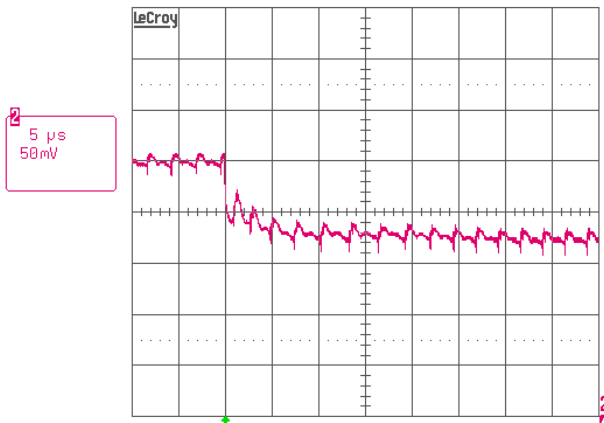


FIGURE 39. LOAD TRANSIENT RESPONSE WITH OVERSHOOT
REDUCTION FUNCTION DISABLED, GPU MODE,
$V_{IN}$ = 12V, VID = 0.9V, $I_O$ = 12A/22A,
di/dt = "FASTEST"
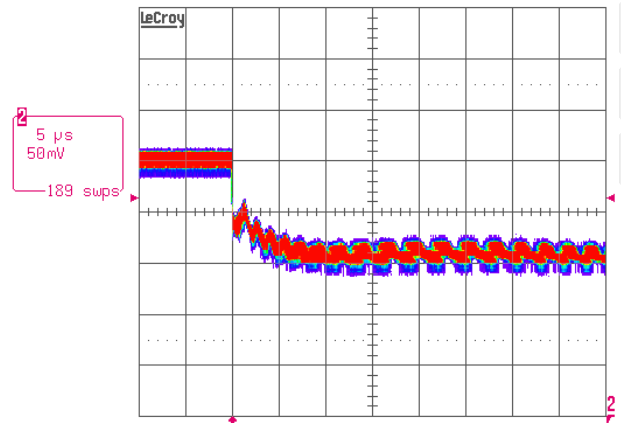


FIGURE 40. LOAD TRANSIENT RESPONSE WITH OVERSHOOT
REDUCTION FUNCTION DISABLED, GPU MODE,
$V_{IN}$ = 12V, VID = 0.9V, $I_O$ = 12A/22A,
di/dt = "FASTEST"
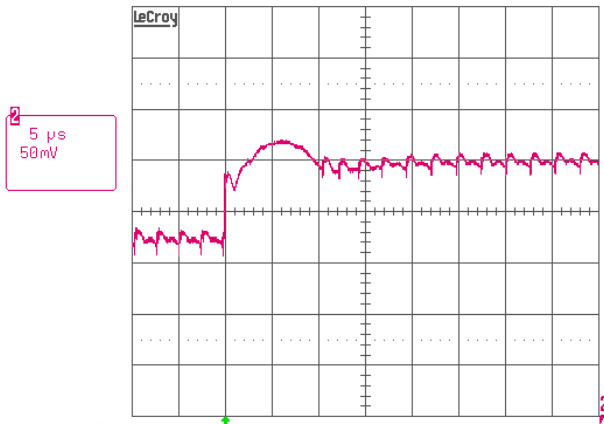


FIGURE 41. LOAD TRANSIENT RESPONSE WITH OVERSHOOT
REDUCTION FUNCTION DISABLED, GPU MODE,
$V_{IN}$ = 12V, VID = 0.9V, $I_O$ = 12A/22A,
di/dt = "FASTEST"
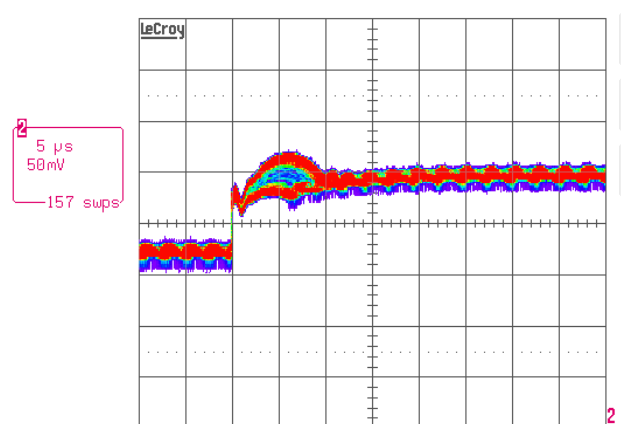


FIGURE 42. LOAD TRANSIENT RESPONSE WITH OVERSHOOT
REDUCTION FUNCTION DISABLED, GPU MODE,
$V_{IN}$ = 12V, VID = 0.9V, $I_O$ = 12A/22A,
di/dt = "FASTEST"
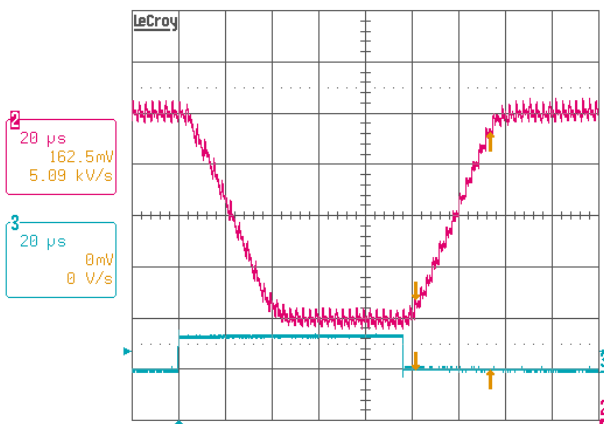


FIGURE 43. CPU MODE VID TRANSITION, DPRSLPVR = 0, $I_O$ = 2A,
VID = 1.2375V/1.0375V, Ch2: $V_O$, Ch3: VID4
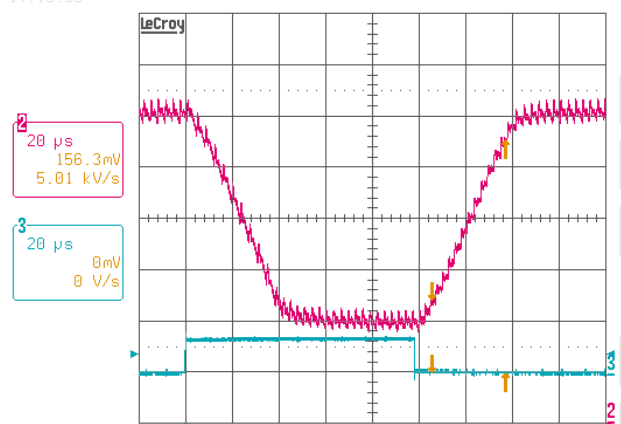


FIGURE 44. GPU MODE VID TRANSITION, DPRSLPVR = 0, $I_O$ = 2A,
VID = 1.2375V/1.0375V, Ch2: $V_O$, Ch3: VID4

## Typical Performance (Continued)
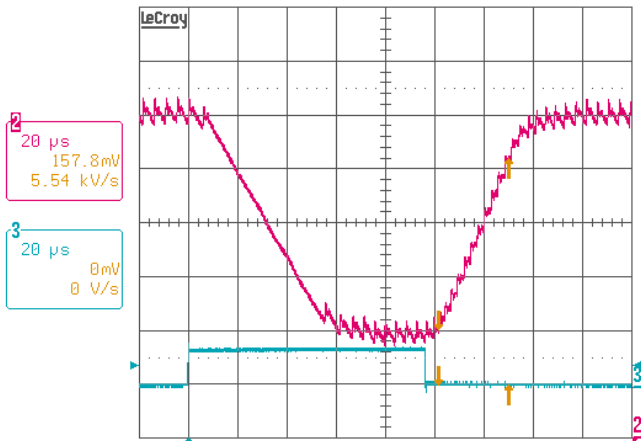


FIGURE 45. CPU MODE VID TRANSITION, DPRSLPVR = 1, $I_O$ = 2A, VID = 1.2375V/1.0375V, Ch2: $V_O$, Ch3: VID4
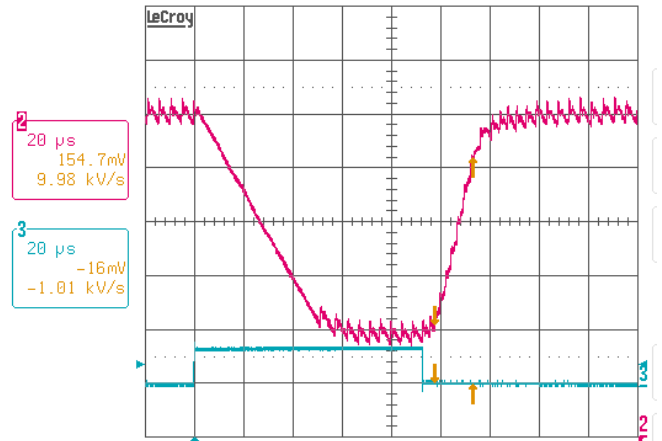


FIGURE 46. GPU MODE VID TRANSITION, DPRSLPVR = 1, $I_O$ = 2A, VID = 1.2375V/1.0375V, Ch2: $V_O$, Ch3: VID4

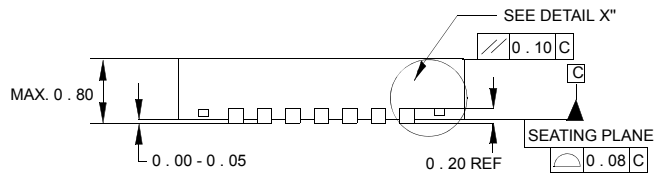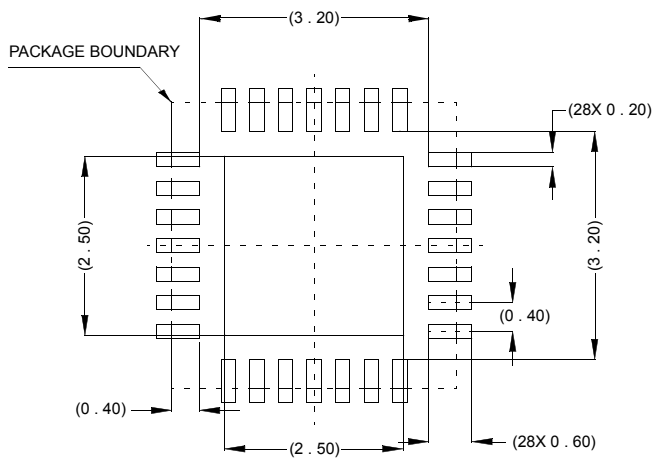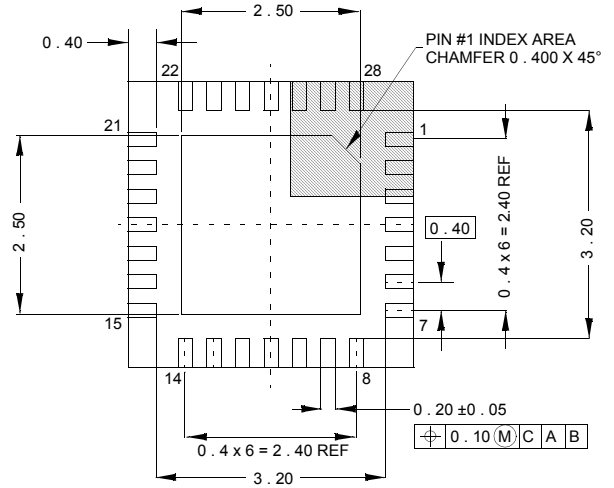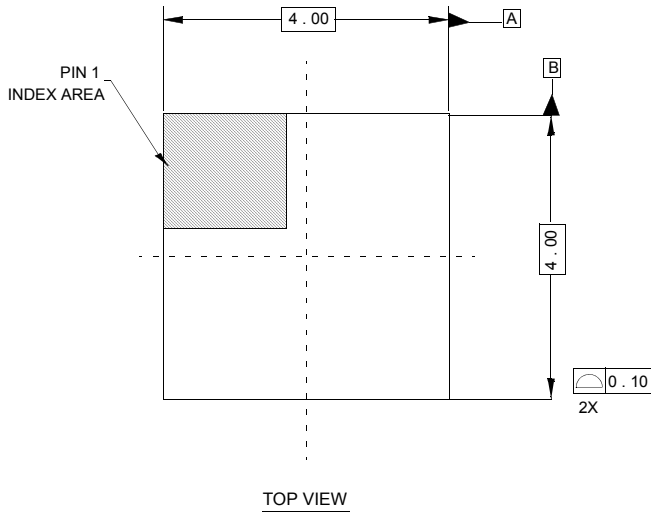For additional products, see www.intersil.com/en/products.html

For information regarding Intersil Corporation and its products, see www.intersil.com

# Package Outline Drawing

## L28.4x4
**28 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE**
**Rev 0, 9/06**



TOP VIEW



BOTTOM VIEW



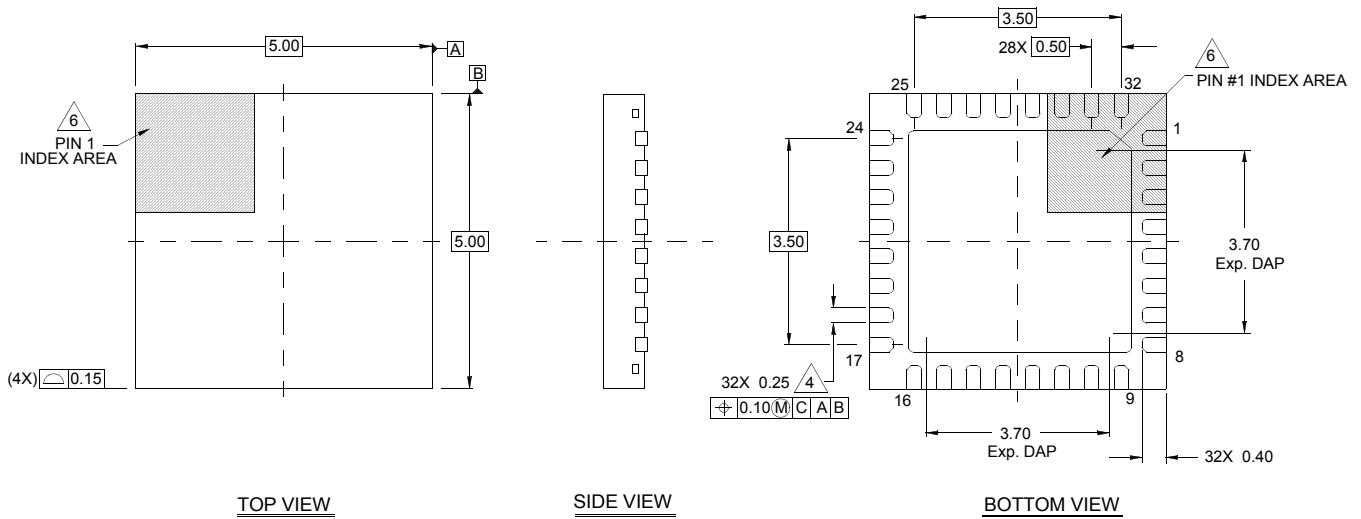TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"
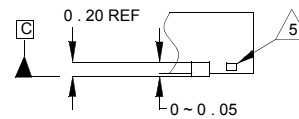
NOTES:
1. Controlling dimensions are in mm.
   Dimensions in ( ) for reference only.
2. Unless otherwise specified, tolerance : Decimal ±0.05
   Angular ±2°
3. Dimensioning and tolerancing conform to AMSE Y14.5M-1994.
4. Bottom side Pin#1 ID is diepad chamfer as shown.
5. Tiebar shown (if present) is a non-functional feature.

# Package Outline Drawing

## L32.5x5E
**32 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE**
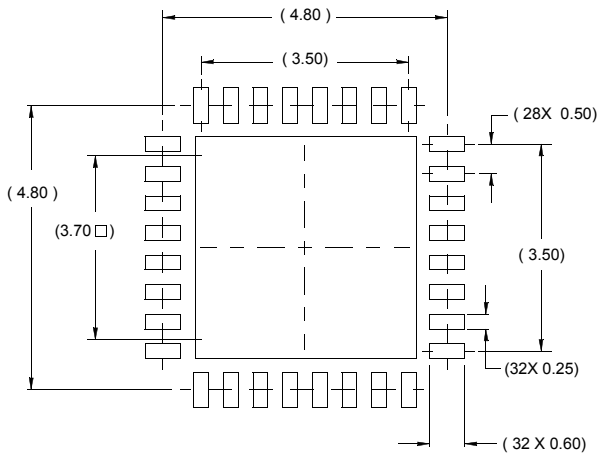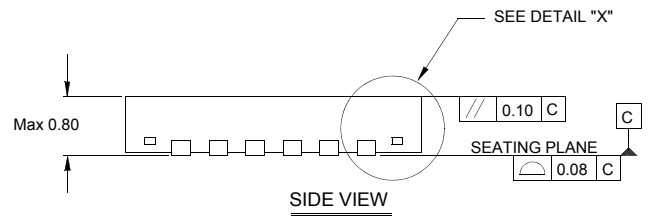**Rev 0, 03/09**

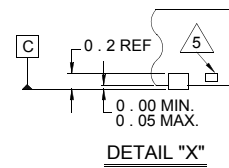TOP VIEW

SIDE VIEW

BOTTOM VIEW

TYPICAL RECOMMENDED LAND PATTERN

SIDE VIEW

DETAIL "X"

NOTES:

1.  Dimensions are in millimeters.
    Dimensions in ( ) for Reference Only.

2.  Dimensioning and tolerancing conform to AMSE Y14.5m-1994.

3.  Unless otherwise specified, tolerance : Decimal ± 0.05

4.  Dimension b applies to the metallized terminal and is measured
    between 0.15mm and 0.30mm from the terminal tip.

5.  Tiebar shown (if present) is a non-functional feature.

6.  The configuration of the pin #1 identifier is optional, but must be
    located within the zone indicated. The pin #1 identifier may be
    either a mold or mark feature.