ISL6294

High Input Voltage Charger

FN9174
Rev 4.00
Jul 9, 2007

The ISL6294 is a cost-effective, fully integrated high input voltage single-cell Li-ion battery charger. The charger uses a CC/CV charge profile required by Li-ion batteries. The charger accepts an input voltage up to 28V but is disabled when the input voltage exceeds the OVP threshold, typically 6.8V, to prevent excessive power dissipation. The 28V rating eliminates the overvoltage protection circuit required in a low input voltage charger.

The charge current and the end-of-charge (EOC) current are programmable with external resistors. When the battery voltage is lower than typically 2.55V, the charger preconditions the battery with typically 20% of the programmed charge current. When the charge current reduces to the programmable EOC current level during the CV charge phase, an EOC indication is provided by the CHG pin, which is an open-drain output. An internal thermal foldback function protects the charger from any thermal failure.

Two indication pins (PPR and CHG) allow simple interface to a microprocessor or LEDs. When no adapter is attached or when disabled, the charger draws less than 1µA leakage current from the battery.

Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL6294IRZ-T	94Z	-40 to +85	8 Ld 2x3 DFN	L8.2x3
ISL6294IBZ	6294 IBZ	-40 to +85	8 Ld SOIC	M8.15
ISL6294IBZ-T	6294 IBZ	-40 to +85	8 Ld SOIC	M8.15

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

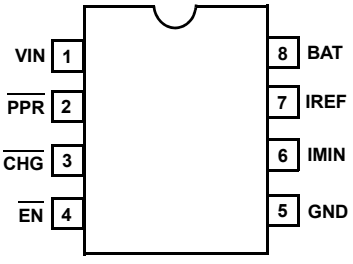
- Complete Charger for Single-Cell Li-ion/Polymer Batteries
- Integrated Pass Element and Current Sensor
- No External Blocking Diode Required
- Low Component Count and Cost
- 1% Voltage Accuracy
- Programmable Charge Current
- **Programmable End-of-Charge Current**
- **Charge Current Thermal Foldback for Thermal Protection**
- Trickle Charge for Fully Discharged Batteries
- **28V Maximum Voltage for the Power Input**
- Power Presence and Charge Indications
- Less Than 1µA Leakage Current off the Battery When No Input Power Attached or Charger Disabled
- Ambient Temperature Range: -40°C to +85°C
- **8 Ld 2x3 DFN and 8 Ld SOIC Packages**
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

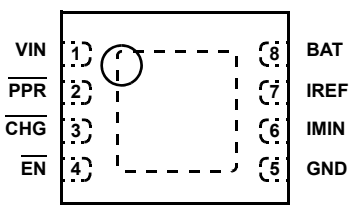
- Mobile Phones
- Blue-Tooth Devices
- PDAs
- MP3 Players
- Stand-Alone Chargers
- Other Handheld Devices

Pinouts

ISL6294
(8 LD SOIC)
TOP VIEW



ISL6294
(8 LD DFN)
TOP VIEW



Absolute Maximum Ratings (Reference to GND)

V_{IN} . . . . . -0.3V to 30V
IMIN, IREF, BAT, CHG, EN, PPR. . . . . .-0.3V to 7V
ESD Rating
Human Body Model (Per EIA JESD22 Method A114-B) 7kV
Machine Model (Per EIA JED-4701 Method C-111) 450V

Recommended Operating Conditions

Ambient Temperature Range . . . . . .-40°C to +85°C
Maximum Supply Voltage (VIN Pin). 28V
Operating Supply Voltage (VIN Pin). . . . . .4.5V to 6.5V
Programmed Charge Current (DFN) . . . . . 100mA to 900mA
Programmed Charge Current (SOIC) . . . . . 100mA to 600mA

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
DFN Package (Notes 1, 2).	59	4.5
SOIC Package (Notes 1, 2)	95	NA

Maximum Junction Temperature (Plastic Package) . . . . . .+150°C
Maximum Storage Temperature Range. . . . . .-65°C to +150°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
2. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Typical Values Are Tested at V_{IN} = 5V and the Ambient Temperature at +25°C. All Maximum and Minimum Values Are Guaranteed Under the Recommended Operating Supply Voltage Range and Ambient Temperature Range, Unless Otherwise Noted.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
POWER-ON RESET						
Rising POR Threshold	V_{POR}	V_{BAT} = 3.0V, use PPR to indicate the comparator output.	3.3	3.9	4.3	V
Falling POR Threshold	V_{POR}		3.1	3.6	4.15	V
VIN-BAT OFFSET VOLTAGE						
Rising Edge	V_{OS}	V_{BAT} = 4.0V, use CHG pin to indicate the comparator output (Note 3)	-	90	150	mV
Falling Edge	V_{OS}		10	50	-	mV
OVERVOLTAGE PROTECTION						
Overvoltage Protection Threshold	V_{OVP}	(Note 4) Use PPR to indicate the comparator output	6.5	6.8	7.1	V
OVP Threshold Hysteresis			100	240	400	mV
STANDBY CURRENT						
BAT Pin Sink Current	$I_{STANDBY}$	Charger disabled or the input is floating	-	-	1.0	µA
VIN Pin Supply Current	I_{VIN}	Charger disabled	-	300	400	µA
VIN Pin Supply Current	I_{VIN}	Charger enabled	-	400	600	µA
VOLTAGE REGULATION						
Output Voltage	V_{CH}	4.3V < V_{IN} < 6.5V, charge current = 20mA	4.158	4.20	4.242	V
PMOS On Resistance	$r_{DS(ON)}$	V_{BAT} = 3.8V, charge current = 0.5A	-	0.6	-	Ω
CHARGE CURRENT (Note 5)						
IREF Pin Output Voltage	I_{IREF}	V_{BAT} = 3.8V	1.18	1.22	1.26	V
Constant Charge Current	I_{CHG}	R_{IREF} = 24.3kΩ, V_{BAT} = 2.8V to 4.0V	450	500	550	mA
Trickle Charge Current	I_{TRK}	R_{IREF} = 24.3kΩ, V_{BAT} = 2.4V	70	95	130	mA
End-of-Charge Current	I_{MIN}	R_{IMIN} = 243kΩ	33	45	57	mA
EOC Rising Threshold		R_{IMIN} = 243kΩ	325	380	415	mA
PRECONDITIONING CHARGE THRESHOLD						
Preconditioning Charge Threshold Voltage	V_{MIN}		2.45	2.55	2.65	V
Preconditioning Voltage Hysteresis	V_{MINHYS}		40	100	150	mV

Electrical Specifications Typical Values Are Tested at V_{IN} = 5V and the Ambient Temperature at +25°C. All Maximum and Minimum Values Are Guaranteed Under the Recommended Operating Supply Voltage Range and Ambient Temperature Range, Unless Otherwise Noted. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INTERNAL TEMPERATURE MONITORING						
Charge Current Foldback Threshold	T_{FOLD}		-	115	-	°C
LOGIC INPUT AND OUTPUTS						
EN Pin Logic Input High			1.3	-	-	V
EN Pin Logic Input Low			-	-	0.5	V
EN Pin Internal Pull Down Resistance			100	200	400	kΩ
CHG Sink Current when LOW		Pin Voltage = 1V	10	20	-	mA
CHG Leakage Current When HIGH		V_{CHG} = 6.5V	-	-	1	µA
PPR Sink Current when LOW		Pin Voltage = 1V	10	20	-	mA
PPR Leakage Current When HIGH		V_{PPR} = 6.5V	-	-	1	µA

NOTES:

3. The 4.0V V_{BAT} is selected so that the CHG output can be used as the indication for the offset comparator output indication. If the V_{BAT} is lower than the POR threshold, no output pin can be used for indication.
4. For junction temperature below +100°C.
5. The charge current can be affected by the thermal foldback function if the IC under the test setup cannot dissipate the heat.

Pin Descriptions

VIN - Power input. The absolute maximum input voltage is 28V. A 0.47µF or larger value X5R ceramic capacitor is recommended to be placed very close to the input pin for decoupling purpose. Additional capacitance may be required to provide a stable input voltage.

PPR - Open-drain power presence indication. The open-drain MOSFET turns on when the input voltage is above the POR threshold but below the OVP threshold and off otherwise. This pin is capable to sink 10mA (minimum) current to drive an LED. The maximum voltage rating for this pin is 7V. This pin is independent on the EN-pin input.

CHG - Open-drain charge indication pin. This pin outputs a logic LOW when a charge cycle starts and turns to HIGH when the end-of-charge (EOC) condition is qualified. This pin is capable to sink 10mA minimum current to drive an LED. When the charger is disabled, the CHG outputs high impedance.

EN - Enable input. This is a logic input pin to disable or enable the charger. Drive to HIGH to disable the charger. When this pin is driven to LOW or left floating, the charger is enabled. This pin has an internal 200kΩ pull-down resistor.

GND - System ground.

IMIN - End-of-charge (EOC) current program pin. Connect a resistor between this pin and the GND pin to set the EOC current. The EOC current IMIN can be programmed by the Equation 1:

$$I_{MIN} = \frac{11000}{R_{IMIN}} \quad (mA) \qquad \text{(EQ. 1)}$$

Where R_{IMIN} is in kΩ. The programmable range covers 5% (or 10mA, whichever is higher) to 50% of IREF. When programmed to less than 5% or 10mA, the stability is not guaranteed.

IREF - Charge-current program and monitoring pin. Connect a resistor between this pin and the GND pin to set the charge current limit determined by the Equation 2:

$$I_{REF} = \frac{12089}{R_{IREF}} \quad (mA) \qquad \text{(EQ. 2)}$$

Where R_{IREF} is in kΩ. The IREF pin voltage also monitors the actual charge current during the entire charge cycle, including the trickle, constant-current, and constant-voltage phases. When disabled, V_{IREF} = 0V.

BAT - Charger output pin. Connect this pin to the battery. A 1µF or larger X5R ceramic capacitor is recommended for decoupling and stability purposes. When the EN pin is pulled to logic HIGH, the BAT output is disabled.

EPAD - Exposed pad. Connect as much as possible copper to this pad either on the component layer or other layers through thermal vias to enhance the thermal performance.

Typical Applications

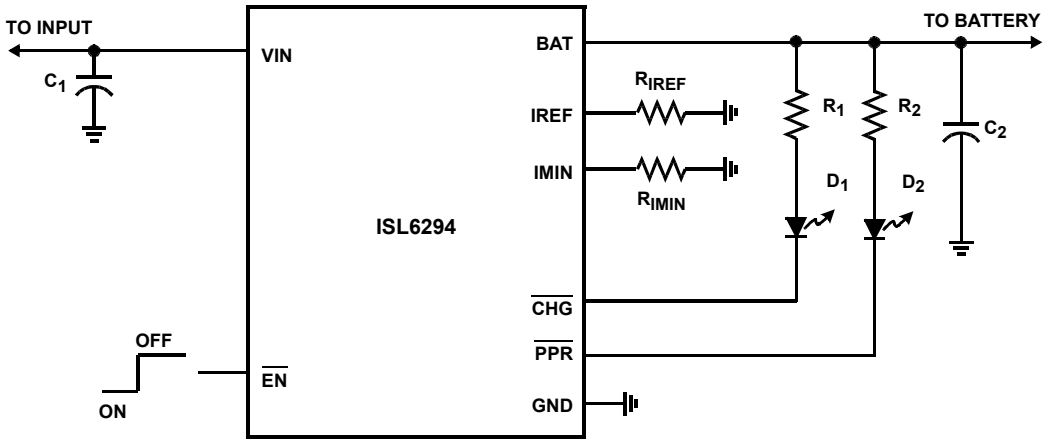


FIGURE 1. TYPICAL APPLICATION CIRCUIT INTERFACING TO INDICATION LEDs

COMPONENT DESCRIPTION FOR FIGURE 1

PART	DESCRIPTION
C_1	1µF X5R ceramic cap
C_2	1µF X5R ceramic cap
R_{IREF}	24.3kΩ, 1%, for 500mA charge current
R_{IMIN}	243kΩ, 1%, for 45mA EOC current
R_1, R_2	300Ω, 5%
D_1, D_2	LEDs for indication

COMPONENT DESCRIPTION FOR FIGURE 2

PART	DESCRIPTION
C_1	1µF X5R ceramic cap
C_2	1µF X5R ceramic cap
R_{IREF}	24.3kΩ, 1%, for 500mA charge current
R_{IMIN}	243kΩ, 1%, for 45mA EOC current
R_1, R_2	100kΩ, 5%

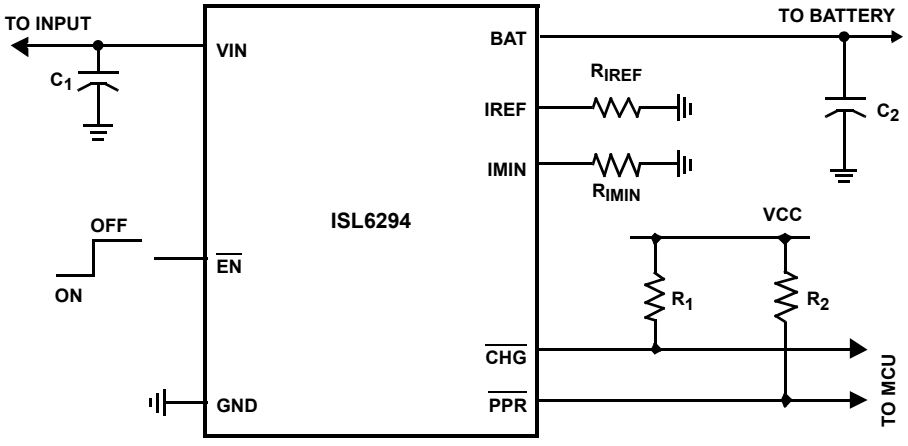


FIGURE 2. TYPICAL APPLICATION CIRCUIT WITH THE INDICATION SIGNALS INTERFACING TO A MCU

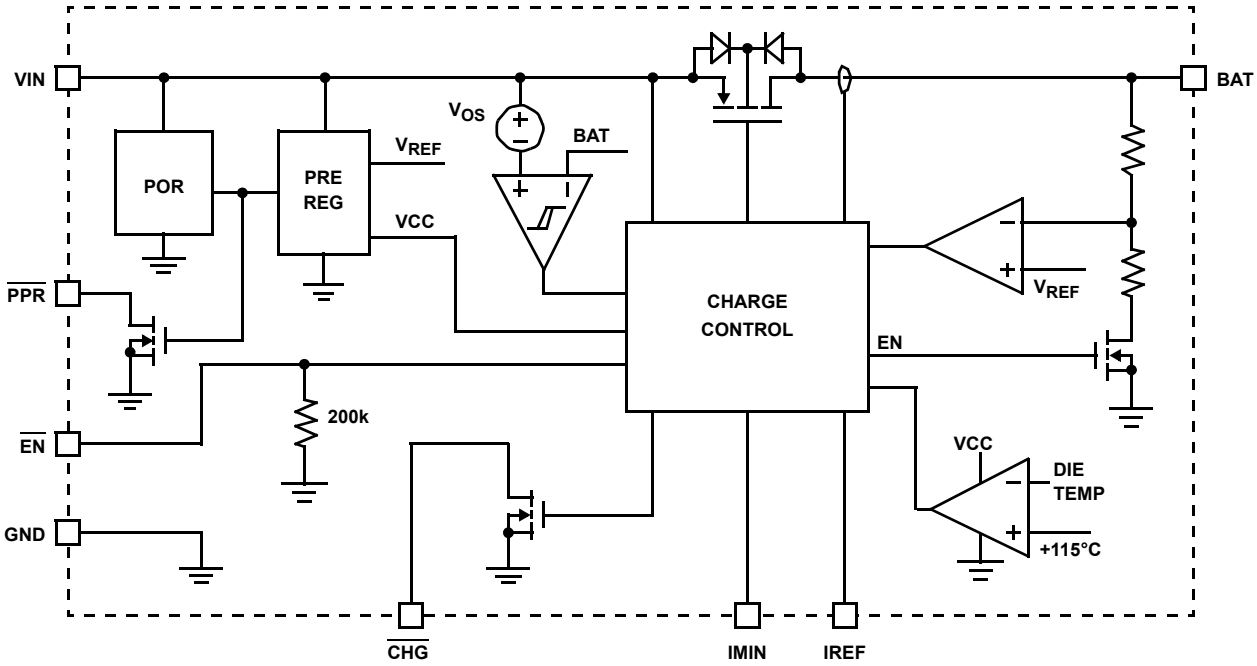


FIGURE 3. BLOCK DIAGRAM

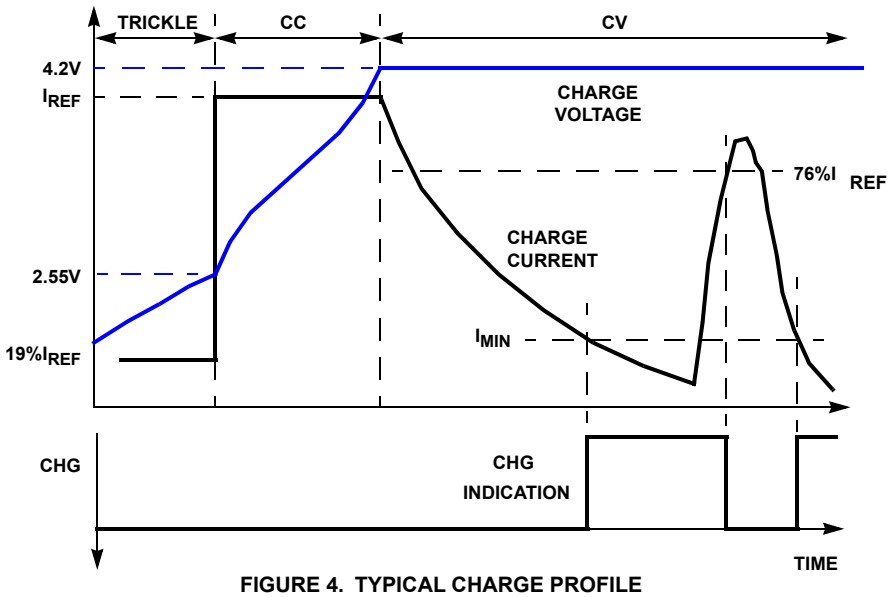


FIGURE 4. TYPICAL CHARGE PROFILE

Description

The ISL6294 charges a Li-ion battery using a CC/CV profile. The constant current I_{REF} is set with the external resistor R_{IREF} (See Figure 1) and the constant voltage is fixed at 4.2V. If the battery voltage is below a typical 2.55V trickle-charge threshold, the ISL6294 charges the battery with a trickle current of 19% of I_{REF} until the battery voltage rises above the trickle charge threshold. Fast charge CC mode is maintained at the rate determined by programming I_{REF} until the cell voltage rises to 4.2V. When the battery voltage reaches 4.2V, the charger enters a CV mode and regulates the battery voltage at 4.2V to fully charge the battery without the risk of over charge. Upon reaching an end-of-charge (EOC) current, the charger indicates the charge completion with the CHG pin, but the charger continues to output the 4.2V voltage. Figure 4 shows the typical charge waveforms after the power is on.

The EOC current level I_{MIN} is programmable with the external resistor R_{IMIN} (See Figure 1). The CHG signal turns

to LOW when the trickle charge starts and rises to HIGH at the EOC. After the EOC is reached, the charge current has to rise to typically 76% I_{REF} for the CHG signal to turn on again, as shown in Figure 4. The current surge after EOC can be caused by a load connected to the battery.

A thermal foldback function reduces the charge current anytime when the die temperature reaches typically +115°C. This function guarantees safe operation when the printed circuit board (PCB) is not capable of dissipating the heat generated by the linear charger. The ISL6294 accepts an input voltage up to 28V but disables charging when the input voltage exceeds the OVP threshold, typically 6.8V, to protect against unqualified or faulty AC adapters.

PPR Indication

The PPR pin is an open-drain output to indicate the presence of the AC adapter. Whenever the input voltage is higher than the POR threshold, the PPR pin turns on the internal open-drain MOSFET to indicate a logic LOW signal, independent on the EN pin input. When the internal open-drain FET is turned off, the PPR pin should leak less than 1µA current. When turned on, the PPR pin should be able to sink at least 10mA current under all operating conditions.

The PPR pin can be used to drive an LED (see Figure 1) or to interface with a microprocessor.

Power-Good Range

The power-good range is defined by the following three conditions:

1. $V_{IN} > V_{POR}$
2. $V_{IN} - V_{BAT} > V_{OS}$
3. $V_{IN} < V_{OVP}$

where the V_{OS} is the offset voltage for the input and output voltage comparator, discussed shortly, and the V_{OVP} is the overvoltage protection threshold given “Electrical Specifications” on page 2. All V_{POR}, V_{OS}, and V_{OVP} have hysteresis, as given in “Electrical Specifications” on page 2. The charger will not charge the battery if the input voltage is not in the power-good range.

Input and Output Comparator

The charger will not be enabled unless the input voltage is higher than the battery voltage by an offset voltage VOS. The purpose of this comparator is to ensure that the charger is turned off when the input power is removed from the charger. Without this comparator, it is possible that the charger will fail to power down when the input is removed and the current can leak through the PFET pass element to continue biasing the POR and the Pre-Regulator blocks shown in the Block Diagram on page 5.

CHG Indication

The CHG is an open-drain output capable to at least 10mA current when the charger starts to charge and turns off when the EOC current is reached. The CHG signal is interfaced either with a micro-processor GPIO or an LED for indication.

EN Input

EN is an active-low logic input to enable the charger. Drive the EN pin to LOW or leave it floating to enable the charger. This pin has a 200kΩ internal pulldown resistor so when left floating, the input is equivalent to logic LOW. Drive this pin to HIGH to disable the charger. The threshold for HIGH is given in “Electrical Specifications”on page 2.

IREF Pin

The IREF pin has the two functions as described in the Pin Description section. When setting the fast charge current, the charge current is guaranteed to have 10% accuracy with the charge current set at 500mA. When monitoring the charge current, the accuracy of the IREF pin voltage vs the actual charge current has the same accuracy as the gain from the IREF pin current to the actual charge current. The accuracy is 10% at 500mA and is expected to drop to 30% of the actual current (not the set constant charge current) when the current drops to 50mA.

Operation Without the Battery

The ISL6294 relies on a battery for stability and is not guaranteed to be stable if the battery is not connected. With a battery, the charger will be stable with an output ceramic decoupling capacitor in the range of 1µF to 200µF. The maximum load current is limited by the dropout voltage or the thermal foldback.

Dropout Voltage

The constant current may not be maintained due to the $r_{DS(ON)}$ limit at a low input voltage. The worst case on resistance of the pass FET is 1.2Ω the maximum operating temperature, thus if tested with 0.5A current and 3.8V battery voltage, constant current could not be maintained when the input voltage is below 4.4V.

Thermal Foldback

The thermal foldback function starts to reduce the charge current when the internal temperature reaches a typical value of +115°C.

Applications Information

Input Capacitor Selection

The input capacitor is required to suppress the power supply transient response during transitions. Mainly this capacitor is selected to avoid oscillation during the start up when the input supply is passing the POR threshold and the VIN - BAT comparator offset voltage. When the battery voltage is above the POR threshold, the VIN - VBAT offset voltage dominates the hysteresis value. Typically, a 1µF X5R ceramic capacitor should be sufficient to suppress the power supply noise.

Output Capacitor Selection

The criteria for selecting the output capacitor is to maintain the stability of the charger as well as to bypass any transient load current. The minimum capacitance is a 1µF X5R ceramic capacitor. The actual capacitance connected to the output is dependent on the actual application requirement.

Charge Current Limit

The actual charge current in the CC mode is limited by several factors in addition to the set I_{REF}. Figure 1 shows three limits for the charge current in the CC mode. The charge current is limited by the on resistance of the pass element (power P-Channel MOSFET) if the input and the output voltage are too close to each other. The solid curve shows a typical case when the battery voltage is 4.0V and the charge current is set to 700mA. The non-linearity on the r_{ON}-limited region is due to the increased resistance at higher die temperature. If the battery voltage increases to higher than 4.0V, the entire curve moves towards right side. As the input voltage increases, the charge current may be reduced due to the thermal foldback function. The limit caused by the thermal limit is dependent on the thermal impedance. As the thermal impedance increases, the thermal-limited curve moves towards left, as shown in Figure 1.

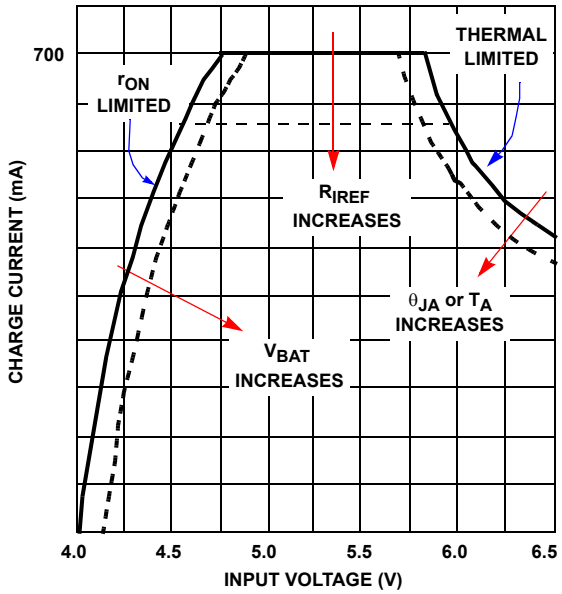


FIGURE 1. CHARGE CURRENT LIMITS IN THE CC MODE

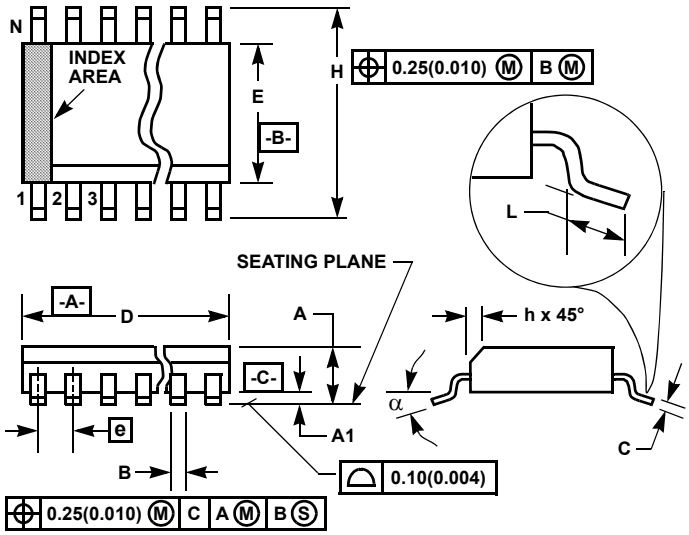
Layout Guidance

The ISL6294 uses a thermally-enhanced DFN package that has an exposed thermal pad at the bottom side of the package. The layout should connect as much as possible to copper on the exposed pad. Typically the component layer is more effective in dissipating heat. The thermal impedance can be further reduced by using other layers of copper connecting to the exposed pad through a thermal via array. Each thermal via is recommended to have 0.3mm diameter and 1mm distance from other thermal vias.

Input Power Sources

The input power source is typically a well-regulated wall cube with 1-meter length wire or a USB port. The input voltage ranges from 4.25V to 6.5V under full-load and unloaded conditions. The ISL6294 can withstand up to 28V on the input without damaging the IC. If the input voltage is higher than typically 6.8V, the charger stops charging.

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0°	8°	0°	8°	-

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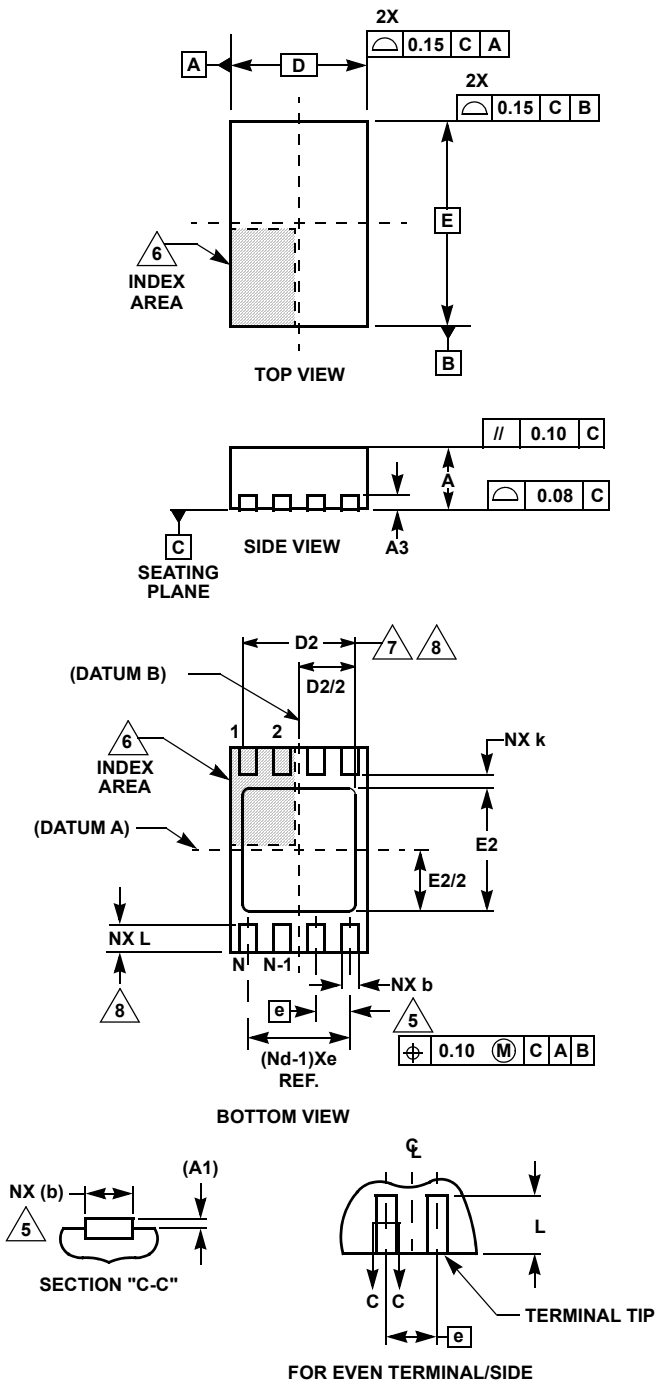
Dual Flat No-Lead Plastic Package (DFN)



L8.2x3

8 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A3		0.20 REF		-
b	0.20	0.25	0.32	5,8
D		2.00 BSC		-
D2	1.50	1.65	1.75	7,8
E		3.00 BSC		-
E2	1.65	1.80	1.90	7,8
e		0.50 BSC		-
k	0.20	-	-	-
L	0.30	0.40	0.50	8
N		8		2
Nd		4		3

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NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd refers to the number of terminals on D.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.25mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.

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