ISL70024SEH, ISL73024SEH

200V, 7.5A Enhancement Mode GaN Power Transistor

The ISL70024SEH and ISL73024SEH are 200V N-channel enhancement mode GaN power transistors. These GaN FETs have been characterized for destructive Single Event Effects (SEE) and tested for Total Ionizing Dose (TID) radiation. Applications for these devices include commercial aerospace, medical, and nuclear power generation.

GaN's exceptionally high electron mobility and low temperature coefficient allows for very low $r_{DS(ON)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and near zero Q_{RR}. The end result is a device that can operate at a higher switching frequency with more efficiency while reducing the overall solution size.

By combining the exceptional performance of the GaN FET in a hermetically sealed Surface Mount Device (SMD) package with manufacturing in a MIL-PRF-38535 like flow results in best-in-class power transistors that are ideally suited for high reliability applications.

Applications

- Switching regulation
- Motor drives
- Relay drives
- Inrush protection
- Down hole drilling
- High reliability industrial

Features

- Very low $r_{DS(ON)}$ 45mΩ (typical)
- Ultra low total gate charge 2.5nC (typical)
- SEE hardness (see SEE report for details)
  - SEL/SEB LET_{TH} (V_{DS} = 160V, V_{GS} = 0V): 86MeV•cm^2/mg(Si)
- ISL70024SEH radiation acceptance (see TID report)
  - High dose rate (50-300rad(Si)/s): 100krad(Si)
  - Low dose rate (0.01rad(Si)/s): 75krad(Si)
- ISL73024SEH radiation acceptance (see TID report)
  - Low dose rate (0.01rad(Si)/s): 75krad(Si)
- Ultra small hermetically sealed 4 Ld Surface Mount Device (SMD) package
  - Package area: 42mm^2
- Full military-temperature range operation
  - T_A = -55°C to +125°C
  - T_J = -55°C to +150°C
- Qualified to Renesas Rad Hard GaN FET Screening and QCI Flow (R34TB0003EU)
  - All screening and QCI is in accordance with MIL-PRF-38535L Class-V

Figure 1. ISL70024SEH 4 Ld SMD Package

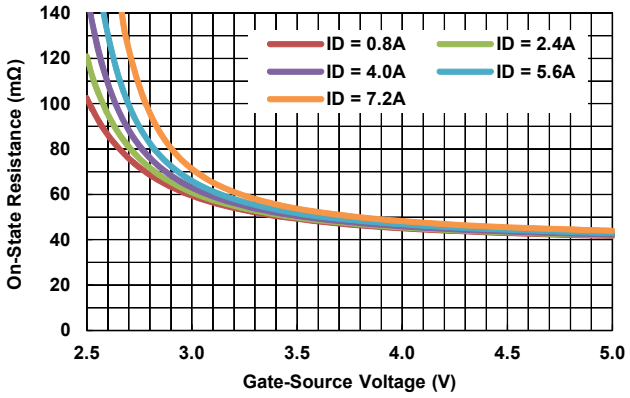


Figure 2. On-State Resistance (+25°C)

Contents

1. Overview

1.1 Ordering Information

Ordering Part Number[1]	Radiation Hardness (Total Ionizing Dose)	Package Description (RoHS Compliant)	Package Drawing	Temperature Range (°C)
ISL70024SEHML	HDR to 100krad(Si) LDR to 75krad(Si)	4 Ld SMD	J4.A	-55 to +125
ISL73024SEHML	LDR to 75krad(Si)			
ISL70024SEHMX[2][3]	HDR to 100krad(Si) LDR to 75krad(Si)	Die	-	
ISL73024SEHMX[2][3]	LDR to 75krad(Si)			
ISL70024SEHX/SAMPLE[2][3][4]	N/A			
ISL73024SEHX/SAMPLE[2][3][4]	N/A			
ISL70024SEHL/PROTO[4]	N/A	4 Ld SMD	J4.A	
ISL73024SEHL/PROTO[4]	N/A			
ISL70040SEHEV3Z[5]	Evaluation board with the ISL70040SEH low-side driver and ISL70024SEH 200V GaN FET			
ISL73040SEHEV4Z[5]	Half bridge power stage using the ISL73040SEH, ISL73024SEH, and the ISL71610M			

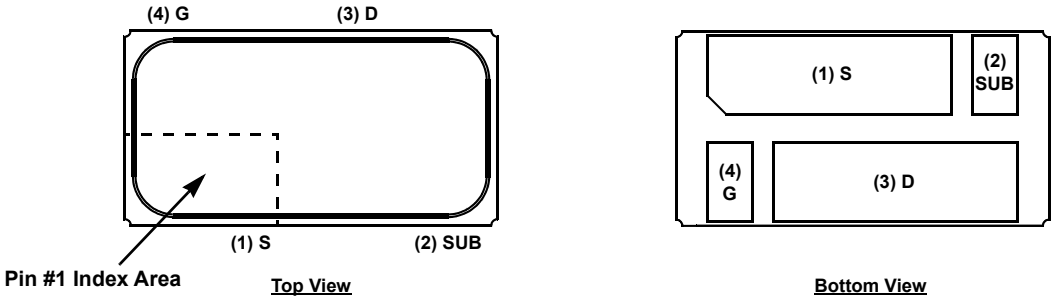
1. These Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
2. Die product tested at TA = + 25°C. The wafer probe test includes functional and parametric testing sufficient to make the die capable of meeting the electrical performance outlined in <Hyperlink>“Electrical Specifications” on page 6.
3. The die solder bump composition is PbSn (95%/5%) with a melt point of 312°C. Recommended reflow profile includes a ramp-up to a peak of 350-360°C with a dwell time of 3 minutes at/near the peak before ramp-down in a hydrogen forming gas with 3% hydrogen.
4. The /PROTO and /SAMPLE are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions across temperature specified in this datasheet. The /SAMPLE parts are capable of meeting the electrical limits and conditions specified in this datasheet. The /SAMPLE parts do not receive 100% screening across temperature to the electrical limits. These part types do not come with a Certificate of Conformance.
5. Evaluation boards use the /PROTO parts and /PROTO parts are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity.

Table 1. Key Differences Between Family of Parts

Part Number	Breakdown Voltage (V)	Drain Current (A)	$r_{DS(ON)}$ (mΩ)	Q_G (nC)
ISL7x020SEH	40	65	3.5	19
ISL7x023SEH	100	60	5	14
ISL7x024SEH	200	7.5	45	2.5

2. Pin Information

2.1 Pin Assignments



Note: The ESD triangular mark indicates Pin #1. It is a part of the device marking and is placed on the lid in the quadrant where Pin #1 is located.

4 Ld SMD

2.2 Pin Descriptions

Pin Number	Pin Name	Description
1	S	Source connection for the GaN FET.
2	SUB	Substrate connection for the GaN FET which is internally shorted in to source. Tie this pin to source on the PCB.
3	D	Drain connection for the GaN FET.
4	G	Gate connection for the GaN FET. Minimize trace inductance from driver to reduce over-stressing the gate.
NA	Lid	Internally tied to the source pin.

3. Specifications

3.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Maximum	Unit
V_{DS}	200	V
V_{DS}[1]	160	V
V_{GS}	-4 to 6	V
ESD Rating (Drain-to-Source)		
Human Body Model (Tested per MIL-STD-883 TM3015)	2	kV
Machine Model (Tested per JESD22-A115C)	200	V
Charged Device Model (Tested per JS-002-2014)	750	V
ESD Rating (Gate-to-Source)		
Human Body Model (Tested per MIL-STD-883 TM3015)	500	V
Machine Model (Tested per JESD22-A115C)	200	V
Charged Device Model (Tested per JS-002-2014)	750	V

1. Tested in a heavy ion environment at LET = 86.4MeV•cm^2/mg(Si) at +125°C (T_C).

3.2 Thermal Information

Parameter	Package	Symbol	Conditions	Typical Value	Maximum	Unit
Thermal Resistance	SMD Package J4.A	θ_{JA}[1]	Junction to air	42	-	°C/W
		θ_{JC}[2]	Junction to case	18.7	23.4	°C/W

1. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with “direct attach” features. See TB379.
2. For θ_{JC}, the case temperature location is on the solder terminations adjacent to the center of the package underside.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature	-	+150	°C
Storage Temperature Range	-65	+150	°C

3.3 Recommended Operating Conditions

Parameter	Maximum	Unit
Temperature	-55 to +125	°C
V_{DS}	160	V
I_D (V_{GS} = 5.0V, T_C = +25°C)[1]	7.5	A
I_D (V_{GS} = 5.0V, T_C = +105°C)[1]	4.5	A

1. T_J = +150°C. Current limited by package constraints.

3.4 Electrical Specifications

Unless otherwise noted, V_{DS} = 160V. **Boldface limits apply across the operating temperature range, -55°C to +125°C; over a total ionizing dose of 100krad(Si) with exposure at a high dose rate of 50-300rad(Si)/s (ISL70024SEH only); or over a total ionizing dose of 75krad(Si) with exposure at a low dose rate of <10mrad(Si)/s.**

Parameter	Symbol	Test Conditions	Min[1]	Typ[2]	Max[1]	Unit
Static Characteristics						
Drain-to-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 125µA	**200**	-	-	V
Drain-to-Source Leakage Current	I_{DSS}	V_{DS} = 160V, V_{GS} = 0V	-	1	**115**	µA
Drain-to-Gate Leakage Current	I_{GSX}	V_{DS} = 160V, V_{GS} = 0V	-	1	**115**	µA
Gate-to-Source Forward Leakage	I_{GSS}	V_{GS} = 5V	-	0.8	**2.5**	mA
Gate-to-Source Reverse Leakage		V_{GS} = -4V	**-100**	-20	-	µA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1.5mA	**0.8**	1.4	**2.5**	V
Drain-to-Source ON-Resistance	$r_{DS(ON)}$	V_{GS} = 5V, I_D = 7A	-	45	**110**	mΩ
Source-to-Drain Forward Voltage	V_{SD}	I_S = 0.5A, V_{GS} = 0V	**0.8**	1.8	**3.5**	V
Dynamic Characteristics						
Input Capacitance[3]	C_{ISS}	V_{DS} = 100V, V_{GS} = 0V	-	270	-	pF
Output Capacitance	C_{OSS}	V_{DS} = 100V, V_{GS} = 0V, T_A = +25°C	-	150	200	pF
Reverse Transfer Capacitance[3]	C_{RSS}	V_{DS} = 100V, V_{GS} = 0V	-	1	-	pF
Gate Resistance[3]	r_G	T_A = +25°C	-	60	-	mΩ
Total Gate Charge	Q_G	V_{DS} = 100V, V_{GS} = 5V, I_D = 7A, T_A = +25°C	-	2.5	5	nC
Gate Charge at Threshold[3]	$Q_{G(th)}$	V_{DS} = 100V, I_D = 7A	-	0.4	-	nC
Gate-to-Source Charge	Q_{GS}	V_{DS} = 100V, I_D = 7A, T_A = +25°C	-	0.8	2.0	nC
Gate-to-Drain Charge	Q_{GD}	V_{DS} = 100V, I_D = 7A, T_A = +25°C	-	0.6	2.0	nC
Output Charge[3]	Q_{OSS}	V_{DS} = 100V, V_{GS} = 0V	-	23	-	nC

1. Parameters with MIN and/or MAX limits are 100% tested at -55°C, +25°C, and +125°C, unless otherwise specified.
2. Typical values shown are not guaranteed.
3. Limits are established by characterization and/or design and are not tested.

4. Typical Performance Curves

Unless otherwise noted, V_{DS} = 160V; T_A = +25°C.

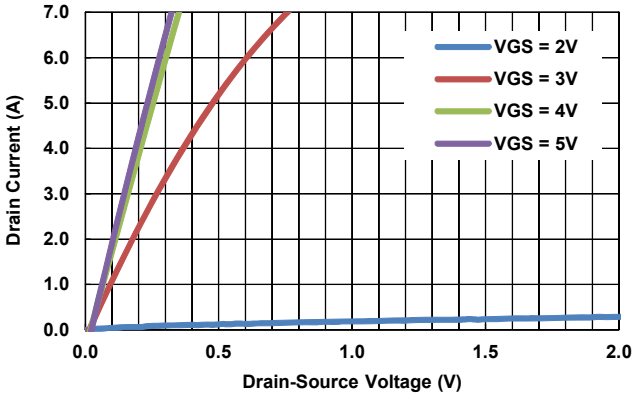


Figure 3. Output Characteristics (+25°C)

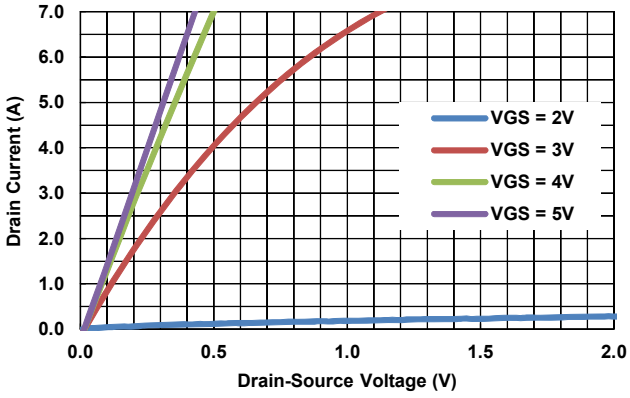


Figure 4. Output Characteristics (+125°C)

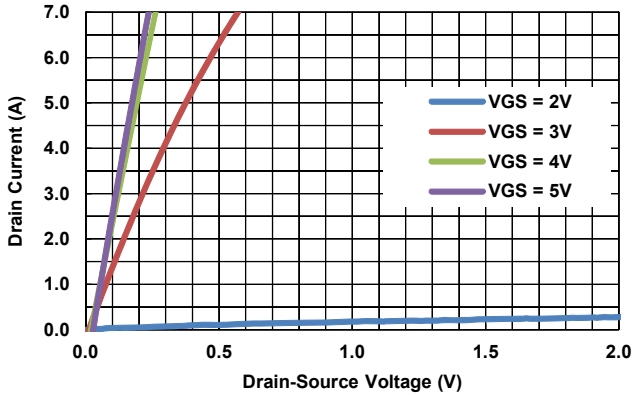


Figure 5. Output Characteristics (-55°C)

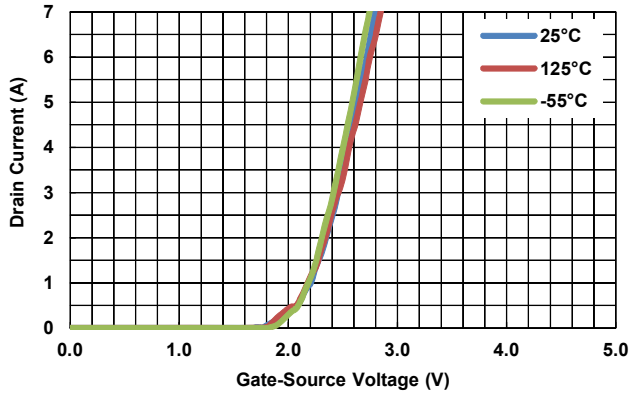


Figure 6. Transfer Characteristics

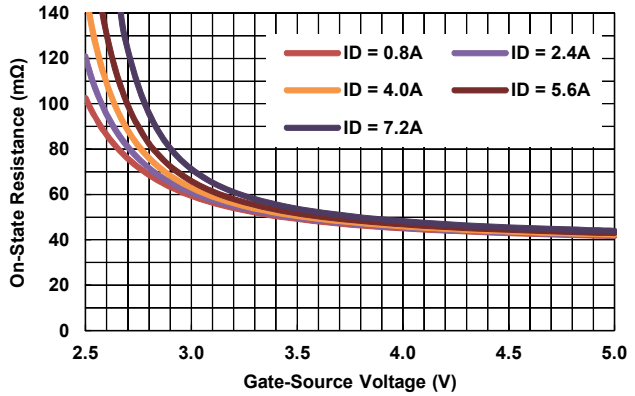


Figure 7. On-State Resistance (+25°C)

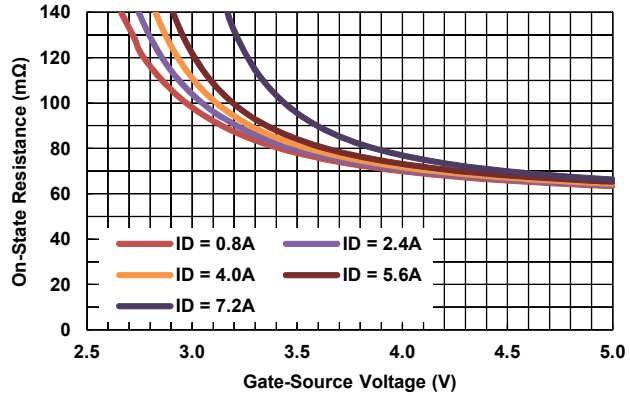


Figure 8. On-State Resistance (+125°C)

Unless otherwise noted, V_{DS} = 160V; T_A = +25°C. (Cont.)

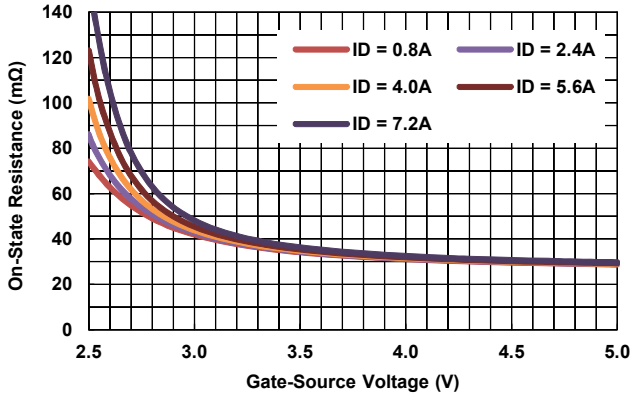


Figure 9. On-State Resistance (-55°C)

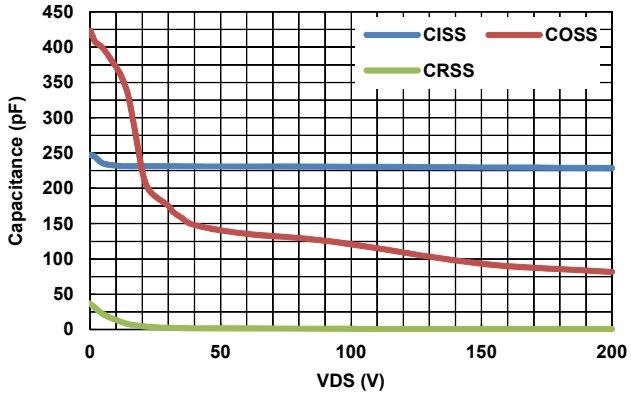


Figure 10. Capacitance (Linear Scale)

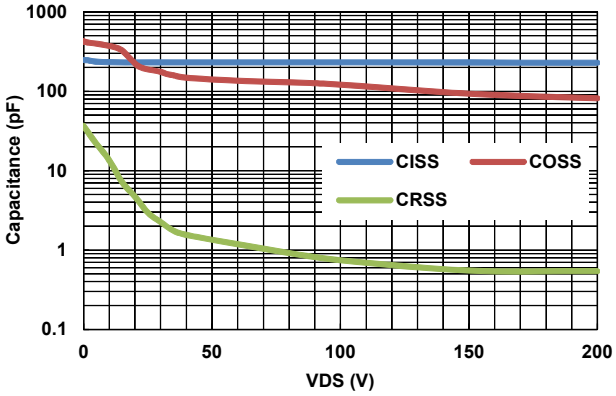


Figure 11. Capacitance (Log Scale)

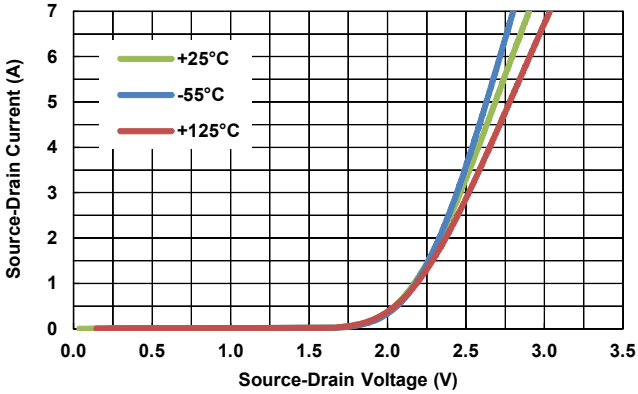


Figure 12. Reverse Drain-Source Characteristics

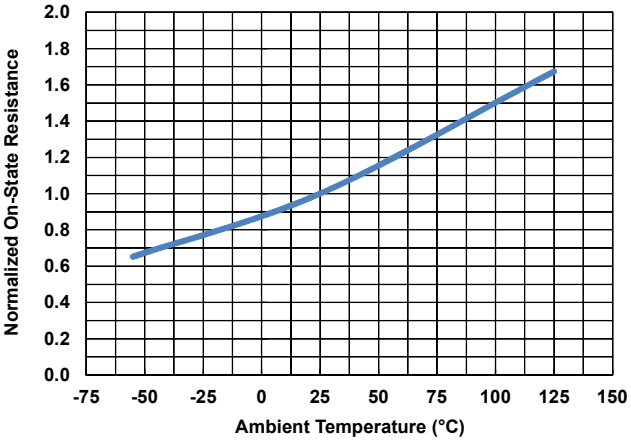


Figure 13. Normalized On-State Resistance

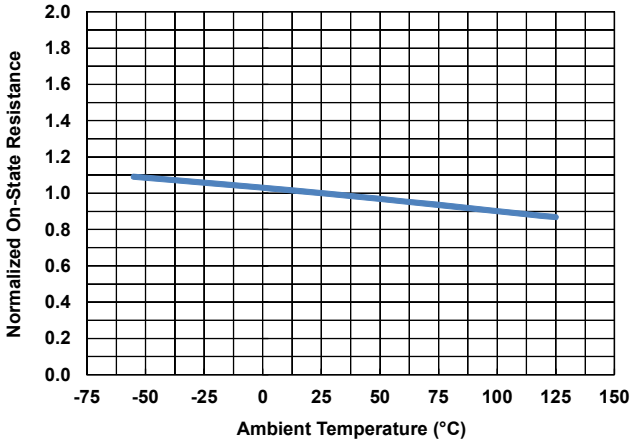


Figure 14. Normalized Threshold Voltage

Unless otherwise noted, V_{DS} = 160V; T_A = +25°C. (Cont.)

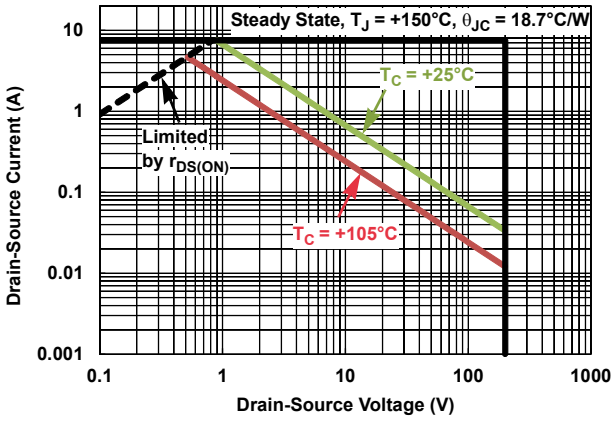


Figure 15. Safe Operating Area

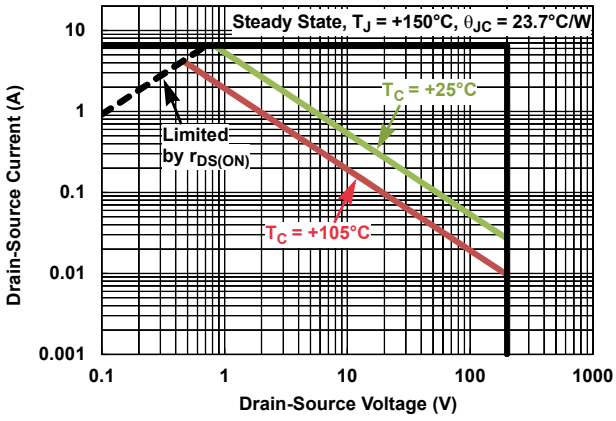


Figure 16. Safe Operating Area (Derated)

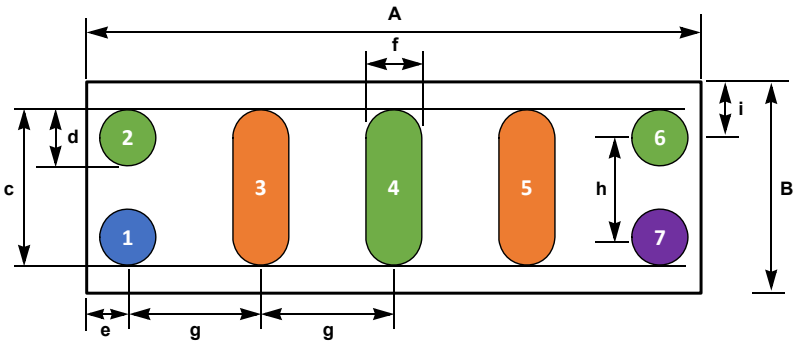
5. Die Characteristics

Table 2. Die and Assembly Related Information

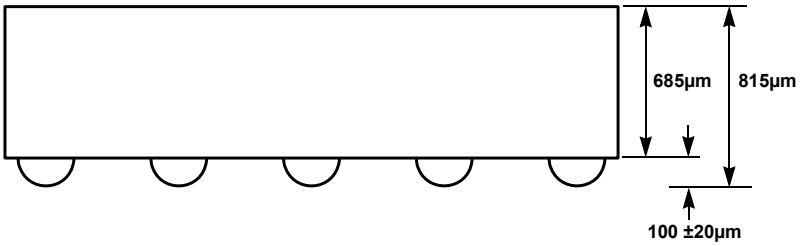
Die Information	
Dimensions	2766µm×950µm (108.90 mils×37.40 mils) Thickness: 685µm (26.97 mils)

ISL70024SEH, ISL73024SEH

Solder Bar View



Side View



Color Key:

- Pads in Green are the Source
- Pads in Orange are the Drain
- Pad in Blue is the Gate
- Pad in Purple is the Substrate

Table 3. Dimensions

Dimension	Min (µm)	Nominal (µm)	Max (µm)
A	2736	2766	2796
B	920	950	980
c	697	700	703
d	247	250	253
e	168	183	198
f	245	250	255
g	600	600	600
h	450	450	450
i	235	250	265

6. Revision History

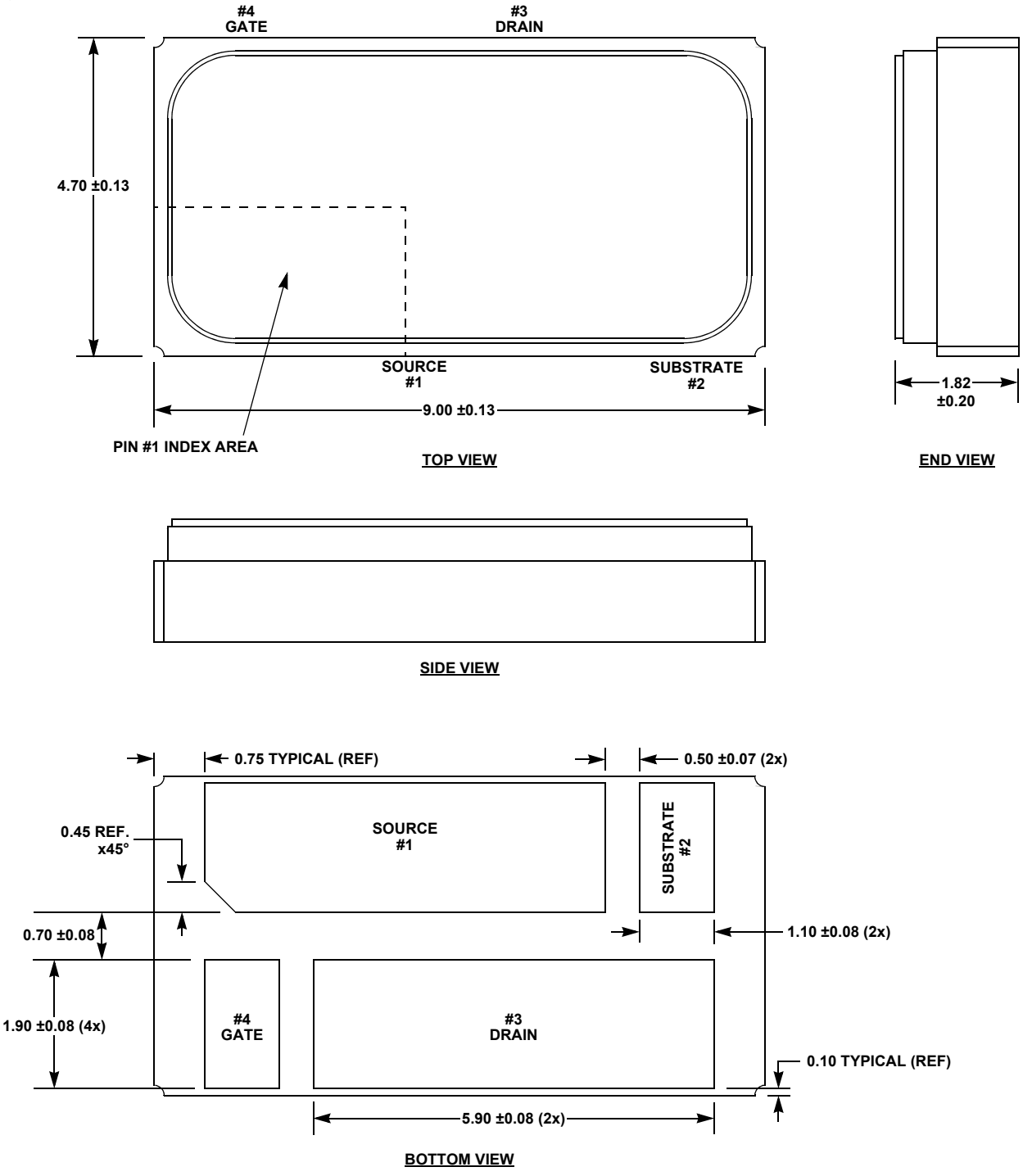
Rev.	Date	Description
6.03	Mar 28, 2024	Clarified that LETs were calculated using a silicon target substrate.
6.02	Jun 9, 2023	Applied latest template. Added the screening features bullet.
6.01	May 5, 2022	Removed related literature section. Updated Table 1. Updated Abs Max and Recommended Operating Conditions sections by removing the minimum column. Moved ESD Ratings to its own section.
6.00	Jan 28, 2021	Updated links. Updated Table 1. Added Notes 3 and 4.
5.00	Aug 16, 2019	Updated SEE and TID ratings in Features section. Added radiation levels to ordering information table. Updated Table 1 on page 2.
4.00	Feb 8, 2019	Updated ordering information table by adding evaluation boards and Note 3. Updated disclaimer.
3.00	Mar 8, 2018	Updated ordering information table by correcting /SAMPLE part numbers and adding Die where applicable. Updated Section 4 heading from “Die and Assembly Characteristics” to “Die Characteristics”.
2.00	Feb 5, 2018	Changed 55mΩ to 45mΩ in the first Features bullet.
1.00	Jan 15, 2018	Updated Figure 1. Added ISL73024SEH part to datasheet. Ordering Information table on page 2 and updated Note 2. Added Table of Differences on page 2. Electrical Spec table - updated Note 9 on page 5. Added Die and Assembly Characteristics section on page 9. Removed “About Intersil” section. Updated disclaimer and moved to last page.
0.00	Oct 4, 2017	Initial release

7. Package Outline Drawing

For the most recent package outline drawing, see J4.A.

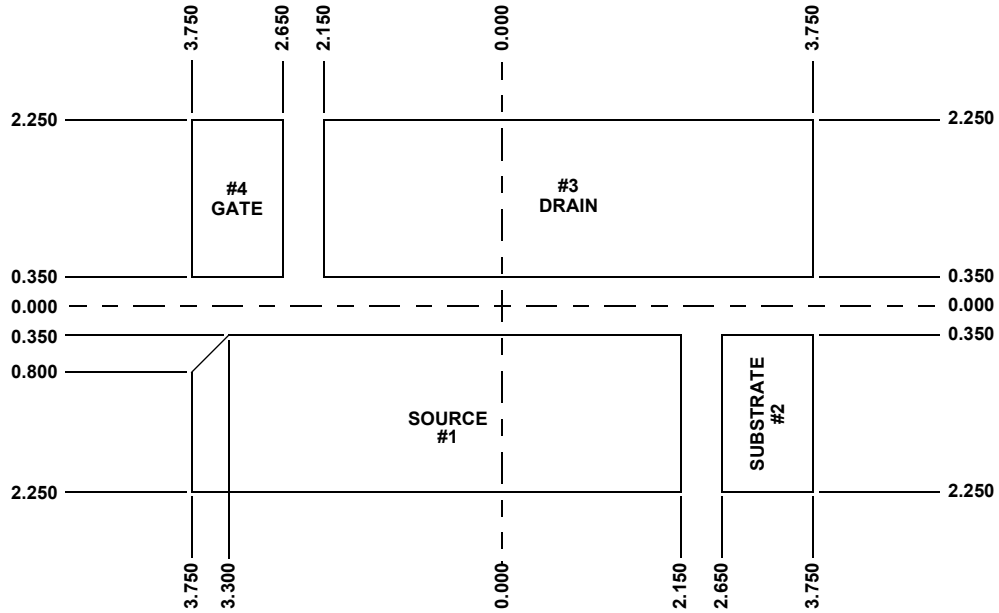
J4.A

4-Pin 9.0mmx4.7mm Hermetic Surface Mount Package
Rev 0, 2/16



NOTES:

1. The corner shape (radius, chamfer, etc.) may vary at the manufacturer's option from that shown on the drawing.
2. The package thickness dimension is the package height before being solder dipped.
3. Dimensions are in millimeters.



TYPICAL RECOMMENDED LAND PATTERN

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