ISL71010B25

Ultra Low Noise, 2.5V Precision Voltage Reference

Description

The ISL71010B25 is an ultra low noise, high DC accuracy precision voltage reference with a wide input voltage range from 4V to 30V. The ISL71010B25 uses the dielectrically isolated PR40 process to achieve 1.9µV_{P-P} noise at 0.1Hz to 10Hz with an initial voltage accuracy of ±0.05%.

The ISL71010B25 offers a 2.5V output voltage with 10ppm/°C temperature coefficient and also provides excellent line and load regulation. The device is offered in an 8 Ld SOIC package.

The ISL71010B25 is ideal for high-end instrumentation, data acquisition, and processing applications requiring high DC precision where low noise performance is critical.

Applications

- Low Earth Orbit (LEO)
- High altitude avionics
- Precision instruments
- Data acquisition systems for space applications
- Strain and pressure gauges for space applications
- Active sources for sensors

Features

- Qualified to Renesas Rad Tolerant Screening and QCI Flow (R34TB0004EU)
- Reference output voltage: 2.5V ±0.05%
- Accuracy over temperature/radiation: ±0.15%
- Output voltage noise: 1.9µV_{P-P} typical (0.1Hz to 10Hz)
- Supply current: 930µA (typical)
- Temperature coefficient: 10ppm/°C (max)
- Output current capability: 20mA
- Line regulation: 18ppm/V (max)
- Load regulation: 17ppm/mA (max)
- NiPdAu-Ag lead finish (Sn free)
- Dielectrically isolated PR40 process
- Operating temperature range: -55°C to +125°C
- Passes NASA Low Outgassing Specifications
- TID Radiation Lot Acceptance Testing (RLAT) (LDR: ≤10mrad(Si)/s)
  - ISL71010BM30B25Z: 30krad(Si)
  - ISL71010BM50B25Z: 50krad(Si)
- SEE Characterization
  - No DSEE for V_{IN} = 39V at 43MeV·cm^2/mg
  - V_{OUT} SET shorter than 20µs and $|\Delta V_{OUT}| \leq$ 235mV at 28MeV·cm^2/mg

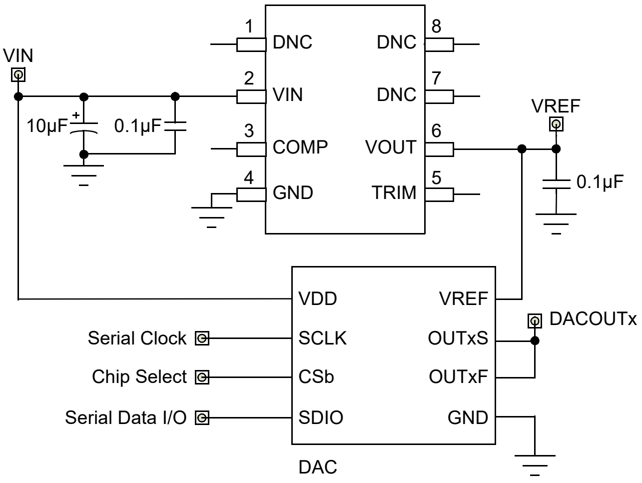

Figure 1. ISL71010B25 Typical Application Diagram

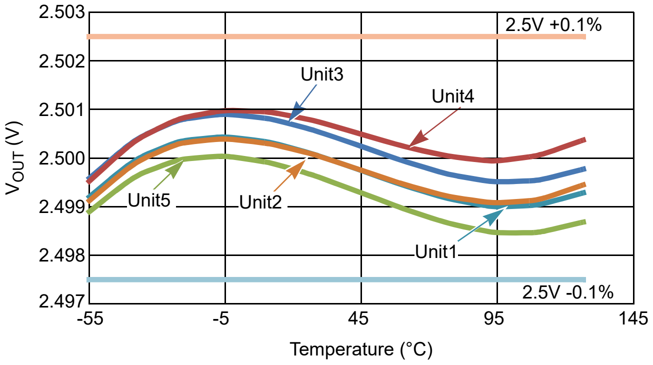

Figure 2. V_{OUT} vs Temperature

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1. Overview

1.1 Functional Block Diagram

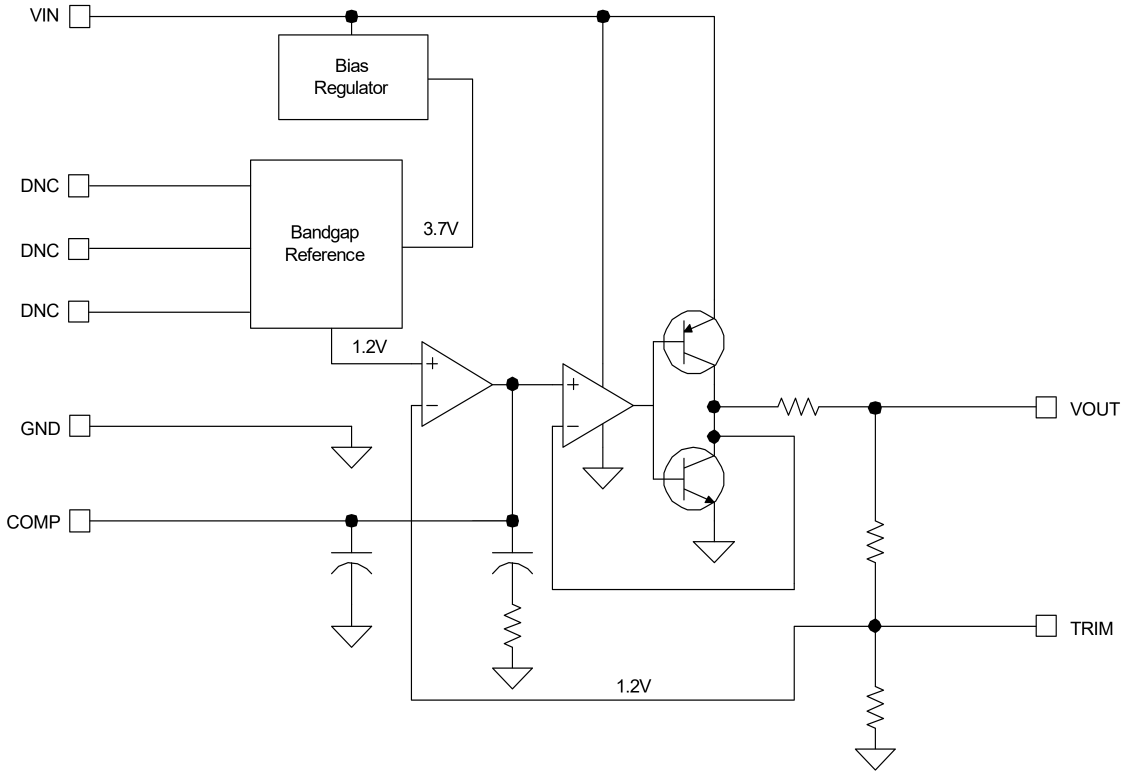


Figure 3. Functional Block Diagram

2. Pin Information

2.1 Pin Assignments

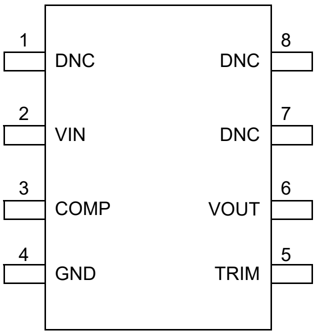
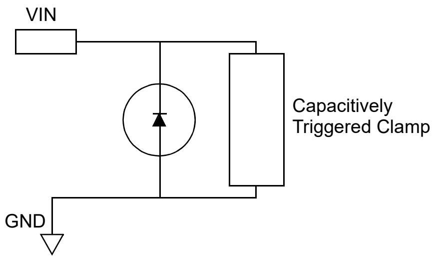


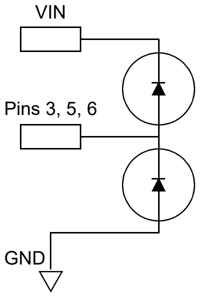
Figure 4. Pin Assignments - Top View

2.2 Pin Description

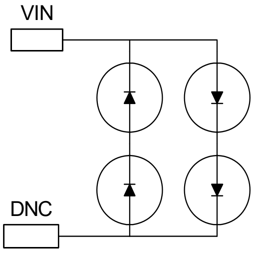
Pin Number	Pin Name	ESD Circuit	Description
1, 7, 8	DNC	3	Do not connect. Internally terminated.
2	VIN	1	Input voltage connection
3	COMP	2	Compensation and noise reduction capacitor
4	GND	1	Ground connection.
5	TRIM	2	Voltage reference trim input
6	VOUT	2	Voltage reference output



ESD Circuit 1



ESD Circuit 2



ESD Circuit 3

3. Specifications

3.1 Absolute Maximum Ratings

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
Max Voltage			
V_{IN} to GND	-0.5	+40	V
V_{OUT} to GND (10s)	-0.5	V_{OUT} + 0.5	V
Voltage on any Pin to Ground	-0.5	V_{OUT} + 0.5	V
Voltage on DNC pins	No connections permitted to these pins		
Input Voltage Slew Rate (Max)	-	0.1	V/µs
Continuous Power Dissipation (T_A = +125°C)		217	mW
Maximum Junction Temperature (T_{JMAX})		+150	°C
Storage Temperature Range	-65	+150	°C
Human Body Model (Tested per JS-001-2014)	-	3	kV
Machine Model (Tested per JESD22-A115-C)	-	200	V
Charged Device Model (Tested per JS-002-2014)	-	2	kV
Latch-Up (Tested per JESD-78E; Class 2, Level A) at +125°C	-	±100	mA

3.2 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
V_{IN}	4.0	+30	V
Temperature Range	-55	+125	°C

3.3 Thermal Information

Parameter	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance	8 Ld SOIC Package	θ_{JA}[1]	Junction to ambient	110	°C/W
		θ_{JC}[2]	Junction to case	60	°C/W

1. θ_{JA} is measured with the component mounted on a high-effective thermal conductivity test board in free air. See TB379 for details.
2. For θ_{JC}, the case temperature location is taken at the package top center.

3.4 Outgas Testing

Specification (Tested per ASTM E 595, 1.5)	Value	Unit
Total Mass Lost[1]	0.06	%
Collected Volatile Condensible Material[1]	<0.01	%
Water Vapor Recovered	0.03	%

1. Results meet NASA low outgassing requirements of “Total Mass Lost” of <1% and “Collected Volatile Condensible Material” of <0.1%.

3.5 Electrical Specifications

V_{IN} = 5V, I_{OUT} = 0mA, C_{OUT} = 0.1µF, COMP = 1nF unless otherwise specified. **Boldface limits apply across the operating temperature range, -55°C to +125°C by characterization with production testing at +25°C; over a total ionizing dose of 30krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL71010BM30B25Z); or over a total ionizing dose of 50krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL71010BM50B25Z).**

Description	Parameter	Test Conditions	Min[1]	Typ	Max[1]	Unit
Output Voltage	V_{OUT}	V_{IN} = 5V	-	2.5	-	V
V_{OUT} Accuracy[2]	V_{OA}	V_{OUT} = 2.5V, T_A = +25°C	-0.05	-	+0.05	%
		V_{OUT} = 2.5V, T_A = -55°C to +125°C	**-0.15**	-	**+0.15**	%
		V_{OUT} = 2.5V, T_A = +25°C, 30krad(Si)	-0.15	-	+0.15	%
		V_{OUT} = 2.5V, T_A = +25°C, 50krad(Si)	-0.20	-	+0.20	%
Output Voltage Temperature Coefficient[3]	TC V_{OUT}	-	-	-	**10**	ppm/°C
Input Voltage Range	V_{IN}	V_{OUT} = 2.5V	**4**	-	**30**	V
Supply Current	I_{IN}	-	-	0.92	**1.28**	mA
Line Regulation	$\Delta V_{OUT} / \Delta V_{IN}$	V_{IN} = 4V to 30V, V_{OUT} = 2.5V	-	6	**18**	ppm/V
Load Regulation	$\Delta V_{OUT}/\Delta I_{OUT}$	Sourcing: $0mA \leq I_{OUT} \leq 20mA$	-	2.5	**17**	ppm/mA
		Sinking: $-10mA \leq I_{OUT} \leq 0mA$	-	2.5	**17**	ppm/mA
Dropout Voltage[4]	V_D	V_{OUT} = 2.5V at 10mA	-	1.1	**1.7**	V
Short-Circuit Current	I_{SC+}	T_A = +25°C, V_{OUT} tied to GND	-	54	75	mA
Short-Circuit Current	I_{SC-}	T_A = +25°C, V_{OUT} tied to V_{IN}	-100	-60	-	mA
Turn-on Settling Time	t_R	90% of final value, C_L = 1.0µF, C_C = open	-	150	-	µs
Ripple Rejection		f = 120Hz	-	90	-	dB
Noise Voltage	e_{np-p}	$0.1Hz \leq f \leq 10Hz$, V_{OUT} = 2.5V	-	1.9	-	μV_{P-P}
Broadband Voltage Noise	V_n	$10Hz \leq f \leq 1kHz$, V_{OUT} = 2.5V	-	1.6	-	μV_{RMS}
Noise Voltage Density	e_n	f = 1kHz, V_{OUT} = 2.5V	-	50	-	nV/√Hz
Long Term Stability	$\Delta V_{OUT}/\Delta t$	T_A = +25°C	-	20	-	ppm

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.
2. Post-reflow drift for the ISL71010B25 devices can exceed 100µV to 1.0mV based on experimental results with devices on FR4 double sided boards. The system engineer must take this into account when considering the reference voltage after assembly.
3. Over the specified temperature range. Temperature coefficient is measured by the box method whereby the change in V_{OUT} is divided by the temperature range; in this case, -55°C to +125°C = +180°C. See Specifying Temperature Coefficient (Box Method) for more information.
4. Dropout Voltage is the minimum V_{IN} - V_{OUT} differential voltage measured at the point where V_{OUT} drops 1mV from V_{IN} = nominal at T_A = +25°C.

4. Typical Performance Curves

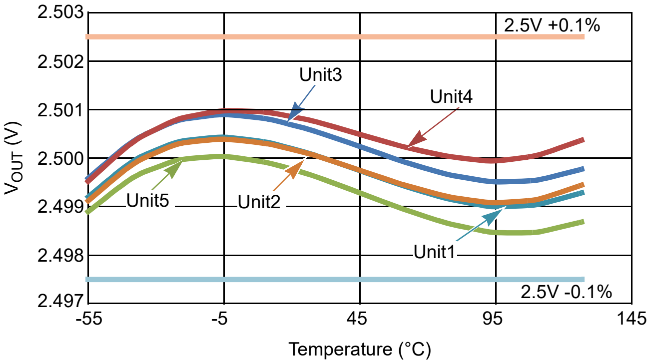


Figure 5. V_{OUT} vs Temperature, Five Units

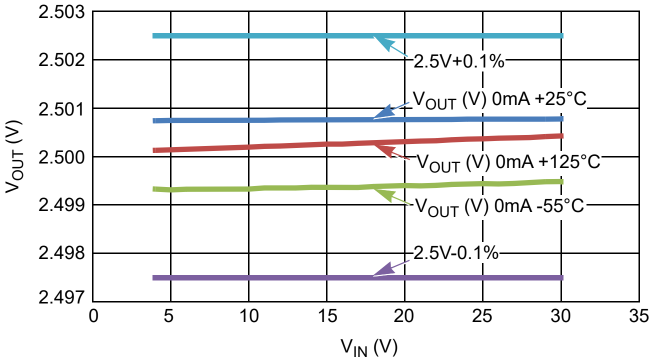


Figure 6. V_{OUT} Accuracy Over-Temperature

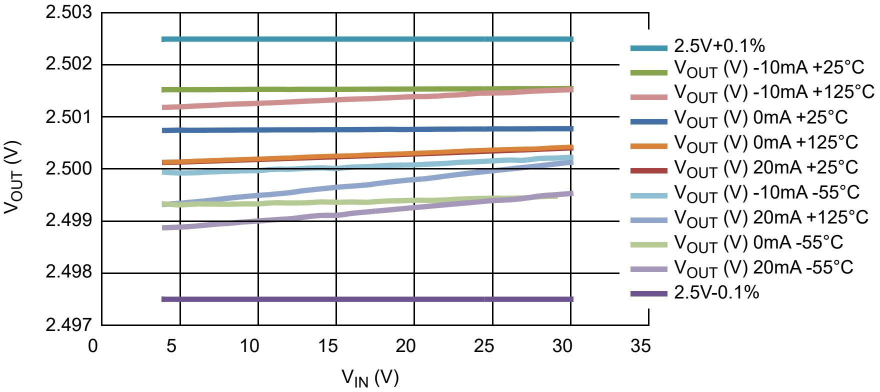


Figure 7. V_{OUT} vs V_{IN} at 0mA, 20mA, and -10mA

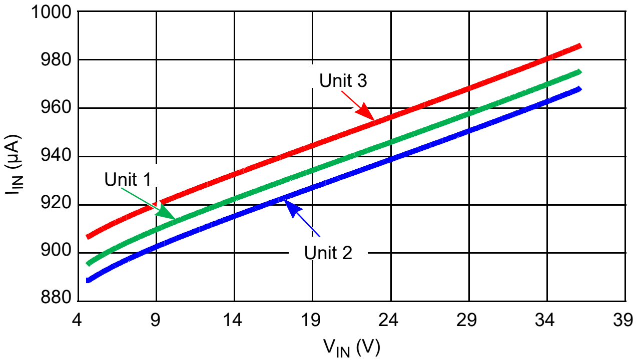


Figure 8. I_{IN} vs V_{IN}, Three Units

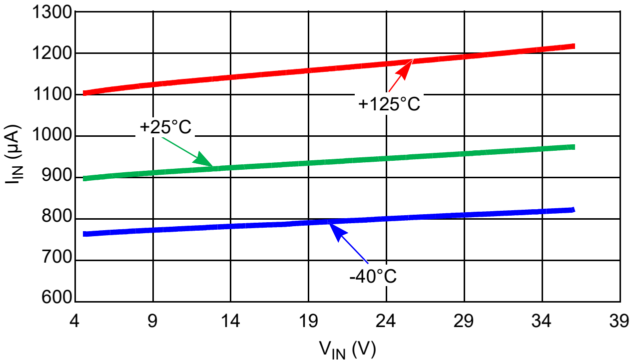


Figure 9. I_{IN} vs V_{IN}, Three Temperatures

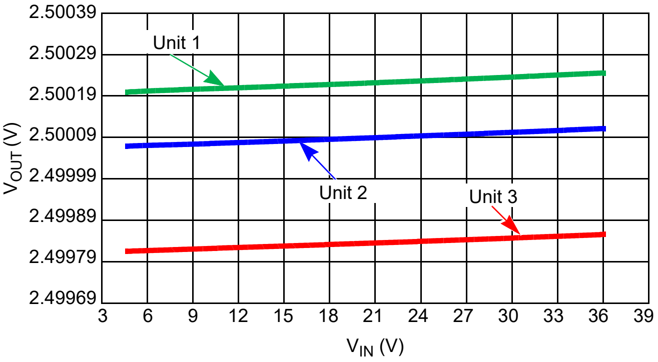


Figure 10. Line Regulation, Three Units

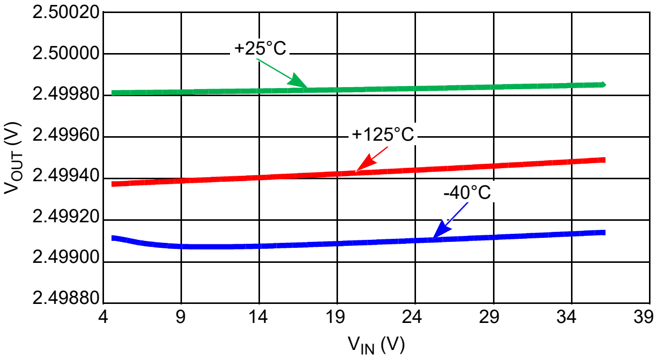


Figure 11. Line Regulation, Three Temperatures

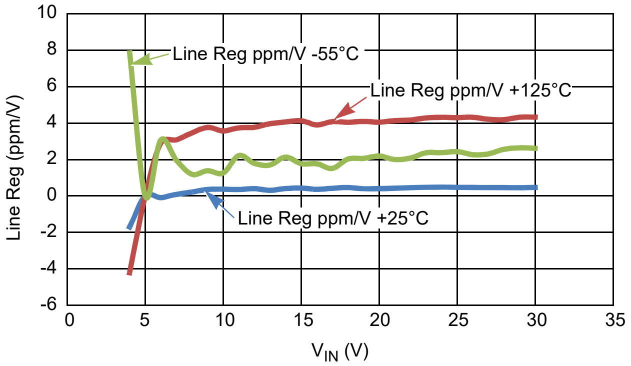


Figure 12. Line Regulation Over-Temperature (0mA)

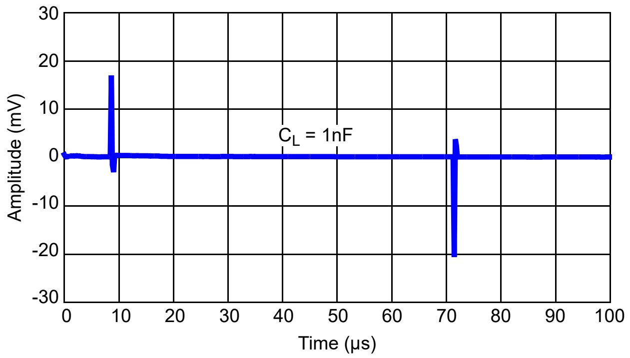


Figure 13. Line Transient with 1nF Load ($\Delta V_{IN} = \pm 500mV$)

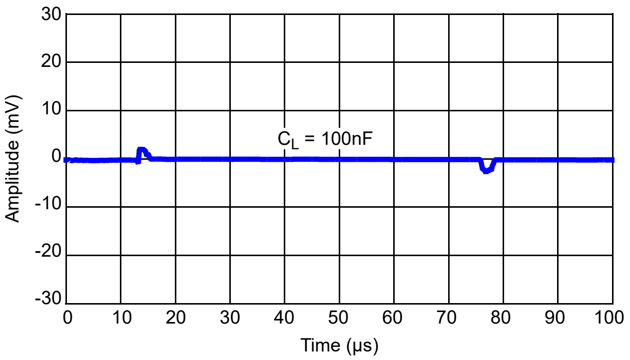


Figure 14. Line Transient with 100nF Load ($\Delta V_{IN} = \pm 500mV$)

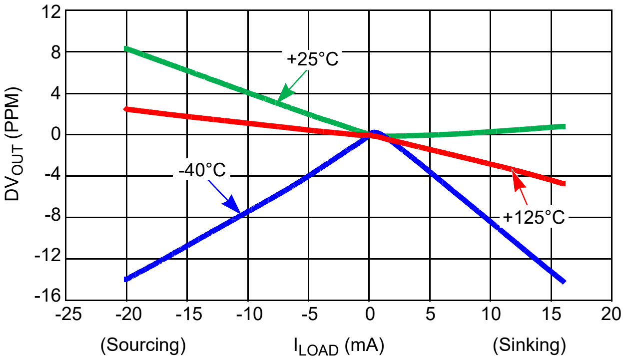


Figure 15. Load Regulation, Three Temperatures

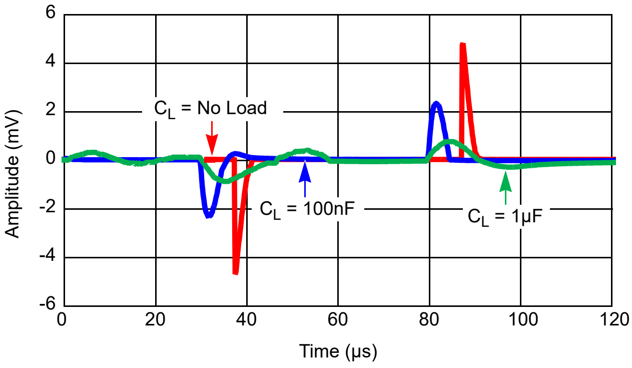


Figure 16. Load Transient (ΔI_{LOAD} = ±1mA)

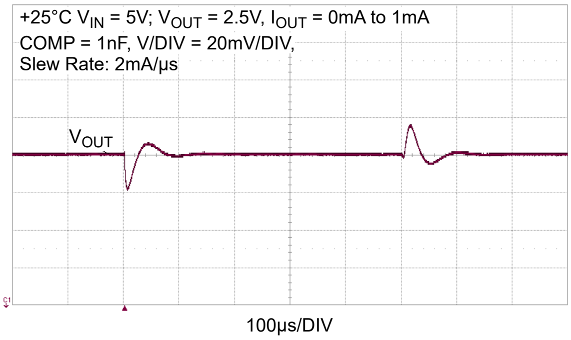


Figure 17. Load Transient (0mA to 1mA)

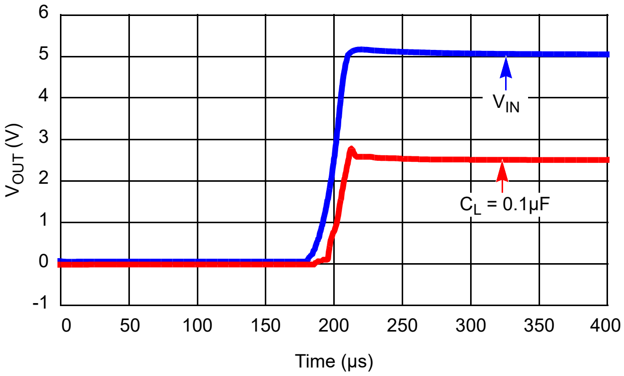


Figure 18. Turn-On Time with 0.1µF

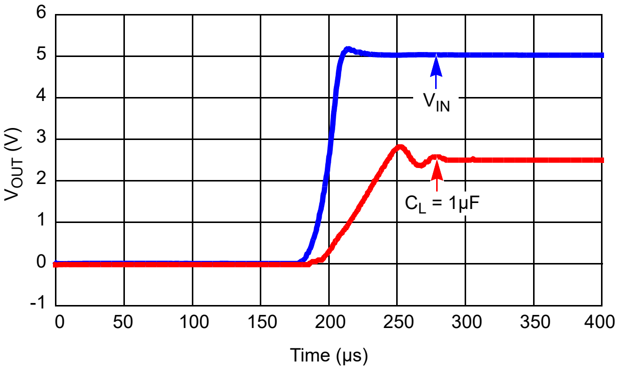


Figure 19. Turn-On Time with 1µF

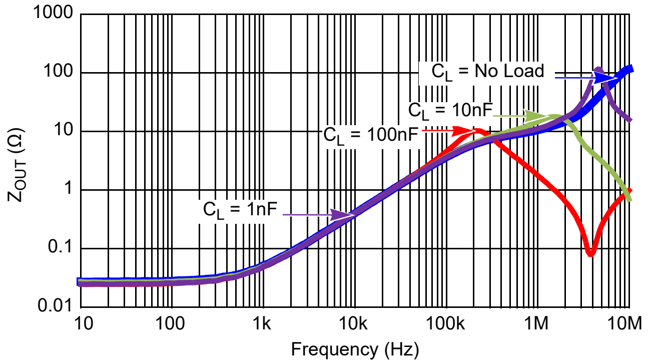


Figure 20. Z_{OUT} vs Frequency

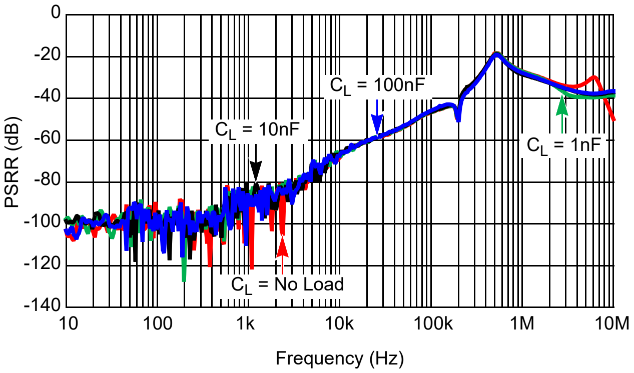


Figure 21. PSRR at Different Capacitive Loads

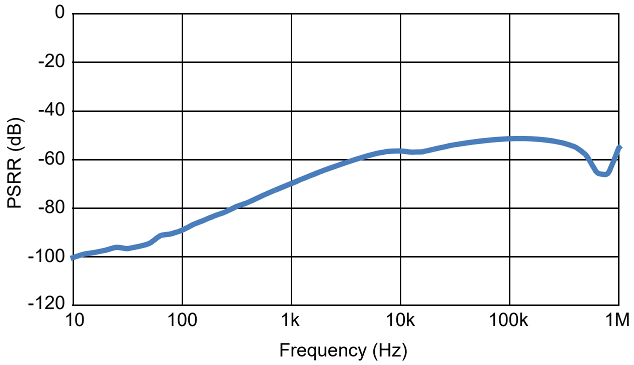


Figure 22. PSRR (+25°C, V_{IN} = 5V, V_{OUT} = 2.5V, I_{OUT} = 0mA, C_{IN} = C_{OUT} = 0.1µF, COMP = 1nF, VSIG = 300mV_{P-P})

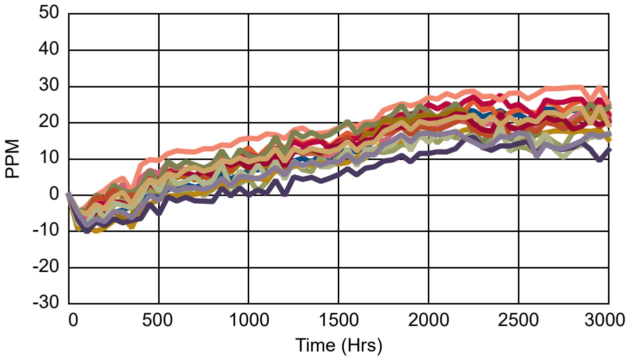


Figure 23. Long Term Stability

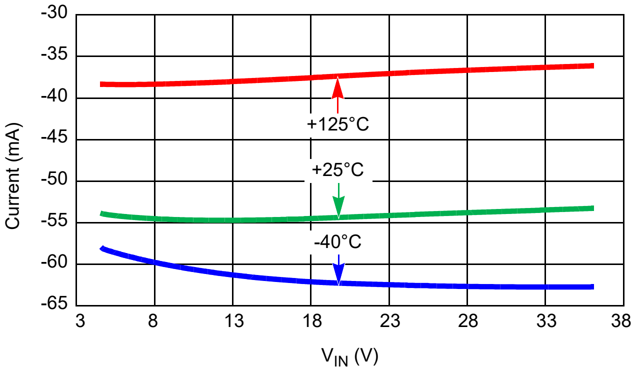


Figure 24. Short-Circuit to GND

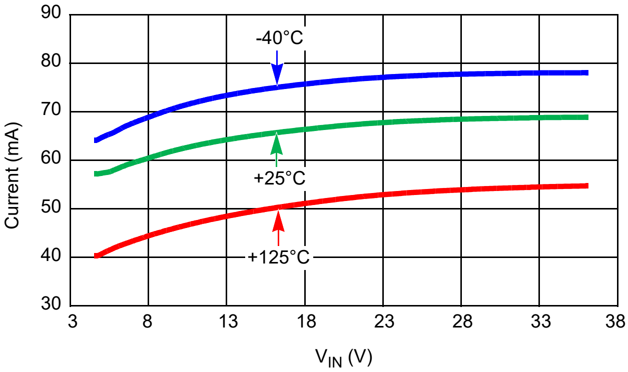


Figure 25. Short-Circuit to V_{IN}

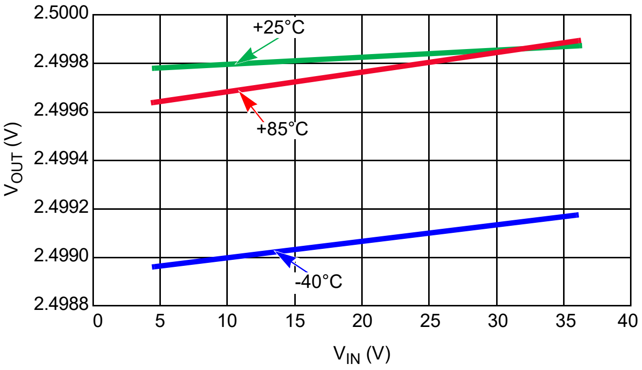


Figure 26. Dropout with -10mA Load

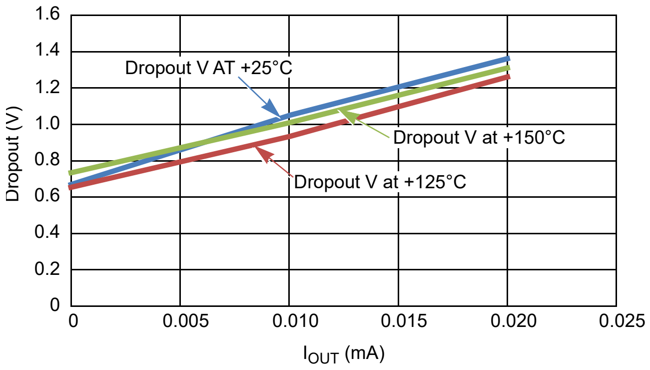


Figure 27. Dropout Voltage for 2.5V

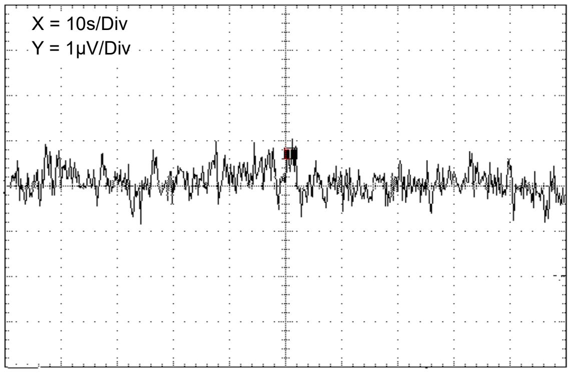


Figure 28. V_{OUT} vs Noise, 0.1Hz to 10Hz

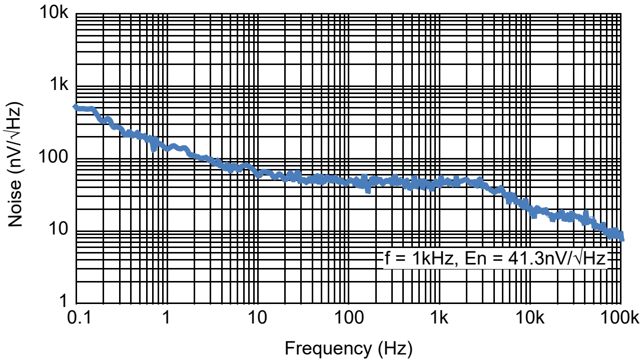


Figure 29. Noise Density vs Frequency (V_{IN} = 5.0V, I_{OUT} = 0mA, C_{IN} = 0.1µF, C_{OUT} = 1µF, COMP = 1nF)

5. Applications Information

5.1 Bandgap Precision Reference

The ISL71010B25 uses a bandgap architecture and special trimming circuitry to produce a temperature compensated, precision voltage reference with high input voltage capability and moderate output current drive. Low noise performance is achieved using optimized biasing techniques. Key features for precision low noise portable applications, such as handheld meters and instruments, are supply current (930µA) and noise (1.9µ$V_{P-P,}$ 0.1Hz to 10Hz bandwidth). Data converters in particular can use the ISL71010B25 as an external voltage reference. Low power DAC and ADC circuits realize maximum resolution with the lowest noise. The device maintains output voltage during conversion cycles with fast response, although it is helpful to add an output capacitor, typically 1µF.

5.2 Board Mounting Considerations

For applications requiring the highest accuracy, the board mounting location should be considered. The device uses a plastic SOIC package, which subjects the die to mild stresses when the Printed Circuit Board (PCB) is heated and cooled, which slightly changes the shape. Because of these die stresses, placing the device in areas subject to slight twisting can degrade the reference voltage accuracy. It is normally best to place the device near the edge of a board, or on the shortest side, because the axis of bending is most limited in that location. Mounting the device in a cutout also minimizes flex. Obviously, mounting the device on flexprint or extremely thin PC material will likewise cause loss of reference accuracy.

5.3 Board Assembly Considerations

Some PCB assembly precautions are necessary. Normal output voltage shifts of 100µV can be expected with Pb-free reflow profiles or wave solder on multi-layer FR4 PCBs. Precautions should be taken to avoid excessive heat or extended exposure to high reflow or wave solder temperatures.

5.4 Noise Performance and Reduction

The output noise voltage in a 0.1Hz to 10Hz bandwidth is typically 1.9µV_{P-P} (V_{OUT} = 2.5V). The noise measurement is made with a bandpass filter. The filter is made of a 1-pole high-pass filter, with a corner frequency at 0.1Hz, and a 2-pole low-pass filter, with a corner frequency (3dB) at 9.9Hz, to create a filter with a 9.9Hz bandwidth. Noise in the 10Hz to 1kHz bandwidth is approximately 1.6µV_{RMS} (V_{OUT} = 2.5V), with 0.1µF capacitance on the output. This noise measurement is made with a 2 decade bandpass filter. The filter is made of a 1-pole high-pass filter with a corner frequency at 10Hz of the center frequency, and 1-pole low-pass filter with a corner frequency at 1kHz. Load capacitance up to 10µF can be added, but will result in only marginal improvements in output noise and transient response.

5.5 Turn-On Time

Normal turn-on time is typically 150µs. The circuit designer must take this into account when looking at power-up delays or sequencing.

5.6 Specifying Temperature Coefficient (Box Method)

The limits stated for temperature coefficient (Tempco) are governed by the method of measurement. The overwhelming standard for specifying the temperature drift of a reference is to measure the reference voltage at two temperatures, which provide for the maximum voltage deviation. Divide the total variation, (V_{HIGH} - V_{LOW}) by the temperature extremes of measurement (T_{HIGH} – T_{LOW}). The result is divided by the nominal reference voltage (at T = +25°C) and multiplied by 10^6 to yield ppm/°C. This is the “Box” method for specifying temperature coefficient.

5.7 Output Voltage Adjustment

The output voltage can be adjusted above and below the factory-calibrated value using the trim terminal. The trim terminal is the negative feedback divider point of the output operational amplifier. The voltage at the TRIM pin is set at approximately 1.216V by the internal bandgap and amplifier circuitry of the voltage reference.

The suggested method to adjust the output is to connect a 1MΩ external resistor directly to the trim terminal and connect the other end to the wiper of a potentiometer that has a 100kΩ resistance and with outer terminals that connect to V_{OUT} and ground. If a 1MΩ resistor is connected to trim, the output adjust range will be ±6.3mV. The TRIM pin should not have any capacitor tied to its output. It is important to minimize the capacitance on the trim terminal during layout to preserve output amplifier stability. It is also best to connect the series resistor directly to the trim terminal, to minimize that capacitance and also to minimize noise injection. Small trim adjustments will not disturb the factory-set temperature coefficient of the reference, but trimming near the extreme values can.

5.8 Output Stage

The output stage of the device has a push-pull configuration with a high-side PNP and a low-side NPN. This helps the device to act as a source and sink. The device can source 20mA and sink 10mA.

5.9 Use of COMP Capacitors

The reference can be compensated for the C_{OUT} capacitors used by adding a capacitor from the COMP pin to GND. See Table 1 for recommended values of the COMP capacitor.

Table 1. COMP Capacitor Recommended Values

C_{OUT} (µF)	C_{COMP} (nF)
0.1	1
1	1
10	10

6. Radiation Tolerance

The ISL71010B25 is a radiation tolerant device for commercial space applications, Low Earth Orbit (LEO) applications, high altitude avionics, launch vehicles, and other harsh environments. This device’s response to Total Ionizing Dose (TID) radiation effects and Single-Event Effects (SEE) has been measured, characterized, and reported in the following sections. The TID performance of the ISL71010B25 is not guaranteed through radiation lot acceptance testing. The ISL71010BM30B25Z is Radiation Lot Acceptance Tested (RLAT) to 30krad(Si), and the ISL71010BM50B25Z is RLAT to 50krad(Si).

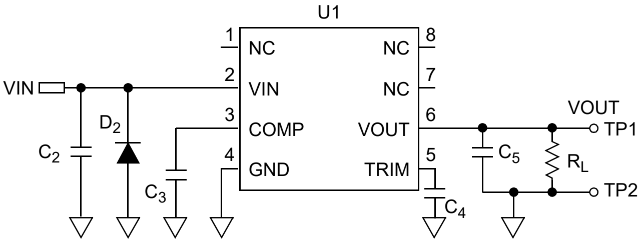
6.1 Total Ionizing Dose (TID) Testing

6.1.1 Introduction

This test was conducted to determine the sensitivity of the part to the total dose environment. Testing was performed on two separate sample sets. For the first sample set, test downpoints were 0krad(Si), 10krad(Si), 20krad(Si), and 30krad(Si). The second sample set was irradiated to 50krad(Si).

Total dose testing was performed using a Hopewell Designs N40 panoramic ^{60}Co irradiator. The irradiations were performed at 10mrad(Si)/s. A PbAl box was used to shield the test fixture and devices under test against low energy secondary gamma radiation.

The characterization matrix of the first sample set consisted of 23 samples irradiated under bias and 12 samples irradiated with all pins grounded. The characterization matrix of the second sample set consisted of 7 samples irradiated under bias and 7 samples irradiated with all pins grounded. Two control units were used to ensure repeatable data. Two different wafers were used. The bias configuration is shown in Figure 30.



Parts:
V_{IN} = +36V ±10%
R_1 = 3.86k, 1%, 1W
R_2 = 470, 1%, 1W
R_L = 5k, 1%, 1/4W

C_2 = 0.1µF, 50V, 10%, X7R
C_3, C_4 = 0.01µF, 50V, 10%, X7R
C_5 = 0.1µF, 10V, 10%, X7R

Figure 30. Irradiation Bias Configuration and Power Supply Sequencing for the ISL71010B25

All electrical testing was performed outside the irradiator using the production Automated Test Equipment (ATE), with data logging at each down point (including anneal). Downpoint electrical testing was performed at room temperature.

6.1.2 Results

Table 2 summarizes the attributes data.

Table 2. ISL71010B25 Total Dose Test Attributes Data

Dose Rate (mrad(Si)/s)	Bias	Sample Size	Down Point	Bin 1[1]	Rejects
10	Figure 30	23	Pre-rad	23	0
			10krad(Si)	23	0
			30krad(Si)	23	0
		7	50krad(Si)	7	0
10	Grounded	12	Pre-rad	12	0
			10krad(Si)	12	0
			30krad(Si)	12	0
		7	50krad(Si)	7	0

1. Bin 1 indicates a device that passes all datasheet specification limits

The plots in Figure 31 to Figure 36 show data for key parameters at all down points. The plots show the average as a function of total dose for each of the irradiation conditions. The error bars, if visible, show the minimum and maximum measured values. All parts showed excellent stability over irradiation.

Table 3 shows the average of the key parameters with respect to total dose in tabular form.

6.2 Data Plots

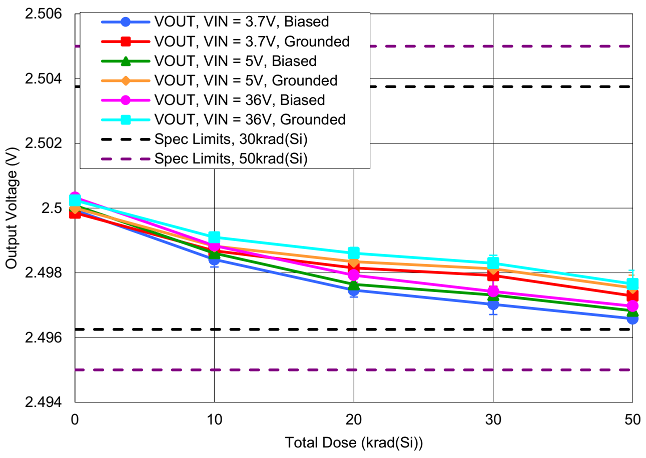


Figure 31. V_{REF} Output Voltage vs TID

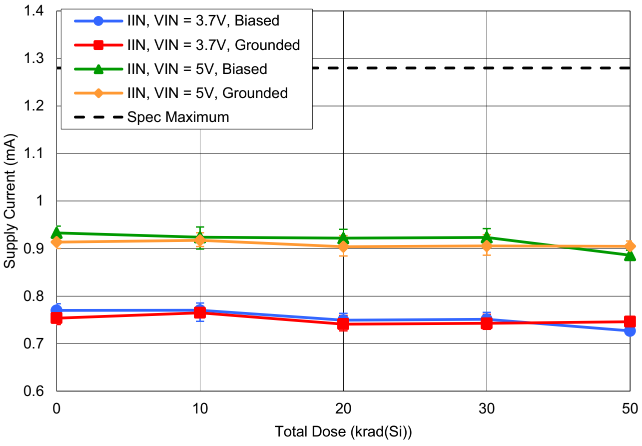


Figure 32. Supply Current vs TID

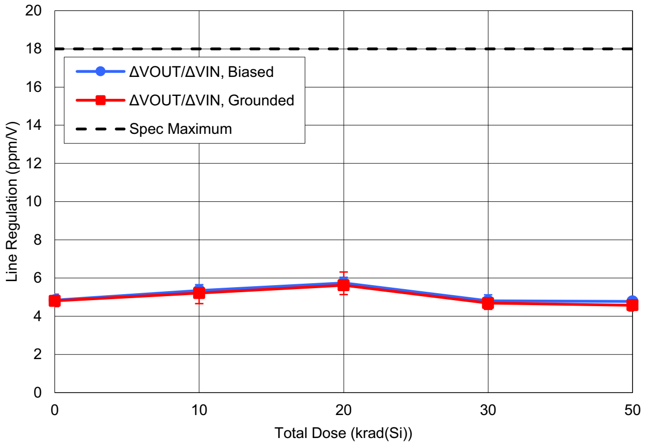


Figure 33. Line Regulation vs TID

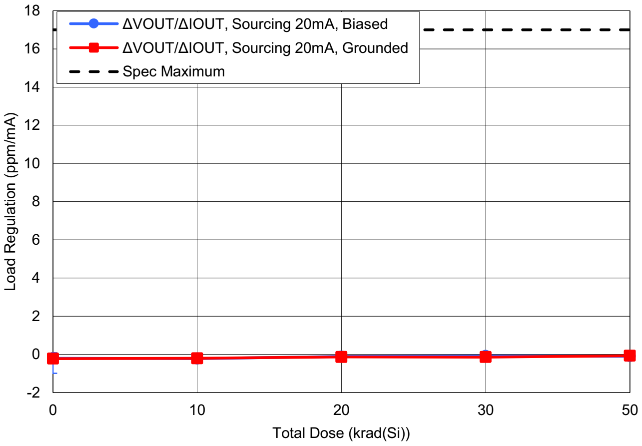


Figure 34. Load Regulation 20mA Sourcing vs TID

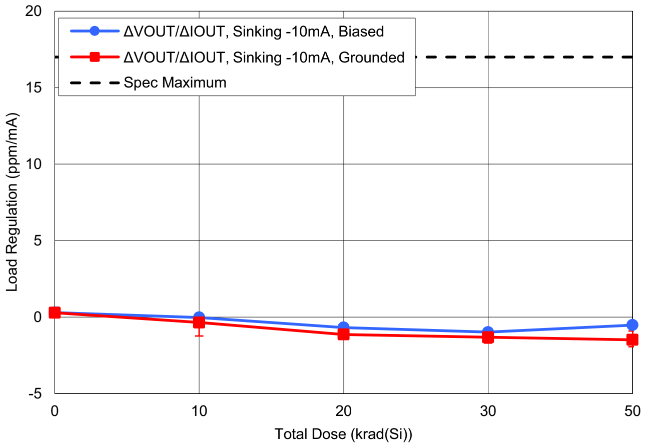


Figure 35. Load Regulation -10mA Sinking vs TID

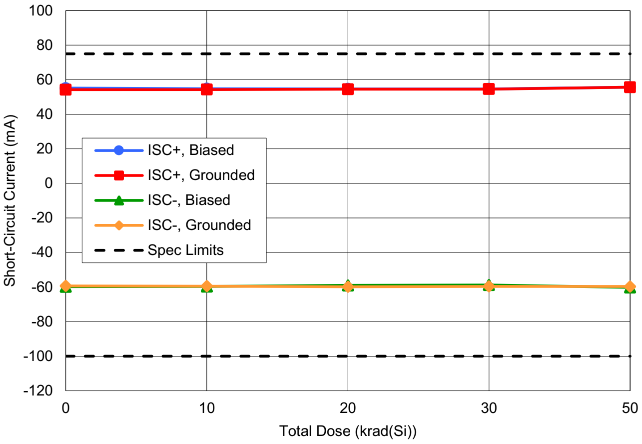


Figure 36. Short-Circuit Current vs TID

6.2.1 Conclusion

ATE characterization testing showed no rejects to the datasheet limits at all down points. Variables data for selected parameters is presented in Figure 31 to Figure 36. No differences between biased and unbiased irradiation were noted, and the part is not considered bias sensitive.

Table 3. ISL71010B25 Response of Key Parameters vs TID

Parameter	Symbol	Condition	Bias	0krad(Si)	10krad(Si)	20krad(Si)	30krad(Si)	50krad(Si)	Unit
Output Voltage	V_{OUT}	V_{IN} = 3.7V	Bias	2.499935	2.498409	2.497462	2.497026	2.496583	V
			Grounded	2.499851	2.498677	2.498152	2.497917	2.497285	V
		V_{IN} = 5V	Bias	2.50008	2.498605	2.497645	2.497313	2.496827	V
			Grounded	2.50000	2.498824	2.498346	2.498124	2.497534	V
		V_{IN} = 36V	Bias	2.500326	2.49884	2.497926	2.497422	2.496968	V
			Grounded	2.500239	2.499098	2.498607	2.498295	2.497655	V
Supply Current	I_{IN}	V_{IN} = 3.7V	Bias	0.769745	0.770239	0.74926	0.751033	0.726834	mA
			Grounded	0.753588	0.764798	0.740917	0.742755	0.746205	mA
		V_{IN} = 5V	Bias	0.932934	0.923849	0.921882	0.923466	0.886037	mA
			Grounded	0.913717	0.917348	0.903889	0.905463	0.904745	mA
Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = 4V to 30V, V_{OUT} = 2.5V	Bias	4.843192	5.347662	5.743502	4.806794	4.777919	ppm/V
			Grounded	4.806634	5.213798	5.626061	4.687299	4.575793	ppm/V
Load Regulation	$\Delta V_{OUT}/\Delta I_{OUT}$	20mA Sourcing	Bias	-0.19286	-0.21943	-0.10849	-0.07873	-0.09162	ppm/mA
			Grounded	-0.22109	-0.20001	-0.12771	-0.13486	-0.06687	ppm/mA
		-10mA Sinking	Bias	0.296484	-0.02579	-0.68384	-0.97837	-0.5177	ppm/mA
			Grounded	0.285307	-0.34957	-1.13324	-1.31472	-1.48525	ppm/mA
Short-Circuit Current	I_{SC+}	V_{OUT} = GND	Bias	55.14103	54.81855	54.66817	54.69348	55.6684	mA
			Grounded	54.2462	54.32929	54.5196	54.54143	55.67061	mA
	I_{SC-}	V_{OUT} = V_{IN}	Bias	-59.8068	-59.6621	-59.0124	-58.7974	-60.17	mA
			Grounded	-59.3318	-59.485	-59.8141	-59.6128	-59.678	mA

6.3 Single-Event Effects Testing

6.3.1 Introduction

The intense heavy ion environment encountered in space applications can cause a variety of Single-Event Effects (SEE). SEE can lead to system-level performance issues including disruption, degradation, and destruction. For predictable and reliable space system operation, individual electronic components should be characterized to determine their SEE response. The following is a summary of the ISL71010B25 SEE testing.

6.3.2 SEE Test Setup

Testing was performed at the Texas A&M University (TAMU) Cyclotron Institute heavy ion facility.

A schematic of the ISL71010B25 SEE test circuit is shown in Figure 43. The test circuit is configured to accept an input voltage from 4V to 30V and generate the 2.5V nominal output voltage. The output current of the reference was adjusted using fixed load resistors on test board. The output capacitor, C_4, and the compensation capacitor C_2 were 0.1µF and 1nF, respectively.

Digital multimeters were used to monitor input voltage (V_{IN}), output voltage (V_{OUT}), and input current (I_{IN}). A LeCroy Waverunner digital oscilloscope was used to monitor, capture and store key signal waveforms. The scope was configured to trigger with V_{OUT} signal levels of ±20mV.

6.3.3 SEB Testing Results

For the SEB tests, conditions were selected to maximize the electrical and thermal stresses on the Device Under Test (DUT), thus insuring worst-case conditions. The input voltage (V_{IN}) was initially set to 35V and then increased in 1V increments. The output current (I_{OUT}) was set to 20mA which is the maximum recommended current rating for load regulation of the device. Case temperature was maintained at +125ºC by controlling the current flowing into a resistive heater bonded to the underside of the DUT. Four DUTs were irradiated with Ag ions at a normal incident angle, resulting in an effective LET of 43MeV•cm^2/mg.

The failure criterion for destructive SEE was an increase in operating input current (I_{IN}) greater than 5% measured at 20mA output current. I_{IN} is defined as the total current drawn by the device. Failed devices were not further irradiated.

Four parts passed irradiation to 1x10^7 ions/cm^2 with 43MeV•cm^2/mg at 39V and +125ºC case temperature.

6.3.4 Single-Event Transient Testing

SET testing was done on four samples of the ISL71010B25, which were irradiated at room temperature across a range of LET from 2.7MeV•cm^2/mg to 28MeV•cm^2/mg to observe SET performance. Samples were separately tested to V_{IN} of 4V and 30V. The parts were configured with a 0.1µF output capacitor, a 1nF compensation capacitor, and a 20mA load current to set up the worst conditions for negative going transients. Table 4 shows the SET summary giving the cross section for each input voltage and LET level.

Figure 37 to Figure 42 represent output waveform responses of the DUTs at the respective bias conditions and LET levels. The plots are composites of all the transients captured on the scope.

The worst case SET appeared for the case of LET = 28 and V_{IN} = 30V with about 235mV in negative SET and a recovery time of about 20µs.

Table 4. SET Summary of the Fully Functional ISL71010B25[1]

Supply Voltage (V)	Ion/Angle	Eff LET (MeV•cm^2/mg)	Fluence per Run (Particles/cm^2)	Number of Runs	Total SET	Events CS (cm^2)
4	Ne/0	2.7	2.00E+06	4	40	5.00E-06
30	Ne/0	2.7	2.00E+06	4	6	7.50E-07
4	Ar/0	8.5	2.00E+06	4	256	3.20E-05
30	Ar/0	8.5	2.00E+06	4	365	4.56E-05
4	Kr/0	28	2.00E+06	4	439	5.49E-05
30	Kr/0	28	2.00E+06	4	754	9.43E-05

1. Samples at 4.0V and 30V input voltage, C_{OUT} = 0.1µF, C_{COMP} = 1nF and I_{OUT} = 20mA. Trigger level for the output voltage set to ±20mV.

6.3.5 Data Plots

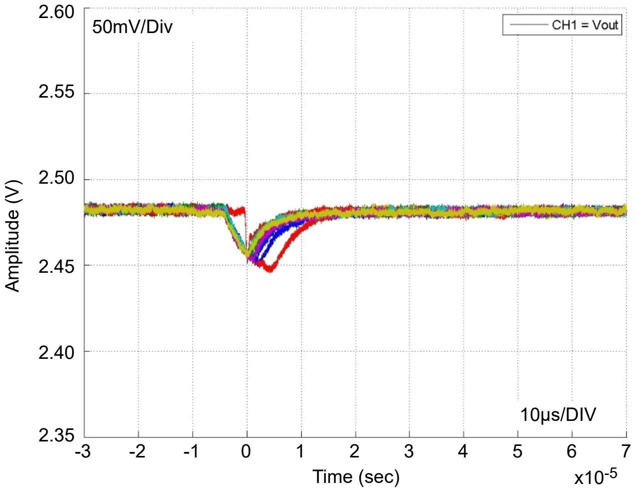


Figure 37. Composite SET Plot for ISL71010B25 at LET 2.7 V_{IN} = 4V, I_{OUT} = 20mA, C_{OUT} = 0.1µF, C_{COMP} = 1nF

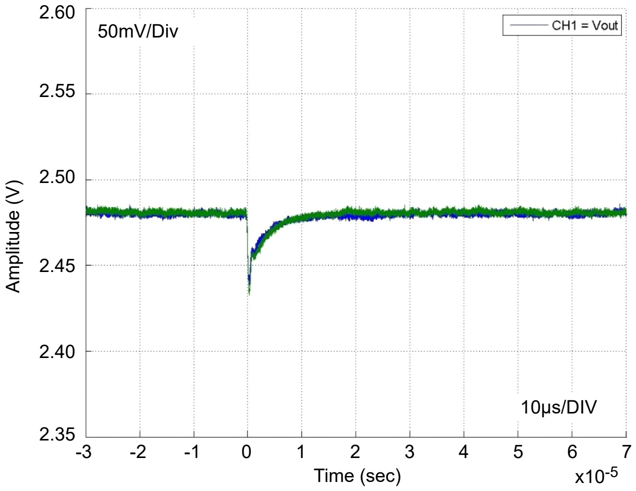


Figure 38. Composite SET Plot for ISL71010B25 at LET 2.7 V_{IN} = 30V, I_{OUT} = 20mA, C_{OUT} = 0.1µF, C_{COMP} = 1nF

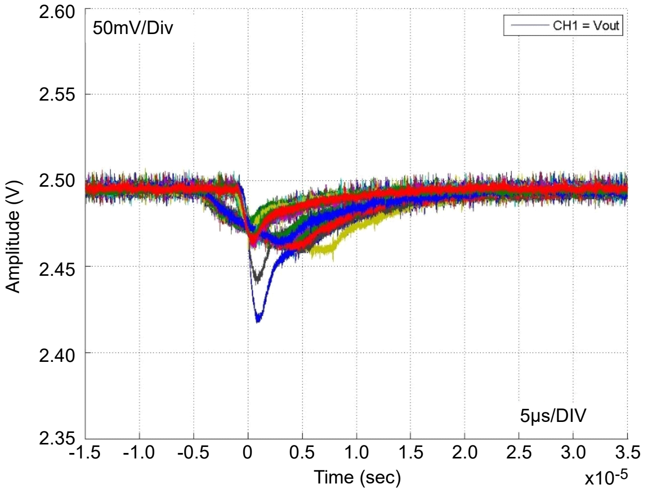


Figure 39. Composite SET Plot for ISL71010B25 at LET 8.5 V_{IN} = 4V, I_{OUT} = 20mA, C_{OUT} = 0.1µF, C_{COMP} = 1nF

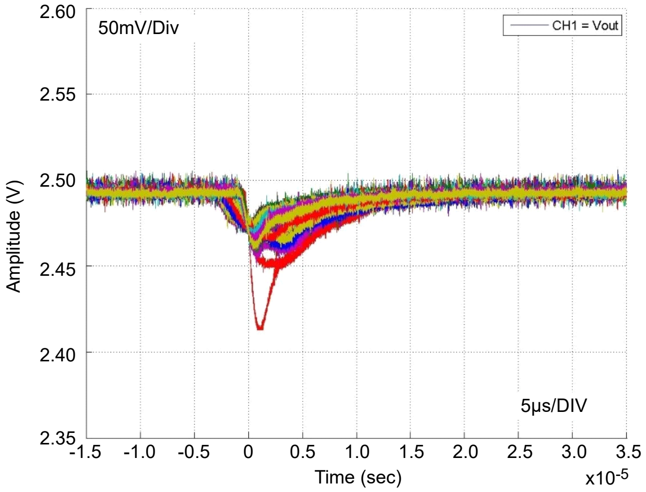


Figure 40. Composite SET Plot for ISL71010B25 at LET 8.5 V_{IN} = 30V, I_{OUT} = 20mA, C_{OUT} = 0.1µF, C_{COMP} = 1nF

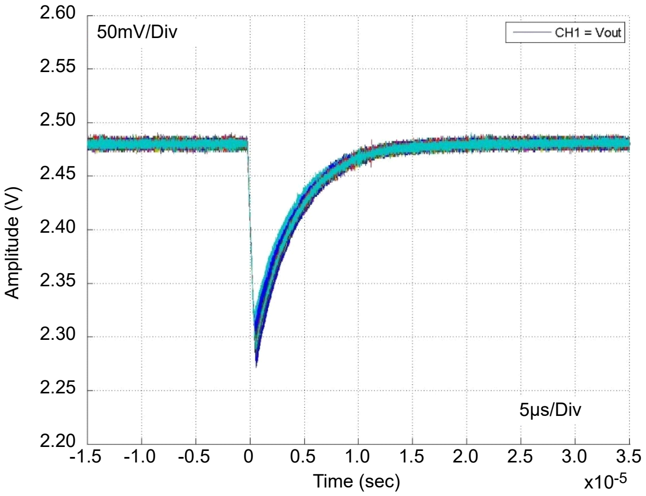


Figure 41. Composite SET Plot for ISL71010B25 at LET 28 V_{IN} = 4V, I_{OUT} = 20mA, C_{OUT} = 0.1µF, C_{COMP} = 1nF

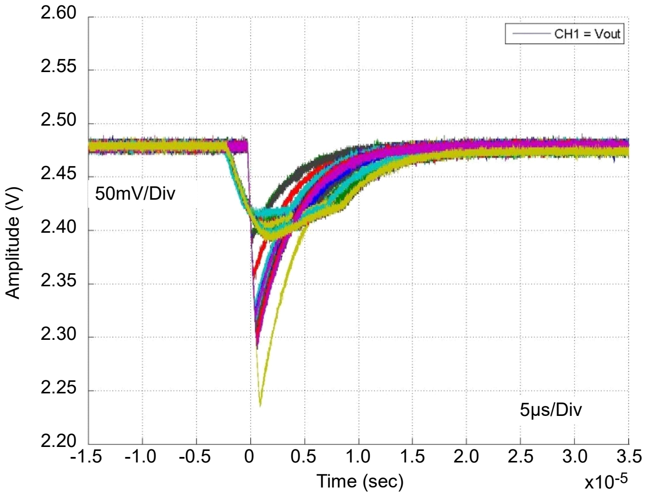


Figure 42. Composite SET Plot for ISL71010B25 at LET 28 V_{IN} = 30V, I_{OUT} = 20mA, C_{OUT} = 0.1µF, C_{COMP} = 1nF

6.3.6 Conclusion

SEE testing has demonstrated that the ISL71010B25 is not susceptible to Single Event Burnout (SEB) at an LET of 43MeV•cm^2/mg with an input voltage of 39V and a load current of 20mA. This represents conditions that are over 30% above the recommended input voltage of 30V and 100% of the load regulation drive capability of the IC (20mA).

SET testing demonstrated that all transients are negative and the higher the LET level, the greater the magnitude of the negative transient. At LET = 28MeV•cm^2/mg and V_{IN} = 30V with C_{OUT} = 0.10µF, showed a 235mV negative transient during an SET event. The longest recovery times were about 20µs.

A larger C_{OUT} capacitance value will suppress the SET magnitude but the SET disturbance duration will stretch out. Capacitor selection represents a compromise between SET magnitude and recovery duration.

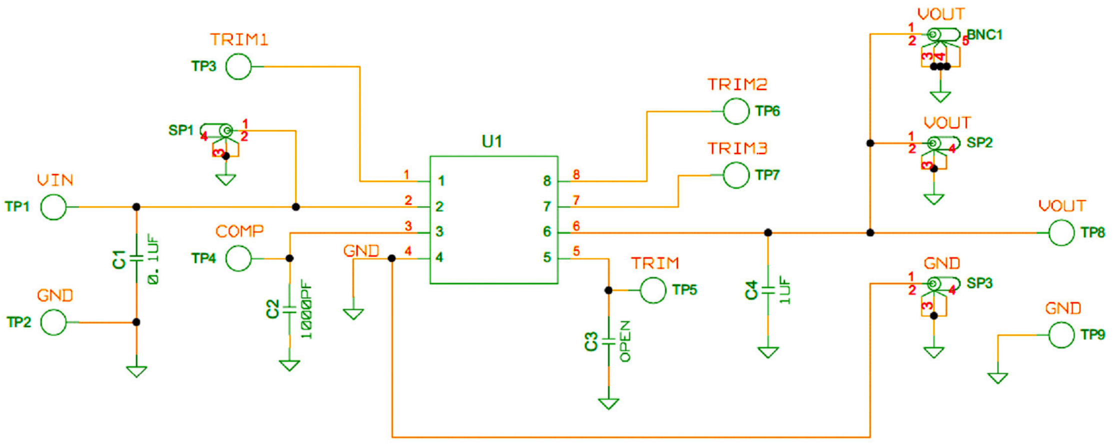


Figure 43. SEE Testing Schematic for the ISL71010B25

7. Package Outline Drawing

The package outline drawing is located at the end of this document and is accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

8. Ordering Information

Part Number[1][2]	Part Marking	Radiation Lot Acceptance Testing	V_{OUT} Option (V)	Accuracy (%)	Tempco (ppm/°C)	Carrier Type[3]	Package Description[4] (RoHS Compliant)	Pkg. Dwg. #	Temp Range
ISL71010BMB25Z	71010 BMZ25	N/A	2.50	±0.05	10	Tube	8 Ld SOIC	M8.15	-55 to +125°C
ISL71010BMB25Z-TK						Reel, 1k			
ISL71010BM30B25Z	71010 BMZ25	30krad(Si)	2.50	±0.15	10	Tube	8 Ld SOIC	M8.15	-55 to +125°C
ISL71010BM30B25Z-TK						Reel, 1k			
ISL71010BM50B25Z	71010 BMZ25	50krad(Si)	2.50	±0.20	10	Tube	8 Ld SOIC	M8.15	-55 to +125°C
ISL71010BM50B25Z-TK						Reel, 1k			
ISL71010BM25EV1Z	Evaluation Board								

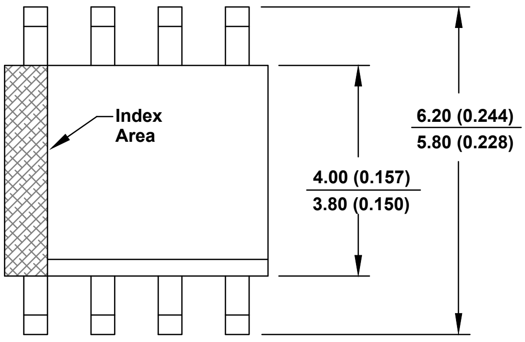
1. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials and NiPdAu-Ag plate-e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. For Moisture Sensitivity Level (MSL), see the ISL71010B25 product information page. For more information about MSL refer to TB363.
3. See TB347 for details about reel specifications.
4. For the Pb-Free Reflow Profile, see TB493.

9. Revision History

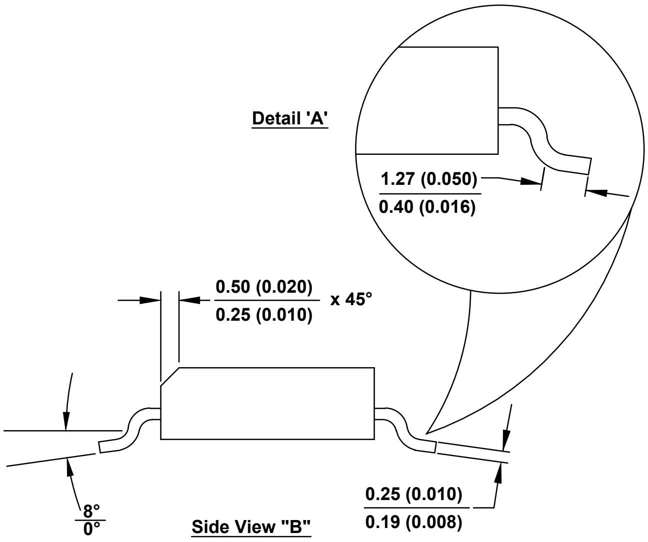
Revision	Date	Description
1.01	Sep 18, 2025	Applied latest template. Added M30 and M50 part information throughout. Updated Radiation bullets. Updated Radiation Tolerance sections. Updated POD M8.15 to the latest version. Updated Ordering Information table.
1.00	Apr 12, 2018	Added Outgassing Feature bullet. Updated Ordering information by adding -TK part to table and updated Note 1. Added Outgassing specification information. Removed About Intersil and updated disclaimer.
0.00	Sep 26, 2017	Initial release

Package Outline Drawing

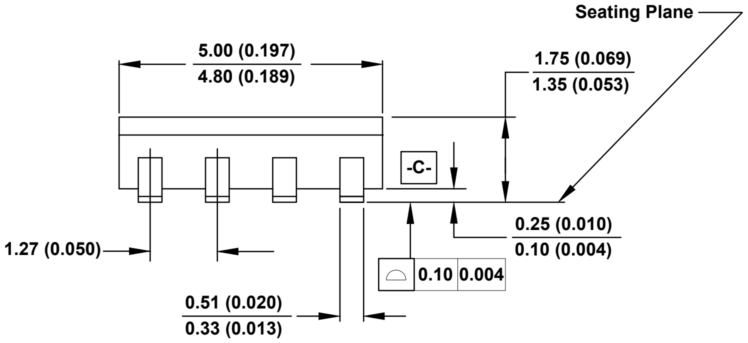
M8.15
GS0008AC
8-Lead Narrow Body Small Outline Plastic Package 4.90 x 3.90 x 1.43 mm Body, 1.27 mm Pitch
Rev08, Jul 7, 2025



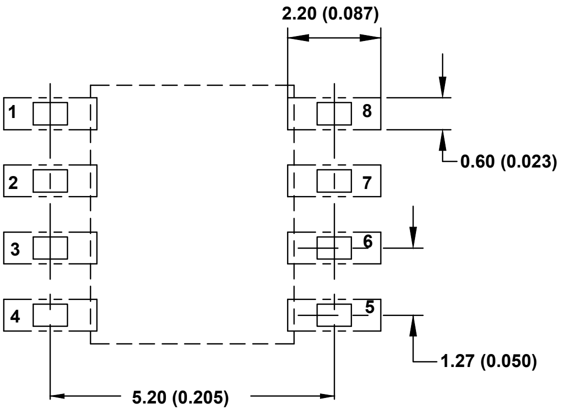
Top View



Side View "B"



Side View "A"



Typical Recommended Land Pattern

Notes:

1. Dimensioniong and tolerancing conform to ASME Y14.5M-1994.
2. Package length does not include mold flash, protrusion or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
7. Controlling dimension: MILLIMETER. Converted inch dimension are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.

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