ISL71091SEH33

3.3V Radiation Hardened Ultra Low Noise, Precision Voltage Reference

The ISL71091SEH33 is an ultra low noise, high DC accuracy precision voltage reference with a wide input voltage range from 4.6V to 30V. It uses advanced bipolar technology to achieve 5.2µV_{P-P} 0.1Hz to 10Hz noise with an initial voltage accuracy of 0.05%.

The ISL71091SEH33 offers a 3.3V output voltage option with 6ppm/°C temperature coefficient and also provides excellent line and load regulation. The device is offered in an 8 Ld flatpack package.

The ISL71091SEH33 is ideal for high-end instrumentation, data acquisition and processing applications requiring high DC precision where low noise performance is critical.

Applications

- Precision voltage sources for data acquisition system for space applications
- Strain and pressure gauge for space applications
- Radiation hardened PWM requiring precision outputs

Features

- Reference output voltage: 3.3V ±0.05%
- Accuracy over temperature: ±0.15%
- Accuracy over radiation: ±0.25%
- Output voltage noise: 5.2µV_{P-P} typical (0.1Hz to 10Hz)
- Supply current: 300µA (typical)
- V_{OS} temperature coefficient: 6ppm/°C maximum
- Output current capability: 10mA/-5mA
- Line regulation: 5ppm/V maximum
- Load regulation (sourcing): 25ppm/mA maximum
- Operating temperature range: -55°C to +125°C
- Radiation acceptance testing (see TID report)
  - High dose rate (50-300rad(Si)/s): 100krad(Si)
  - Low dose rate (0.01rad(Si)/s): 50krad(Si)
- SEE hardness (see SEE report for details)
  - SET/SEL/SEB (V_{CC} = 36V): 86MeV•cm^2/mg
- Electrically screened to SMD 5962-14208

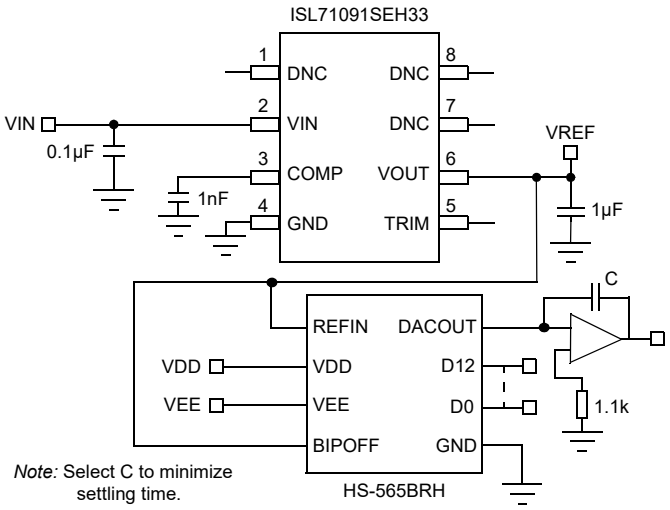


Figure 1. ISL71091SEH33 Typical Application Diagram

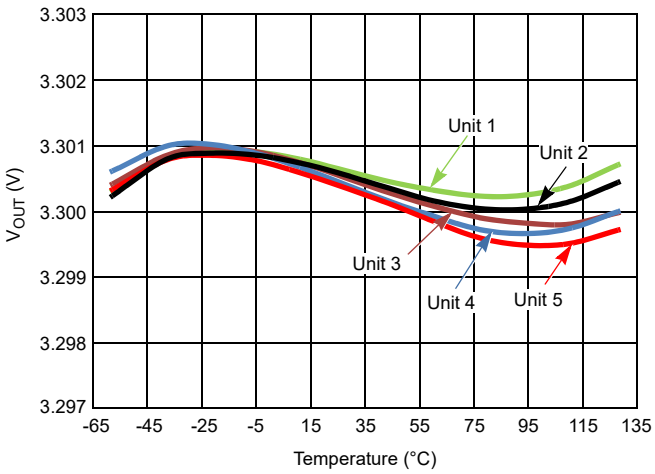


Figure 2. V_{OUT} vs Temperature

Contents

1. Overview

1.1 Functional Block Diagram

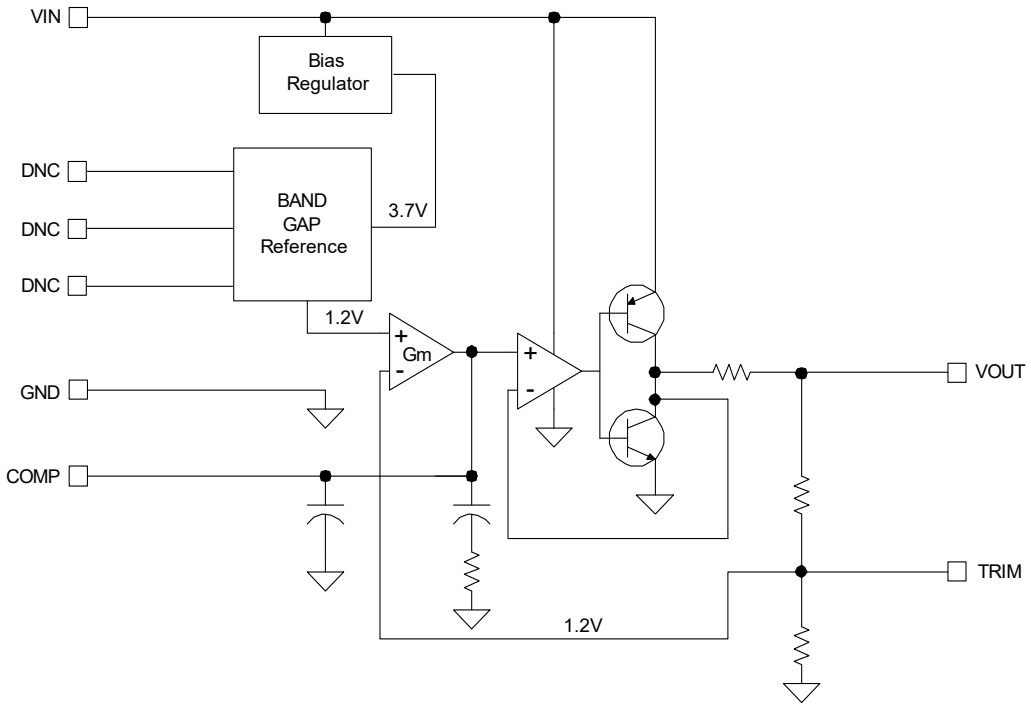


Figure 3. Functional Block Diagram

1.2 Typical Trim Application Diagram

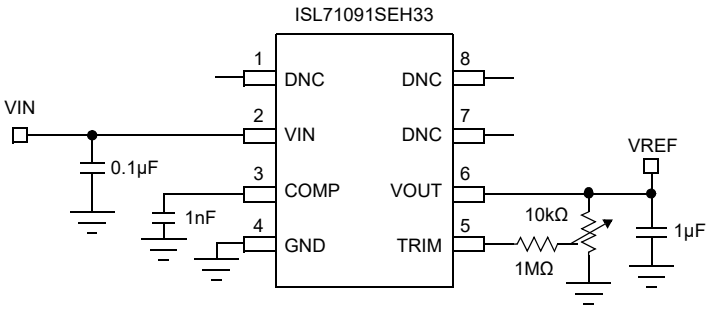
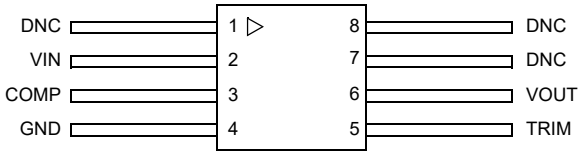


Figure 4. Typical Trim Application Diagram

2. Pin Information

2.1 Pin Assignments

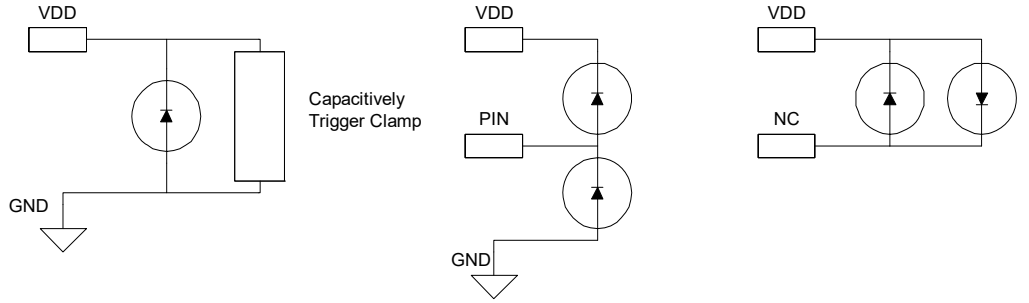


Note: The ESD triangular mark is indicative of pin #1. It is part of the device marking and is placed on the lid in the quadrant where pin #1 is located.

Figure 5. Pin Assignments - Top View

2.2 Pin Descriptions

Pin Number	Pin Name	ESD Circuit	Description
1, 7, 8	DNC	3	Do not connect. Internally terminated.
2	VIN	1	Input voltage connection.
3	COMP	2	Compensation and noise reduction capacitor.
4	GND	1	Ground connection. Also connected to the lid.
5	TRIM	2	Voltage reference trim input.
6	VOUT	2	Voltage reference output.



3. Specifications

3.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
VIN to GND	-0.5	40	V
VIN to GND at an LET = 86MeV•cm^2/mg	-0.5	36	V
VOUT to GND (10s)	-0.5	V_{OUT} + 0.5V	V
Voltage on any Pin to Ground	-0.5	V_{OUT} + 0.5V	V
Voltage on DNC Pins[1]	-	-	-
Maximum Junction Temperature	-	+150	°C
Maximum Storage Temperature Range	-65	+150	°C
Human Body Model (Tested per MIL-PRF-883 3015.7)	-	2	kV
Machine Model (Tested per JESD22-A115-A)	-	200	V
Charged Device Model (Tested per JESD22-C101D)	-	750	V

1. No connections permitted to these pins.

3.2 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Input Voltage, V_{IN}	4.6	30	V
Ambient Temperature	-55	+125	°C

3.3 Thermal Specifications

Parameter	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance	8 Ld Flatpack Package	θ_{JA}[1]	Junction to ambient	135	°C/W
		θ_{JC}[2]	Junction to case	11	°C/W

1. θ_{JA} is measured with the component mounted on a high-effective thermal conductivity test board in free air. See TB379 for details.
2. For θ_{JC}, the case temperature location is the center of the ceramic on the package underside.

3.4 Electrical Specifications

3.4.1 Flatpack Packaged Device

V_{IN} = 5V, I_{OUT} = 0mA, C_L = 1µF and C_{COMP} = 0.001µF unless otherwise specified. **Boldface limits apply after radiation at +25°C and across the operating temperature range, -55°C to +125°C without radiation, unless otherwise specified.**

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Output Voltage	V_{OUT}	-	-	3.3	-	V
V_{OUT} Accuracy	V_{OA}	V_{OUT} = 3.3V[2], T_A = +25°C	-0.05	-	+0.05	%
		V_{OUT} = 3.3V[2], T_A = -55°C to +125°C	**-0.15**	-	**+0.15**	%
		V_{OUT} = 3.3V[2], T_A = +25°C, Post Radiation	-0.25	-	+0.25	%
Output Voltage Temperature Coefficient[3]	TC V_{OUT}	-	-	-	**6**	ppm/°C
Input Voltage Range	V_{IN}	V_{OUT} = 3.3V	**4.6**		**30**	V
Supply Current	I_{IN}	-	-	0.3	**0.5**	mA
Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = 4.6V to 30V, V_{OUT} = 3.3V	-	0.3	**5**	ppm/V
Load Regulation	$\Delta V_{OUT}/\Delta I_{OUT}$	Sourcing: 0mA ≤ I_{OUT} ≤ 10mA	-	11	**25**	ppm/mA
		Sinking: -5mA ≤ I_{OUT} ≤ 0mA	-	25	**60**	
Dropout Voltage[4]	V_D	I_{OUT} = 10mA	-	1.1	**1.6**	V
Short-Circuit Current	I_{SC+}	T_A = +25°C, V_{OUT} tied to GND	-	55	-	mA
Short-Circuit Current	I_{SC-}	T_A = +25°C, V_{OUT} tied to V_{IN}	-	-61	-	mA
Turn-On Settling Time	t_R	90% of final value, C_L = 1.0µF, C_C = 1000pF	-	250	-	µs
Ripple Rejection	PSRR	f = 120Hz	-	90	-	dB
Output Voltage Noise	$e_N V_{P-P}$	0.1Hz ≤ f ≤ 10Hz, V_{OUT} = 3.3V	-	5.2	-	μV_{P-P}
Broadband Voltage Noise	$e_N V_{RMS}$	10Hz ≤ f ≤ 1kHz, V_{OUT} = 3.3V	-	5.8	-	μV_{RMS}
Noise Density	e_N	f = 1kHz, V_{OUT} = 3.3V	-	91	-	$nV/\sqrt{Hz}$
Long Term Stability	$\Delta V_{OUT}/\Delta t$	T_A = +25°C, 1000 hours	-	20	-	ppm

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
2. Post-reflow drift for the ISL71091SEH33 devices can exceed 100µV based on experimental results with devices on FR4 double-sided boards. The engineer must take this into account when considering the reference voltage after assembly.
3. Over the specified temperature range. Temperature coefficient is measured by the box method whereby the change in V_{OUT} is divided by the temperature range; in this case, -55°C to +125°C = +180°C.
4. Dropout Voltage is the minimum V_{IN} - V_{OUT} differential voltage measured at the point where V_{OUT} drops 1mV from V_{IN} = nominal at T_A = +25°C.

3.4.2 Die

V_{IN} = 5V, I_{OUT} = 0, C_L = 1µF and C_{COMP} = 0.001µF unless otherwise specified. **Boldface limits apply after radiation at +25°C and across the operating temperature range, -55°C to +125°C without radiation, unless otherwise specified. Specifications over temperature are guaranteed but not production tested on die.**

Parameter	Symbol	Conditions	Min[1]	Typ	Max[1]	Unit
Output Voltage	V_{OUT}	-	-	3.3	-	V
V_{OUT} Accuracy	V_{OA}	V_{OUT} = 3.3V[2], T_A = +25°C	-0.05	-	+0.05	%
		V_{OUT} = 3.3V[2], T_A = -55°C to +125°C	**-0.15**	-	**+0.15**	
		V_{OUT} = 3.3V[2], T_A = +25°C, Post Radiation	-0.25	-	+0.25	
Output Voltage Temperature Coefficient [3]	TC V_{OUT}	-	-	-	**6**	ppm/°C
Input Voltage Range	V_{IN}	V_{OUT} = 3.3V	**4.6**	-	**30.0**	V
Supply Current	I_{IN}	-	-	0.3	**0.5**	mA
Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = 4.6V to 30V	-	0.3	**5.0**	ppm/V
Load Regulation	$\Delta V_{OUT}/\Delta I_{OUT}$	Sourcing: 0mA ≤ I_{OUT} ≤ 10mA	-	11	**25**	ppm/mA
		Sinking: -5mA ≤ I_{OUT} ≤ 0mA	-	25	**60**	
Dropout Voltage[4]	V_D	I_{OUT} = 10mA	-	1.1	**1.6**	V

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
2. The V_{OUT} accuracy is based on die mount with Silver Glass die attach material such as QMI 2569 or equivalent in a package with an Alumina ceramic substrate.
3. Over the specified temperature range. Temperature coefficient is measured by the box method whereby the change in V_{OUT} is divided by the temperature range; in this case, -55°C to +125°C = +180°C.
4. Dropout Voltage is the minimum V_{IN} - V_{OUT} differential voltage measured at the point where V_{OUT} drops 1mV from V_{IN} = nominal at T_A = +25°C.

4. Total Dose Radiation Characteristics

This data is typical mean test data post total dose radiation exposure at both low dose rate (LDR) of <10mrad(Si)/s to 50krads and at a high dose rate (HDR) of 50 to 300rad(Si)/s to 100krads. This data is intended to show typical parameter shifts due to low dose rate radiation. These are not limits nor are they guaranteed. LDR data to 150krads will be added when available. V_{IN} = 5V, T_A = +25°C, I_{OUT} = 0, C_{IN} = 0.1µF, C_L = 1µF and C_{COMP} = 0.001µF unless otherwise specified.

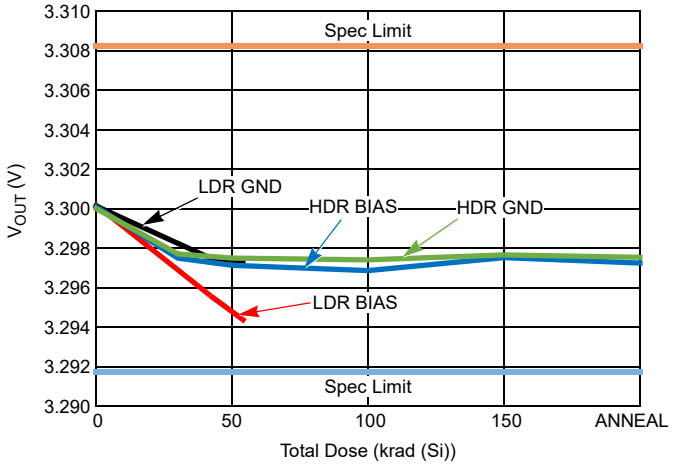


Figure 6. V_{OUT} Accuracy Shift

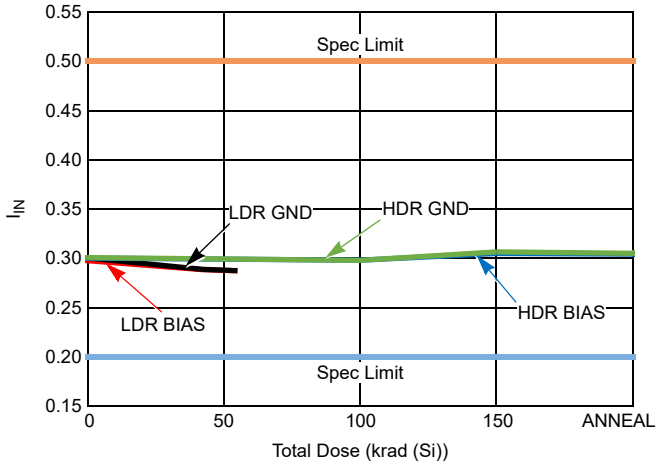


Figure 7. Supply Current Shift

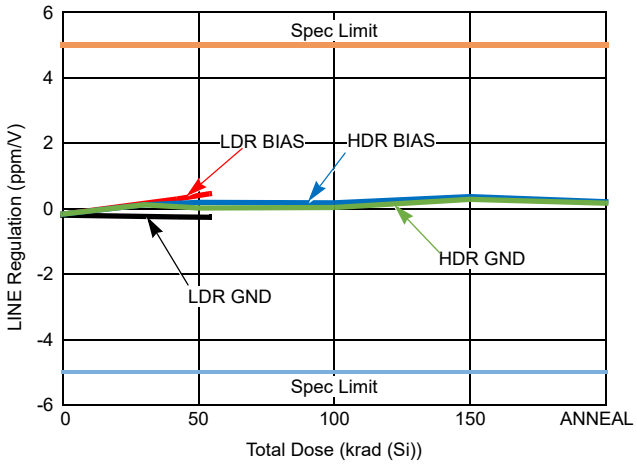


Figure 8. Line Regulation Shift

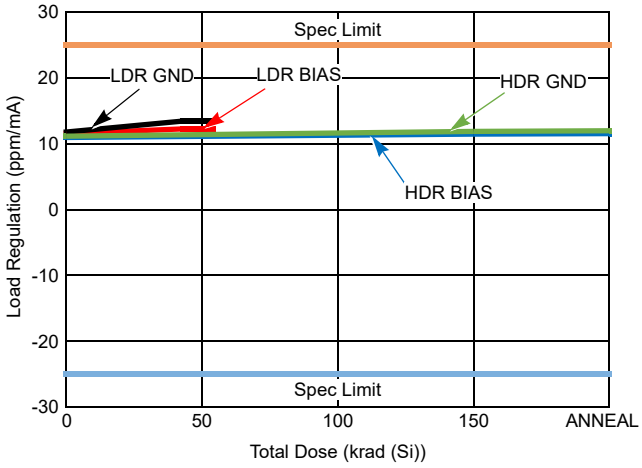


Figure 9. Load Regulation (Sourcing) Shift

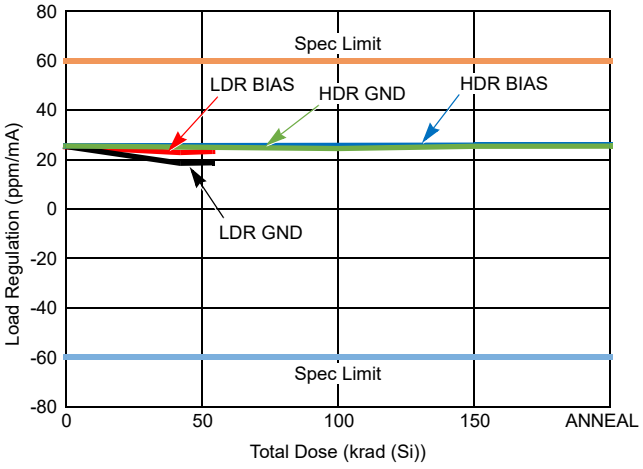


Figure 10. Load Regulation (Sinking) Shift

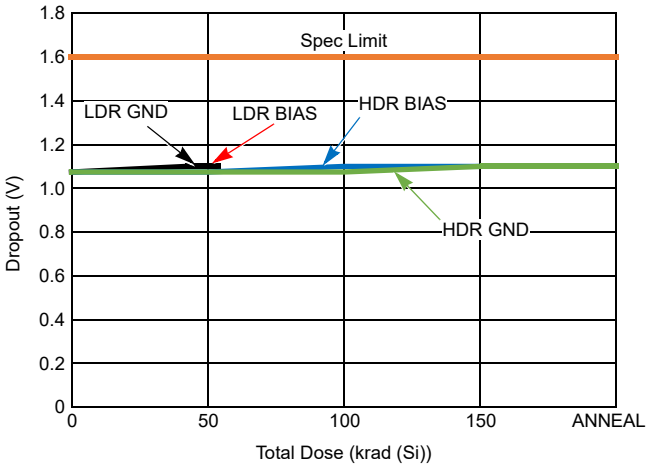


Figure 11. Dropout Shift

5. Typical Performance Curves

V_{IN} = 5V, T_A = +25°C, I_{OUT} = 0, C_{IN} = 0.1µF, C_L = 1µF and C_{COMP} = 0.001µF, unless otherwise specified.

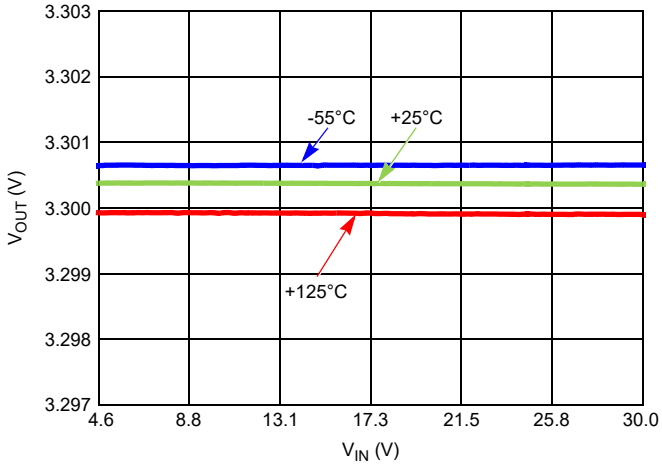


Figure 12. Line Regulation vs V_{OUT} (V) Over Temperature

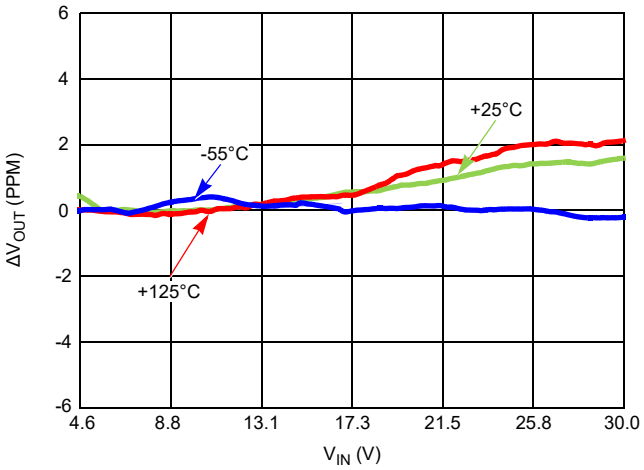


Figure 13. Line Regulation vs ΔV_{OUT} (PPM) Over Temperature

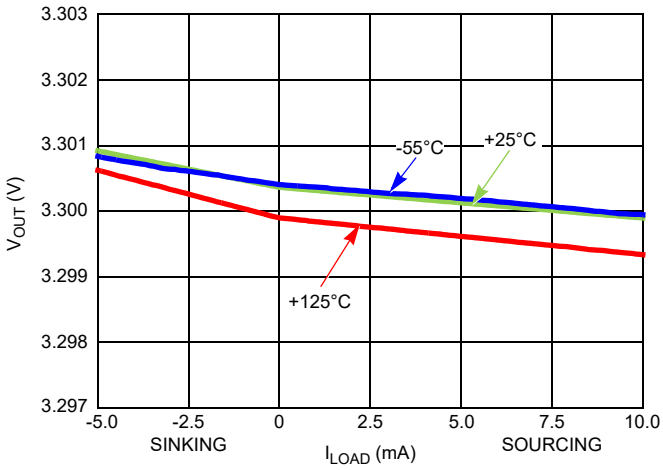


Figure 14. Load Regulation vs V_{OUT} (V) Over Temperature

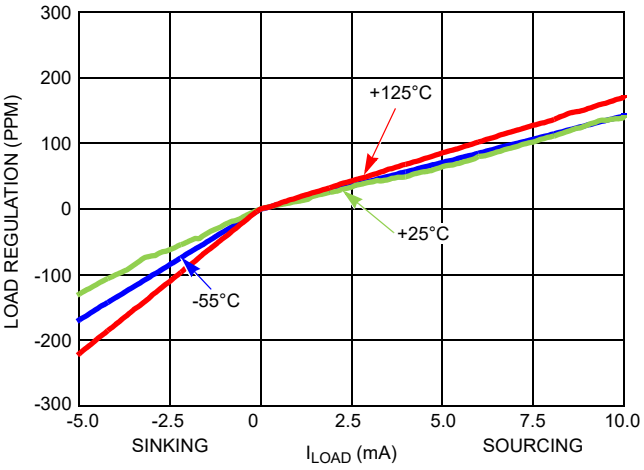


Figure 15. Load Regulation vs V_{OUT} (PPM) Over Temperature

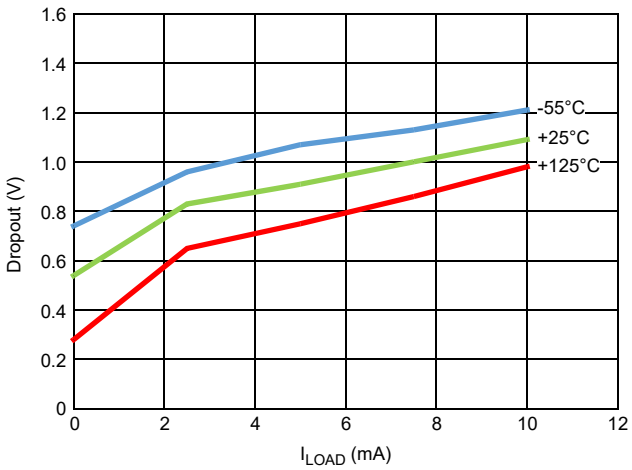


Figure 16. Dropout Voltage vs Output Current

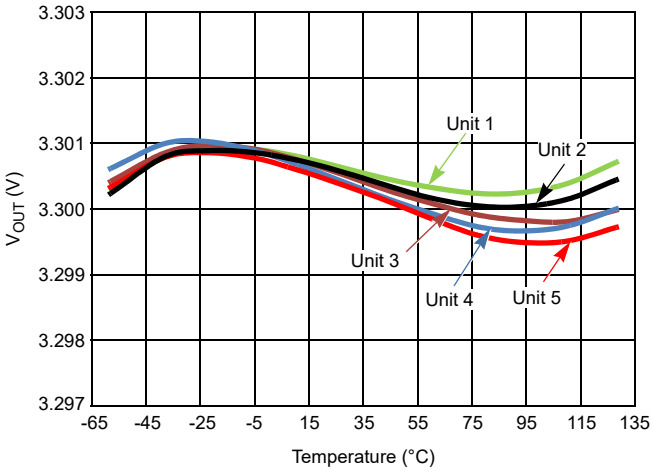


Figure 17. V_{OUT} vs Temperature

V_{IN} = 5V, T_A = +25°C, I_{OUT} = 0, C_{IN} = 0.1µF, C_L = 1µF and C_{COMP} = 0.001µF, unless otherwise specified. (Cont.)

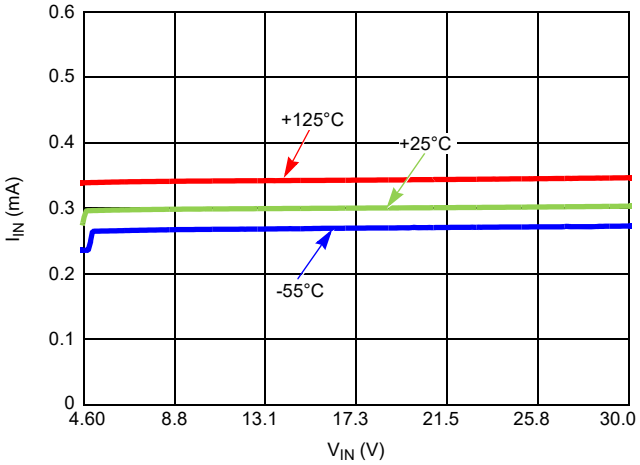


Figure 18. I_{IN} vs V_{IN} Over Temperature

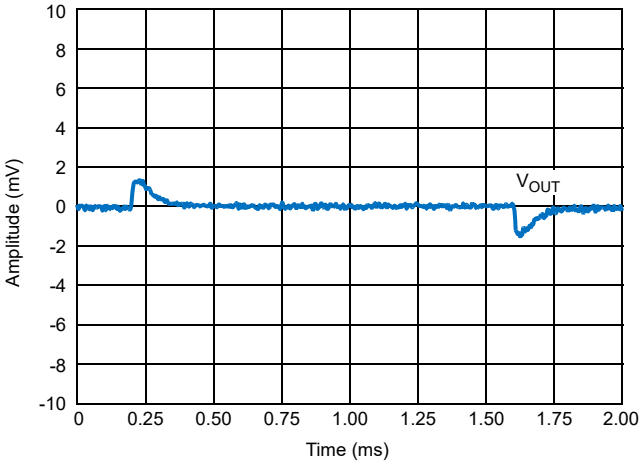


Figure 19. Line Transient (ΔV_{IN} = 500mV)

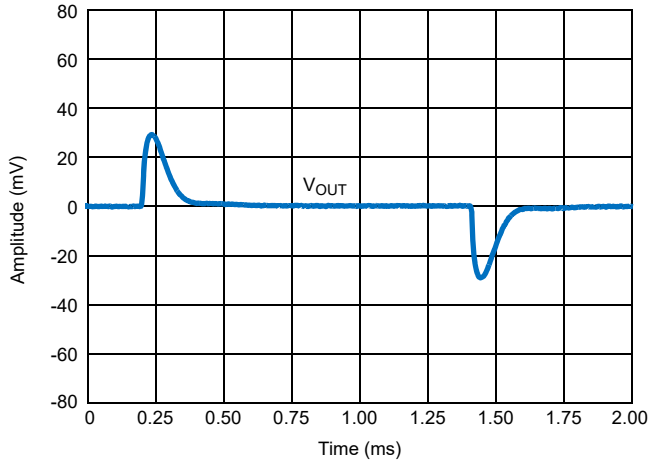


Figure 20. Load Transient (ΔI_L = 1mA)

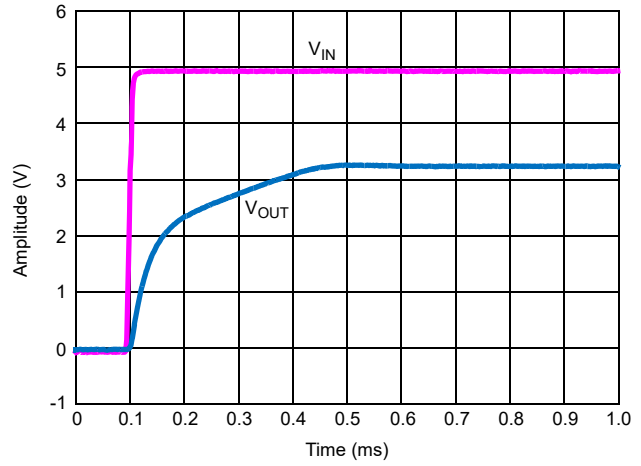


Figure 21. Turn-On Time

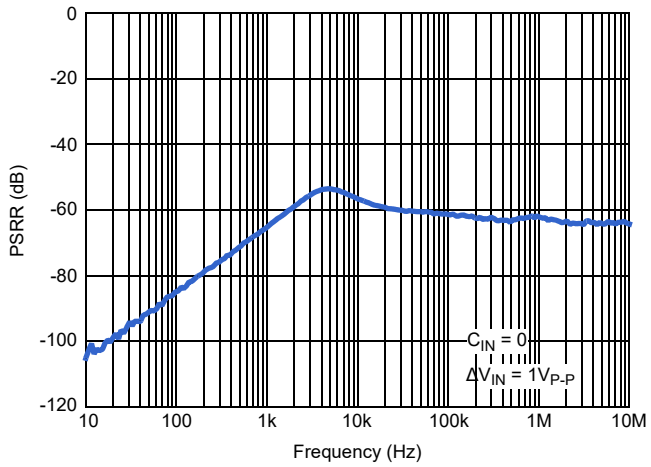


Figure 22. Ripple Rejection vs Frequency

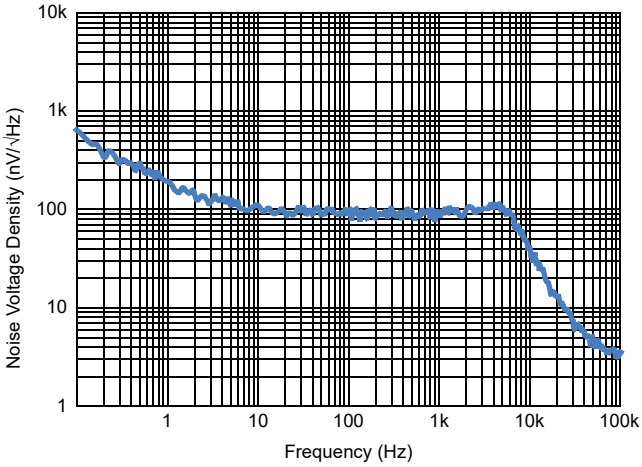


Figure 23. Noise Voltage Density vs Frequency

V_{IN} = 5V, T_A = +25°C, I_{OUT} = 0, C_{IN} = 0.1µF, C_L = 1µF and C_{COMP} = 0.001µF, unless otherwise specified. (Cont.)

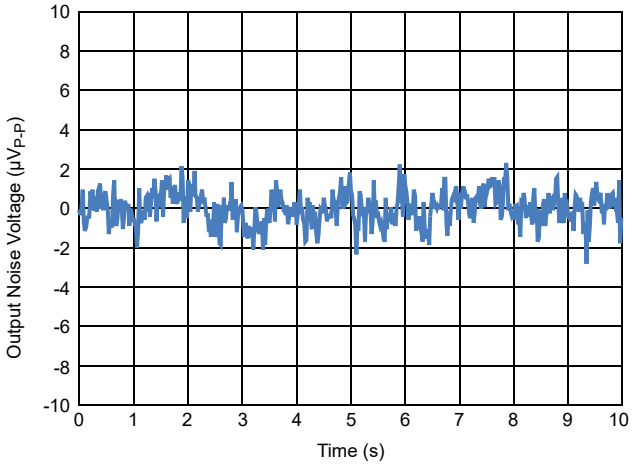


Figure 24. V_{OUT} vs Noise, 0.1Hz to 10Hz

6. Device Operation

6.1 Bandgap Precision References

The ISL71091SEH33 uses a bandgap architecture and special trimming circuitry to produce a temperature compensated, precision voltage reference with high input voltage capability and moderate output current drive.

7. Applications Information

7.1 Board Mounting Considerations

For applications requiring the highest accuracy, board mounting location should be reviewed. The device uses a ceramic flatpack package. Generally, mild stresses to the die when the Printed Circuit (PC) board is heated and cooled, can slightly change the shape. Because of these die stresses, placing the device in areas subject to slight twisting can cause degradation of reference voltage accuracy. It is normally best to place the device near the edge of a board, or on the shortest side, because the axis of bending is most limited in that location. Mounting the device in a cutout also minimizes flex. Obviously, mounting the device on flexprint or extremely thin PC material will likewise cause loss of reference accuracy.

7.2 Board Assembly Considerations

Some PC board assembly precautions are necessary. Normal output voltage shifts of 100µV to 500µV can be expected with Pb-free reflow profiles or wave solder on multilayer FR4 PC boards. Precautions should be taken to avoid excessive heat or extended exposure to high reflow or wave solder temperatures.

7.3 Noise Performance and Reduction

The output noise voltage in a 0.1Hz to 10Hz bandwidth is typically 5.2µV_{P-P} (V_{OUT} = 3.3V). The noise measurement is made with a bandpass filter. The filter is made of a 1-pole high-pass filter, with a corner frequency at 0.1Hz, and a 2-pole low-pass filter, with a corner frequency (3dB) at 9.9Hz, to create a filter with a 9.9Hz bandwidth. Noise in the 10Hz to 1kHz bandwidth is approximately 5.8µV_{RMS} (V_{OUT} = 3.3V), with 0.1µF capacitance on the output. This noise measurement is made with a 2 decade bandpass filter. The filter is made of a 1-pole high-pass filter with a corner frequency at 10Hz of the center frequency, and 1-pole low-pass filter with a corner frequency at 1kHz. Load capacitance up to 10µF can be added but will result in only marginal improvements in output noise and transient response.

7.4 Turn-On Time

Normal turn-on time is typically 250µs, as shown in Figure 21. The circuit designer must take this into account when looking at power-up delays or sequencing.

7.5 Temperature Coefficient

The limits stated for temperature coefficient (Tempco) are governed by the method of measurement. The overwhelming standard for specifying the temperature drift of a reference is to measure the reference voltage at two temperatures, take the total variation, ($V_{HIGH} – V_{LOW}$), and divide by the temperature extremes of measurement ($T_{HIGH} – T_{LOW}$). The result is divided by the nominal reference voltage (at T = +25°C) and multiplied by 10^6 to yield ppm/°C. This is the “Box” method for specifying temperature coefficient.

7.6 Output Voltage Adjustment

The output voltage can be adjusted above and below the factory-calibrated value via the trim terminal. The trim terminal is the negative feedback divider point of the output op amp. The voltage at the trim pin is set at approximately 1.216V by the internal bandgap and amplifier circuitry of the voltage reference.

The suggested method to adjust the output is to connect a very high value external resistor directly to the trim terminal and connect the other end to the wiper of a potentiometer that has a much lower total resistance and whose outer terminals connect to V_{OUT} and ground. It is important to minimize the capacitance on the trim terminal to preserve output amplifier stability. It is also best to connect the series resistor directly to the trim terminal, to minimize that capacitance and also to minimize noise injection. Small trim adjustments, such as ±0.25%, will not disturb the factory-set temperature coefficient of the reference, but trimming by large amounts can.

7.7 Output Stage

The output stage of the device has a push-pull configuration with a high-side PNP and a low-side NPN. This helps the device to act as a source and sink. The device can source 10mA and sink 5mA.

7.8 Use of COMP Capacitor

The reference can be compensated for the C_{OUT} capacitors used by adding a capacitor from the COMP pin to GND. See Table 1 for recommended values of the COMP capacitor.

Table 1. Recommended Values of COMP Capacitor

C_{OUT} (µF)	C_{COMP} (nF)
0.1	1
1	1
10	10

Data from SEE testing suggests the best option to use is 1µF for C_{OUT} and 1nF for C_{COMP}. Refer to the *ISL71091SEHxx SEE Test Repor*t for more details.

7.9 DNC Pins

These pins are for trimming purposes and for factory use only. Do not connect these to the circuit in any way. It will adversely effect the performance of the reference.

7.10 Simulation Model

A SPICE simulation model is available on the ISL71091SEH33 page. Figure 25 through Figure 30 show a comparison of the characterized part performance and the simulated part performance.

7.10.1 Characterization vs Simulation Results

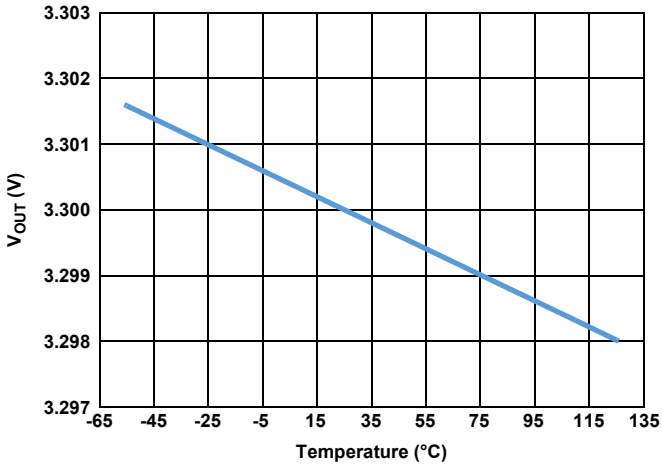


Figure 25. Simulated (Worse Case) V_{OUT} vs Temperature

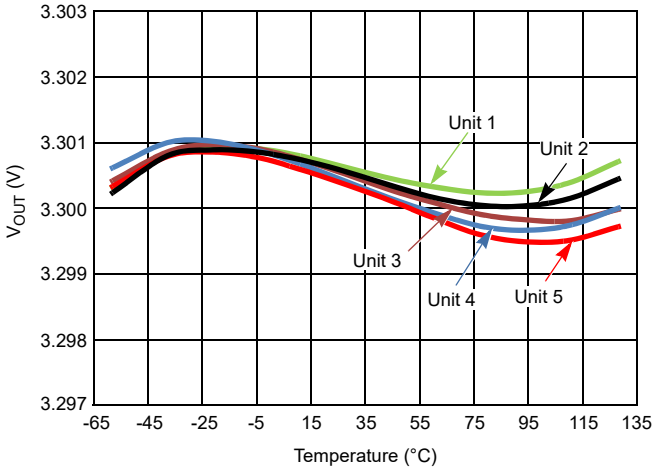


Figure 26. Characterized V_{OUT} vs Temperature

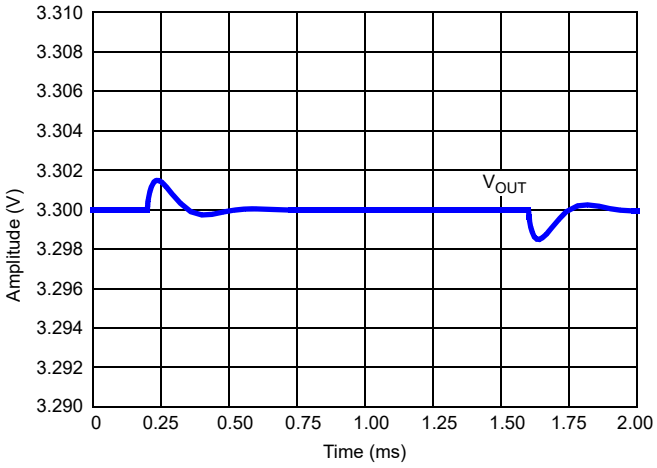


Figure 27. Simulated Line Transient (ΔV_{IN} = 500mV)

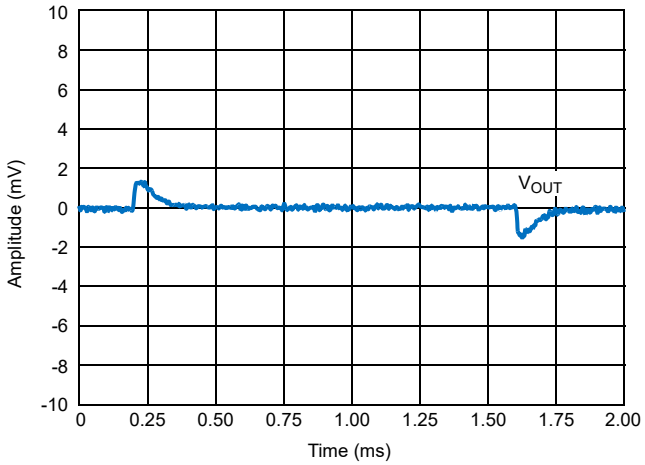


Figure 28. Characterized Line Transient (ΔV_{IN} = 500mV)

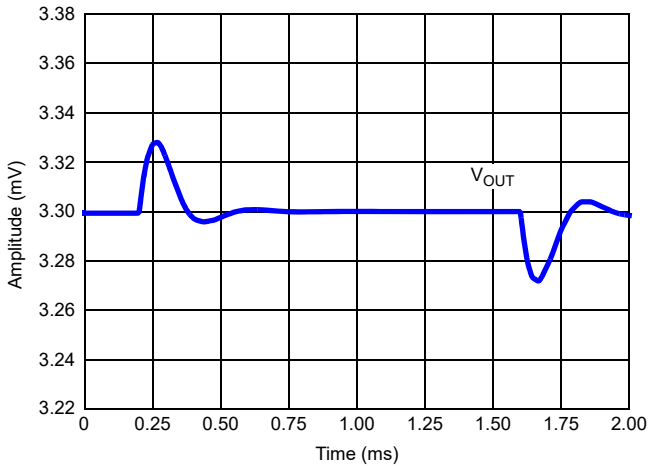


Figure 29. Simulated Load Transient (ΔI_L = 1mA)

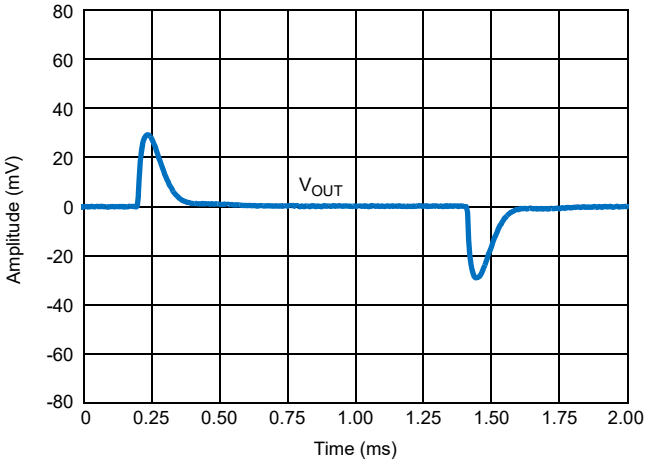


Figure 30. Characterized Load Transient (ΔI_L = 1mA)

8. Package and Die Characteristics

Table 2. Die and Assembly Related Information

Die Information	
Dimensions	1990µm x 2380µm (78 mils x 94 mils) Thickness: 483µm ±25µm (19 mils ±1 mil)
Interface Materials	
Glassivation	Type: Nitrox Thickness: 15kÅ
Top Metallization	Type: AlCu (99.5%/0.5%) Thickness: 30kÅ
Backside Finish	Silicon
Process	Dielectrically Isolated Advanced Bipolar Technology- PR40
Assembly Information	
Substrate Potential	Floating
Additional Information	
Worst Case Current Density	$<2 \times 10^5 A/cm^2$
Transistor Count	182
Weight of Packaged Device	0.31 grams (Typical)
Lid Characteristics	Finish: Gold Potential: Connected to Pin #4 (GND) Case Isolation to Any Lead: $20 \times 10^9 \Omega$ (min)

8.1 Metallization Mask Layout

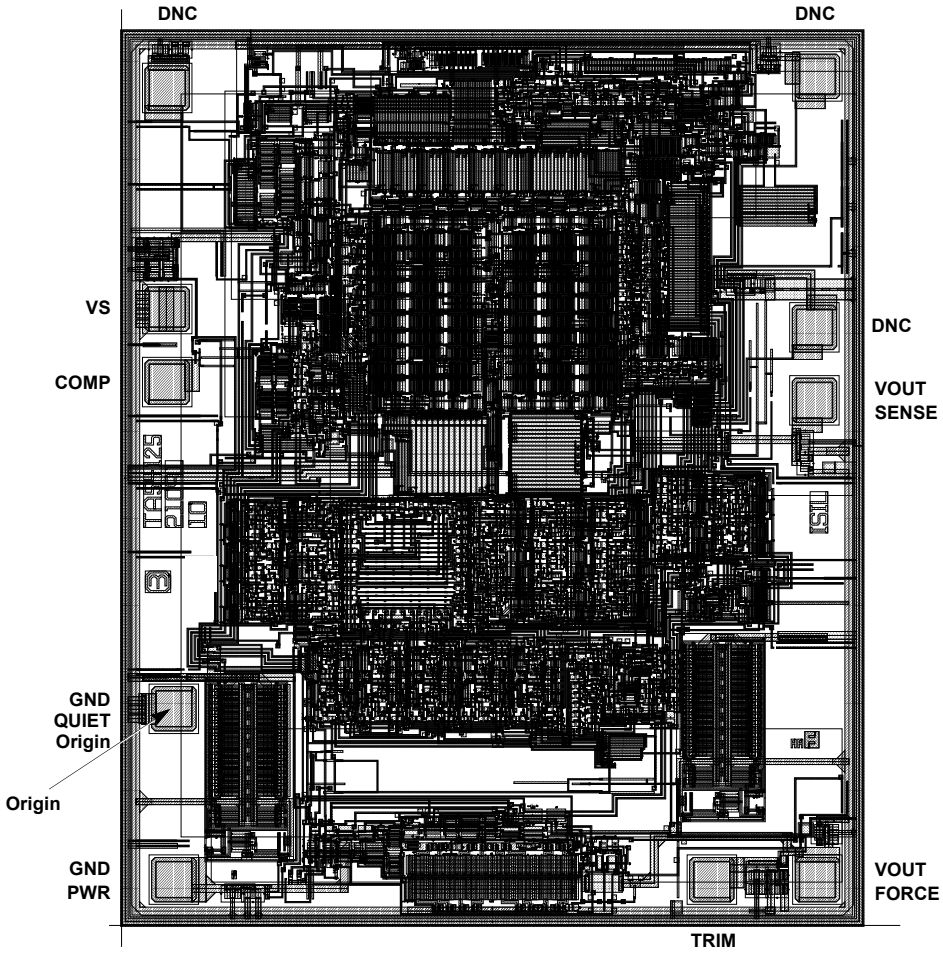


Table 3. Die Layout X-Y Coordinates

Pad Name	Pad Number	X (µm)	Y (µm)	Bond Wires Per Pad[1]
GND PWR	1	1	-436	1
GND QUIET[2]	2	0	0	1
COMP	3	-15	831	1
VS	4	-17	1018	1
DNC	5			
DNC	6			
DNC	7			
VOUT SENSE	8	1633	786	1
VOUT FORCE	9	1640	-436	1
TRIM	10	1505	-436	1

1. Bond wire size is 1 mil.
2. Origin of coordinates is the centroid of GND QUIET.

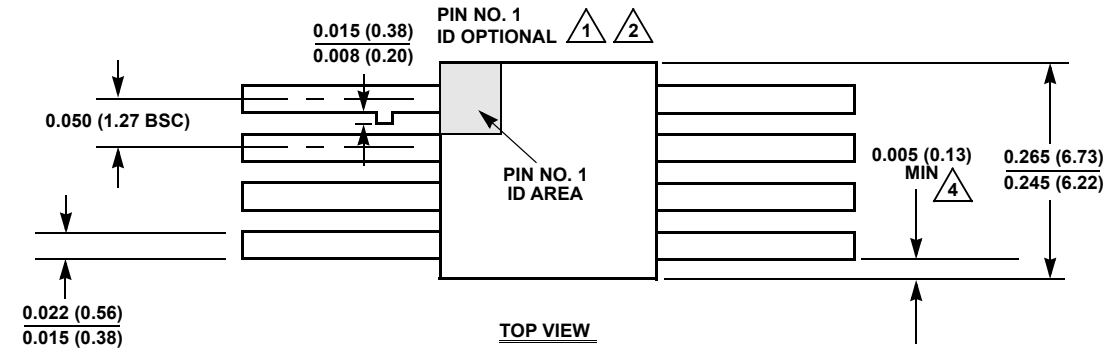
9. Package Outline Drawing

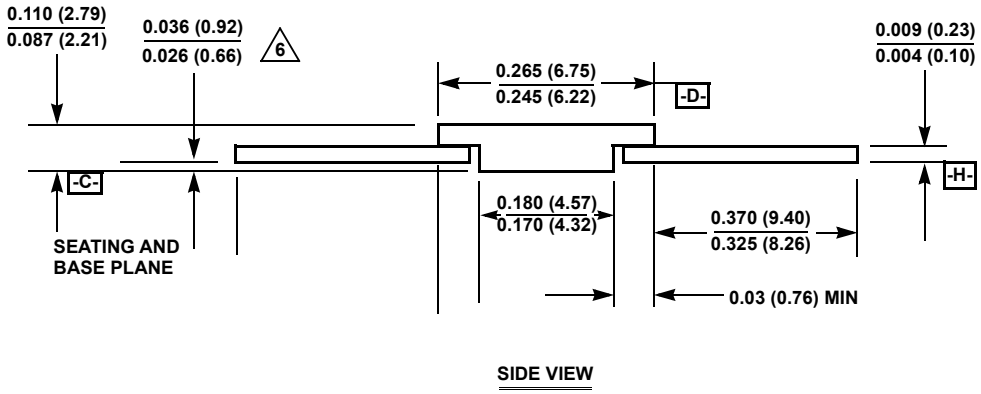
For the most recent package outline drawing, see K8.A.

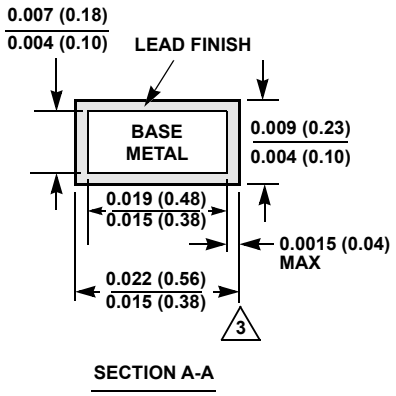
K8.A

8 Lead Ceramic Metal Seal Flatpack Package

Rev 4, 12/14







NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab may be used to identify pin one.
2. If a pin one identification mark is used in addition to or instead of a tab, the limits of the tab dimension do not apply.
3. The maximum limits of lead dimensions (section A-A) shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
4. Measure dimension at all four corners.
5. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
6. Dimension shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
7. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
8. Controlling dimension: INCH.

10. Ordering Information

SMD Ordering Number[1]	Part Number[2]	Package Description (RoHS Compliant)	Pkg. Dwg. #	Carrier Type	Radiation Hardness (Total Ionizing Dose)	V_{OUT} Option[3] (V)	Temp Range
5962R1420802VXC	ISL71091SEHVF33	8 Ld Flatpack	K8.A	Tray	HDR to 100krad(Si), LDR to 50krad(Si)	3.30	-55 to +125°C
5962R1420802V9A	ISL71091SEHVX33[4]	Die	-	-			
N/A	ISL71091SEHF33/PROTO[5]	8 Ld Flatpack	K8.A	Tray	N/A		
	ISL71091SEHX33SAMPLE[4][5]	Die	-	-			
	ISL71091SEH33EV1Z[6]	Evaluation Board					

1. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed must be used when ordering.
2. These Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
3. For alternate V_{OUT} options, visit the Rad Hard Voltage References page.
4. Die product tested at T_A = + 25°C. The wafer probe test includes functional and parametric testing sufficient to make the die capable of meeting the electrical performance outlined in Electrical Specifications.
5. The /PROTO and /SAMPLE are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions across temperature specified in the DLA SMD and are in the same form and fit as the qualified device. The /SAMPLE parts are capable of meeting the electrical limits and conditions specified in the DLA SMD. The /SAMPLE parts do not receive 100% screening across temperature to the DLA SMD electrical limits. These part types do not come with a Certificate of Conformance because they are not DLA qualified devices.
6. Evaluation board uses the /PROTO parts and /PROTO parts are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity.

Table 4. Key Differences Between Family of Parts

Part Number	V_{OUT} (V)	Grade (%)	TEMPCO (ppm/°C)	Output Voltage Noise (μV_{P-P})	Load Regulation (ppm/mA)
ISL71091SEH20	2.048	0.05	6	3.8	40
ISL71091SEH33	3.3	0.05	6	5.2	25
ISL71091SEH40	4.096	0.05	6	6.2	20
ISL71091SEH10	10	0.05	6	14.8	15

11. Revision History

Revision	Date	Description
2.01	Oct 5, 2023	Applied new template formatting throughout. Updated Radiation Acceptance Tested feature bullets. Removed Related Literature and About Intersil sections. Updated ordering information table and added Notes 4, 5, 6.
2.0	Mar 18, 2016	-Updated Related Literature document titles to match titles on the actual documents. -Added Table 1 on page 2. -On page 5: -Added testing information to ESD ratings in Abs Max table. -Changed Electrical Specification for Flatpack note from: “Boldface limits apply over the operating temperature range, -55°C to +125°C and radiation.” to: “Boldface limits apply after radiation at +25°C or across the operating temperature range, -55°C to +125°C without radiation, unless otherwise specified. -For parameters V_{OA} (rows 2, 3, 4) in Electrical Specifications for Flatpack table in the Test Conditions column updated note cross reference”. -On page 6: -Changed Electrical Specification for Die note from: “Boldface limits apply over the operating temperature range, -55°C to +125°C and radiation.” To: “Boldface limits apply after radiation at +25°C and across the operating temperature range, -55°C to +125°C without radiation, unless otherwise specified. -For parameter V_{OA} Post Radiation (row 4) in Electrical Specifications for Die table changed description from: “V_{OUT} Accuracy at T_A = -55°C to +125°C, Post Radiation”, to: “V_{OUT} Accuracy at T_A = +25°C, Post Radiation”. -Updated POD K8.A to the latest revision. Changes to POD are as follows: -Modified Note 2 by adding the words “...in addition to or instead of...”.
1.0	Jul 11, 2014	Page 1 - changed title from: “Radiation Hardened Ultra Low Noise, Precision Voltage Reference” to: “3.3V Radiation Hardened Ultra Low Noise, Precision Voltage Reference”
0.0	May 21, 2014	Initial Release.

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