ISL71148SLH

Radiation Hardened 8-Channel 14-Bit 900/480ksps SAR ADC

Description

The ISL71148SLH is a radiation hardened 8-channel high precision 14-bit, 900/480ksps SAR Analog-to-Digital Converter (ADC). The ADC core is preceded by eight fully differential analog input channels, a buffered 8-to-1 multiplexer, and a PGA (Programmable Gain Amplifier). The device features a peak SNR of 83.2dBFS when operating at 900ksps. With the PGA enabled, sampling rates up to 480ksps are supported. The PGA can be bypassed to increase the sample rate to 900ksps.

The product features 900/480ksps throughput with no data latency, excellent linearity, and dynamic accuracy. The ISL71148SLH offers a high-speed SPI-compatible serial interface that supports logic ranging from 2.2V to 3.6V using a separate digital I/O supply pin.

The ISL71148SLH offers a separate low-power mode (LPM) pin that reduces power dissipation at lower sample rates. An external reference with a supported input range of 2.4V to 2.6V determines the analog input signal range.

The ISL71148SLH is available in a 48-lead Thin Quad Flat-Pack (TQFP) space plastic.

Applications

- Precision signal processing
- Propulsion, payload systems
- High-end industrial
- Engine control
- Down-hole drilling

Features

- Qualified to Renesas rad hard QML-P Equivalent Screening and QCI Flow (R34TB0005EU)
  - All screening and QCI is in accordance with MIL-PRF-38535L Class-P
- 8 Buffered Differential Analog Input Channels with Multiplexer
- Bypassable PGA with selectable gain ($1 \le G \le 16$)
- Fully Differential Bipolar Operation
- Channel Scan Sequencer
- Full throughput rate with no data latency
- Excellent linearity: ±0.2 LSB DNL, ±0.4 LSB INL
- Low noise: 83.2dBFS (PGA bypassed), 77dBFS SNR (PGA Gain = 2)
- 5V AV_{CC} supply and 2.5V/3.3V DV_{CC} supply
- Analog input impedance: >1GΩ, <5pF
- Wide 50MHz -3dB input bandwidth
- Low power mode operation at lower sample rates
- High speed SPI-compatible serial I/O
- Full military temperature range operation T_A = -55°C to +125°C
- TID Rad Hard Assurance (RHA) testing
  - LDR (≤10mrad(Si)/s): 75krad(Si)
- SEE Characterization
  - No DSEE for AV_{CC} = 6.2V, DV_{CC} = 4.6V, and V_{REF} = 3.6V at 86MeV•cm^2/mg
  - SEFI <3.1µm^2 at 86MeV•cm^2/mg

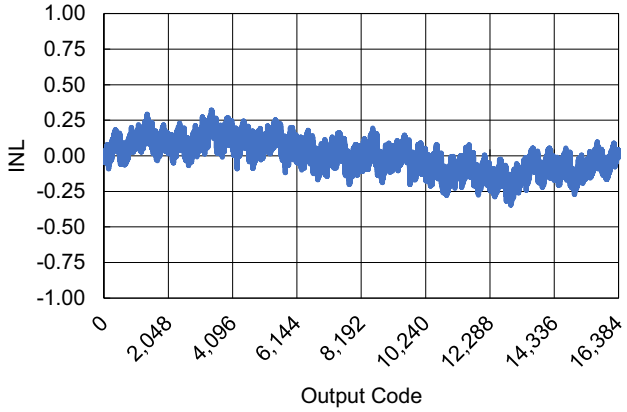


Figure 1. INL vs Output Code

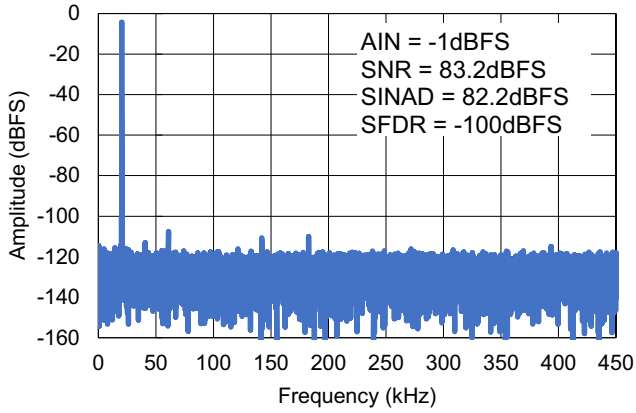


Figure 2. FFT - 20.3kHz

Contents

1. Overview

1.1 Typical Application Schematic

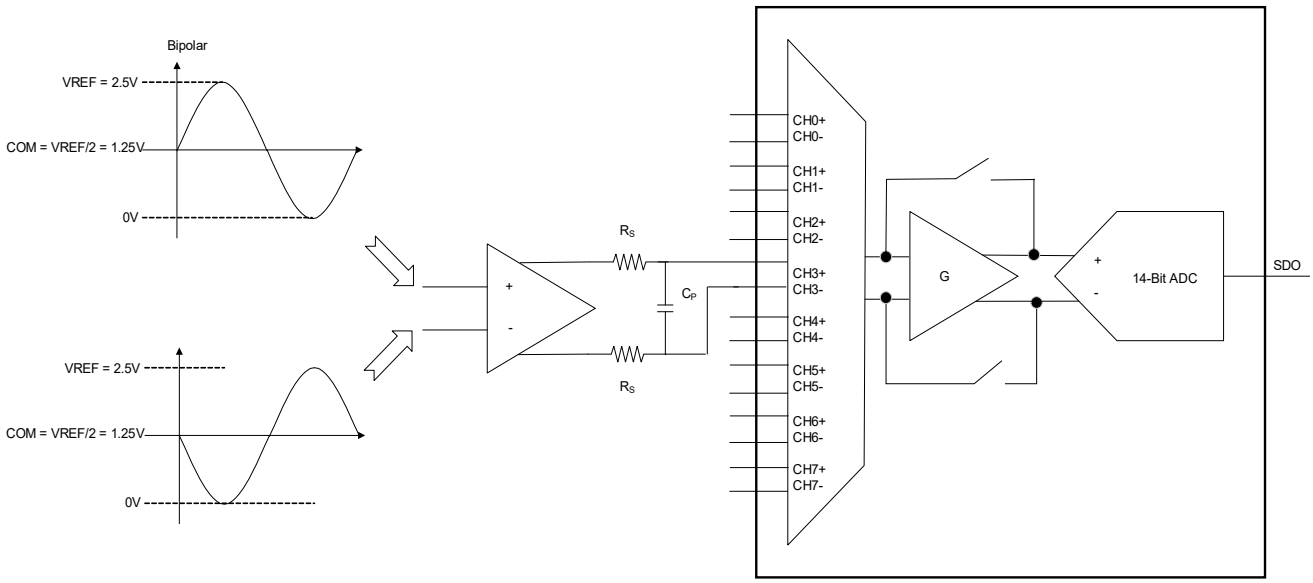


Figure 3. Typical Application Example Circuit

1.2 Functional Block Diagram

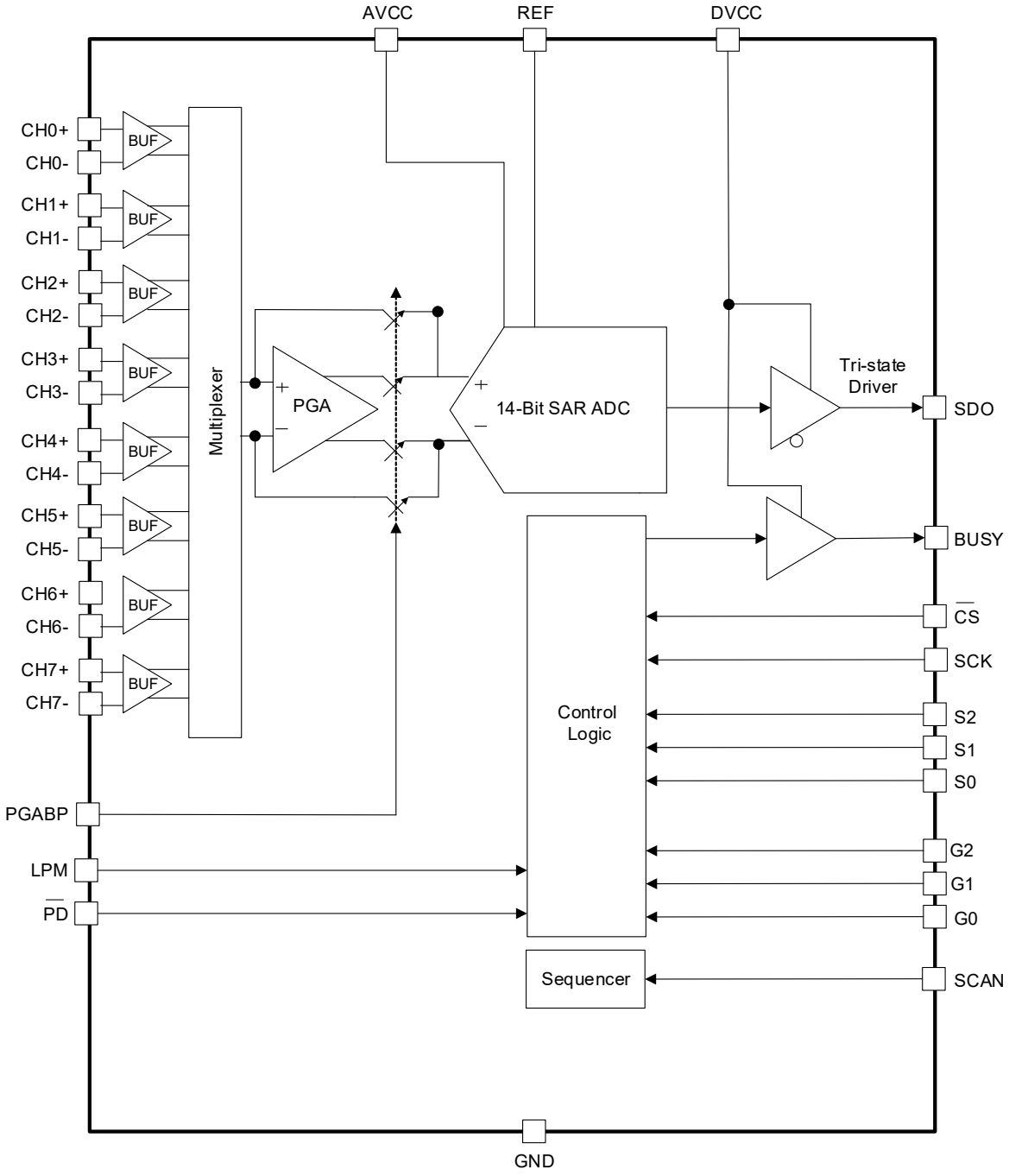


Figure 4. Block Diagram

2. Pin Information

2.1 Pin Assignments

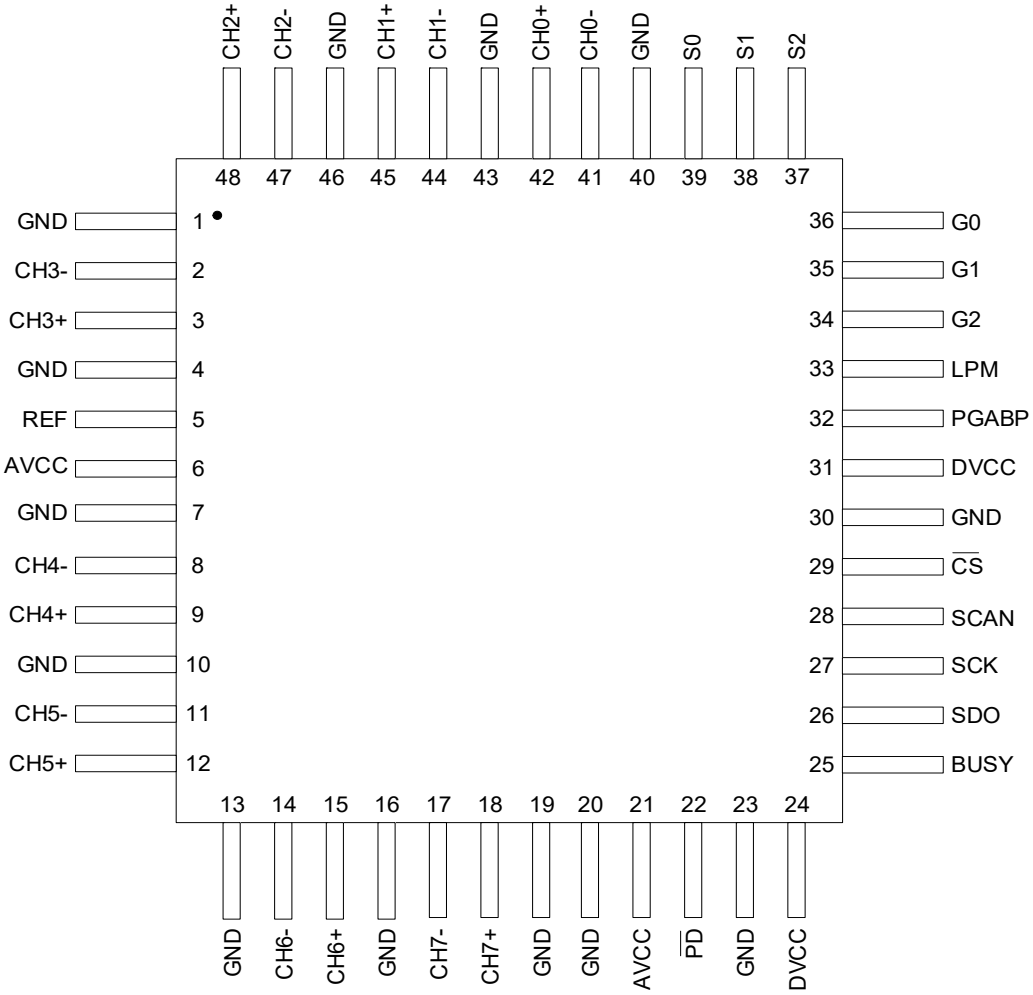


Figure 5. Pin Assignments - Top View

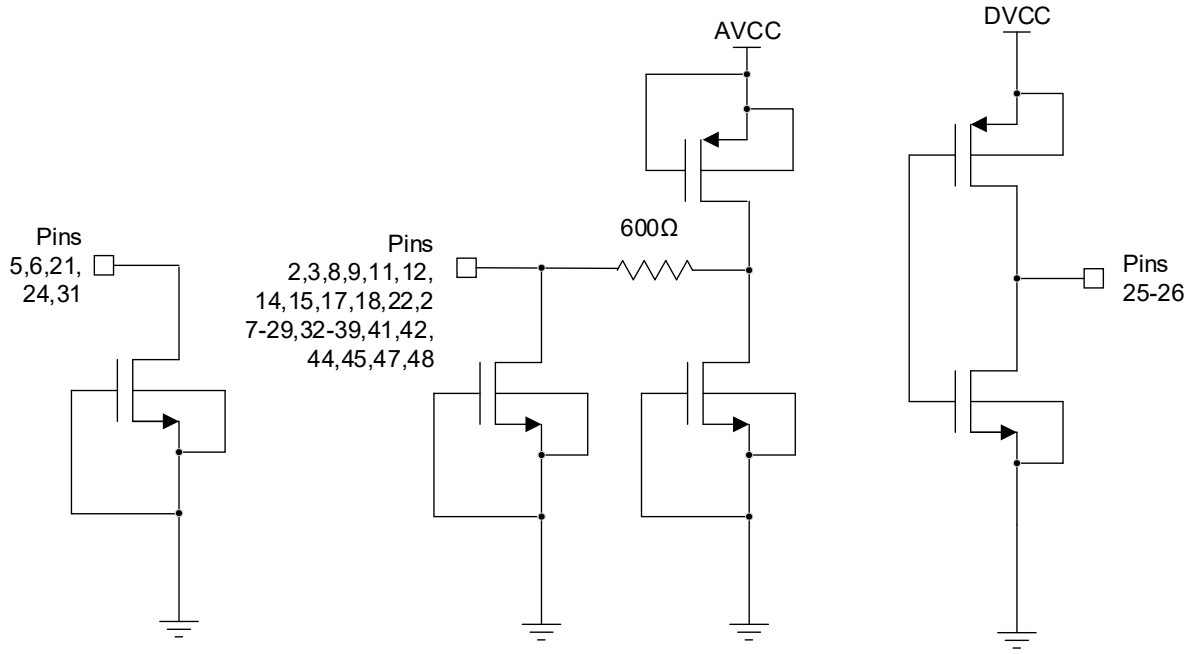
2.2 Pin Descriptions

Pin Number	Pin Name	ESD Circuit	Description
1, 4, 7, 10, 13, 16, 19, 20, 23, 30, 40, 43, 46	GND	-	Analog and digital supply ground. Tie directly to the PCB ground plane (GND).
6,21	AVCC	1	Analog supply. The supply range is 4.5V to 5.5V. Bypass this pin to GND with a 10µF ceramic capacitor.
5	REF	1	Reference Input. The input range of REF is 2.4V to 2.6V. The voltage at the REF pin (V_{REF}) defines the input range of each Analog Input Channel as 0V to V_{REF}. Bypass REF to GND with a 10µF ceramic capacitor.

Pin Number	Pin Name	ESD Circuit	Description
2	CH3-	2	Analog Input Channel Pairs. CH0± to CH7± are eight fully differential input channel pairs. Each Analog Input Channel pin can be driven within the voltage range from 0V to V_{REF}.
3	CH3+		
8	CH4-		
9	CH4+		
11	CH5-		
12	CH5+		
14	CH6-		
15	CH6+		
17	CH7-		
18	CH7+		
41	CH0-		
42	CH0+		
44	CH1-		
45	CH1+		
47	CH2-		
48	CH2+		
22	$\overline{PD}$	2	Power-Down Low Input. When this input is logic low, the chip is powered down. If this occurs during a conversion, the conversion is halted, and the SDO pin is placed in Hi-Z. DV_{CC} determines logic levels. This pin has an internal 500kOhm pull-up resistor to DVCC.
24, 31	DVCC	1	Digital I/O supply. The voltage range on this pin is 2.2V to 3.6V. DV_{CC} is nominally set to the same supply voltage as the host interface (2.5V or 3.3V). Bypass DVCC to GND with a 0.1µF capacitor.
25	BUSY	3	Busy output. A logic high indicates a conversion is in progress. The BUSY indicator returns low following the completion of a conversion. DV_{CC} determines logic levels.
26	SDO	3	Serial data output. The current conversion result is serially shifted on this pin on the rising edges of SCK, from MSB first to LSB last. The data stream comprises 14 bits of conversion data followed by the channel select and gain select bits corresponding to the conversion result. DV_{CC} determines logic levels.
27	SCK	2	Serial data clock input. When $\overline{CS}$ is low, and the BUSY indicator is low, the conversion result is shifted out on SDO on the rising edges of SCK, with the Most Significant Bit (MSB) first to the Least Significant Bit (LSB) last. D_{VCC} determines logic levels. SCK should be held low when it is not being asserted.
28	SCAN	2	Channel scan input. When this input is logic-high, the internal sequencer controls the channel selected. CH0 is the first channel selected following the rising edge of SCAN. Each subsequent channel is selected on each new rising edge of $\overline{CS}$. DV_{CC} determines logic levels.
29	$\overline{CS}$	2	Convert Start Low input. A falling edge on this input completes the sampling process and starts a new conversion. The conversion is timed using an internal oscillator. The device automatically powers down following the conversion process. The logic state of the $\overline{CS}$ pin controls the state of the SDO pin. A logic high on the $\overline{CS}$ pin disables the SDO pin driver, and the SDO pin impedance is Hi-Z. A logic low on the $\overline{CS}$ pin enables the SDO driver (unless $\overline{PD}$ is low) and allows data to be read out following a conversion. Hold this pin low at power-up and when in power-down or when the device is inactive.
32	PGABP	2	PGA bypass mode input. When this input is logic high, the PGA is bypassed, and the input buffer/multiplexer directly drives the ADC. The maximum throughput rate is increased to 900ksps. DV_{CC} determines logic levels.
33	LPM	2	Low power mode input. When this input is logic high, the acquisition time is directly controlled by the $\overline{CS}$ pin logic state held high. The ADC is automatically powered down between conversions to reduce power consumption for lower sample rates. This pin is a device configuration pin and should not be switched dynamically during operation.

Pin Number	Pin Name	ESD Circuit	Description
34	G2	2	Logic Inputs. These three pins program the gain of the PGA. The G2, G1, and G0 logic inputs are latched internally on the rising edge of $\overline{CS}$. DV_{CC} determines logic levels.
35	G1		
36	G0		
37	S2	2	Channel selection logic inputs. These three pins select the input channel passed through the input multiplexer to the PGA (or ADC if the PGA is bypassed). The S2, S1, and S0 logic inputs are latched internally on the rising edge of $\overline{CS}$. DV_{CC} determines logic levels.
38	S1		
39	S0		

Equivalent Input Circuits



Circuit 1 Circuit 2 Circuit 3

3. Specifications

3.1 Absolute Maximum Ratings

***Caution**:* Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Min	Max	Unit
Supply Voltage (AVCC to GND)	-0.3	6.5	V
Supply Voltage (AVCC to GND)[1]	-0.3	6.2	V
Supply Voltage (DVCC to GND)	-0.3	4.6	V
Supply Voltage (DVCC to GND)[1]	-0.3	4.6	V
Reference Input Voltage (REF to GND)	-0.3	3.6	V
Reference Input Voltage (REF to GND)[1]	-0.3	3.6	V
(CH0:7+, CH0:7- to GND) Voltage	-0.3	(A_{VCC} + 0.3)	V
Digital Input Voltage ($\overline{PD}$, $\overline{CS}$, SCK, S2, S1, S0, G2, G1, G0, SCAN, LPM, PGABP)	-0.3	(DV_{CC} + 0.3)	V
CH0:7+, CH0:7- Input Current[2]	-3	3	mA
Maximum Junction Temperature	-	+150	°C
Storage Temperature Range	-65	+150	°C
Human Body Model (Tested per MIL-STD-883 TM3015.7)	-	2.5	kV
Charged Device Model (Tested per JS-002-2022)	-	750	V

1. Tested in a heavy ion (Au) environment at LET = 86Mev•cm^2/mg at 125°C.
2. When an input voltage transient exceeds maximum operating conditions (voltage at the ±channel input pins less than GND or greater than AVCC), limit the input current to less than ±3mA.

3.2 Recommended Operating Conditions

Parameter	Min	Max	Unit
Temperature	-55	+125	°C
Analog Supply Voltage, A_{VCC}	4.5	5.5	V
Digital Supply Voltage, D_{VCC}	2.2	3.6	V
Reference Input Voltage, V_{REF}	2.4	2.6	V
Analog Input Differential Voltage, A_{IN}	0	V_{REF}	V

3.3 Outgas Testing

Specification (Tested per ASTM E595, 1.5)	Value	Unit
Total Mass Loss[1]	0.04	%
Collected Volatile Condensible Material[1]	0.01	%
Water Vapor Recovered	0.03	%

1. Outgassing results meet NASA requirements of total mass loss <1% and collected volatile condensible material <0.1%.

3.4 Thermal Information

Parameter	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance	48 LD TQFP	θ_{JA}[1]	Junction to ambient	48	°C/W
		θ_{JC}[2]	Junction to case	11	°C/W

1. θ_{JA} is measured in free air with the component on high-effective thermal conductivity test board. See TB379.
2. For θ_{JC}, the case temperature location is the center of package top.

3.5 Electrical Specifications

3.5.1 Normal Operating Mode

AV_{CC} = 5.0V; DV_{CC} = 2.5V, REF = 2.5V, GND = 0V, PGA Bypassed, LPM = 0V, f_{SAMP} = 900.901ksps, F_{IN} = 20.3kHz, A_{IN} = -1dBFS; T_A = 25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C by production testing; over a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s .**

Parameter	Symbol	Test Conditions	Min	Typ[1]	Max	Unit
Converter Characteristics						
Resolution	-	-	**14**	-	-	bits
No Missing Codes	-	-	**14**	-	-	bits
Transition Noise	-	RMS noise, 14-bit LSB	-	0.29	-	LSB_{RMS}
Zero-Scale Error	ZSE	Measured with input set to V_{REF}/2.	**-4**	±0.1	**4**	LSB
Zero-Scale Error Drift	ZSED	Measured with input set to V_{REF}/2.	-	±0.001	-	LSB/°C
Zero-Scale Error Match	ZSEM	Measured with input set to V_{REF}/2.	**-4**	±0.5	**4**	LSB
Positive Full-Scale Error	+FSE	Measured with input connected to V_{REF}	**-7**	±0.1	**7**	LSB
Positive Full-Scale Error Drift	+FSED	Measured with input connected to V_{REF}	-	±0.003	-	LSB/°C
Positive Full-Scale Error Match	+FSEM	Measured with input connected to V_{REF}	**-4**	±1	**4**	LSB
Negative Full-Scale Error	-FSE	Measured with input connected to GND	**-7**	±1	**7**	LSB
Negative Full-Scale Error Drift	-FSED	Measured with input connected to GND	-	±0.014	-	LSB/°C
Negative Full-Scale Error Match	-FSEM	Measured with input connected to GND	**-4**	±1	**4**	LSB
Integral Non-Linearity[2]	INL	Measured with full-scale input signal.	**-1**	±0.4	**1**	LSB
Differential Non-Linearity[2]	DNL	Measured with full-scale input signal.	**-0.5**	±0.2	**0.5**	LSB
Dynamic Accuracy						
Signal-to-Noise Ratio	SNR	PGA Bypassed	**82**	83.2	-	dBFS
		PGA Gain = 2, f_{SAMP} = 483.092ksps	**76**	77	-	
		PGA Gain = 16, f_{SAMP} = 483.092ksps, A_{IN} = -3dBFS	**59.5**	62	-	
Signal-to-Noise + Distortion Ratio	SINAD	PGA Bypassed	**81**	82.2	-	dBFS
		PGA Gain = 2, f_{SAMP} = 483.092ksps	**75**	76	-	
		PGA Gain = 16, f_{SAMP} = 483.092ksps, A_{IN} = -3dBFS	**58.5**	61	-	
Effective Number of Bits	ENOB	PGA Bypassed	**13.1**	13.5	-	bits
		PGA Gain = 2, f_{SAMP} = 483.092ksps	**12.1**	12.5	-	
		PGA Gain = 16, f_{SAMP} = 483.092ksps, A_{IN} = -3dBFS	**9.4**	9.8	-	

AV_{CC} = 5.0V; DV_{CC} = 2.5V, REF = 2.5V, GND = 0V, PGA Bypassed, LPM = 0V, f_{SAMP} = 900.901ksps, F_{IN} = 20.3kHz, A_{IN} = -1dBFS; T_A = 25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C by production testing; over a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s . (Cont.)**

Parameter	Symbol	Test Conditions	Min	Typ[1]	Max	Unit
Total Harmonic Distortion	THD	PGA Bypassed	**85**	95	-	dBFS
		PGA Gain = 2, f_{SAMP} = 483.092ksps	**85**	95	-	
		PGA Gain = 16, f_{SAMP} = 483.092ksps, A_{IN} = -3dBFS	**80**	85	-	
Spurious Free Dynamic Range	SFDR	PGA Bypassed	**90**	100	-	dBFS
		PGA Gain = 2, f_{SAMP} = 483.092ksps	**90**	100	-	
		PGA Gain = 16, f_{SAMP} = 483.092ksps, A_{IN} = -3dBFS	-	90	-	
Channel-to-Channel Isolation	-	Full-scale signal applied to one channel, other channels connected to GND	-	-100	-	dB
Input Bandwidth	-	Source impedance = 50Ω, -3dB point	-	50	-	MHz
Aperture Delay	t_{AD}	$\overline{CS}$ falling edge to sample edge	-	2.5	-	ns
Aperture Jitter	$t_{AJITTER}$	-	-	500	-	fs_{RMS}
Power Supply Characteristics (AVCC, DVCC)						
Analog Supply Voltage	AV_{CC}	-	**4.5**	-	**5.5**	V
Analog Supply Current - Active	I_{AVCC}	Active, PGA enabled, f_{SAMP} = 483.092ksps	-	17.6	**20.5**	mA
		Active, PGA bypassed, f_{SAMP} = 900.901ksps	-	20	**23**	mA
Analog Supply Current - Static	I_{Static}	PGA enabled. $\overline{CS}$ held Low	-	10.5	**13**	mA
		PGA bypassed. $\overline{CS}$ held Low	-	6	**9**	mA
Analog Supply Current - Sleep	I_{SLAVCC}	$\overline{PD}$ held Low	-	20	-	µA
Digital Supply Voltage	DV_{CC}	-	**2.2**	-	**3.6**	V
Digital Supply Current - Active	I_{DVCC}	PGA enabled. f_{SCK} = 50MHz	-	346	**600**	µA
		PGA bypassed. f_{SCK} = 50MHz	-	512	**700**	µA
Digital Supply Current - Static	I_{STDVCC}	PGA enabled. $\overline{CS}$ held Low.	-	100	**120**	µA
		PGA bypassed. $\overline{CS}$ held Low.	-	70	**90**	µA
Digital Supply Current - Sleep	I_{SLDVCC}	$\overline{PD}$ held Low	-	6	-	µA
P_D	P_{ACTIVE}	PGA enabled, f_{SAMP} = 483.092ksps	-	89	**104**	mW
	P_{ACTIVE}	PGA bypassed, f_{SAMP} = 900.091ksps	-	101	**117**	mW
	P_{STATIC}	PGA enabled, $\overline{CS}$ held Low	-	53	**70**	mW
	P_{STATIC}	PGA bypassed, $\overline{CS}$ held Low.	-	30	**50**	mW
	P_{SLEEP}	$\overline{PD}$ held Low	-	115	-	µW

1. Typical values are not guaranteed.
2. Characterized on all channels, production tested on Channel 0 only.

3.5.2 Low Power Mode

AV_{CC} = 5.0V; DV_{CC} = 2.5V, REF = 2.5V, GND = 0V, PGA Bypassed, LPM = 2.5V, f_{SAMP} = 684.932ksps, F_{IN} = 20.3kHz, A_{IN} = -1dBFS; T_A = 25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C by production testing; over a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s.**

Parameter	Symbol	Test Conditions	Min	Typ[1]	Max	Unit
Converter Characteristics						
Resolution	-	-	**14**	-	-	bits

AV_{CC} = 5.0V; DV_{CC} = 2.5V, REF = 2.5V, GND = 0V, PGA Bypassed, LPM = 2.5V, f_{SAMP} = 684.932ksps, F_{IN} = 20.3kHz, A_{IN} = -1dBFS; T_A = 25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C by production testing; over a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s. (Cont.)**

Parameter	Symbol	Test Conditions	Min	Typ[1]	Max	Unit
No Missing Codes	-	-	**14**	-	-	bits
Transition Noise	-	RMS noise, 14-bit LSB	-	0.29	-	LSB_{RMS}
Zero-Scale Error	ZSE	Measured with input set to V_{REF}/2.	**-4**	±0.1	**4**	LSB
Zero-Scale Error Drift	ZSED	Measured with input set to V_{REF}/2.	-	±0.001	-	LSB/°C
Zero-Scale Error Match	ZSEM	Measured with input set to V_{REF}/2.	**-4**	±0.5	**4**	LSB
Positive Full-Scale Error	+FSE	Measured with input connected to V_{REF}	**-7**	±0.1	**7**	LSB
Positive Full-Scale Error Drift	+FSED	Measured with input connected to V_{REF}	-	±0.003	-	LSB/°C
Positive Full-Scale Error Match	+FSEM	Measured with input connected to V_{REF}	**-4**	±1	**4**	LSB
Negative Full-Scale Error	-FSE	Measured with input connected to GND	**-7**	±1	**7**	LSB
Negative Full-Scale Error Drift	-FSED	Measured with input connected to GND	-	±0.014	-	LSB/°C
Negative Full-Scale Error Match	-FSEM	Measured with input connected to GND	**-4**	±1	**4**	LSB
Integral Non-Linearity[2]	INL	Measured with full scale input signal.	**-1**	±0.4	**1**	LSB
Differential Non-Linearity[2]	DNL	Measured with full scale input signal.	**-0.5**	±0.2	**0.5**	LSB
Dynamic Accuracy						
Signal-to-Noise Ratio	SNR	PGA Bypassed	**82**	83.2	-	dBFS
		PGA Gain = 2, f_{SAMP} = 413.223ksps	**76**	77	-	
		PGA Gain = 16, f_{SAMP} = 413.223ksps, A_{IN} = -3dBFS	**59.5**	62	-	
Signal-to-Noise + Distortion Ratio	SINAD	PGA Bypassed	**81**	82.2	-	dBFS
		PGA Gain = 2, f_{SAMP} = 413.223ksps	**75**	76	-	
		PGA Gain = 16, f_{SAMP} = 413.223ksps, A_{IN} = -3dBFS	**58.5**	61	-	
Effective Number of Bits	ENOB	PGA Bypassed	**13.1**	13.5	-	bits
		PGA Gain = 2, f_{SAMP} = 413.223ksps	**12.1**	12.5	-	
		PGA Gain = 16, f_{SAMP} = 413.223ksps, A_{IN} = -3dBFS	**9.4**	9.8	-	
Total Harmonic Distortion	THD	PGA Bypassed	**85**	95	-	dBFS
		PGA Gain = 2, f_{SAMP} = 413.223ksps	**85**	95	-	
		PGA Gain = 16, f_{SAMP} = 413.223ksps, A_{IN} = -3dBFS	**80**	85	-	
Spurious Free Dynamic Range	SFDR	PGA Bypassed	**90**	100	-	dBFS
		PGA Gain = 2, f_{SAMP} = 413.223ksps	**90**	100	-	
		PGA Gain = 16, f_{SAMP} = 413.223ksps, A_{IN} = -3dBFS	-	90	-	
Channel-to-Channel Isolation	-	Full-scale signal applied to one channel, other channels connected to GND	-	-100	-	dB
Input Bandwidth	-	Source impedance = 50Ω, -3dB point	-	50	-	MHz
Aperture Delay	t_{AD}	$\overline{CS}$ falling edge to sample edge	-	2.5	-	ns
Aperture Jitter	$t_{AJITTER}$	-	-	500	-	fs_{RMS}

AV_{CC} = 5.0V; DV_{CC} = 2.5V, REF = 2.5V, GND = 0V, PGA Bypassed, LPM = 2.5V, f_{SAMP} = 684.932ksps, F_{IN} = 20.3kHz, A_{IN} = -1dBFS; T_A = 25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C by production testing; over a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s. (Cont.)**

Parameter	Symbol	Test Conditions	Min	Typ[1]	Max	Unit
Power Supply Characteristics (AVCC, DVCC)						
Analog Supply Voltage	AV_{CC}	-	**4.5**	-	**5.5**	V
Analog Supply Current - Active	I_{AVCC}	Active, PGA enabled, f_{SAMP} = 413.223ksps	-	13.9	**16.9**	mA
		Active, PGA bypassed, f_{SAMP} = 670ksps	-	15.8	**17.5**	mA
Analog Supply Current - Static	I_{Static}	PGA enabled. $\overline{CS}$ held Low	-	6	**7.5**	mA
		PGA bypassed. $\overline{CS}$ held Low.	-	6	**7.5**	mA
Analog Supply Current - Sleep	I_{SLAVCC}	$\overline{PD}$ held Low	-	20	-	µA
Digital Supply Voltage	DV_{CC}	-	**2.2**	-	**3.6**	V
Digital Supply Current - Active	I_{DVCC}	PGA enabled. f_{SCK} = 50MHz	-	346	**600**	µA
		PGA bypassed. f_{SCK} = 50MHz	-	512	**700**	µA
Digital Supply Current - Static	I_{STDVCC}	PGA enabled. $\overline{CS}$ held Low	-	92	**140**	µA
		PGA bypassed. $\overline{CS}$ held Low	-	64	**120**	µA
Digital Supply Current - Sleep	I_{SLDVCC}	$\overline{PD}$ held Low	-	6	-	µA
P_D	P_{ACTIVE}	PGA enabled, f_{SAMP} = 413.223ksps	-	70	**86**	mW
	P_{ACTIVE}	PGA bypassed, f_{SAMP} = 684.932ksps	-	80	**89**	mW
	P_{STATIC}	PGA enabled, $\overline{CS}$ held Low	-	30	**40**	mW
	P_{STATIC}	PGA bypassed, $\overline{CS}$ held Low	-	30	**40**	mW
	P_{SLEEP}	$\overline{PD}$ held Low	-	115	-	µW

1. Typical values are not guaranteed.
2. Characterized on all channels, production tested on Channel 0 only.

3.5.3 Channel Input Specifications

AV_{CC} = 5.0V; DV_{CC} = 2.5V, REF = 2.5V, GND = 0V, T_A = 25°C, F_{IN} = 20.3kHz, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C by production testing; over a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s.**

Parameter	Symbol	Test Conditions	Min	Typ[1]	Max	Unit
Channel Input Characteristics (CH0 to CH7)						
Absolute Input Range (CH0+ to CH7+ to GND, CH0- to CH7- to GND)	-	Recommended Operating Condition	**-0.1**	-	**V_{REF} + 0.1**	V
Input Differential Range (CHn+ - CHn-)	-	-	**$-V_{REF}$/GAIN**	-	**V_{REF}/GAIN**	V
Common Mode Input Range ½×(CHn+ + CHn-)	-	-	**V_{REF}/2 - 0.1**	V_{REF}/2	**V_{REF}/2 + 0.1**	V
Input Common Mode Rejection Ratio	-	-	-	90	-	dB
Input Leakage Current	IA_{IN}	-	**-1**		**1**	µA
Input Capacitance	C_{IN}	-	-	4	-	pF
Input Resistance	R_{IN}	-	-	1	-	GΩ

AV_{CC} = 5.0V; DV_{CC} = 2.5V, REF = 2.5V, GND = 0V, T_A = 25°C, F_{IN} = 20.3kHz, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C by production testing; over a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s. (Cont.)**

Parameter	Symbol	Test Conditions	Min	Typ[1]	Max	Unit
PGA Gain Accuracy	-	Gain = 1, G2:G0 = 000	**-0.45**	-0.2	**0.15**	%
		Gain = 2, G2:G0 = 001	**-0.45**	-0.2	**0.15**	%
		Gain = 3, G2:G0 = 010	**-0.45**	-0.2	**0.15**	%
		Gain = 4, G2:G0 = 011	**-0.45**	-0.2	**0.15**	%
		Gain = 6, G2:G0 = 100	**-0.8**	-0.3	**0.35**	%
		Gain = 8, G2:G0 = 101	**-0.8**	-0.4	**0.35**	%
		Gain = 12, G2:G0 = 110	**-1**	-0.5	**0.2**	%
		Gain = 16, G2:G0 = 111	**-1**	-0.7	**0.2**	%

1. Typical values are not guaranteed.

3.5.4 I/O Specifications

AV_{CC} = 5.0V; DV_{CC} = 2.5V, REF = 2.5V, GND = 0V, T_A = 25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C by production testing; over a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s.**

Parameter	Symbol	Test Conditions	Min	Typ[1]	Max	Unit
Digital Inputs and Outputs ($\overline{PD}$, $\overline{CS}$, SCK, BUSY, SDO, LPM, PGABP, S2, S1, S0, G2, G1, G0, SCAN)						
High Level Input	V_{IH}	-	**0.8×DV_{CC}**	-	-	V
Low Level Input	V_{IL}	-	-	-	**0.2×DV_{CC}**	V
Input Current ($\overline{CS}$, SCK, PGABP, S2, S1, S0, G2, G1, G0, SCAN)	I_{IN}	V_{IN} = 0V to DV_{CC}	**-1**	-	**1**	µA
Input Capacitance	C_{IN}	-	-	5	-	pF
High Level Output	V_{OH}	DV_{CC} - Output, I_O = -500µA	**DV_{CC} - 0.2**	-	-	V
Low Level Output	V_{OL}	I_O = 500µA	-	-	**0.2**	V
Output Source Current	I_{SRC}	V_{OUT} = 0V to DV_{CC}	-	-10	-	mA
Output Sink Current	I_{SNK}	V_{OUT} = 0V to DV_{CC}	-	10	-	mA
Hi-Z Output Leakage Current	I_{OZ}	V_{OUT} = 0V to DV_{CC}	**-1**		**1**	µA
$\overline{PD}$ Input Resistance	R_{INPDL}	Internal pull-up resistance to D_{VCC}	**375**	475	**600**	kΩ
LPM Input Resistance	R_{INLPM}	Internal pull-down resistance to GND	**375**	475	**600**	kΩ
Reference Input Characteristics (REF)						
REF Input Voltage Range	V_{REF}	-	**2.4**	2.5	**2.6**	V
REF Input Current	I_{REF}	-	-	150	**200**	µA

1. Typical values are not guaranteed.

3.5.5 Operation Burn-In Deltas

AV_{CC} = 5.0V; DV_{CC} = 2.5V, REF = 2.5V, GND = 0V, PGA Bypassed, LPM = 0V (Normal Mode) and LPM = DV_{CC} (Low Power Mode), f_{SAMP} = 900.901ksps (Normal Mode) and 684.932ksps (Low Power Mode), F_{IN} = 20.3kHz, A_{IN} = -1dBFS, T_A = +25°C, S2, S1, and S0 = 0V (Channel 0 selected); unless otherwise noted.

Parameter	Symbol	Test Conditions	Min	Max	Unit
Integral Non-Linearity	INL	Measured with full scale input signal	-0.5	0.5	LSB
Signal to Noise Ratio	SNR	F_{IN} = 20.3kHz	-1	1	dBFS
Effective Number of Bits	ENOB	F_{IN} = 20.3kHz	-0.2	0.2	bits

3.6 Timing Specifications

3.6.1 Normal Operating Mode

AV_{CC} = 4.5V to 5.5V; DV_{CC} = 2.2V to 3.6V, REF = 2.5V, GND = 0V, PGA Bypassed, LPM = 0V, f_{SAMP} = 900.901ksps, A_{IN} = -1dBFS; T_A = 25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C by production testing; over a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s.**

Parameter	Symbol	Test Conditions	Min	Typ[1]	Max	Unit
Maximum Sampling Frequency	f_{SAMP}	PGA Bypassed	-	-	**900.901**	kHz
		PGA Enabled	-	-	**483.092**	kHz
Conversion Time	t_{CONV}	BUSY Output High Time, PGA Bypassed	-	-	**660**	ns
		BUSY Output High Time, PGA Enabled	-	-	**1550**	ns
$\overline{CS}$ High Time	t_{CSH}	-	**150**	-	-	ns
SCK Held Low to $\overline{CS}\downarrow$	t_{QUIET}	-	**150**	-	-	ns
$\overline{CS}\downarrow$ to BUSY↑	t_{BUSYLH}	PGA enabled, C_L = 10pF	-	-	**100**	ns
$\overline{CS}\downarrow$ to BUSY↑	t_{BUSYLH}	PGA bypassed, C_L = 10pF	-	-	**30**	ns
SCK Period	t_{SCK}	-	**20**	-	-	ns
SCK High Time	t_{SCKH}	-	**8**	-	-	ns
SCK Low Time	t_{SCKL}	-	**8**	-	-	ns
SDO Data Valid Delay from BUSY↓	$t_{DBUSYLSDOV}$	C_L = 10pF	-	-	**0**	ns
SDO Data Valid Delay from SCK↑	$t_{DSCKSDOV}$	C_L = 10pF	-	-	**20**	ns
SDO Data Valid Hold Time from SCK↑	t_{HSDOV}	C_L = 10pF	**7**	-	-	ns
SDO Bus Acquisition Time from $\overline{CS}\downarrow$	$t_{DCSLSDOL}$	C_L = 10pF	-	-	**25**	ns
SDO Bus Relinquish Time after $\overline{CS}\uparrow$	$t_{DCSHSDOZ}$	C_L = 10pF	-	-	**25**	ns
G2:0, S2:0 to $\overline{CS}\uparrow$	$t_{SUDIGCSH}$	Setup time for gain and channel select bits.	**5**	-	-	ns
G2:0, S2:0 from $\overline{CS}\uparrow$	$t_{HDIGCSH}$	Hold time for gain and channel select bits.	**25**	-	-	ns
SCAN to $\overline{CS}\uparrow$	$t_{SCANCSH}$	Setup time for SCAN input.	**20**	-	-	ns
Wake-Up time from Power-Down Mode	t_{WAKE}	Time to wait after $\overline{PD}\uparrow$ to first sample	-	15	**25**	µs

1. Typical values are not guaranteed.

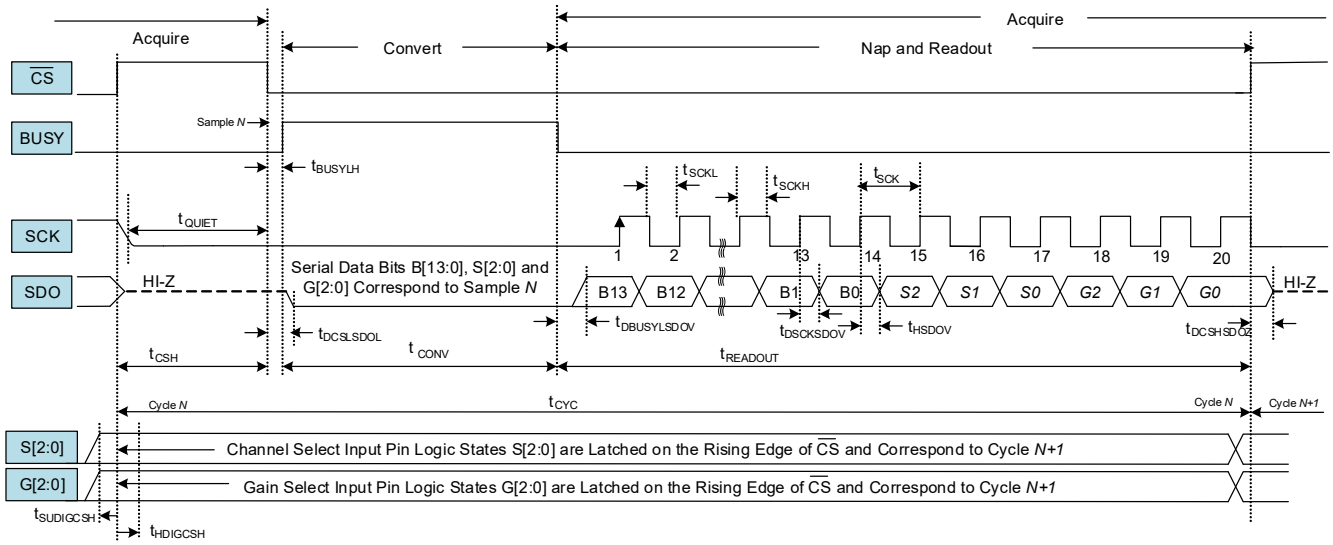
3.6.2 Low Power Mode

AV_{CC} = 4.5V to 5.5V; DV_{CC} = 2.2V to 3.6V, REF = 2.5V, GND = 0V, PGA Bypassed, LPM =2.5V, f_{SAMP} = 684.932ksps, A_{IN} = -1dBFS; T_A = 25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C by production testing; over a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s.**

Parameter	Symbol	Test Conditions	Min	Typ[1]	Max	Unit
Maximum Sampling Frequency	f_{SAMP}	PGA Bypassed	-	-	**684.932**	kHz
		PGA Enabled	-	-	**413.223**	kHz
Conversion Time	t_{CONV}	BUSY Output High Time, PGA Bypassed	-	-	**660**	ns
		BUSY Output High Time, PGA Enabled	-	-	**1550**	ns
$\overline{CS}$ High Time	t_{CSH}	-	**500**	-	-	ns
SCK Held Low to $\overline{CS}\downarrow$	t_{QUIET}	-	**500**	-	-	ns
$\overline{CS}\downarrow$ to BUSY↑	t_{BUSYLH}	C_L = 10pF, PGA enabled.	-	-	**100**	ns
		C_L = 10pF, PGA bypassed.	-	-	**30**	ns
SCK Period	t_{SCK}	-	**20**	-	-	ns
SCK High Time	t_{SCKH}	-	**8**	-	-	ns
SCK Low Time	t_{SCKL}	-	**8**	-	-	ns
SDO Data Valid Delay from BUSY↓	$t_{DBUSYLSDOV}$	C_L = 10pF	-	-	**0**	ns
SDO Data Valid Delay from SCK↑	$t_{DSCKSDOV}$	C_L = 10pF	-	-	**20**	ns
SDO Data Valid Hold Time from SCK↑	t_{HSDOV}	C_L = 10pF	**7**	-	-	ns
SDO Bus Acquisition Time from $\overline{CS}\downarrow$	$t_{DCSLSDOL}$	C_L = 10pF	-	-	**25**	ns
SDO Bus Relinquish Time after $\overline{CS}\uparrow$	$t_{DCSHSDOZ}$	C_L = 10pF	-	-	**25**	ns
G2:0, S2:0 to $\overline{CS}\uparrow$	$t_{SUDIGCSH}$	Setup time for gain and channel select bits.	**15**	-	-	ns
G2:0, S2:0 from $\overline{CS}\uparrow$	$t_{HDIGCSH}$	Hold time for gain and channel select bits.	**10**	-	-	ns
SCAN to $\overline{CS}\uparrow$	t_{SCAN}	Setup time for SCAN input.	**20**	-	-	ns
Wake-Up time from Power-Down Mode[2]	t_{WAKE}	Time to wait after $\overline{PD}\uparrow$ to first sample	-	15	**25**	µs

1. Typical values are not guaranteed.
2. Production tested in normal mode.

3.7 Timing Diagrams



Note: Bits S2, S1, S0, G2, G1, and G0 are optional and not required. For maximum sample rate, do not provide additional clocks for these bits.

Figure 6. Operational Timing Diagram - Normal Operation

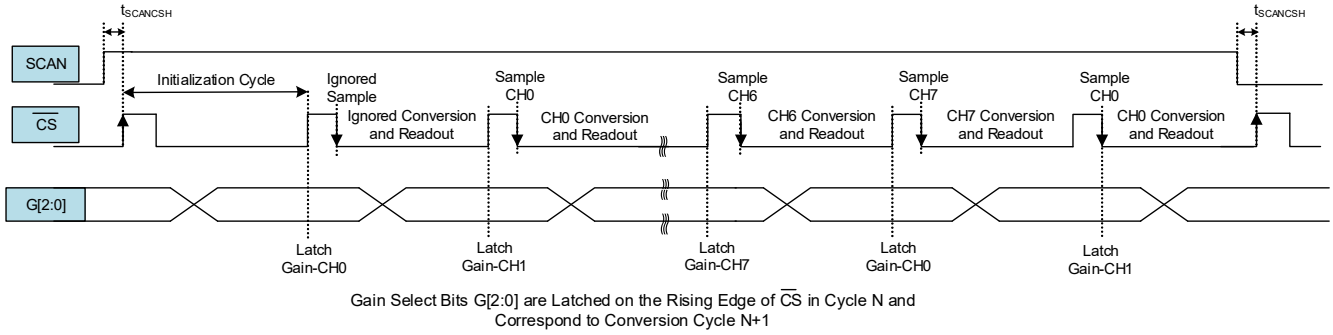
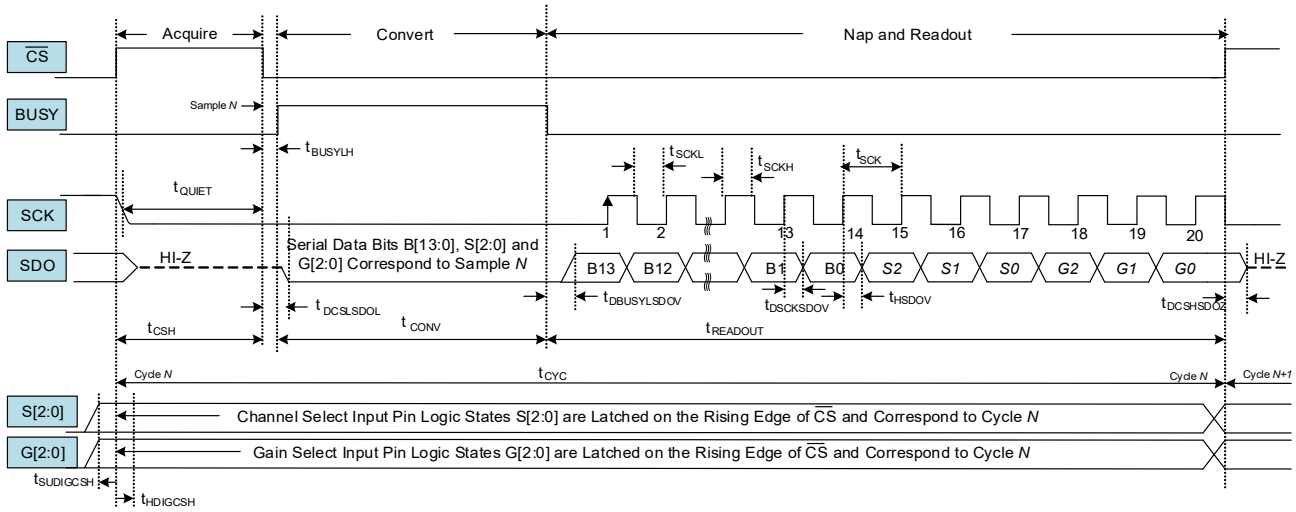


Figure 7. SCAN Timing Diagram - Normal Mode



Note: Bits S2, S1, S0, G2, G1, and G0 are optional and not required. For maximum sample rate, do not provide additional clocks for these bits.

Figure 8. Operational Timing Diagram - Low Power Mode

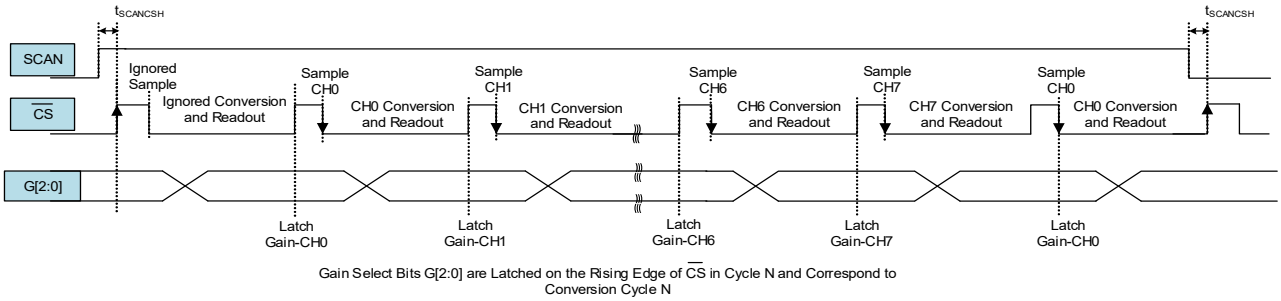


Figure 9. SCAN Timing Diagram - Low Power Mode

4. Typical Performance Curves

4.1 Normal Operation

Unless otherwise noted, AV_{CC} = 5.0V; DV_{CC} = 2.5V, REF = 2.5V, GND = 0V, PGA Bypassed, LPM = 0V, f_{SAMP} = 900.901ksps, F_{IN} = 20.3kHz, A_{IN} = -1dBFS; T_A = 25°C.

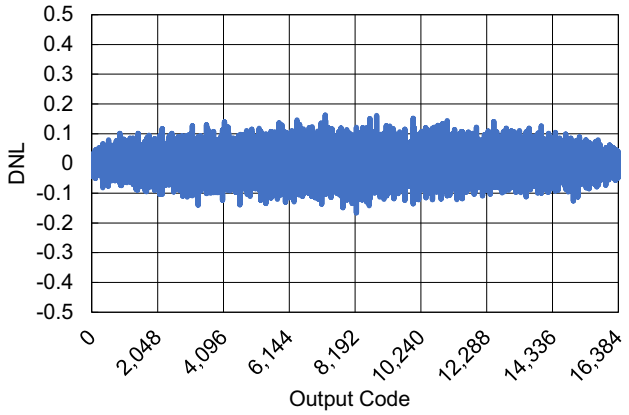


Figure 10. Differential Non-Linearity (DNL)

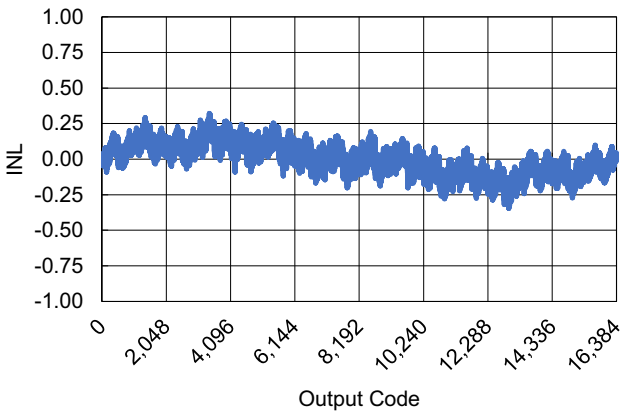


Figure 11. Integral Non-Linearity (INL)

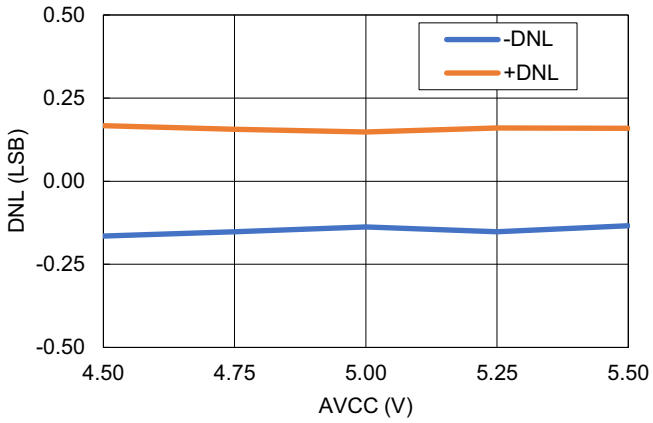


Figure 12. DNL vs AVCC

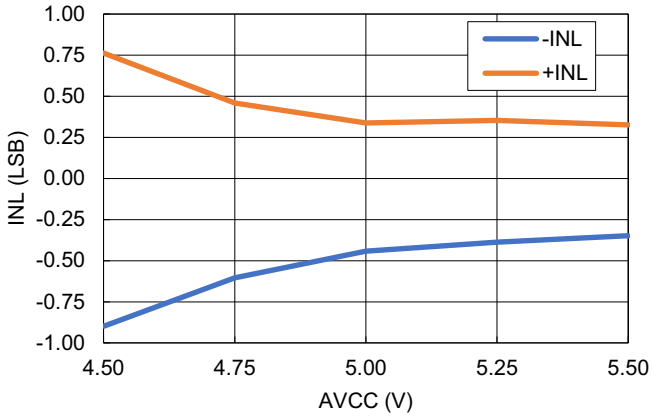


Figure 13. INL vs AVCC

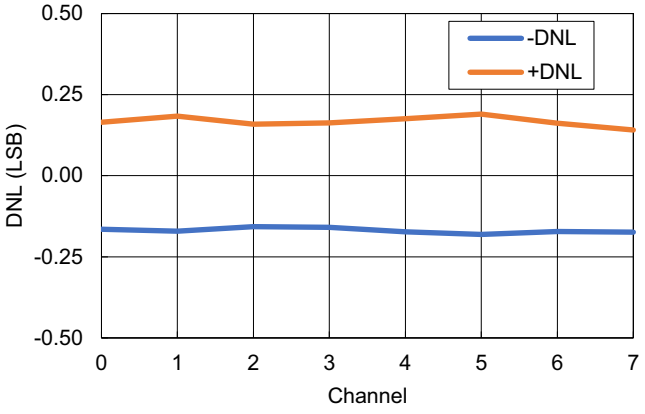


Figure 14. DNL vs Channel

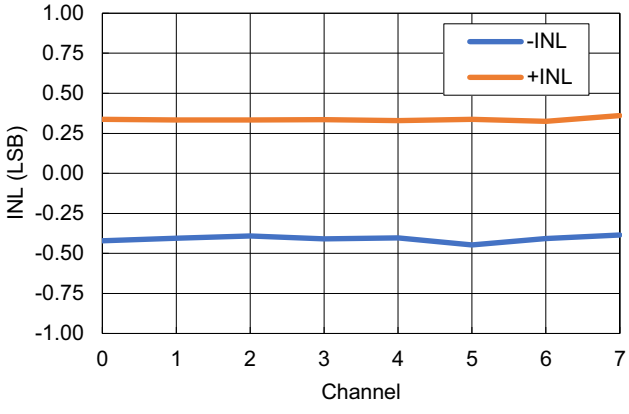


Figure 15. INL vs Channel

Unless otherwise noted, AV_{CC} = 5.0V; DV_{CC} = 2.5V, REF = 2.5V, GND = 0V, PGA Bypassed, LPM = 0V, f_{SAMP} = 900.901ksps, F_{IN} = 20.3kHz, A_{IN} = -1dBFS; T_A = 25°C.

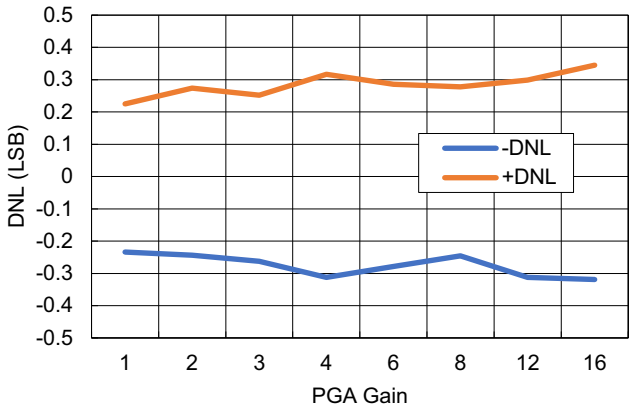


Figure 16. DNL vs PGA Gain

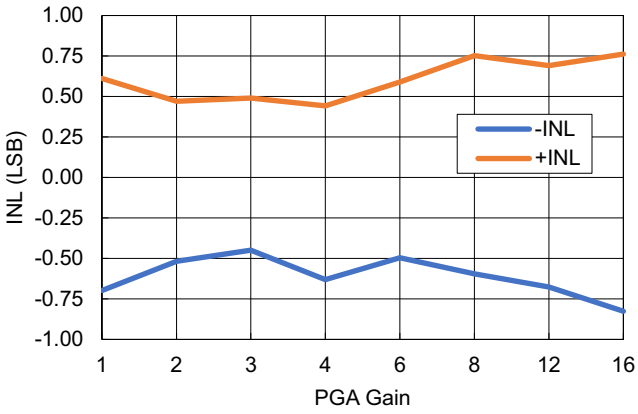


Figure 17. INL vs PGA Gain

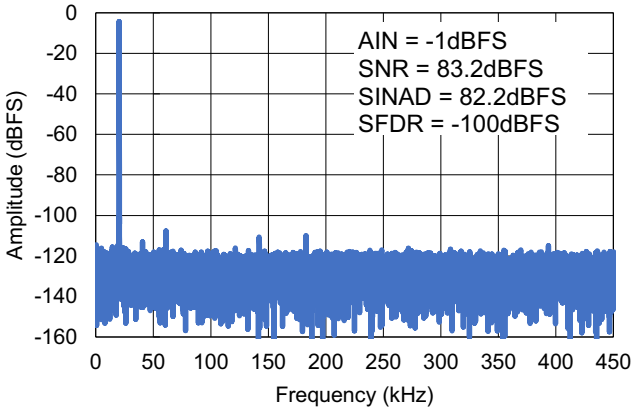


Figure 18. 32k FFT - 20.3kHz

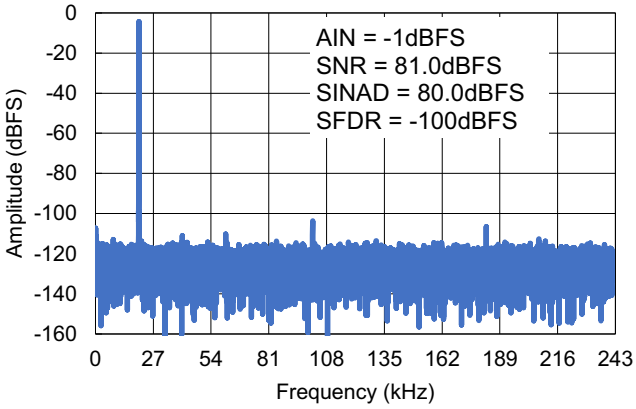


Figure 19. 32k FFT - 20.3kHz, PGA = 1

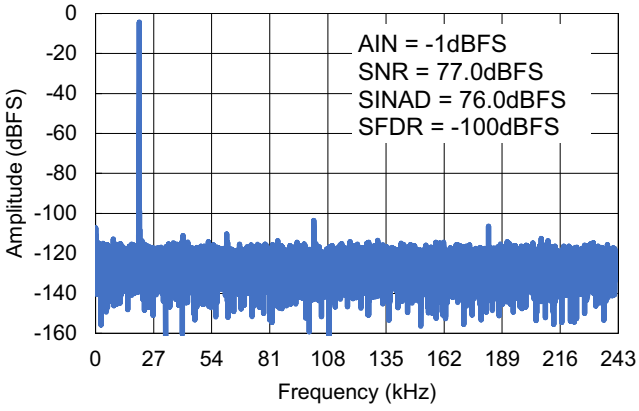


Figure 20. 32k FFT - 20.3kHz, PGA = 2

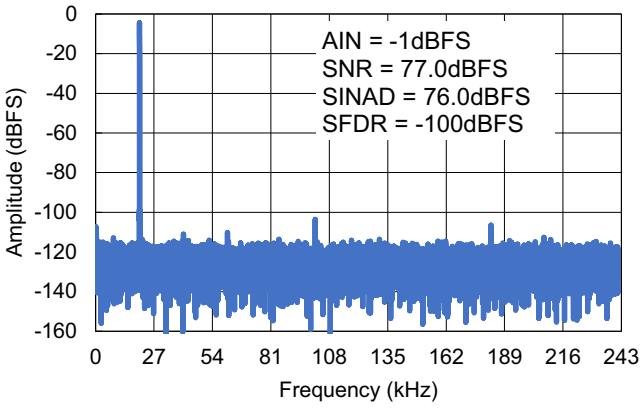


Figure 21. 32k FFT - 20.3kHz, PGA = 4

Unless otherwise noted, AV_{CC} = 5.0V; DV_{CC} = 2.5V, REF = 2.5V, GND = 0V, PGA Bypassed, LPM = 0V, f_{SAMP} = 900.901ksps, F_{IN} = 20.3kHz, A_{IN} = -1dBFS; T_A = 25°C.

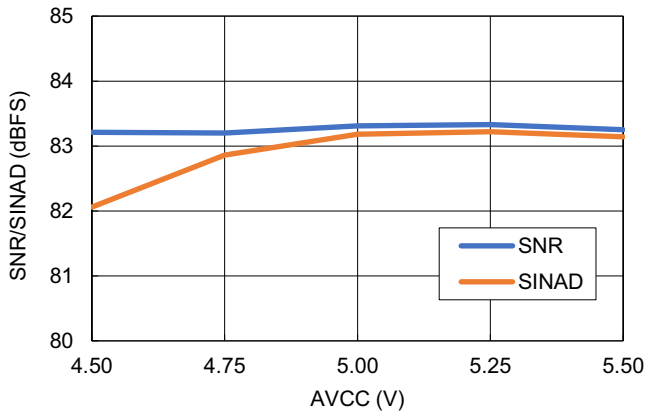


Figure 22. SNR and SINAD vs AVCC

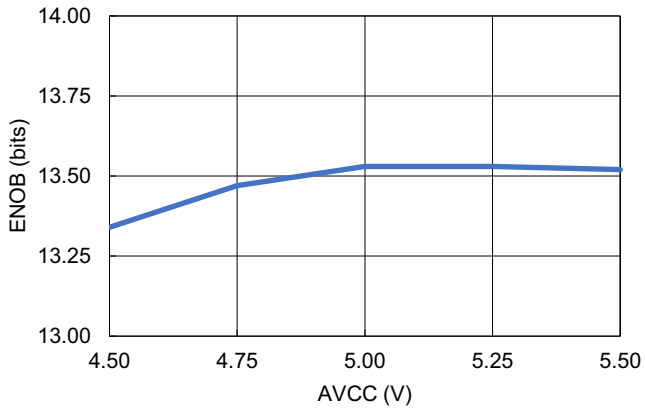


Figure 23. ENOB vs AVCC

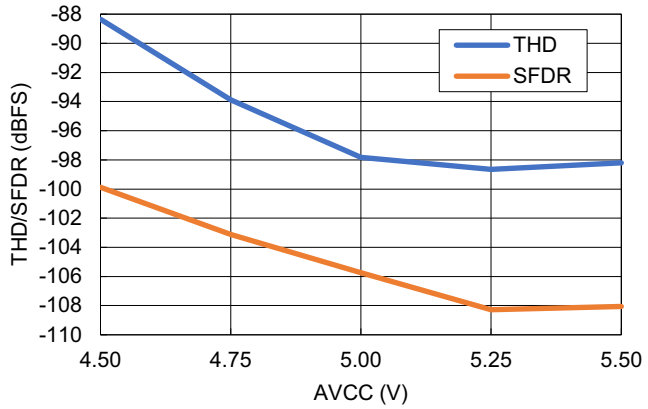


Figure 24. THD and SFDR vs AVCC

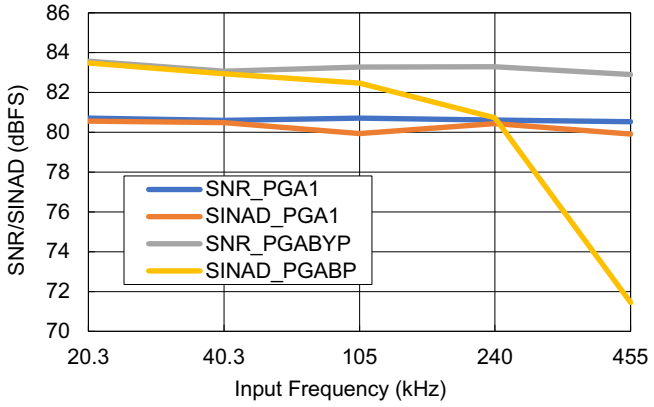


Figure 25. SNR and SINAD vs Frequency

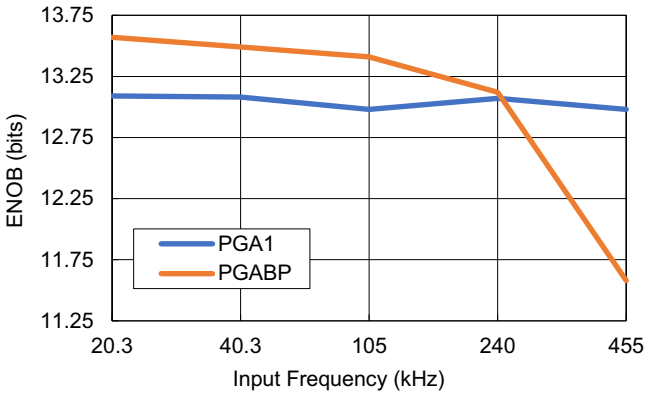


Figure 26. ENOB vs Frequency

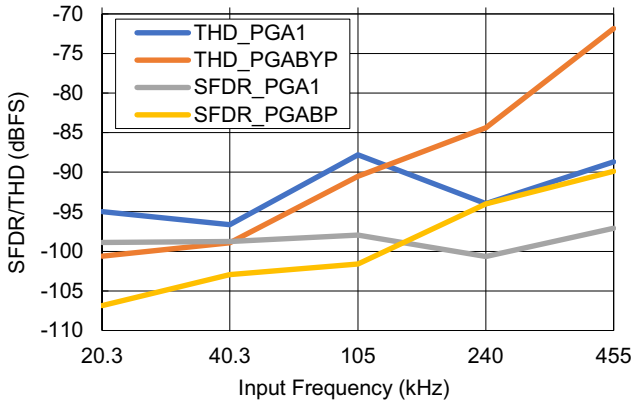


Figure 27. THD and SFDR vs Frequency

Unless otherwise noted, AV_{CC} = 5.0V; DV_{CC} = 2.5V, REF = 2.5V, GND = 0V, PGA Bypassed, LPM = 0V, f_{SAMP} = 900.901ksps, F_{IN} = 20.3kHz, A_{IN} = -1dBFS; T_A = 25°C.

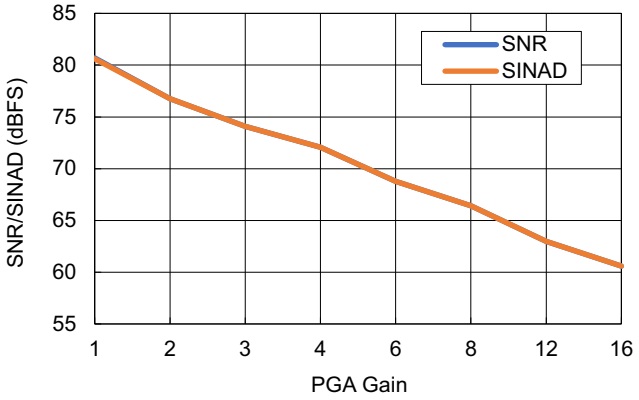


Figure 28. SNR and SINAD vs PGA Gain

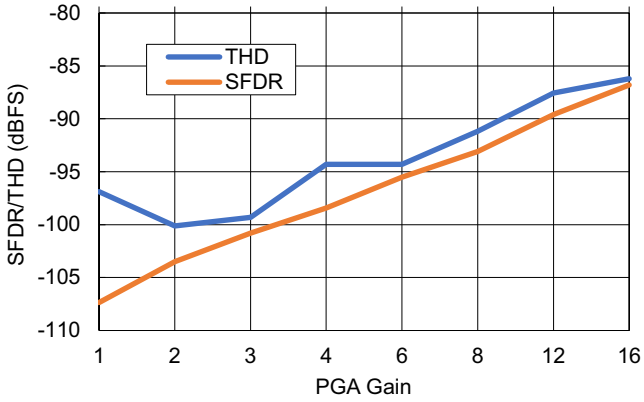


Figure 29. THD and SFDR vs PGA Gain

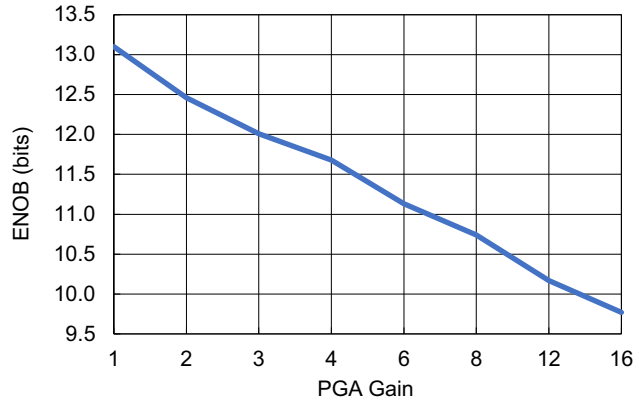


Figure 30. ENOB vs PGA Gain

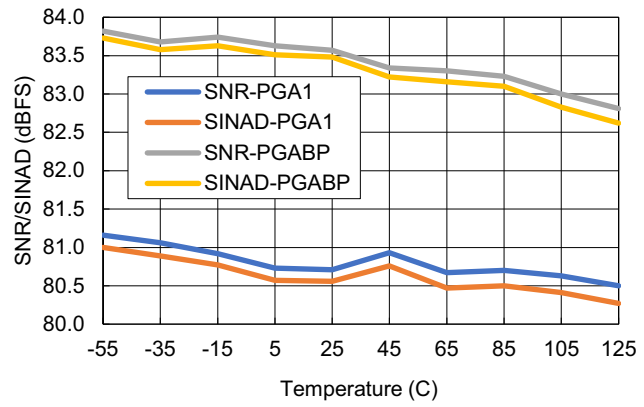


Figure 31. SNR and SINAD vs Temperature

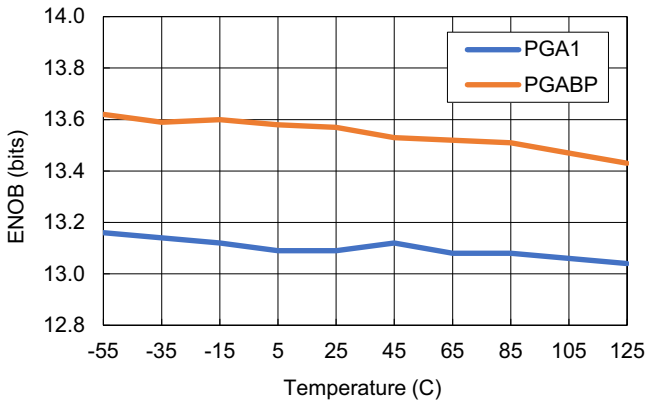


Figure 32. ENOB vs Temperature

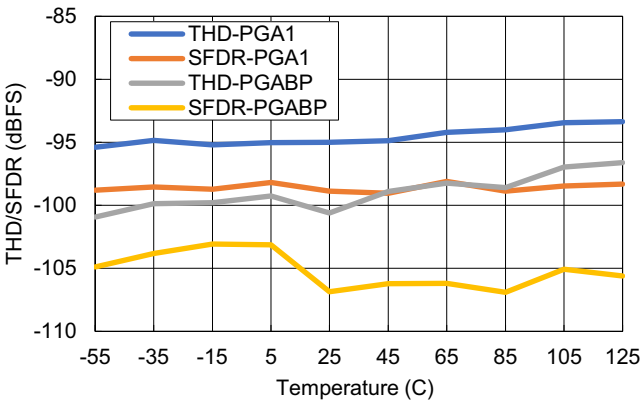


Figure 33. THD and SFDR vs Temperature

Unless otherwise noted, AV_{CC} = 5.0V; DV_{CC} = 2.5V, REF = 2.5V, GND = 0V, PGA Bypassed, LPM = 0V, f_{SAMP} = 900.901ksps, F_{IN} = 20.3kHz, A_{IN} = -1dBFS; T_A = 25°C.

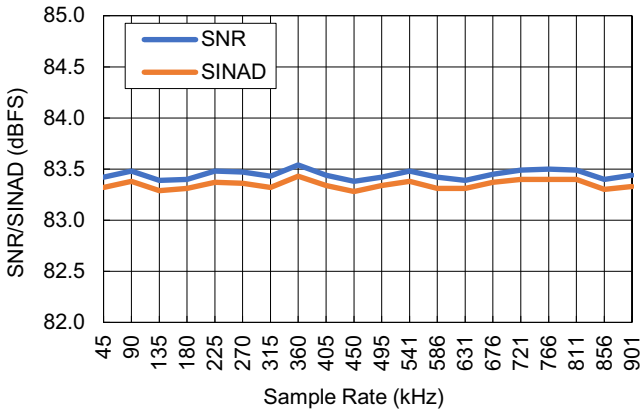


Figure 34. SNR and SINAD vs Sample Rate

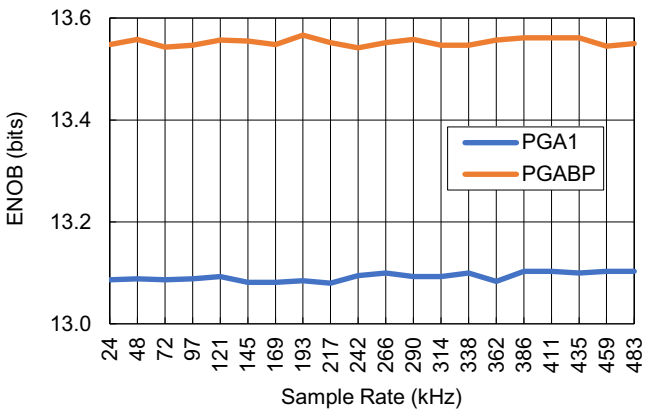


Figure 35. ENOB vs Sample Rate

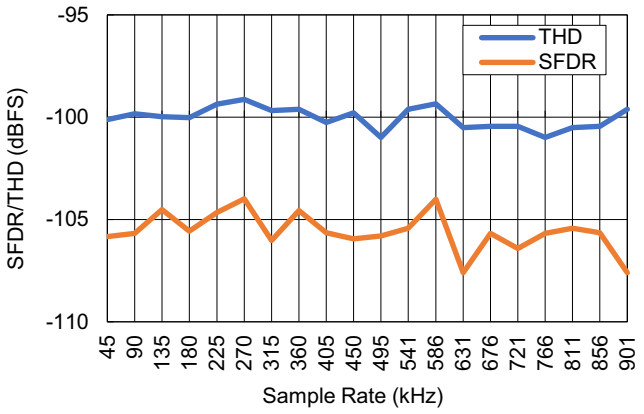


Figure 36. THD and SFDR vs Sample Rate

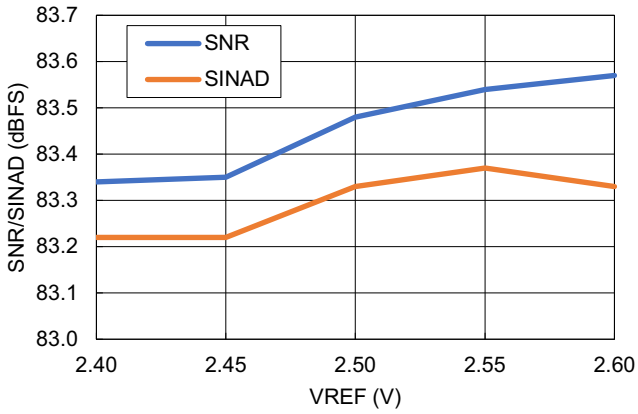


Figure 37. SNR and SINAD vs VREF

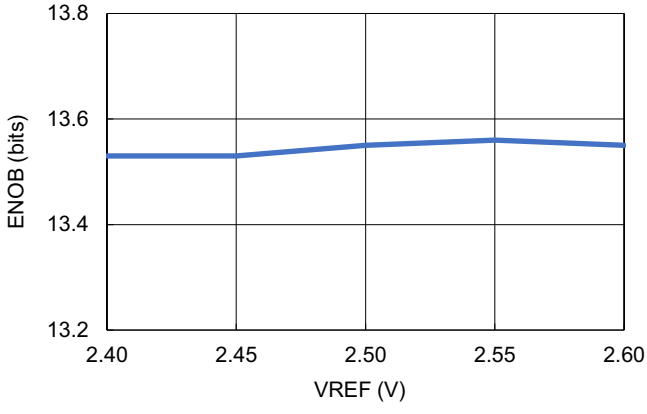


Figure 38. ENOB vs VREF

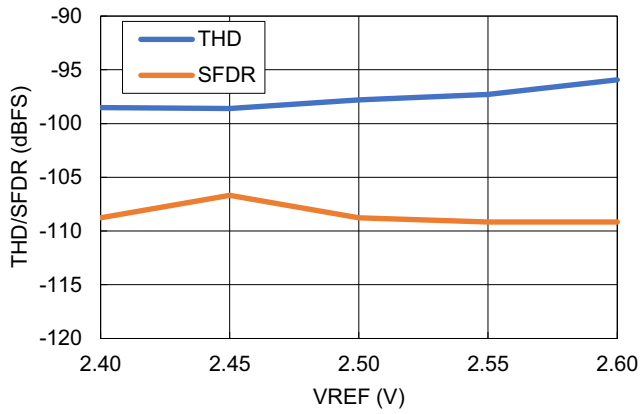


Figure 39. THD and SFDR vs VREF

Unless otherwise noted, AV_{CC} = 5.0V; DV_{CC} = 2.5V, REF = 2.5V, GND = 0V, PGA Bypassed, LPM = 0V, f_{SAMP} = 900.901ksps, F_{IN} = 20.3kHz, A_{IN} = -1dBFS; T_A = 25°C.

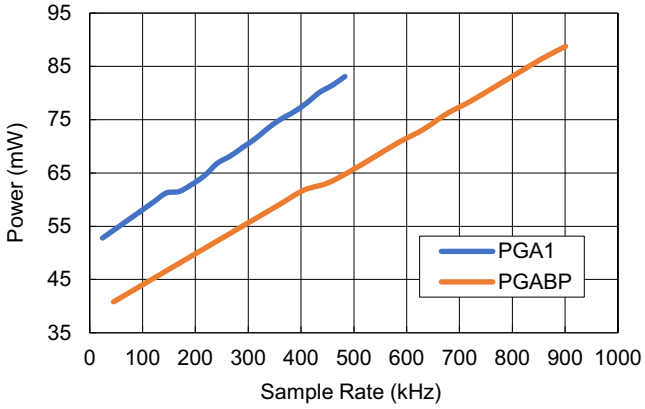


Figure 40. Power vs Sample Rate

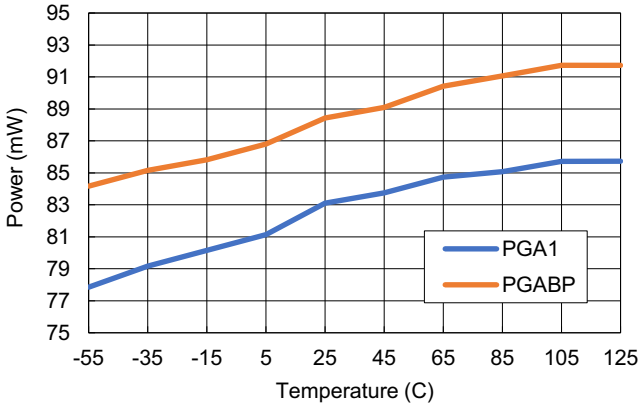


Figure 41. Power vs Temperature

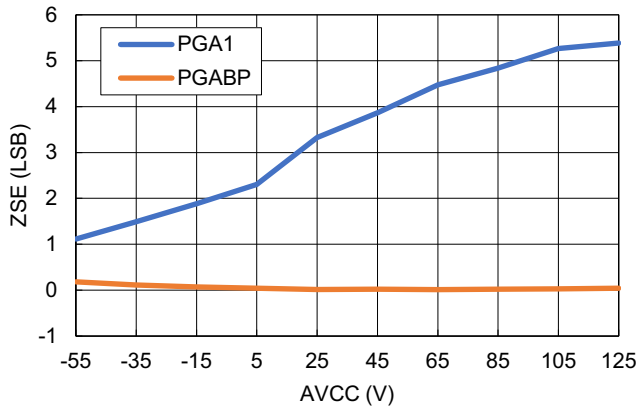


Figure 42. Zero Scale Error vs Temperature

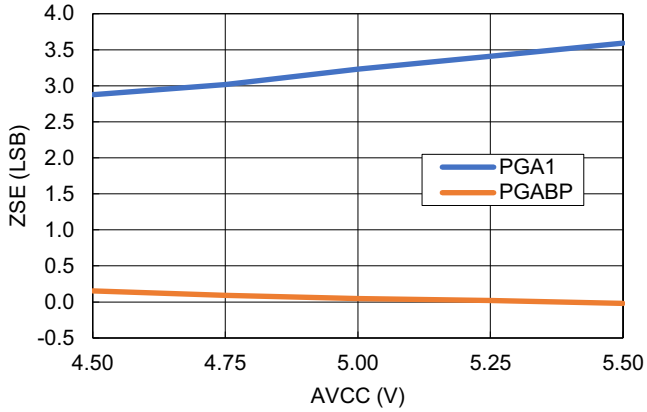


Figure 43. Zero-Scale Error vs AVCC

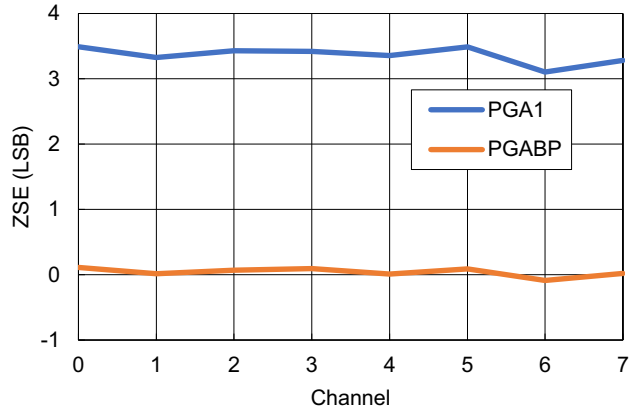


Figure 44. Zero-Scale Error vs Channel

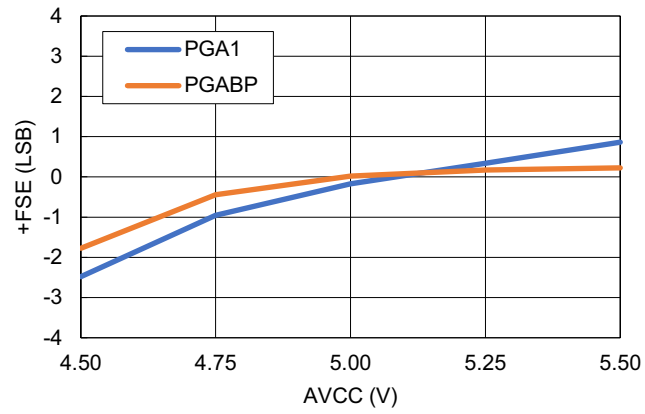


Figure 45. +Full-Scale Error vs AVCC

Unless otherwise noted, AV_{CC} = 5.0V; DV_{CC} = 2.5V, REF = 2.5V, GND = 0V, PGA Bypassed, LPM = 0V, f_{SAMP} = 900.901ksps, F_{IN} = 20.3kHz, A_{IN} = -1dBFS; T_A = 25°C.

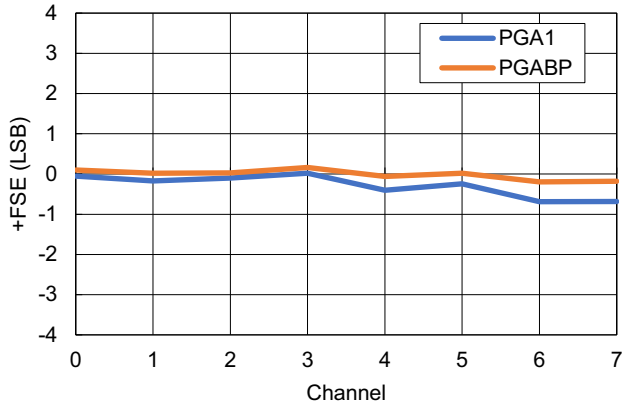


Figure 46. +Full-Scale Error vs Channel

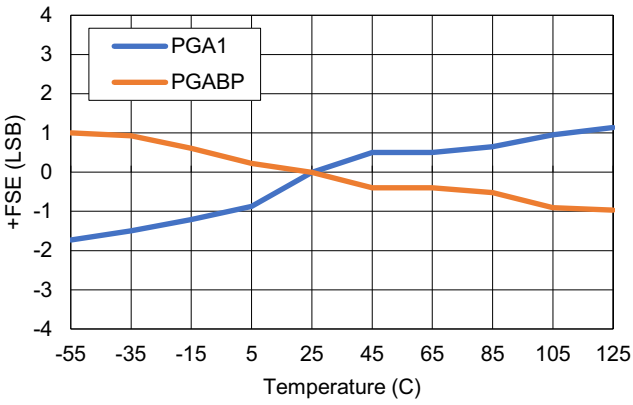


Figure 47. +Full-Scale Error vs Temperature

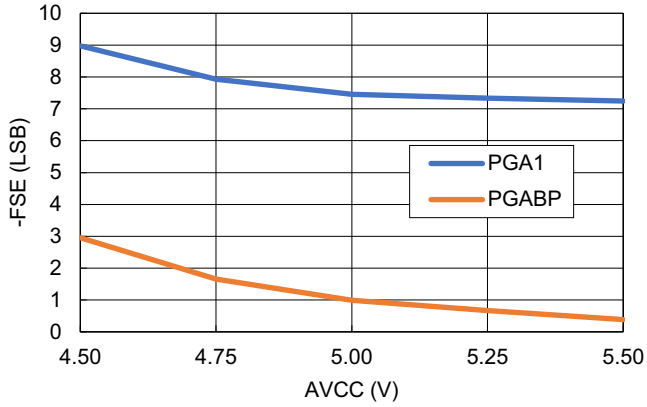


Figure 48. -Full-Scale Error vs AVCC

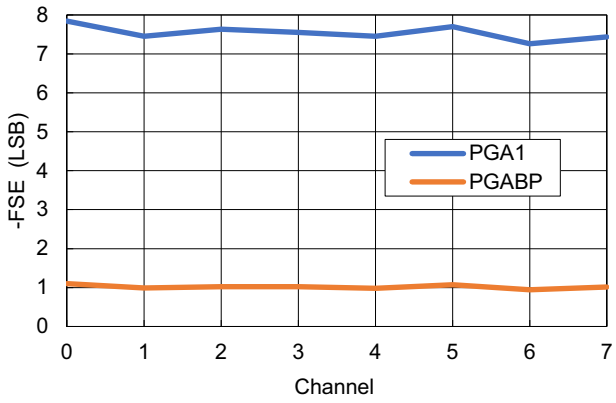


Figure 49. -Full-Scale Error vs Channel

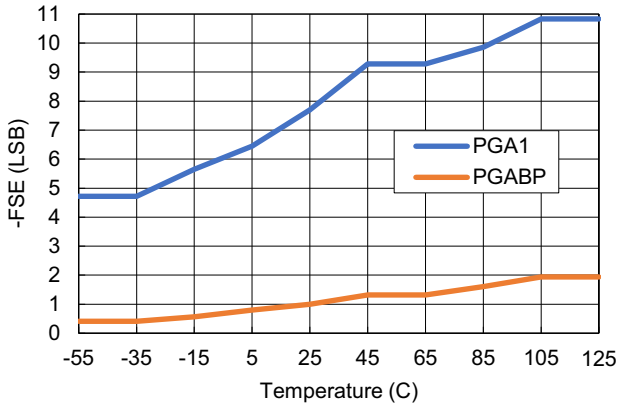


Figure 50. -Full-Scale Error vs Temperature

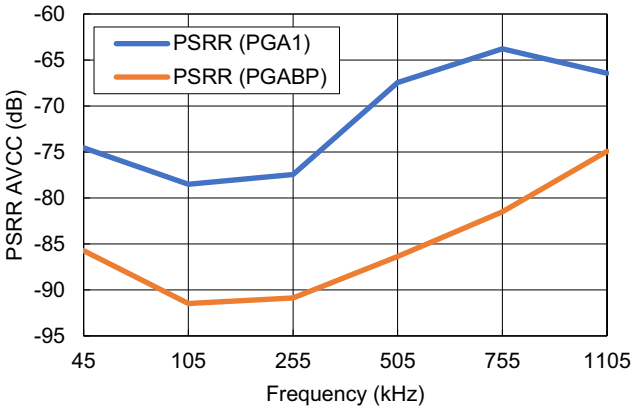


Figure 51. PSRR vs Frequency- AVCC

Unless otherwise noted, AV_{CC} = 5.0V; DV_{CC} = 2.5V, REF = 2.5V, GND = 0V, PGA Bypassed, LPM = 0V, f_{SAMP} = 900.901ksps, F_{IN} = 20.3kHz, A_{IN} = -1dBFS; T_A = 25°C.

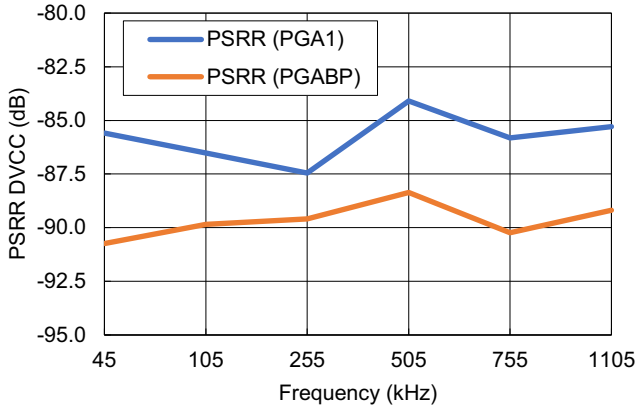


Figure 52. PSRR vs Frequency- DVCC

4.2 Low Power Mode

Unless otherwise noted, AV_{CC} = 5.0V; DV_{CC} = 2.5V, REF = 2.5V, GND = 0V, PGA Bypassed, LPM = DV_{CC}, f_{SAMP} = 684.932ksps, F_{IN} = 20.3kHz, A_{IN} = -1dBFS; T_A = 25°C.

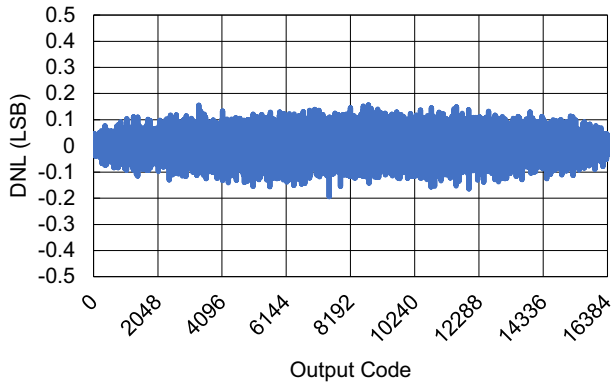


Figure 53. Differential Non-Linearity (DNL)

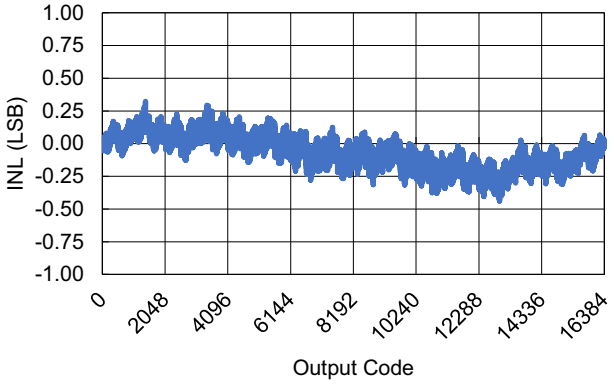


Figure 54. Integral Non-Linearity (INL)

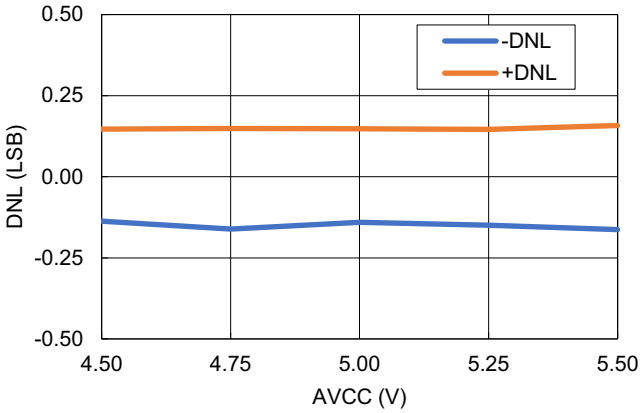


Figure 55. DNL vs AVCC

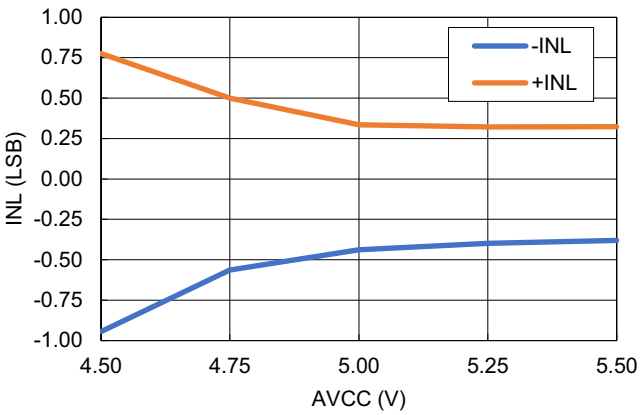


Figure 56. INL vs AVCC

Unless otherwise noted, AV_{CC} = 5.0V; DV_{CC} = 2.5V, REF = 2.5V, GND = 0V, PGA Bypassed, LPM = DV_{CC}, f_{SAMP} = 684.932ksps, F_{IN} = 20.3kHz, A_{IN} = -1dBFS; T_A = 25°C.

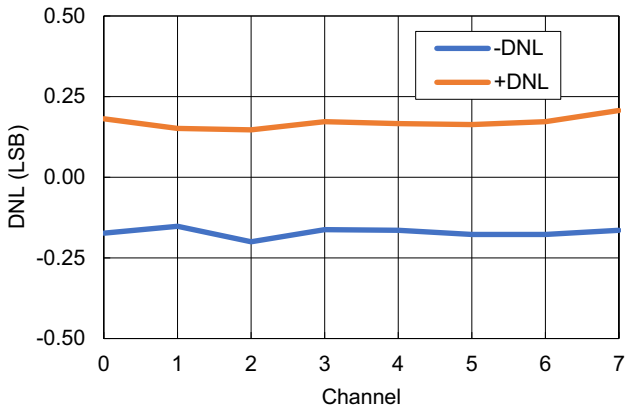


Figure 57. DNL vs Channel

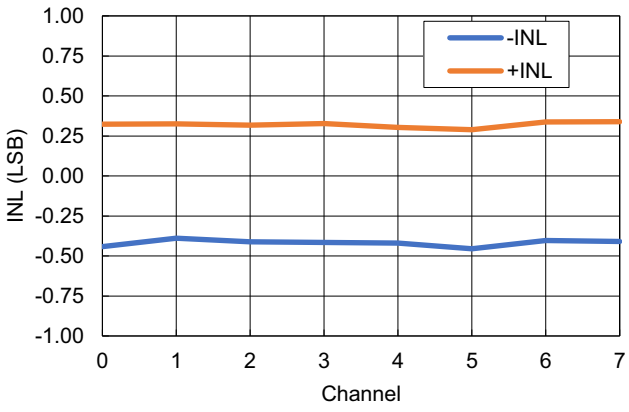


Figure 58. INL vs Channel

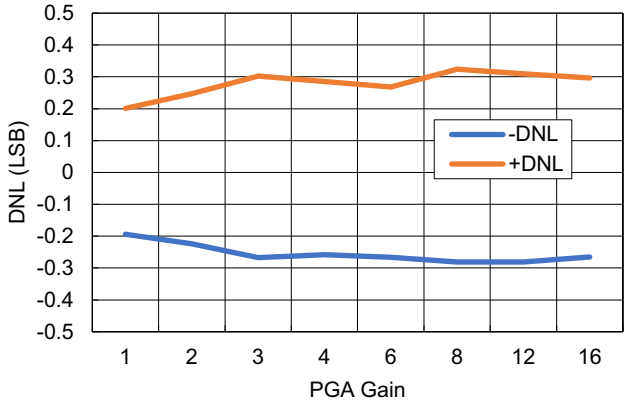


Figure 59. DNL vs PGA Gain

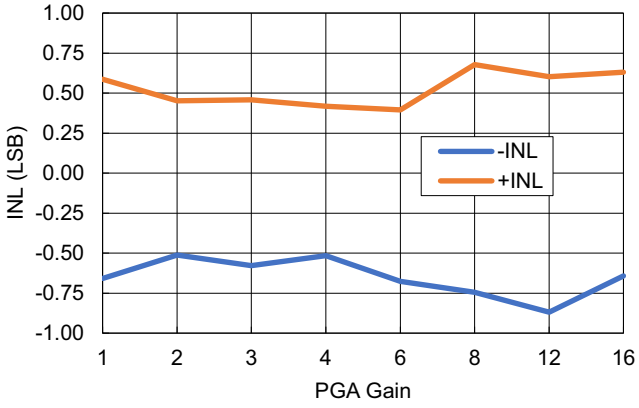


Figure 60. INL vs PGA Gain

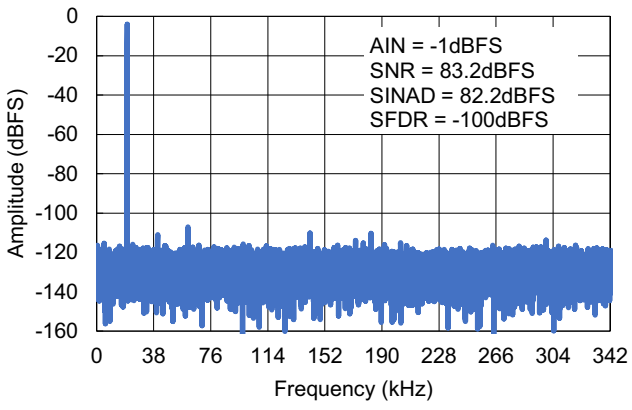


Figure 61. 32k FFT - 20.3kHz

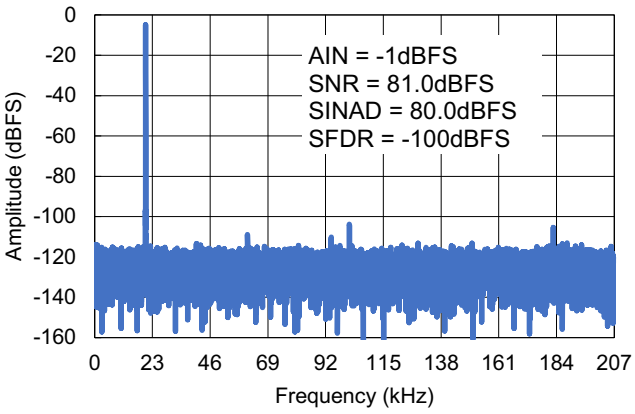


Figure 62. 32k FFT - 20.3kHz, PGA = 1

Unless otherwise noted, AV_{CC} = 5.0V; DV_{CC} = 2.5V, REF = 2.5V, GND = 0V, PGA Bypassed, LPM = DV_{CC}, f_{SAMP} = 684.932ksps, F_{IN} = 20.3kHz, A_{IN} = -1dBFS; T_A = 25°C.

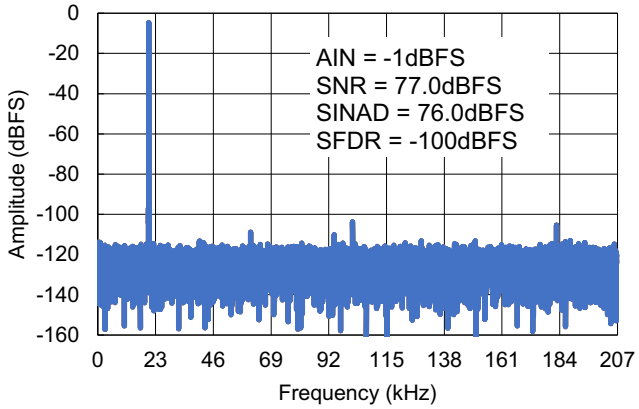


Figure 63. 32k FFT - 20.3kHz, PGA = 2

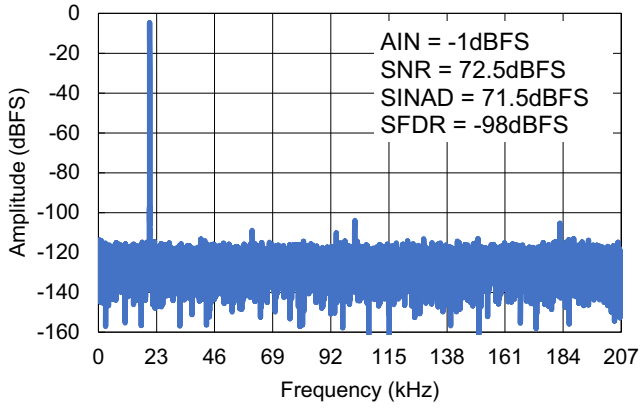


Figure 64. 32k FFT - 20.3kHz, PGA = 4

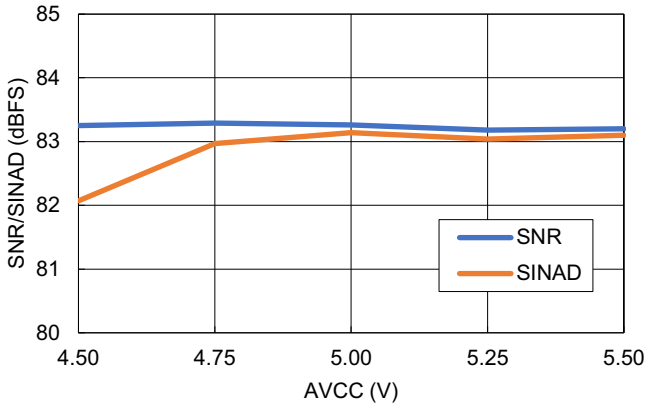


Figure 65. SNR and SINAD vs AVCC

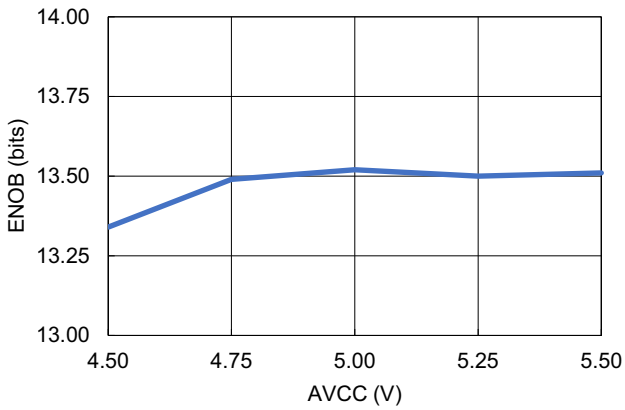


Figure 66. ENOB vs AVCC

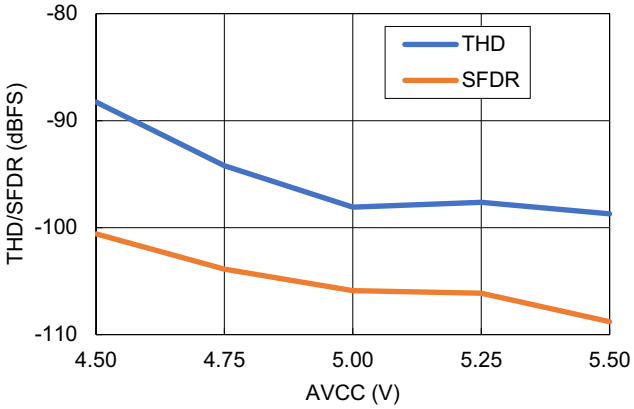


Figure 67. THD and SFDR vs AVCC

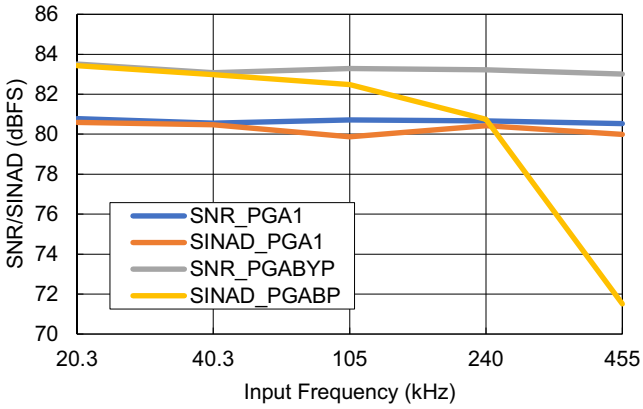


Figure 68. SNR and SINAD vs Frequency

Unless otherwise noted, AV_{CC} = 5.0V; DV_{CC} = 2.5V, REF = 2.5V, GND = 0V, PGA Bypassed, LPM = DV_{CC}, f_{SAMP} = 684.932ksps, F_{IN} = 20.3kHz, A_{IN} = -1dBFS; T_A = 25°C.

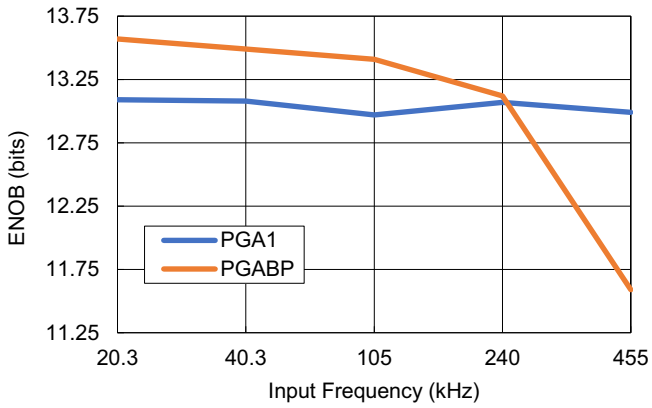


Figure 69. ENOB vs Frequency

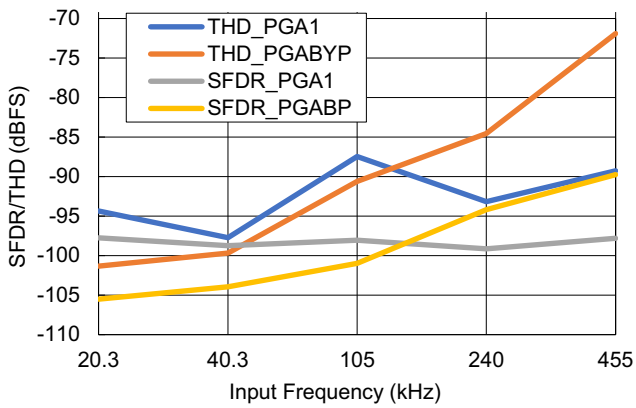


Figure 70. THD and SFDR vs Frequency

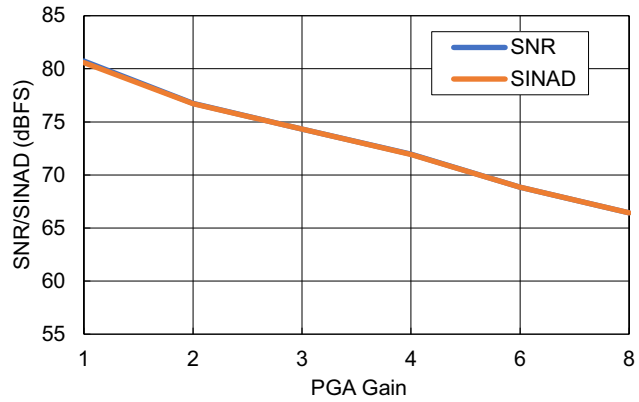


Figure 71. SNR and SINAD vs PGA Gain

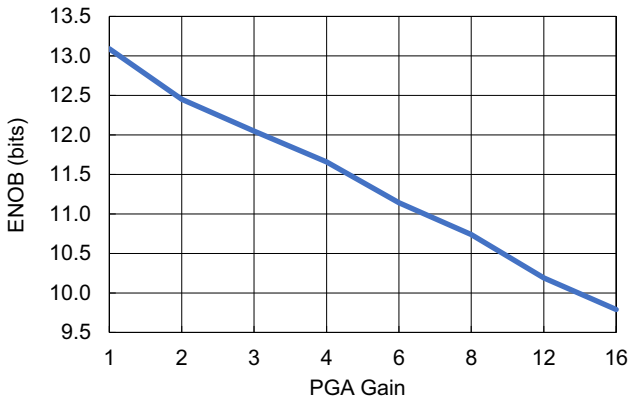


Figure 72. ENOB vs PGA Gain

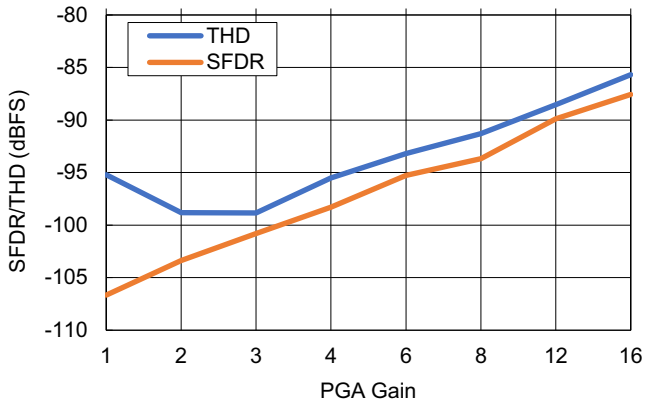


Figure 73. THD and SFDR vs PGA Gain

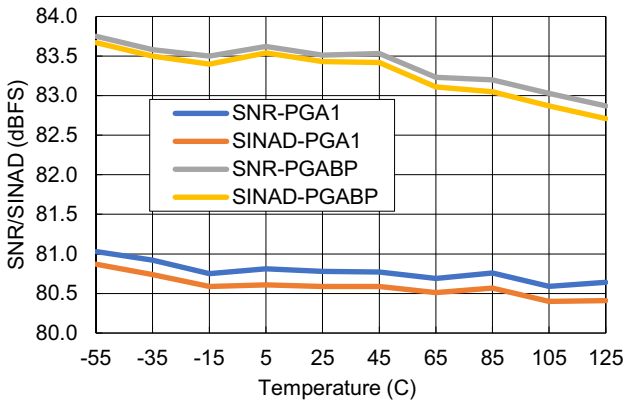


Figure 74. SNR and SINAD vs Temperature

Unless otherwise noted, AV_{CC} = 5.0V; DV_{CC} = 2.5V, REF = 2.5V, GND = 0V, PGA Bypassed, LPM = DV_{CC}, f_{SAMP} = 684.932ksps, F_{IN} = 20.3kHz, A_{IN} = -1dBFS; T_A = 25°C.

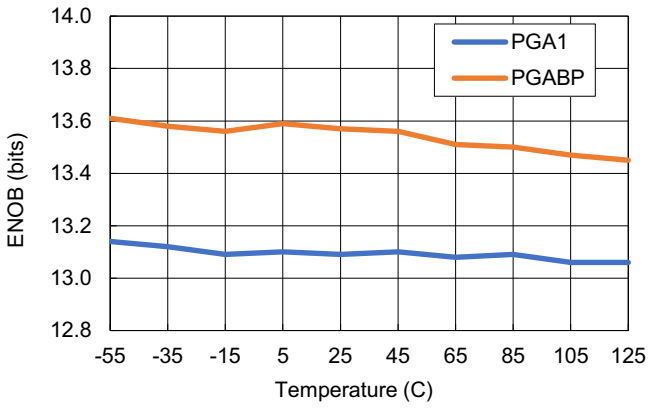


Figure 75. ENOB vs Temperature

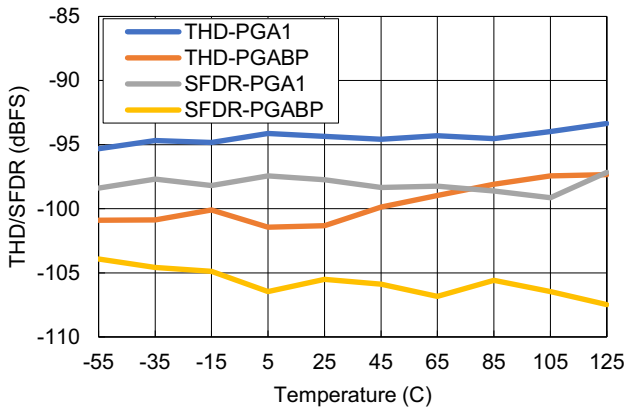


Figure 76. THD and SFDR vs Temperature

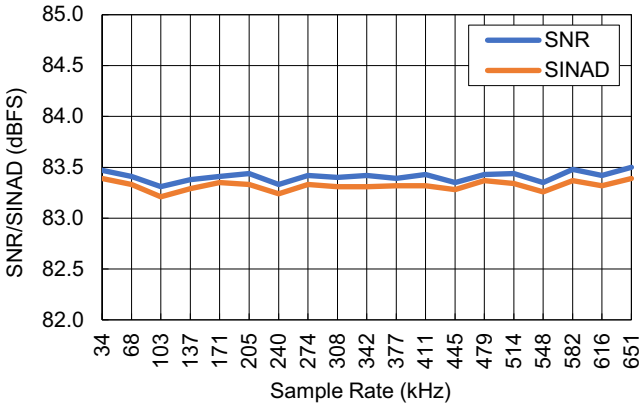


Figure 77. SNR and SINAD vs Sample Rate

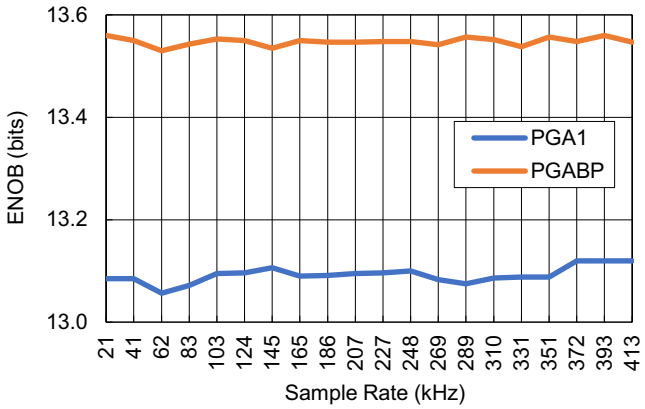


Figure 78. ENOB vs Sample Rate

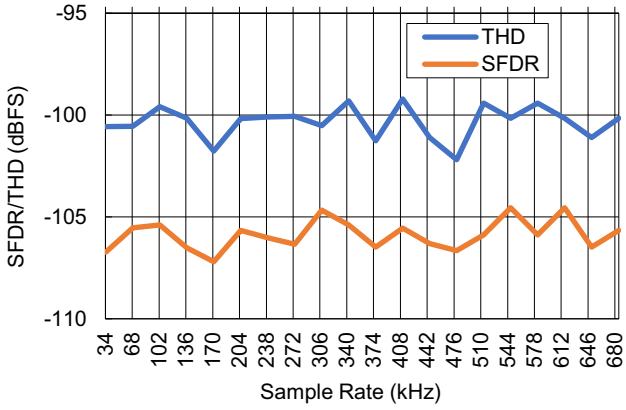


Figure 79. THD and SFDR vs Sample Rate

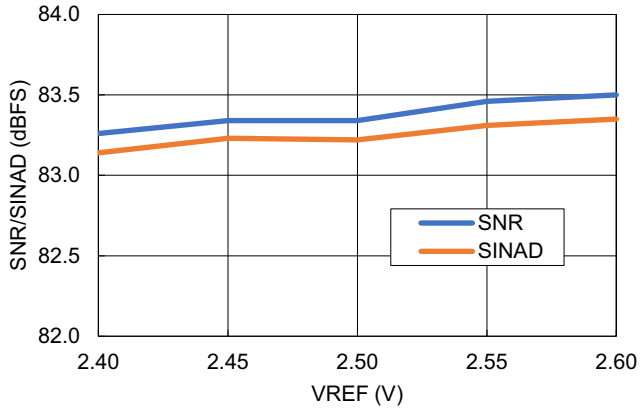


Figure 80. SNR and SINAD vs VREF

Unless otherwise noted, AV_{CC} = 5.0V; DV_{CC} = 2.5V, REF = 2.5V, GND = 0V, PGA Bypassed, LPM = DV_{CC}, f_{SAMP} = 684.932ksps, F_{IN} = 20.3kHz, A_{IN} = -1dBFS; T_A = 25°C.

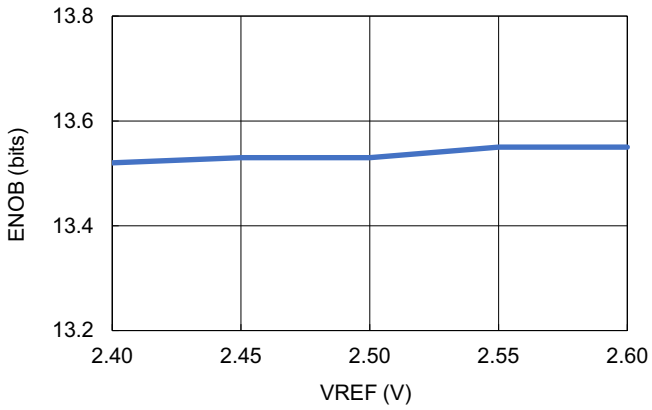


Figure 81. ENOB vs VREF

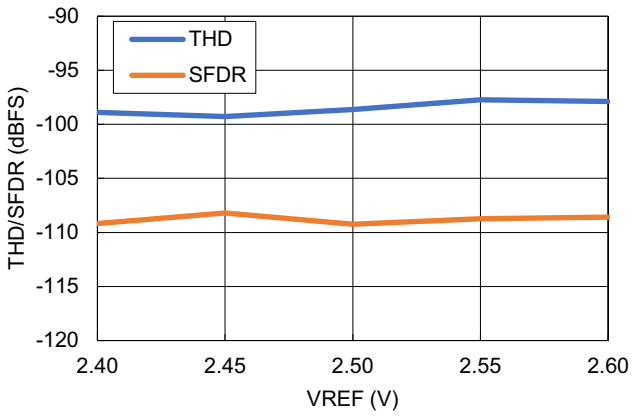


Figure 82. THD and SFDR vs VREF

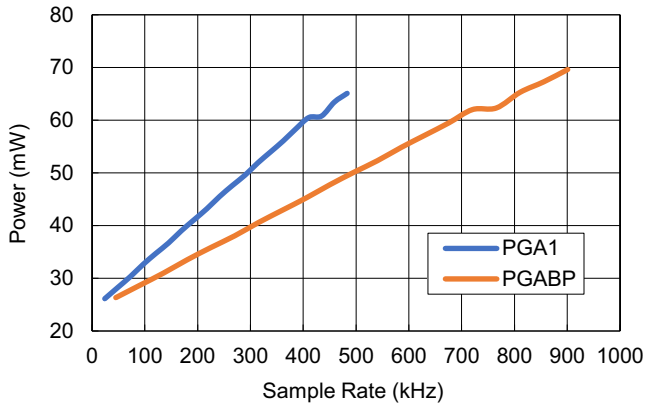


Figure 83. Power vs Sample Rate

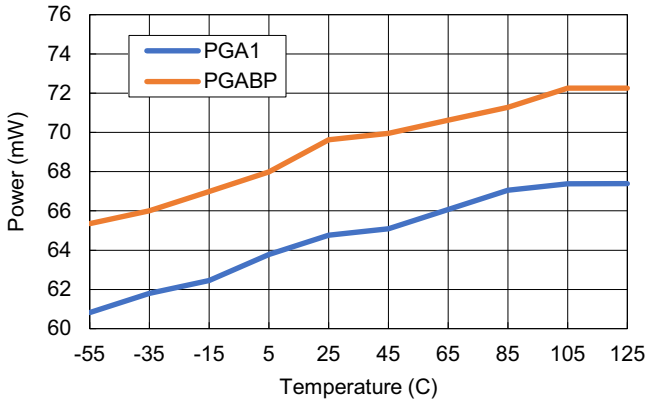


Figure 84. Power vs Temperature

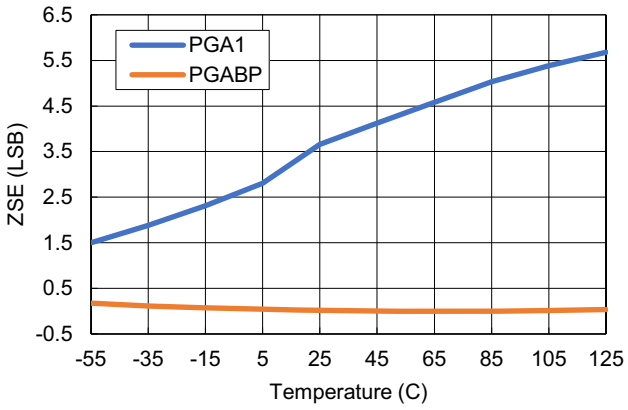


Figure 85. Zero Scale Error vs Temperature

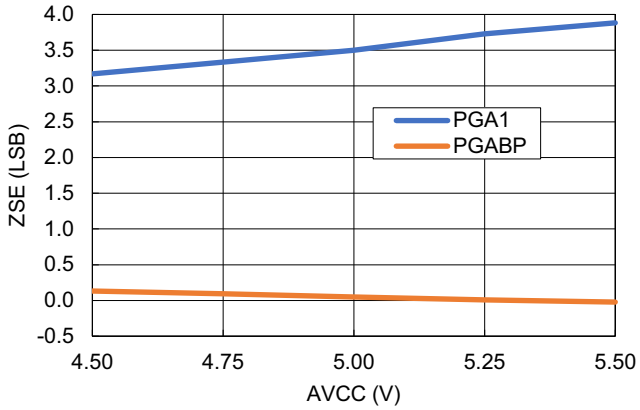


Figure 86. Zero-Scale Error vs AVCC

Unless otherwise noted, AV_{CC} = 5.0V; DV_{CC} = 2.5V, REF = 2.5V, GND = 0V, PGA Bypassed, LPM = DV_{CC}, f_{SAMP} = 684.932ksps, F_{IN} = 20.3kHz, A_{IN} = -1dBFS; T_A = 25°C.

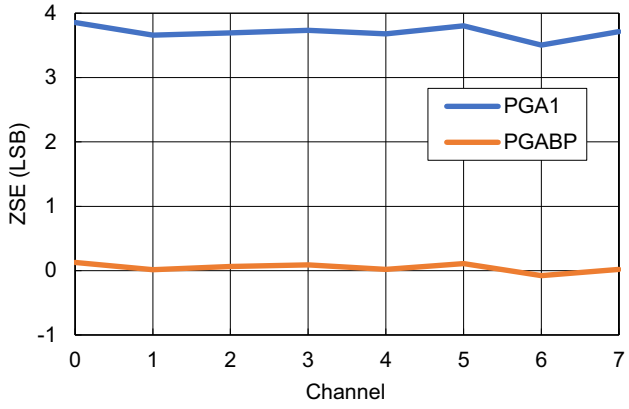


Figure 87. Zero-Scale Error vs Channel

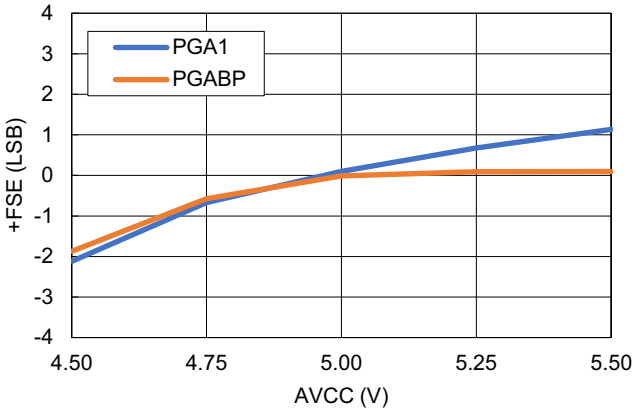


Figure 88. +Full-Scale Error vs AVCC

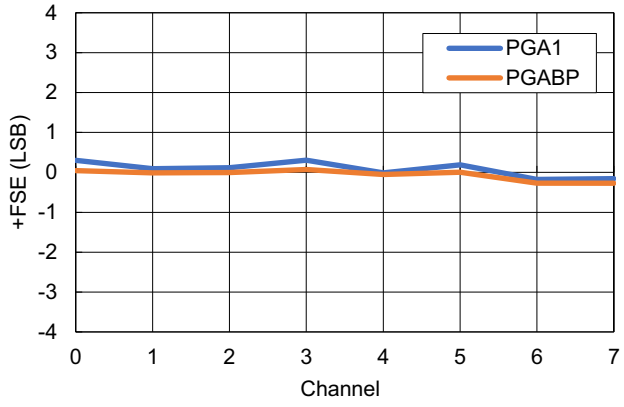


Figure 89. +Full-Scale Error vs Channel

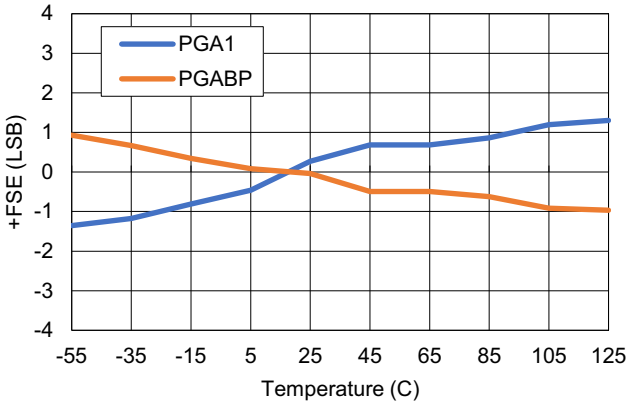


Figure 90. +Full-Scale Error vs Temperature

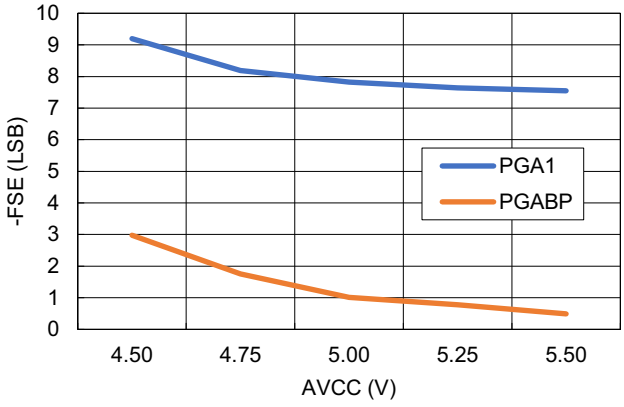


Figure 91. -Full-Scale Error vs AVCC

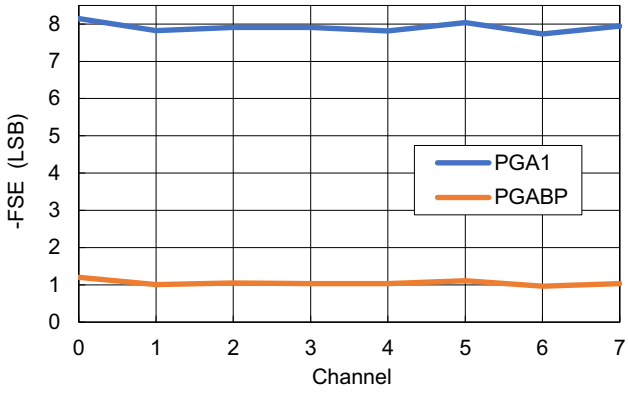


Figure 92. -Full-Scale Error vs Channel

Unless otherwise noted, AV_{CC} = 5.0V; DV_{CC} = 2.5V, REF = 2.5V, GND = 0V, PGA Bypassed, LPM = DV_{CC}, f_{SAMP} = 684.932ksps, F_{IN} = 20.3kHz, A_{IN} = -1dBFS; T_A = 25°C.

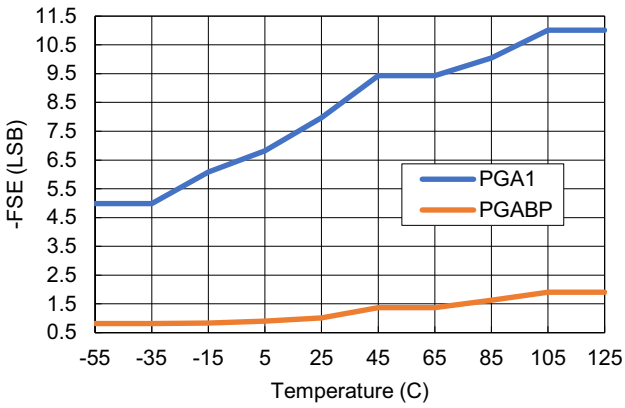


Figure 93. -Full-Scale Error vs Temperature

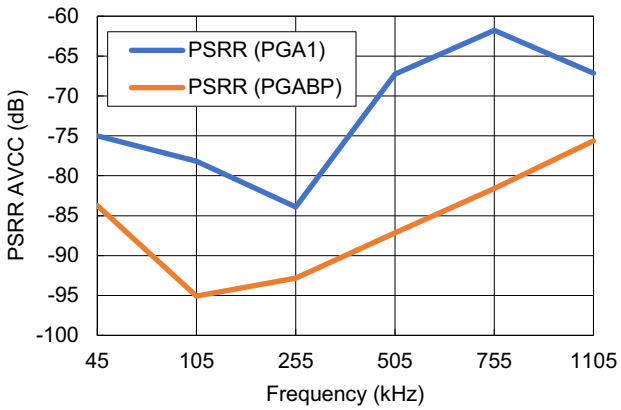


Figure 94. PSRR vs Frequency- AVCC

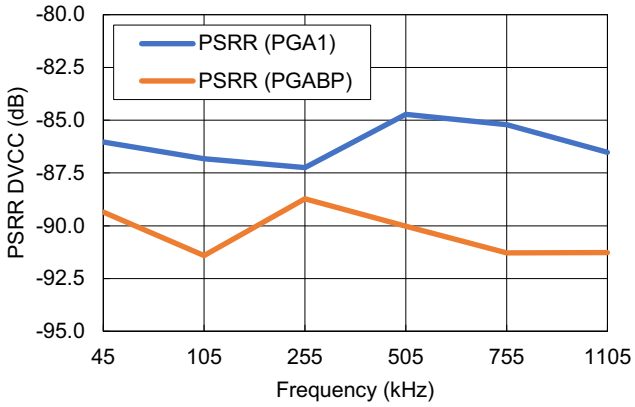


Figure 95. PSRR vs Frequency- DVCC

4.3 Single Ended Operation - Normal Mode

Unless otherwise noted, AV_{CC} = 5.0V; DV_{CC} = 2.5V, REF = 2.5V, GND = 0V, PGA Bypassed, LPM = 0V, f_{SAMP} = 684.932ksps, F_{IN} = 20.3kHz, A_{IN} = -7dBFS, CH(0:7)- connected to $V_{REF}/2$; T_A = 25°C.

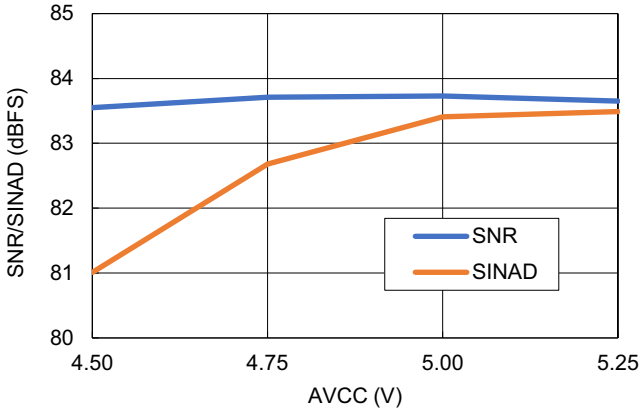


Figure 96. SNR and SINAD vs AVCC

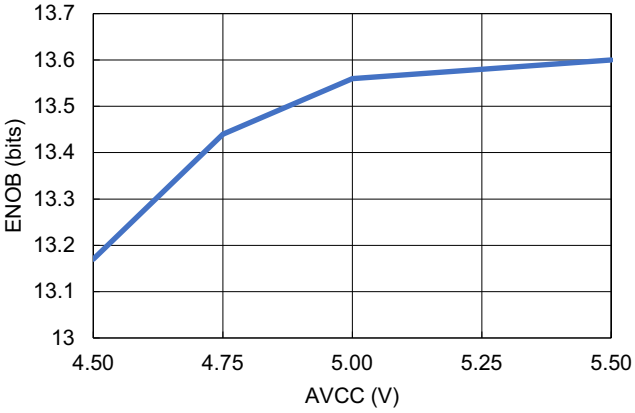


Figure 97. ENOB vs AVCC

Unless otherwise noted, AV_{CC} = 5.0V; DV_{CC} = 2.5V, REF = 2.5V, GND = 0V, PGA Bypassed, LPM = 0V, f_{SAMP} = 684.932ksps, F_{IN} = 20.3kHz, A_{IN} = -7dBFS, CH(0:7)- connected to $V_{REF}/2$; T_A = 25°C.

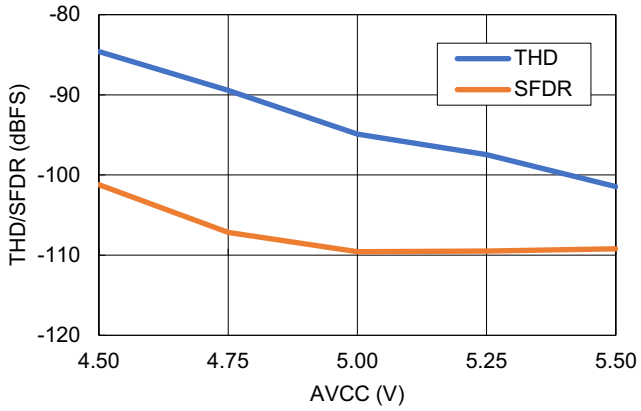


Figure 98. THD and SFDR vs AVCC

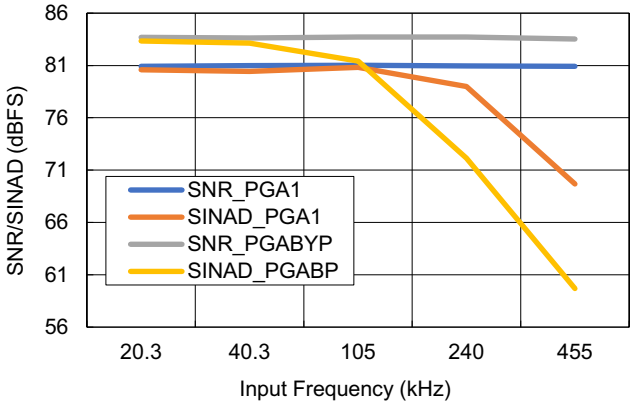


Figure 99. SNR and SINAD vs Frequency

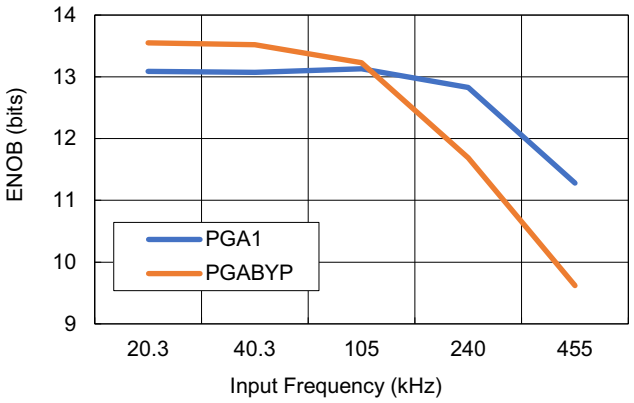


Figure 100. ENOB vs Frequency

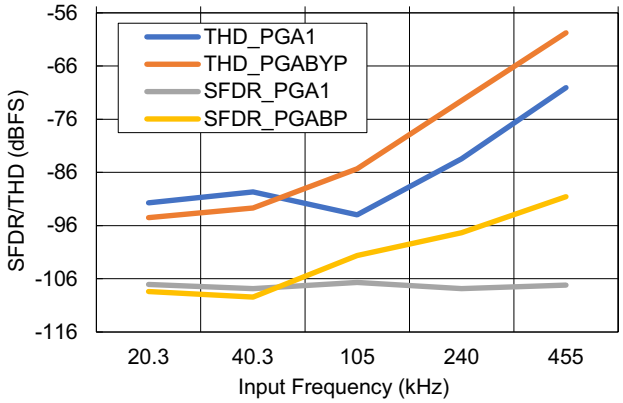


Figure 101. THD and SFDR vs Frequency

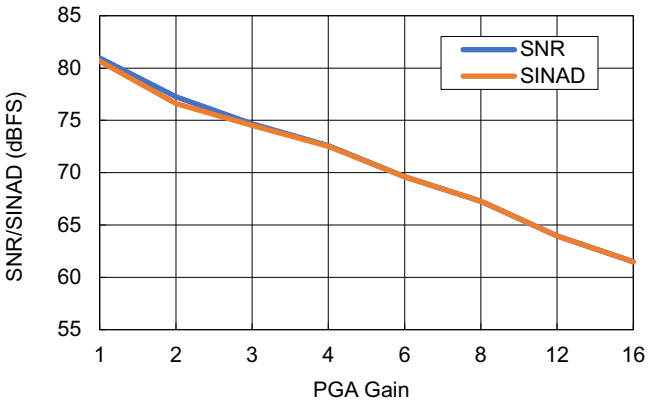


Figure 102. SNR and SINAD vs PGA Gain

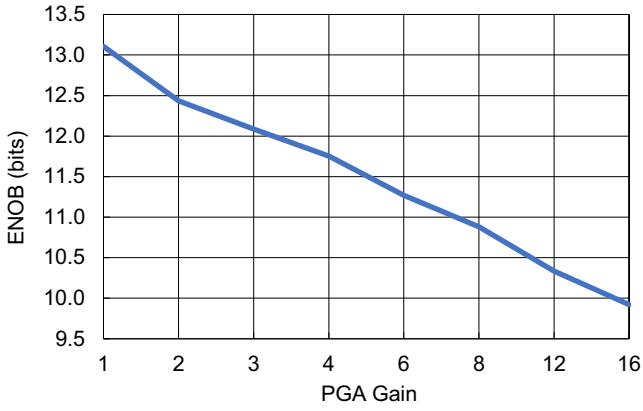


Figure 103. ENOB vs PGA Gain

Unless otherwise noted, AV_{CC} = 5.0V; DV_{CC} = 2.5V, REF = 2.5V, GND = 0V, PGA Bypassed, LPM = 0V, f_{SAMP} = 684.932ksps, F_{IN} = 20.3kHz, A_{IN} = -7dBFS, CH(0:7)- connected to $V_{REF}/2$; T_A = 25°C.

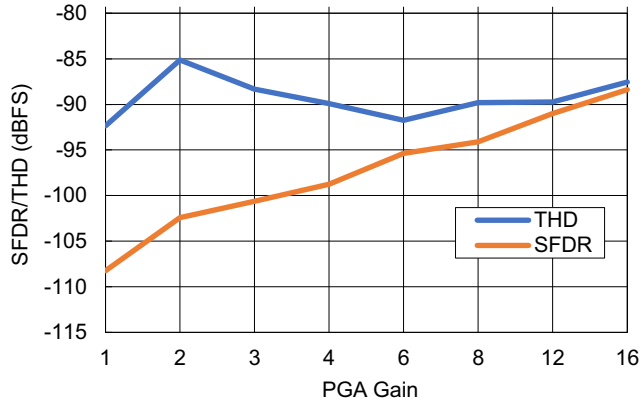


Figure 104. THD and SFDR vs PGA Gain

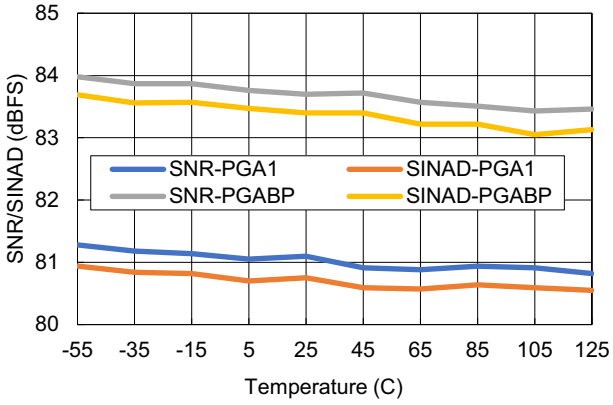


Figure 105. SNR and SINAD vs Temperature

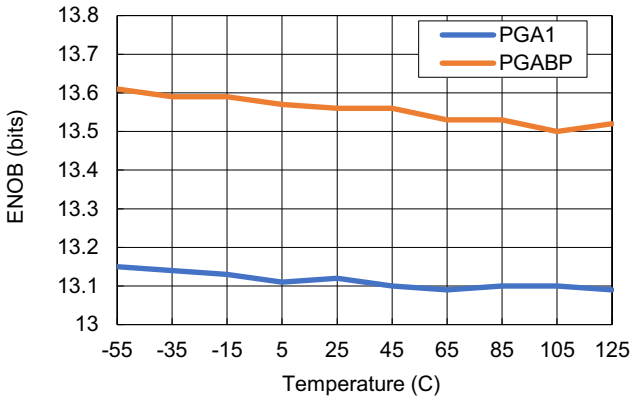


Figure 106. ENOB vs Temperature

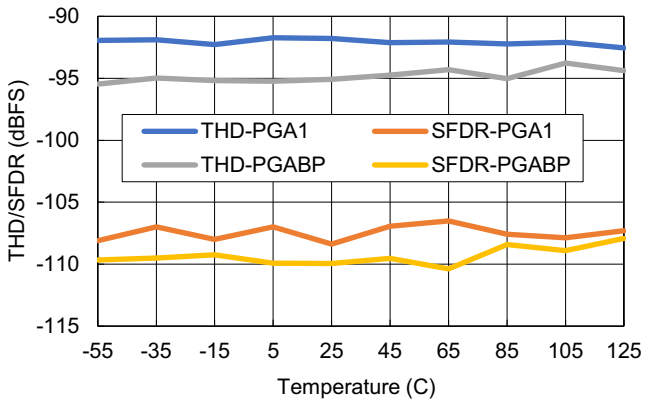


Figure 107. THD and SFDR vs Temperature

4.4 Single Ended Operation - Low Power Mode

Unless otherwise noted, AV_{CC} = 5.0V; DV_{CC} = 2.5V, REF = 2.5V, GND = 0V, PGA Bypassed, LPM = DV_{CC}, f_{SAMP} = 684.932ksps, F_{IN} = 20.3kHz, A_{IN} = -7dBFS, CH(0:7)- connected to $V_{REF}/2$; T_A = 25°C.

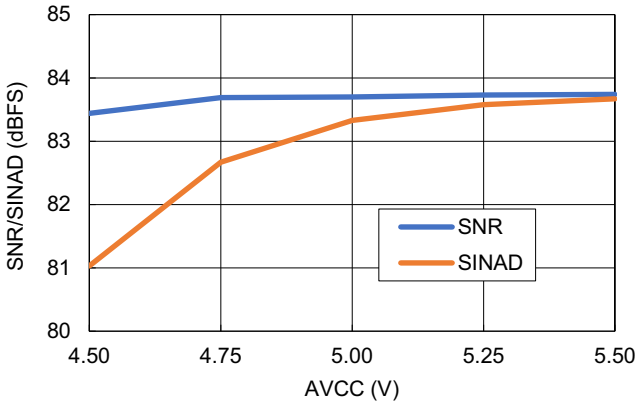


Figure 108. SNR and SINAD vs AVCC

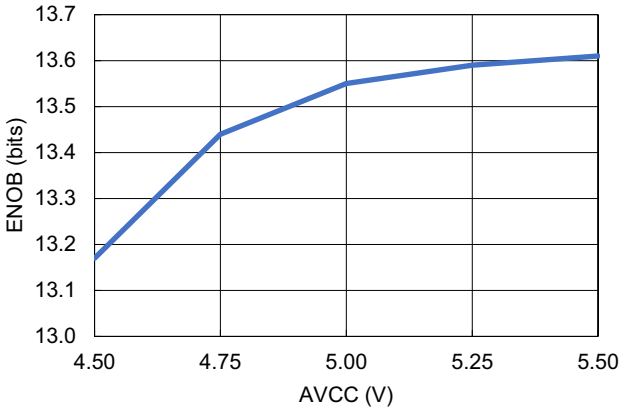


Figure 109. ENOB vs AVCC

Unless otherwise noted, AV_{CC} = 5.0V; DV_{CC} = 2.5V, REF = 2.5V, GND = 0V, PGA Bypassed, LPM = DV_{CC}, f_{SAMP} = 684.932ksps, F_{IN} = 20.3kHz, A_{IN} = -7dBFS, CH(0:7)- connected to $V_{REF}/2$; T_A = 25°C.

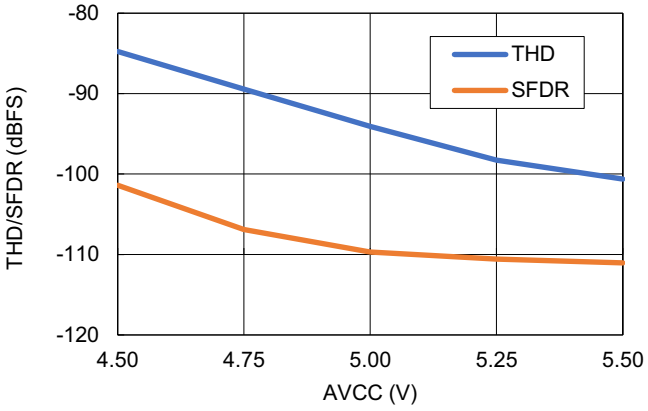


Figure 110. THD and SFDR vs AVCC

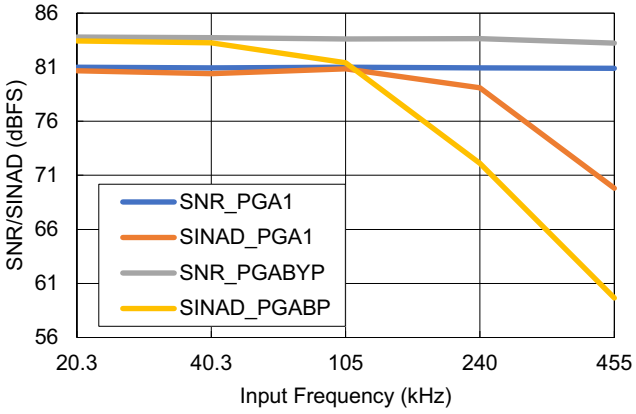


Figure 111. SNR and SINAD vs Frequency

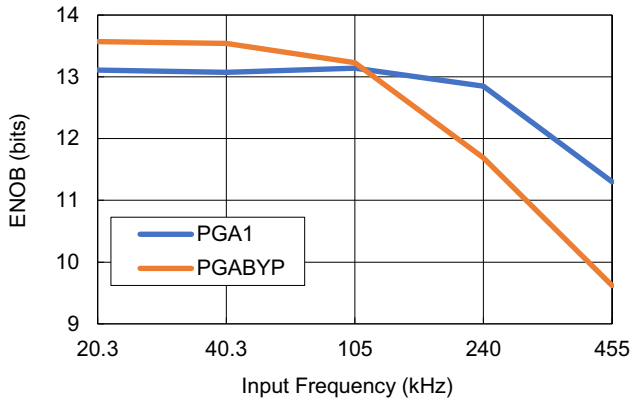


Figure 112. ENOB vs Frequency

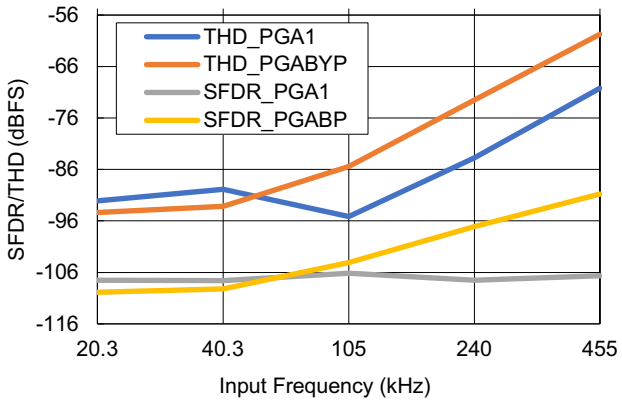


Figure 113. THD and SFDR vs Frequency

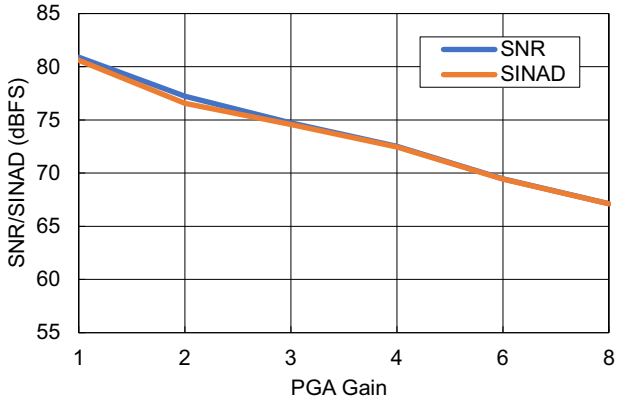


Figure 114. SNR and SINAD vs PGA Gain

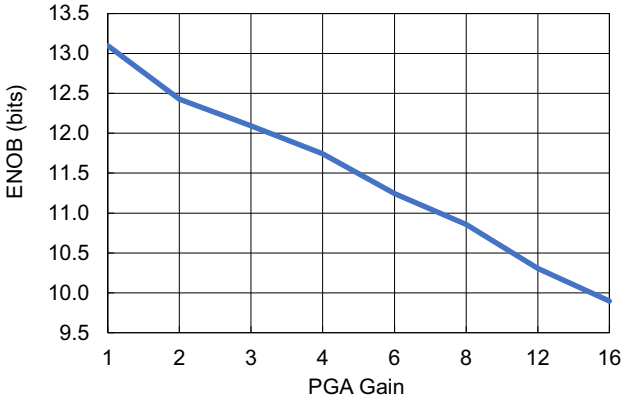


Figure 115. ENOB vs PGA Gain

Unless otherwise noted, AV_{CC} = 5.0V; DV_{CC} = 2.5V, REF = 2.5V, GND = 0V, PGA Bypassed, LPM = DV_{CC}, f_{SAMP} = 684.932ksps, F_{IN} = 20.3kHz, A_{IN} = -7dBFS, CH(0:7)- connected to V_{REF}/2; T_A = 25°C.

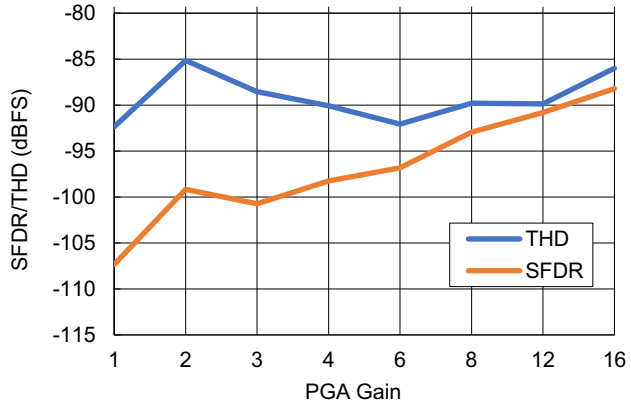


Figure 116. THD and SFDR vs PGA Gain

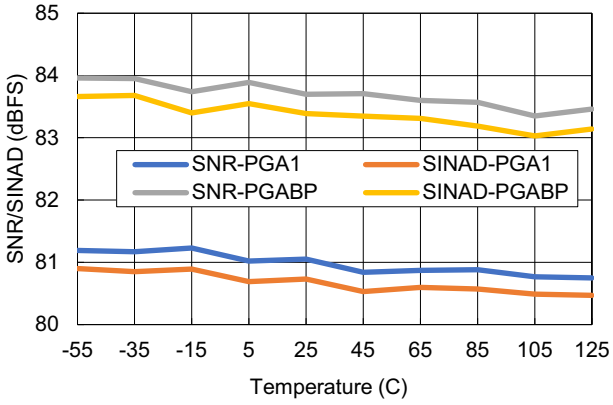


Figure 117. SNR and SINAD vs Temperature

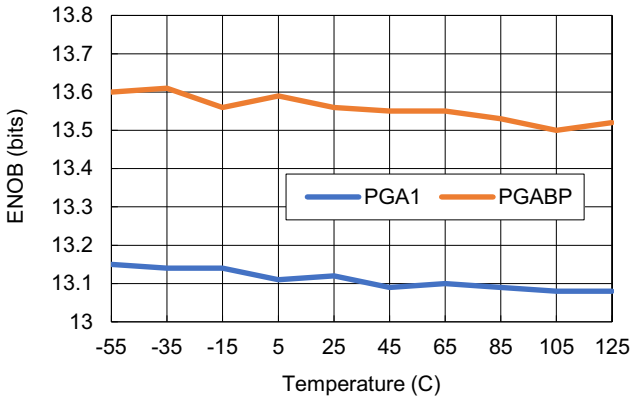


Figure 118. ENOB vs Temperature

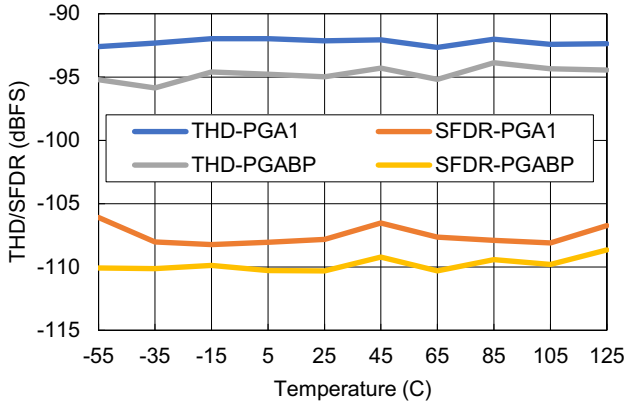


Figure 119. THD and SFDR vs Temperature

5. Applications Information

5.1 Overview

The ISL71148SLH is a high precision, low noise, 8-channel 14-bit Successive Approximation Register (SAR) ADC. The ADC core is preceded by eight independently buffered differential analog input channels, an 8-to-1 multiplexer, and a Programmable Gain Amplifier (PGA). The PGA features a bypass mode and 8-pin selectable gain settings: 1, 2, 3, 4, 6, 8, 12, and 16. Both channel and gain selection are controlled using pin-driven digital inputs.

The device operates with a fully differential analog input. The ISL71148SLH has a supply voltage range of 4.5V to 5.5V, a digital supply voltage range of 2.2V to 3.6V, and a dedicated reference input (REF). Each analog input ranges from 0V to V_{REF} with a common mode of V_{REF}/2.

The ISL71148SLH supports sample rates up to 900ksps with the PGA bypassed and up to approximately 480ksps with the PGA enabled, allowing system optimization based on the type of analog signal sampled. The ISL71148SLH with the PGA bypassed achieves excellent dynamic performance (83.2 dB SNR, 95dB THD) and linearity (INL ±0.4LSB, DNL ±0.2 LSB) while still maintaining a low power consumption of 101mW. A low-power mode is available that reduces the power consumption of the ISL71148SLH by approximately 20% at maximum sampling rates. Additionally, the device offers a sleep mode that minimizes power consumption to <115µW during idle operation.

The ISL71148SLH offers a high-speed serial interface with an independent digital supply (DV_{CC}) range of 2.2V to 3.6V, making it ideal for interfacing with 2.5V or 3.3V systems. The conversion data is output on the SDO pin with no latency. The ISL71148SLH supports up to a 50MHz serial data read clock on the SCK input.

The analog input voltage (A_{IN}) is sampled from the selected input channel on the falling edge of $\overline{CS}$. The REF pin voltage and the PGA gain setting determine the input range of the ISL71148SLH. The ISL71148SLH supports excellent THD and SFDR sampling input signal frequencies up to and beyond Nyquist (such as $f_{IN} \geq 450kHz$ with $f_{SAMP} = 900ksps$).

5.2 Serial Interface and BUSY

The ISL71148SLH uses a 3-wire serial port interface to communicate with microcontrollers and external circuitry devices. A falling edge on $\overline{CS}$ initiates conversion in the ISL71148SLH. Renesas requires holding $\overline{CS}$ high for at least 150ns before initiating the conversion in normal operation and at least 500ns when operating in lower power mode. An internal oscillator times the conversion. During the conversion process, the BUSY signal is asserted high. When the conversion is complete, BUSY is de-asserted. Renesas requires holding SCK low during t_{CONV}. The MSB is immediately available on the SDO pin when BUSY is de-asserted. Each subsequent rising edge of SCK serially outputs data on SDO from the MSB-1 to the LSB. The input logic level of $\overline{CS}$ and SCK is determined by the DV_{CC} supply voltage that operates across a range of 2.2V up to 3.6V. Similarly, the output voltage level of BUSY is also determined by the DV_{CC} supply voltage.

5.3 Operational Phases and Timing

The conversion results in MSB being available for serial readout at the SDO pin immediately following a completed conversion. The BUSY indicator flag is high during conversion and transitions low following completion of the conversion. When the BUSY indicator flag goes LOW after a conversion, the MSB of the conversion result (B13) is immediately available at the SDO pin. Subsequent rising edges of SCK shift bits MSB-1 (B12) through the LSB (B0) to SDO for readout. Optionally, the channel and gain selection for the current sample can be clocked out on the SDO pin after the LSB of the ADC data, which requires up to six additional rising edges of SCK. The channel and gain selection bits are clocked out in order from MSB to LSB, with the channel select bits output first (S2, S1, S0) and the gain bits output last (G2, G1, G0). If less than six rising edges of SCK are provided after the 14 rising edges for the ADC data, the ISL71148SLH outputs only the amount of channel and gain bits equal to the number of rising edges of SCK provided. For example, if three rising edges of SCK are provided after the 14 rising edges for the ADC data, the ISL71148SLH only outputs the channel selection bits S2, S1, and S0; the gain selection bits are not output on SDO in this case. The output voltage level of SDO is determined by the DV_{CC} supply voltage, which can operate across a range of 2.2V to 3.6V.

The ISL71148SLH can be configured to operate in normal operation or low power mode. The operational timing of the device changes between these two modes. In both modes, the channel and gain selection bits can optionally be clocked out with the ADC data after each sample word. If these bits are also clocked out, the sample period of the ISL71148SLH must be extended to accommodate the clocking of the additional bits.

The following are the three operation phases in the ISL71148SLH that are shown in Figure 120 and Figure 121.

- Acquisition
- Conversion
- Readout

The Acquisition phase begins immediately following the completion of the conversion. During $\overline{CS}$ high, the SDO pin is held in high impedance (high-Z). The falling edge of $\overline{CS}$ defines the sampling instant of the ISL71148SLH, initiates a conversion, and enables the SDO output to a low state. The conversion cycle is internally timed through an internal oscillator and takes a maximum time of t_{CONV} to complete. Following conversion, several internal blocks are powered down to reduce power consumption. This phase of power-down is referred to as NAP mode. The ISL71148SLH stays in NAP mode until the next rising edge of $\overline{CS}$, where the ISL71148SLH is fully powered up.

The first sample output in normal mode immediately after supplying power to the device or exiting power-down mode is invalid. This is due to power reduction methods that place portions of the internal circuitry of the ISL71148SLH into sleep mode and the short duration of the $\overline{CS}$ pulse in normal mode. When a $\overline{CS}$ pulse is applied to the device, these portions of the internal circuitry are powered up, and a valid sample can be acquired on the falling edge of the next subsequent $\overline{CS}$ pulse. If it is important for the first sample after power-up to be valid, operate the ISL71148SLH in low-power mode.

5.3.1 Normal Operation Mode Timing

Figure 120 shows the basic timing of the ISL71148SLH in a conversion cycle during normal operation.

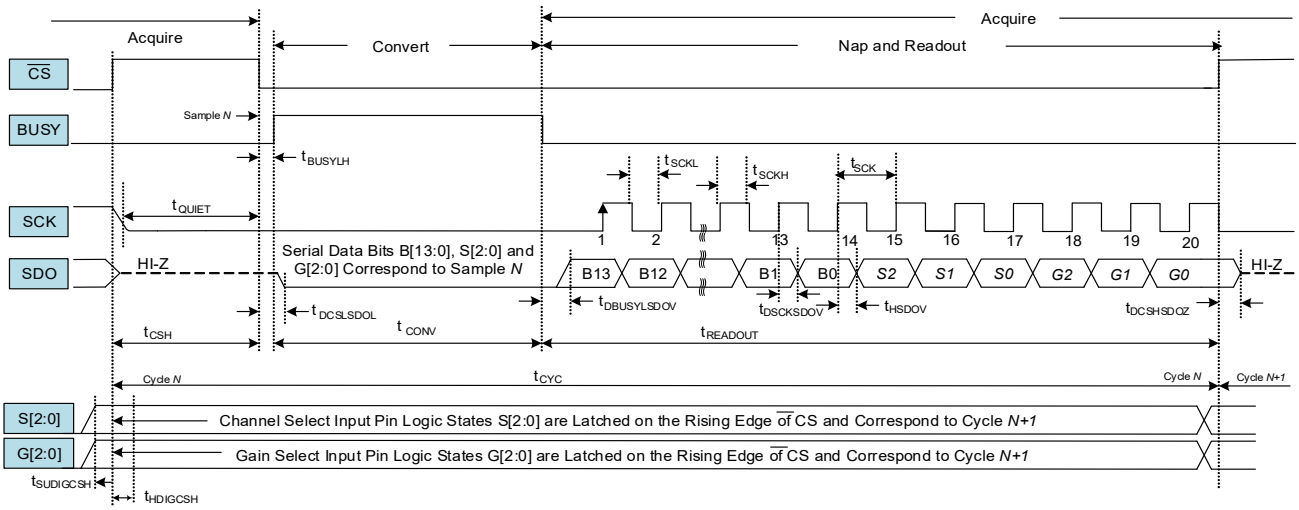


Figure 120. Timing Diagram - Normal Operation

When deriving timing, using the appropriate maximum and minimum specifications is imperative. The following is an example of timing calculation in an application operating the ISL71148SLH at 483.092ksps for the case where the channel and gain select bits are not clocked out on SDO with the ADC data and the ISL71148SLH is configured in normal operation with the PGA enabled. The $\overline{CS}$ input must be held high for 150ns (t_{CSH}). The time between the falling edge of $\overline{CS}$ and the rising edge of BUSY is a maximum of 100ns (t_{BUSYLH}) with the PGA enabled and 30ns with the PGA bypassed. The conversion time (t_{CONV}) is a maximum of 1550ns. There must be 14 rising edges of SCK ($t_{READOUT}$) to clock the data out of the ADC. The 14th SCK falling edge must coincide with the rising edge of $\overline{CS}$ for the subsequent sample to achieve the maximum sample rate. Using the maximum SCK frequency of 50MHz yields a readout time of:

$$t_{READOUT} = 13 \times 20ns + 10ns = 270ns$$

Note: The 14th SCK edge is coincident with the rising edge of $\overline{CS}$ so there is only a 1/2 period for the 14th SCK. Use Equation 1 to calculate the cycle time.

(EQ. 1) $$t_{CYC} = t_{CSH} + t_{BUSYLH} + t_{CONV} + t_{READOUT}$$

Using the timing parameters previously discussed, use Equation 2 to calculate the sampling period and Equation 3 to calculate the sampling rate.

(EQ. 2) $$t_{CYC} = 150ns + 100ns + 1550ns + 270ns = 2070ns$$

(EQ. 3) $$f_{SAMP} = \frac{1}{2070ns} = 483.092ksps$$

When the channel and gain selection bits are clocked out on SDO along with the data, additional time must be allotted, reducing the sample rate of the ISL71148SLH. The six bits require an additional 6 SCK clock cycles read on SDO. In this case, the 20th SCK falling edge must coincide with the rising edge of $\overline{CS}$ for the subsequent sample. Using the maximum SCK frequency of 50MHz yields a readout time of:

$$t_{READOUT} = 19 \times 20ns + 10ns = 390ns$$

Reduce the sample rate of the ISL71148SLH to accommodate the additional 120ns required to clock out the six additional bits for channel and gain information. Increase the sample period to accommodate time for clocking out these additional bits. The minimum sample period and corresponding maximum sample rate when clocking out the channel and gain selection bits are shown in Equation 4 and Equation 5.

(EQ. 4) $$t_{CYC} = 150ns + 100ns + 1550 + 390ns = 2190ns$$

(EQ. 5) $$f_{SAMP} = \frac{1}{2190ns} = 456.621ksps$$

The PGA can be bypassed to achieve the maximum possible sample rate in normal mode. Note: In PGA bypass mode, t_{BUSYLH} = 30ns and t_{CONV} = 660ns. Use Equation 6 to calculate the timing and Equation 7 to calculate the sample rate.

(EQ. 6) $$t_{CYC} = t_{CSH} + t_{BUSYLH} + t_{CONV} + t_{READOUT} = 150ns + 30ns + 660ns + 270ns = 1110ns$$

(EQ. 7) $$f_{SAMP} = \frac{1}{1110ns} = 900.901ksps$$

Table 1 provides the minimum sample period for various configurations of PGA state and bits read out on SDO. *Note:* The channel and gain bits can consistently be clocked out with the data. If these bits are clocked out, increase the sample period to accommodate the required clock cycles. Channel bits are clocked out first, from MSB to LSB, followed by the gain bits from MSB to LSB.

Table 1. Minimum Sample Periods in Normal Mode

PGA	Channel Bits	Gain Bits	Sample Period (µs)
Disabled	No	No	1.11
Disabled	Yes	No	1.17
Enabled	No	No	2.07
Enabled	Yes	Yes	2.19

5.3.2 Low Power Mode Timing

The ISL71148SLH can also be operated in low power mode to reduce total power dissipation or to allow an accurate first sample following initial power-up or exiting power-down. When operating in lower power mode, the timing requirements differ from normal operation. In low-power mode, the $\overline{CS}$ input directly controls the acquisition time. The logic high pulse width on the $\overline{CS}$ input defines the acquisition time. The direct control of the acquisition time by $\overline{CS}$ permits significant power savings, especially at lower sampling rates where power dissipation may be less than 50% of that in normal mode. Because the pulse width of $\overline{CS}$ directly controls the acquisition time, the minimum pulse width of $\overline{CS}$ in low power mode is 500ns, which is significantly higher than the 150ns required in normal mode. Renesas recommends using the minimum $\overline{CS}$ width of 500ns for maximum power savings at low sample rates.

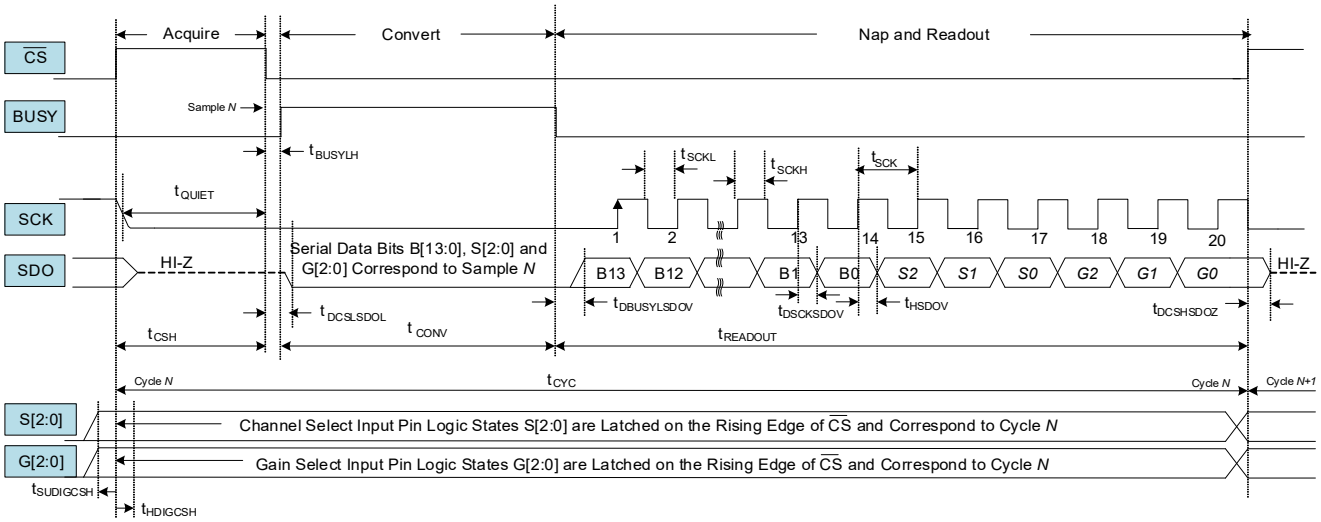


Figure 121. Timing Diagram - Low Power Mode

The following is an example of required timing calculation in an application where the ISL71148SLH is operated at its maximum sample rate of 684.932ksps in low power mode. For this case, the channel and gain select bits are not clocked out on SDO, and the ISL71148SLH is configured in low power mode with the PGA bypassed. The $\overline{CS}$ input must be held high for 500ns (t_{CSH}) in low power mode. The time between the falling edge of $\overline{CS}$ and the rising edge of BUSY is a maximum of 30ns (t_{BUSYLH}). The conversion time (t_{CONV}) is a maximum of 660ns in PGA bypass mode. There must be 14 rising edges of SCK ($t_{READOUT}$) to clock the data out of the ADC. The 14th SCK falling edge must coincide with the rising edge of $\overline{CS}$ for the subsequent sample to achieve the maximum sample rate. Using the maximum SCK frequency of 50MHz yields the same readout period in low power mode as it is in normal operation.

$$t_{READOUT} = 13 \times 20ns + 10ns = 270ns$$

Note: The 14th SCK edge coincides with the rising edge of $\overline{CS}$ so there is only a 1/2 period for the 14th SCK. Use Equation 8 to calculate the cycle time.

(EQ. 8) $$t_{CYC} = t_{CSH} + t_{BUSYLH} + t_{CONV} + t_{READOUT}$$

Using the previously discussed timing parameters, when in low power mode, use Equation 9 to calculate the sampling period and Equation 10 to calculate the sampling rate.

(EQ. 9) $$t_{CYC} = 500ns + 30ns + 660ns + 270ns = 1460ns$$

(EQ. 10) $$f_{SAMP} = \frac{1}{1460ns} = 684.932ksps$$

With the PGA enabled in low power mode, use Equation 11 to calculate the timing and Equation 12 to calculate the sample rate.

(EQ. 11) $$t_{CYC} = 500ns + 100ns + 1550ns + 270ns = 2420ns$$

(EQ. 12) $$f_{SAMP} = \frac{1}{2420ns} = 413.22ksps$$

When the ISL71148SLH has the PGA enabled, and the channel and gain selection bits are clocked out on SDO along with the data, allot additional time, reducing the sample rate. The six additional bits require six clock cycles of SCK to clock out on SDO. In this case, to achieve the maximum sample rate, the 20th SCK falling edge must coincide with the rising edge of $\overline{CS}$ for the subsequent sample. Using the maximum SCK frequency of 50MHz yields:

$$t_{READOUT} = 19 \times 20ns + 10ns = 390ns$$

Reduce the sample rate of the ISL71148SLH to accommodate the additional 180ns of readout time. With the PGA enabled when clocking out the channel and the gain selection bits, the minimum sample period is:

$$t_{CYC} = 500ns + 100ns + 1550ns + 390ns = 2540ns$$

The longer sample period of 2540ns results in a maximum sample rate of:

$$f_{SAMP} = \frac{1}{2540ns} = 393.701ksps$$

Table 2 provides the minimum sample period for various configurations of PGA state and bits read out on SDO. *Note:* The channel and gain bits can always be clocked out with the data. If these bits are clocked out, increase the sample period to accommodate the required clock cycles. Channel bits are clocked out first, from MSB to LSB, followed by the gain bits from MSB to LSB.

Table 2. Minimum Sample Periods in Low Power Mode

PGA	Channel Bits	Gain Bits	Sample Period (µs)
Disabled	No	No	1.46
Disabled	Yes	No	1.52
Enabled	No	No	2.42
Enabled	Yes	Yes	2.54

5.3.3 Gain and Channel Select Bits Timing

The logic values on the channel select pins (S2, S1, and S0) and the gain select pins (G2, G1, G0) are internally latched on the rising edge of $\overline{CS}$. In normal operation (shown in Figure 120), there is a one-sample cycle delay for both the channel and gain settings to be applied. This means the channel and gain selection bits latched into the ISL71148SLH on sample *n* are applied on sample *n + 1*. In low power mode (shown in Figure 121), the channel and gain select bits are latched on the rising edge of $\overline{CS}$ and applied to the conversion initiated on the next falling edge of $\overline{CS}$. This means that the channel and gain selection bits latched into the ISL71148SLH on sample *n* are applied on sample *n*. Although the user can update the channel and gain select signals before the setup time required before the rising edge of $\overline{CS}$, Renesas recommends not changing the signal state during the conversion process (for example, when BUSY is a logic high).

5.3.4 PGA Gain and Analog Input Range

The ISL71148SLH can operate with either the PGA bypassed or the PGA gain set to 1, 2, 3, 4, 6, 8, 12, or 16. There is a single PGA in the ISL71148SLH. Therefore, if a different gain is required for each channel, change the gain select pins before sampling the channel analog inputs. Set the common-mode voltage on the analog input to $V_{REF}/2$. Proper setup and hold times must be met.

Table 3. Analog Input Range

PGA Gain Setting	Common Mode Input Range	Input Range
PGA Bypass	1.25V ± 100mV	±2.5V
Gain = 1	1.25V ± 100mV	±2.5V
Gain = 2	1.25V ± 100mV	±1.25V
Gain = 3	1.25V ± 100mV	±833mV
Gain = 4	1.25V ± 100mV	±625mV
Gain = 6	1.25V ± 100mV	±417mV
Gain = 8	1.25V ± 100mV	±312mV
Gain = 12	1.25V ± 100mV	±208mV
Gain = 16	1.25V ± 100mV	±156mV

5.3.5 Digital Clamping and Full Scale Range

The ISL71148SLH has a digital clamp that limits the output code range so that the output code values do not roll over in either the positive (full scale) or negative (zero scale) directions. The output code range is limited to the range of 10 0000 0000 0000 (-8192) to 01 1111 1111 1111 (8191). It is impossible to see an output code greater than the expected full-scale value or smaller than the zero-scale value.

5.3.6 Input Channel Sequencer (SCAN Mode)

The ISL71148SLH features an internal sequencer which, when enabled, cycles through all eight differential channel pairs from CH0 to CH7, repeating while SCAN is asserted. The SCAN input acts as a digital gating window for the sequencing function. The initialization cycle is the first sample after SCAN is asserted in normal mode. The second sample after SCAN is asserted should be ignored. The channel sequence begins with the sampling of CH0. The sampling instant for CH0 occurs on the 2nd falling edge of $\overline{CS}$ following the rising edge of SCAN, as shown in Figure 122, which ensures a full acquisition period for the sample of the CH0 analog input. Subsequent rising edges of $\overline{CS}$ increment the sequencer to acquire the next channel (CH1, CH2,...CH7). Following CH7, the sequencer returns to CH0. The SCAN pin should be asserted for the duration of the required sequence. The gain selection (G2, G1, G0) values are clocked in on the rising edge of $\overline{CS}$ on sample *n* and applied to sample *n+1*, as shown in Figure 122. When the SCAN pin is de-asserted, the channel select inputs (S2, S1, S0) resume control of the active channel. While SCAN is asserted, the channel select inputs (S2, S1, S0) are ignored.

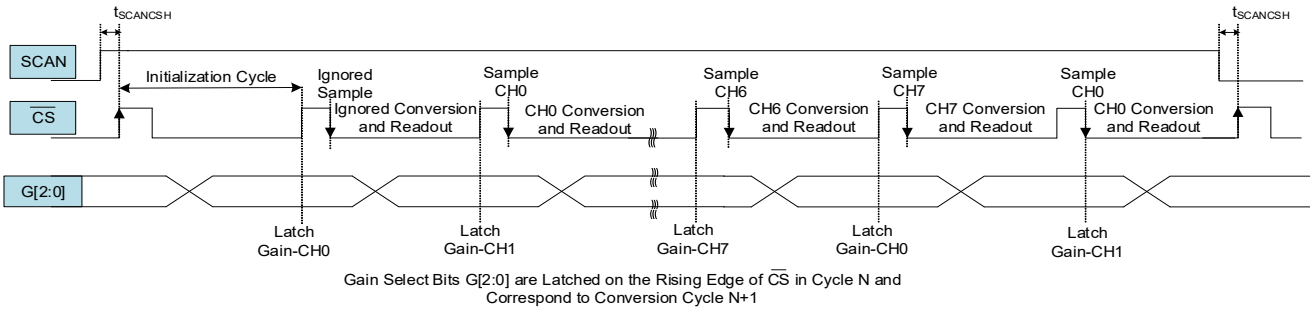


Figure 122. SCAN and Gain Select Timing Diagram - Normal Mode

When SCAN mode is selected while operating the ISL71148SLH in low power mode (LPM enabled), the sample following the first rising edge of $\overline{CS}$ where SCAN is asserted should be ignored. The sampling instant for CH0 occurs on the 2nd falling edge of $\overline{CS}$ following the rising edge of SCAN as shown in Figure 123. This ensures a full acquisition period for the sample of the CH0 analog input. Subsequent rising edges of $\overline{CS}$ increment the sequencer to acquire the next channel (such as CH0, CH1,...CH7) as shown in Figure 123. Following CH7, the

sequencer returns to CH0. The SCAN pin should be asserted for the duration of the required sequence. The gain selection (G2, G1, G0) values are clocked in on the rising edge of $\overline{CS}$ on sample *n* and applied to sample *n* as shown in Figure 123. When the SCAN pin is de-asserted, the channel select inputs (S2, S1, S0) resume control of the active channel. While SCAN is asserted, the channel select inputs (S2, S1, S0) are ignored.

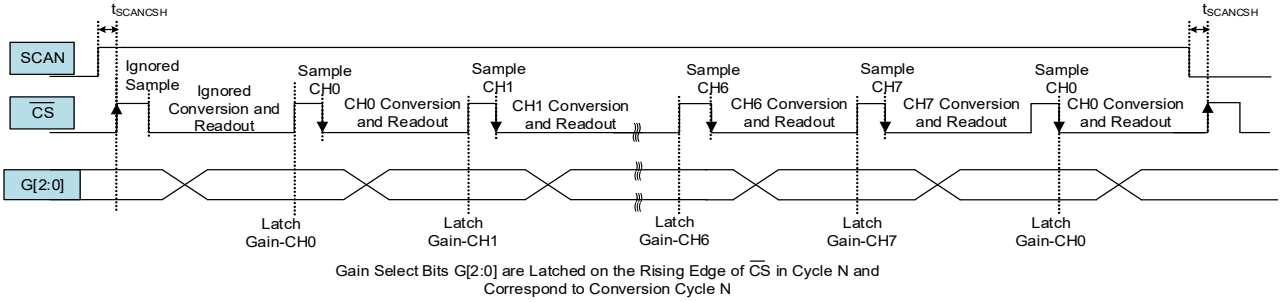


Figure 123. SCAN and Gain Select Timing Diagram - Low Power Mode

In both normal operation and low power modes of operation, the ISL71148SLH data readout on SDO in SCAN mode is performed with the same timing as given in Figure 120 and Figure 121. The active channel and gain settings for the conversion can still be optionally read out following the LSB (adjusting the sample rate period accordingly). In SCAN mode, the active channel bits correspond to the sequencer-selected channel and not the channel input pin states (S2, S1, and S0). Gain can be adjusted when operating in SCAN mode as long as specified setup and hold times are obeyed. Gain settings are applied to the current sample in lower power mode and are applied one cycle later in normal operation mode as shown in Figure 122 and Figure 123. When SCAN is de-asserted, the sample at the subsequent rising edge of $\overline{CS}$ is from the last channel selected by the sequencer. For example, if SCAN is de-asserted when the sequencer selects CH1, the next sample is CH2. Following the CH2 sample, the channel select pins (S2, S1, S0) drive the output channel selection.

5.4 Convert Start ($\overline{CS}$) Pin

The convert start input ($\overline{CS}$) initiates a conversion in the ISL71148SLH. The input logic level of $\overline{CS}$ is determined by the DV_{CC} supply voltage, which operates across a range of 2.2V up to 3.6V. A falling edge on this input starts a new conversion. The conversion is timed using an internal oscillator. The logic state of the $\overline{CS}$ pin controls the state of the SDO pin. A logic high on the $\overline{CS}$ pin disables the SDO pin driver resulting in a high-impedance state on the SDO pin. A logic low on the $\overline{CS}$ pin enables the SDO driver (unless $\overline{PD}$ is low) and allows data to be read out following a conversion. Renesas recommends using a low jitter (low phase noise) source to provide the input to this pin. Exact jitter requirements depend highly on the acceptable noise in a given application. Hold this pin low at power-up and when in power-down or the device is inactive.

5.5 Power-Down ($\overline{PD}$) Pin

The ISL71148SLH has a separate power-down pin that is active low ($\overline{PD}$). Anytime the ISL71148SLH is powered up and operated statically without a required conversion (CSB held low), this pin should be asserted. When this pin is asserted, the ISL71148SLH is powered down to ≤115µW of total power dissipation. If $\overline{PD}$ is asserted during a conversion, the conversion is halted, and the SDO pin is held in high impedance (high-Z). The ISL71148SLH is brought out of power-down mode by de-asserting $\overline{PD}$. When operating the ISL71148SLH in normal mode (LPM = 0V), there is a one-sample delay before output data is valid and the channel and gain selections are applied (see Figure 120). When operating the ISL71148SLH in low power mode (LPM = DV_{CC}), the sample on the first rising edge of $\overline{CS}$ is valid, and the channel and gain selections are applied to that sample (see Figure 121). The wake-up time for the ISL71148SLH to come out of power-down and be ready to begin sampling is specified in the electrical tables as Wake-Up time from Power-Down Mode. The input logic level of $\overline{PD}$ is determined by the DV_{CC} supply voltage, which operates across a range of 2.2V up to 3.6V. There is an internal 500kΩ pull-up resistor connected to DVCC on this pin.

5.6 Reference Input (REF) Pin

The ISL71148SLH voltage reference input determines the full-scale input range. The input voltage range of this pin is from 2.4V up to 2.6V. Decouple this pin to ground with a high-quality, low ESR 10µF ceramic capacitor. Renesas recommends placing a capacitor with a voltage rating of 10V or greater as close as possible to the REF pin.

Use a low noise, low-temperature drift reference to drive this pin. Input noise from the input reference directly impacts the noise performance of the device. Temperature drift of the external reference affects the full-scale error performance over temperature for the ISL71148SLH. Exact specifications for the noise and temperature drift requirements depend heavily on the application. For example, the ISL71148SLH evaluation board uses a 2.5V voltage reference with a typical output noise voltage of $1.9\mu V_{P-P}$ and a maximum temperature coefficient of 7ppm/°C.

5.7 PGA Bypass (PGABP) Pin

The PGABP pin can be set high to enable the input coming from the buffer/multiplexer to drive the ADC directly. This mode of operation allows the highest sample rate for the ISL71148SLH. The input logic level of PGABP is determined by the DV_{CC} supply voltage, which operates across a range of 2.2V up to 3.6V. When the PGABP pin is de-asserted, the gain select inputs (G2, G1, G0) resume control of the active channel. While PGABP is asserted, the gain select inputs (G2, G1, G0) are ignored.

5.8 ±(CH0 - CH7) Input Pins

The analog input pins are independently buffered and exhibit high input impedance (1GΩ) and low input capacitance (4pF) to ease input drive requirements. Any unused input pair pins should always be terminated to ground.

The ISL71148SLH is specified and tested with a differential analog input but also supports sampling single-ended signals. *Note*: For single-ended inputs, apply a signal to the +CHx input pins while connecting the -CHx input pins to a low noise DC input voltage equal to VREF/2 or connected directly to GND. See Single-Ended Operation for more details. The ISL71148SLH evaluation board can be used as a guide for proper circuit optimization. Due to the high bandwidth (50MHz) of the analog input, Renesas recommends using an Anti-Alias Filter (AAF) appropriate for the required application. Operating the ISL71148SLH with an input amplifier is not required because the device has an integrated PGA. Still, it can ease input common mode biasing and/or provide additional gain in certain applications. An example topology is given in Figure 124, which uses a driver amplifier and an RC input filter. Care must be taken when choosing an amplifier with low noise and distortion because the ADC performance is directly impacted. ***IMPORTANT****:* Choose feedback resistance values that are less than 1kΩ (typically, 100Ω to 200Ω) to minimize the impact of resistor thermal noise. The noise of the resistor is directly related to its value by Equation 13, where k is the Boltzmann constant (1.38×10^{-23} J/K), T is the temperature in Kelvin (room temperature = 27°C = 300K), and R is the resistance value (Ω).

(EQ. 13) $\text{Power Spectral Density (PSD)} = 4kTR\ (V^2/Hz)$

At the input to the ADC, a simple RC filter should be sufficient for most applications. Choose the RC circuit values appropriately for the application. A low-value resistor ($R_S \leq 50\ \Omega$) is recommended for low noise performance. Add a high-quality shunt capacitor (C_P) as close as possible to each differential channel input pin to limit the input bandwidth to the ISL71148SLH. This capacitor should have a low ESR value with a low temperature and voltage coefficient. The exact requirements depend highly on the application and the sampled signal(s). The recommended value for the C_P is 20-50pF. Larger values for C_P can be used for slower conversion rates.

Note: Large values of shunt capacitance are not required to squelch charge kickback from the multiplexer or the ADC because each analog input is independently buffered.

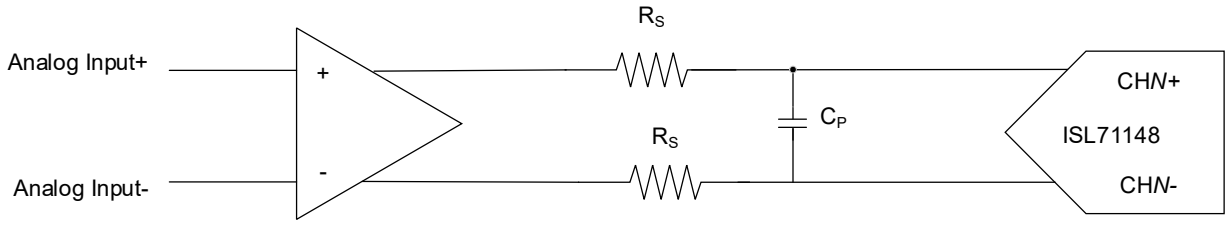


Figure 124. Analog Input Amplifier Example Circuit

Renesas recommends using a high-quality ceramic capacitor (C_P) in shunt on the analog input that is at an appropriate value for the required application. Choose the series resistance in the analog input circuit based on the output impedance of the driver amplifier and the input bandwidth requirements. An example topology is given in Figure 125, which converts a 0V input common-mode voltage to the ADC input common-mode voltage of $V_{REF}/2$. This circuit is employed on the ISL71148SLH evaluation board to allow the ADC to be driven from various types of signal generators.

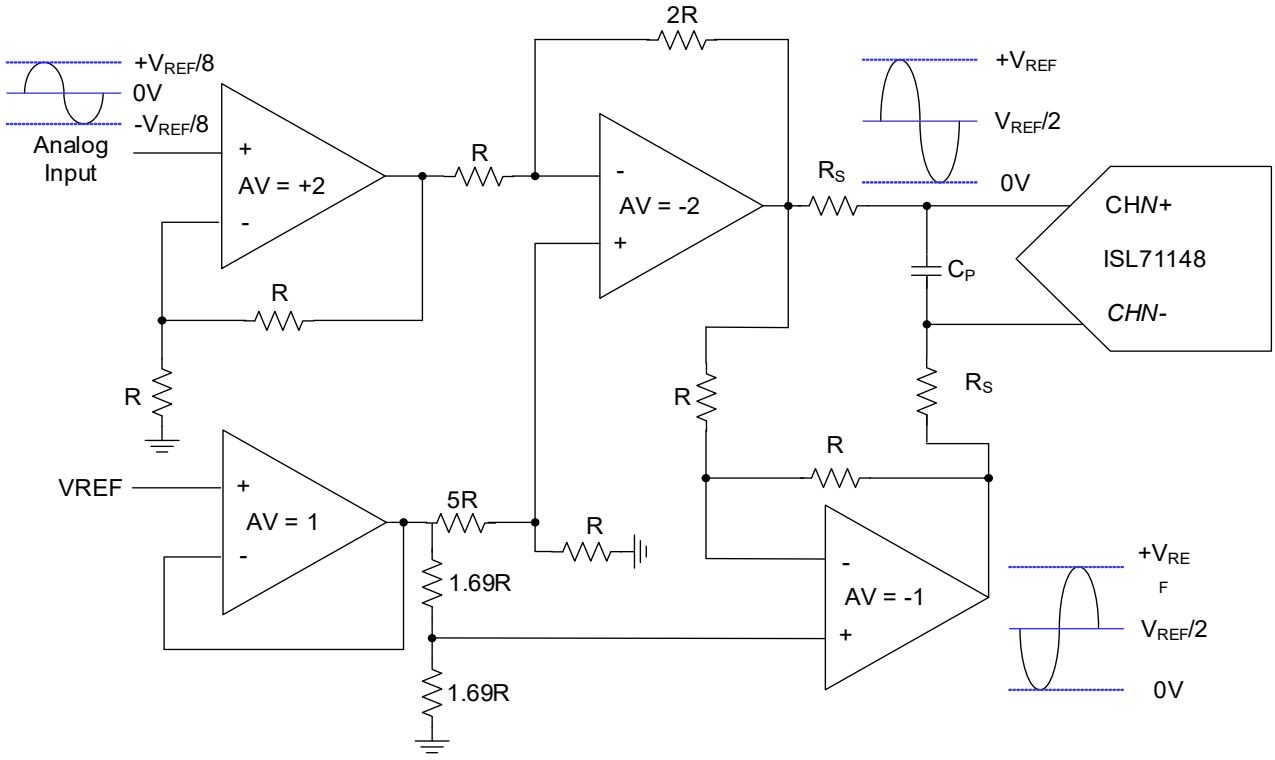


Figure 125. Common-Mode Conversion Amplifier Example Circuit

5.9 Low Power Mode (LPM) Pin

The ISL71148SLH has a low power mode (LPM) pin that can be asserted high to enable the device to operate in a mode with significantly lower power dissipation, especially at lower sample rates. Low power mode also offers accurate sampling immediately following initial power-up or exiting from power-down mode. The input logic level of LPM is determined by the DV_{CC} supply voltage, which operates across a range of 2.2V up to 3.6V. There is an internal 500kΩ pull-down resistor connected to GND on this pin.

5.10 SCAN Pin

The ISL71148SLH has a SCAN pin that enables an internal sequencer to control the channel selection. When the SCAN pin is asserted high, the sequencer is enabled, and the device sequences through the eight input channels

beginning on the next rising edge of $\overline{CS}$. The channel selection begins with CH0 and consecutively selects through all eight channels up to CH7 on each subsequent rising edge of $\overline{CS}$. As long as SCAN is asserted high, the ISL71148SLH continues to sequence through the eight input channel pairs consecutively from CH0 to CH7 on each rising edge of $\overline{CS}$. While SCAN is asserted, the channel selection pins (S2, S1, and S0) are ignored. The input logic level of LPM is determined by the DV_{CC} supply voltage, which operates across a range of 2.2V up to 3.6V.

5.11 Channel Selection (S2, S1, and S0) Pins

The ISL71148SLH has three channel selection input pins: S2, S1, and S0. These three pins determine which of the analog input channels, ±CH0 to ±CH7, are selected. If the SCAN pin is asserted, the channel selection input pins are ignored. The channel selection is determined by the logic states of pins S2, S1, and S0 and is given in Table 4. The input logic level of LPM is determined by the DV_{CC} supply voltage, which operates across a range of 2.2V up to 3.6V. These inputs are ignored when the SCAN pin is asserted.

Table 4. Channel Selection Logic (S2, S1, S0)

S2	S1	S0	Channel
0	0	0	CH0+,CH0-
0	0	1	CH1+,CH1-
0	1	0	CH2+,CH2-
0	1	1	CH3+,CH3-
1	0	0	CH4+,CH4-
1	0	1	CH5+,CH5-
1	1	0	CH6+,CH6-
1	1	1	CH7+,CH7-

5.12 Gain Selection (G2, G1, and G0) Pins

The ISL71148SLH has three gain selection input pins: G2, G1, and G0. These three pins determine the gain setting of the PGA. The gain selection of the PGA is determined by the logic states of pins G2, G1, and G0, which are shown in Table 5. The PGABP pin is of higher priority than G2, G1, and G0. The gain can be adjusted dynamically during operation so long as setup and hold times are met with or without the sequencer being enabled (sequencer is enabled when SCAN is asserted to a logic high). The input logic level of these pins is determined by the DV_{CC} supply voltage, which operates across a range of 2.2V up to 3.6V.

Table 5. Gain Selection Logic (G2, G1, G0)

PGABP	G2	G1	G0	Gain
1	X	X	X	1
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
0	0	1	1	4
0	1	0	0	6
0	1	0	1	8
0	1	1	0	12
0	1	1	1	16

5.13 Transfer Function

Figure 126 gives the transfer function of the ISL71148SLH when operating with differential input channels. Code transitions in the digital output bits of the device occur at midway points between successive integer LSB values that range from 0.5 LSB, 1.5 LSB, 2.5 LSB, 3.5 LSB... and FS - 3.5 LSB, FS - 2.5 LSB, FS - 1.5 LSB, FS - 0.5 LSB.

The output data is in two's complement format. The device operates as a 14-bit ADC with an output code range in two's complement from -2^{N-1} to $2^{N-1}-1$ where N = 14, making the total code range -8192 to 8191 inclusive.

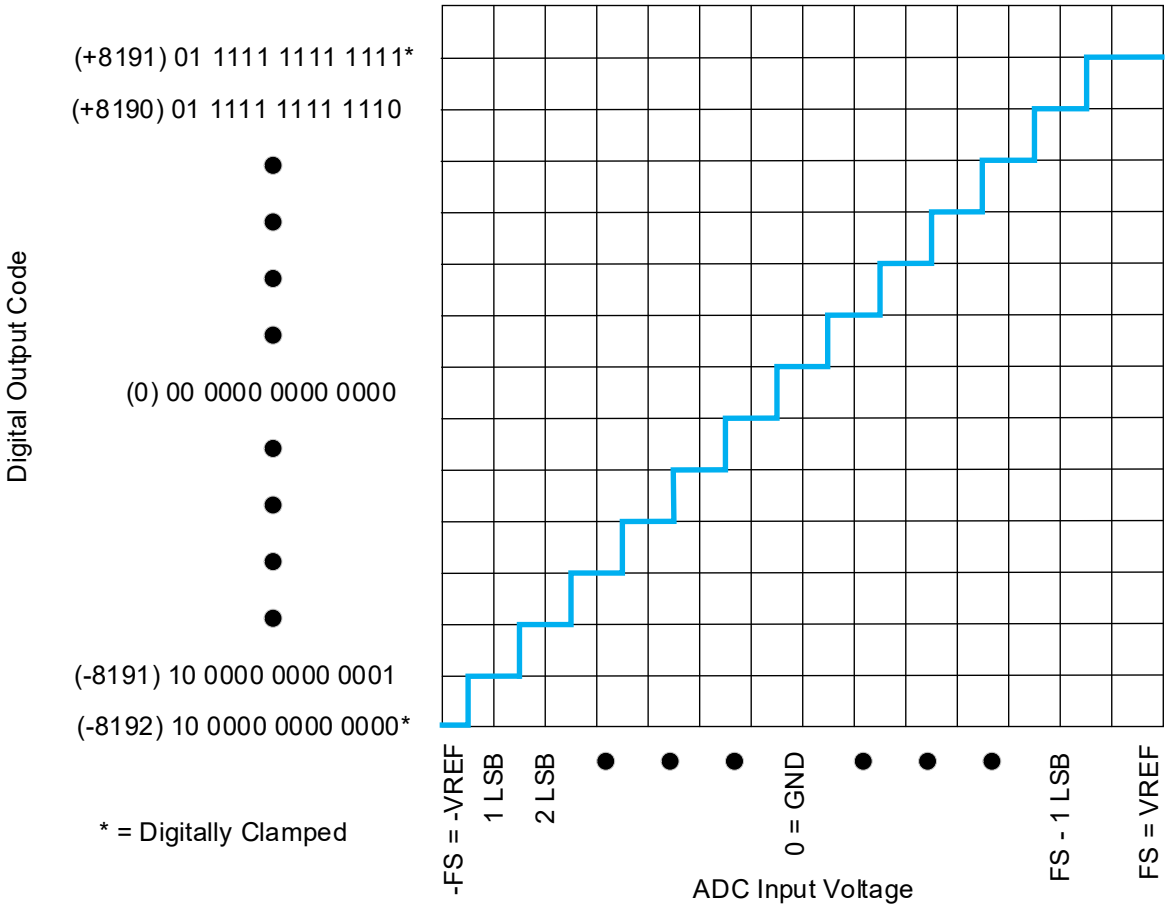


Figure 126. Transfer Function - Differential Input Channels

Figure 127 shows the transfer function for the ISL71148SLH when operating with a single ended input configuration in bipolar mode and in unipolar mode.

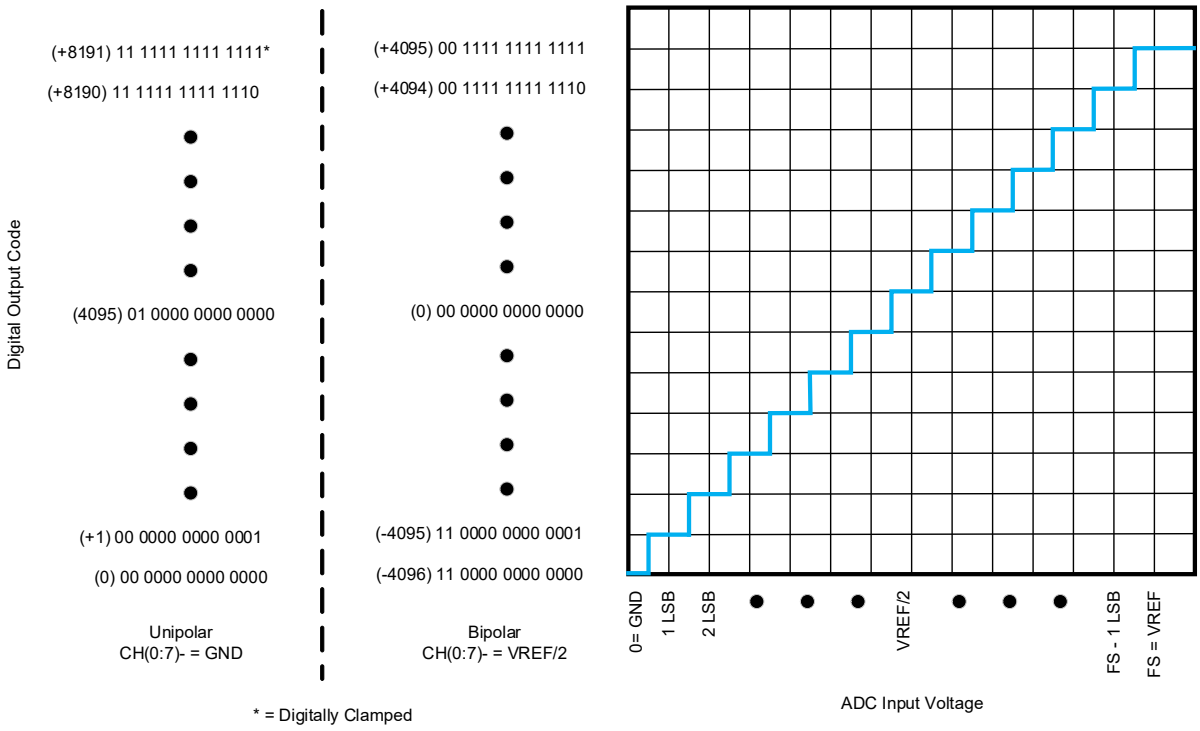


Figure 127. Transfer Function – Single Ended Input Channels – PGA Bypassed or PGA Gain = 1

When the negative channel inputs are connected to ground, the device operates in unipolar mode. The device operates effectively as a 13-bit ADC with an output code range in decimal from 0 to 2^N-1 where N = 13, making the total code range 0 to 8191 inclusive.

The negative channels inputs can also have a low-impedance connection to a $V_{REF}/2$ to operate the device in bipolar mode. In this case, the output code range in two's complement from $-2^{(N-1)}$ to $2^{(N-1)}$-1 where N = 13, making the total code range -4096 to 4095 inclusive. As seen in Figure 128, with the PGA gain set to a value of 2 or greater, the device operates as a 14-bit ADC with an output code range in two's complement from $-2^{(N-1)}$ to $2^{(N-1)}$-1 where N = 14, making the total code range -8192 to 8191 inclusive.

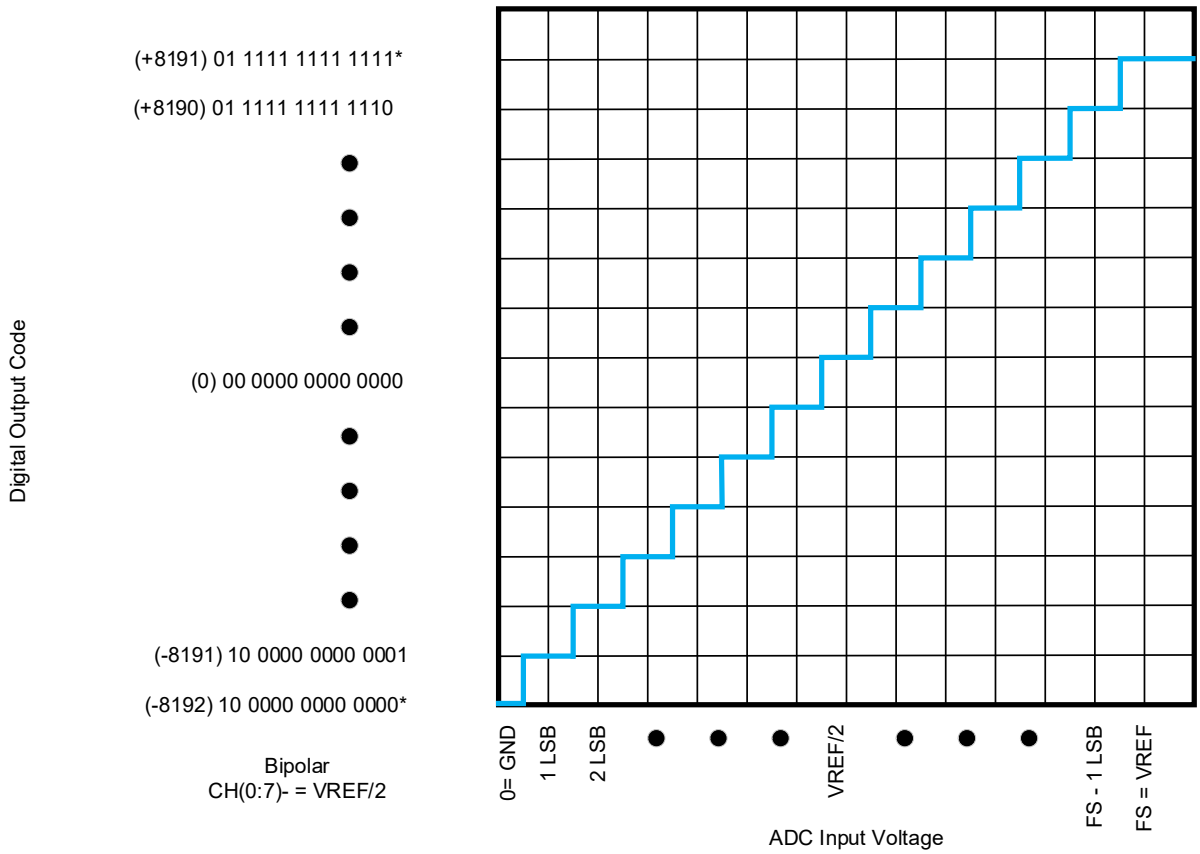


Figure 128. Transfer Function – Single Ended Input Channels – Bipolar (Gain ≥ 2) Operation

5.14 Power Supply Sequencing

The ISL71148SLH does not have any specific power sequencing requirements. ***Important:*** Follow the guidelines in the recommended operating conditions and observe the maximum supply voltage conditions outlined in the Absolute Maximum Ratings section.

5.15 Cold Sparing Operation

The ISL71148SLH can be used in applications requiring connections to multiple input devices with only one active at a given time, commonly called cold sparing. The analog input of the ISL71148SLH connects to an 8-channel multiplexer with high-impedance inputs. Select only one channel at a given time for sampling. In many cold-sparing applications, the unused devices connected to the unused channels are completely powered down with the supply voltage removed. However, for the ISL71148SLH, any device connected to one of the eight analog inputs should be provided a supply voltage but can be placed into power-down mode using the $\overline{PD}$ pin of the individual devices.

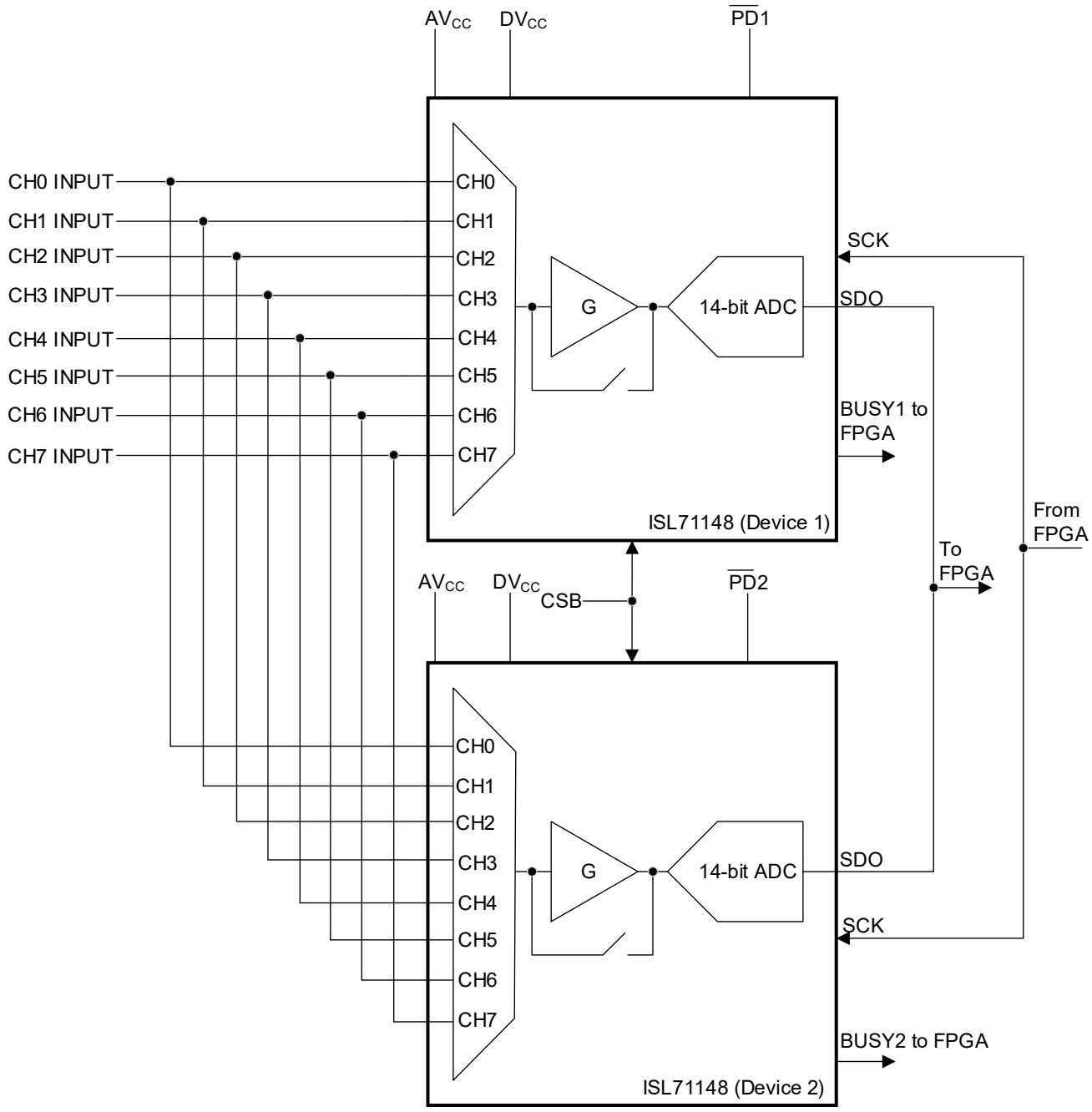


Figure 129. Cold Sparing Example Circuit

5.16 Configuration Examples

The ISL71148SLH can be used in various applications that require the device to be set up in a particular configuration. There are several ways to configure the ISL71148SLH to provide the best performance for a given application. A key configuration parameter for the ISL71148SLH is the data format. *Note:* In the following examples shown in sections Normal Mode, PGA Gain through Single-Ended Operation, an arbitrary channel is chosen. However, any channel can be used, or the ISL71148SLH can be placed in SCAN mode, where all eight channels are selected sequentially in a repeating mode. See Input Channel Sequencer (SCAN Mode) for more details on SCAN mode.

5.16.1 Normal Mode, PGA Gain

In applications that require amplification of an input and a higher sample rate from the ADC, the ISL71148SLH can be configured into normal mode, setting the PGA gain to a value of any gain. This feature allows the user to amplify the input signal to use the full input range of the ISL71148SLH for best signal-to-noise performance when a small signal is sampled. For example, to select this operating with a PGA gain of 2 using Channel 1, the pin configuration should be set as shown in Table 6.

Table 6. Pin Configuration - PGA Gain of 2 using Channel 1

S2	S1	S0	PGABP	G2	G1	G0	LPM
0	0	1	0	0	0	1	0

5.16.2 Normal Mode, PGA Bypassed

In applications that require the highest sample rate from the ADC, the user can configure the ISL71148SLH into normal mode with the PGA bypassed. There is no input amplification in this case, but the ADC can operate at its highest possible sample rate. An input signal can still be applied to one of the eight channels with a voltage up to the full input range. For example, to select this operating mode with the PGA bypassed using Channel 4 of the ISL71148SLH, set the pin configuration as shown in Table 7.

Table 7. Pin Configuration - PGA bypassed using Channel 4

S2	S1	S0	PGABP	G2	G1	G0	LPM
1	0	0	1	X	X	X	0

5.16.3 Low Power Mode, PGA Enabled

In applications that require lower power consumption and where a lower sample rate is sufficient, the ISL71148SLH can be configured into low-power mode. This gives the user the ability to amplify the input signal to use the full range of the ISL71148SLH for best signal-to-noise performance when a small signal is sampled. Although the sample rate is only slightly reduced in low power mode, the power consumption is significantly reduced, especially for lower sample rates. For example, to select this operating mode with a PGA gain of 4 using Channel 1 of the ISL71148SLH, set the pin configuration as shown in Table 8.

Table 8. Pin Configuration - PGA Gain of 4 using Channel 1

S2	S1	S0	PGABP	G2	G1	G0	LPM
0	0	1	0	0	1	1	1

5.16.4 Low Power Mode, PGA Bypassed

In applications that require lower power consumption where a lower sample rate is sufficient and no input amplification is necessary, the ISL71148SLH can be configured into low-power mode with the PGA bypassed. The sample rate is only slightly reduced compared to normal mode with the PGA bypassed, and the power consumption is significantly reduced. For example, to select this operating mode using Channel 5 of the ISL71148SLH, set the pin configuration as shown in Table 9.

Table 9. Pin Configuration - PGA bypassed using Channel 5

S2	S1	S0	PGABP	G2	G1	G0	LPM
1	0	1	1	X	X	X	1

5.16.5 Single-Ended Operation

The ISL71148SLH can be configured for applications that require single-ended inputs. To implement this operating mode, apply the full input range (0V - 2.5V) to the positive channel input and apply $V_{REF}/2$ or ground to the negative channel input as shown in Figure 130.

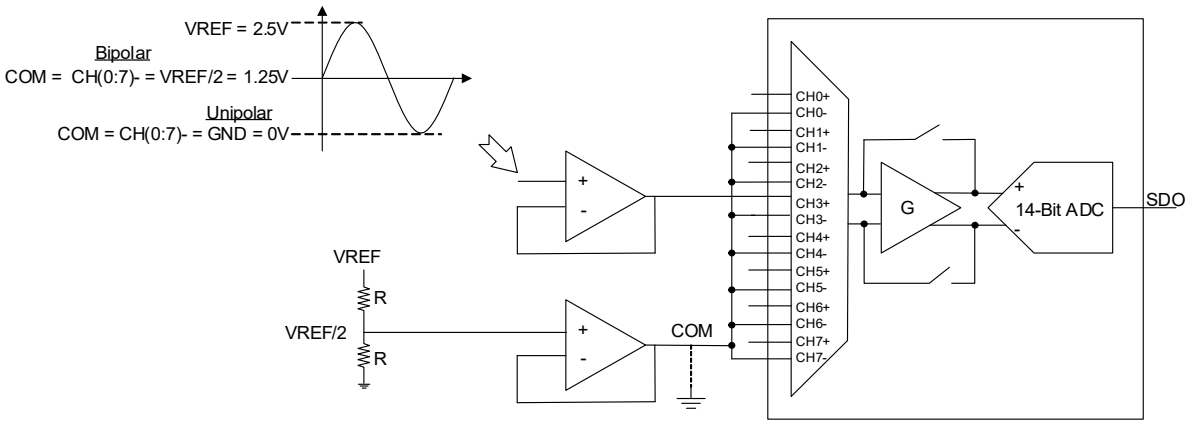


Figure 130. Single-Ended Application Schematic

The negative channel inputs should have a low-impedance connection to a $V_{REF}/2$ plane on the circuit board layout to operate the device in bipolar mode. $V_{REF}/2$ can be obtained from V_{REF} using a precision resistor divider network but should be buffered before driving the negative input channel. The output code range for a bipolar mode configuration would be from -2^{N-2} to $2^{N-2}-1$, where N = 14, making the total code range from -4096 to 4095. The full output range of the ADC can be exercised by configuring the PGA to a gain of 2 or more.

The negative channel inputs should have a ground connection to operate the device in unipolar mode. This unipolar configuration exercises an output code range from 0 to $2^{N-1}-1$, where N = 14, making the total code range from 0 to 8191. When running the device in unipolar mode, the analog input to the positive channel should be adjusted depending on the PGA gain applied, as shown in Table 10.

Table 10. Single-Ended Analog Input Range

PGA Gain Setting	Common Mode	Input Range
PGA Bypass	1.25V	0V to 2.5V
Gain = 1	1.25V	0V to 2.5V
Gain = 2	625mV	0V to 1.25V
Gain = 3	416.7mV	0V to 833mV
Gain = 4	312.5mV	0V to 625mV
Gain = 6	208.5mV	0V to 417mV
Gain = 8	156mV	0V to 312mV
Gain = 12	104mV	0V to 208mV
Gain = 16	78mV	0V to 156mV

5.16.6 Dual Footprint ISL73148SEH/ISL71148SLH

The ISL71148SLH can be configured inside an ISL73148SEH footprint. Figure 131 shows a connection diagram to configure the ISL71148SLH in a single-ended operation. The negative input channels can be connected to low-impedance VREF/2 or ground planes (see Single-Ended Operation). Moreover, a PGA Bypass pin is added to the footprint because it is a dual-purpose pin in the ISL73148SEH.

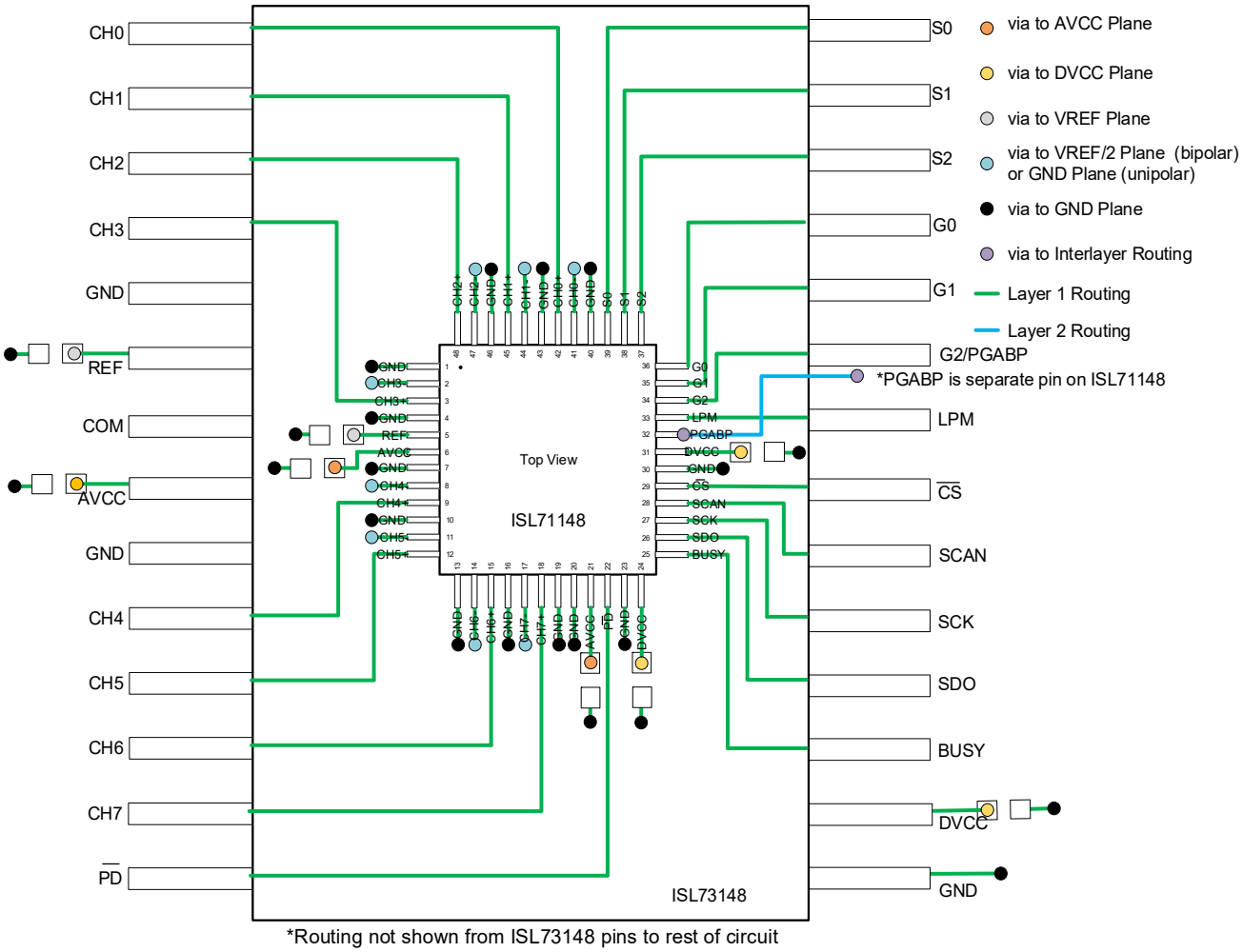


Figure 131. Dual Footprint ISL73148/ISL71148

6. Die and Assembly Characteristics

Table 11. Die and Assembly Related Information

Die Information	
Dimensions	4495µm×4495µm (177 mils×177 mils) Thickness: 292µm (11.5 mils)
Interface Materials	
Passivation	Oxide/Nitride Total Thickness 24.5kA with 5µm of Polyimide
Top Metallization	Top metal/Bond Pad Composition 99.5% Al, 0.5%Cu
Process	0.25µm CMOS
Assembly Information	

Table 11. Die and Assembly Related Information

Substrate Potential	GND
Additional Information	
Transistor Count	142139
Weight of Packaged Device	0.178 grams (typical) - Q48.7×7package

7. Package Outline Drawing

The package outline drawing is located at the end of this document and is accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

8. Ordering Information

Part Number[1][2]	Part Marking	Radiation Hardness (Total Ionizing Dose)	Package Description[3] (RoHS Compliant)	Pkg. Dwg #	Carrier Type	Temp. Range
ISL71148SLHMNZ	ISL71148 SLHMNZ	LDR to 75krad(Si)	48 Ld TQFP	Q48.7x7	Tray	-55 to +125°C

1. These Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu-Ag plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. For Moisture Sensitivity Level (MSL), see the ISL71148SLH product page. For more information about MSL, see TB363.
3. For the Pb-Free Reflow Profile, see TB493.

9. Revision History

Revision	Date	Description
1.04	Feb 18, 2025	Added SCAN to the list of pins in the I/O Specifications table for the first subheading and Input Current parameter. Updated Transfer Function section. Updated Single-Ended Operation section. Updated POD Q48.7x7 to the latest revision; changes are as follows: ▪ Placed POD into the latest template Added ECAD Information.
1.03	Dec 11, 2024	Updated feature bullet.
1.02	Nov 18, 2024	Added Outgas Testing section.
1.01	Sep 30, 2024	Updated Circuit 2 drawing. Updated Channel Voltage Abs Max spec. Added CH0:7+, CH0:7- Input Current Abs max spec. Updated the Cold Sparing Example Circuit figure. Updated ±(CH0 - CH7) Input Pins section. Updated Single-Ended Operation section.
1.00	Jul 12, 2024	Initial release

A. ECAD Design Information

This information supports the development of the PCB ECAD model for this device. It is intended to be used by PCB designers.

A.1 Part Number Indexing

Orderable Part Number	Number of Pins	Package Type	Package Code/POD Number
ISL71148SLHMNZ	48	QFP	Q48.7x7

A.2 Symbol Pin Information

A.2.1 48-QFP

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
1	GND	Power	-
2	CH3-	Input	-
3	CH3+	Input	-
4	GND	Power	-
5	REF	Power	-
6	AVCC	Power	-
7	GND	Power	-
8	CH4-	Input	-
9	CH4+	Input	-
10	GND	Power	-
11	CH5-	Input	-
12	CH5+	Input	-
13	GND	Power	-
14	CH6-	Input	-
15	CH6+	Input	-
16	GND	Power	-
17	CH7-	Input	-
18	CH7+	Input	-
19	GND	Power	-
20	GND	Power	-
21	AVCC	Power	-
22	$\overline{PD}$	Input	-
23	GND	Power	-
24	DVCC	Power	-
25	BUSY	Output	-
26	SDO	Output	-
27	SCK	Input	-
28	SCAN	Input	-
29	$\overline{CS}$	Input	-
30	GND	Power	-
31	DVCC	Power	-
32	PGABP	Input	-
33	LPM	Input	-
34	G2	Input	-

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
35	G1	Input	-
36	G0	Input	-
37	S2	Input	-
38	S1	Input	-
39	S0	Input	-
40	GND	Power	-
41	CH0-	Input	-
42	CH0+	Input	-
43	GND	Power	-
44	CH1-	Input	-
45	CH1+	Input	-
46	GND	Power	-
47	CH2-	Input	-
48	CH2+	Input	-

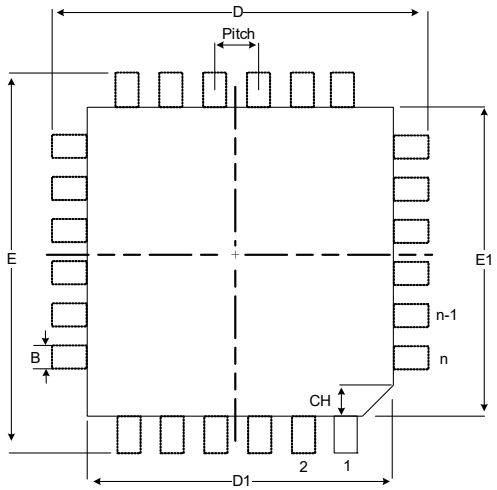
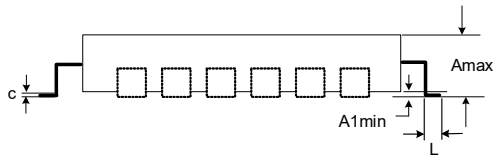
A.3 Symbol Parameters

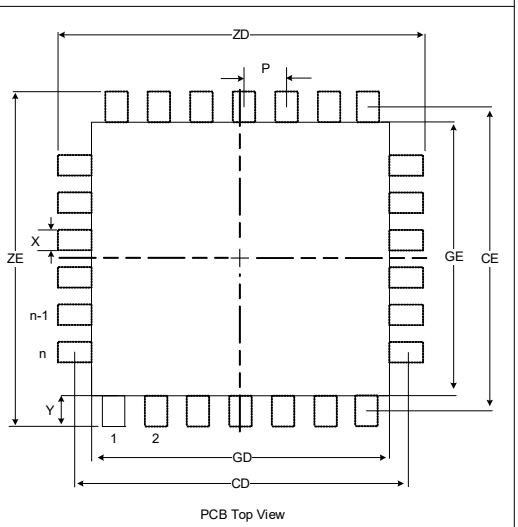
Orderable Part Number	Qualification	Radiation Qualification	LDR	Mounting Type	Min Operating Temperature	Max Operating Temperature	RoHS	Differential Nonlinearity (DNL)	Number of Bits	Integral Nonlinearity (INL)	Min Reference Input Voltage	Max Reference Input Voltage	Min Analog Supply Voltage	Max Analog Supply Voltage	Min Digital Supply Voltage	Max Digital Supply Voltage	Number of Channels	Sampling Rate	Signal to Noise Ratio (SNR)
ISL71148SLHMNZ	Space	QML Class P Equiv.	75 krad(Si)	SMD	-55 °C	125 °C	Compliant	±0.2 LSB	14	±0.4 LSB	2.4 V	2.6 V	4.5 V	5.5 V	2.2 V	3.6 V	8	900 ksps	83.2 dBFS

A.4 Footprint Design Information

A.4.1 48-QFP

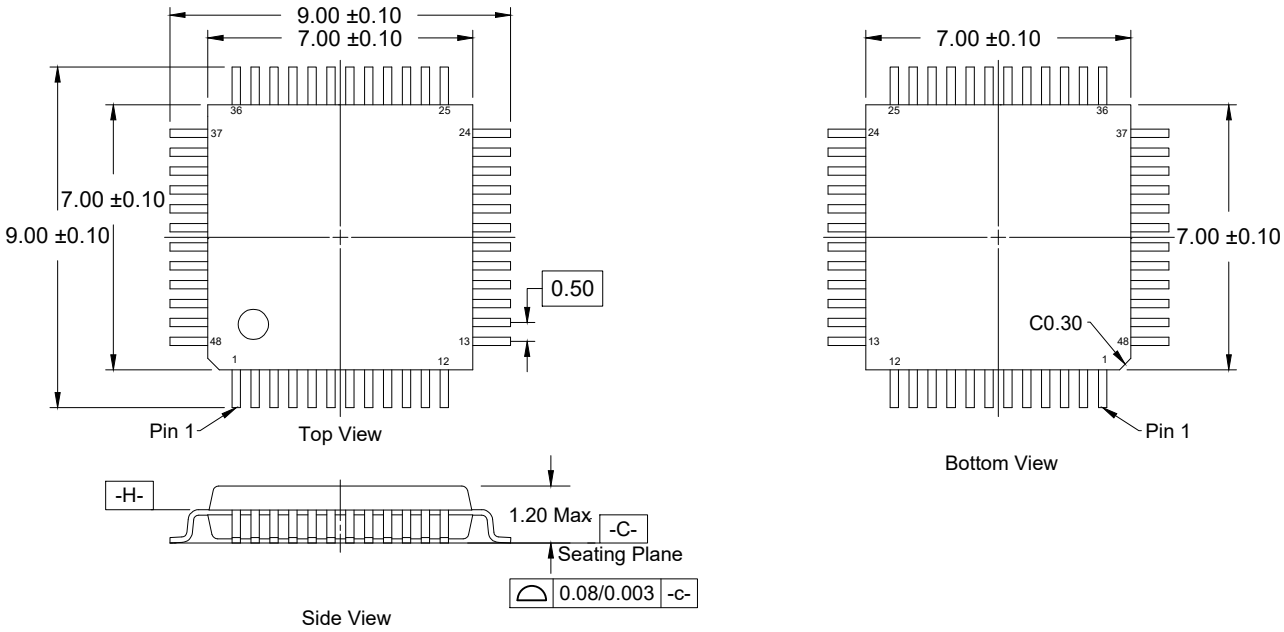
IPC Footprint Type	Package Code/ POD Number	Number of Pins
QFP	Q48.7x7	48

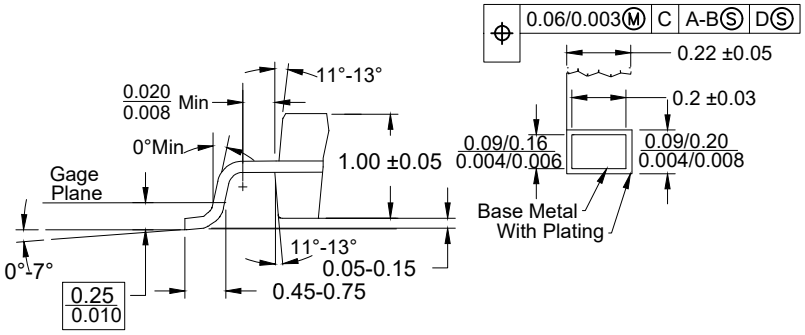
Description	Dimension	Value (mm)	Diagram
Minimum lead span (pin1 side)	Dmin	8.90	
Maximum lead span (pin1 side)	Dmax	9.10	
Minimum lead span	Emin	8.90	
Maximum lead span	Emax	9.10	
Minimum body span (pin1 side)	D1min	6.90	
Maximum body span (pin1 side)	D1max	7.10	
Minimum body span	E1min	6.90	
Maximum body span	E1max	7.10	
Minimum Lead Width	Bmin	0.17	
Maximum Lead Width	Bmax	0.27	
Minimum Lead Length	Lmin	0.45	
Maximum Lead Length	Lmax	0.75	
Number of pins	PinCountD	12	
Number of pins	PinCountE	12	
Distance between the center of any two adjacent pins	Pitch	0.50	
Thermal pad Chamfer/body chamfer	CH	0.30	
Location of pin 1; S2 = Corner of D side, C1 = Center of E side (center).	Pin1	S2	
Maximum Height	Amax	1.2	
Minimum Standoff Height	A1min	0.05	
Minimum Lead Thickness	cmin	0.09	
Maximum Lead Thickness	cmax	0.20	

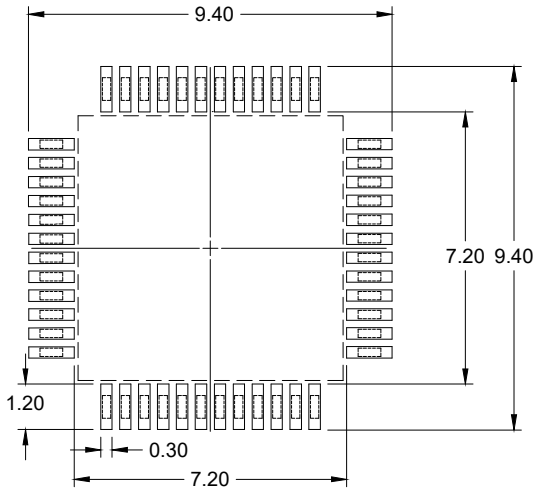
Recommended Land Pattern			
Description	**Dimension**	**Value (mm)**	**Diagram**
Distance between left pad toe to right pad toe	ZE	9.40	
Distance between top pad toe to bottom pad toe	ZD	9.40	
Distance between left pad heel to right pad heel	GE	7.20	
Distance between top pad heel to bottom pad heel	GD	7.20	
Pad Width	X	0.30	
Pad Length	Y	1.20	

Package Outline Drawing

48 Thin Plastic Quad Flatpack Packages (TQFP)
POD Number: Q48.7x7, Revision: 02, Date Created:Dec 18, 2024







Recommended Land Pattern

Notes:

1. Jedec compatible. All dimensions and tolerances per ANSI Y14.5M-1982.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Foot length is measured at gauge plane 0.25 mm above seating plane.
5. Tip to tip dimensions to be determined at seating place -C-.
6. Package body dimensions to be determined at datum plane -H-.
7. Package body dimensions do not include mold protrusion. Allowable protrusion is 0.25mm per side.
8. Lead width does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed max lead width by more than 0.08mm.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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