ISL71710M

Radiation Tolerant Active-Input High Speed Digital Isolator

Description

The ISL71710M is an active input digital signal isolator with CMOS output, using Giant Magnetoresistive (GMR) technology for small size, high speed, and low power. The ISL71710M is the fastest isolator of its type, with a 150Mbps typical data rate. The symmetric magnetic coupling barrier provides a typical propagation delay of only 10ns and a pulse-width distortion as low as 0.3ns, achieving the best specifications of any isolator.

The ISL71710M has unsurpassed common-mode transient immunity of 50kV/µs. It is ideal for isolating applications such as PROFIBUS, RS-485, and RS-422.

The ISL71710M is offered in an 8 Ld 5mm×4mm SOIC package and is fully specified across the military ambient temperature range of -55°C to +125°C.

Applications

- Isolated power
- RS-485 and RS-422
- CAN bus/device net
- Multiplexed data transmission
- Data interfaces
- Board-to-board communication
- Ground loop elimination
- Peripheral interfaces
- Serial communication
- Logic level shifting

Features

- Qualified to Renesas Rad Tolerant Screening and QCI Flow (R34TB0004EU)
- Barrier Voltage Endurance
  - 2.5kV$_{RMS}$ for 1 minute, 600VRMS continuous (VDE V 0884-10 certified: file 5022321-4880-0001)
  - 1.5kV$_{DC}$ continuous
  - 500V$_{DC}$ at 43MeV•cm^2/mg SEDR
- UL 1577 recognized: file reference E483309
- 5V/3.3V CMOS/TTL compatible
- High speed: 150Mbps typical
- 10ns typical propagation delay
- 300ps typical pulse-width distortion
- 4ns typical propagation delay skew
- 50kV/µs typical common-mode transient immunity
- Low EMI/RFI emissions
- Excellent magnetic immunity
- Passes NASA low outgassing specifications
- NiPdAu-Ag leadframes (Pb-free, Sn-free)
- Full military temperature range operation
  - T_A = -55°C to +125°C
  - T_J = -55°C to +150°C
- TID Radiation Lot Acceptance Testing (RLAT) (LDR: <0.01rad(Si)/s)
  - ISL71710M30BZ: 30krad(Si)
  - ISL71710M50BZ: 50krad(Si)
- SEE characterization
  - No DSEE for V_{DD} = 7V at LET = 43MeV•cm^2/mg

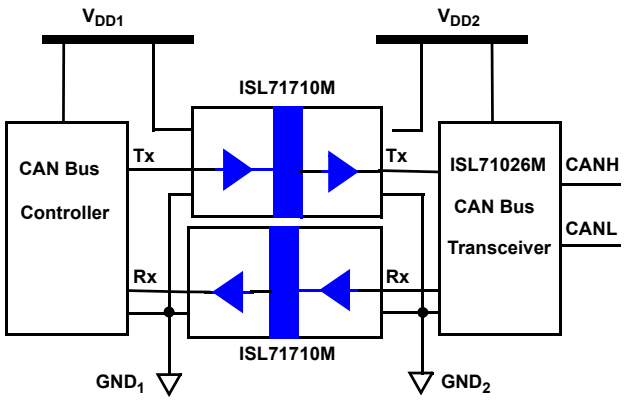


Figure 1. Typical CAN Bus Application

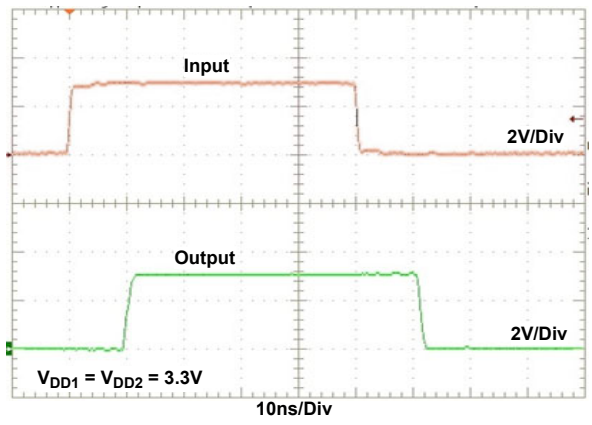
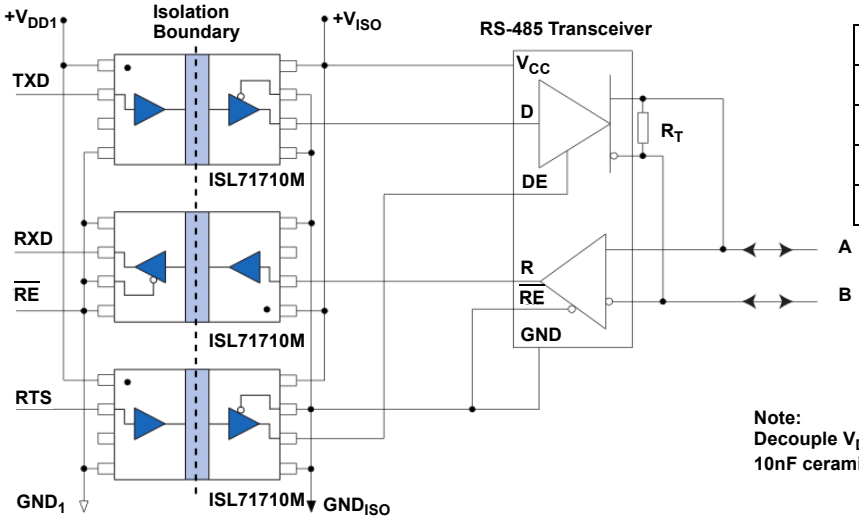


Figure 2. 10MHz Input and Output Waveforms



RS-485 Truth Table

TXD	RTS	A	B	RXD
1	0	Z	Z	X
0	0	Z	Z	X
1	1	1	0	1
0	1	0	1	0

Figure 3. RS-485 Multi-Chip Isolated Transceiver Application Schematic

Contents

1. Overview

1.1 Functional Block Diagram

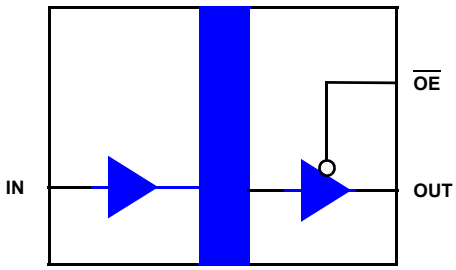


Figure 4. ISL71710M Block Diagram

2. Pin Information

2.1 Pin Assignments

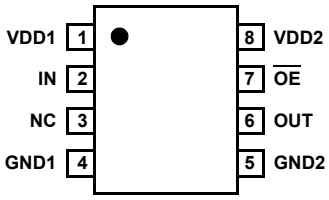
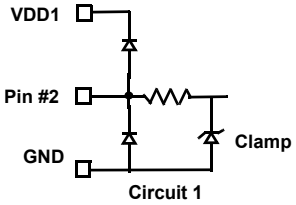
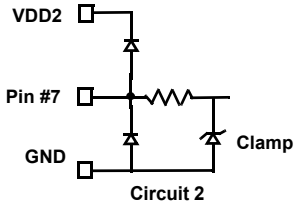


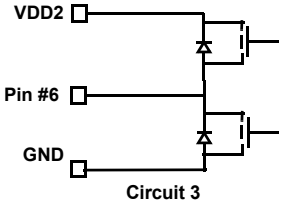
Figure 5. Pin Assignments - Top View

2.2 Pin Descriptions

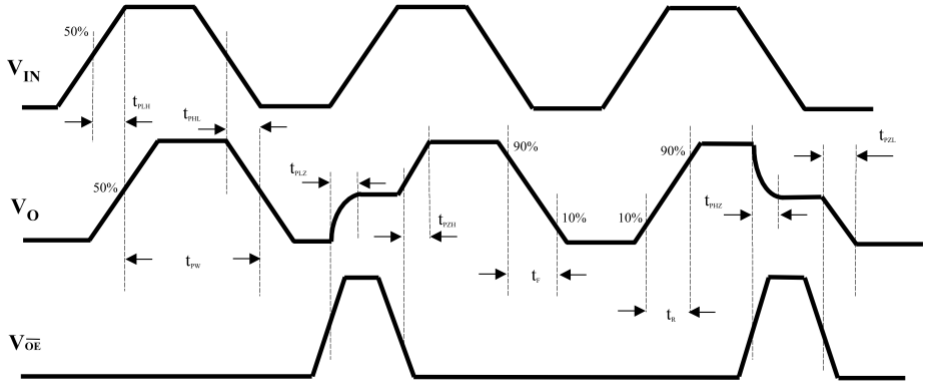
Pin Number	Pin Name	ESD Circuit	Description
1	VDD1	N/A	Supply voltage
2	IN	1	Data in
3	NC	N/A	No internal connection. Leave this pin floating or connect it to VDD1 or GND1.
4	GND1	N/A	Ground return for VDD1
5	GND2	N/A	Ground return for VDD2
6	OUT	3	Data output
7	$\overline{OE}$	2	Output enable, active low. Internally pulled low with 100kΩ to enable the output when this pin is not connected.
8	VDD2	N/A	Supply voltage







2.3 Timing Diagram



Legend

t_{PLH}	Propagation Delay, Low-to-High
t_{PHL}	Propagation Delay, High-to-Low
t_{PW}	Minimum Pulse Width
t_{PLZ}	Propagation Delay, Low-to-High Impedance
t_{PZH}	Propagation Delay, High Impedance-to-High
t_{PHZ}	Propagation Delay, High-to-High Impedance
t_{PZL}	Propagation Delay, High Impedance-to-Low
t_R	Rise Time
t_F	Fall Time

Figure 6. Timing Diagram

3. Specifications

3.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
Maximum Supply Voltage, VDD1 to GND1	-0.5	+7	V
Maximum Supply Voltage, VDD2 to GND2	-0.5	+7	V
In-Beam Maximum Supply Voltage VDD1 to GND1	-0.5	+7	V
In-Beam Maximum Supply Voltage VDD2 to GND2	-0.5	+7	V
IN Voltage	-0.5	V_{DD1} + 0.5	V
$\overline{OE}$ Voltage	-0.5	V_{DD2} + 0.5	V
OUT Voltage	-0.5	V_{DD2} + 0.5	V
Output Current Drive	-	10	mA
Human Body Model (Tested per AEC-Q100-002)	-	1.2	kV
Charge Device Model (Tested per AEC-Q100-011)	-	1.5	kV
Latch-up (Tested per JESD-78E; Class 2, Level A) at +125°C	-	100	mA

3.2 Outgas Testing

Specification (Tested per ASTM E 595, 1.5)	Value	Unit
Total Mass Lost[1]	0.06	%
Collected Volatile Condensible Material [1]	<0.01	%
Water Vapor Recovered	0.03	%

1. Results meet NASA low outgassing requirements of “Total Mass Loss” of <1% and “Collected Volatile Condensible Material” of <0.1%.

3.3 Thermal Information

Parameter	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance	8 Ld SOIC Package	θ_{JA}[1]	Junction to ambient	60	°C/W
		Ψ_{JT}[2]	Junction to case	10	°C/W

1. θ_{JA} is measured with the component soldered to double-sided board; free air.
2. For Ψ_{JT} characterization parameter, the package top temperature is measured at the top center of the mounted package. See TB379.

Parameter	Minimum	Maximum	Unit
Power Dissipation, P_D	-	675	mW
Maximum Junction Temperature	-	+150	°C
Storage Temperature Range	-65	+150	°C
Pb-Free Reflow Profile	See TB493		

3.4 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Ambient Operating Temperature	-55	+125	°C
Supply Voltage V_{DD1}, V_{DD2}	3.0	5.5	V
IN Logic High Voltage	2.4	V_{DD1}	V
IN Logic Low Voltage	0	0.8	V
$\overline{OE}$ Logic High Voltage	2.4	V_{DD2}	V
$\overline{OE}$ Logic Low Voltage	0	0.8	V
Input Signal Rise and Fall Time	-	1	µs

3.5 Insulation Specifications

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Creepage Distance (external)	-	-	4.03	-	-	mm
Total Barrier Thickness (internal)	-	-	12	13	-	µm
Leakage Current[1]	-	$240V_{RMS}$, 60Hz	-	200	-	nA
Barrier Resistance[1]	R_{IO}	$500V_{DC}$	-	$>10^{14}$	-	Ω
Barrier Capacitance[1]	C_{IO}	1MHz	-	1.1	-	pF
Comparative Tracking Index	CTI	Per IEC:60112	≥175	-	-	V
Working Voltage	V_{IORM}	Per VDE V 0884-10, V084-11 pending	600	-	-	V_{RMS}
Barrier Life	-	100°C, $1000V_{RMS}$, 60% Confidence Level activation energy	-	44000	-	Years

1. Device is considered a two terminal device: Pins 1-4 shorted and Pins 5-8 shorted.

3.6 Safety and Approvals

- VDE V 0884-10 (VDE V 0884-11 pending) (Basic Isolation; VDE File Number 5022321-4880-0001)
  - Working voltage (V_{IORM}): $600V_{RMS}$ ($848V_{PK}$); basic insulation; pollution degree 2
  - Isolation voltage (V_{ISO}): $2500V_{RMS}$
  - Transient overvoltage (V_{IOTM}): $4000V_{PK}$
  - Surge rating: 4000V
  - Each part tested at $1590V_{PK}$ for 1s, 5pC partial discharge limit
  - Samples tested at $4000V_{PK}$ for 60s; then $1358V_{PK}$ for 10s with 5pC partial discharge limit

Safety-Limiting Values	Symbol	Value	Unit
Safety Rating Ambient Temperature	T_S	+180	°C
Safety Rating Power	P_S	270	mW
Supply Current Safety Rating (Total of Supplies)	I_S	54	mA

- UL 1577 (Component Recognition Program File Number E483309)
  - Each part tested at $3000V_{RMS}$ ($4240V_{PK}$) for 1s; each lot sample tested at $2500V_{RMS}$ ($3530V_{PK}$) for 1min

3.7 Electrical Specifications

Unless otherwise noted, V_{DD1} V_{DD2} = 3V - 5.5V; OUT and $\overline{OE}$ are open, V_{DD1} and V_{DD2} are bypassed to GND with a 47nF X7R capacitor; T_A = T_J = +25°C. Limits apply across the operating temperature range, -55°C to +125°C unless otherwise stated.

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
3.3V Electrical Specifications						
Input Quiescent Supply Current (Figure 13)	I_{DD1}	-	-	8	40	µA
Output Quiescent Supply Current (Figure 14)	I_{DD2}	-	-	1.2	1.75	mA
Logic Input Current	I_I	-	-10	-	10	µA
Logic High Output Voltage (Figure 21)	V_{OH}	I_O = -20µA, V_I = V_{IH}	V_{DD} - 0.1	V_{DD}	-	V
		I_O = -4mA, V_I = V_{IH}	0.8 x V_{DD}	0.9 x V_{DD}	-	V
Logic Low Output Voltage (Figure 22)	V_{OL}	I_O = 20µA, V_I = V_{IL}	-	0	0.1	V
		I_O = 4mA, V_I = V_{IL}	-	0.5	0.8	V
Switching Specifications (V_{DD} = 3.3V)						
Maximum Data Rate		C_L = 15pF	130	140	-	Mbps
Pulse Width[2]	PW	50% Points, V_O	10	7.5	-	ns
Propagation Delay Input to Output (High-to-Low) (Figure 15)	t_{PHL}	C_L = 15pF	-	12	18	ns
Propagation Delay Input to Output (Low-to-High) (Figure 16)	t_{PLH}	C_L = 15pF	-	12	18	ns
Propagation Delay Enable to Output (High-to-High Impedance) (Figure 23)	t_{PHZ}	C_L = 15pF	-	3	7	ns
Propagation Delay Enable to Output (Low-to-High Impedance) (Figure 24)	t_{PLZ}	C_L = 15pF	-	3	7	ns
Propagation Delay Enable to Output (High Impedance-to-High) (Figure 25)	t_{PZH}	C_L = 15pF	-	3	7	ns
Propagation Delay Enable to Output (High Impedance-to-Low) (Figure 26)	t_{PZL}	C_L = 15pF	-	3	7	ns
Pulse-Width Distortion[3] (Figure 19)	PWD	C_L = 15pF	-	1	4	ns
Pulse Jitter[4]	t_J	C_L = 15pF	-	100	-	ps
Propagation Delay Skew[5]	t_{PSK}	C_L = 15pF	-	4	6	ns
Output Rise Time (10% to 90%) (Figure 17)	t_R	C_L = 15pF	-	2	5	ns
Output Fall Time (10% to 90%) (Figure 18)	t_F	C_L = 15pF	-	2	5	ns
Common-Mode Transient Immunity (Output Logic High or Logic Low)[6]	$\|CM_H\|$,$\|CM_L\|$	V_{CM} = 1500V_{DC} , $t_{TRANSIENT}$ = 25ns	30	50	-	kV/µs
Dynamic Power Consumption[7] (Figure 20)	-	-	-	140	240	µA/Mbps
Magnetic Field Immunity[8] (V_{DD2} = 3V, 3V < V_{DD1} < 5.5V)						
Power Frequency Magnetic Immunity	H_{PF}	50Hz/60Hz	1000	1500	-	A/m
Pulse Magnetic Field Immunity	H_{PM}	t_P = 8µs	1800	2000	-	A/m
Damped Oscillatory Magnetic Field	H_{OSC}	0.1Hz - 1MHz	1800	2000	-	A/m
Cross-Axis Immunity Multiplier[9]	K_X	-	-	2.5	-	-
5V Electrical Specifications						
Input Quiescent Supply Current (Figure 13)	I_{DD1}	-	-	10	75	µA
Output Quiescent Supply Current (Figure 14)	I_{DD2}	-	-	1.8	2.5	mA

Unless otherwise noted, V_{DD1} V_{DD2} = 3V - 5.5V; OUT and $\overline{OE}$ are open, V_{DD1} and V_{DD2} are bypassed to GND with a 47nF X7R capacitor; T_A = T_J = +25°C. Limits apply across the operating temperature range, -55°C to +125°C unless otherwise stated. **(Cont.)**

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Logic Input Current	I_I	-	-10	-	10	µA
Logic High Output Voltage (Figure 21)	V_{OH}	I_O = -20µA, V_I = V_{IH}	V_{DD} - 0.1	V_{DD}	-	V
		I_O = -4mA, V_I = V_{IH}	0.8 x V_{DD}	0.9 x V_{DD}	-	V
Logic Low Output Voltage (Figure 22)	V_{OL}	I_O = 20µA, V_I = V_{IL}	-	0	0.1	V
		I_O = 4mA, V_I = V_{IL}	-	0.5	0.8	V
Switching Specifications (V_{DD} = 5V)						
Maximum Data Rate	-	C_L = 15pF	130	150	-	Mbps
Pulse Width[2]	PW	50% Points, V_O	10	7.5	-	ns
Propagation Delay Input to Output (High-to-Low) (Figure 15)	t_{PHL}	C_L = 15pF	-	10	16	ns
Propagation Delay Input to Output (Low-to-High) (Figure 16)	t_{PLH}	C_L = 15pF	-	10	16	ns
Propagation Delay Enable to Output (High-to-High Impedance) (Figure 23)	t_{PHZ}	C_L = 15pF	-	3	7	ns
Propagation Delay Enable to Output (Low-to-High Impedance) (Figure 24)	t_{PLZ}	C_L = 15pF	-	3	7	ns
Propagation Delay Enable to Output (High Impedance-to-High) (Figure 25)	t_{PZH}	C_L = 15pF	-	3	7	ns
Propagation Delay Enable to Output (High Impedance-to-Low) (Figure 26)	t_{PZL}	C_L = 15pF	-	3	7	ns
Pulse-Width Distortion[3] (Figure 19)	PWD	C_L = 15pF	-	0.3	4	ns
Propagation Delay Skew[5]	t_{PSK}	C_L = 15pF	-	4	6	ns
Output Rise Time (10% to 90%) (Figure 17)	t_R	C_L = 15pF	-	1	4	ns
Output Fall Time (10% to 90%) (Figure 18)	t_F	C_L = 15pF	-	1	4	ns
Common Mode Transient Immunity (Output Logic High or Logic Low)[6]	$\|CM_H\|$,$\|CM_L\|$	V_{CM} = 1500V_{DC}, $t_{TRANSIENT}$ = 25ns	30	50	-	kV/µs
Dynamic Power Consumption[7] (Figure 20)	-	-	-	200	340	µA/Mbps
Magnetic Field Immunity[8] (V_{DD2} = 5V, 3V < V_{DD1} < 5.5V)						
Power Frequency Magnetic Immunity	H_{PF}	50Hz/60Hz	2800	3500	-	A/m
Pulse Magnetic Field Immunity	H_{PM}	t_P = 8µs	4000	4500	-	A/m
Damped Oscillatory Magnetic Field	H_{OSC}	0.1Hz - 1MHz	4000	4500	-	A/m
Cross-axis Immunity Multiplier[9]	K_X	-	-	2.5	-	-

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.
2. Minimum pulse width is the minimum value at which specified PWD is ensured.
3. PWD is defined as $|t_{PHL} - t_{PLH}|$. %PWD is equal to PWD divided by pulse width.
4. 66535-bit pseudo-random binary signal (PRBS) NRZ bit pattern with no more than five consecutive 1s or 0s; 800ps transition time.
5. t_{PSK} is the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} between devices at +25°C.
6. CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V_{DD2}. CML is the maximum common-mode input voltage that can be sustained while maintaining V_O < 0.8V. The common-mode voltage slew rate apply to both rising and falling common-mode voltage edges.
7. Dynamic power consumption is calculated per channel and is supplied by the channel's input side power supply.
8. The relevant test and measurement methods are given in Electromagnetic Compatibility.
9. External magnetic field immunity is improved by this factor if the field direction is "end-to-end" rather than to "pin-to-pin" (see Figure 27).

4. Typical Performance Curves

T_A = +25°C, unless otherwise specified.

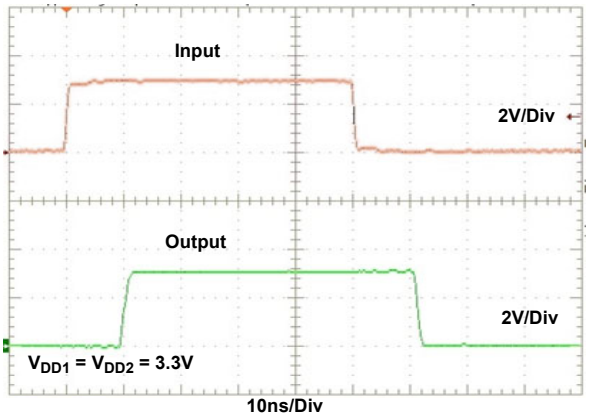


Figure 7. 10MHz Input and Output Waveforms

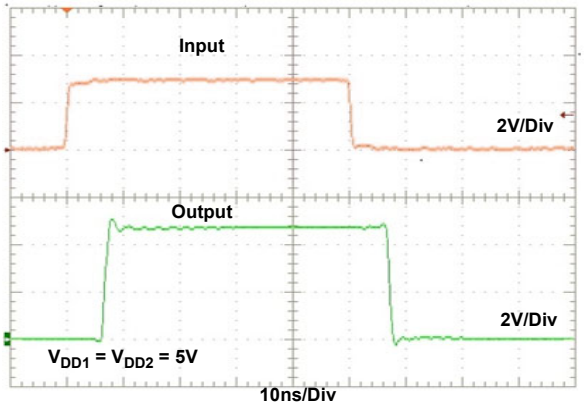


Figure 8. 10MHz Input and Output Waveforms

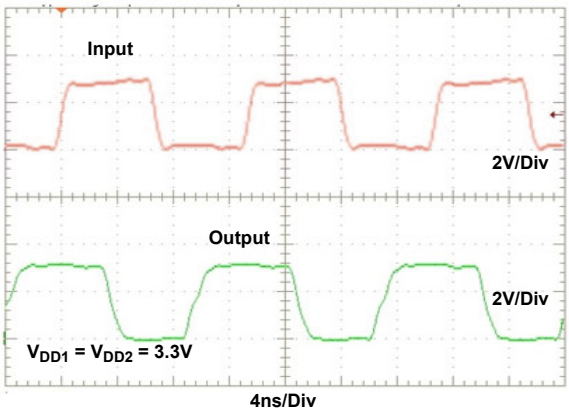


Figure 9. 75MHz Input and Output Waveforms

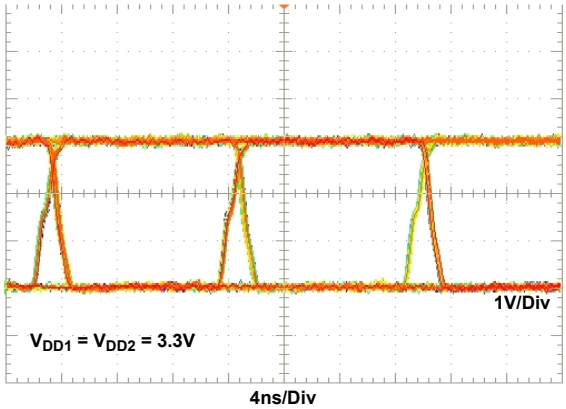


Figure 10. 75Mbps Eye Diagram

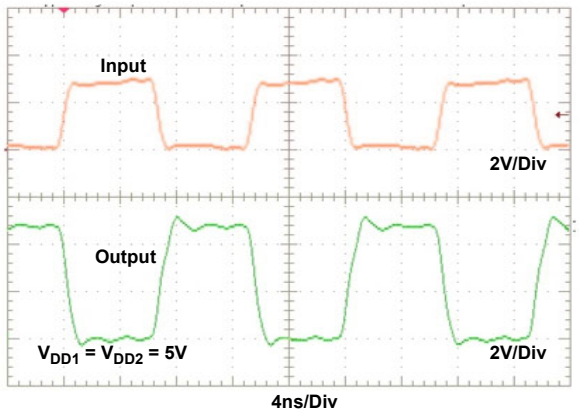


Figure 11. 75MHz Input and Output Waveforms

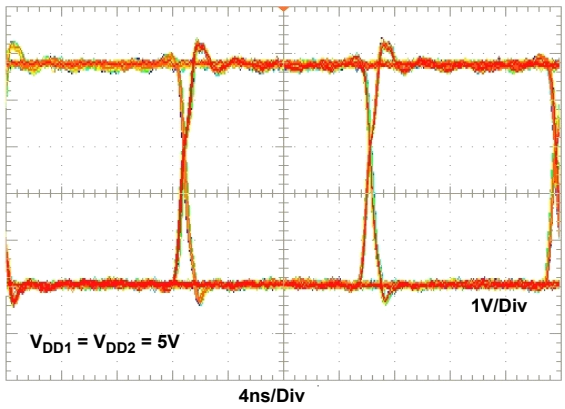


Figure 12. 75Mbps Eye Diagram

T_A = +25°C, unless otherwise specified. (Cont.)

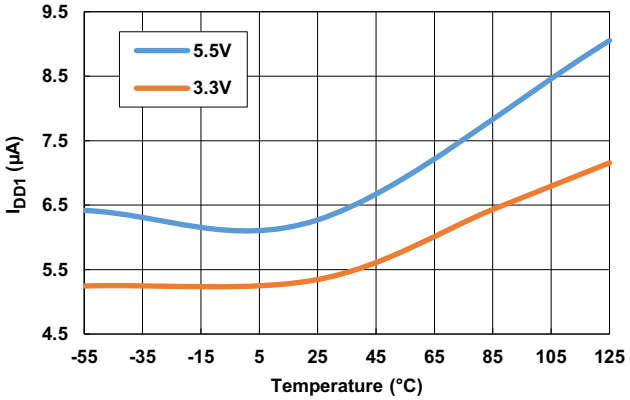


Figure 13. Input Quiescent Supply Current vs Temperature vs V_{DD1} Voltage

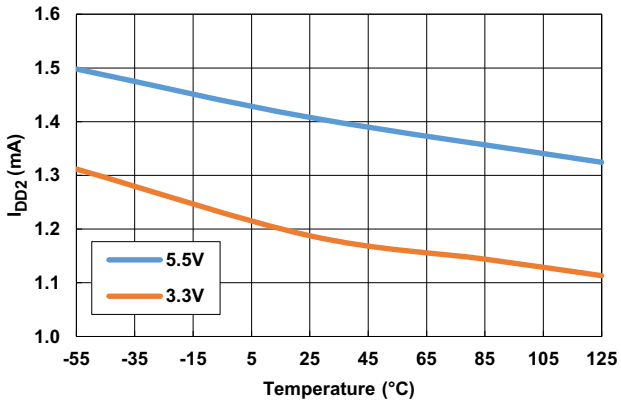


Figure 14. Output Quiescent Supply Current vs Temperature vs V_{DD2} Voltage

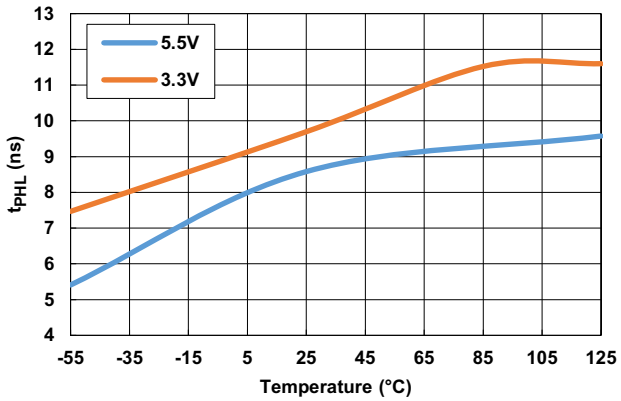


Figure 15. Propagation Delay (High-to-Low) vs Temperature vs V_{DD} Voltage

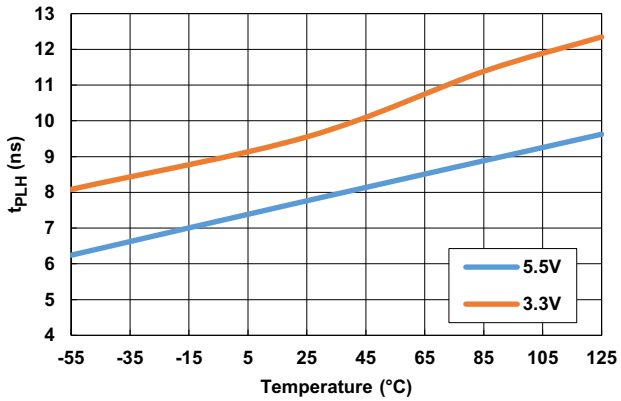


Figure 16. Propagation Delay (Low-to-High) vs Temperature vs V_{DD} Voltage

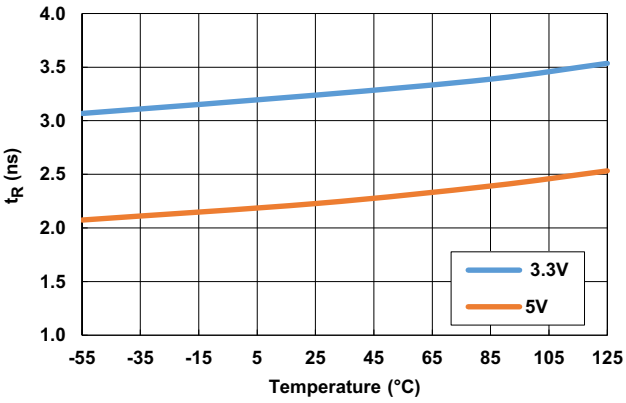


Figure 17. Output Rise Time vs Temperature vs V_{DD} Voltage

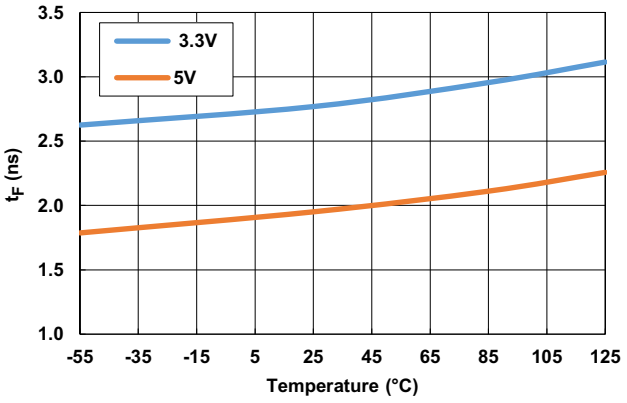


Figure 18. Output Fall Time vs Temperature vs V_{DD} Voltage

T_A = +25°C, unless otherwise specified. (Cont.)

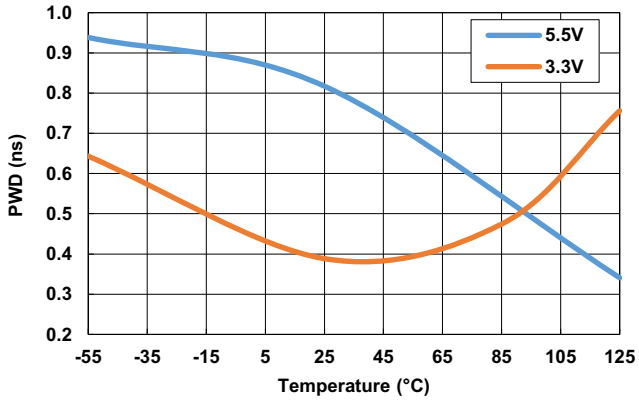


Figure 19. 5.5V Pulse-Width Distortion vs Temperature vs V_{DD} Voltage

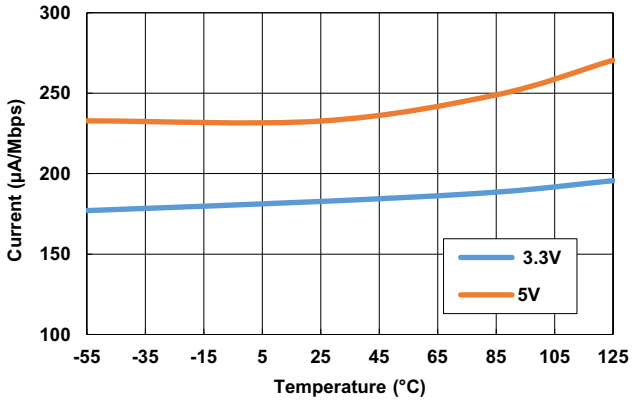


Figure 20. Dynamic Power Consumption vs Temperature

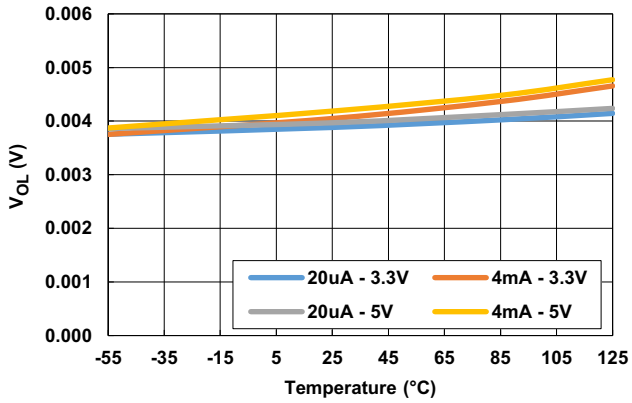


Figure 21. Logic Low Output Voltage vs Temperature

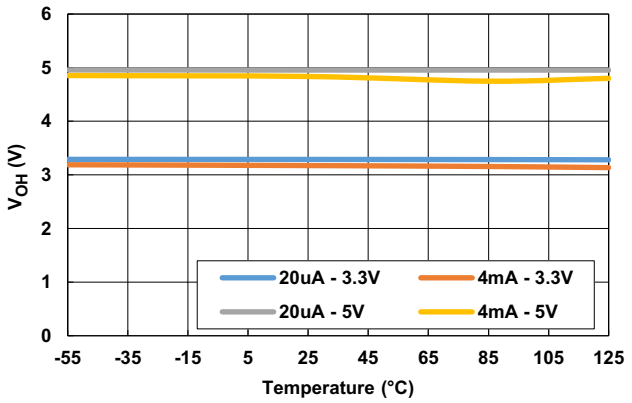


Figure 22. Logic High Output Voltage vs Temperature

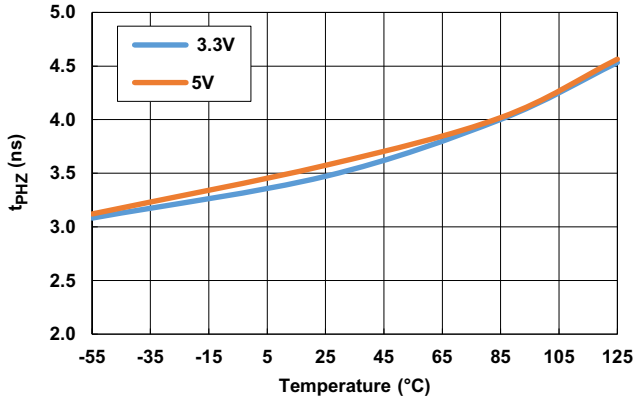


Figure 23. Propagation Delay Enable to Output (High-to-High Impedance) vs Temperature

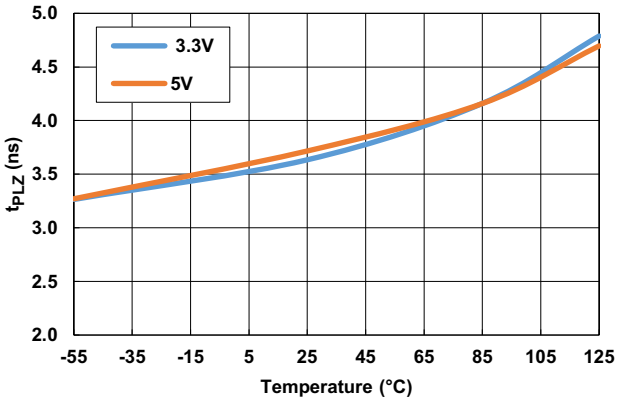


Figure 24. Propagation Delay Enable to Output (Low-to-High Impedance) vs Temperature

T_A = +25°C, unless otherwise specified. (Cont.)

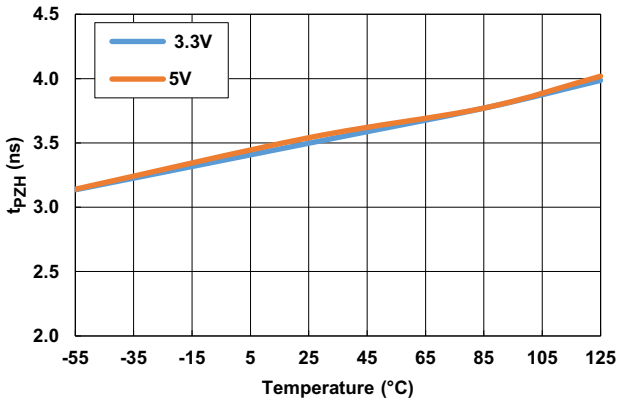


Figure 25. Propagation Delay Enable to Output (High Impedance-to-High) vs Temperature

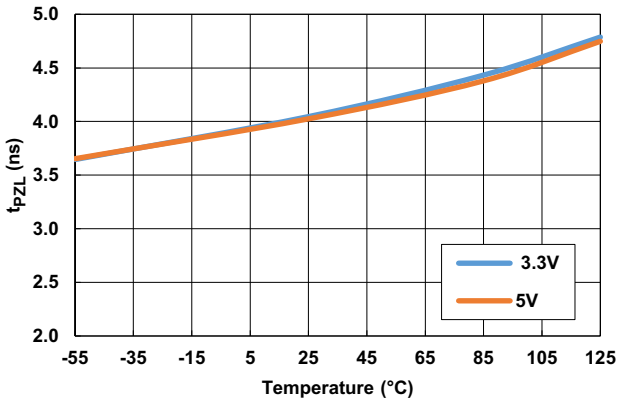


Figure 26. Propagation Delay Enable to Output (High Impedance-to-Low) vs Temperature

5. Device Information

5.1 Electrostatic Discharge Sensitivity

This product has been tested for electrostatic sensitivity to the limits stated in Absolute Maximum Ratings. However, Renesas recommends that all integrated circuits are handled with appropriate care to avoid damage. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.

5.2 Electromagnetic Compatibility

The ISL71710M has the lowest EMC footprint of any isolation technology. Its Wheatstone bridge configuration and differential magnetic field signaling ensure excellent EMC performance against all relevant standards.

Immunity to external magnetic fields is even higher if the field direction is “end-to-end” rather than to “pin-to-pin” as shown in Figure 27.

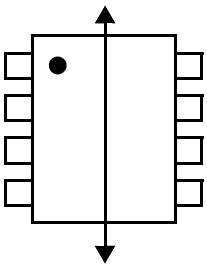


Figure 27. Cross-Axis Field Direction

5.3 Dynamic Power Consumption

The ISL71710M achieves its low power consumption from the way it transmits data across the isolation barrier. By detecting the edge transitions of the input logic signal and converting these to narrow current pulses, a magnetic field is created around the GMR Wheatstone bridge. Depending on the direction of the magnetic field, the bridge causes the output comparator to switch following the input logic signal. The power consumption is independent of mark-to-space ratio and solely dependent on frequency, because the current pulses are narrow, about 2.5ns. This has obvious advantages over optocouplers, which have power consumption heavily dependent on mark-to-space ratio.

5.4 Power Supply Decoupling

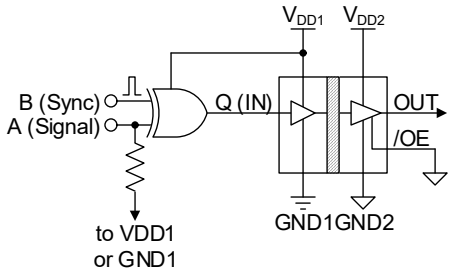
Both power supplies to these devices should be decoupled with low ESR 47nF ceramic capacitors. Ground planes for both GND1 and GND2 are highly recommended for data rates above 10Mbps. Capacitors must be located as close as possible to the VDD pins.

5.5 Signal Status on Start-Up

To minimize power dissipation, input signals are differentiated and then per GMR technology magnetically latched on the output side of the isolation barrier. Here, the latched state of the GMR resistor bridge on the isolator's secondary side is independent of the secondary supply, V_{DD2}. Applying V_{DD2} only enables the comparator to detect the GMR bridge voltage and to reconstruct the output signal electrically.

Magnetic latching has the advantage that the magnetic state of the GMR bridge remains, even during a loss of V_{DD2}. However, it can also lead to an indeterminate output state after power-up, shutdown, and power loss sequencing events.

To ensure that the isolator is in a known output state, the input signal must be EXOR-ed with a sync-pulse (see Figure 28). Here, the required output state after power-up is defined by the logic state of EXOR input A. When V_{DD1} is fully established, applying a sync-pulse (low – high – low) to EXOR input B causes a pulse at the isolator input (IN). This latches the logic state at input A into the GMR bridge across the barrier. *Note*: The pulse width at IN must be ≥10ns. After the application of the sync pulse, powering up V_{DD2}, the isolator output assumes the required output state.



Sig A	Sync B	IN Q
0	0	0
	1	1
	0	0
1	0	1
	1	0
	0	1

Figure 28. Sync Circuit with EXOR Truth Table

Complete the following supply sequencing steps to ensure the output starts in a known output state:

1. Start with V_{DD1}, V_{DD2}, and /OE being at 0V.
2. Apply V_{DD1}.
3. After V_{DD1} is fully established, apply the sync-pulse at input B. Ensure that the pulse width at IN is ≥10ns.
4. Apply V_{DD2}. Observe that V_{OUT} starts in the state set by input A.

5.6 Data Transmission Rates

The reliability of a transmission system is directly related to the accuracy and quality of the transmitted digital information. For a digital system, parameters that determine the limits of the data transmission are pulse-width distortion and propagation delay skew.

Propagation delay is the time taken for the signal to travel through the device. This is usually different when sending a low-to-high than when sending a high-to-low signal. This difference, or error, is called Pulse-Width Distortion (PWD) and is usually in nanoseconds. It may also be expressed as a percentage:

- PWD% = [Maximum Pulse-Width Distortion (ns)/Signal Pulse Width (ns)] x 100%

For example, with data rates of 12.5Mbps:

- PWD% = [3ns/80ns] x 100% = 3.75%

This figure is almost three times better than any available optocoupler with the same temperature range, and two times better than any optocoupler regardless of published temperature range. The ISL71710M exceeds the 10% maximum PWD recommended by PROFIBUS, and runs to nearly 35Mbps within the 10% limit.

Propagation delay skew is the signal propagation difference between two or more channels. This becomes significant in clocked systems because it is undesirable for the clock pulse to arrive before the data has settled. Short propagation delay skew is therefore especially critical in high data rate parallel systems for establishing and maintaining accuracy and repeatability. Worst-case channel-to-channel skew in an ISL71710M isolator is only 4ns, which is ten times better than any optocoupler. ISL71710M isolators have a maximum propagation delay skew of 6ns, which is five times better than any optocoupler.

5.7 Truth Table

Table 1 displays the ISL71710M truth table.

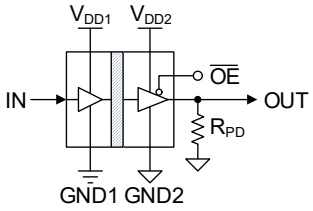
Table 1. Truth Table

IN	VDD1	GMR	VDD2	$\overline{OE}$	OUT
H	Powered	H	Powered	L	H
L	Powered	L	Powered	L	L
X	Powered	X	Powered	H	Z
X	Unpowered	indeterminate	Powered	L	indeterminate
X	Unpowered	indeterminate	Powered	H	Z
X	X	X	Unpowered	X	Z_{wk}[1]

1. A weak high-impedance state can occur under the following conditions:
   - If VDD2 is floating, the output transistors are usually turned off, resulting in a high-impedance state, but parasitic body diodes may still conduct. Leakage currents through these diodes can cause the OUT pin to float at an undefined voltage. Therefore, despite being in a high-impedance state, the OUT pin is not truly disconnected, especially if other signals are still driving the output while its supply is floating. This might violate input voltage ratings and potentially inject current into the unpowered circuit. Hence, a floating VDD2 turns the push-pull output into an uncontrolled high-impedance state rather than a clean, open-circuit high-impedance state.
   - If VDD2 is grounded (0V), the ESD protection diodes clamp the output to VDD2 (0V). Any voltage applied to the output cannot rise above 0.7V; therefore, creating a low-impedance, power-consuming path.

5.8 Fail-Safe Resemblance

As the ISL71710M has no inherent fail-safe state. One method to achieve a defined output state (preferrable Low) when VDD1 is lost is by disabling the output ($\overline{OE}$ = High) and pulling it low with a pull-down resistor (Figure 29).



IN	VDD1	VDD2	$\overline{OE}$	OUT
H	Powered	Powered	L	H
L	Powered	Powered	L	L
X	Powered	Powered	H	L_{pd}[1]
X	X	Unpowered	X	L_{pd}[1]
X	Unpowered	Powered	L	Indeterminate
X	Unpowered	Powered	H	L_{pd}[1]

1. Pull-Down Low

Figure 29. Fail-Safe Low Resemblance with Modified Output and Corresponding Truth Table

The truth table in Figure 29 shows that if VDD2 is lost, the output Z_{wk} state is turned into a defined L_{pd} state. If VDD1 is lost while the output driver is active, OUT can still be high or low and is therefore indeterminate. To achieve a defined low, $\overline{OE}$ must be asserted high.

6. Radiation Tolerance

The ISL71710M isolator is a radiation tolerant device for commercial space applications, Low Earth Orbits (LEO) applications, high altitude avionics, launch vehicles, and other harsh environments. This device's response to Total Ionizing Dose (TID) radiation effects, and Single Event Effects (SEE) has been measured, characterized, and reported in the proceeding sections. The TID performance of the ISL71710MBZ is not guaranteed through radiation acceptance testing. The ISL71710M30BZ is radiation lot acceptance tested (RLAT) to 30krd (Si), and the ISL71710M50BZ is radiation lot acceptance tested to 50krad (Si).

6.1 Total Ionizing Dose (TID) Testing

Total dose testing of the ISL71710MBZ proceeded in accordance with the guidelines of MIL-STD-883 Test Method 1019. The experimental matrix consisted of 32 samples irradiated at a 5.5V bias, as shown in Table 2, and 16 samples irradiated with all pins grounded (unbiased). Three control units were used. The bias configuration is shown in Figure 46.

Samples of the ISL71710MBZ were packaged in the production 8 Ld plastic NSOIC, Package Outline Drawing (POD) M8.15G. The samples were screened to datasheet limits at +125°C temperature only before irradiation.

Total dose irradiations were performed using a Hopewell Designs N40 panoramic vault-type low dose rate ^{60}Co irradiator located in the Renesas Palm Bay, Florida facility. The dose rate was < 10mrad(Si)/s). PbAl spectrum hardening filters were used to shield the test board and devices under test against low energy secondary gamma radiation.

Down points for the testing were 0krad(Si), 10krad(Si), 30krad(Si), and 50krad(Si). All electrical testing was performed outside the irradiator using production Automated Test Equipment (ATE) with data logging of all parameters at each down point. All down point electrical testing was performed at +25°C temperature.

6.1.1 Results

Table 2 summarizes the attributes data.

Table 2. ISL71710M Total Dose Test Attributes Data

Dose Rate (mrad(Si)/s)	Bias	Sample Size	Down Point	Bin 1[1]	Rejects
8.9	Biased Figure 46	32	Pre-rad	32	-
			10krad(Si)	32	0
			30krad(Si)	32	0
			50krad(Si)	32	0
8.9	Grounded	16	Pre-rad	16	-
			10krad(Si)	16	0
			30krad(Si)	16	0
			50krad(Si)	16	0

1. Bin 1 indicates a device that passes all datasheet specification limits.

The plots in Figure 30 through Figure 45 show data for key parameters at all down points. The plots show the average as a function of total dose for each of the irradiation conditions; we chose to use the average because of the relatively large sample sizes. All parts showed excellent stability over irradiation.

Table 3 shows the average of some of these key parameters with respect to total dose in tabular form.

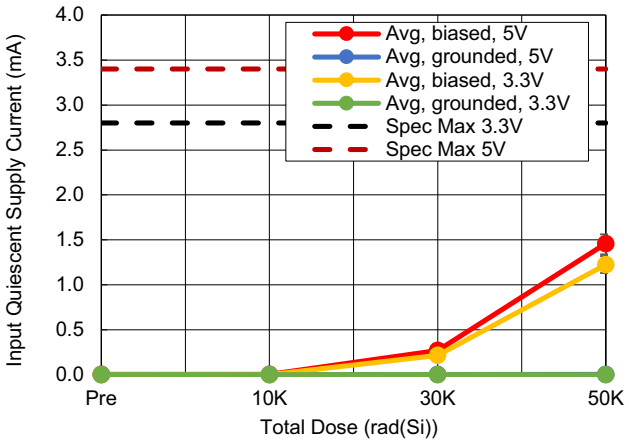


Figure 30. Input Quiescent Supply Current vs TID

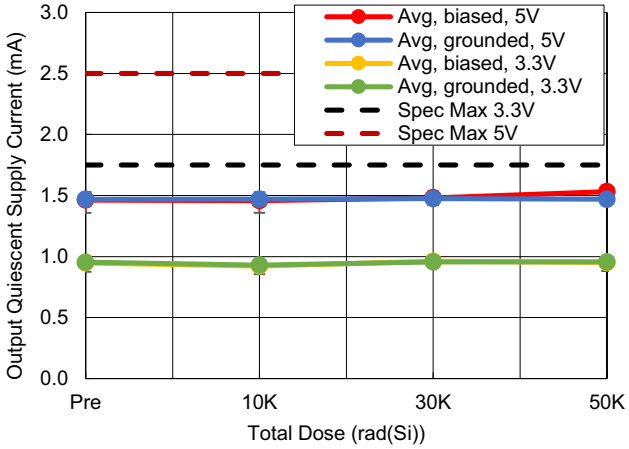


Figure 31. Output Quiescent Supply Current vs TID

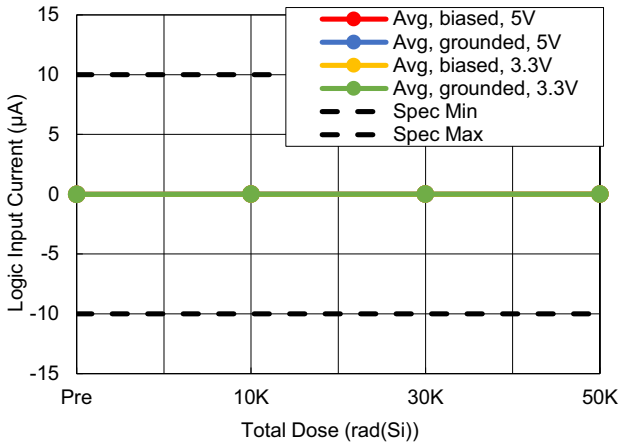


Figure 32. Logic Input Current vs TID

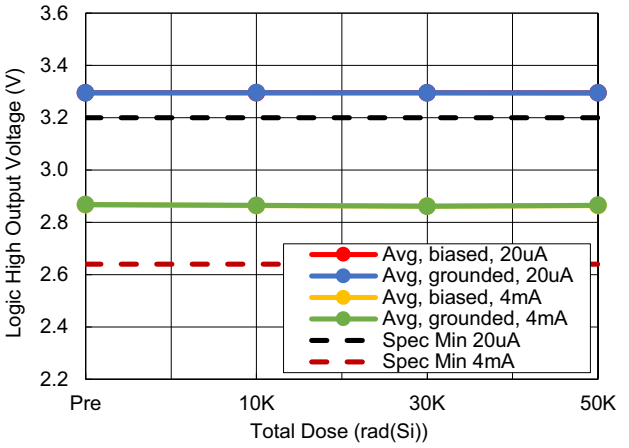


Figure 33. 3.3V Logic High Output Voltage vs TID

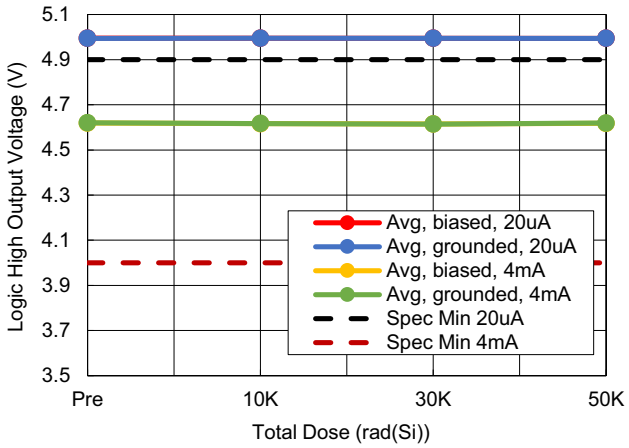


Figure 34. 5V Logic High Output Voltage vs TID

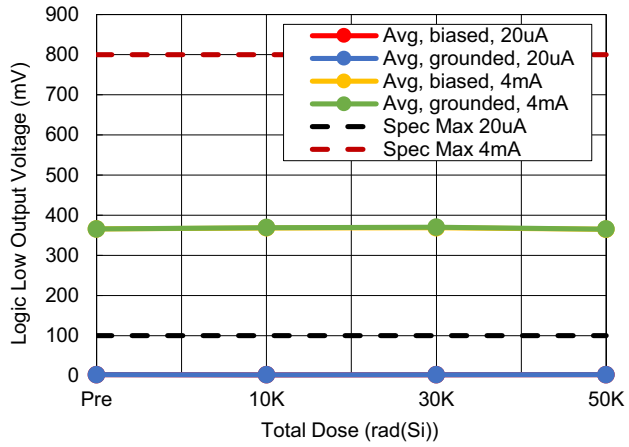


Figure 35. 3.3V Logic Low Output Voltage vs TID

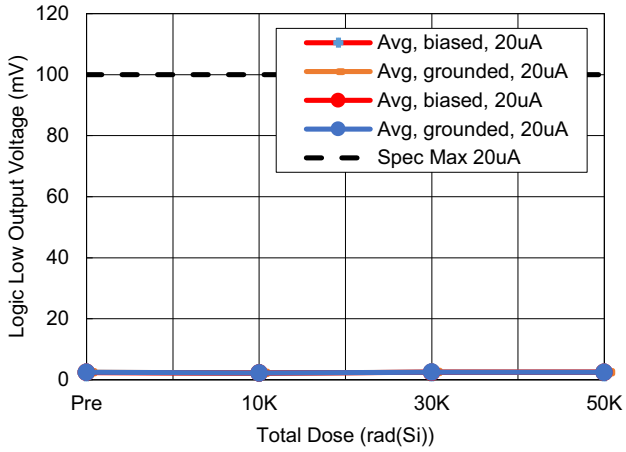


Figure 36. 5V Logic Low Output Voltage vs TID, 20µA

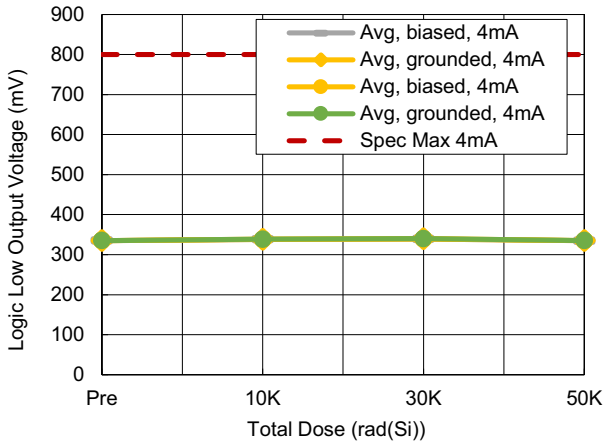


Figure 37. 5V Logic Low Output Voltage vs TID, 4mA

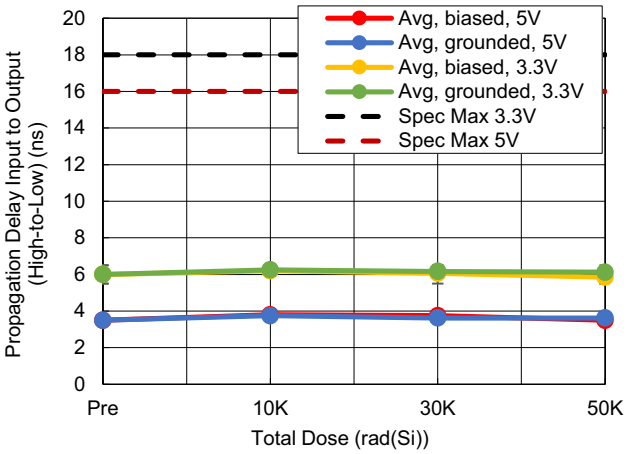


Figure 38. Propagation Delay (High-to-Low) vs TID

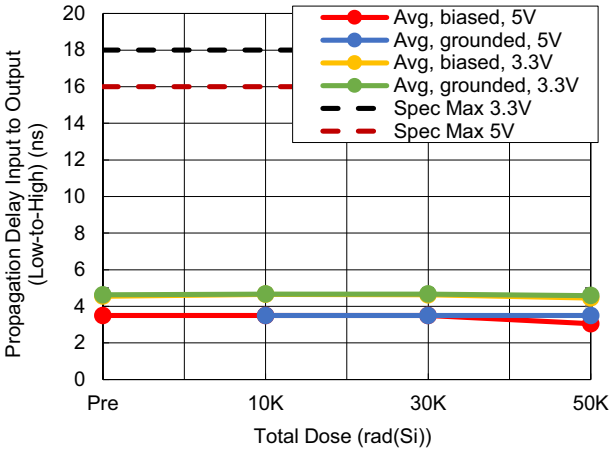


Figure 39. Propagation Delay (Low-to-High) vs TID

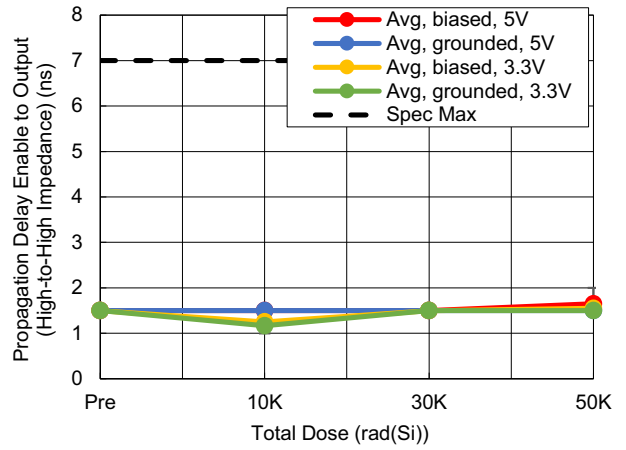


Figure 40. Propagation Delay EN (High-to-High Z) vs TID

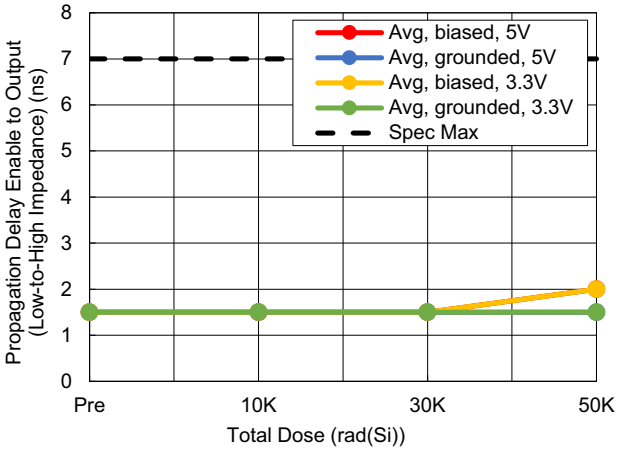


Figure 41. Propagation Delay EN (Low-to-High Z) vs TID

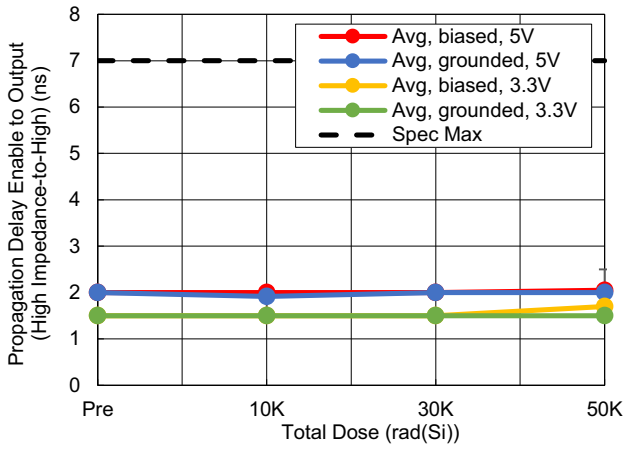


Figure 42. Propagation Delay EN (High Z to High) vs TID

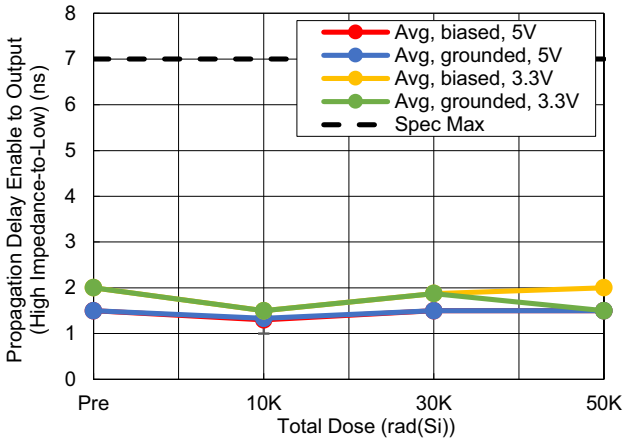


Figure 43. Propagation Delay EN (High Z to Low) vs TID

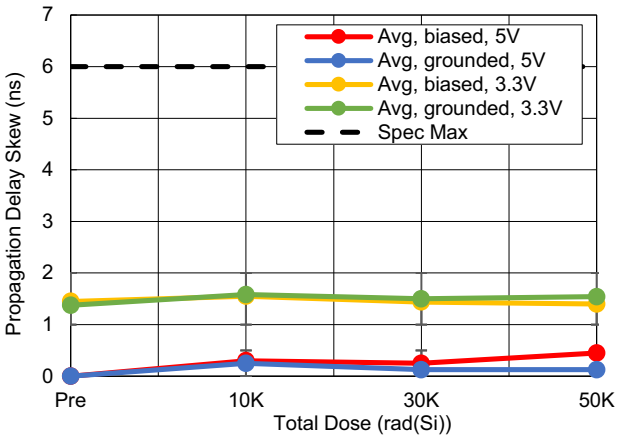


Figure 44. Propagation Delay Skew vs TID

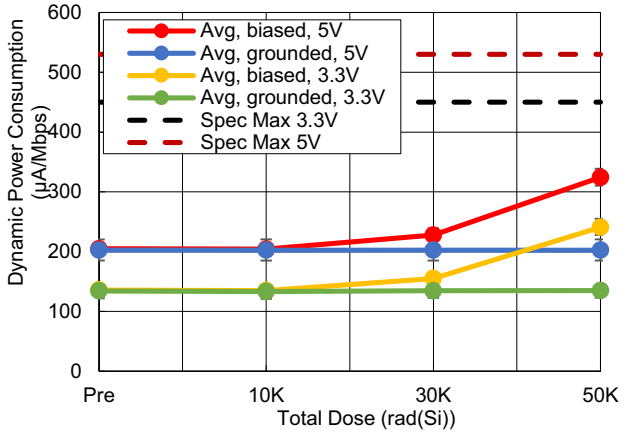


Figure 45. Dynamic Power Consumption vs TID

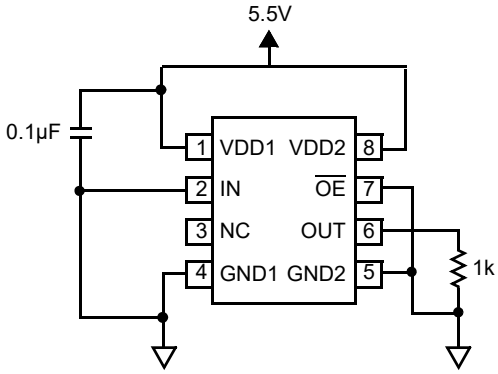


Figure 46. ISL71710M TID Biased Configuration

6.1.2 Conclusion

ATE characterization testing showed no rejects to the datasheet limits at all down points. Variables data for selected parameters is presented in Figure 30 through Figure 45. No differences between biased and unbiased irradiation were noted, and the part is not considered bias sensitive.

Table 3. ISL71710M Response of Selected Key Parameters vs TID

Parameter	Bias	0krad(Si)	10krad(Si)	30krad(Si)	50krad(Si)	Unit
5V Output Quiescent Supply Current	Biased	1.46348	1.46977	1.48083	1.53151	mA
	Grounded	1.46848	1.46977	1.47479	1.46881	
5V Input Quiescent Supply Current	Biased	0.00555	0.00546	0.27117	1.46017	mA
	Grounded	0.00556	0.00548	0.00548	0.00546	
5V Propagation Delay Input to Output (Low-to-High)	Biased	3.5	3.5	3.5	3.5	ns
	Grounded	3.5	3.5	3.5	3.5	
5V Propagation Delay Input to Output (High-to-Low)	Biased	3.50	3.80	3.75	3.50	ns
	Grounded	3.50	3.75	3.63	3.63	
5V Logic Input Current	Biased	-0.00836	0.00554	0.00551	0.00791	µA
	Grounded	-0.00887	0.01019	0.00464	0.00581	
5V Dynamic Power Consumption	Biased	204.73	204.22	227.67	324.29	µA/Mbps
	Grounded	202.56	202.47	202.45	202.49	
3.3V Output Quiescent Supply Current	Biased	0.94754	0.92189	0.96138	0.95411	mA
	Grounded	0.95292	0.92933	0.95567	0.95141	
3.3V Input Quiescent Supply Current	Biased	0.00222	0.00218	0.21798	1.22563	mA
	Grounded	0.00226	0.00216	0.00225	0.00221	
3.3V Propagation Delay Input to Output (Low-to-High)	Biased	4.55	4.65	4.625	4.45	ns
	Grounded	4.625	4.667	4.667	4.583	
3.3V Propagation Delay Input to Output (High-to-Low)	Biased	6.000	6.200	6.063	5.850	ns
	Grounded	6.000	6.250	6.166	6.125	
3.3V Logic Input Current	Biased	-0.00743	0.00789	0.00785	0.00814	µA
	Grounded	-0.00887	0.00843	0.00892	0.00892	
3.3V Dynamic Power Consumption	Biased	135.77	134.82	155.21	240.77	µA/Mbps
	Grounded	134.17	133.23	134.64	134.84	

6.2 Single Event Effects Testing

The intense heavy ion environment encountered in space applications can cause a variety of Single Event Effects (SEE). SEE can lead to system-level performance issues including disruption, degradation, and destruction. For predictable and reliable space system operation, individual electronic components should be characterized to determine their SEE response. The following is a summary of the SEE testing of the ISL71710M.

6.2.1 SEE Test Facility

Testing was performed at the Texas A&M University (TAMU) Cyclotron Institute heavy ion facility. This facility is coupled to a K500 superconducting cyclotron that is capable of generating a wide range of test particles with the various energy, flux, and fluence level needed for advanced radiation testing.

6.2.2 Scope of the ISL71710M SEE Testing

The ISL71710M is a single channel, active input, digital isolator in an 8 Ld NSOIC package. The testing described here was undertaken to do a preliminary evaluation of the ISL71710M for use in space applications. Both destructive Single Event Dielectric Rupture (SEDR) of the barrier isolation and non-destructive Single Event Transients (SET) were tested. In addition, destructive Single Event Burnout (SEB) and Single Event Latch-Up (SEL) of the CMOS circuitry were tested.

6.2.3 Testing Set Up

The plastic packages were opened chemically to expose the die surface so that SEE testing could be accomplished. Care had to be observed to ensure that the plastic was opened but that the isolation barrier was not compromised. This took a bit of trial and error, but a process to open the parts was found. When opened, the barrier isolation was degraded by free air breakdown to about $750V_{DC}$.

Four parts were mounted close together on boards for simultaneous irradiation. For the barrier SEDR testing the pins on either side of the barrier were all shorted together (1-4 on one side and 5-8 on the other side) so that a high voltage could be applied across the isolation barrier. For SEB and SEL testing the parts were powered with various V_{DD1} and V_{DD2} voltages while irradiating. For both forms of destructive SEE the parts were heated to 125°C. For the SET testing the parts were at 25°C and biased with either 3.0V or 5.5V supplies with static inputs of both states tested.

6.2.4 Isolation Barrier SEDR Testing

Because the ISL71710M digital isolator has the same barrier and isolation construction as the ISL71610M digital isolator, the ISL71610M SEDR test results qualify by extension the ISL71710M part and it is rated to $500V_{DC}$ at 43MeV•cm^2/mg SEDR. The following is the summary of the ISL71610M SEDR testing.

The ISL71610M barrier isolation SEDR was tested by biasing the four parts with 200V to 500V in 50V increments while irradiating with normal incidence silver (Ag) for a surface LET of 43MeV•cm^2/mg to a fluence of $1x10^7$ ion/cm^2 at each of the seven voltages. The four parts were heated to +125°C for the testing. The leakage current across the barrier of each part was measured before and after each irradiation to assess the change. The leakages all measured below 75nA both before and after irradiation. No leakage changed by more than 50% as a result of the irradiation being observed. The isolation barrier is rated to 500V over the entire temperature and voltage ranges.

6.2.5 SEB and SEL Testing

For SEB and SEL testing, the isolation barrier voltage was set to 0V and the four parts were powered with supply voltages for both V_{DD1} and V_{DD2} of 5.5V, 6.0V, 6.5V, and 7.0V. The parts were heated to +125°C during the testing. Before and after each irradiation to $1x10^7$ ion/cm^2 with normal incidence silver (Ag) for a surface LET of 43MeV•cm^2/mg the supply currents and the output voltages were measured at V_{DD} of 5.0V at both input states to exercise both output conditions. During irradiation the input had a 500kHz signal applied (0V-5V). None of the monitored values changed significantly (more than 1%) during the irradiations.

6.2.6 SET Testing

The ISL71710M was tested for qualification of Single Event Transients (SET) on October 16, 2018. The testing was done at Texas A&M University's Cyclotron Institute.

For SET testing the ISL71710 parts were tested two at a time (all within the beam diameter). The parts were tested in static operation for unambiguous detection of the SET. Each output was buffered and monitored by an oscilloscope that stored a trace whenever triggered. The triggers were set according to the nominal output. When the nominal output was a logic low (GND), the trigger was set for any transition through 0.8V. When the nominal output was logic high (V_{DD2}) the trigger was set for any transition through 2.0V. The supply voltages, V_{DD1} and V_{DD2}, were set together and to either 3.00V or 4.25V. These represent the lowest voltages anticipated for supplies of a 3.3V nominal and for a 5.0V nominal (including use with the ISL70040SEH low side GaN FET driver). The input voltage was set to either 0.8V or 2.4V to provide the marginal logic voltages. The summary of the SET counts appears in Table 4.

Table 4. SET Count Summary for the Testing of ISL71710M

LET (MeV•cm^2/mg)	V_{IN} (V)	Trigger (V)	V_{DD1} and V_{DD2} (V)	SET Counts in 1x10^{7}ions/cm^2				Totals
				DUT1	DUT2	DUT3	DUT4	
43	0.8	0.8	3.00	9	4	11	2	26
			4.25	9	7	3	10	29
	2.4	2.0		0	0	0	7	7
			3.00	0	2	2	13	17
				DUT5	DUT6	DUT7	DUT8	
20	0.8	0.8	3.00	8	7	1	3	19
			4.25	6	1	4	1	12
	2.4	2.0		0	0	0	4	4
			3.00	0	4	7	8	19
8.5	0.8	0.8	3.00	8	2	4	2	16
			4.25	3	0	0	0	3
	2.4	2.0		0	0	0	0	0
			3.00	0	0	0	0	0

The captured SET traces for the case of 43MeV•cm^2/mg were post processed with a MATLAB® routine to find the duration of the triggering SET. The duration was calculated as the initial transient time beyond the trigger level, either 0.8V or 2.0V depending on the nominal output. These results were plotted in a form similar to a probability plot and are presented in Figure 47. The longest SET observed was 18.4ns, for the case of V_{DD} at 3.00V and a high output. Durations were the output SET time below 2.0V for nominal high output, and the duration above 0.8V for a nominal low output. The legend identifies the V_{DD} setting and the input voltage setting.

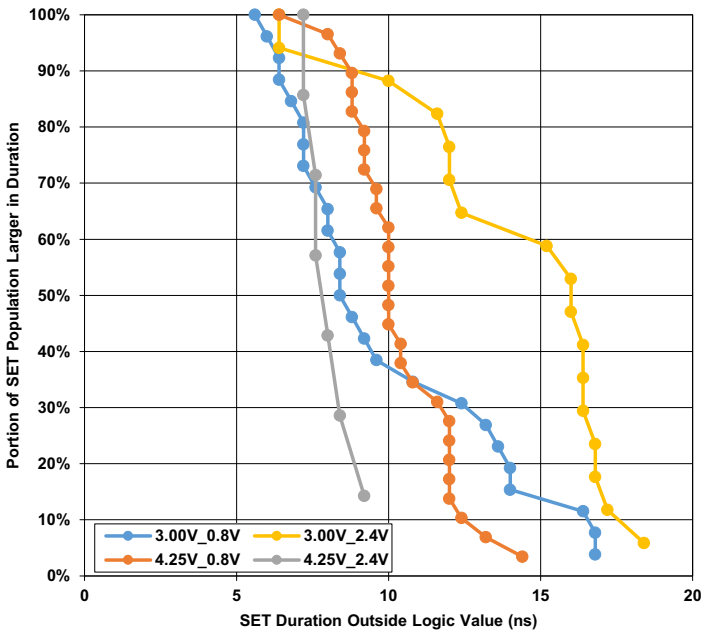


Figure 47. Plot of Cumulative SET Population Portion that is Above an Indicated SET Duration at LET 43MeV•cm^2/mg

The longest SET transient captured for the ISl71710M at 43MeV•cm^2/mg is presented in Figure 48. The twenty foot coaxial cable used to connect the oscilloscope to the buffer on the DUT induced considerable ringing that appears in Figure 48. No filtering was applied at the receiving end so as not to spread the initial events. The initial event in the figure is the sharp spike down that persists below 2.0V for 18.4ns. The smallest duration events

barely reached the 2.0V or 0.8 trigger levels and persisted for as little as 5.6ns. No significant difference was seen for either choice of V_{DD} (3.00V or 4.25V) or for the state of the output.

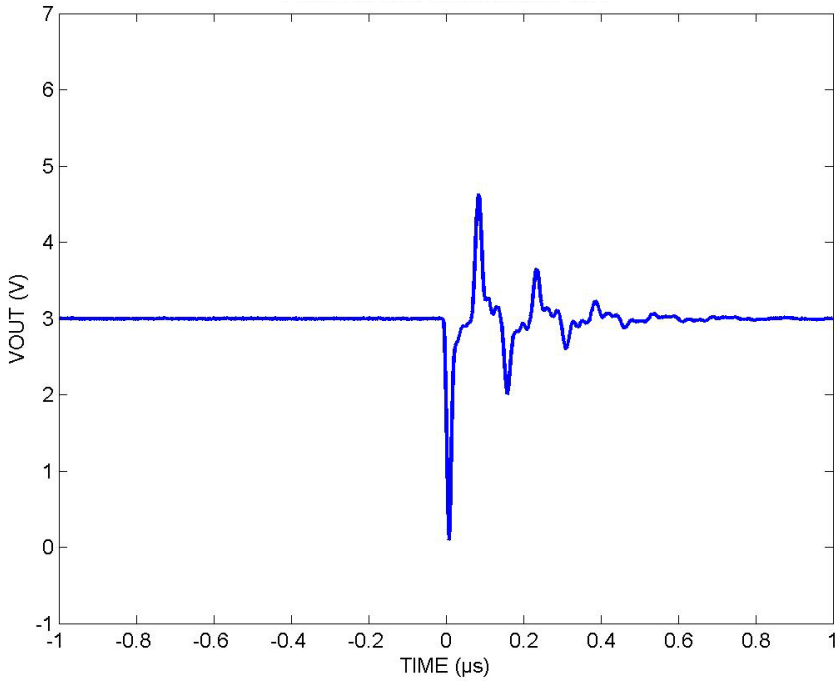


Figure 48. The SET of Extracted Duration of 18.4ns Below 2.0V in the First Impulse.

6.2.7 Summary

The ISL71710M common barrier isolation was immune to SEDR with normal incidence Ag for a LET of 43MeV•cm^2/mg to a fluence of 1x10^{7}ion/cm^2 at an isolation voltage of 500V.

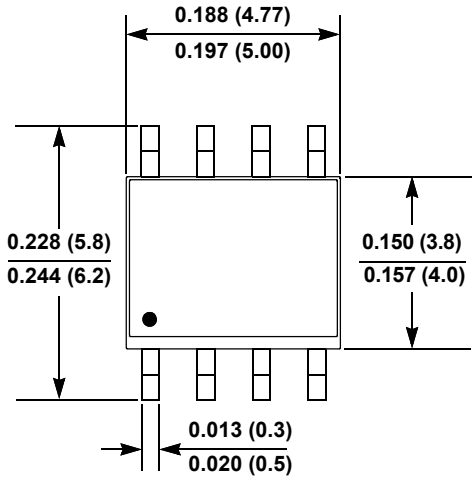
The ISL71710M circuitry was immune to SEL and SEB with normal incidence Ag for an LET of 43MeV•cm^2/mg to a fluence of 1x10^7 ion/cm^2 at a supply voltage of 7.0V.

The ISL71710M SET registered a maximum cross section of 130µm^2 at 43MeV•cm^2/mg. This occurred for a V_{DD} of 3.0V with a nominally high output and had a maximum duration of 18.4ns. At 8.5MeV•cm^2/mg the SET registered a maximum cross section of 80µm^2 with a maximum duration of 60ns. This is an unusual event in its length and magnitude. As can be seen in Figure 47 the bulk of the SET even at 43MeV•cm^2/mg were well below 20ns in duration.

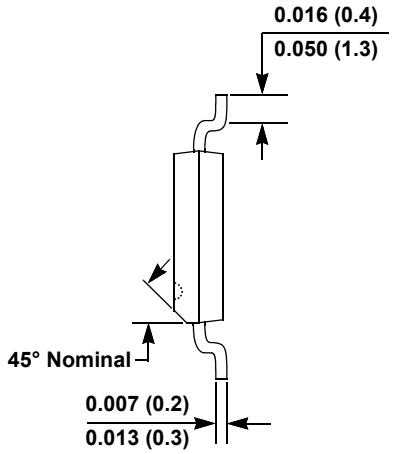
7. Package Outline Drawing

For the most recent package outline drawing, see M8.15G.

M8.15G
8 Lead Narrow Body Small Outline Plastic Package
Rev 2, 10/18

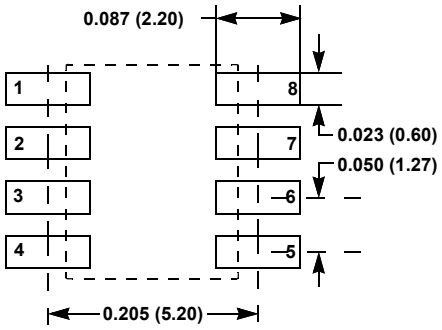


Top View



Side View

End View



Typical Recommended Land Pattern

Notes:
1. Dimensions in inches (mm); scale = approximately 5X.
2. Pin spacing is a BASIC dimension; tolerances do not accumulate.

8. Ordering Information

Ordering Part Number[1][2]	Part Marking	Radiation Lot Acceptance Testing	Package Description (RoHS Compliant)	Package Drawing	Carrier Type[3]	Temp. Range
ISL71710MBZ	71710 MBZ	N/A	8 Ld NSOIC	M8.15G	Tube	-55 to +125 (°C)
ISL71710MBZ-T					Reel, 2.5k	
ISL71710MBZ-T7A					Reel, 250	
ISL71710M30BZ		30krad(Si)	8 Ld NSOIC	M8.15G	Tube	-55 to +125 (°C)
ISL71710M30BZ-T					Reel, 2.5k	
ISL71710M30BZ-T7A					Reel, 250	
ISL71710M50BZ		50krad(Si)	8 Ld NSOIC	M8.15G	Tube	-55 to +125 (°C)
ISL71710M50BZ-T					Reel, 2.5k	
ISL71710M50BZ-T7A					Reel, 250	
ISL71610-710EV1Z	Evaluation Board					

1. These Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu-Ag plate-e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. For Moisture Sensitivity Level (MSL), see the ISL71710M product information page. For more information about MSL, see TB363.
3. Refer to TB347 for details about reel specifications.

9. Revision History

Revision	Date	Description
1.03	Feb 19, 2026	Added the Truth Table and Fail-Safe Resemblance sections.
1.02	Feb 4, 2026	Updated Signal Status on Start-Up section.
1.01	Mar 28, 2025	▪ Updated to the latest template. ▪ Updated Features bullets. ▪ Added ISL71710M30BZ and ISL71710M50BZ part information throughout document.
1.00	Mar 11, 2021	Updated Figure 34 “ISL71710M TID Biased Configuration” to connect Pin 2 (IN) to GND1, and Pin 3 (NC) floating.
0.00	Nov 9, 2018	Initial release

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