

# ISL71710SLHM

Radiation Hardened Active-Input High Speed Digital Isolator

The **ISL71710SLHM** is an active input digital signal isolator with CMOS output, using Giant Magnetoresistive (GMR) technology for small size, high speed, and low power. The ISL71710SLHM is the fastest isolator of its type, with a 150Mbps typical data rate. The symmetric magnetic coupling barrier provides a typical propagation delay of only 10ns and a pulse-width distortion as low as 0.3ns, achieving the best specifications of any isolator.

The ISL71710SLHM has unsurpassed common-mode transient immunity of 50kV/μs. It is ideal for isolating applications such as PROFIBUS, RS-485, and RS-422.

The ISL71710SLHM is offered in an 8 Ld 5mmx4mm SOIC package and is fully specified across the military ambient temperature range of -55°C to +125°C.

## Applications

- RS-485 and RS-422
- CAN bus/device net
- Multiplexed data transmission
- Data interfaces
- Ground loop elimination
- Peripheral interfaces
- Serial communication
- Logic level shifting
- Isolated power

## Features

- Electrically screened to VID [V62/23615](#)
- Barrier Voltage Endurance
  - 2.5kV<sub>RMS</sub> for 1 minute, 600V<sub>RMS</sub> continuous (VDE V 0884-10 certified: file 5022321-4880-0001)
  - 1.5kV<sub>DC</sub> continuous
  - 500V<sub>DC</sub> at 60MeV•cm<sup>2</sup>/mg SEDR
- Production testing and qualification follow the AS6294/1 standard (see [Radiation Hardened Plastic Production and QCI Flow](#))
- UL 1577 recognized: file reference E483309
- 5V/3.3V CMOS/TTL compatible
- High speed: 150Mbps typical
- 10ns typical propagation delay
- 300ps typical pulse-width distortion
- 4ns typical propagation delay skew
- 50kV/μs typical common-mode transient immunity
- Low EMI/RFI emissions
- Excellent magnetic immunity
- Passes NASA low outgassing specifications
- NiPdAu-Ag leadframes (Pb-free, Sn-free)
- Full military temperature range operation
  - T<sub>A</sub> = -55°C to +125°C
- TID Rad Hard Assurance (RHA) testing
  - Low Dose Rate (LDR) (0.01rad(Si)/s): 75krad(Si)
- SEE characterization
  - No DSEE with V<sub>DD</sub> = 6.5V at LET 86MeV•cm<sup>2</sup>/mg

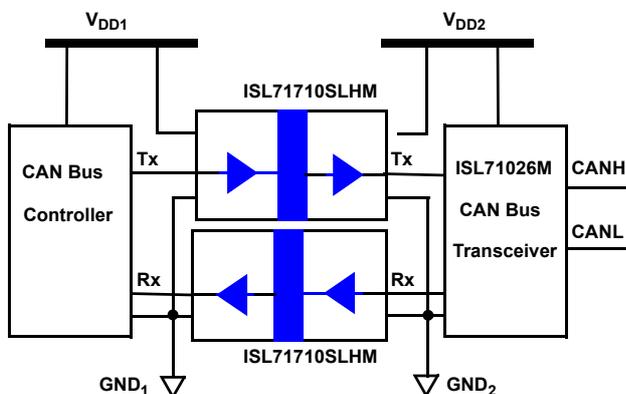


Figure 1. Typical CAN Bus Application

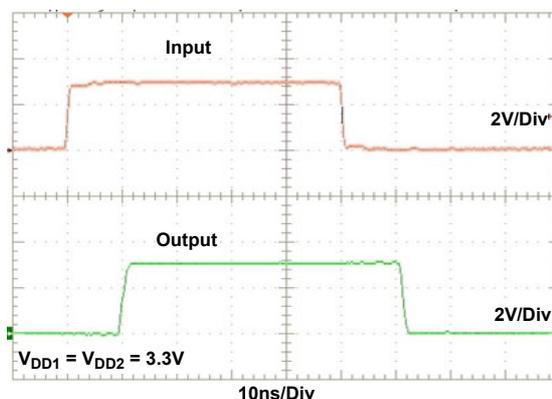


Figure 2. 10MHz Input and Output Waveforms

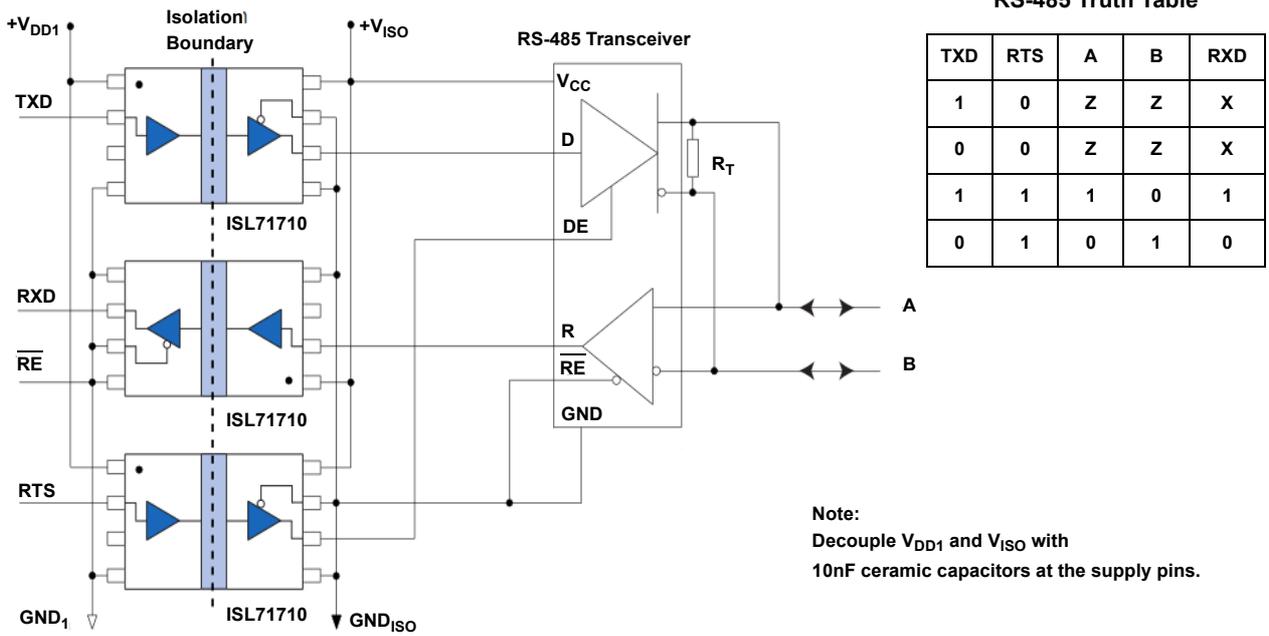


Figure 3. RS-485 Multi-Chip Isolated Transceiver Application Schematic

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# 1. Overview

## 1.1 Functional Block Diagram

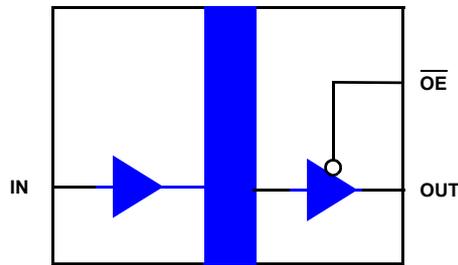
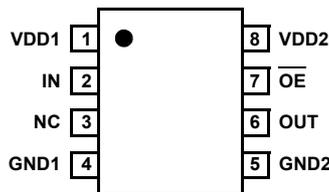


Figure 4. ISL71710SLHM Block Diagram

# 2. Pin Information

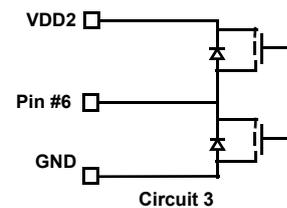
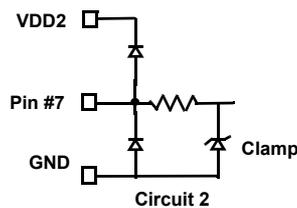
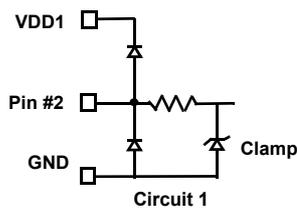
## 2.1 Pin Assignments



Top View

## 2.2 Pin Descriptions

Pin Number	Pin Name	ESD Circuit	Description
1	VDD1	N/A	Supply voltage
2	IN	1	Data in
3	NC	N/A	No internal connection. Leave this pin floating or connect it to VDD1 or GND1.
4	GND1	N/A	Ground return for VDD1
5	GND2	N/A	Ground return for VDD2
6	OUT	3	Data output
7	$\overline{OE}$	2	Output enable, active low. Internally pulled low with 100kΩ to enable the output when this pin is not connected.
8	VDD2	N/A	Supply voltage



### 3. Specifications

#### 3.1 Absolute Maximum Ratings

**CAUTION:** Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
Maximum Supply Voltage, VDD1 to GND1	-0.5	+7	V
Maximum Supply Voltage, VDD2 to GND2	-0.5	+7	V
In-Beam Maximum Supply Voltage VDD1 to GND1	-0.5	+7	V
In-Beam Maximum Supply Voltage VDD2 to GND2	-0.5	+7	V
IN Voltage	-0.5	$V_{DD1} + 0.5$	V
$\overline{OE}$ Voltage	-0.5	$V_{DD2} + 0.5$	V
OUT Voltage	-0.5	$V_{DD2} + 0.5$	V
Output Current Drive	-	10	mA
Human Body Model (Tested per AEC-Q100-002)	-	1.2	kV
Charge Device Model (Tested per AEC-Q100-011)	-	1.5	kV
Latch-up (Tested per JESD-78E; Class 2, Level A) at +125°C	-	100	mA

#### 3.2 Outgas Testing

Specification (Tested per ASTM E 595, 1.5)	Value	Unit
Total Mass Lost <sup>[1]</sup>	0.06	%
Collected Volatile Condensable Material <sup>[1]</sup>	<0.01	%
Water Vapor Recovered	0.03	%

1. Outgassing results meet NASA low requirements of total mass loss of <1% and collected volatile condensable material of <0.1%.

#### 3.3 Thermal Information

Thermal Resistance (Typical)	$\theta_{JA}$ (°C/W) <sup>[1]</sup>	$\theta_{JC}$ (°C/W) (Top)	$\theta_{JC}$ (°C/W) (Bottom)	$\Psi_{JT}$ (°C/W) <sup>[2]</sup>
8 Ld NSOIC Package	60	61	37	10

1.  $\theta_{JA}$  is measured with the component soldered to double-sided board; free air.

2. For  $\Psi_{JT}$  characterization parameter, the package top temperature is measured at the top center of the mounted package. See [TB379](#).

Parameter	Minimum	Maximum	Unit
Power Dissipation, $P_D$	-	675	mW
Maximum Junction Temperature	-	+150	°C
Storage Temperature Range	-65	+150	°C
Pb-Free Reflow Profile	See <a href="#">TB493</a>		

### 3.4 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Ambient Operating Temperature	-55	+125	°C
Supply Voltage $V_{DD1}$ , $V_{DD2}$	3.0	5.5	V
IN Logic High Voltage	2.4	$V_{DD1}$	V
IN Logic Low Voltage	0	0.8	V
$\overline{OE}$ Logic High Voltage	2.4	$V_{DD2}$	V
$\overline{OE}$ Logic Low Voltage	0	0.8	V
Input Signal Rise and Fall Time	-	1	$\mu$ s

### 3.5 Insulation Specifications

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Creepage Distance (external)	-	-	4.03	-	-	mm
Total Barrier Thickness (internal)	-	-	12	13	-	$\mu$ m
Leakage Current <sup>[1]</sup>	-	240V <sub>RMS</sub> , 60Hz	-	200	-	nA
Barrier Resistance <sup>[1]</sup>	$R_{IO}$	500V <sub>DC</sub>	-	>10 <sup>14</sup>	-	$\Omega$
Barrier Capacitance <sup>[1]</sup>	$C_{IO}$	1MHz	-	1.1	-	pF
Comparative Tracking Index	CTI	Per IEC:60112	≥175	-	-	V
Working Voltage	$V_{IORM}$	Per VDE V 0884-10, V084-11 pending	600	-	-	V <sub>RMS</sub>
Barrier Life	-	100°C, 1000V <sub>RMS</sub> , 60% Confidence Level activation energy	-	44000	-	Years

1. Device is considered a two terminal device: Pins 1-4 shorted and Pins 5-8 shorted.

### 3.6 Safety and Approvals

- VDE V 0884-10 (VDE V 0884-11 pending) (Basic Isolation; VDE File Number 5022321-4880-0001)
  - Working voltage ( $V_{IORM}$ ): 600V<sub>RMS</sub> (848V<sub>PK</sub>); basic insulation; pollution degree 2
  - Isolation voltage ( $V_{ISO}$ ): 2500V<sub>RMS</sub>
  - Transient overvoltage ( $V_{IOTM}$ ): 4000V<sub>PK</sub>
  - Surge rating: 4000V
  - Each part tested at 1590V<sub>PK</sub> for 1s, 5pC partial discharge limit
  - Samples tested at 4000V<sub>PK</sub> for 60s; then 1358V<sub>PK</sub> for 10s with 5pC partial discharge limit

Safety-Limiting Values	Symbol	Value	Unit
Safety Rating Ambient Temperature	$T_S$	+180	°C
Safety Rating Power	$P_S$	270	mW
Supply Current Safety Rating (Total of Supplies)	$I_S$	54	mA

- UL 1577 (Component Recognition Program File Number E483309)
  - Each part tested at 3000V<sub>RMS</sub> (4240V<sub>PK</sub>) for 1s; each lot sample tested at 2500V<sub>RMS</sub> (3530V<sub>PK</sub>) for 1min

### 3.7 Electrical Specifications

Unless otherwise noted,  $V_{DD1}$   $V_{DD2} = 3V - 5.5V$ ; OUT and  $\overline{OE}$  are open,  $V_{DD1}$  and  $V_{DD2}$  are bypassed to GND with a 47nF X7R capacitor;  $T_A = T_J = +25^\circ C$ . Limits apply across the operating temperature range,  $-55^\circ C$  to  $+125^\circ C$  unless otherwise stated.

Parameter	Symbol	Test Conditions	Min <sup>[1]</sup>	Typ	Max <sup>[1]</sup>	Unit
<b>3.3V Electrical Specifications</b>						
Input Quiescent Supply Current Figure 12	$I_{DD1}$	-	-	4	40	$\mu A$
		Post Radiation 75krad(Si)	-	2.6	2.8	mA
Output Quiescent Supply Current Figure 13	$I_{DD2}$	-	-	1.2	1.75	mA
Logic Input Current	$I_I$	-	-10	-	10	$\mu A$
Logic High Output Voltage Figure 20	$V_{OH}$	$I_O = -20\mu A, V_I = V_{IH}$	$V_{DD} - 0.1$	$V_{DD}$	-	V
		$I_O = -4mA, V_I = V_{IH}$	$0.8 \times V_{DD}$	$0.9 \times V_{DD}$	-	V
Logic Low Output Voltage Figure 21	$V_{OL}$	$I_O = 20\mu A, V_I = V_{IL}$	-	0	0.1	V
		$I_O = 4mA, V_I = V_{IL}$	-	0.5	0.8	V
<b>Switching Specifications (<math>V_{DD} = 3.3V</math>)</b>						
Maximum Data Rate		$C_L = 15pF$	130	140	-	Mbps
Pulse Width <sup>[2]</sup>	PW	50% Points, $V_O$	10	7.5	-	ns
Propagation Delay Input to Output (High-to-Low) Figure 14	$t_{PHL}$	$C_L = 15pF$	-	12	18	ns
Propagation Delay Input to Output (Low-to-High) Figure 15	$t_{PLH}$	$C_L = 15pF$	-	12	18	ns
Propagation Delay Enable to Output (High-to-High Impedance) Figure 22	$t_{PHZ}$	$C_L = 15pF$	-	3	7	ns
Propagation Delay Enable to Output (Low-to-High Impedance) Figure 23	$t_{PLZ}$	$C_L = 15pF$	-	3	7	ns
Propagation Delay Enable to Output (High Impedance-to-High) Figure 24	$t_{PZH}$	$C_L = 15pF$	-	3	7	ns
Propagation Delay Enable to Output (High Impedance-to-Low) Figure 25	$t_{PZL}$	$C_L = 15pF$	-	3	7	ns
Pulse-Width Distortion <sup>[3]</sup> Figure 18	PWD	$C_L = 15pF$	-	1	4	ns
Pulse Jitter <sup>[4]</sup>	$t_j$	$C_L = 15pF$	-	100		ps
Propagation Delay Skew <sup>[5]</sup>	$t_{PSK}$	$C_L = 15pF$	-	4	6	ns
Output Rise Time (10% to 90%) Figure 16	$t_R$	$C_L = 15pF$	-	2	5	ns
Output Fall Time (10% to 90%) Figure 17	$t_F$	$C_L = 15pF$	-	2	5	ns
Common-Mode Transient Immunity (Output Logic High or Logic Low) <sup>[6]</sup>	$ CM_H ,  CM_L $	$V_{CM} = 1500V_{DC}$ , $t_{TRANSIENT} = 25ns$	30	50	-	kV/ $\mu s$
Dynamic Power Consumption <sup>[7]</sup> , Figure 19	-	-	-	140	240	$\mu A/Mbps$
		Post Radiation 75krad(Si)	-	400	450	$\mu A/Mbps$
<b>Magnetic Field Immunity<sup>[8]</sup> (<math>V_{DD2} = 3V, 3V &lt; V_{DD1} &lt; 5.5V</math>)</b>						
Power Frequency Magnetic Immunity	$H_{PF}$	50Hz/60Hz	1000	1500	-	A/m
Pulse Magnetic Field Immunity	$H_{PM}$	$t_p = 8\mu s$	1800	2000	-	A/m

Unless otherwise noted,  $V_{DD1}$   $V_{DD2} = 3V - 5.5V$ ; OUT and  $\overline{OE}$  are open,  $V_{DD1}$  and  $V_{DD2}$  are bypassed to GND with a 47nF X7R capacitor;  $T_A = T_J = +25^\circ C$ . Limits apply across the operating temperature range,  $-55^\circ C$  to  $+125^\circ C$  unless otherwise stated. **(Cont.)**

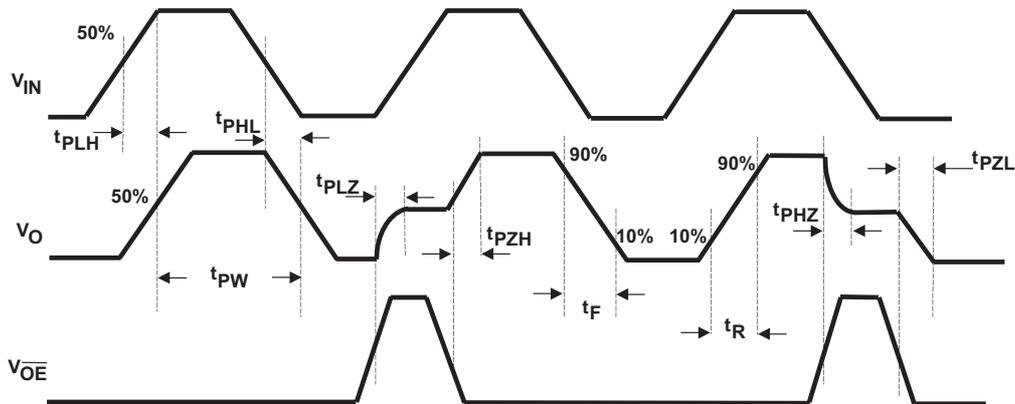
Parameter	Symbol	Test Conditions	Min <sup>[1]</sup>	Typ	Max <sup>[1]</sup>	Unit
Damped Oscillatory Magnetic Field	$H_{OSC}$	0.1Hz - 1MHz	1800	2000	-	A/m
Cross-Axis Immunity Multiplier <sup>[9]</sup>	$K_X$	-	-	2.5	-	-
<b>5V Electrical Specifications</b>						
Input Quiescent Supply Current Figure 12	$I_{DD1}$	-	-	6	75	$\mu A$
		Post Radiation 75krad(Si)	-	3	3.4	mA
Output Quiescent Supply Current Figure 13	$I_{DD2}$	-	-	1.8	2.5	mA
Logic Input Current	$I_I$	-	-10	-	10	$\mu A$
Logic High Output Voltage Figure 20	$V_{OH}$	$I_O = -20\mu A, V_I = V_{IH}$	$V_{DD} - 0.1$	$V_{DD}$	-	V
		$I_O = -4mA, V_I = V_{IH}$	$0.8 \times V_{DD}$	$0.9 \times V_{DD}$	-	V
Logic Low Output Voltage Figure 21	$V_{OL}$	$I_O = 20\mu A, V_I = V_{IL}$	-	0	0.1	V
		$I_O = 4mA, V_I = V_{IL}$	-	0.5	0.8	V
<b>Switching Specifications (<math>V_{DD} = 5V</math>)</b>						
Maximum Data Rate	-	$C_L = 15pF$	130	150	-	Mbps
Pulse Width <sup>[2]</sup>	PW	50% Points, $V_O$	10	7.5	-	ns
Propagation Delay Input to Output (High-to-Low) Figure 14	$t_{PHL}$	$C_L = 15pF$	-	10	16	ns
Propagation Delay Input to Output (Low-to-High) Figure 15	$t_{PLH}$	$C_L = 15pF$	-	10	16	ns
Propagation Delay Enable to Output (High-to-High Impedance) Figure 22	$t_{PHZ}$	$C_L = 15pF$	-	3	7	ns
Propagation Delay Enable to Output (Low-to-High Impedance) Figure 23	$t_{PLZ}$	$C_L = 15pF$	-	3	7	ns
Propagation Delay Enable to Output (High Impedance-to-High) Figure 24	$t_{PZH}$	$C_L = 15pF$	-	3	7	ns
Propagation Delay Enable to Output (High Impedance-to-Low) Figure 25	$t_{PZL}$	$C_L = 15pF$	-	3	7	ns
Pulse-Width Distortion <sup>[3]</sup> , Figure 18	PWD	$C_L = 15pF$	-	0.3	4	ns
Propagation Delay Skew <sup>[5]</sup>	$t_{PSK}$	$C_L = 15pF$	-	4	6	ns
Output Rise Time (10% to 90%) Figure 16	$t_R$	$C_L = 15pF$	-	1	4	ns
Output Fall Time (10% to 90%) Figure 17	$t_F$	$C_L = 15pF$	-	1	4	ns
Common Mode Transient Immunity (Output Logic High or Logic Low) <sup>[6]</sup>	$ CM_H ,  CM_L $	$V_{CM} = 1500V_{DC}$ , $t_{TRANSIENT} = 25ns$	30	50	-	kV/ $\mu s$
Dynamic Power Consumption <sup>[7]</sup> , Figure 19	-	-	-	200	340	$\mu A/Mbps$
		Post Radiation 75krad(Si)	-	480	530	$\mu A/Mbps$

Unless otherwise noted,  $V_{DD1}$   $V_{DD2} = 3V - 5.5V$ ; OUT and  $\overline{OE}$  are open,  $V_{DD1}$  and  $V_{DD2}$  are bypassed to GND with a 47nF X7R capacitor;  $T_A = T_J = +25^\circ C$ . Limits apply across the operating temperature range,  $-55^\circ C$  to  $+125^\circ C$  unless otherwise stated. **(Cont.)**

Parameter	Symbol	Test Conditions	Min <sup>[1]</sup>	Typ	Max <sup>[1]</sup>	Unit
<b>Magnetic Field Immunity<sup>[8]</sup> (<math>V_{DD2} = 5V, 3V &lt; V_{DD1} &lt; 5.5V</math>)</b>						
Power Frequency Magnetic Immunity	$H_{PF}$	50Hz/60Hz	2800	3500	-	A/m
Pulse Magnetic Field Immunity	$H_{PM}$	$t_p = 8\mu s$	4000	4500	-	A/m
Damped Oscillatory Magnetic Field	$H_{OSC}$	0.1Hz - 1MHz	4000	4500	-	A/m
Cross-axis Immunity Multiplier <sup>[9]</sup>	$K_X$	-	-	2.5	-	-

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.
2. Minimum pulse width is the minimum value at which specified PWD is ensured.
3. PWD is defined as  $|t_{PHL} - t_{PLH}|$ . %PWD is equal to PWD divided by pulse width.
4. 66535-bit pseudo-random binary signal (PRBS) NRZ bit pattern with no more than five consecutive 1s or 0s; 800ps transition time.
5.  $t_{PSK}$  is the magnitude of the worst-case difference in  $t_{PHL}$  and/or  $t_{PLH}$  between devices at  $+25^\circ C$ .
6.  $CM_H$  is the maximum common-mode voltage slew rate that can be sustained while maintaining  $V_O > 0.8 V_{DD2}$ . CML is the maximum common-mode input voltage that can be sustained while maintaining  $V_O < 0.8V$ . The common-mode voltage slew rate apply to both rising and falling common-mode voltage edges.
7. Dynamic power consumption is calculated per channel and is supplied by the input side power supply of the channel.
8. The relevant test and measurement methods are given in [Electromagnetic Compatibility](#).
9. External magnetic field immunity is improved by this factor if the field direction is end-to-end rather than pin-to-pin (see [Figure 26](#)).

### 3.8 Timing Diagram



**Legend**

$t_{PLH}$	Propagation Delay, Low-to-High
$t_{PHL}$	Propagation Delay, High-to-Low
$t_{PW}$	Minimum Pulse Width
$t_{PLZ}$	Propagation Delay, Low-to-High Impedance
$t_{PZH}$	Propagation Delay, High Impedance-to-High
$t_{PHZ}$	Propagation Delay, High-to-High Impedance
$t_{PZL}$	Propagation Delay, High Impedance-to-Low
$t_R$	Rise Time
$t_F$	Fall Time

Figure 5. Timing Diagram

## 4. Typical Performance Curves

$T_A = +25^\circ\text{C}$ , unless otherwise specified.

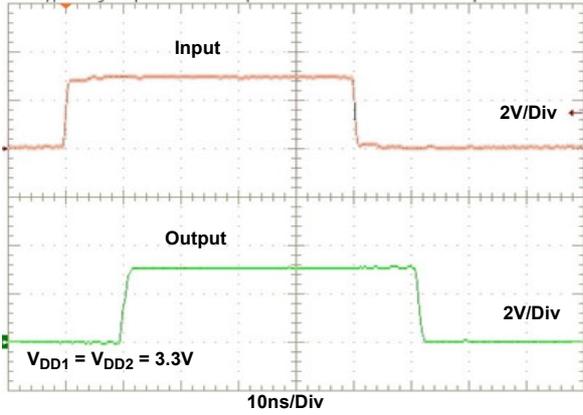


Figure 6. 10MHz Input and Output Waveforms

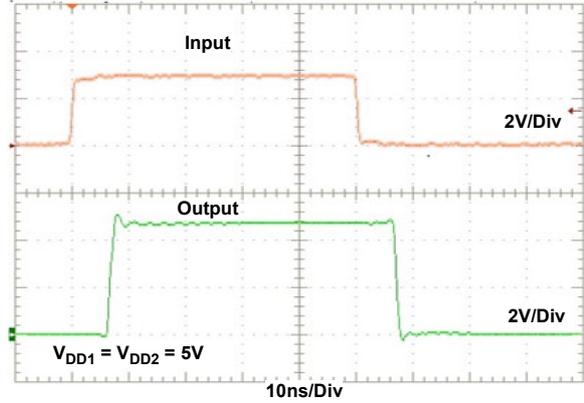


Figure 7. 10MHz Input and Output Waveforms

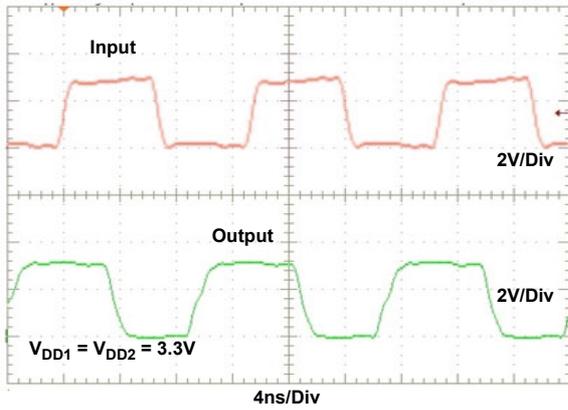


Figure 8. 75MHz Input and Output Waveforms

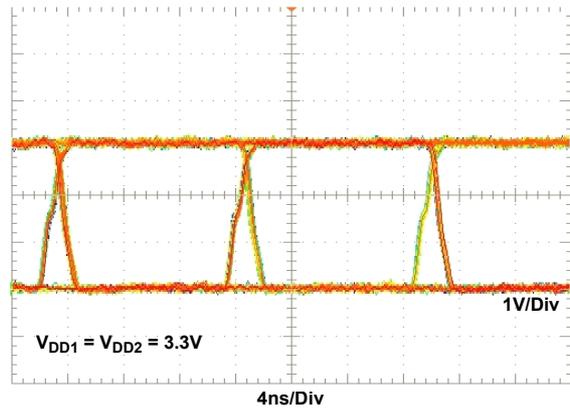


Figure 9. 75Mbps Eye Diagram

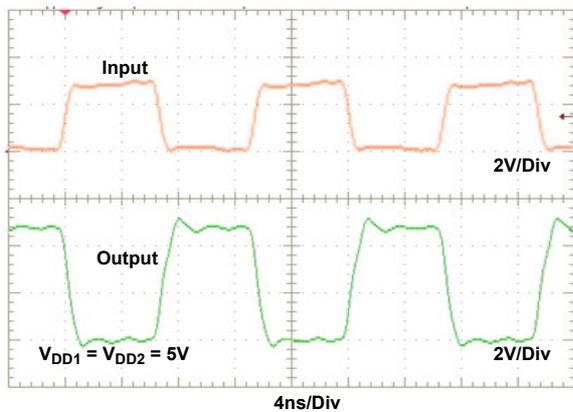


Figure 10. 75MHz Input and Output Waveforms

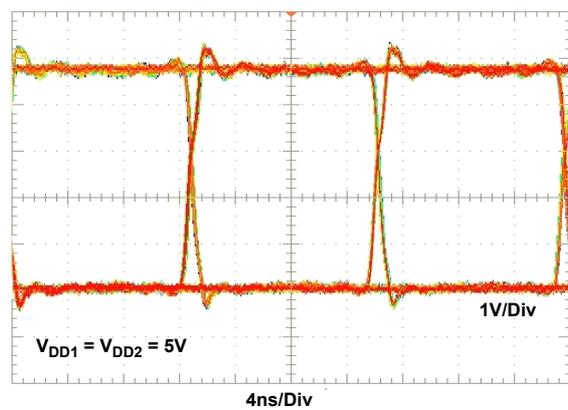


Figure 11. 75Mbps Eye Diagram

T<sub>A</sub> = +25°C, unless otherwise specified. (Cont.)

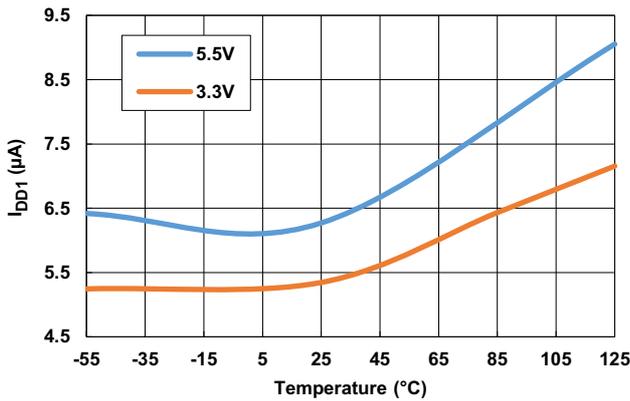


Figure 12. Input Quiescent Supply Current vs Temperature vs V<sub>DD1</sub> Voltage

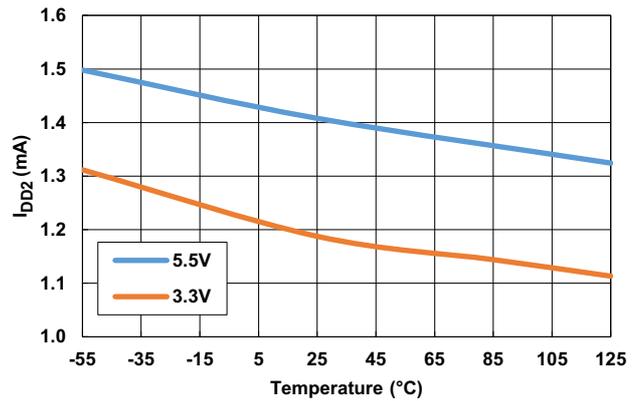


Figure 13. Output Quiescent Supply Current vs Temperature vs V<sub>DD2</sub> Voltage

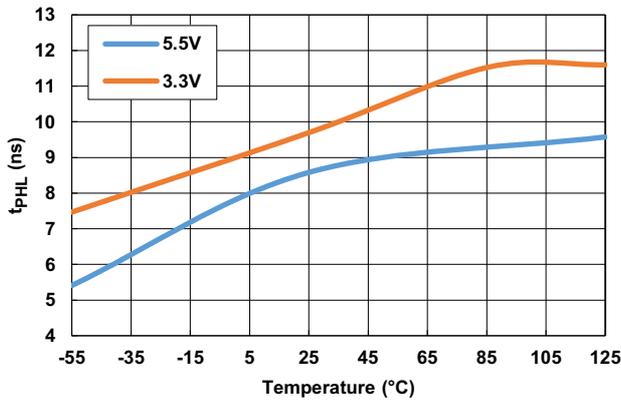


Figure 14. Propagation Delay (High-to-Low) vs Temperature vs V<sub>DD</sub> Voltage

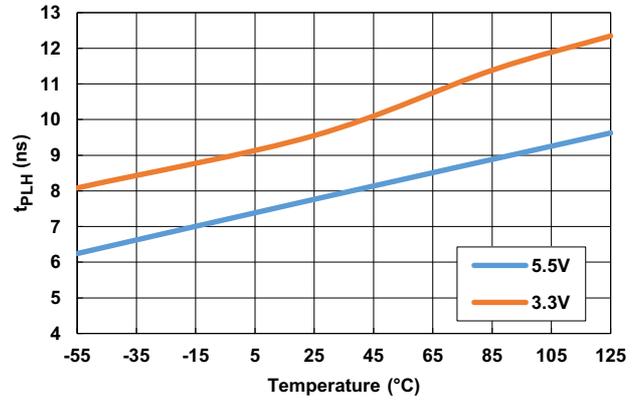


Figure 15. Propagation Delay (Low-to-High) vs Temperature vs V<sub>DD</sub> Voltage

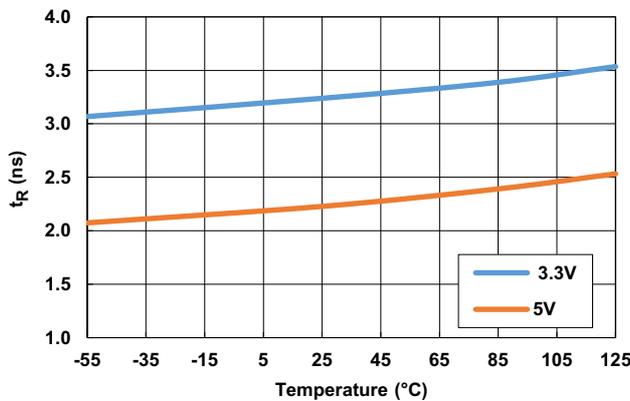


Figure 16. Output Rise Time vs Temperature vs V<sub>DD</sub> Voltage

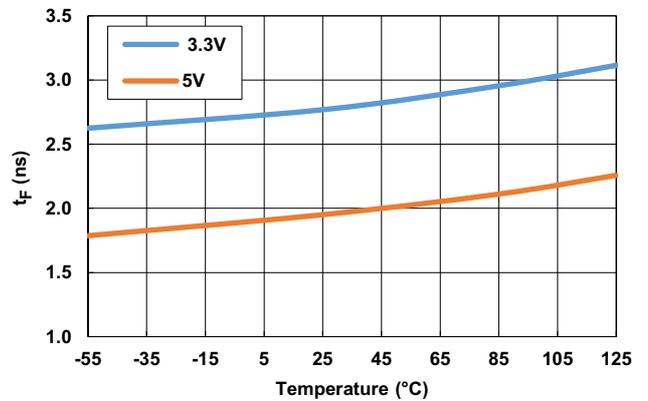


Figure 17. Output Fall Time vs Temperature vs V<sub>DD</sub> Voltage

T<sub>A</sub> = +25°C, unless otherwise specified. (Cont.)

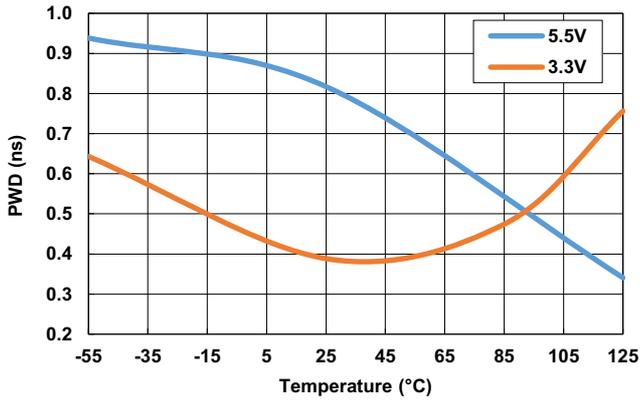


Figure 18. 5.5V Pulse-Width Distortion vs Temperature vs V<sub>DD</sub> Voltage

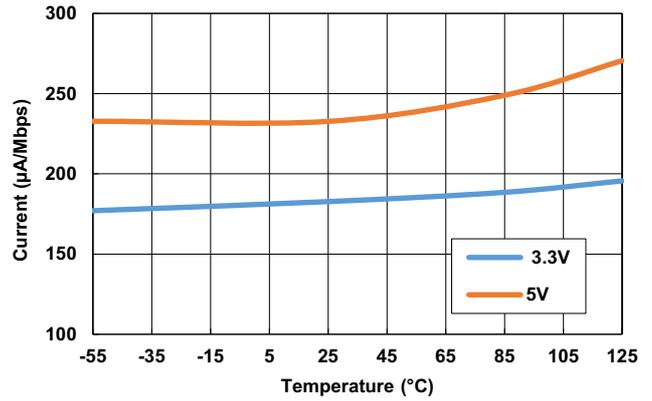


Figure 19. Dynamic Power Consumption vs Temperature

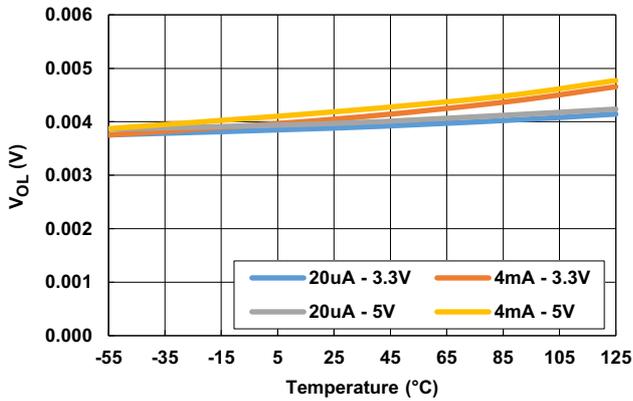


Figure 20. Logic Low Output Voltage vs Temperature

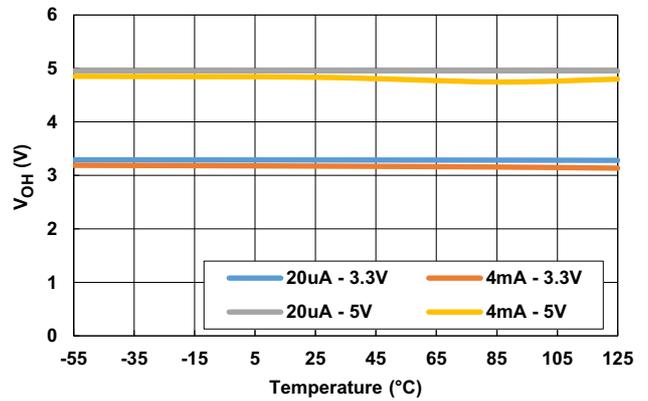


Figure 21. Logic High Output Voltage vs Temperature

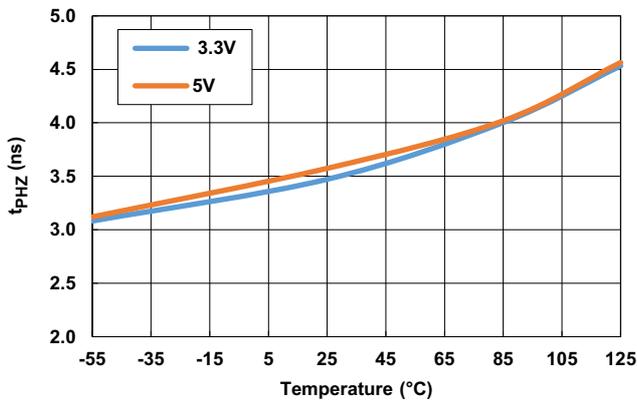


Figure 22. Propagation Delay Enable to Output (High-to-High Impedance) vs Temperature

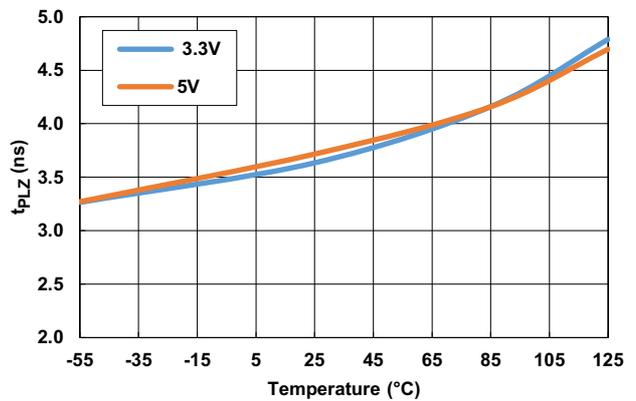


Figure 23. Propagation Delay Enable to Output (Low-to-High Impedance) vs Temperature

T<sub>A</sub> = +25°C, unless otherwise specified. (Cont.)

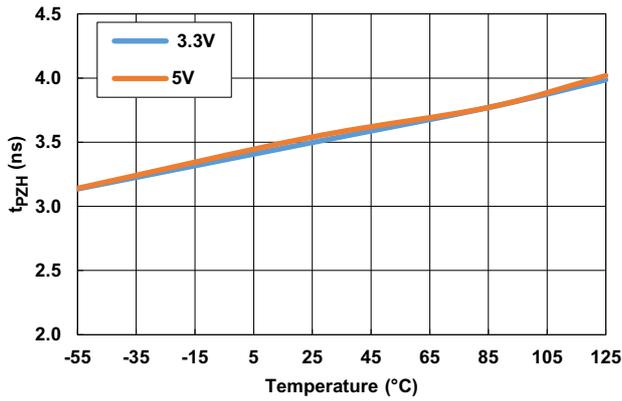


Figure 24. Propagation Delay Enable to Output (High Impedance-to-High) vs Temperature

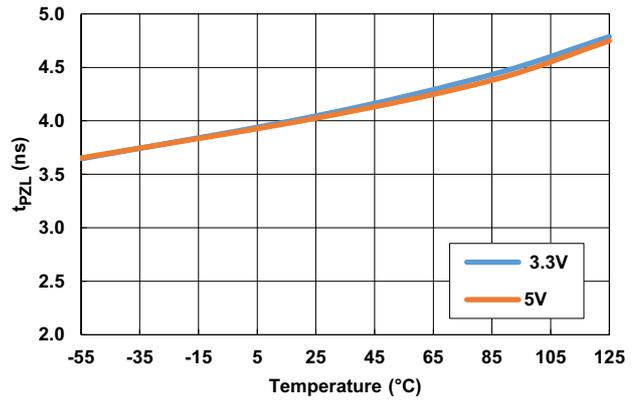


Figure 25. Propagation Delay Enable to Output (High Impedance-to-Low) vs Temperature

## 5. Device Information

### 5.1 Electrostatic Discharge Sensitivity

This product has been tested for electrostatic sensitivity to the limits stated in [Absolute Maximum Ratings](#). However, Renesas recommends that all integrated circuits are handled with appropriate care to avoid damage. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.

### 5.2 Electromagnetic Compatibility

The ISL71710SLHM has the lowest EMC footprint of any isolation technology. Its Wheatstone bridge configuration and differential magnetic field signaling ensure excellent EMC performance against all relevant standards.

Immunity to external magnetic fields is even higher if the field direction is end-to-end rather than pin-to-pin as shown in [Figure 26](#):

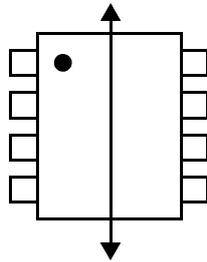


Figure 26. Cross-Axis Field Direction

### 5.3 Dynamic Power Consumption

The ISL71710SLHM achieves its low power consumption from the way it transmits data across the isolation barrier. By detecting the edge transitions of the input logic signal and converting these to narrow current pulses, a magnetic field is created around the GMR Wheatstone bridge. Depending on the direction of the magnetic field, the bridge causes the output comparator to switch following the input logic signal. The power consumption is independent of mark-to-space ratio and solely dependent on frequency, because the current pulses are narrow, about 2.5ns. This has obvious advantages over optocouplers, which have power consumption heavily dependent on mark-to-space ratio.

### 5.4 Power Supply Decoupling

Decouple both power supplies to this device with low ESR 47nF ceramic capacitors. Ground planes for both GND1 and GND2 are highly recommended for data rates above 10Mbps. Capacitors must be located as close as possible to the VDD pins.

### 5.5 Signal Status on Start-Up

To minimize power dissipation, input signals are differentiated and then per GMR technology magnetically latched on the output side of the isolation barrier. Here, the latched state of the GMR resistor bridge on the isolator's secondary side is independent of the secondary supply,  $V_{DD2}$ . Applying  $V_{DD2}$  only enables the comparator to detect the GMR bridge voltage and to reconstruct the output signal electrically.

Magnetic latching has the advantage that the magnetic state of the GMR bridge remains, even during a loss of  $V_{DD2}$ . However, it can also lead to an indeterminate output state after power-up, shutdown, and power loss sequencing events.

To ensure that the isolator is in a known output state, the input signal must be EXOR-ed with a sync-pulse (see Figure 27). Here, the required output state after power-up is defined by the logic state of EXOR input A. When  $V_{DD1}$  is fully established, applying a sync-pulse (low – high – low) to EXOR input B causes a pulse at the isolator input (IN). This latches the logic state at input A into the GMR bridge across the barrier. *Note:* The pulse width at IN must be  $\geq 10\text{ns}$ . After the application of the sync pulse, powering up  $V_{DD2}$ , the isolator output assumes the required output state.

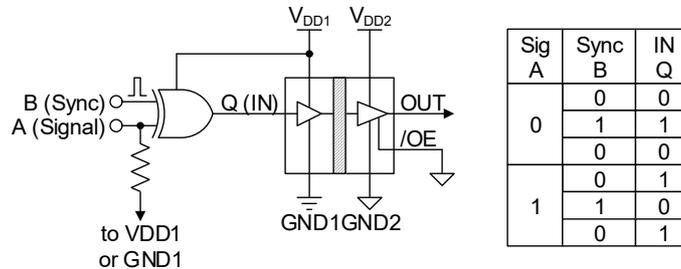


Figure 27. Sync Circuit with EXOR Truth Table

Complete the following supply sequencing steps to ensure the output starts in a known output state:

1. Start with  $V_{DD1}$ ,  $V_{DD2}$ , and  $/OE$  being at  $0V$ .
2. Apply  $V_{DD1}$ .
3. After  $V_{DD1}$  is fully established, apply the sync-pulse at input B. Ensure that the pulse width at IN is  $\geq 10\text{ns}$ .
4. Apply  $V_{DD2}$ . Observe that  $V_{OUT}$  starts in the state set by input A.

## 5.6 Data Transmission Rates

The reliability of a transmission system is directly related to the accuracy and quality of the transmitted digital information. For a digital system, parameters that determine the limits of the data transmission are pulse-width distortion and propagation delay skew.

Propagation delay is the time taken for the signal to travel through the device. This is usually different when sending a low-to-high signal than when sending a high-to-low signal. This difference, or error, is called Pulse-Width Distortion (PWD) and is usually in nanoseconds. It may also be expressed as a percentage:

- $\text{PWD}\% = [\text{Maximum Pulse-Width Distortion (ns)} / \text{Signal Pulse Width (ns)}] \times 100\%$

For example, with data rates of 12.5Mbps:

- $\text{PWD}\% = [3\text{ns}/80\text{ns}] \times 100\% = 3.75\%$

This figure is almost three times better than any available optocoupler with the same temperature range, and two times better than any optocoupler regardless of published temperature range. The ISL71710SLHM exceeds the 10% maximum PWD recommended by PROFIBUS, and runs to nearly 35Mbps within the 10% limit.

Propagation delay skew is the signal propagation difference between two or more channels. This becomes significant in clocked systems because it is undesirable for the clock pulse to arrive before the data has settled. Short propagation delay skew is therefore especially critical in high data rate parallel systems for establishing and maintaining accuracy and repeatability. Worst-case channel-to-channel skew in an ISL71710SLHM isolator is only 4ns, which is ten times better than any optocoupler. ISL71710SLHM isolators have a maximum propagation delay skew of 6ns, which is five times better than any optocoupler.

## 5.7 Truth Table

Table 1 displays the ISL71710M truth table.

Table 1. Truth Table

IN	VDD1	GMR	VDD2	$\overline{OE}$	OUT
H	Powered	H	Powered	L	H
L	Powered	L	Powered	L	L
X	Powered	X	Powered	H	Z
X	Unpowered	indeterminate	Powered	L	indeterminate
X	Unpowered	indeterminate	Powered	H	Z
X	X	X	Unpowered	X	$Z_{wk}^{[1]}$

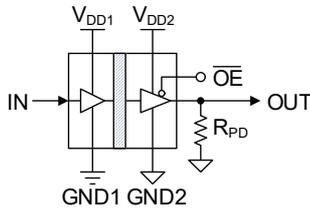
1. A weak high-impedance state can occur under the following conditions:

If VDD2 is floating, the output transistors are usually turned off, resulting in a high-impedance state, but parasitic body diodes may still conduct. Leakage currents through these diodes can cause the OUT pin to float at an undefined voltage. Therefore, despite being in a high-impedance state, the OUT pin is not truly disconnected, especially if other signals are still driving the output while its supply is floating. This might violate input voltage ratings and potentially inject current into the unpowered circuit. Hence, a floating VDD2 turns the push-pull output into an uncontrolled high-impedance state rather than a clean, open-circuit high-impedance state.

If VDD2 is grounded (0V), the ESD protection diodes clamp the output to VDD2 (0V). Any voltage applied to the output cannot rise above 0.7V; therefore, creating a low-impedance, power-consuming path.

## 5.8 Fail-Safe Resemblance

As the ISL71710M has no inherent fail-safe state. One method to achieve a defined output state (preferable Low) when VDD1 is lost is by disabling the output ( $\overline{OE} = \text{High}$ ) and pulling it low with a pull-down resistor (Figure 28).



IN	VDD1	VDD2	$\overline{OE}$	OUT
H	Powered	Powered	L	H
L	Powered	Powered	L	L
X	Powered	Powered	H	$L_{pd}^{[1]}$
X	X	Unpowered	X	$L_{pd}^{[1]}$
X	Unpowered	Powered	L	Indeterminate
X	Unpowered	Powered	H	$L_{pd}^{[1]}$

1. Pull-Down Low

Figure 28. Fail-Safe Low Resemblance with Modified Output and Corresponding Truth Table

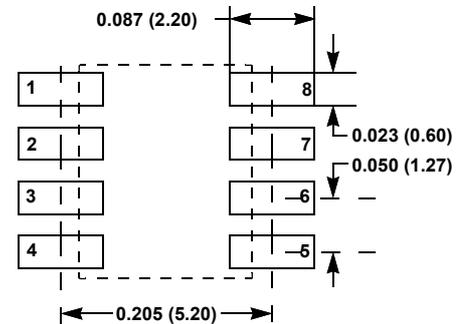
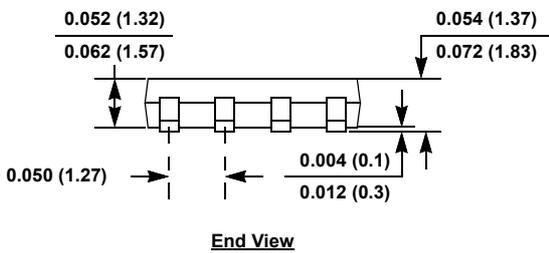
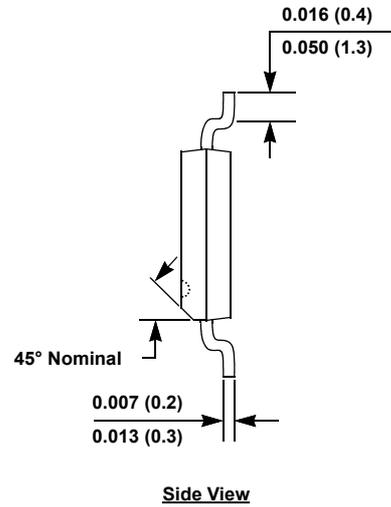
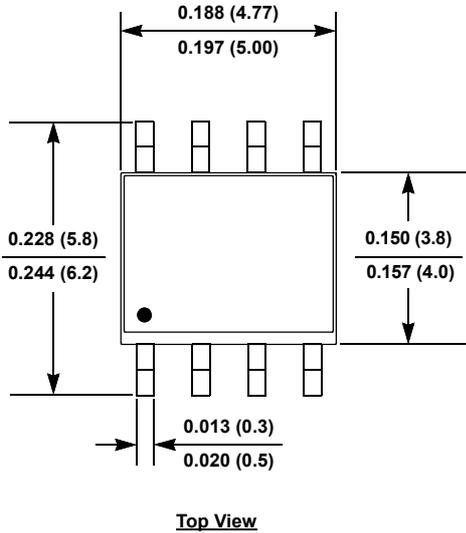
The truth table in Figure 28 shows that if VDD2 is lost, the output  $Z_{wk}$  state is turned into a defined  $L_{pd}$  state. If VDD1 is lost while the output driver is active, OUT can still be high or low and is therefore indeterminate. To achieve a defined low,  $\overline{OE}$  must be asserted high.

## 6. Package Outline Drawing

For the most recent package outline drawing, see [M8.15G](#).

M8.15G

8 Lead Narrow Body Small Outline Plastic Package  
Rev 2, 10/18



Typical Recommended Land Pattern

Notes:

1. Dimensions in inches (mm); scale = approximately 5X.
2. Pin spacing is a BASIC dimension; tolerances do not accumulate.

## 7. Ordering Information

Part Number <sup>[1][2]</sup>	Part Marking	Radiation Tolerance (Total Ionizing Dose)	Package Description (RoHS Compliant)	Pkg. Dwg #	Carrier Type	Temp. Range
ISL71710SLHMBZ	71710MBZ	LDR to 75krad(Si)	8 Ld NSOIC	<a href="#">M8.15G</a>	Tray	-55 to +125°C
ISL71610-710EV1Z	Evaluation Board					

1. These Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu-Ag plate-e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. For Moisture Sensitivity Level (MSL), see the Product Options on the [ISL71710SLHM](#) product page (click the packaging icon). For more information about MSL, see [TB363](#).

## 8. Revision History

Revision	Date	Description
1.03	Feb 19, 2026	Added the Truth Table and Fail-Safe Resemblance sections.
1.02	Feb 4, 2026	Updated Signal Status on Start-Up section.
1.01	Dec 1, 2023	Updated Features section.
1.00	Jul 26, 2021	Initial release

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