

ISL71934M

Radiation Tolerant SP2T RF Switch, 50MHz to 10GHz

Description

The ISL71934M is a high reliability, low insertion loss, 50Ω SP2T absorptive RF switch designed for a multitude of wireless and other RF applications. This device covers a broad frequency range from 50MHz to 10GHz. In addition to providing low insertion loss, the ISL71934M delivers high linearity and high isolation performance while providing a 50Ω termination to the unused RF input port.

The ISL71934M uses a single positive supply voltage of 2.7V to 5.25V supporting three states using either 3.3V or 1.8V control logic.

Competitive Advantage

The ISL71934M provides the following advantages:

- Constant impedance K_{|Z|} during switching transition
- Insertion loss = 0.7dB (at 2GHz)
- RFX to RFC isolation = 71dB (at 1GHz)
- IIP3 = +64dBm (at 1GHz)
- Active port operating power handling = 34dBm
- Term port operating power handling = 27dBm

Applications

- · Satellite communications system
- Antenna switching
- IF switching
- Digital pre-distortion feedback

Features

- Qualified to Renesas Rad Tolerant Screening and QCI Flow (R34TB0004EU)
- · High isolation:
 - 71dB at 1GHz
 - 60dB at 4GHz
- High linearity:
 - IIP2 of 111dBm
 - · IIP3 of 64dBm at 1GHz
- Wide single 2.75V to 5.25V supply voltage range
- 3.3V and 1.8V compatible control logic
- Operating temperature: -55°C to +125°C
- 3x3mm 16-TQFN package
- Ni/Pd/Au lead finish (Tin (Sn)-free)
- TID Characterization (LDR: ≤10mrad(Si)/s): 30krad(Si)
- SEE Characterization
 - No DSEE with VDD = 6.2V at 43MeV•cm²/mg
 - SET <10ns with F_{RF} = 10MHz at 43MeV•cm²/mg
- Manufactured using SOI wafer fab process

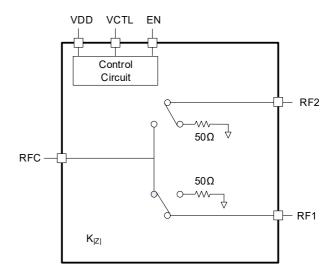


Figure 1. Block Diagram

Contents

1.	Pin In	nformatio	n	3
	1.1	Pin Ass	signments	3
	1.2	Pin Des	scriptions	3
2.	Speci	ifications		4
	2.1	Absolut	te Maximum Ratings	4
	2.2	Therma	al Information	4
	2.3	Recom	mended Operating Conditions	5
	2.4	Electric	cal Specifications	6
	2.5	Control	Mode	8
3.	Typic	al Perforr	mance Graphs	9
4.	Appli	cations Ir	nformation	11
	4.1	Default	Start-up	11
	4.2	Logic C	Control	11
	4.3	Power:	Supplies	11
	4.4	Control	l Pin Interface	11
5.	Radia	tion Tole	rance	12
	5.1	Total lo	nizing Dose (TID) Testing	12
		5.1.1	Introduction	12
		5.1.2	TID Results	13
	5.2	Single-	Event Effects Testing	14
		5.2.1	SEE Test Facility	14
		5.2.2	SEE Test Setup	14
		5.2.3	Single Event Burnout and Latch-Up (SEB/L) Results	14
		5.2.4	SET Results	14
		5.2.5	Conclusion	14
6.	Packa	age Outlir	ne Drawing	15
7.	Orde	ring Infori	mation	17
8.	Revis	ion Histo	ory	17



1. Pin Information

1.1 Pin Assignments

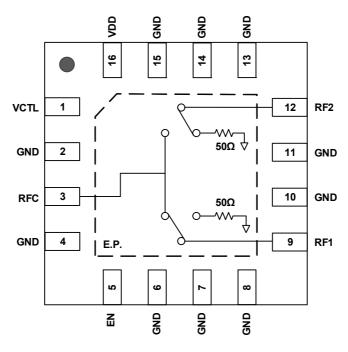


Figure 2. Pin Assignments - Top View

1.2 Pin Descriptions

Pin	Name	Function
1	VCTL	Controls the selected path when EN is low. It is disabled when EN is logic high (see Absolute Maximum Ratings). <i>Note</i> : VDD must be applied before or concurrently to voltage being applied to this pin.
I 3 I REC I		RF Common Port. Matched to 50Ω when one of the two RF ports is selected. <i>Note</i> : If this pin is not 0V DC, an external coupling capacitor must be used.
2, 4, 6, 7, 8, 10, 11, 13, 14, 15	GND	Ground. Also, internally connected to the ground paddle. Ground this pin as close to the device as possible.
5	EN	EN as a logic low allows VCTL to control the selected switch path. With EN set to logic high puts the part in all paths off state and disables the control of VCTL (Absolute Maximum Ratings). Note: VDD must be applied before or concurrently to voltage being applied to this pin.
9	RF1	RF1 Port. Matched to 50Ω . <i>Note</i> : If this pin is not 0V DC, an external coupling capacitor must be used.
12	RF2	RF2 Port. Matched to 50Ω . <i>Note</i> : If this pin is not 0V DC, an external coupling capacitor must be used.
16	VDD	Power Supply. Bypass to GND with capacitors shown in the Typical Application Circuit as close as possible to pin.
	EP	Exposed Pad. Internally connected to GND. Solder this exposed pad to a PCB pad that uses multiple ground vias to provide heat transfer out of the device and into the PCB ground planes. These multiple ground vias are also required to achieve the specified RF performance.



2. Specifications

2.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Paran	neter/Condition	Symbol	Minimum	Maximum	Unit
VDD to GND		V_{DD}	-0.3	+5.5	V
VCTL, EN to GND		V _{logic}	-0.3	3.6	V
RF1, RF2, RFC to GND		V_{RF}	-0.3	+0.3	V
	RF1 or RF2 as an input (Connected to RFC)	P _{RF12}	-	36	dBm
	RFC as an input (Connected to RF1 or RF2)	P _{RFC}	-	36	dBm
RF Input Power ^[1]	RFC as an input (All off state)	P _{RFC_OFF}	-	30	dBm
	RF1 or RF2 as input (Terminated states)		-	30	dBm
	RF1 and RF2 as inputs (All off state)	P _{RF12_OFF}	-	30[2]	dBm
Human Body Model (Tested p	V _{ESDHBM}	-	1.5	kV	
Charged Device Model (Teste	V _{ESDCDM}	-	2	kV	

^{1.} V_{DD} = 2.7V to 5.25V, 250MHz \leq F_{RF} \leq 10GHz, T_C = 105°C, Z_S = Z_L = 50 Ω .

2.2 Thermal Information

Thermal Resistance (Typical)	θ _{JA} (°C/W) ^[1]	θ _{JC} (°C/W) ^[2]	
16 Ld TQFN	59	17	

^{1.} θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.

^{2.} For θ_{JC} , the case temperature location is the center of the exposed metal pad on the package underside.

Parameter	Minimum	Maximum	Unit	
Maximum Junction Temperature (T _{JMAX})		+125	°C	
Storage Temperature Range (T _{ST})	-65	+150	°C	
Pb-Free Reflow Profile	See TB493			



^{2.} Each port.

2.3 Recommended Operating Conditions

Parameter	Symbol	Condition		Minimum	Typical	Maximum	Units
Supply Voltage	V_{DD}	-		2.7	-	5.25	V
Operating Temperature Range	T _{CASE}	Exposed Paddle Temp	erature	-55	-	+125	°C
RF Frequency Range	F _{RF}	-		0.05	-	10	GHz
		RFC connected to RF1	or RF2 ^[2]	-	-	34	dBm
RF Continuous Input CW Power (Non-Switched) ^[1]	P_{RF}	RF1/ RF2 Input, Termin	nated State ^{[3][4]}	-	-	27	dBm
(RFC Input, All off State		-	-	27	dBm
		RFC Input, switching	T _C = 85 °C	-	-	30	dBm
		between RF1 and RF2.	T _C = 105 °C	-	-	30	dBm
		RFC Input, switching into or out of, All off State.	T _C = 85 °C	-	-	27	dBm
RF Continuous Input Power			T _C = 105 °C	-	-	27	dBm
(RF Hot Switching CW) ^[1]	P _{RFSW}	PRFSW RF1 or RF2 as input, switched between RFC and Term.	T _C = 85 °C	-		27	dBm
			T _C = 105 °C	-	-	27	dBm
		RF1 and RF2 as	T _C = 85 °C	-	-	27	dBm
		inputs, switching into or out of All off State. ^[4]	T _C = 105 °C	-	-	27	dBm
RF1/2 Port Impedance	Z _{RFx}	-	•	-	50	-	Ω
RFC Port Impedance	Z _{RFC}	-		-	50	-	Ω

- 1. Levels based on: V_{DD} = 3.1V to 5.25V, 250MHz \leq F_{RF} \leq 10GHz, Z_{S} = Z_{L} = 50 Ω . See Figure 3 for power handling derating vs. RF frequency.
- 2. Input could be: RFC, RF1, or RF2 (applied to only one input).
- 3. Any RF1 / RF2 termination state. Power level specified is for each port.
- 4. Power level specified is for each port.

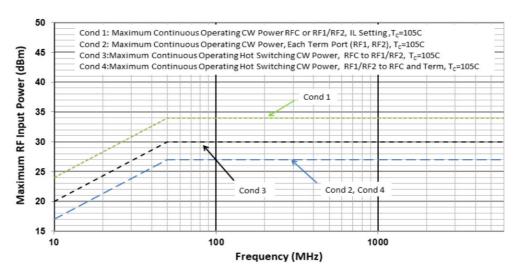


Figure 3. Maximum RF Input Operating Power vs. Frequency

2.4 Electrical Specifications

Typical Application Circuit, V_{DD} = 5.0V, T_{C} = +25°C, F_{RF} = 2000MHz, Driven Port = RF1 or RF2, input power = 0dBm, ZS = ZL = 50 Ω , PCB board trace and connector losses are de-embedded unless otherwise noted. **Boldface limits apply across the operating temperature range**, -55°C to +125°C by characterization with production testing at +25°C.

Parameter	Symbol	Condition	Minimum ^{[1][2]}	Typical	Maximum ^{[1][2]}	Units
Logic Input High Threshold	V _{IH}		1.1	-	3.6	V
Logic Input Low Threshold	V _{IL}		-0.3	-	0.6	V
Logic Current	I _{IH} , I _{IL}	For each control pin	-1	-	+1	μA
DC Current	1	V _{DD} = 3.3 V	-	200	400	μΑ
DO Guiterii	I _{DD}	V _{DD} = 5.0 V	-	260	450	μΑ
		50MHz	-	0.7	-	dB
		1GHz	-	0.7	-	dB
		2GHz	-	0.7	1.1	dB
Insertion Loss	IL	3GHz	-	0.7	-	dB
RFC to RF1 / RF2		4GHz	-	0.7	-	dB
		6GHz	-	0.8	-	dB
		8GHz	-	1.0	-	dB
		10GHz	-	1.2	-	dB
		50MHz	76	79	-	dB
	ISOC	1GHz	67	71	-	dB
		2GHz	62	66	-	dB
Isolation		3GHz	61	64	-	dB
RFC to RF1 / RF2		4GHz	58	60	-	dB
		6GHz	47	51	-	dB
		8GHz	-	43	-	dB
		10GHz	-	35	-	dB
	ISOX	50MHz	-	72	-	dB
		1GHz	-	62	-	dB
		2GHz	-	56	-	dB
Isolation		3GHz	-	52	-	dB
RF1 to RF2	130%	4GHz	-	50	-	dB
		6GHz	-	44	-	dB
		8GHz	-	40	-	dB
		10GHz	-	32	-	dB
		50MHz	-	25	-	dB
		1GHz	-	25	-	dB
		2GHz	-	24	-	dB
Return Loss RFC	DEC	3GHz	-	23	-	dB
Netulli LUSS INFU	RFC _{RL}	4GHz	-	25	-	dB
		6GHz	-	24	-	dB
		8GHz	-	17	-	dB
		10GHz	-	12	-	dB



Typical Application Circuit, V_{DD} = 5.0V, T_{C} = +25°C, F_{RF} = 2000MHz, Driven Port = RF1 or RF2, input power = 0dBm, ZS = ZL = 50 Ω , PCB board trace and connector losses are de-embedded unless otherwise noted. **Boldface limits apply across the operating temperature range**, -55°C to +125°C by characterization with production testing at +25°C. (Cont.)

Parameter	Symbol	Cond	dition	Minimum ^{[1][2]}	Typical	Maximum ^{[1][2]}	Units
		50MHz		-	25	-	dB
		1GHz	1GHz		26	-	dB
		2GHz		-	27	-	dB
Return Loss RF1, RF2	DEON	3GHz		-	24	-	dB
On State, EN = 0	RFON _{RL}	4GHz		-	23	-	dB
		6GHz		-	26	-	dB
		8GHz		-	18	-	dB
		10GHz		-	13	-	dB
		50MHz		-	39	-	dB
		1GHz		-	32	-	dB
		2GHz		-	40	-	dB
Return Loss RF1, RF2	RFOFF _{RI}	3GHz		-	32	-	dB
Off State, EN = 0	Krorr _{RL}	4GHz		-	25	-	dB
		6GHz		-	25	-	dB
		8GHz		-	33	-	dB
		10GHz		-	27	-	dB
			50MHz	-	30	-	dBm
		V _{DD} = 5.0 V	2GHz	-	32	-	dBm
			3GHz	-	32	-	dBm
			4GHz	-	32	-	dBm
	ssion IP _{0.1dB}		6GHz	-	34	-	dBm
			8GHz	-	33	-	dBm
Input 0.1dB Compression			10GHz	-	32	-	dBm
input of tub Compression		V _{DD} = 3.1 V	50MHz	-	30	-	dBm
			2GHz	-	32	-	dBm
			3GHz	-	32	-	dBm
			4GHz	-	32	-	dBm
			6GHz	-	34	-	dBm
			8GHz	-	33	-	dBm
			10GHz	-	32	-	dBm
Input IP2	IIP2	$F_{RF1} = 2000MH:$ $F_{RF2} = 1990MH:$ $RFIN = RF1 \text{ or } F$ $PIN = +20dBm /$ $F_{IP2} = F_{RF1} + F_{F}$	z RF2 tone	-	111	-	dBm
			50MHz	-	58	-	dBm
			1GHz	-	64	-	dBm
		RF Input = RF1	2GHz	-	64	-	dBm
Input IP3	IIP3	or RF2 PIN = +15	2.5GHz	-	63	-	dBm
inpacii o	0	dBm/tone	4GHz	-	63	-	dBm
		ΔF = 1MHz	6GHz	-	64	-	dBm
			8GHz	-	64	-	dBm
			10GHz	-	61	-	dBm



Typical Application Circuit, V_{DD} = 5.0V, T_{C} = +25°C, F_{RF} = 2000MHz, Driven Port = RF1 or RF2, input power = 0dBm, ZS = ZL = 50 Ω , PCB board trace and connector losses are de-embedded unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C by characterization with production testing at +25°C.** (Cont.)

Parameter	Symbol	Condition	Minimum ^{[1][2]}	Typical	Maximum ^{[1][2]}	Units
Non-RF Driven Spurious ^[3]	Spur _{MAX} At any RF port when externally terminated into 50Ω		-	-114	-	dBm
Switching Time ^[4]	Т	50% control to 90% RF	-	325	-	ns
Switching fillier	T _{SW}	50% control to 10% RF	-	255	-	ns
Maximum Switching Rate ^[5]	SW _{RATE}	-	-	25	-	kHz

- 1. Items in minimum/maximum columns in bold are established by Test.
- 2. Items in minimum/maximum columns that are not bold are established by Design Characterization.
- 3. Spurious due to on-chip negative voltage generator. Typical generator fundamental frequency is 5.2MHz.
- 4. F_{RF} = 1GHz.
- 5. Minimum time required between switching of states = 1 / Maximum Switching Rate.

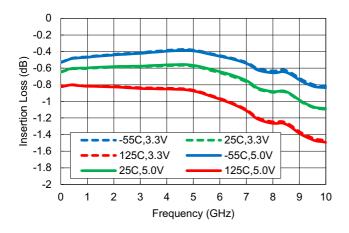
2.5 Control Mode

Table 1. Switch Control Truth Table

VCTL	EN	RFC to RF1	RFC to RF2
0	0	OFF	ON
1	0	ON	OFF
0	1	OFF	OFF
1	1	OFF	OFF

3. Typical Performance Graphs

 V_{DD} = 3.3V or 5.0V, T_{C} = +25°C (T_{C} = Temperature of Exposed Paddle), F_{RF} = 2000MHz, Z_{S} = Z_{L} = 50 Ω , P_{IN} = +0dBm for all small signal tests, RFC is the driven port and RF1 or RF2 is the output port, all unused RF ports terminated into 50 Ω , unless otherwise specified



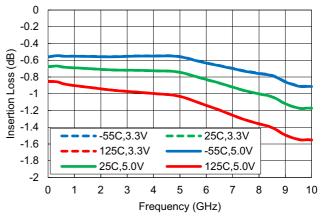
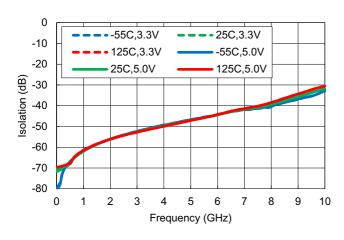


Figure 4. RFC to RF1 Insertion Loss

Figure 5. RFC to RF2 Insertion Loss



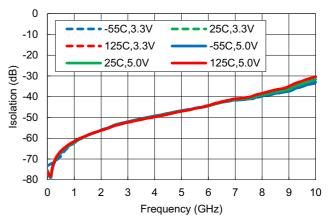
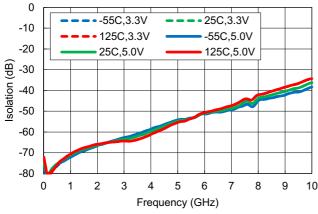
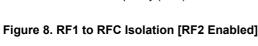


Figure 6. RF1 to RF2 to Isolation [RF2 Enabled]

Figure 7. RF2 to RF1 Isolation [RF1 Enabled]





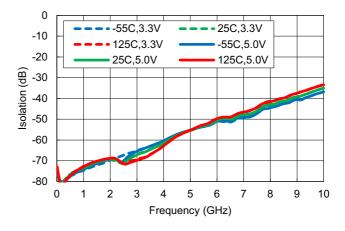
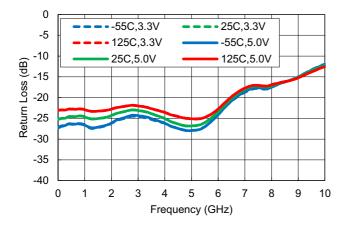


Figure 9. RF2 to RFC Isolation [RF1 Enabled]



 V_{DD} = 3.3V or 5.0V, T_{C} = +25°C (T_{C} = Temperature of Exposed Paddle), F_{RF} = 2000MHz, Z_{S} = Z_{L} = 50 Ω , P_{IN} = +0dBm for all small signal tests, RFC is the driven port and RF1 or RF2 is the output port, all unused RF ports terminated into 50 Ω , unless otherwise specified (Cont.)



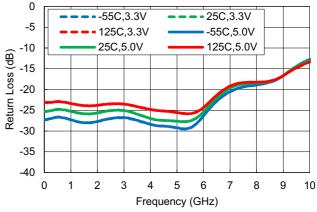
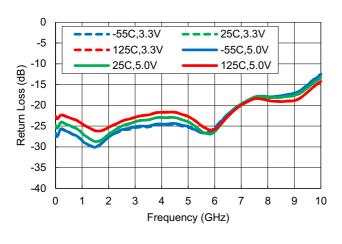


Figure 10. RFC Return Loss [RF1 Enabled]

Figure 11. RFC Return Loss [RF2 Enabled]



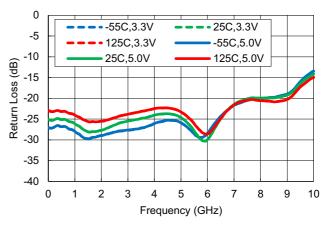
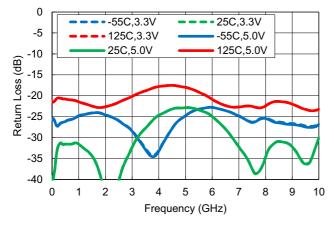


Figure 12. RF1 Return Loss [RF1 Enabled]

Figure 13. RF2 Return Loss [RF2 Enabled]



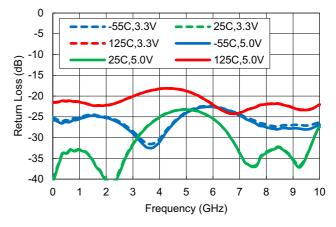


Figure 14. RF1 Return Loss [RF1 Off]

Figure 15. RF2 Return Loss [RF2 Off]



4. Applications Information

4.1 Default Start-up

There are no internal pull-up or pull-down resistors on the VCTL or EN pins.

4.2 Logic Control

Control pins VCTL and EN are used to set the state of the SP2T switch (see Absolute Maximum Ratings).

4.3 Power Supplies

Use a common V_{CC} power supply for all pins requiring DC power. Bypass all supply pins with external capacitors to minimize noise and fast transients. Supply noise can degrade noise figures and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change or transients should have a slew rate smaller than $1V/20\mu s$. In addition, keep all control pins at 0V ($\pm 0.3V$) while the supply voltage ramps or while it returns to zero.

4.4 Control Pin Interface

If control signal integrity is a concern and clean signals cannot be ensured because of issues such as overshoot, undershoot, and ringing, the following circuit at the input of each control pin is recommended. This applies to control Pin 1 (VCTL) and Pin 5 (EN) as shown in Figure 16.

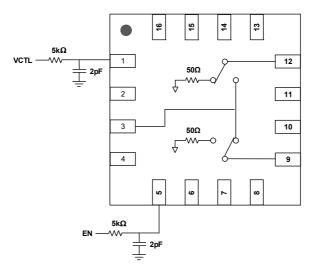


Figure 16. Typical Application Circuit

5. Radiation Tolerance

The ISL71934M is a radiation tolerant device for commercial space applications, Low Earth Orbit (LEO) applications, high altitude avionics, launch vehicles, and other harsh environments. The response of the device to Total Ionizing Dose (TID) radiation effects and Single-Event Effects (SEE) has been measured, characterized, and reported in the following sections. However, TID performance is not guaranteed through radiation acceptance testing.

5.1 Total lonizing Dose (TID) Testing

5.1.1 Introduction

To determine the sensitivity of the ISL71934M to the total dose environment, the TID test was conducted. Test downpoints were 0krad(Si), 10krad(Si), 20krad(Si), and 30krad(Si). Total dose testing was performed using a Hopewell Designs N40 panoramic 60Co irradiator. The irradiations were performed at a dose rate of 0.00875rad(Si)/s. A PbAI box shielded the test fixture and devices under test against low energy secondary gamma radiation. The characterization matrix consisted of 18 samples irradiated under bias and 18 samples irradiated with all pins grounded. All electrical testing was performed outside the irradiator using Automated Test Equipment (ATE) with data logging at each downpoint. Downpoint electrical testing was performed at room temperature.

The bias configuration is shown in Figure 17.

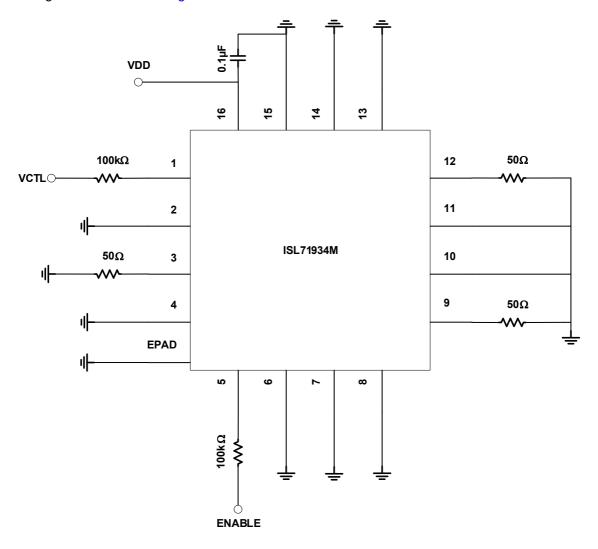
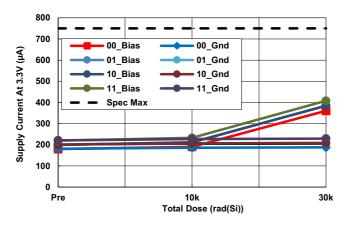


Figure 17. Bias Configuration



5.1.2 TID Results

Figure 18 through Figure 21 show the performance parameters for key specifications over TID.



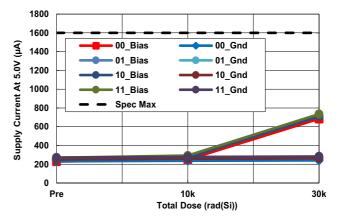
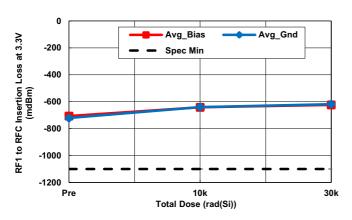


Figure 18. I_{DD} for V_{DD} = 3.3V vs TID

Figure 19. I_{DD} for V_{DD} = 5V vs TID



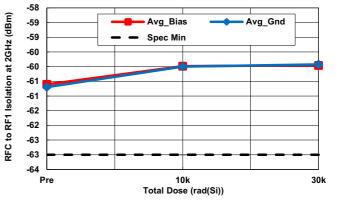


Figure 20. Insertion Loss RF1 to RFC at 2GHz and $$V_{DD}=3.3V\mbox{ vs TID}$$

Figure 21. RFC to RF1 Isolation at 2GHz and V_{DD} = 3.3V vs TID

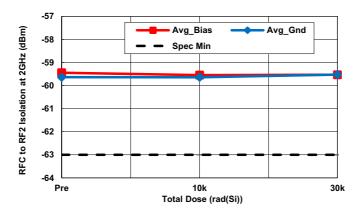


Figure 22. RFC to RF2 Isolation at 2GHz and V_{DD} = 3.3V vs TID



5.2 Single-Event Effects Testing

The intense heavy ion environment encountered in space applications can cause a variety of Single-Event Effects (SEE). SEE can lead to system-level performance issues, including disruption, degradation, and destruction. For predictable and reliable space system operation, characterize individual electronic components to determine their SEE response. The following is a summary of the ISL71934M SEE testing.

5.2.1 SEE Test Facility

Testing was performed at Texas A&M University (TAMU Cyclotron Institute heavy ion facility. The overall test setup includes the test jig containing the evaluation cards mounted and wired through 20ft cable to the data room. The input pins RFC, RF1, and RF2 were connected with a series 10µF capacitor to ensure that only AC signals were applied to the ISL71934M. The power and control pins VDD, VCLT, and EN all had a 1µF decoupling capacitor to ground to minimize noise.

5.2.2 SEE Test Setup

For SEB and SEL testing, VDD was set to 5.5V, 5.8V, 6.2V, and 6.8V. The RFC pin was stimulated using a 10MHz signal with a peak amplitude of ±5V (24dBm). The inputs VCLTL and EN were set to 2.5V so that all three RF inputs were open. The supply current through the VDD pin was monitored to look for increases because of radiation.

5.2.3 Single Event Burnout and Latch-Up (SEB/L) Results

No SEB was observed for the device LET of $43 \text{MeV} \cdot \text{cm}^2/\text{mg}$ (+125°C) for V_{DD} = 5.5V, 5.8V, and 6.2V. Runaway currents were observed for 1 DUT at V_{DD} = 6.5V. For V_{DD} = 5.5V, 5.8V, and 6.2V, no current increases were seen outside of ±2%.

5.2.4 SET Results

The SET testing was performed with VCTL = 1.1V (logic 1) and EN = 0V (logic 0). This enables the connection from the RFC to RF1 pins, with minimal margin on the digital control pins. A 10MHz, \pm 5V peak sine wave was applied to RFC. Both RF1 and RF2 were monitored using an oscilloscope. The oscilloscope was set to trigger on a \pm 10ns deviation in zero crossings. The part was operated at V_{DD} = 2.7V and 4.5V. The oscilloscope did not trigger on any of the four parts tested, indicating no SET events.

5.2.5 Conclusion

The ISL71934M shows no sensitivity to SEB/L or exhibits any SET for the full supply voltage range, including margin up to $V_{DD} = 6.2V$ under the condition of LET value of $43 \text{MeV} \cdot \text{cm}^2/\text{mg}$.



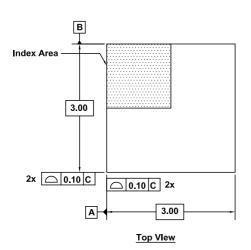
6. Package Outline Drawing

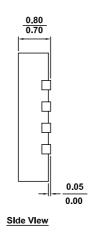
For the most recent package outline drawing, see L16.3x3F.

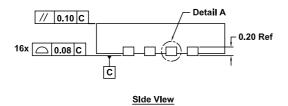
_16.3x3F

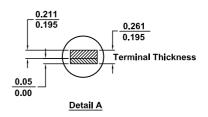
16 Lead Thin Quad Flat No-Lead Package

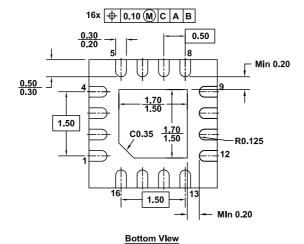
Rev 0, 2/20







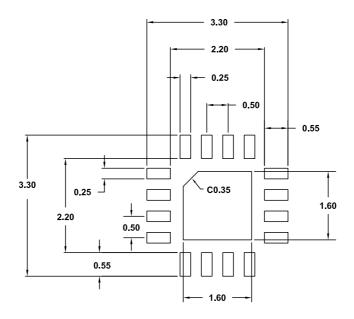




Notes:

- 1. All dimensions are in mm. Angles are in degrees.
- 2. Coplanarity applies to the exposed pad and the terminals. Coplanarity shall not exceed 0.05mm.
- 3. Warpage shall not exceed 0.05mm.
- 4. The package length and package width are considered as special characteristics.
- 5. See JEDEC MO-220.





Recommended Land Pattern Dimension

Notes:

- 1. All dimensions are in mm. Angles are in degrees.
- 2. Top down view. As viewed on PCB.
- 3. Land pattern recommendation per IPC-7351B generic requirement for surface mount design and land pattern.



7. Ordering Information

Part Number ^[1]	Part Marking	LDR	Package Description (RoHS Compliant)	Pkg. Dwg. #	MSL Rating ^[2]	Carrier Type ^[3]	Temp. Range
ISL71934MRTZ	71934	30krad(Si)	16 Ld TQFN	L16.3x3F	1	Tray	-55 to +125°C
ISL71934MRTZ-T	71354	JUNIAU(JI)	10 Lu TQT N	L10.5X51	'	Reel, 1k	-55 to 1125 C

^{1.} These Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.

- 2. For more information about Moisture Sensitivity Level (MSL), see TB363.
- 3. See TB347 for details about reel specifications.

8. Revision History

Rev.	Date	Description
1.03	Nov 6, 2025	Updated TID Features bullet. Added Boldface statement to EC table.
1.02	May 19, 2025	Updated page 1 content. Updated Note 1 in Abs Max section. Updated the RF Frequency Range spec units from MHz to GHz and the max spec from 6000MHz to 10GHz. Updated Note 1 in the Recommended Operating Conditions table. Updated the following typical values in the Electrical Specifications table: Insertion Loss Isolation Return Loss Input 0.1dB Compression Added more conditions to Input IP3 specification. Removed Input 1dB Compression spec and applicable note. Updated Typical Performance Graphs to show extended frequency. Updated Note 1 in ordering table.
1.01	Feb 24, 2021	Updated the Ordering Information table and moved it to the end to follow new formatting.
1.00	Dec 4, 2020	Initial release



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