ISL72027SEH

3.3V Radiation Tolerant CAN Transceiver, with Listen Mode and Split Termination Output

The ISL72027SEH is a 3.3V radiation tolerant CAN transceiver that is compatible with the ISO11898-2 standard for applications calling for Controller Area Network (CAN) serial communication in satellites and aerospace communications and telemetry data processing in harsh industrial environments.

The transceiver can transmit and receive at bus speeds up to 5Mbps. It can drive a 40m cable at 1Mbps per the ISO11898-2 specification. The device operates over a common-mode range of -7V to +12V with a maximum of 120 nodes. The device has three discrete selectable driver rise/fall time options, a listen mode feature and a split termination output.

Receiver (Rx) inputs feature a “full fail-safe” design, which ensures a logic high Rx output if the Rx inputs are floating, shorted, or terminated but undriven.

The ISL72027SEH is available in an 8 Ld hermetic ceramic flatpack and die form that operate across the temperature range of the -55°C to +125°C. The logic inputs are tolerant with 5V systems.

Other CAN transceivers available are the ISL72026SEH and ISL72028SEH. For a list of differences see Table 3.

Applications

- Satellites and aerospace communications
- Telemetry data processing
- High-end industrial environments
- Harsh environments

Features

- DLA SMD 5962-15228
- ESD Protection on all pins: 4kV HBM
- Compatible with ISO11898-2
- Operating supply range: 3.0V to 3.6V
- Bus pin fault protection to ±20V
- Undervoltage lockout
- Cold spare: powered down devices/nodes do not affect active devices operating in parallel
- Three selectable driver rise and fall times
- Glitch free bus I/O during power-up and power-down
- Full fail-safe (open, short, terminated/undriven) receiver
- Hi-Z input allows for 120 nodes on the bus
- High data rates: up to 5Mbps
- Quiescent supply current: 7mA (max)
- Listen mode supply current: 2mA (max)
- -7V to +12V common-mode input voltage range
- 5V tolerant logic inputs
- Thermal shutdown
- Acceptance tested to 75krad(Si) (LDR) wafer-by-wafer
- Radiation tolerance
    - SEL/B immune to LET 60MeV•cm^2/mg
    - Low dose rate (0.01rad(Si)/s): 75krad(Si)

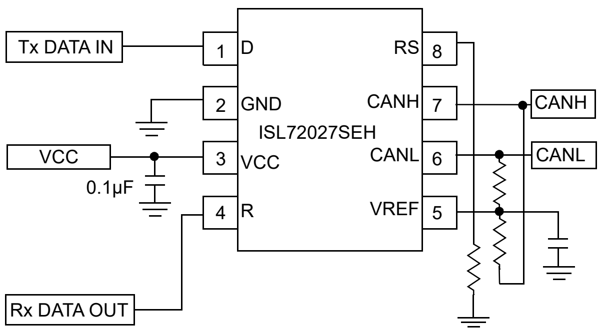

Figure 1. Typical Application

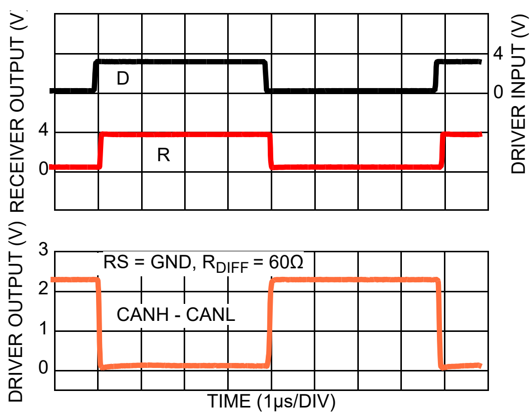

Figure 2. Fast Driver and Receiver Waveforms

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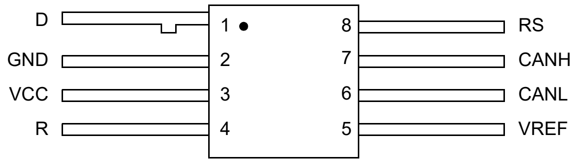
Contents

1. Pin Information

1.1 Pin Assignments



Note: The package lid is tied to ground.

Figure 3. Pin Assignments - Top View

1.2 Pin Descriptions

Pin Number	Pin Name	Function
1	D	CAN driver digital input. The bus states are LOW = dominant and HIGH = recessive. Internally tied HIGH.
2	GND	Ground connection.
3	VCC	System power supply input (3.0V to 3.6V). The typical voltage for the device is 3.3V.
4	R	CAN data receiver output. The bus states are LOW = dominant and HIGH = recessive.
5	VREF	VCC/2 reference output for split mode termination.
6	CANL	CAN bus line for low level output.
7	CANH	CAN bus line for high level output.
8	RS	A resistor to GND from this pin controls the rise and fall time of the CAN output waveform. Drive RS HIGH to put into listen mode.

1.3 Equivalent Input and Output Schematic Diagrams

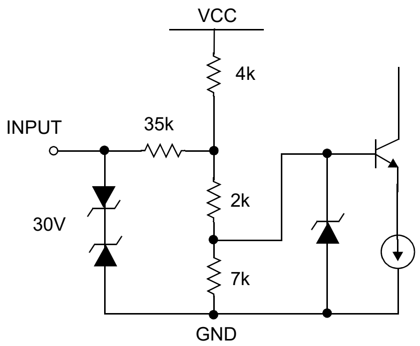


Figure 4. CANH and CANL Inputs

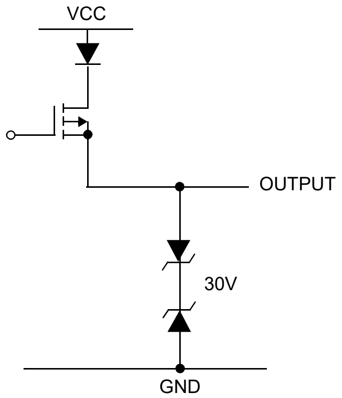


Figure 5. CANH Output

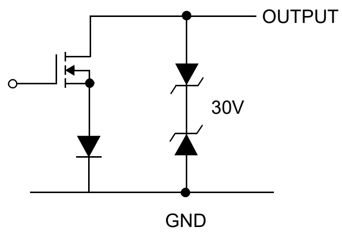


Figure 6. CANL Output

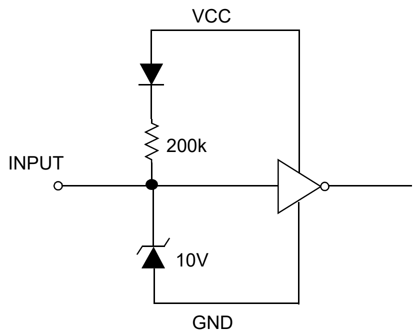


Figure 7. D Input

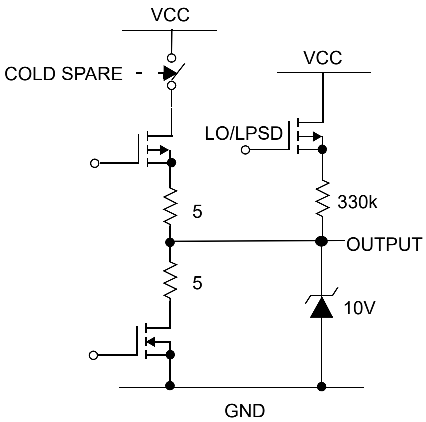


Figure 8. R Output

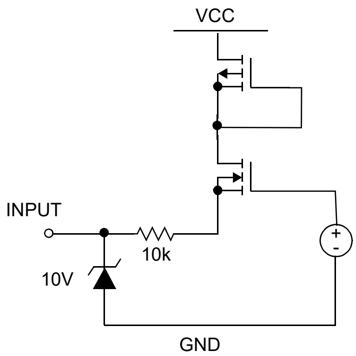


Figure 9. RS Input

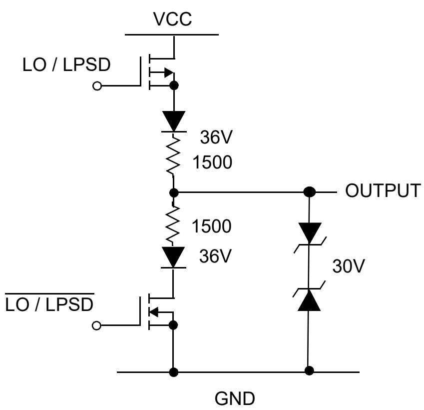


Figure 10. VREF

2. Specifications

2.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
VCC to GND with/without Ion Beam	-0.3	+5.5	V
CANH, CANL, VREF Under Ion Beam	-	±18	V
CANH, CANL, VREF	-	±20	V
I/O Voltages D, R, RS	-0.5	7	V
Receiver Output Current	-10	10	mA
Output Short-circuit Duration	Continuous		
Maximum Junction Temperature	-	+175	°C
Maximum Storage Temperature Range	-65	+150	°C
Human Body Model (Tested per MIL-PRF-883 3015.7)			
CANH, CANL Bus Pins	-	4	kV
All Other Pins	-	4	kV
Charged Device Model (Tested per JESD22-C101D)	-	750	V
Machine Model (Tested per JESD22-A115-A)	-	200	V

2.2 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Temperature Range	-55	+125	°C
V_{CC} Supply Voltage	3	3.6	V
Voltage on CAN I/O	-7	12	V
V_{IH} D Logic Pin	2	5.5	V
V_{IL} D Logic Pin	0	0.8	V
IOH Driver (CANH - CANL = 1.5V, V_{CC} = 3.3V)	-	-40	mA
IOH Receiver (V_{OH} = 2.4V)	-	-4	mA
IOL Driver (CANH - CANL = 1.5V, V_{CC} = 3.3V)	-	40	mA
IOL Receiver (V_{OL} = 0.4V)	-	4	mA

2.3 Thermal Specifications

Parameter	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance	8 Ld FP Package	θ_{JA}[1]	Junction to ambient	39	°C/W
		θ_{JC}[2]	Junction to case	7	°C/W

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board (two buried 1oz copper planes) with direct attach features package base mounted to PCB thermal land with a 10 mil gap fill material having a k of 1W/m-K. See TB379.
2. For θ_{JC}, the case temperature location is the center of the package underside.

2.4 Electrical Specifications

Test Conditions: V_{CC} = 3V to 3.6V; Typical are at T_A = +25°C[1]; unless otherwise specified[2]. **Boldface limits apply across the operating temperature range, -55°C to +125°C or across a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s.**

Parameter	Symbol	Test Conditions	Temp (°C)	Min[3]	Typ[1]	Max[3]	Unit
Driver Electrical Characteristics							
Dominant Bus Output Voltage	$V_{O(DOM)}$	D = 0V, CANH, RS = 0V, 3V ≤ V_{CC} ≤ 3.6V, Figure 11, Figure 12	Full	**2.25**	2.85	**V_{CC}**	V
		D = 0V, CANL, RS = 0V, 3V ≤ V_{CC} ≤ 3.6V, Figure 11, Figure 12	Full	**0.10**	0.65	**1.25**	V
Recessive Bus Output Voltage	$V_{O(REC)}$	D = 3V, CANH, RS = 0V, 60Ω and no load, 3V ≤ V_{CC} ≤ 3.6V, Figure 11, Figure 12	Full	**1.80**	2.30	**2.70**	V
		D = 3V, CANL, RS = 0V, 60Ω and no load, 3V ≤ V_{CC} ≤ 3.6V, Figure 11, Figure 12	Full	**1.80**	2.30	**2.80**	V
Dominant Output Differential Voltage	$V_{OD(DOM)}$	D = 0V, RS = 0V, 3V ≤ V_{CC} ≤ 3.6V, Figure 11, Figure 12	Full	**1.5**	2.2	**3.0**	V
		D = 0V, RS = 0V, 3V ≤ V_{CC} ≤ 3.6V, Figure 12, Figure 13	Full	**1.2**	2.1	**3.0**	V
Recessive Output Differential Voltage	$V_{OD(REC)}$	D = 3V, RS = 0V, 3V≤ V_{CC} ≤ 3.6V, Figure 11, Figure 12	Full	**-120**	0.2	**12**	mV
		D = 3V, RS = 0V, 3.0V ≤ V_{CC} ≤ 3.6V, no load	Full	**-500**	-34	**50**	mV
Logic Input High Voltage (D)[4]	V_{IH}	3V ≤ V_{CC} ≤ 3.6V	Full	**2.0**	-	**5.5**	V
Logic Input Low Voltage (D)[4]	V_{IL}	3V≤ V_{CC} ≤ 3.6V	Full	**0**	-	**0.8**	V
High Level Input Current (D)	I_{IH}	D = 2V, 3V ≤ V_{CC} ≤ 3.6V	Full	**-30**	-3	**30**	µA
Low Level Input Current (D)	I_{IL}	D = 0.8V, 3V ≤ V_{CC} ≤ 3.6V	Full	**-30**	-7	**30**	µA
RS Input Voltage for Listen Mode	$V_{IN(RS)}$	3V ≤ V_{CC} ≤ 3.6V	Full	**0.75xV_{CC}**	1.90	**5.5**	V

Test Conditions: V_{CC} = 3V to 3.6V; Typical are at T_A = +25°C[1]; unless otherwise specified[2]. **Boldface limits apply across the operating temperature range, -55°C to +125°C or across a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s. (Cont.)**

Parameter	Symbol	Test Conditions	Temp (°C)	Min[3]	Typ[1]	Max[3]	Unit
Output Short-Circuit Current	I_{OSC}	V_{CANH} = -7V, CANL = OPEN, 3V ≤ V_{CC} ≤ 3.6V, Figure 24, Figure 25	Full	**-250**	-100	-	mA
		V_{CANH} = +12V, CANL = OPEN, 3V ≤ V_{CC} ≤ 3.6V, Figure 24, Figure 25	Full	-	0.4	**1.0**	mA
		V_{CANL} = -7V, CANH = OPEN, 3V ≤ V_{CC} ≤ 3.6V, Figure 24, Figure 25	Full	**-1.0**	-0.4	-	mA
		V_{CANL} = +12V, CANH = OPEN, 3V ≤ V_{CC} ≤ 3.6V, Figure 24, Figure 25	Full	-	100	**250**	mA
Thermal Shutdown Temperature	T_{SHDN}	3V < V_{IN} < 3.6V	-	-	163	-	°C
Thermal Shutdown Hysteresis	T_{HYS}	3V < V_{IN} < 3.6V	-	-	12	-	°C
Receiver Electrical Characteristics							
Input Threshold Voltage (Rising)	V_{THR}	RS = 0V, 10k, 50k, (recessive to dominant), Figure 16, Figure 17, Figure 18, Figure 19	Full	-	750	**900**	mV
Input Threshold Voltage (Falling)	V_{THF}	RS = 0V, 10k, 50k, (dominant to recessive), Figure 16, Figure 17, Figure 18, Figure 19	Full	**500**	650	-	mV
Input Hysteresis	V_{HYS}	(V_{THR} - V_{THF}), RS = 0V, 10k, 50k, Figure 16, Figure 17, Figure 18, Figure 19	Full	**40**	90	-	mV
Listen Mode Input Threshold Voltage (Rising)	V_{THRLM}	RS = V_{CC}, (recessive to dominant), Figure 22, Figure 23	Full	-	920	**1150**	mV
Listen Mode Input Threshold Voltage (Falling)	V_{THFLM}	RS = V_{CC}, (dominant to recessive), Figure 22, Figure 23	Full	**525**	820	-	mV
Listen Mode Input Hysteresis	V_{HYSLM}	(V_{THR} - V_{THF}), RS = V_{CC}, Figure 22, Figure 23	Full	**50**	100	-	mV
Receiver Output High Voltage	V_{OH}	I_O = -4mA	Full	**2.4**	VCC - 0.2	-	V
Receiver Output Low Voltage	V_{OL}	I_O = +4mA	Full	-	0.2	**0.4**	V
Input Current for CAN Bus	I_{CAN}	CANH or CANL at 12V, D = 3V, other bus pin at 0V, RS = 0V	Full	-	420	**500**	µA
		CANH or CANL at 12V, D = 3V, V_{CC} = 0V, other bus pin at 0V, RS = 0V	Full	-	150	**250**	µA
		CANH or CANL at -7V, D = 3V, other bus pin at 0V, RS = 0V	Full	**-400**	-300	-	µA
		CANH or CANL at -7V, D = 3V, V_{CC} = 0V, other bus pin at 0V, RS = 0V	Full	**-150**	-85	-	µA
Input Capacitance (CANH or CANL)	C_{IN}	Input to GND, D = 3V, RS = 0V	25	-	35	-	pF

Test Conditions: V_{CC} = 3V to 3.6V; Typical are at T_A = +25°C[1]; unless otherwise specified[2]. **Boldface limits apply across the operating temperature range, -55°C to +125°C or across a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s. (Cont.)**

Parameter	Symbol	Test Conditions	Temp (°C)	Min[3]	Typ[1]	Max[3]	Unit
Differential Input Capacitance	C_{IND}	Input to Input, D = 3V, RS = 0V	25	-	15	-	pF
Input Resistance (CANH or CANL)	R_{IN}	Input to GND, D = 3V, RS = 0V	Full	**20**	40	**50**	kΩ
Differential Input Resistance	R_{IND}	Input to Input, D = 3V, RS = 0V	Full	**40**	80	**100**	kΩ
Supply Current							
Supply Current, Listen Mode	$I_{CC(L)}$	RS = D = V_{CC}, 3V ≤ V_{CC} ≤ 3.6V	Full	-	1	**2**	mA
Supply Current, Dominant	$I_{CC(DOM)}$	D = RS = 0V, no load, 3V ≤ V_{CC} ≤ 3.6V	Full	-	5	**7**	mA
Supply Current, Recessive	$I_{CC(REC)}$	D = V_{CC}, RS = 0V, no load, 3V ≤ V_{CC} ≤ 3.6V	Full	-	2.6	**5.0**	mA
Cold Sparing BUS Current							
CANH Leakage Current	$I_{L(CANH)}$	V_{CC} = 0.2V, CANH = -7V or 12V, CANL = float, D = V_{CC}, RS = 0V	Full	**-25**	-4	**25**	µA
CANL Leakage Current	$I_{L(CANL)}$	V_{CC} = 0.2V, CANL = -7V or 12V, CANH = float, D = V_{CC}, RS = 0V	Full	**-25**	-4	**25**	µA
VREF Leakage Current	$I_{L(VREF)}$	V_{CC} = 0.2V, V_{REF} = -7V or 12V, D = V_{CC}	Full	**-25.00**	0.01	**25.00**	µA
Driver Switching Characteristics							
Propagation Delay LOW to HIGH	t_{PDLH1}	RS = 0V, Figure 14, Figure 15	Full	-	75	**150**	ns
	t_{PDLH2}	RS = 10kΩ, Figure 14, Figure 15	Full	-	520	**850**	ns
	t_{PDLH3}	RS = 50kΩ, Figure 14, Figure 15	Full	-	850	**1400**	ns
Propagation Delay HIGH to LOW	t_{PDHL1}	RS = 0V, Figure 14, Figure 15	Full	-	80	**155**	ns
	t_{PDHL2}	RS = 10kΩ, Figure 14, Figure 15	Full	-	460	**800**	ns
	t_{PDHL3}	RS = 50kΩ, Figure 14, Figure 15	Full	-	725	**1300**	ns
Output Skew	t_{SKEW1}	RS = 0V, (|t_{PHL} - t_{PLH}|), Figure 14, Figure 15	Full	-	5	**50**	ns
	t_{SKEW2}	RS = 10kΩ, (|t_{PHL} - t_{PLH}|), Figure 14, Figure 15	Full	-	60	**510**	ns
	t_{SKEW3}	RS = 50kΩ, (|t_{PHL} - t_{PLH}|), Figure 14, Figure 15	Full	-	110	**800**	ns
Output Rise Time	t_{r1}	RS = 0V, (fast speed) Figure 14, Figure 15	Full	**20**	55	**100**	ns
Output Fall Time	t_{f1}		Full	**10**	25	**75**	ns
Output Rise Time	t_{r2}	RS = 10kΩ, (medium speed - 250Kbps) Figure 14, Figure 15	Full	**200**	400	**780**	ns
Output Fall Time	t_{f2}		Full	**175**	300	**500**	ns
Output Rise Time	t_{r3}	RS = 50kΩ, (slow speed - 125Kbps) Figure 14, Figure 15	Full	**400**	700	**1400**	ns

Test Conditions: V_{CC} = 3V to 3.6V; Typical are at T_A = +25°C[1]; unless otherwise specified[2]. **Boldface limits apply across the operating temperature range, -55°C to +125°C or across a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s. (Cont.)**

Parameter	Symbol	Test Conditions	Temp (°C)	Min[3]	Typ[1]	Max[3]	Unit
Output Fall Time	t_{f3}		Full	**300**	650	**1000**	ns
Total Loop Delay, Driver Input to Receiver Output, Recessive to Dominant	$t_{(LOOP1)}$	RS = 0V, Figure 20, Figure 21	Full	-	115	**210**	ns
		RS = 10kΩ, Figure 20, Figure 21	Full	-	550	**875**	ns
		RS = 50kΩ, Figure 20, Figure 21	Full	-	850	**1400**	ns
Total Loop Delay, Driver Input to Receiver Output, Dominant to Recessive	$t_{(LOOP2)}$	RS = 0V, Figure 20, Figure 21	Full	-	130	**270**	ns
		RS = 10kΩ, Figure 20, Figure 21	Full	-	500	**825**	ns
		RS = 50kΩ, Figure 20, Figure 21	Full	-	750	**1300**	ns
Listen to Valid Dominant Time	$t_{L-DOM)}$	Figure 22, Figure 23	Full	-	5	**15**	us
Receiver Switching Characteristics							
Propagation Delay LOW to HIGH	t_{PLH}	Figure 16, Figure 17, Figure 18, Figure 19	Full	-	50	**110**	ns
Propagation Delay HIGH to LOW	t_{PHL}	Figure 16, Figure 17, Figure 18, Figure 19	Full	-	50	**110**	ns
Rx Skew	t_{SKEW1}	$\lvert(t_{PHL} - t_{PLH})\rvert$, Figure 16, Figure 17, Figure 18, Figure 19	Full	-	2	**35**	ns
Rx Rise Time	t_r	Figure 16, Figure 17, Figure 18, Figure 19	Full	-	2	-	ns
Rx Fall Time	t_f	Figure 16, Figure 17, Figure 18, Figure 19	Full	-	2	-	ns
VREF/RS Pin Characteristics							
VREF Pin Voltage	VREF	-5µA<IREF<5µA	Full	**0.45xV_{CC}**	1.60	**0.55xV_{CC}**	V
		-50µA<IREF<50µA	Full	**0.4xV_{CC}**	1.6	**0.6xV_{CC}**	V
RS Pin Input Current	IRS(H)	RS = 0.75 x V_{CC}	Full	**-10.0**	-0.2	-	µA
	$I_{RS(L)}$	V_{RS} = 0V	Full	**-450**	-125	**0**	µA

1. Typical values are at 3.3V. Parameters with a single entry in the “TYP” column apply to 3.3V. Typical values shown are not guaranteed.
2. All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.
3. Parameters with MIN and/or MAX limits are 100% tested at -55°C, +25°C and +125°C, unless otherwise specified.
4. Parameter included in functional testing.

2.5 Test Circuits and Waveforms

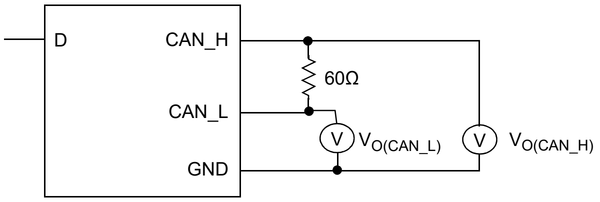


Figure 11. Driver Test Circuit

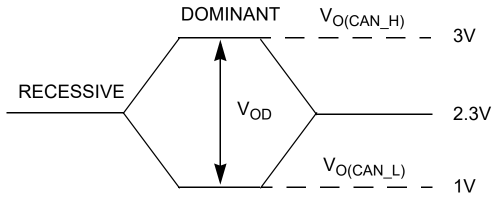


Figure 12. Driver Bus Voltage Definitions

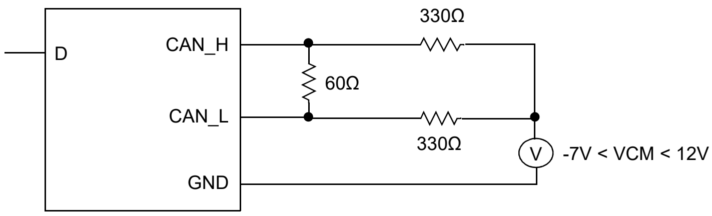
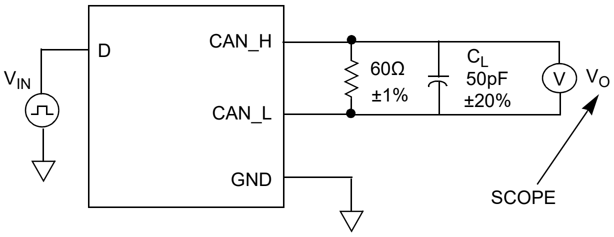


Figure 13. Driver Common-Mode Circuit



V_{IN} = 125kHz, 0V to V_{CC}, Duty Cycle 50%, $t_r = t_f \leq 6ns$, $Z_O = 50\Omega$
C_L includes fixture and instrumentation capacitance.

Figure 14. Driver Timing Test Circuit

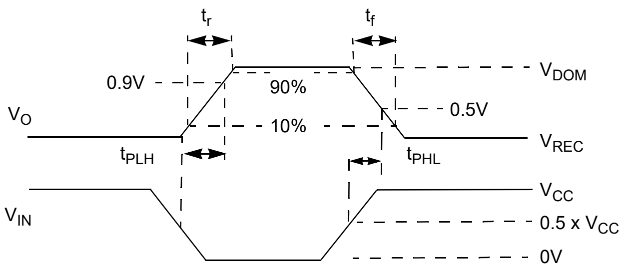


Figure 15. Driver Timing Measurement Points

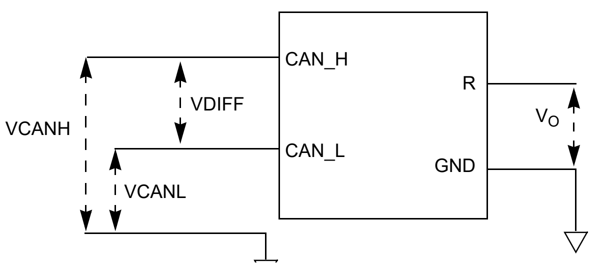
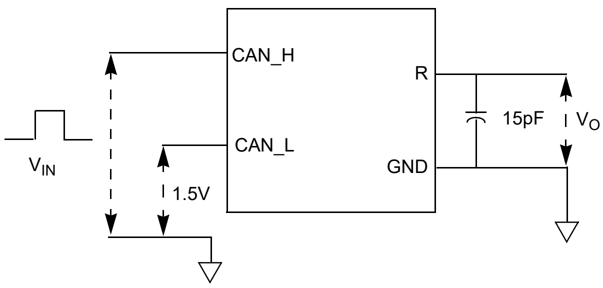


Figure 16. Receiver Voltage Definitions



V_{IN} = 125kHz, Duty Cycle 50%, $t_r = t_f$ = 6ns, $Z_O = 50\Omega$
C_L includes test setup capacitance

Figure 17. Receiver Test Circuit

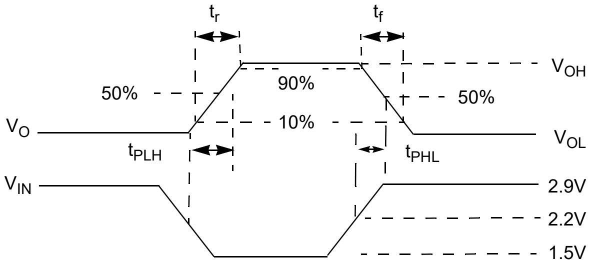


Figure 18. Receiver Test Measurement Points

Input		Output	Measured
VCANH	**VCANL**	**R**	**VDIFF**
–6.1V	–7V	L	900mV
12V	11.1V	L	900mV
–1V	–7V	L	6V
12V	6V	L	6V
–6.5V	–7V	H	500mV
12V	11.5V	H	500mV
–7V	–1V	H	6V
6V	12V	H	6V
Open	Open	H	X

Figure 19. Differential Input Voltage Threshold Test

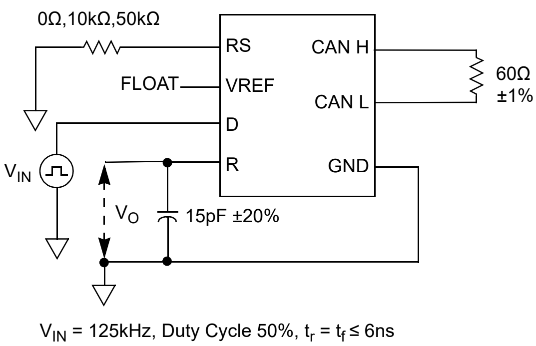


Figure 20. Total Loop Delay Test Circuit

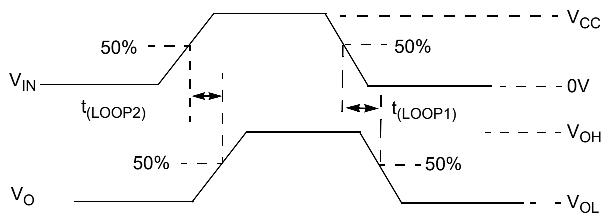


Figure 21. Total Loop Delay Measurement Points

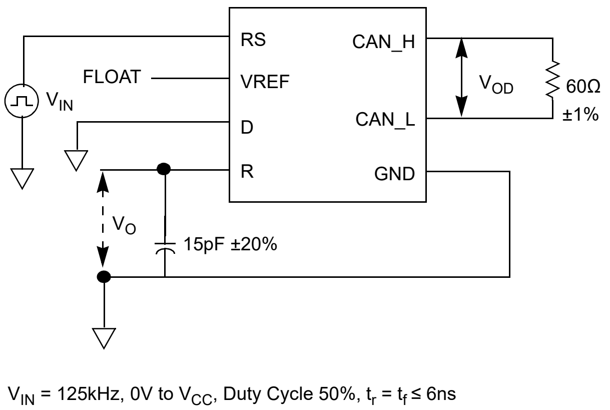


Figure 22. Listen to Valid Dominant Time Circuit

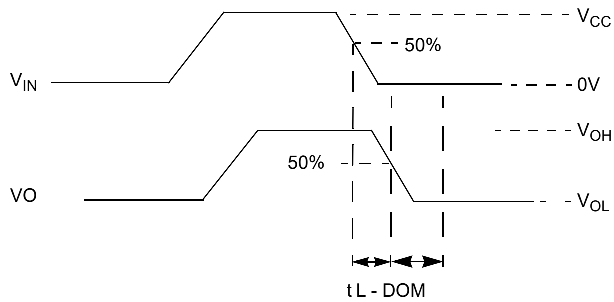


Figure 23. Listen to Valid Dominant Time Measurement Points

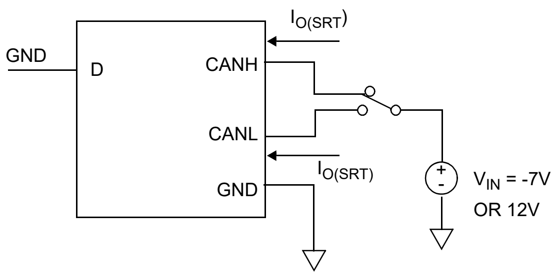


Figure 24. Output Short-Circuit Current Circuit

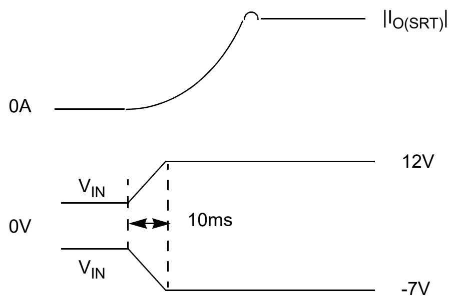


Figure 25. Output Short-Circuit Current Waveforms

3. Typical Performance Curves

V_{CC} = 3.3V, C_L = 15pF, T_A = +25°C; unless otherwise specified.

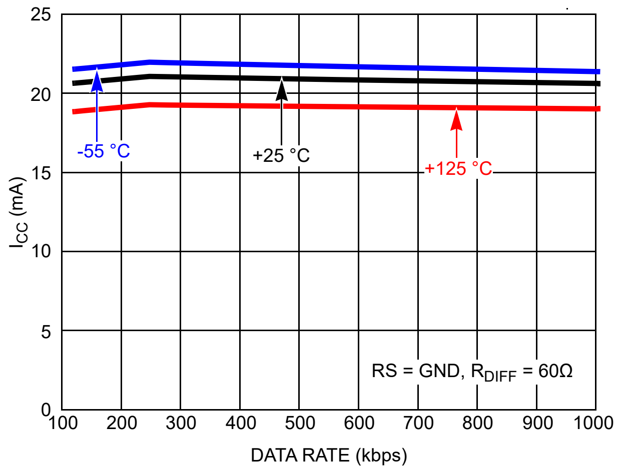


Figure 26. Supply Current vs Fast Data Rate vs Temperature

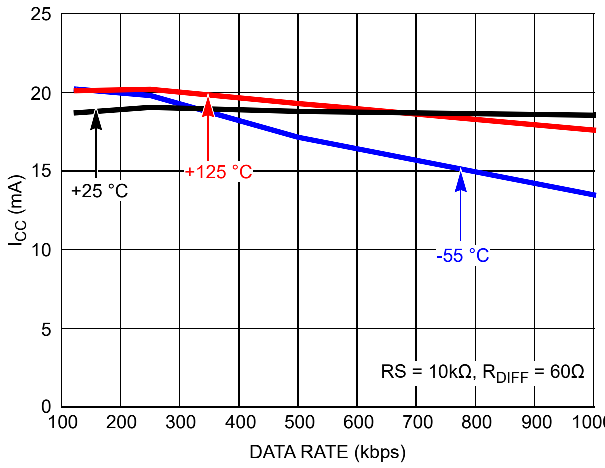


Figure 27. Supply Current vs Medium Data Rate vs Temperature

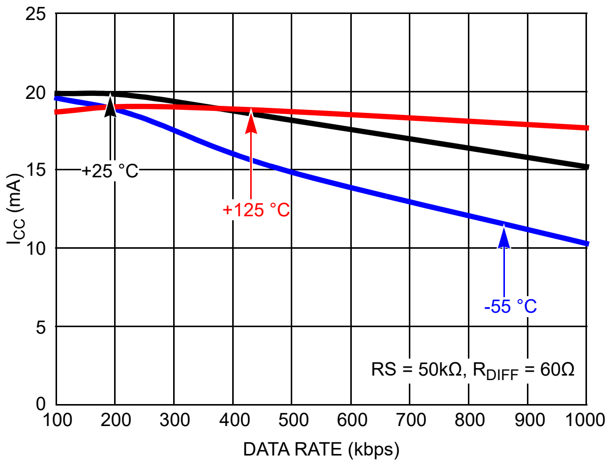


Figure 28. Supply Current vs Slow Data Rate vs Temperature

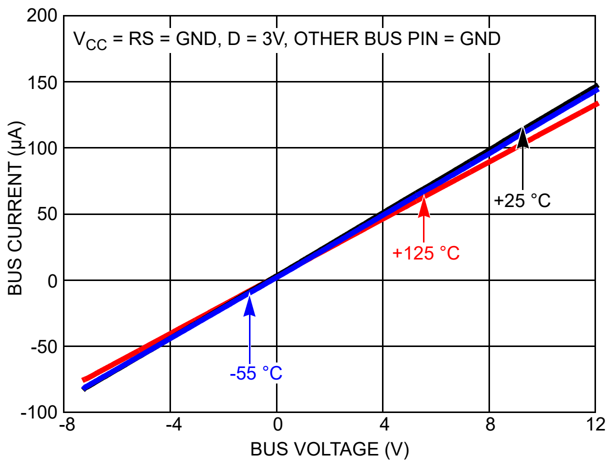


Figure 29. Bus Pin Leakage vs VCM at V_{CC} = 0V

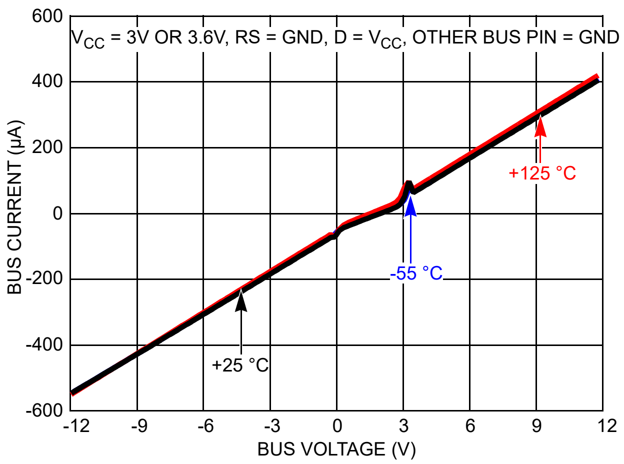


Figure 30. Bus Pin Leakage vs ±12V VCM

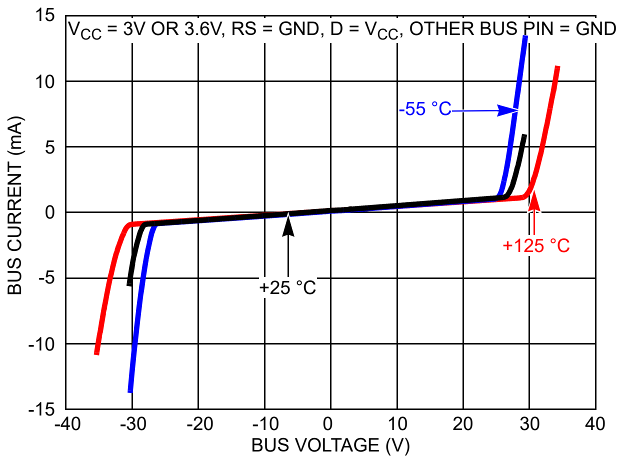


Figure 31. Bus Pin Leakage vs ±35V VCM

V_{CC} = 3.3V, C_L = 15pF, T_A = +25°C; unless otherwise specified. **(Cont.)**

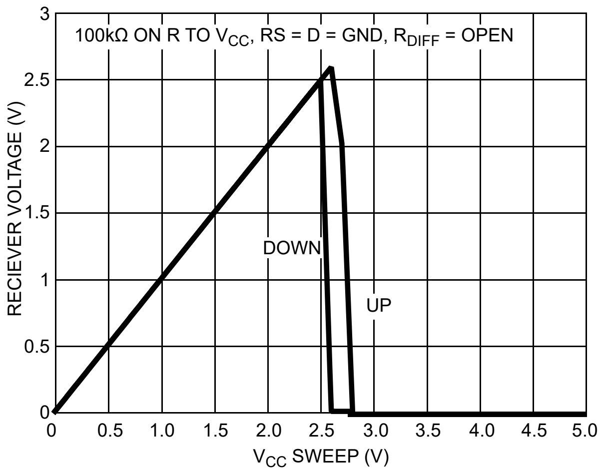


Figure 32. V_{CC} Undervoltage Lockout

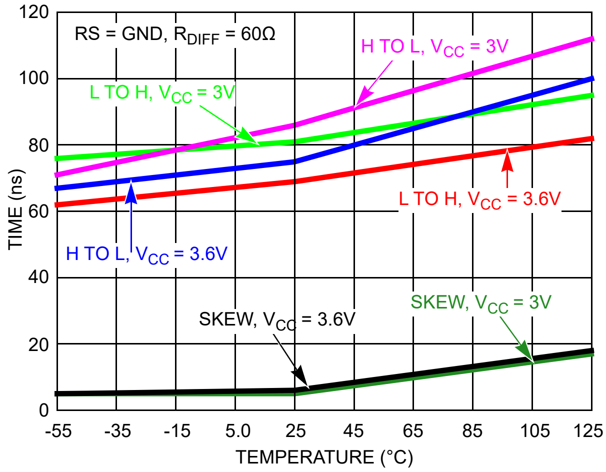


Figure 33. Transmitter Propagation Delay and Skew vs Temperature at Fast Speed

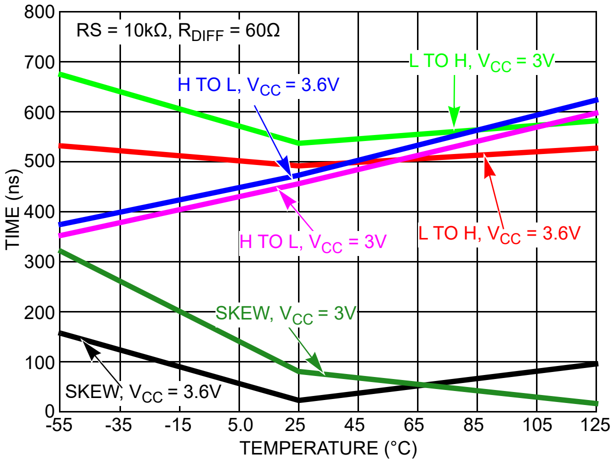


Figure 34. Transmitter Propagation Delay and Skew vs Temperature at Medium Speed

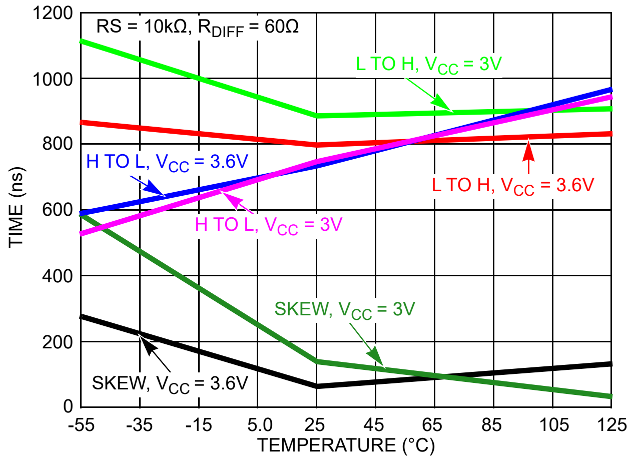


Figure 35. Transmitter Propagation Delay and Skew vs Temperature at Slow Speed

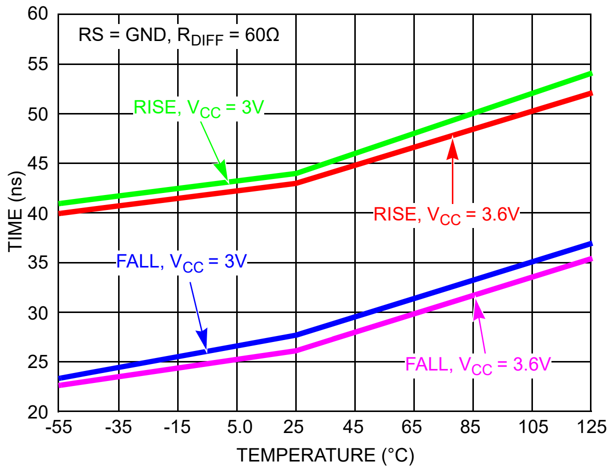


Figure 36. Transmitter Rise and Fall Times vs Temperature at Fast Speed

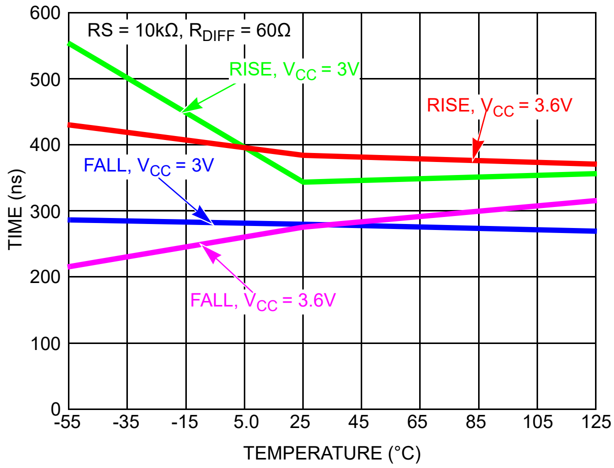


Figure 37. Transmitter Rise and Fall Times vs Temperature at Medium Speed

V_{CC} = 3.3V, C_L = 15pF, T_A = +25°C; unless otherwise specified. **(Cont.)**

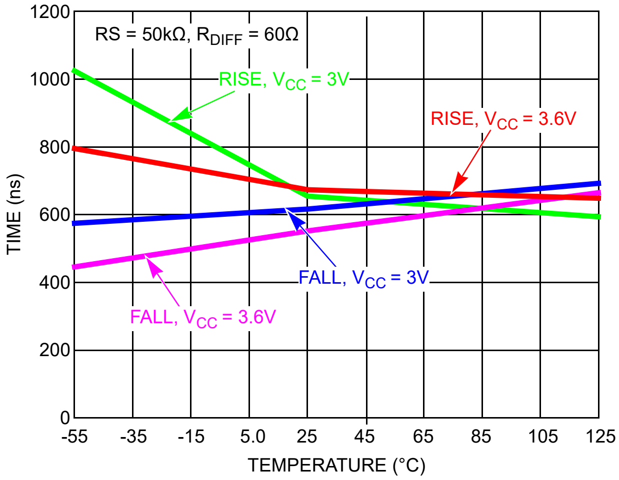


Figure 38. Transmitter Rise and Fall Times vs Temperature at Slow Speed

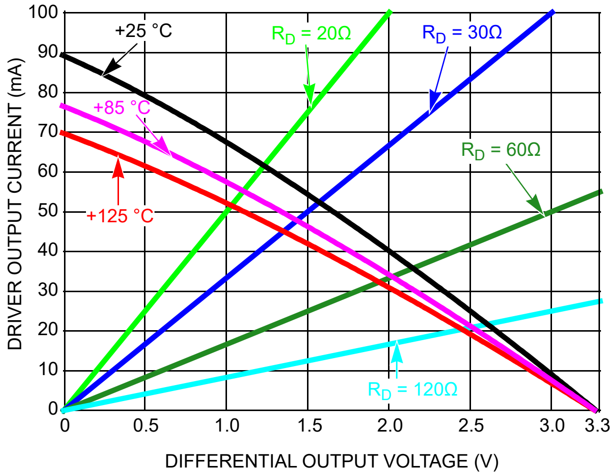


Figure 39. Driver Output Current vs Differential Output Voltage

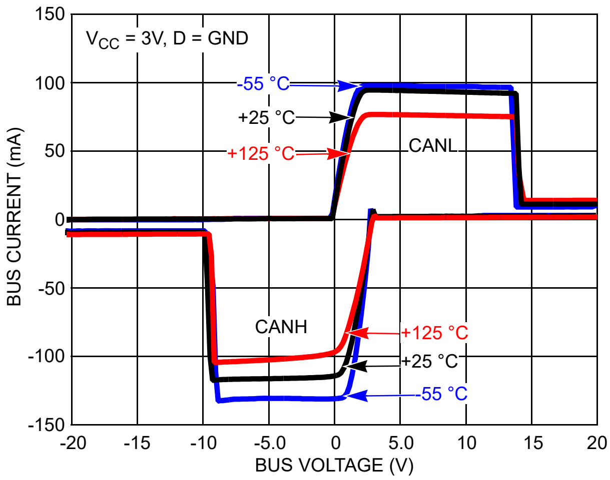


Figure 40. Driver Output Current vs Short-Circuit Voltage vs Temperature

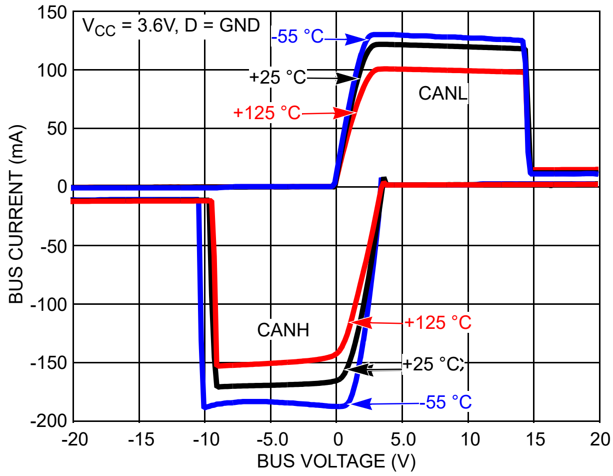


Figure 41. Driver Output Current vs Short-Circuit Voltage vs Temperature

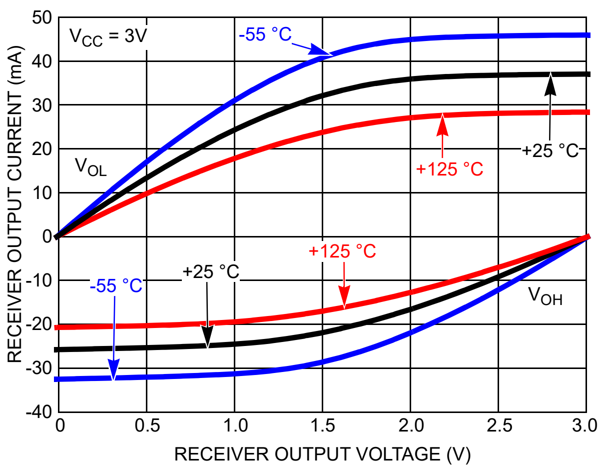


Figure 42. Receiver Output Current vs Receiver Output Voltage at VCC = 3V

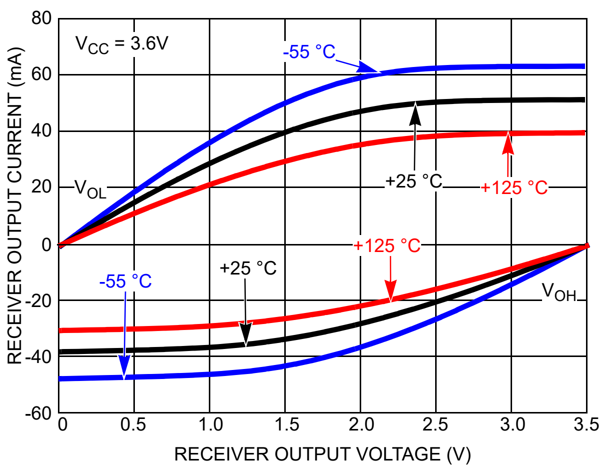


Figure 43. Receiver Output Current vs Receiver Output Voltage at VCC = 3.6V

V_{CC} = 3.3V, C_L = 15pF, T_A = +25°C; unless otherwise specified. **(Cont.)**

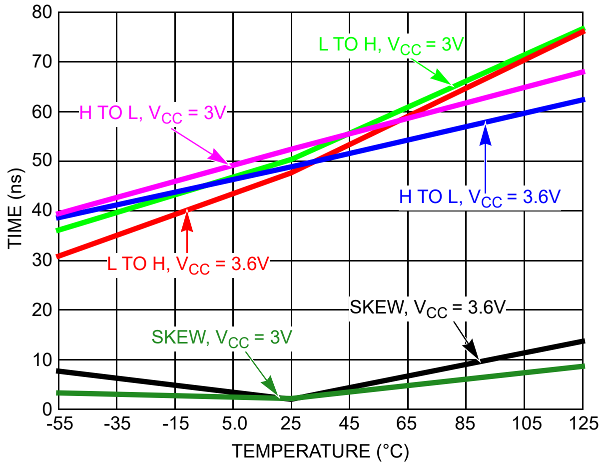


Figure 44. Receiver Propagation Delay and Skew vs Temperature

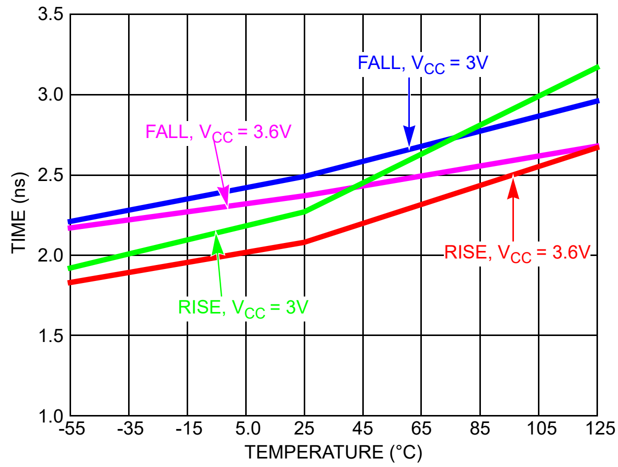


Figure 45. Receiver Rise and Fall Times vs Temperature

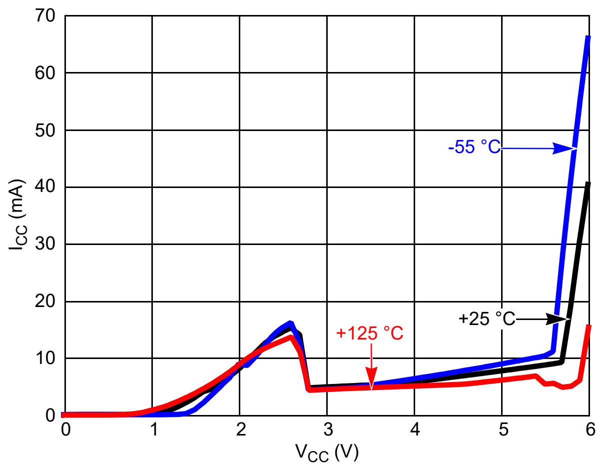


Figure 46. Supply Current vs Supply Voltage vs Temperature

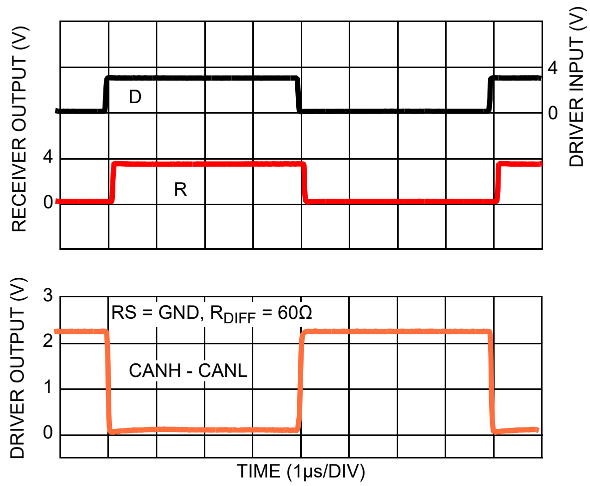


Figure 47. Fast Driver and Receiver Waveforms

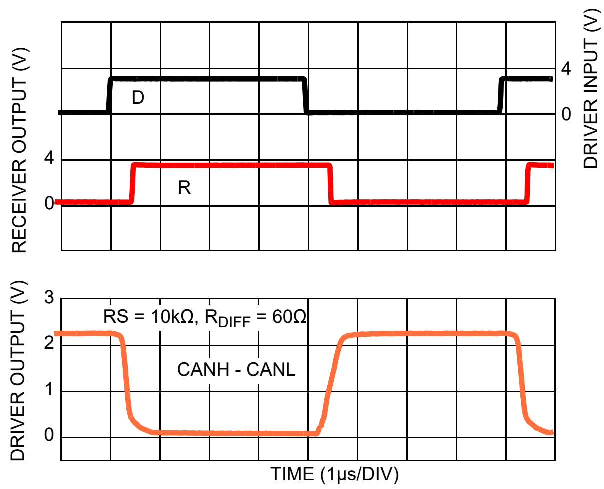


Figure 48. Medium Driver and Receiver Waveforms

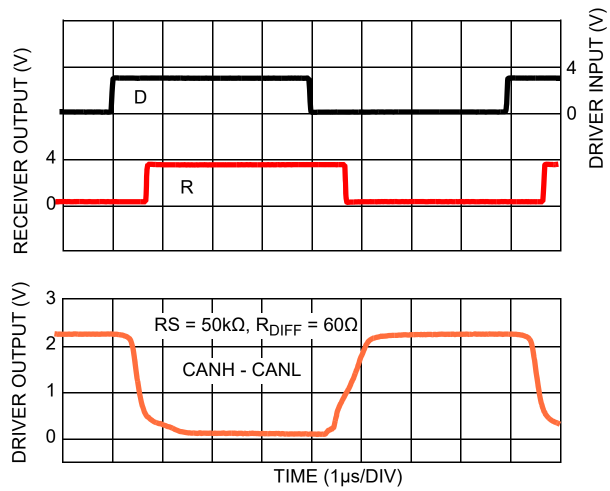


Figure 49. Slow Driver and Receiver Waveforms

4. Functional Description

4.1 Overview

The ISL72027SEH is a 3.3V radiation tolerant CAN transceiver that is compatible with the ISO11898-2 standard for use in CAN (Controller Area Network) serial communication systems.

The device performs transmit and receive functions between the CAN controller and the CAN differential bus. It can transmit and receive at bus speeds of up to 5Mbps. It operates over a common-mode range of -7V to +12V with a maximum of 120 nodes. The device can withstand ±20V on the CANH and CANL bus pins outside of ion beam and ±16V under ion beam.

4.2 Slope Adjustment

The output driver rise and fall time has three distinct selections that may be chosen by using a resistor from the RS pin to GND. Connecting the RS pin directly to GND results in output switching times that are the fastest, limited only by the drive capability of the output stage. RS = 10kΩ provides for a typical slew rate of 8V/µs and RS = 50kΩ provides for a typical slew rate of 4V/µs.

Putting a high logic level to the RS pin places the device in a low current listen mode. The protocol controller uses this mode to switch between low power listen mode and a normal transmit mode.

4.3 Cable Length

The device can work per ISO11898 specification with a 40m cable and stub length of 0.3m and 60 nodes at 1Mbps. This is greater than the ISO requirement of 30 nodes. The cable type specified is a twisted pair (shielded or unshielded) with a characteristic impedance of 120Ω. Resistors equal to this are to be terminated at both ends of the cable. Stubs should be kept as short as possible to prevent reflections.

4.4 Cold Spare

High reliability system designers implementing data communications have to be sensitive to the potential for single point failures. To mitigate the risk of a failure they will use redundant bus transceivers in parallel. Space systems call for high reliability in data communications that are resistant to single point failures. This is achieved by using a redundant bus transceiver in parallel. In this arrangement, both active and quiescent devices can be present simultaneously on the bus. The quiescent devices are powered down for cold spare and do not affect the communication of the other active nodes.

To achieve this, a powered down transceiver (V_{CC} < 200mV) has a resistance between the VREF pin or the CANH pin or CANL pin and the V_{CC} supply rail of >480kΩ (max) with a typical resistance >2MΩ. The resistance between CANH and CANL of a powered down transceiver has a typical resistance of 80kΩ.

4.5 Listen Mode

When a high level is applied to the RS pin, the device enters a low power listen mode. The driver of the transceiver is switched off to conserve power while the receiver remains active. In listen mode the transceiver draws 2mA (max) of current.

A low level on the RS pin brings the device back to normal operation.

4.6 Using 3.3V Devices in 5V Systems

Looking at the differential voltage of both the 3.3V and 5V devices, the differential voltage is the same, the recessive common-mode output is the same. The dominant common-mode output voltage is slightly lower than the 5V counterparts. The receiver specs are also the same. Though the electrical parameters appear compatible, it is advised that necessary system testing be performed to verify interchangeable operation.

4.7 Split Mode Termination

The VREF pin provides a $V_{CC}/2$ output voltage for split mode termination. The VREF pin has the same ESD protection, short-circuit protection, and common-mode operating range as the bus pins. The split mode termination technique is shown in Figure 50.

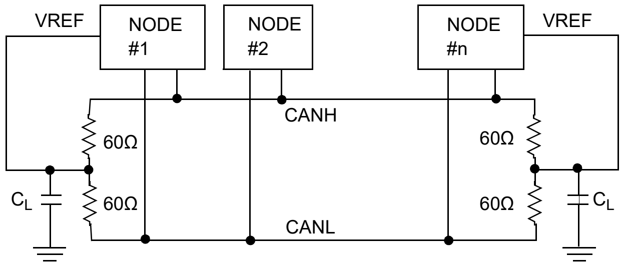


Figure 50. Split Termination

The technique stabilizes the bus voltage at $V_{CC}/2$ and prevent it from drifting to a high common-mode voltage during periods of inactivity. The technique improves the electromagnetic compatibility of a network. The split mode termination is put at each end of the bus.

The C_L capacitor between the two 60Ω resistors filters unwanted high frequency noise to ground. The resistors should have a tolerance of 1% or better and the two resistors should be carefully matched to provide the most effective EMI immunity. A typical value of C_L for a high speed CAN network is 4.7nF, which generates a 3dB point at 1.1Mbps. The capacitance value used is dependent on the signaling rate of the network.

5. Package and Die Characteristics

Table 1. Die and Assembly Related Information

Die Information	
Dimensions	2413µm x 3322µm (95 mils x 130.79 mils) Thickness: 305µm ±25µm (12 mils ±1 mil)
Interface Materials	
Glassivation	Type: 12kÅ Silicon Nitride on 3kÅ Oxide
Top Metallization	Type: 300Å TiN on 2.8µm AlCu In Bondpads, TiN has been removed.
Backside Finish	Silicon
Process	P6SOI
Assembly Information	
Substrate Potential	Floating
Additional Information	
Worst Case Current Density	$1.6 \times 10^5 A/cm^2$
Transistor Count	4055
Weight of Packaged Device	0.31 grams
Lid Characteristics	Finish: Gold Potential: Grounded, tied to package Pin 2

5.1 Metalization Mask Layout

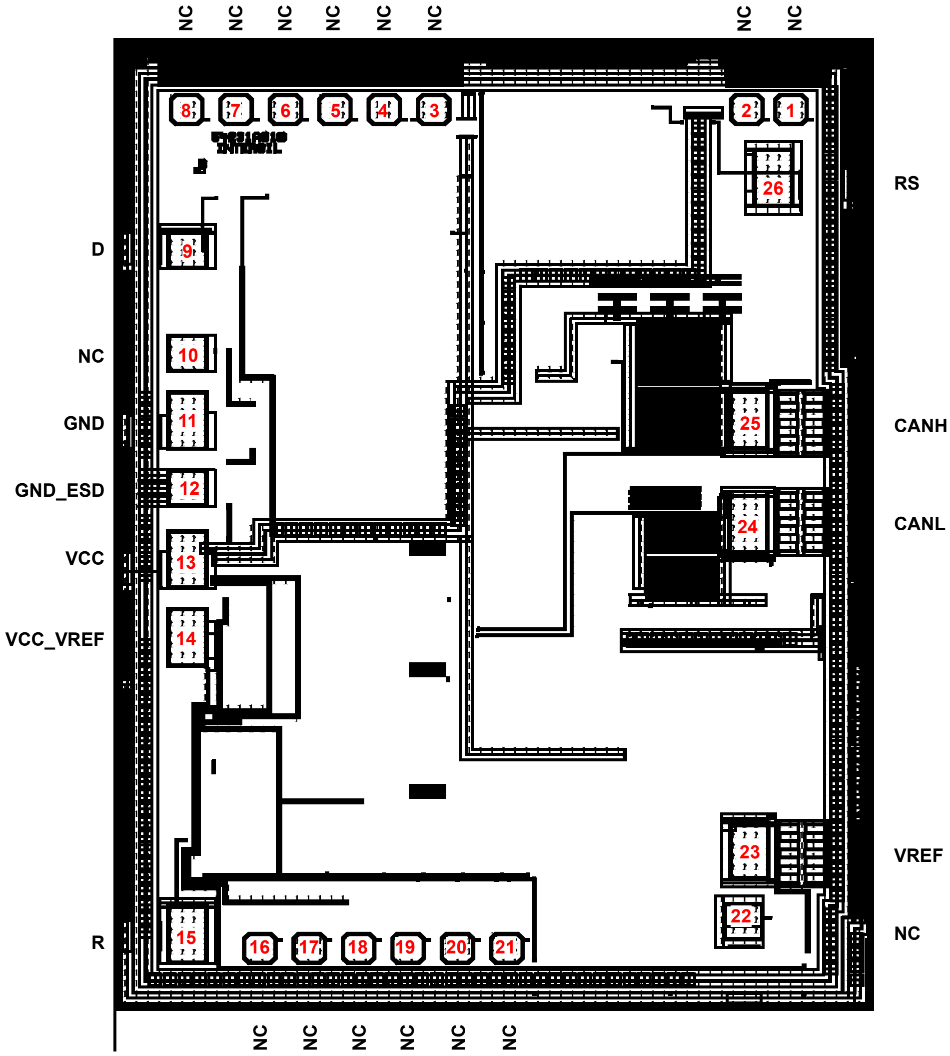


Table 2. ISL72027SEH Die Layout X-Y Coordinates[1]

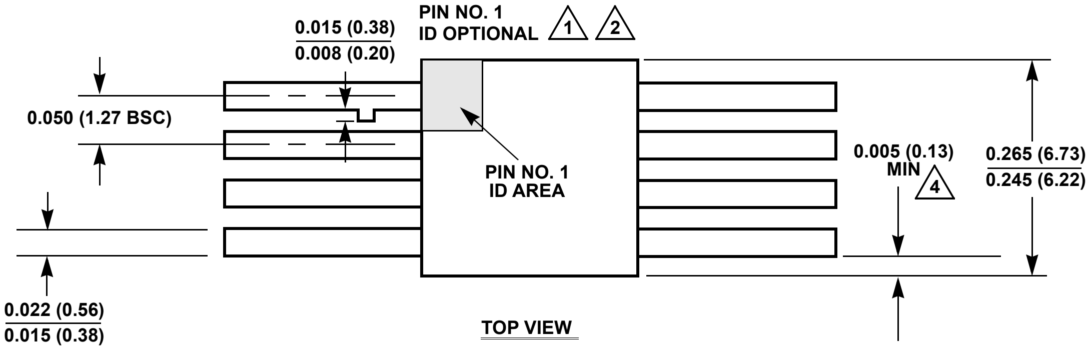
Pad Number	Pad Name	X (µm)	Y (µm)	X	Y
1	NC	90.0	90.0	901.4	1365.6
2	NC	90.0	90.0	767.4	1365.6
3	NC	90.0	90.0	-183.23	1365.6
4	NC	90.0	90.0	-333.25	1365.6
5	NC	90.0	90.0	-483.25	1365.6
6	NC	90.0	90.0	-633.25	1365.6
7	NC	90.0	90.0	-783.25	1365.6
8	NC	90.0	90.0	-933.25	1365.6
9	D	110.0	110.0	-931.1	901.85
10	NC	110.0	110.0	-931.1	563.25
11	GND	110.0	180.0	-931.1	342.25
12	GND_ESD	110.0	110.05	-931.1	119.42
13	VCC	110.0	180.0	-931.1	-115.05
14	VCC_VREF	110.0	180.05	-931.1	-371.08
15	R	110.0	180.0	-931.1	-1350.0
16	NC	90.0	90.0	-711.1	-1394.95
17	NC	90.0	90.0	-561.1	-1394.95
18	NC	90.0	90.0	-411.1	-1394.95
19	NC	90.0	90.0	-261.1	-1394.95
20	NC	90.0	90.0	-111.1	-1394.95
21	NC	90.0	90.0	38.9	-1394.95
22	NC	110.0	110.0	756.9	-1307.3
23	VREF	110.0	180.0	775.3	-1072.3
24	CANL	110.0	180.0	772.1	2.15
25	CANH	110.0	180.05	772.1	343.33
26	RS	110.0	180.0	848.1	1140.6

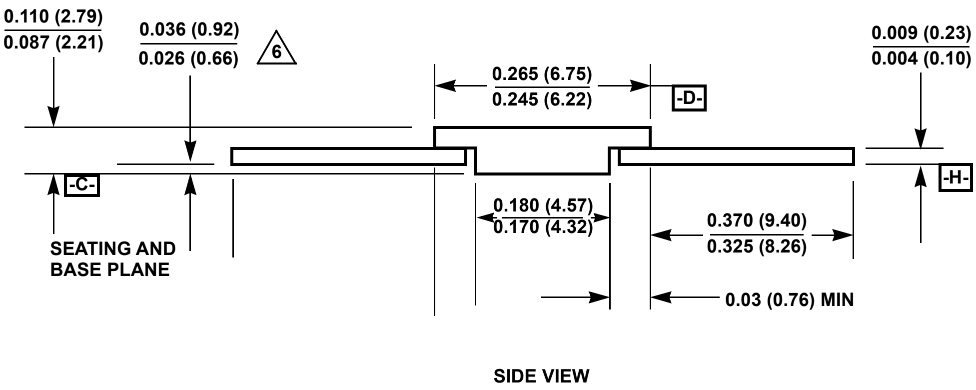
1. Origin of coordinates is the center of the die. NC - No Connect

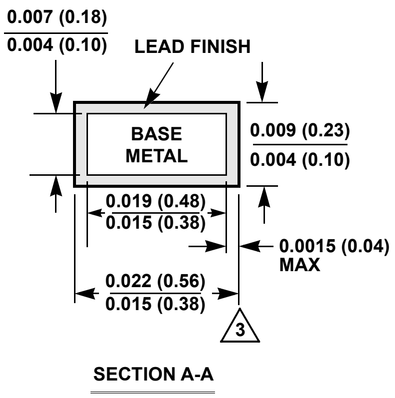
6. Package Outline Drawing

For the most recent package outline drawing, see K8.A.

K8.A
8 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE
Rev 4, 12/14







NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab may be used to identify pin one.
2. If a pin one identification mark is used in addition to or instead of a tab, the limits of the tab dimension do not apply.
3. The maximum limits of lead dimensions (section A-A) shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
4. Measure dimension at all four corners.
5. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
6. Dimension shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
7. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
8. Controlling dimension: INCH.

7. Ordering Information

Ordering/SMD Number[1]	Part Number[2]	Radiation Hardness (Total Ionizing Dose)	Package Description (RoHS Compliant)	Pkg. Dwg. #	Temp. Range
5962L1522802VXC	ISL72027SEHVF	LDR to 75krad(Si)	8 Ld Ceramic Flatpack	K8.A	-55 to +125°C
N/A	ISL72027SEHF/PROTO[3]	N/A			
5962L1522802V9A	ISL72027SEHVX[4]	LDR to 75krad(Si)	Die	-	
N/A	ISL72027SEHX/SAMPLE[3][4]	N/A			
N/A	ISL72027SEHEVAL1Z[5]	Evaluation Board			

1. Specifications for Radiation Tolerant QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed must be used when ordering.
2. These Pb-free Hermetic packaged products employ 100% Au plate -e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
3. The /PROTO and /SAMPLE are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions over-temperature specified in the DLA SMD and are in the same form and fit as the qualified device. The /SAMPLE die is capable of meeting the electrical limits and conditions specified in the DLA SMD at +25°C only. The /SAMPLE is a die and does not receive 100% screening over-temperature to the DLA SMD electrical limits. These part types do not come with a Certificate of Conformance because there is no Radiation Assurance testing and they are not DLA qualified devices.
4. Die product tested at T_A = + 25°C. The wafer probe test includes functional and parametric testing sufficient to make the die capable of meeting the electrical performance outlined in Electrical Specifications.
5. Evaluation boards utilize the /PROTO parts and /PROTO parts are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity.

Table 3. ISL7202xSEH Product Family Feature Table[1]

SPEC	ISL72026SEH	ISL72027SEH	ISL72028SEH
Loopback Feature	Yes	No	No
VREF Output	No	Yes	Yes
Listen Mode	Yes	Yes	No
Shutdown Mode	No	No	Yes
VTHRLM	1150mV (Max)	1150mV (Max)	N/A
VTHFLM	525mV (Min)	525mV (Min)	N/A
VHYSLM	50mV (Min)	50mV (Min)	N/A
Supply Current, Listen Mode	2mA (Max)	2mA (Max)	N/A
Supply Current, Shutdown Mode	N/A	N/A	50µA (Max)
VREF Leakage Current	N/A	±25µA (Max)	±25µA (Max)

1. N/A: Not Applicable

8. Revision History

Revision	Date	Description
3.01	Nov 16, 2023	Updated the Pin Descriptions table on page 3: Re-Ordered the Pin Numbers in sequential order from 1 - 8; Changed Pin 6 name to CANL and Pin 7 name to CANH to match the Pin Configuration diagram. Removed Related Literature and About Intersil sections. Updated the ordering information table: Added Radiation information; Added Notes 3, 4, and 5.
3.0	Aug 16, 2016	“Absolute Maximum Ratings” on page 5 changed voltage value in VCC to GND With/Without Ion Beam From: -0.3V to 4.5V To: -0.3V to 5.5V.
2.0	Apr 29, 2016	- Updated title. - Updated the test condition for Output Rise Time on page 8. - Changed maximum data rate from 1Mbps to 5Mbps in the following locations: - Second paragraph and “Features” section on page 1. - In “Overview” on page 12.
1.0	Nov 9, 2015	Absolute Maximum Ratings table on page 5: changed the value for “CANH, CANL, VREF Under Ion Beam” from ±16V to ±18V.
0.0	Oct 26, 2015	Initial Release

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