intersil

DATASHEET

ISL72028ASEH

3.3V Radiation Tolerant CAN Transceiver with Low Power Shutdown and Split Termination Output

FN8863
Rev.1.00
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The Intersil ISL72028ASEH is a radiation tolerant, 3.3V CAN transceiver that is compatible with the ISO11898-2 standard for applications calling for Controller Area Network (CAN) serial communication in satellites and aerospace communications, and telemetry data processing in harsh industrial environments.

This device can transmit and receive at bus speeds up to 5Mbps. It can drive a 40m cable at 1Mbps according to the ISO11898-2 specification. The device is designed to operate over a common-mode range of -7V to +12V, with a maximum of 120 nodes. The device has three discrete selectable driver rise/fall time options, a Low Power Shutdown mode, and a split termination output.

The Receiver (Rx) inputs feature a “full fail-safe” design, which ensures a logic high Rx output if the Rx inputs are floating, shorted, or terminated but undriven.

The ISL72028ASEH is available in an 8 Ld hermetic ceramic flatpack and die form that operate across the temperature range of -55°C to +125°C. The logic inputs are tolerant with 5V systems.

Other CAN transceivers available are the ISL72026ASEH and ISL72027ASEH. For a list of differences between these devices, refer to Table 1 on page 4.

Related Literature

- For a full list of related documents, visit our website
  - ISL72028ASEH product page

Applications

- Satellites and aerospace communications
- Telemetry data processing
- High-end industrial environments and harsh environments

Features

- Electrically screened to SMD 5962-15228
- ESD protection on all pins: 4kV HBM
- Compatible with ISO11898-2
- Operating supply range: 3.0V to 3.6V
- Bus pin fault protection to ±20V
- Undervoltage lockout
- Cold spare: powered down devices/nodes do not affect active devices operating in parallel
- Three selectable driver rise and fall times:
  - Fast speed (RS = 0V) - edges and propagation delays optimized for a data rate of 1Mbps
  - Medium speed (RS = 10kΩ) - edges and propagation delays optimized for a data rate of 500kbps
  - Slow Speed (RS = 50kΩ) - edges and propagation delays optimized for a data rate of 250kbps
- Glitch-free bus I/O during power-up and power-down
- Full fail-safe (open, short, terminated/undriven) receiver
- Hi-Z input allows for 120 nodes on the bus
- High data rates up to 5Mbps
- Quiescent supply current: 7mA (maximum)
- Low-power Shutdown mode: 50µA (maximum)
- -7V to +12V common-mode input voltage range
- 5V tolerant logic inputs
- Thermal shutdown
- Acceptance tested to 75krad(Si) (LDR) wafer-by-wafer
- Radiation tolerance
  - SEL/B immune to LET_{TH}: 86.4MeV•cm^2/mg
  - Low dose rate (0.01rad(Si)/s): 75krad(Si)

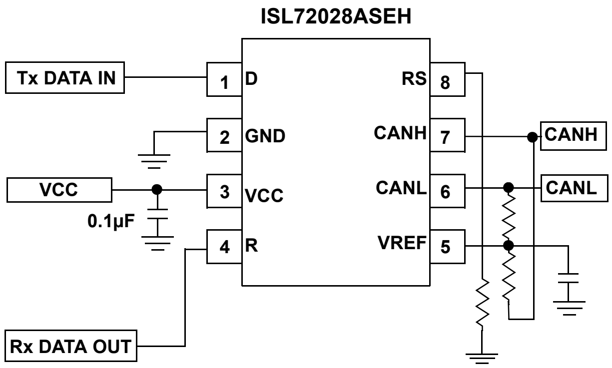


Figure 1. Typical Application

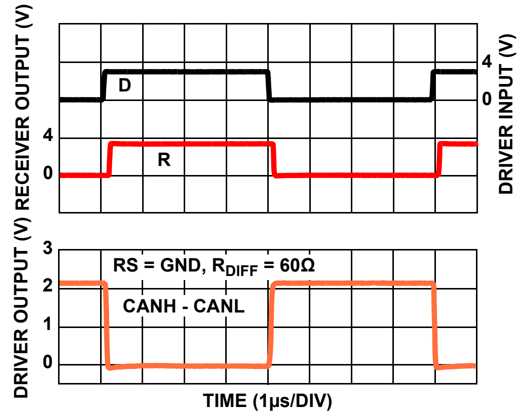


Figure 2. Fast Driver and Receiver Waveforms

Contents

1. Overview

1.1 Ordering Information

Ordering/ SMD Number (Note 1)	Part Number (Note 2)	Temp Range (°C)	Package (RoHS Compliant)	Pkg. Dwg. #
5962L1522809VXC	ISL72028ASEHVF	-55 to +125	8 Ld Ceramic Flatpack	K8.A
N/A	ISL72028ASEHF/PROTO, (Note 3)	-55 to +125	8 Ld Ceramic Flatpack	K8.A
5962L1522809V9A	ISL72028ASEHVX	-55 to +125	Die	
N/A	ISL72028ASEHX/SAMPLE, (Note 3)	-55 to +125	Die	
N/A	ISL72028ASEHEVAL1Z, (Note 4)	Evaluation Board		

Notes:
1. Specifications for Radiation Tolerant QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed in the Ordering Information must be used when ordering.
2. These Intersil Pb-free Hermetic packaged products employ 100% Au plate -e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
3. The /PROTO and /SAMPLE are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions over-temperature specified in the DLA SMD and are in the same form and fit as the qualified device. The /SAMPLE die is capable of meeting the electrical limits and conditions specified in the DLA SMD at +25°C only. The /SAMPLE is a die and does not receive 100% screening over-temperature to the DLA SMD electrical limits. These part types do not come with a Certificate of Conformance because there is no radiation assurance testing and they are not DLA qualified devices.
4. Evaluation boards use the /PROTO parts. The /PROTO parts are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity.

Table 1. ISL7202xASEH Product Family Feature Table

Specification	ISL72026ASEH	ISL72027ASEH	ISL72028ASEH
Loopback Feature	Yes	No	No
VREF Output	No	Yes	Yes
Listen Mode	Yes	Yes	No
Shutdown Mode	No	No	Yes
VTHRLM	900mV (maximum)	900mV (maximum)	N/A
VTHFLM	325mV (minimum)	325mV (minimum)	N/A
VHYSLM	40mV (minimum)	40mV (minimum)	N/A
Supply Current, Listen Mode	2mA (maximum)	2mA (maximum)	N/A
Supply Current, Shutdown Mode	N/A	N/A	50µA (maximum)
VREF Leakage Current	N/A	±25µA (maximum)	±25µA (maximum)

Note: N/A = Not Applicable

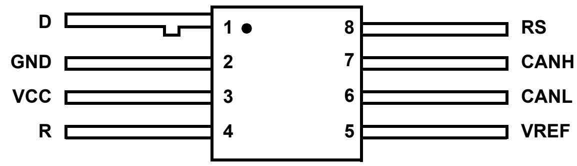
Table 2. Product Family Comparison for Data Rate and Total Dose Radiation Testing

Specification	ISL7202xSEH	ISL7202xASEH	ISL7202xBSEH	ISL7202xCSEH
Data Rate: RS = 0V	1Mbps	1Mbps	1Mbps	1Mbps
Data Rate: RS = 10kΩ	250kbps	500kbps	250kbps	500kbps
Data Rate: RS = 50kΩ	125kbps	250kbps	125kbps	250kbps
HDR 100krad(Si)) Testing	No	No	Yes	Yes
LDR 75krad(Si) Testing	Yes	Yes	Yes	Yes

Note: HDR = High Dose Rate, LDR = Low Dose Rate

1.2 Pin Configuration

ISL72028ASEH
(8 Ld Ceramic Flatpack)
Top View



Note: The package lid is tied to ground.

1.3 Pin Descriptions

Pin Number	Pin Name	Function
1	D	CAN driver digital input. The bus states are LOW = dominant and HIGH = recessive. Internally tied HIGH.
2	GND	Ground connection
3	VCC	System power supply input (3.0V to 3.6V). The typical voltage for the device is 3.3V.
4	R	CAN data receiver output. The bus states are LOW = dominant and HIGH = recessive.
5	VREF	VCC/2 reference output for Split mode termination.
6	CANL	CAN bus line for low level output.
7	CANH	CAN bus line for high level output.
8	RS	A resistor to GND from this pin controls the rise and fall time of the CAN output waveform. Drive RS HIGH to put the device in Low Power Shutdown mode.

1.4 Equivalent Input and Output Schematic Diagrams

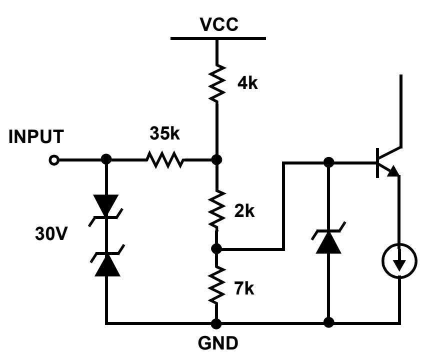


Figure 3. CANH and CANL Inputs

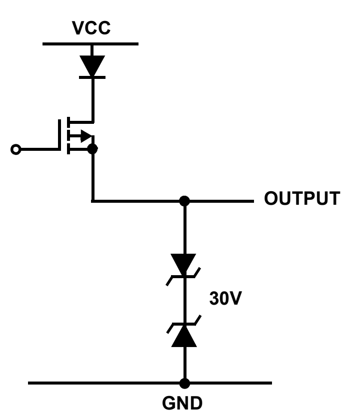


Figure 4. CANH Output

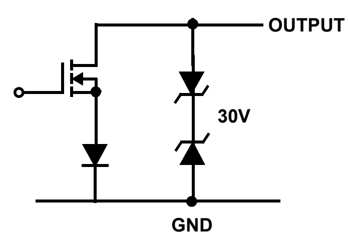


Figure 5. CANL Output

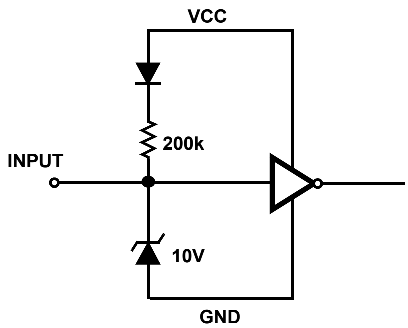


Figure 6. D Input

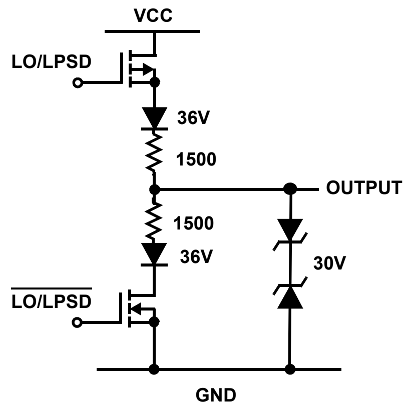


Figure 7. R Output

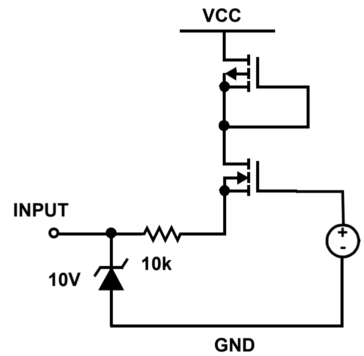


Figure 8. RS Input

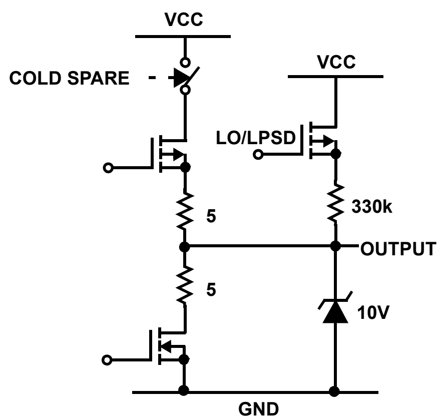


Figure 9. VREF

2. Specifications

2.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
VCC to GND with/without Ion Beam	-0.3	5.5	V
CANH, CANL, VREF Under Ion Beam		±20	V
CANH, CANL, VREF		±20	V
I/O Voltages D, R, RS	-0.5	7	V
Receiver Output Current	-10	10	mA
Output Short-Circuit Duration	Continuous		
ESD Rating	**Value**		**Unit**
Human Body Model (Tested per MIL-PRF-883 3015.7)			
CANH, CANL Bus Pins	4		kV
All Other Pins	4		kV
Charged Device Model (Tested per JS-002-2014)	750		V
Machine Model (Tested per JESD22-A115A)	200		V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

2.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Ld Flatpack Package (Notes 5, 6)	39	7

Notes:
5. θ_{JA} is measured with the component mounted on a high-effective thermal conductivity test board (two buried 1oz copper planes) with “direct attach” features package base mounted to a PCB thermal land with a 10 mil gap fill material having a thermal conductivity of 1W/m-K. Refer to TB379.
6. For θ_{JC}, the “case temp” location is the center of the package underside.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature		+150	°C
Storage Temperature Range	-65	+150	°C

2.3 Recommended Operation Conditions

Parameter	Minimum	Maximum	Unit
Temperature Range	-55	+125	°C
V_{CC} Supply Voltage	3	3.6	V
Voltage on CAN I/O	-7	12	V
V_{IH} D Logic Pin	2	5.5	V
V_{IL} D Logic Pin	0	0.8	V
I_{OH} Driver (CANH - CANL = 1.5V, V_{CC} = 3.3V)		-40	mA
I_{OH} Receiver (V_{OH} = 2.4V)		-4	mA
I_{OL} Driver (CANH - CANL = 1.5V, V_{CC} = 3.3V)		40	mA
I_{OL} Receiver (V_{OL} = 0.4V)		4	mA

2.4 Electrical Specifications

Test Conditions: V_{CC} = 3V to 3.6V; typical values are at T_A = +25°C (Note 9), unless otherwise specified (Note 7). **Boldface limits apply across the operating temperature range, -55°C to +125°C, over a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s, and over a total ionizing dose of 100krad(SI) at +25°C with exposure of a high dose rate of 50krad(SI)/s to 300krad(SI)/s.**

Parameter	Symbol	Test Conditions		Temp (°C)	Min (Note 8)	Typ (Note 9)	Max (Note 8)	Unit
Driver Electrical Characteristics								
Dominant Bus Output Voltage	$V_{O(DOM)}$	D = 0V, CANH, RS = 0V, Figures 10 and 11	3V ≤ V_{CC} ≤ 3.6V	Full	**2.25**	2.85	**V_{CC}**	V
		D = 0V, CANL, RS = 0V, Figures 10 and 11		Full	**0.10**	0.65	**1.25**	V
Recessive Bus Output Voltage	$V_{O(REC)}$	D = 3V, CANH, RS = 0V, 60Ω and no load, Figures 10 and 11	3V ≤ V_{CC} ≤ 3.6V	Full	**1.80**	2.30	**2.70**	V
		D = 3V, CANL, RS = 0V, 60Ω and no load, Figures 10 and 11		Full	**1.80**	2.30	**2.80**	V
Dominant Output Differential Voltage	$V_{OD(DOM)}$	D = 0V, RS = 0V, 3V ≤ V_{CC} ≤ 3.6V, Figures 10 and 11		Full	**1.5**	2.2	**3.0**	V
		D = 0V, RS = 0V, 3V ≤ V_{CC} ≤ 3.6V, Figures 11 and 12		Full	**1.2**	2.1	**3.0**	V
Recessive Output Differential Voltage	$V_{OD(REC)}$	D = 3V, RS = 0V, 3V ≤ V_{CC} ≤ 3.6V, Figures 10 and 11		Full	**-120**	0.2	**12**	mV
		D = 3V, RS = 0V, 3.0V ≤ V_{CC} ≤ 3.6V, no load		Full	**-500**	-34	**50**	mV
Logic Input High Voltage (D)	V_{IH}	3V ≤ V_{CC} ≤ 3.6V, (Note 10)		Full	**2.0**	-	**5.5**	V
Logic Input Low Voltage (D)	V_{IL}	3V ≤ V_{CC} ≤ 3.6V, (Note 10)		Full	**0**	-	**0.8**	V
High Level Input Current (D)	I_{IH}	D = 2V, 3V ≤ V_{CC} ≤ 3.6V		Full	**-30**	-3	**30**	µA
Low Level Input Current (D)	I_{IL}	D = 0.8V, 3V ≤ V_{CC} ≤ 3.6V		Full	**-30**	-7	**30**	µA
RS Input Voltage for Listen Mode	$V_{IN(RS)}$	3V ≤ V_{CC} ≤ 3.6V		Full	**0.75xV_{CC}**	1.9	**5.5**	V
Output Short-Circuit Current	I_{OSC}	V_{CANH} = -7V, CANL = OPEN, 3V ≤ V_{CC} ≤ 3.6V, Figures 22 and 23		Full	**-250**	-100	-	mA
		V_{CANH} = +12V, CANL = OPEN, 3V ≤ V_{CC} ≤ 3.6V, Figures 22 and 23		Full	-	0.4	**1.0**	mA
		V_{CANL} = -7V, CANH = OPEN, 3V ≤ V_{CC} ≤ 3.6V, Figures 22 and 23		Full	**-1.0**	-0.4	-	mA
		V_{CANL} = +12V, CANH = OPEN, 3V ≤ V_{CC} ≤ 3.6V, Figures 22 and 23		Full	-	100	**250**	mA
Thermal Shutdown Temperature	T_{SHDN}	3V < V_{IN} < 3.6V		-	-	163	-	°C
Thermal Shutdown Hysteresis	T_{HYS}	3V < V_{IN} < 3.6V		-	-	12	-	°C
Receiver Electrical Characteristics								
Input Threshold Voltage (Rising)	V_{THR}	RS = 0V, 10k, 50k, (recessive to dominant), Figures 15, 16, and 17		Full	-	700	**900**	mV
Input Threshold Voltage (Falling)	V_{THF}	RS = 0V, 10k, 50k, (dominant to recessive), Figures 15, 16, and 17		Full	**500**	625	-	mV
Input Hysteresis	V_{HYS}	(V_{THR} - V_{THF}), RS = 0V, 10k, 50k, Figures 15, 16, and 17		Full	**40**	80	-	mV

Test Conditions: V_{CC} = 3V to 3.6V; typical values are at T_A = +25°C (Note 9), unless otherwise specified (Note 7). **Boldface limits apply across the operating temperature range, -55°C to +125°C, over a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s, and over a total ionizing dose of 100krad(SI) at +25°C with exposure of a high dose rate of 50krad(SI)/s to 300krad(SI)/s. (Continued)**

Parameter	Symbol	Test Conditions	Temp (°C)	Min (Note 8)	Typ (Note 9)	Max (Note 8)	Unit
Receiver Output High Voltage	V_{OH}	I_O = -4mA	Full	**2.4**	V_{CC} - 0.2	-	V
Receiver Output Low Voltage	V_{OL}	I_O = +4mA	Full	-	0.2	**0.4**	V
Input Current for CAN Bus	I_{CAN}	CANH or CANL at 12V, D = 3V, other bus pin at 0V, RS = 0V	Full	-	470	**600**	µA
		CANH or CANL at 12V, D = 3V, V_{CC} = 0V, other bus pin at 0V, RS = 0V	Full	-	170	**275**	µA
		CANH or CANL at -7V, D = 3V, other bus pin at 0V, RS = 0V	Full	**-500**	-350	-	µA
		CANH or CANL at -7V, D = 3V, V_{CC} = 0V, other bus pin at 0V, RS = 0V	Full	**-175**	-100	-	µA
Input Capacitance (CANH or CANL)	C_{IN}	Input to GND, D = 3V, RS = 0V	25	-	35	-	pF
Differential Input Capacitance	C_{IND}	Input to Input, D = 3V, RS = 0V	25	-	15	-	pF
Input Resistance (CANH or CANL)	R_{IN}	Input to GND, D = 3V, RS = 0V	Full	**20**	40	**50**	kΩ
Differential Input Resistance	R_{IND}	Input to Input, D = 3V, RS = 0V	Full	**40**	80	**100**	kΩ
Supply Current							
Supply Current, Low Power Shutdown Mode	$I_{CC(LPS)}$	RS = D = V_{CC}, 3V ≤ V_{CC} ≤ 3.6V	Full	-	120	**50**	mA
Supply Current, Dominant	$I_{CC(DOM)}$	D = RS = 0V, no load, 3V ≤ V_{CC} ≤ 3.6V	Full	-	5	**7**	mA
Supply Current, Recessive	$I_{CC(REC)}$	D = V_{CC}, RS = 0V, no load, 3V ≤ V_{CC} ≤ 3.6V	Full	-	2.6	**5.0**	mA
Cold Sparing Bus Current							
CANH Leakage Current	$I_{L(CANH)}$	V_{CC} = 0.2V, CANH = -7V or 12V, D = V_{CC}, CANL = float, RS = 0V	Full	**-25**	**-4**	**25**	µA
CANL Leakage Current	$I_{L(CANL)}$	V_{CC} = 0.2V, CANL = -7V or 12V, D = V_{CC}, CANH = float, RS = 0V	Full	**-25**	-4	**25**	µA
V_{REF} Leakage Current	$I_{L(VREF)}$	V_{CC} = 0.2V, V_{REF} = -7V or 12V, D = V_{CC}	Full	**-25**	0.01	**25**	µA
Driver Switching Characteristics							
Propagation Delay LOW to HIGH	t_{PDLH1}	RS = 0V, Figures 13 and 14	Full	-	90	**160**	ns
Propagation Delay LOW to HIGH	t_{PDLH2}	RS = 10kΩ, Figures 13 and 14	Full	-	350	**550**	ns
Propagation Delay LOW to HIGH	t_{PDLH3}	RS = 50kΩ, Figures 13 and 14	Full	-	475	**800**	ns
Propagation Delay HIGH to LOW	t_{PDHL1}	RS = 0V, Figures 13 and 14	Full	-	115	**180**	ns
Propagation Delay HIGH to LOW	t_{PDHL2}	RS = 10kΩ, Figures 13 and 14	Full	-	410	**600**	ns
Propagation Delay HIGH to LOW	t_{PDHL3}	RS = 50kΩ, Figures 13 and 14	Full	-	550	**900**	ns
Output Skew	t_{SKEW1}	RS = 0V, ($\|t_{PHL} - t_{PLH}\|$), Figures 13 and 14	Full	-	20	**65**	ns

Test Conditions: V_{CC} = 3V to 3.6V; typical values are at T_A = +25°C (Note 9), unless otherwise specified (Note 7). **Boldface limits apply across the operating temperature range, -55°C to +125°C, over a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s, and over a total ionizing dose of 100krad(SI) at +25°C with exposure of a high dose rate of 50krad(SI)/s to 300krad(SI)/s. (Continued)**

Parameter	Symbol	Test Conditions	Temp (°C)	Min (Note 8)	Typ (Note 9)	Max (Note 8)	Unit
Output Skew	t_{SKEW2}	RS = 10kΩ, (|t_{PHL} - t_{PLH}|), Figures 13 and 14	Full	-	60	**275**	ns
Output Skew	t_{SKEW3}	RS = 50kΩ, (|t_{PHL} - t_{PLH}|), Figures 13 and 14	Full	-	75	**400**	ns
Output Rise Time	t_{r1}	RS = 0V, (fast speed - 1Mbps) Figures 13 and 14	Full	**15**	30	**85**	ns
Output Fall Time	t_{f1}		Full	**10**	20	**65**	ns
Output Rise Time	t_{r2}	RS = 10kΩ, (medium speed - 500kbps) Figures 13 and 14	Full	**125**	250	**550**	ns
Output Fall Time	t_{f2}		Full	**100**	250	**425**	ns
Output Rise Time	t_{r3}	RS = 50kΩ, (slow speed - 250kbps) Figures 13 and 14	Full	**200**	360	**800**	ns
Output Fall Time	t_{f3}		Full	**175**	390	**600**	ns
Total Loop Delay, Driver Input to Receiver Output, Recessive to Dominant	$t_{(LOOP1)}$	RS = 0V, Figures 18 and 19	Full	-	140	**225**	ns
		RS = 10kΩ, Figures 18 and 19	Full	-	380	**600**	ns
		RS = 50kΩ, Figures 18 and 19	Full	-	500	**800**	ns
Total Loop Delay, Driver Input to Receiver Output, Dominant to Recessive	$t_{(LOOP2)}$	RS = 0V, Figures 18 and 19	Full	-	160	**285**	ns
		RS = 10kΩ, Figures 18 and 19	Full	-	450	**700**	ns
		RS = 50kΩ, Figures 18 and 19	Full	-	575	**950**	ns
Low Power Shutdown to Valid Dominant Time	$t_{L-DOM)}$	Figures 20 and 21, (Note 11)	Full	-	6	**15**	µs
Receiver Switching Characteristics							
Propagation Delay LOW to HIGH	t_{PLH}	Figures 15, 16, and 17	Full	-	50	**110**	ns
Propagation Delay HIGH to LOW	t_{PHL}	Figures 15, 16, and 17	Full	-	50	**110**	ns
Rx Skew	t_{SKEW1}	|(t_{PHL} - t_{PLH})|, Figures 15, 16, and 17	Full	-	2	**35**	ns
Rx Rise Time	t_r	Figures 15, 16, and 17	Full	-	2	-	ns
Rx Fall Time	t_f	Figures 15, 16, and 17	Full	-	2	-	ns
VREF/RS Pin Characteristics							
VREF Pin Voltage	V_{REF}	-5µA < I_{REF} < 5µA	Full	**0.45xV_{CC}**	1.60	**0.55xV_{CC}**	V
		-50µA < I_{REF} < 50µA	Full	**0.4xV_{CC}**	1.6	**0.6xV_{CC}**	V
RS Pin Input Current	$I_{RS(H)}$	RS = 0.75 x V_{CC}	Full	**-10.0**	-0.2	-	µA
	$I_{RS(L)}$	V_{RS} = 0V	Full	**-450**	-125	**0**	µA

Notes:

7. All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.
8. Parameters with MIN and/or MAX limits are 100% tested at -55°C, +25°C, and +125°C, unless otherwise specified.
9. Typical values are at 3.3V. Parameters with a single entry in the "TYP" column apply to 3.3V. Typical values shown are not guaranteed.
10. Parameter included in functional testing.
11. Performed during the 100% screening operations across the full operating temperature range. Not performed as part of TCI Group E and Group C. Radiation characterization testing performed as part of the initial release and any major changes in design.

2.5 Test Circuits and Waveforms

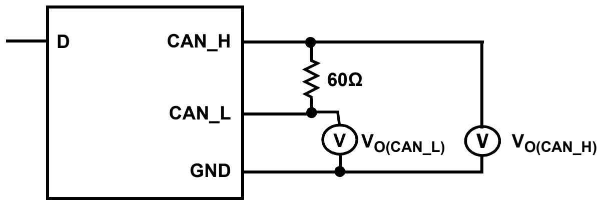


Figure 10. Driver Test Circuit

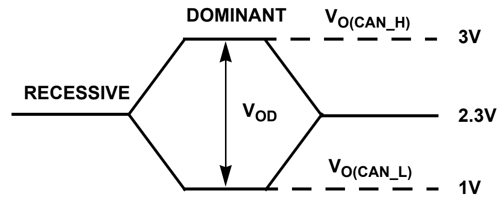


Figure 11. Driver Bus Voltage Definitions

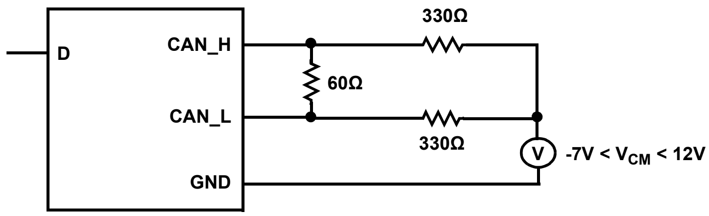
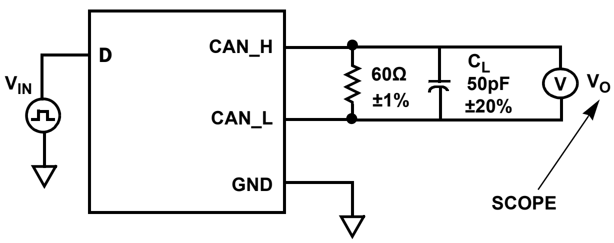


Figure 12. Driver Common-Mode Circuit



V_{IN} = 125kHz, 0V to V_{CC}, duty cycle 50%, $t_r = t_f \leq 6ns$, $Z_O = 50\Omega$
C_L includes fixture and instrumentation capacitance

Figure 13. Driver Timing Test Circuit

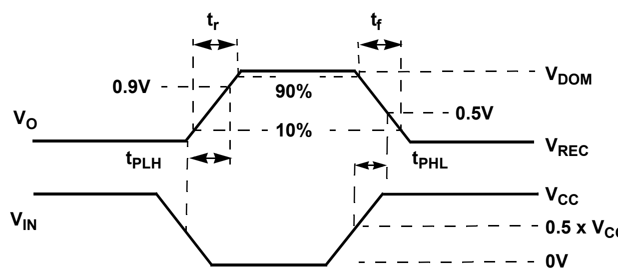


Figure 14. Driver Timing Measurement Points

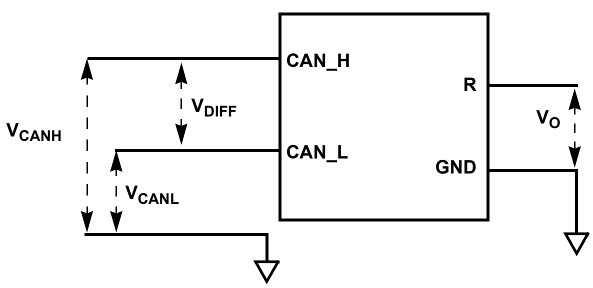
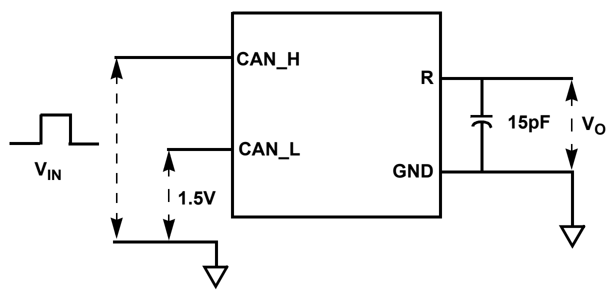


Figure 15. Receiver Voltage Definitions



V_{IN} = 125kHz, duty cycle 50%, $t_r = t_f = 6ns$, $Z_O = 50\Omega$
C_L includes test setup capacitance

Figure 16. Receiver Test Circuit

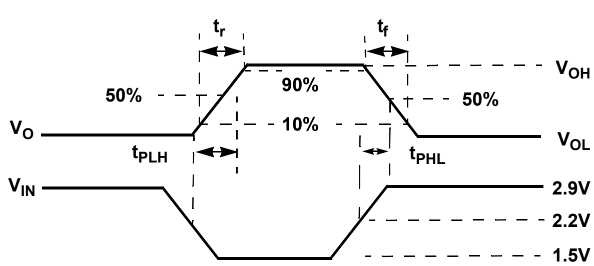


Figure 17. Receiver Test Measurement Points

Table 3. Differential Input Voltage Threshold Test

Input		Output	Measured
V_{CANH}	V_{CANL}	R	V_{DIFF}
-6.1V	-7V	L	900mV
12V	11.1V	L	900mV
-1V	-7V	L	6V
12V	6V	L	6V
-6.5V	-7V	H	500mV
12V	11.5V	H	500mV
-7V	-1V	H	6V
6V	12V	H	6V
Open	Open	H	X

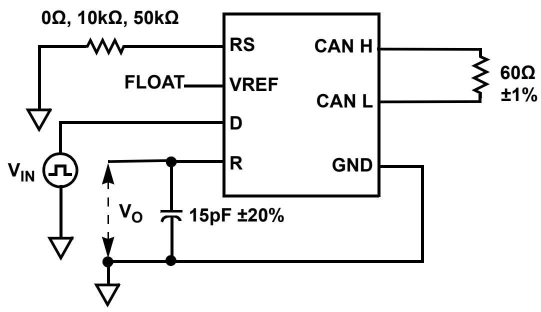


Figure 18. Total Loop Delay Test Circuit

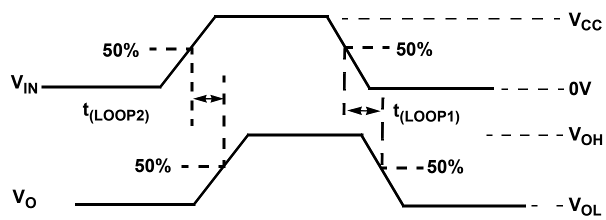


Figure 19. Total Loop Delay Measurement Points

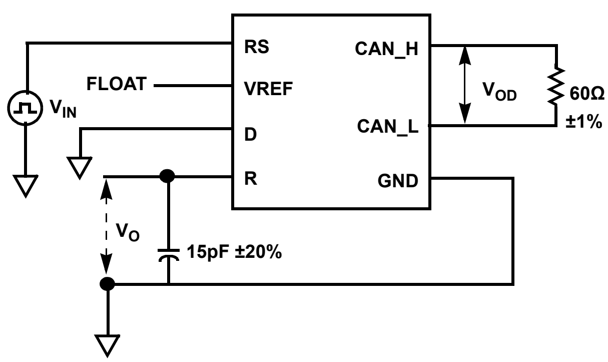


Figure 20. Low Power Shutdown to Dominant Time Circuit

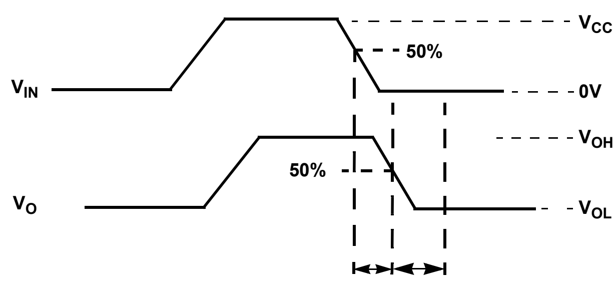


Figure 21. Low Power Shutdown to Dominant Time Measurement Points

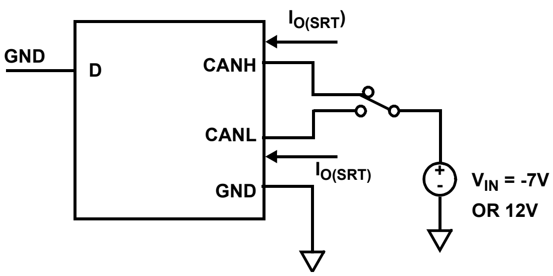


Figure 22. Output Short-Circuit Current Circuit

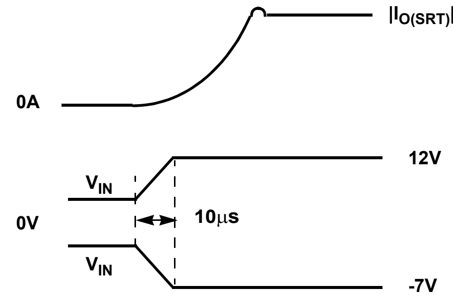


Figure 23. Output Short-Circuit Current Waveforms

3. Typical Performance Curves

V_{CC} = 3.3V, C_L = 15pF, T_A = +25°C; unless otherwise specified.

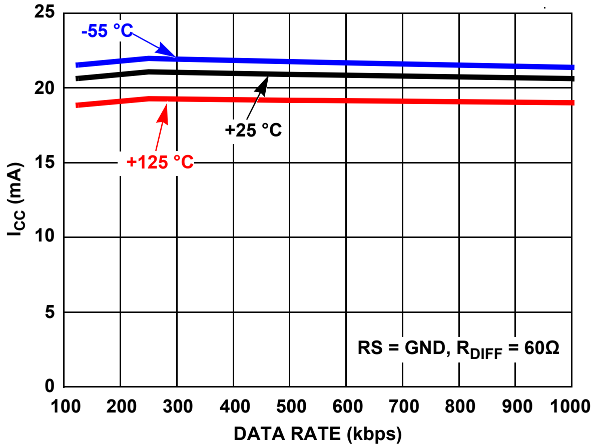


Figure 24. Supply Current vs Fast Data Rate vs Temperature

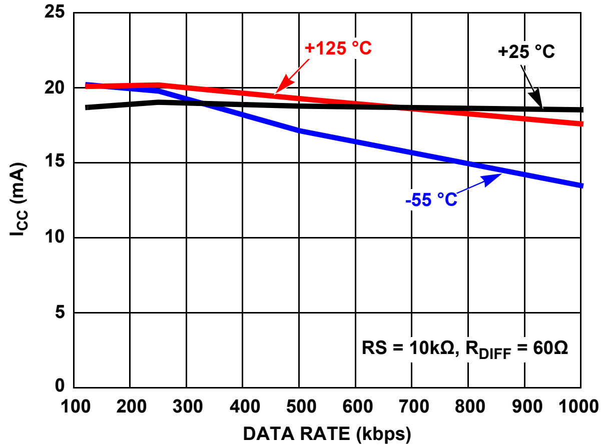


Figure 25. Supply Current vs Medium Data Rate vs Temperature

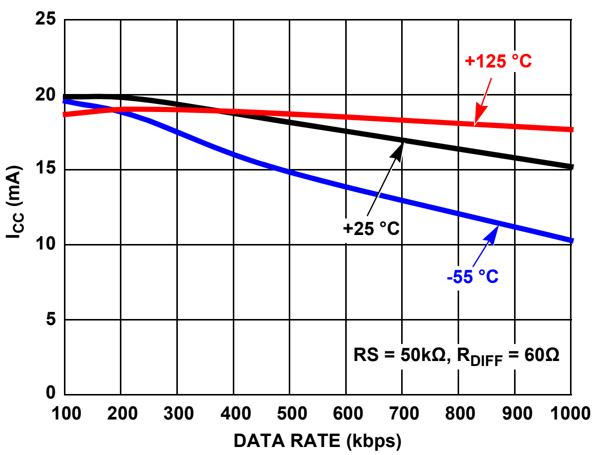


Figure 26. Supply Current vs Slow Data Rate vs Temperature

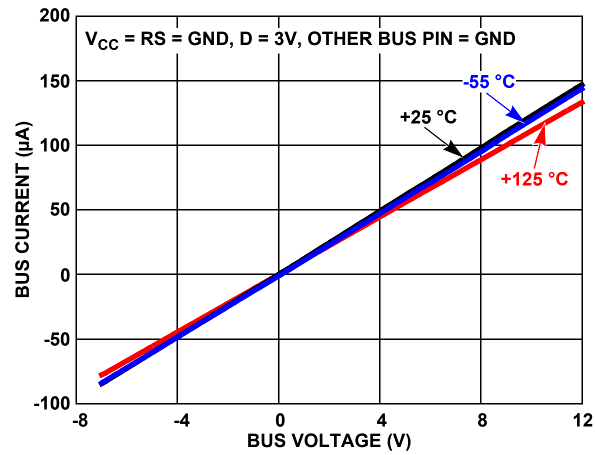


Figure 27. Bus Pin Leakage vs V_{CM} at V_{CC} = 0V

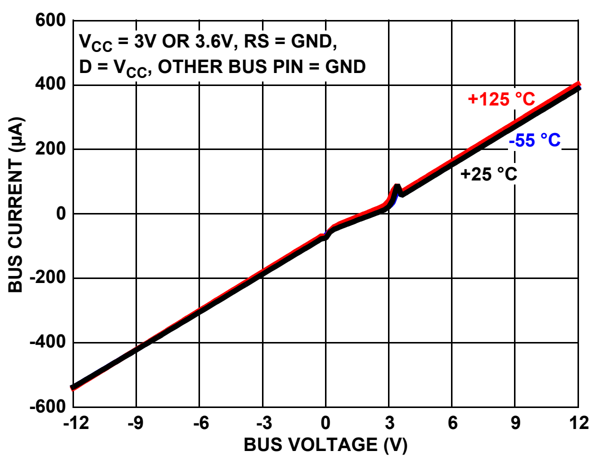


Figure 28. Bus Pin Leakage vs ±12V V_{CM}

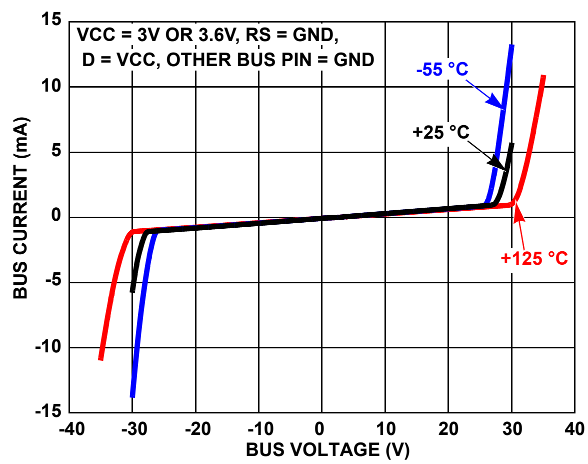


Figure 29. Bus Pin Leakage vs ±35V V_{CM}

V_{CC} = 3.3V, C_L = 15pF, T_A = +25°C; unless otherwise specified. **(Continued)**

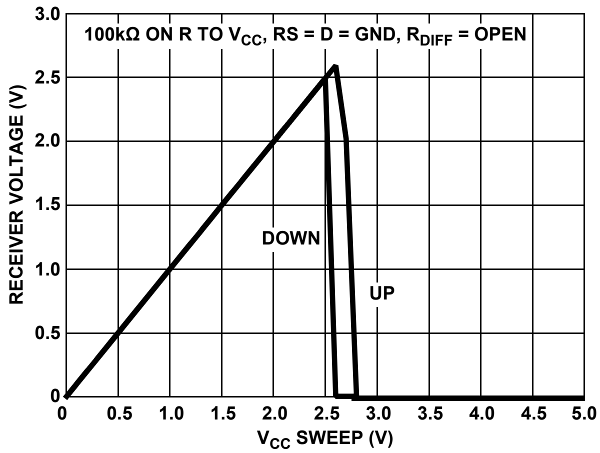


Figure 30. V_{CC} Undervoltage Lockout

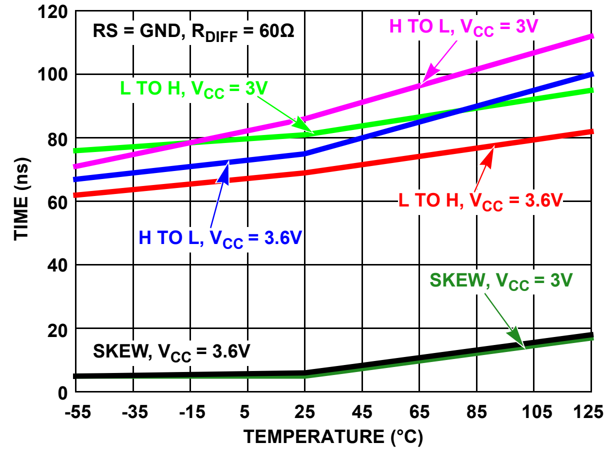


Figure 31. Transmitter Propagation Delay and Skew vs Temperature at Fast Speed

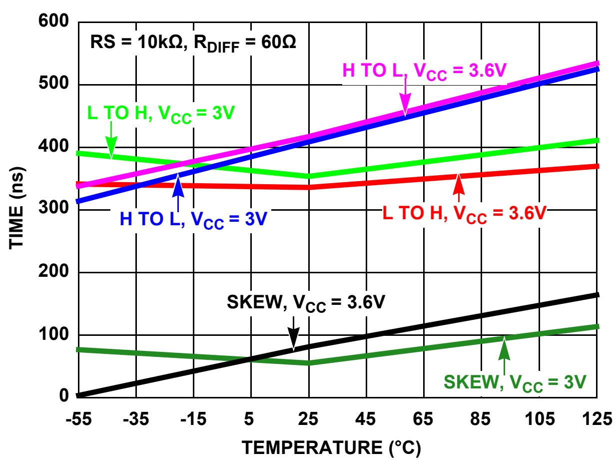


Figure 32. Transmitter Propagation Delay and Skew vs Temperature at Medium Speed

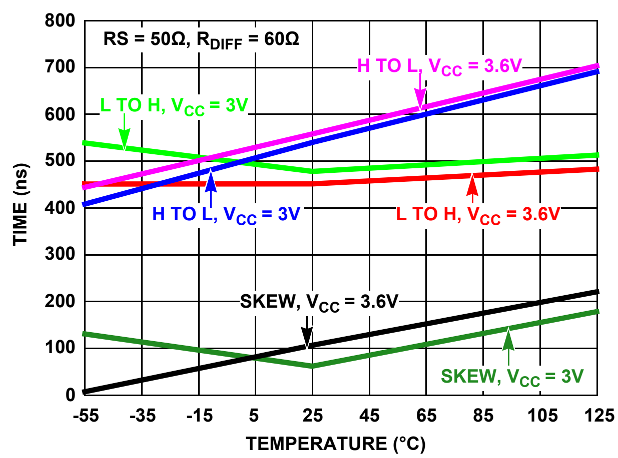


Figure 33. Transmitter Propagation Delay and Skew vs Temperature at Slow Speed

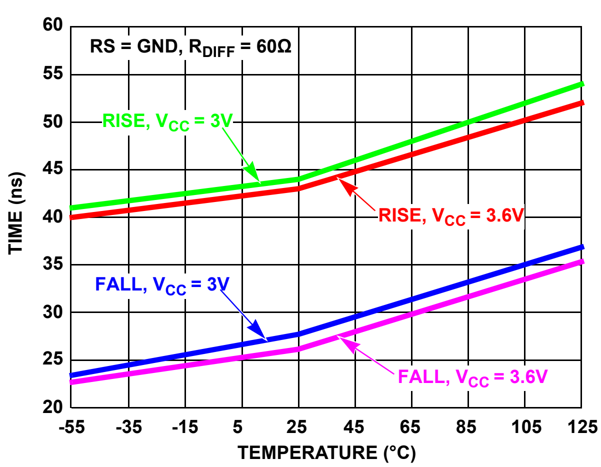


Figure 34. Transmitter Rise and Fall Times vs Temperature at Fast Speed

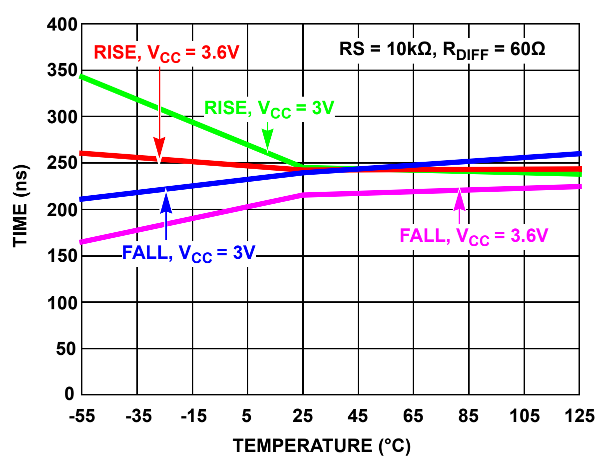


Figure 35. Transmitter Rise and Fall Times vs Temperature at Medium Speed

V_{CC} = 3.3V, C_L = 15pF, T_A = +25°C; unless otherwise specified. **(Continued)**

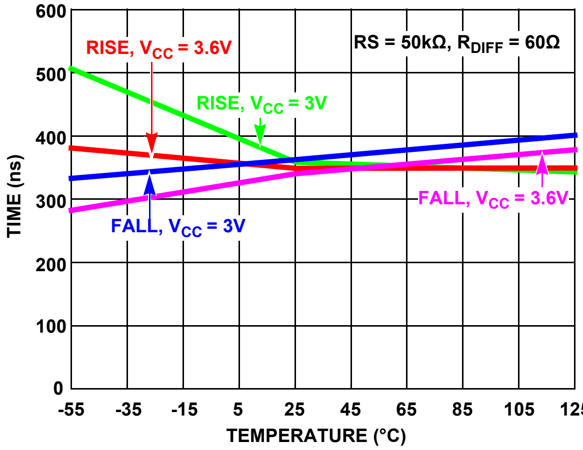


Figure 36. Transmitter Rise and Fall Times vs Temperature at Slow Speed

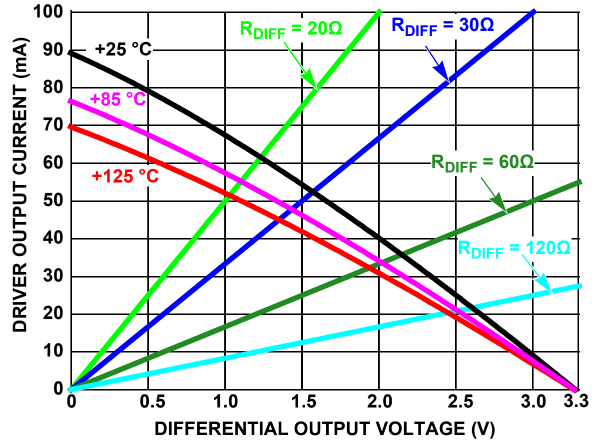


Figure 37. Driver Output Current vs Differential Output Voltage

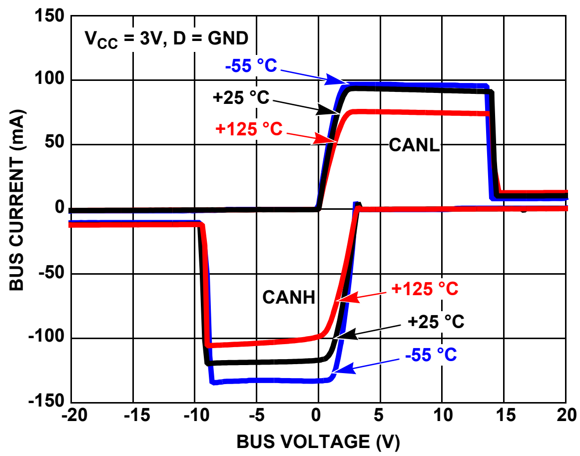


Figure 38. Driver Output Current vs Short-Circuit Voltage vs Temperature

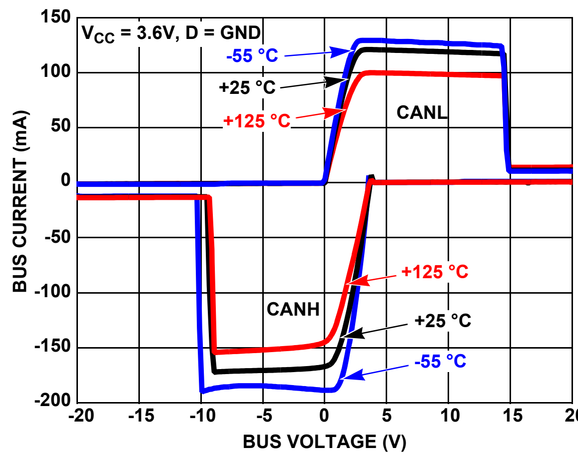


Figure 39. Driver Output Current vs Short-Circuit Voltage vs Temperature

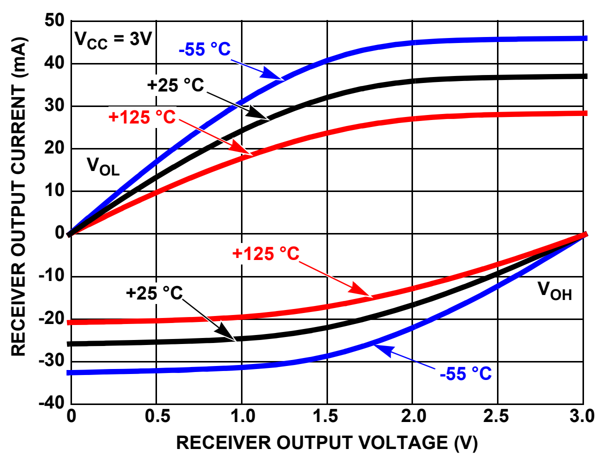


Figure 40. Receiver Output Current vs Receiver Output Voltage at V_{CC} = 3V

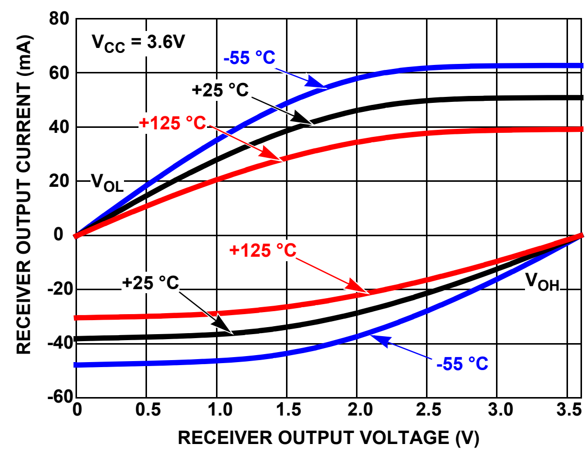


Figure 41. Receiver Output Current vs Receiver Output Voltage at V_{CC} = 3.6V

V_{CC} = 3.3V, C_L = 15pF, T_A = +25°C; unless otherwise specified. **(Continued)**

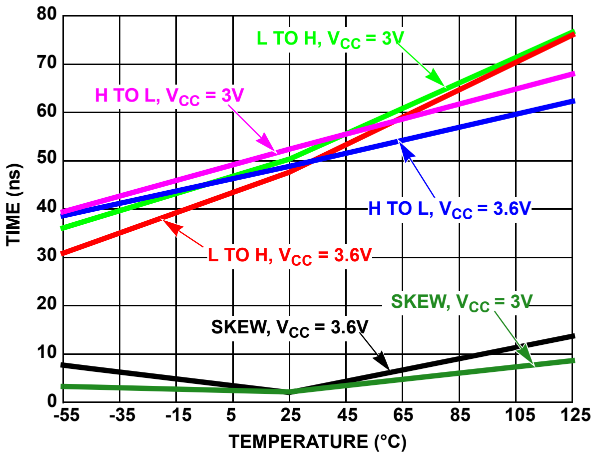


Figure 42. Receiver Propagation Delay and Skew vs Temperature

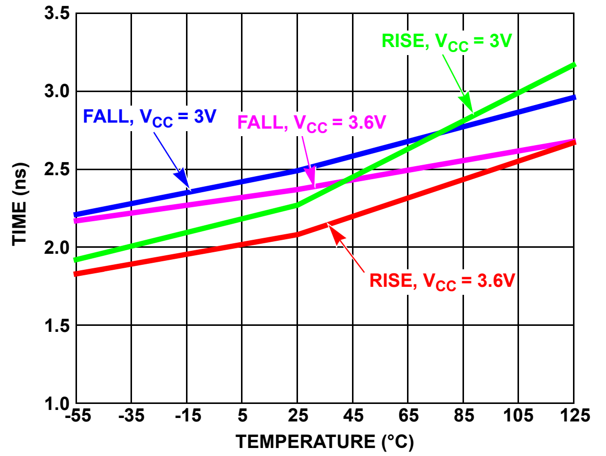


Figure 43. Receiver Rise and Fall Times vs Temperature

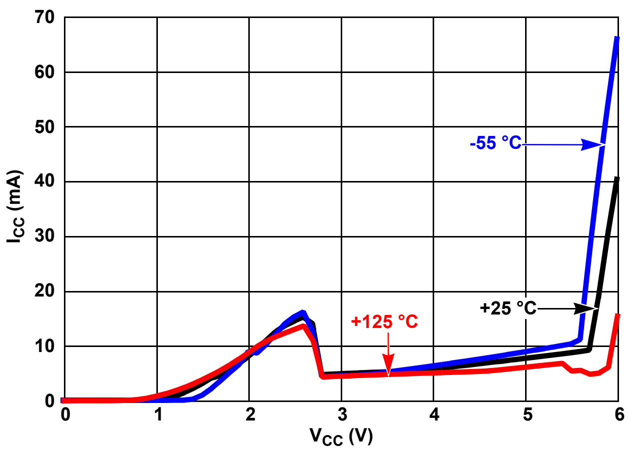


Figure 44. Supply Current vs Supply Voltage vs Temperature

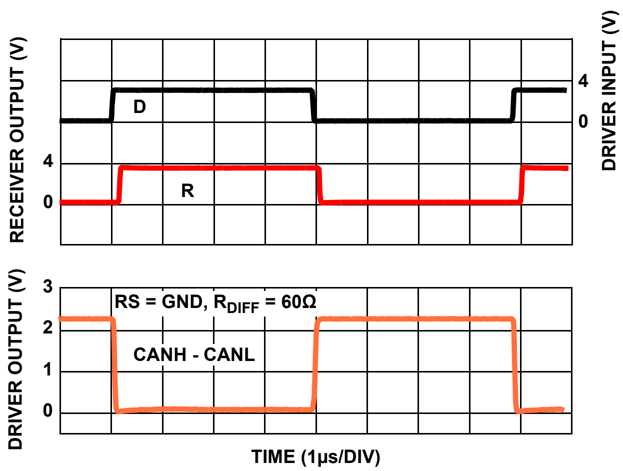


Figure 45. Fast Driver and Receiver Waveforms

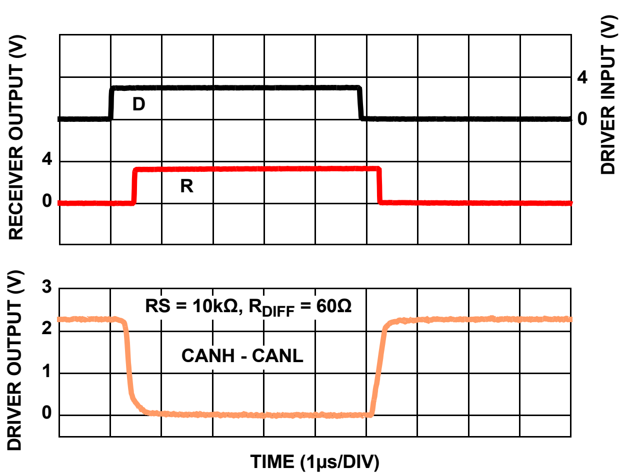


Figure 46. Medium Driver and Receiver Waveforms

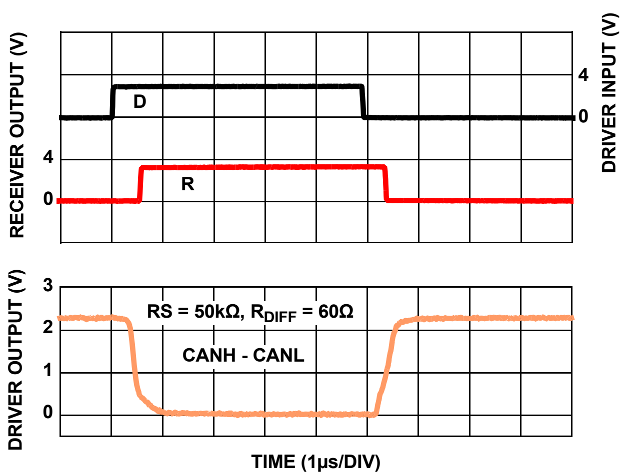


Figure 47. Slow Driver and Receiver Waveforms

4. Functional Description

4.1 Overview

The Intersil ISL72028ASEH is a 3.3V radiation tolerant CAN transceiver that is compatible with the ISO11898-2 standard for use in Controller Area Network (CAN) serial communication systems.

The device performs transmit and receive functions between the CAN controller and the CAN differential bus. It can transmit and receive at bus speeds up to 5Mbps. It is designed to operate over a common-mode range of -7V to +12V with a maximum of 120 nodes. The device is capable of withstanding ±20V on the CANH and CANL bus pins outside of ion beam and ±16V under ion beam.

4.2 Slope Adjustment

The transceiver driver has three programmable rise/fall time options programmed by the resistor value connected from the RS pin to GND. A 0Ω resistor sets the part in Fast Speed mode. A resistor of 10kΩ sets the part in Medium Speed mode. A resistor of 50kΩ puts the part in Slow Speed mode. Putting a high logic level on the RS pin places the part in Low Power Shutdown mode. Refer to "Low Power Shutdown Mode" on page 19 for more information.

4.2.1 Fast Speed Mode

Connecting the RS pin directly to GND (0Ω resistor) results in the fastest driver output switching times, limited only by the drive capability of the output state. In Fast Speed mode (RS = 0V), the rise/fall times, propagation delays, and total loop delays are optimized for a data rate of 1Mbps.

4.2.2 Medium Speed Mode

In Medium Speed mode (RS = 10kΩ), the rise/fall times, propagation delays, and total loop delays are optimized for a data rate of 500kbps. RS = 10kΩ provides for a typical slew rate of 12V/µs. The slower edges in Medium Speed mode at 500kbps provide better EMI results than running at 500kbps in Fast Speed mode.

4.2.3 Slow Speed Mode

In Slow Speed mode (RS = 50kΩ), the rise/fall times, propagation delays, and total loop delays are optimized for a data rate of 250kbps. RS = 50kΩ provides for a typical slew rate of 8V/µs. The slower edges in Slow Speed mode at 250kbps provide better EMI results than running at 250kbps in Medium Speed mode.

4.3 Cable Length

The device can operate according to the ISO11898 specification with a 40m cable and stub length of 0.3m and 60 nodes at 1Mbps. These specifications are greater than the ISO requirement of 30 nodes. The cable type specified is a twisted pair (shielded or unshielded) with a characteristic impedance of 120Ω. Resistors equal to this impedance must be terminated at both ends of the cable. Keep stubs as short as possible to prevent reflections.

4.4 Cold Spare

To reduce the risk of a single-point failure, use redundant bus transceivers in parallel. Space systems call for high reliability in data communications that are resistant to single-point failures. This is achieved by using a redundant bus transceiver in parallel. In this arrangement, both active and quiescent devices can be present simultaneously on the bus. The quiescent devices are powered down for cold spare and do not affect the communication of the other active nodes.

The powered down transceiver (V_{CC} <200mV) has a resistance between the VREF pin or the CANH pin or CANL pin to the V_{CC} supply rail of >480kΩ (maximum) with a typical resistance > 2MΩ. The resistance between CANH and CANL of a powered-down transceiver is typically 80kΩ. The receiver output (R pin) of a powered-down transceiver (V_{CC} <200mV) is internally connected to ground. Therefore, the receiver outputs of an active transceiver and a cold spare transceiver cannot be connected together in the redundant application.

4.5 Low Power Shutdown Mode

When a high level is applied to the RS pin, the device enters Low Power Shutdown mode, in which the driver and receiver are switched off to conserve power. The bus pins are at Hi-Z and the R pin will be at logic high. In Low Power Shutdown mode, the transceiver draws 50µA (maximum) of current.

A low level on the RS pin brings the device back to operation.

4.6 Using 3.3V Devices in 5V Systems

Looking at the differential voltage of both the 3.3V and 5V devices, the differential voltage is the same, and the recessive common-mode output is the same. The dominant common-mode output voltage is slightly lower than that of the 5V counterparts. The receiver specifications are also the same. Although the electrical parameters appear compatible, perform necessary system testing to verify interchangeable operation.

4.7 Split Mode Termination

The VREF pin provides a $V_{CC}/2$ output voltage for Split mode termination. The VREF pin has the same ESD protection, short-circuit protection, and common-mode operating range as the bus pins.

The Split mode termination technique is shown in Figure 48. .

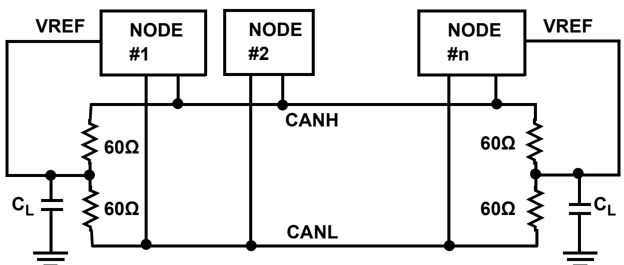


Figure 48. Split Termination

Split mode termination stabilizes the bus voltage at $V_{CC}/2$ and prevents it from drifting to a high common-mode voltage during periods of inactivity. The technique improves the electromagnetic compatibility of a network. The Split mode termination is put at each end of the bus.

The C_L capacitor between the two 60Ω resistors filters unwanted high frequency noise to ground. The resistors should have a tolerance of 1% or better and the two resistors should be carefully matched to provide the most effective EMI immunity. A typical value of C_L for a high speed CAN network is 4.7nF, which generates a 3dB point at 1.1Mbps. The capacitance value used is dependent on the signaling rate of the network.

5. Die Characteristics

Table 4. Die and Assembly Related Information

Die Information	
Dimensions	2413µm x 3322µm (95 mils x 130.79 mils) Thickness: 305µm ±25µm (12 mils ±1 mil)
Interface Materials	
Glassivation	Type: 12kÅ Silicon Nitride on 3kÅ Oxide
Top Metallization	Type: 300Å TiN on 2.8µm AlCu In Bondpads, TiN has been removed.
Backside Finish	Silicon
Process	P6SOI
Assembly Information	
Substrate Potential	Floating
Additional Information	
Worst Case Current Density	$1.6 \times 10^5 A/cm^2$
Transistor Count	4055
Weight of Packaged Device	0.31 grams
Lid Characteristics	Finish: Gold Potential: Grounded, tied to package pin 2

5.1 Metalization Mask Layout

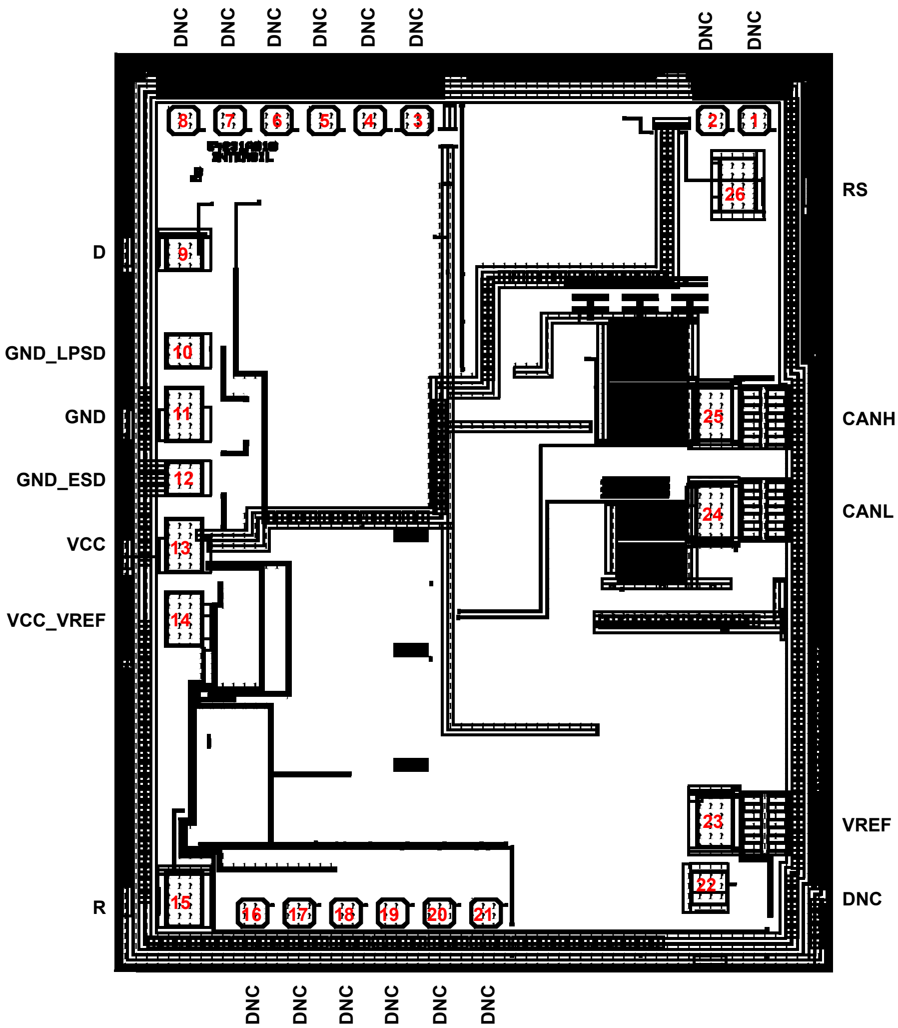


Table 5. ISL72028ASEH Die Layout X-Y Coordinates

Pad Number	Pad Name	X (µm)	Y (µm)	X	Y
1	DNC	90.0	90.0	901.4	1365.6
2	DNC	90.0	90.0	767.4	1365.6
3	DNC	90.0	90.0	-183.23	1365.6
4	DNC	90.0	90.0	-333.25	1365.6
5	DNC	90.0	90.0	-483.25	1365.6
6	DNC	90.0	90.0	-633.25	1365.6
7	DNC	90.0	90.0	-783.25	1365.6
8	DNC	90.0	90.0	-933.25	1365.6
9	D	110.0	110.0	-931.1	901.85
10	GND_LSPD	110.0	110.0	-931.1	563.25
11	GND	110.0	180.0	-931.1	342.25
12	GND_ESD	110.0	110.05	-931.1	119.42
13	VCC	110.0	180.0	-931.1	-115.05
14	VCC_VREF	110.0	180.05	-931.1	-371.08
15	R	110.0	180.0	-931.1	-1350.0
16	DNC	90.0	90.0	-711.1	-1394.95
17	DNC	90.0	90.0	-561.1	-1394.95
18	DNC	90.0	90.0	-411.1	-1394.95
19	DNC	90.0	90.0	-261.1	-1394.95
20	DNC	90.0	90.0	-111.1	-1394.95
21	DNC	90.0	90.0	38.9	-1394.95
22	DNC	110.0	110.0	756.9	-1307.3
23	VREF	110.0	180.0	775.3	-1072.3
24	CANL	110.0	180.0	772.1	2.15
25	CANH	110.0	180.05	772.1	343.33
26	RS	110.0	180.0	848.1	1140.6

Note: Origin of coordinates is the center of the die. DNC - Do No Connect

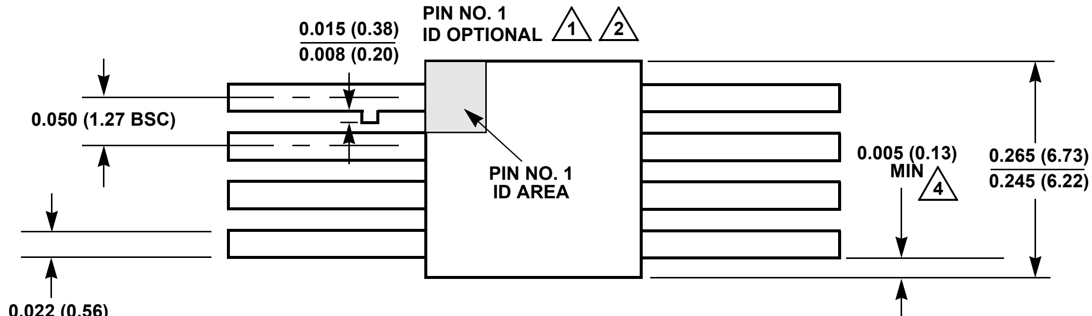
6. Revision History

Rev.	Date	Description
1.00	Jul 27, 2017	In Pin Description table on page 4, Pins 6 and 7 - swapped pin name and description to match Pin Configuration. Electrical Spec table on page 9: Output Rise Time tr2 - changed: “(medium speed - 5000kbps)” to: “(medium speed - 500kbps)”. Changed the limit for Propagation Delay High to Low, tPDHL2, from: 650ns, to: 600ns. Changed the limit for Total Loop Delay, Driver Input to Receiver Output, Dominant to Recessive, t(LOOP2) for RS = 10kΩ from: 750ns, to: 700ns.
0.00	Apr 14, 2017	Initial release

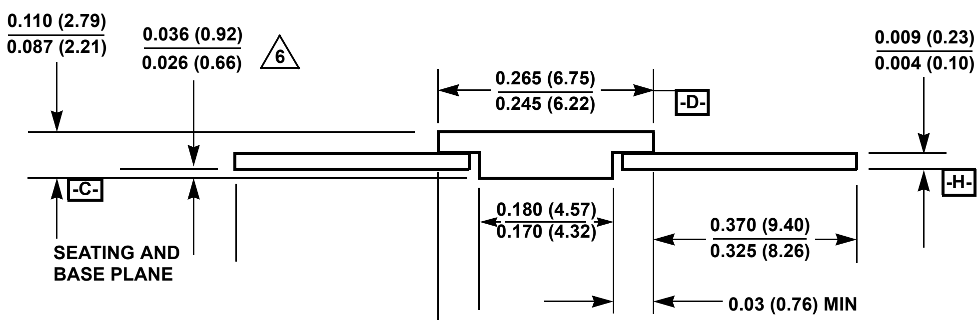
7. Package Outline Drawing

For the most recent package outline drawing, see [K8.A](K8.A).

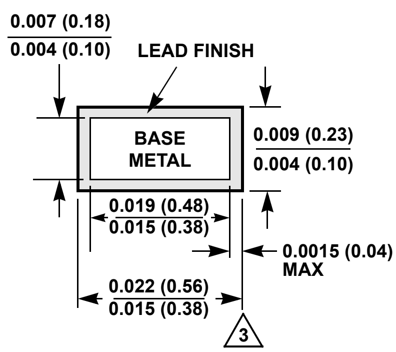
K8.A
8 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE
Rev 4, 12/14



TOP VIEW



SIDE VIEW



SECTION A-A

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab may be used to identify pin one.
2. If a pin one identification mark is used in addition to or instead of a tab, the limits of the tab dimension do not apply.
3. The maximum limits of lead dimensions (section A-A) shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
4. Measure dimension at all four corners.
5. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
6. Dimension shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
7. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
8. Controlling dimension: INCH.

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