ISL73007M

Radiation Tolerant 18V, 3A Point-of-Load Regulator

The ISL73007M is a radiation tolerant Point-of-Load (POL) buck regulator that provides up to 3A of output current capability with an input voltage ranging from 3V to 18V. The device uses constant frequency peak current mode control architecture for fast loop transient response. The device uses internal compensation or an external Type-II compensation to optimize performance and stabilize the loop. The ISL73007M has an internally configured switching frequency of 500kHz. The ISL73007M switching frequency can be adjusted from 300kHz to 1MHz using an external resistor.

The ISL73007M integrates high-side (P-channel) and low-side (N-channel) power FETs. There are options for external or internal compensation, switching frequency, and slope control that can be implemented with a minimum of external components reducing the BOM count and design complexity.

The ISL73007M includes a comprehensive suite of operational features and protections, including preset undervoltage, overvoltage, overcurrent protections, power-good, soft-start, and over-temperature.

The ISL73007M operates across the temperature range of -55°C to +125°C and is available in a 28-lead plastic exposed pad heatsink thin shrink small outline package (HTSSOP).

Features

- Qualified to Renesas Rad Tolerant Screening and QCI Flow (R34TB0004EU)
- Input Bias Voltage
  - 3V to 18V
- Internal or external loop compensation
- 1% reference voltage over-temperature and radiation
- Switching frequency dependent soft-start
- Positive and negative overcurrent, over/undervoltage, and over-temperature protections
- High 500kHz efficiency ≥90% from 1A to 3A
- 300kHz to 1MHz adjustable switching frequency
- Adjustable slope compensation
- TID Radiation Lot Acceptance Testing (RLAT) (LDR: 0.01rad(Si)/s)
  - ISL73007M30VEZ: 30krad(Si)
  - ISL73007M50VEZ: 50krad(Si)
- SEE Characterization
  - No DSEE for V_{IN} = 18V and V_{CC} = 6.2V at 46MeV•cm^2/mg
  - SEFI <2.5μm^2 at 46MeV•cm^2/mg
  - SET <2.0% on V_{OUT} at 46MeV•cm^2/mg

Applications

- Low Power Auxiliary Rails for FPGAs, DSPs, CPUs, and ASICs

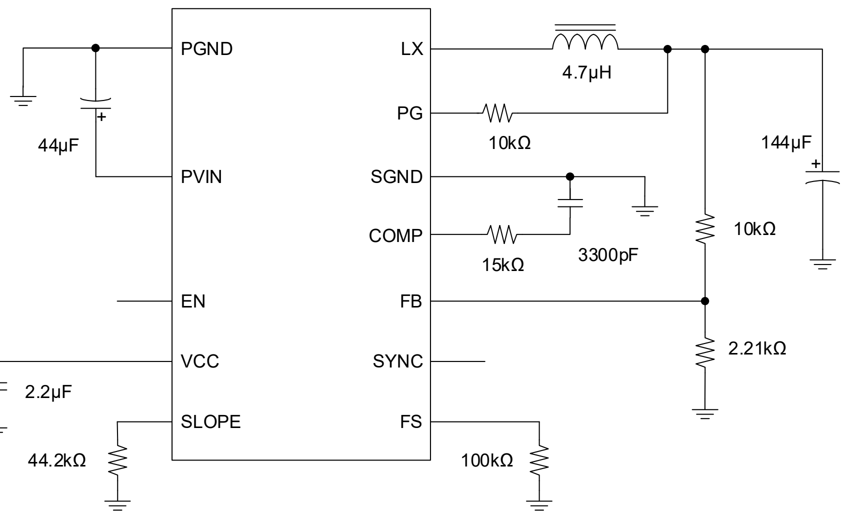


Figure 1. External Compensation Application Diagram for 12V to 3.3V, 500kHz

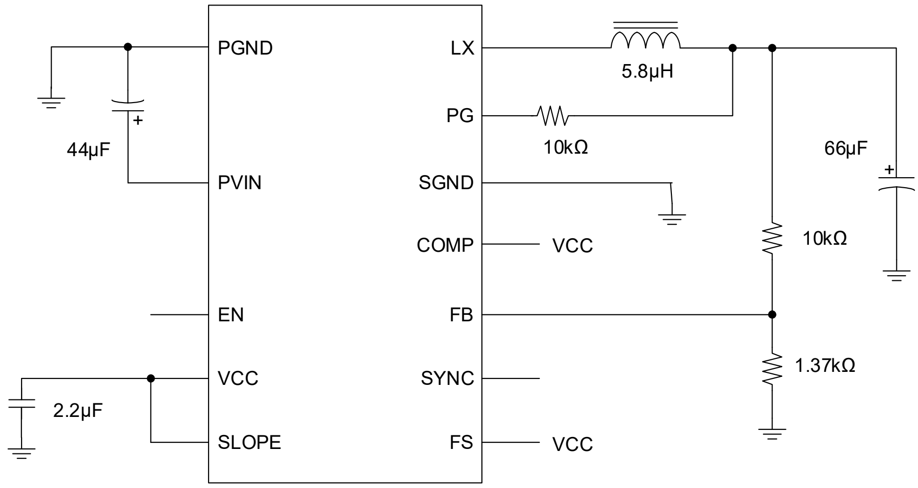


Figure 2. Internal Compensation Application Diagram for 12V to 5V, 500kHz

Contents

1. Overview

1.1 Block Diagram

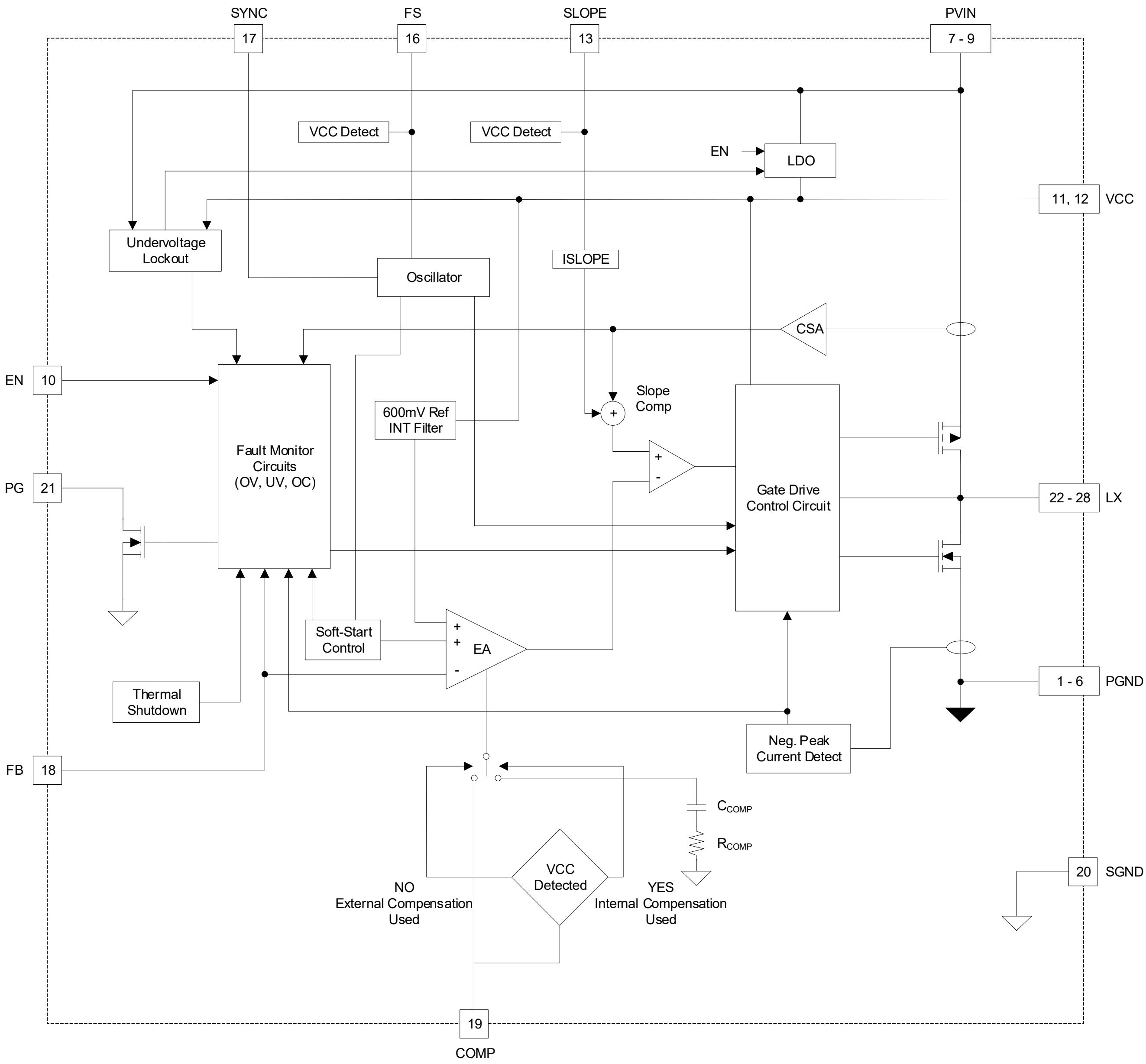


Figure 3. Block Diagram

2. Pin Information

2.1 Pin Assignments

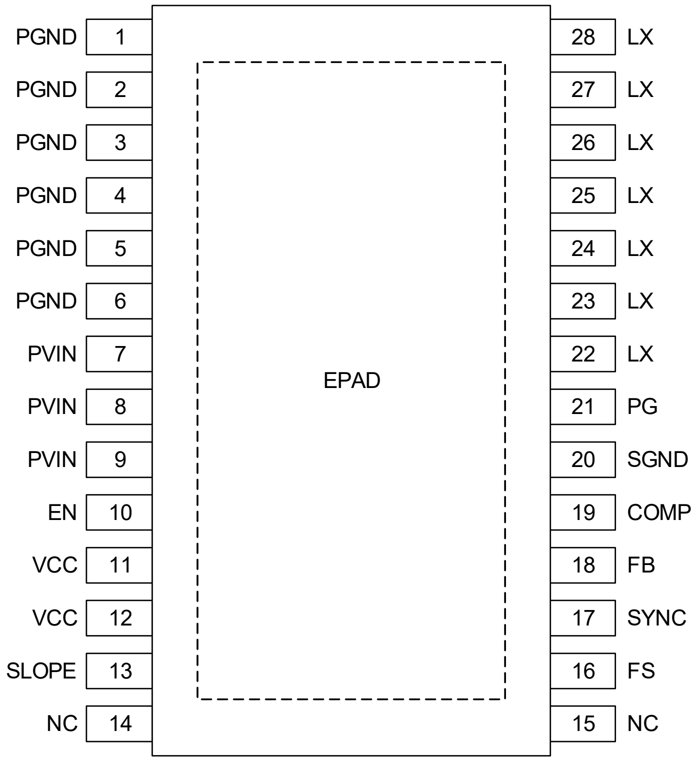


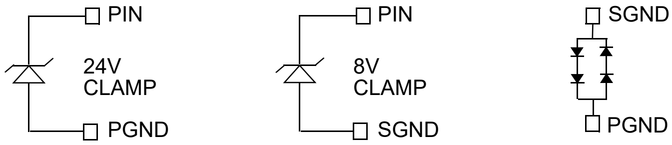
Figure 4. Pin Assignments - Top View

2.2 Pin Descriptions

Pin Number	Pin Name	ESD Circuit	Description
1, 2, 3, 4, 5, 6	PGND	3	Power-ground connection. Ground return for the low-side power MOSFET
7, 8, 9	PVIN	1	Power Input. Supplies the power switches of the buck converter.
10	EN	2	Enable input. This input is a comparator-type input with a rising threshold of 1.2V. Bypass this pin to the PCB ground plane with a 10nF ceramic capacitor to mitigate SEE. Tie this pin to a maximum of 5V.
11, 12	VCC	2	Linear regulator output from PVIN to provide an internal bias supply rail of up to 5V. Bypass this pin to the PCB ground plane with a 2.2µF ceramic or low ESR Tantalum capacitor for stability, SEE, and noise mitigation. VCC is not intended to bias external circuits
13	SLOPE	2	Slope Compensation. Connect a resistor from this pin to GND to externally set the slope compensation. This pin is a current source of 12µA into the external resistor. Connect the SLOPE pin to VCC to use the default internal slope compensation voltage of 1.2V. If not connected to VCC, add a 1nF capacitor from this pin to ground for SEE mitigation.
16	FS	2	Frequency select pin. Tie to VCC for 500kHz operation. Connect a resistor to ground to program the frequency from 300kHz to 1MHz. See Equation 2 for the frequency setting formula.
17	SYNC	2	External synchronizing frequency input pin. Input a clock signal to align device switching frequency and phase. This pin has an internal pull-down; leave it floating if the SYNC function is unnecessary.
18	FB	2	Error Amplifier inverting input. Connect a resistor divider from VOUT to GND with the midpoint driving the FB pin.
19	COMP	2	Error Amplifier output. The external compensation network is connected from this pin to GND. Tie this pin to VCC to use the internal Error Amplifier compensation setup.

Pin Number	Pin Name	ESD Circuit	Description
20	SGND	3	Signal ground. The ground is associated with the internal control circuitry. Connect this pin directly to the PCB ground plane at a single point.
21	PG	1	Power-good output. The pin is an open-drain logic output pulled to SGND when the output is outside of the PGOOD range. The pin can be pulled to any voltage up to the PVIN abs maximum limit. Renesas recommends using a nominal 1kΩ to 10kΩ pull-up resistor. Bypass this pin to the PCB ground plane with a 100pF capacitor for SEE mitigation.
22, 23, 24, 25, 26, 27, 28	LX	N.A.	Switch node connection. Connect this pin to the output filter inductor. Internally, this pin is connected to the common node of the synchronous MOSFET power switches.
14,15	NC	N.A.	Not Connected. These pins are unused and open and can be tied to GND plane.
-	EPAD	N.A.	EPAD is electrically isolated from any pin. Connect to PCB GND. Refer to Layout Considerations for more information.

ESD Circuits



Circuit 1 Circuit 2 Circuit 3

3. Specifications

3.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
PVIN, LX	PGND - 0.3	+20	V
PVIN[1]	PGND - 0.3	PGND + 16.5	V
SGND	PGND - 0.1	PGND + 0.1	V
FB, COMP, SLOPE, FS, SYNC	PGND - 0.3	VCC + 0.3	V
EN	PGND - 0.3	5.3	V
PG	PGND - 0.3	PVIN	V
VCC	PGND - 0.3	6.5	V
VCC[1]	PGND - 0.3	5.8	V
Peak Output Current	-	Overcurrent Protected	A
LX RMS Output Current	-	3.4	A
Maximum Junction Temperature	-55	+150	°C
Maximum Storage Temperature Range	-65	+150	°C
Human Body Model (Tested per MIL-PRF-883 3015.7)	-	2.5	kV
Charged Device Model (Tested per JS-002-2022)	-	1	kV
Latch-Up (Tested per JESD78E; Class 2, Level A)	-	±100	mA

1. LET = 43MeV•cm^2/mg at 125°C (T_C)

3.2 Thermal Information

Parameter	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance	28 Ld HTSSOP Package	θ_{JA}[1]	Junction to ambient	25	°C/W
		θ_{JC}[2]	Junction to case	0.7	°C/W

1. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.
2. For θ_{JC}, the case temperature location is the center of the metallization on the package underside.

3.3 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Input Voltage (PVIN)	PGND + 3.0	+18	V
Output Current	0	3	A
Switching Frequency	300	1000	kHz
External R_{SLOPE} Resistor	25	100	kΩ
Ambient Temperature	-55	+125	°C
Output Voltage	0.6	Limited by min on/off timing constraints & f_{SW}	V

3.4 Electrical Specifications

Unless otherwise noted, PVIN = 3V and 18V; PGND = SGND = 0V; LX = Open Circuit; PGOOD is pulled up to PVIN with a 10k resistor; I_{OUT} = 0A; T_J = T_A, $r_{DS(ON)}$ is pulse tested. **Boldface limits apply across the operating temperature range, -55°C to +125°C by characterization with production testing at +25°C; over a total ionizing dose of 30krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL73007M30VEZ); or over a total ionizing dose of 50krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL73007M50VEZ).**

Parameter	Symbol	Test Conditions	Temp. (°C)	Min	Typ[1]	Max	Unit
Input Power Supply							
Rising Undervoltage Lockout	V_{PVIN_UVLO}	EN = 2.25V	-55 to +125°C	-	2.86	**2.95**	V
Falling Undervoltage Lockout		EN = 2.25V	-55 to +125°C	**2.7**	2.78	-	V
Operating Supply Current[2]	I_{PVIN_OPER}	PVIN = 18V, EN = 5V, ext. 500kHz, no load	-55	15	30	38	mA
			+25	28	35	45	mA
			+125	35	50	65	mA
			+25C (Post Rad)	28	35.2	45	mA
Stand-by Supply Current	I_{PVIN_SB}	PVIN = 3V, EN = 1V	-55 to +125°C	**1.1**	1.37	**1.7**	mA
		PVIN =18V, EN = 1V	-55 to +125°C	**1.1**	1.29	**1.4**	mA
Shutdown Supply Current	I_{PVIN_SD}	PVIN = 3V, EN = 0V	-55 to +125°C	**5**	25	**40**	µA
		PVIN = 18V, EN = 0V	-55 to +125°C	**50**	128	**190**	µA
Output Regulation							
Feedback Voltage Accuracy[2]	V_{FB}	VFB (including Error Amplifier V_{IO} to SGND)	-55	592	598	602	mV
			+25	594	600	603	mV
			+125	594	600	603	mV
			+25 (Post Rad)	594	601	603.5	mV
FB Leakage Current[2]	I_{FB}	PVIN = 12V, V_{FB} = 0.6V	-55	-20	0.492	20	nA
			+25	-20	0.49	20	nA
			+125	-20	1.767	20	nA
			+25 (Post Rad)	-20	0.49	20	nA
Output Voltage Tolerance Over Input Voltage Range	LNREG	PVIN = 3V, 18V using servo loop	-55 to +125°C	**-0.11**	0.039	**0.25**	%
Protection Features							
Positive Peak Current Limit[3]	$I_{IPLIMIT1}$	PVIN = 3V	-55 to +125°C	**3.8**	5.3	**6.76**	A
		PVIN ≥ 5V	-55 to +125°C	**3.8**	5	**6.5**	A
	$I_{IPLIMIT2}$	PVIN = 18	-55 to +125°C	**5**	6.2	**7.95**	A

Unless otherwise noted, PVIN = 3V and 18V; PGND = SGND = 0V; LX = Open Circuit; PGOOD is pulled up to PVIN with a 10k resistor; I_{OUT} = 0A; T_J = T_A, $r_{DS(ON)}$ is pulse tested. **Boldface limits apply across the operating temperature range, -55°C to +125°C by characterization with production testing at +25°C; over a total ionizing dose of 30krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL73007M30VEZ); or over a total ionizing dose of 50krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL73007M50VEZ). (Cont.)**

Parameter	Symbol	Test Conditions	Temp. (°C)	Min	Typ[1]	Max	Unit
Negative Peak Current Limit[2][3]	$-I_{IPLIMIT}$	PVIN = 3V	-55 to +125°C	**-5.7**	-4.4	**-3.7**	A
		PVIN = 12V	-55 to +125°C	**-5.7**	-4.6	**-3.7**	A
		PVIN = 18V	-55 to +125°C	**-5.8**	-4.6	**-3.6**	A
Thermal Shutdown[4]	$Therm_{SD}$	Die Rising Temperature Threshold	-	-	161	-	°C
Thermal Reset[4]	$Therm_{SD}$	Die Falling Temperature Threshold	-	-	148	-	°C
Thermal Shutdown Hysteresis[4]	$Therm_{SDHYS}$	-	-	-	-	20	°C
Compensation							
Internal Error Amplifier Proportional Voltage Gain[4]	A_{EAP}	-	+25	-	12.7	-	V/V
Internal Error Amplifier Zero [4]	EA_{fz}	-	+25	-	5.8	-	kHz
Internal Error Amplifier Gain-Bandwidth Product[4]	EA_{GBP1}	-	+25	-	33	-	MHz
Internal Error Amplifier DC Gain[2][4]	EA_{AV1}	1Hz	+25	55.3	82	-	dB
			+125	58.5	82	-	dB
External Error Amplifier Transconductance[2]	$EA_{transcon2}$	PVIN = 5V, delta COMP current/delta FB Voltage (10mV)	-55	0.93	1.057	1.18	mA/V
			+25	0.82	0.923	1.02	mA/V
			+125	0.68	0.768	0.87	mA/V
			+25C (Post Rad)	0.82	0.926	1.02	mA/V
External Error Amplifier DC Gain[4]	EA_{AV2}	1Hz	+25	66	80	-	dB
External Error Amplifier Gain-Bandwidth Product[4]	EA_{GBP2}	-	+25	15	-	-	MHz
Modulator Tranconductance [4]	G_M	-	-55 to +125°C	-	12	-	A/V
Oscillator/Slope Generator							
Default Switching Frequency	f_{SWd}	FS = VCC	-55 to +125°C	**450**	500	**550**	kHz
300kHz Switching Frequency	f_{SW3}	FS = 174kΩ to GND, V_{SLOPE} = 1.2V	-55 to +125°C	**270**	305	**330**	kHz
500kHz Switching Frequency	f_{SW5}	FS = 100kΩ to GND, V_{SLOPE} = 1.2V	-55 to +125°C	**450**	500	**550**	kHz
1000kHz Switching Frequency	f_{SW10}	FS = 42.7kΩ to GND, V_{SLOPE} = 1.2V	-55 to +125°C	**900**	1000	**1100**	kHz
SLOPE Pin Current Source	I_{SLOPE}	-	-55 to +125°C	**10.5**	12	**13.5**	µA
Internal SLOPE Ramp Rate	t_{SLOPE}	(V_{COMP} at 80%DC - V_{COMP} at 20%DC)/ (t_{MIN_ON}at80%DC - t_{MIN_ON} at 20%DC)	-55 to +125°C	**0.1**	0.13	**0.17**	V/µs

Unless otherwise noted, PVIN = 3V and 18V; PGND = SGND = 0V; LX = Open Circuit; PGOOD is pulled up to PVIN with a 10k resistor; I_{OUT} = 0A; T_J = T_A, $r_{DS(ON)}$ is pulse tested. **Boldface limits apply across the operating temperature range, -55°C to +125°C by characterization with production testing at +25°C; over a total ionizing dose of 30krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL73007M30VEZ); or over a total ionizing dose of 50krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL73007M50VEZ). (Cont.)**

Parameter	Symbol	Test Conditions	Temp. (°C)	Min	Typ[1]	Max	Unit
SYNC							
SYNC Input Voltage High Threshold	V_{SYNCH}	PVIN = 3V	-55 to +125°C	**1.5**	-	**2.2**	V
		PVIN = 18V	-55 to +125°C	**2.7**	-	**3.5**	V
SYNC Input Voltage Low Threshold	V_{SYNCL}	PVIN = 3V	-55 to +125°C	**1.1**	-	**1.5**	V
		PVIN = 18V	-55 to +125°C	**1.7**	-	**2.5**	V
SYNC Input Voltage Range	-	Assured by SYNC VIH, PVIN = 3V	-55 to +125°C	**2.2**	-	**-**	V
		Assured by SYNC VIH, PVIN = 18V	-55 to +125°C	**3.5**	-	**-**	V
		Assured by SYNC VIL, PVIN = 3V	-55 to +125°C	-	-	**1.1**	V
		Assured by SYNC VIL, PVIN = 18V	-55 to +125°C	-	-	**1.7**	V
Input Current	$I_{SYNC-IN}$	V_{SYNC} = 5V	-55 to +125°C	**2.5**	5	**7.0**	µA
SYNC Frequency (Above Internal Oscillator)	f_{SYNC}	R_{FS} = 174kΩ	-55 to +125°C	**15**	-	-	%
		R_{FS} = 100kΩ	-55 to +125°C	**15**	-	-	%
		R_{FS} = 42.7kΩ	-55 to +125°C	**15**	-	-	%
Pull-Down Resistance	$R_{SYNC-PULLDN}$	V_{SYNC} = 5V	-55 to +125°C	**0.8**	1	**1.1**	MΩ
SYNC Input On to PWM Delay	$t_{SYNC-I-DEL}$	-	-55 to +125°C	-	2	-	cycle
SYNC Input Off to PWM Delay	$t_{SYNC-O-DEL}$	-	-55 to +125°C	-	1	-	cycle
Enable							
Rising Enable Voltage Threshold	EN_{VIH}	Enable Rising to LX Switching	-55 to +125°C	**1.18**	1.21	**1.3**	V
Falling Enable Voltage Threshold	EN_{VIL}	Enable Falling to LX Stops Switching	-55 to +125°C	**0.96**	1	**1.06**	V
Enable Voltage LX Hysteresis	EN_{VIHhys}	-	-55 to +125°C	**20**	200	**410**	mV
Standby Enable Voltage	SB_EN_{VIH}	Enable Rising to VCC Enabled	-55 to +125°C	**0.45**	0.76	**1**	V
Shutdown Enable Voltage	SB_EN_{VIL}	Enable Falling to VCC Disabled	-55 to +125°C	**0.3**	0.68	**0.9**	V
Enable Hysteresis Voltage	EN_{HYS}	Enable Rising to VCC Enabled - EN Falling to VCC Disable	-55 to +125°C	**20**	80	**175**	mV
Low Enable Current	EN_{IIL}	Enable = 0V	-55 to +125°C	**-20**	0.426	**20**	nA
High Enable Current	EN_{IIH}	Enable = 5V	-55 to +125°C	**1.5**	2.166	**2.8**	µA

Unless otherwise noted, PVIN = 3V and 18V; PGND = SGND = 0V; LX = Open Circuit; PGOOD is pulled up to PVIN with a 10k resistor; I_{OUT} = 0A; T_J = T_A, $r_{DS(ON)}$ is pulse tested. **Boldface limits apply across the operating temperature range, -55°C to +125°C by characterization with production testing at +25°C; over a total ionizing dose of 30krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL73007M30VEZ); or over a total ionizing dose of 50krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL73007M50VEZ). (Cont.)**

Parameter	Symbol	Test Conditions	Temp. (°C)	Min	Typ[1]	Max	Unit
Enable (EN) Pull-Down Resistance	R_{EN}	PVIN = 12V	-55 to +125°C	**1.7**	2.3	**2.9**	MΩ
VCC							
VCC Output Voltage	$VOUT_{3V,0mA}$	PVIN = 3V, I_{OUT} = 0mA, f_{SW} = 500kHz	-55 to +125°C	**2.96**	2.99	**3**	V
	$VOUT_{3V,10mA}$	PVIN = 3V, I_{OUT} = 10mA, f_{SW} = 500kHz	-55 to +125°C	**2.93**	2.97	**2.98**	V
	$VOUT_{5.5V,0mA}$	PVIN = 5.5V, I_{OUT} = 0mA, f_{SW} = 500kHz	-55 to +125°C	**4.83**	4.95	**5**	V
	$VOUT_{5.5V,10mA}$	PVIN = 5.5V, I_{OUT} = 10mA, f_{SW} = 500kHz	-55 to +125°C	**4.82**	4.94	**5**	V
VCC Foldback Current	I_{CC_SC}	PVIN = 18V, V_{CC} = 0V, EN = 1.6V	-55 to +125°C	**40**	72	**90**	mA
VCC Overcurrent Limit	I_{CC_CL}	PVIN = 18V, V_{CC} = 4.3V, EN = 1.6V	-55 to +125°C	**75**	98	**130**	mA
Power-Good							
Output Overvoltage Error Threshold	OVPG	PVIN = 5V, FB as a % of V_{REF}	-55 to +125°C	**105.5**	106.8	**107.5**	%
Output Undervoltage Error Threshold	UVPG	PVIN = 5V, FB as a % of V_{REF}	-55 to +125°C	**92.25**	93.2	**94.25**	%
Output Overvoltage Fault	OVflt	PVIN = 5V, FB as a % of V_{REF}	-55 to +125°C	**114**	115	**118**	%
Output Undervoltage Fault	UVflt	PVIN = 5V, FB as a % of V_{REF}	-55 to +125°C	**82.5**	85	**88**	%
Low Current Drive	PG_I_{OL}	PVIN = 3V, PG = 0.4V, EN = 0V	-55 to +125°C	**11**	22	**35**	mA
Low V_{OUT}	PG_V_{OL}	PVIN = 18V, FB = 0V, EN = 0V, IPG = 10mA	-55 to +125°C	**-**	0.15	**0.27**	V
Leakage	I_{LKGPG}	PVIN = PG = 18V	-55 to +125°C	**-**	-	**1**	µA
Power Good Rising Delay	$t_{SSPGdlyr}$	PVIN = 5.5V From EN edge to PG high, 300kHz	-55 to +125°C	**8**	12.5	**16.5**	ms
		PVIN = 5.5V From EN edge to PG high, 500kHz	-55 to +125°C	**6.6**	7.4	**8.4**	ms
		PVIN = 5.5V From EN high to PG high, 1000kHz	-55 to +125°C	**3.7**	4	**4.5**	ms
Rising Edge Delay	t_{PGdlyr}	Return to regulation to PG response	-55 to +125°C	**1.9**	3	**4.2**	µs
Falling Edge Delay	t_{PGdlyf}	Out of regulation to PG response	-55 to +125°C	**3.4**	4.3	**5.5**	µs
Phase							
Minimum LX On-Time[5]	t_{MIN_ON}	PVIN = 12V, Forced Min On-Time by COMP bias, No Load	-55 to +125°C	**-**	230	**260**	ns
Minimum LX Off-Time[5]	t_{MIN_OFF}	PVIN = 12V, Forced Min Off-Time by COMP bias, No Load	-55 to +125°C	**-**	171	**210**	ns

Unless otherwise noted, PVIN = 3V and 18V; PGND = SGND = 0V; LX = Open Circuit; PGOOD is pulled up to PVIN with a 10k resistor; I_{OUT} = 0A; $T_J = T_A$, $r_{DS(ON)}$ is pulse tested. **Boldface limits apply across the operating temperature range, -55°C to +125°C by characterization with production testing at +25°C; over a total ionizing dose of 30krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL73007M30VEZ); or over a total ionizing dose of 50krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL73007M50VEZ). (Cont.)**

Parameter	Symbol	Test Conditions	Temp. (°C)	Min	Typ[1]	Max	Unit
HTSSOP Upper FET $r_{DS(ON)}$[2][3]	-55UPR$_{DSON_3}$	PVIN = 3.0V, I_{OUT} = 200mA	-55	55	66.56	80	mΩ
	-55UPR$_{DSON_5}$	PVIN = 5.5V, I_{OUT} = 200mA	-55	45	55.64	65	mΩ
	25UPR$_{DSON_3}$	PVIN = 3.0V, I_{OUT} = 200mA	+25	65	81.43	100	mΩ
	25UPR$_{DSON_5}$	PVIN = 5.5V, I_{OUT} = 200mA	+25	50	66.95	85	mΩ
	125UPR$_{DSON_3}$	PVIN = 3.0V, I_{OUT} = 200mA	+125	85	104.89	125	mΩ
	125UPR$_{DSON_5}$	PVIN = 5.5V, I_{OUT} = 200mA	+125	65	85.75	100	mΩ
	25UPR$_{DSON_3}$	PVIN = 3.0V, I_{OUT} = 200mA	+25 (Post Rad)	65	87.15	120	mΩ
	25UPR$_{DSON_5}$	PVIN = 5.5V, I_{OUT} = 200mA	+25 (Post Rad)	50	87.15	105	mΩ
HTSSOP Lower FET $r_{DS(ON)}$[2][3]	-55LWR$_{DSON_3}$	PVIN = 3.0V, I_{OUT} = 200mA	-55	16	24.35	33	mΩ
	-55LWR$_{DSON_5}$	PVIN = 5.5V, I_{OUT} = 200mA	-55	12	20.33	30	mΩ
	25LWR$_{DSON_3}$	PVIN = 3.0V, I_{OUT} = 200mA	+25	22	32.3	42	mΩ
	25LWR$_{DSON_5}$	PVIN = 5.5V, I_{OUT} = 200mA	+25	18	27.07	35	mΩ
	125LWR$_{DSON_3}$	PVIN = 3.0V, I_{OUT} = 200mA	+125	35	46.18	55	mΩ
	125LWR$_{DSON_5}$	PVIN = 5.5V, I_{OUT} = 200mA	+125	28	38.91	48	mΩ
	25LWR$_{DSON_3}$	PVIN = 3.0V, I_{OUT} = 200mA	+25 (Post Rad)	22	31.75	50	mΩ
	25LWR$_{DSON_5}$	PVIN = 5.5V, I_{OUT} = 200mA	+25 (Post Rad)	18	26.52	40	mΩ

1. Typical values are at 25°C and are not guaranteed.
2. Typical values shown are at stated temperature and are not guaranteed.
3. Parameter tested in a Test Mode not available to user.
4. Limits established by characterization or design analysis and are not production tested.
5. The operating envelope may be reduced by Minimum On-Time and Minimum Off-Time constraints.

4. Typical Performance Curves

T_A = Room Ambient, unless otherwise noted

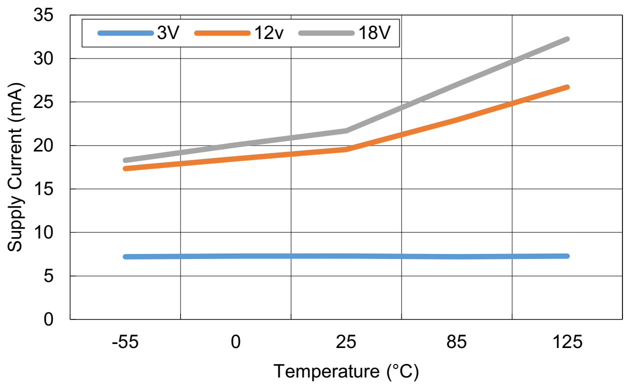


Figure 5. 300kHz - Supply Current vs Temperature

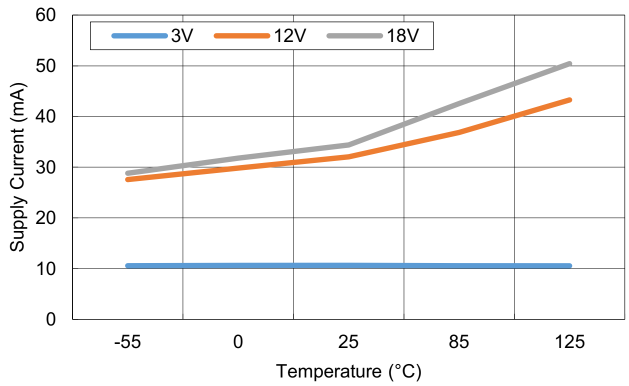


Figure 6. 500kHz - Supply Current vs Temperature

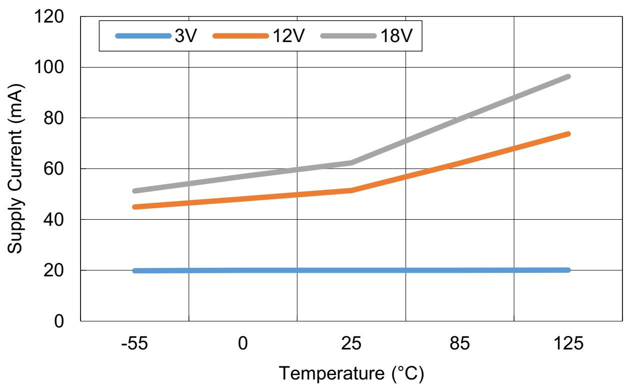


Figure 7. 1000kHz Supply Current vs Temperature

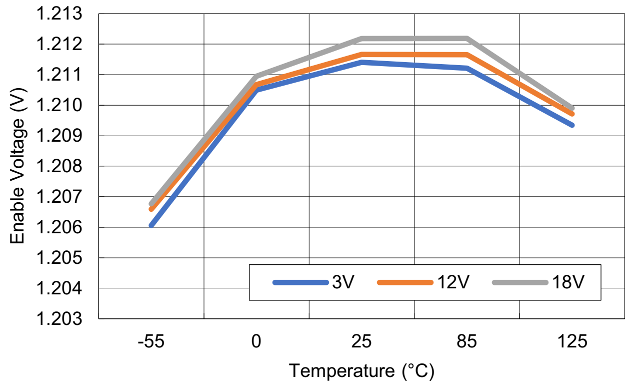


Figure 8. Enable Voltage vs Temperature

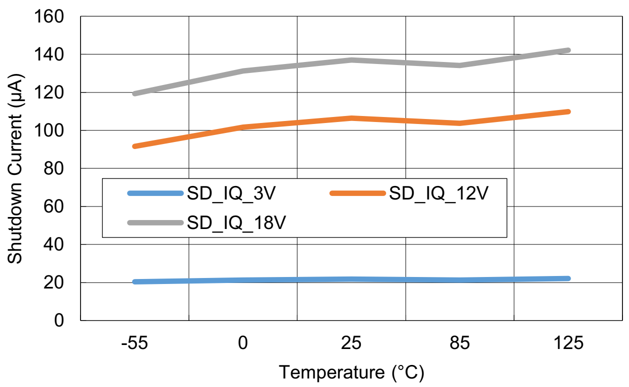


Figure 9. Shutdown Current vs Temperature

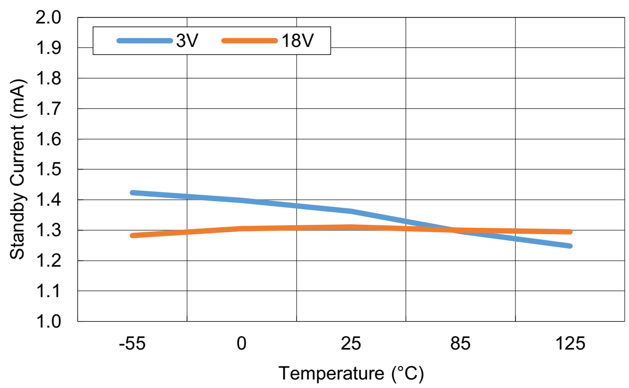


Figure 10. Standby Current vs Temperature

T_A = Room Ambient, unless otherwise noted (Cont.)

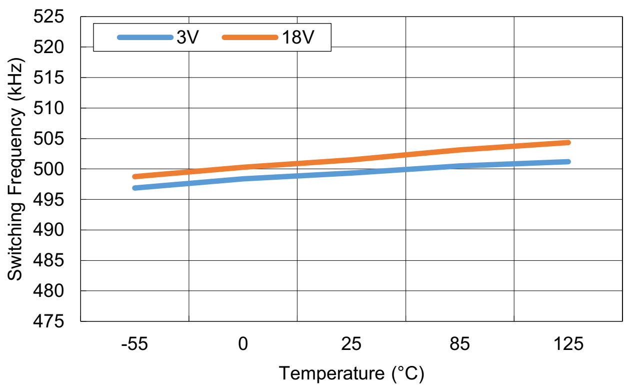


Figure 11. Internal 500kHz Switching Frequency vs Temperature

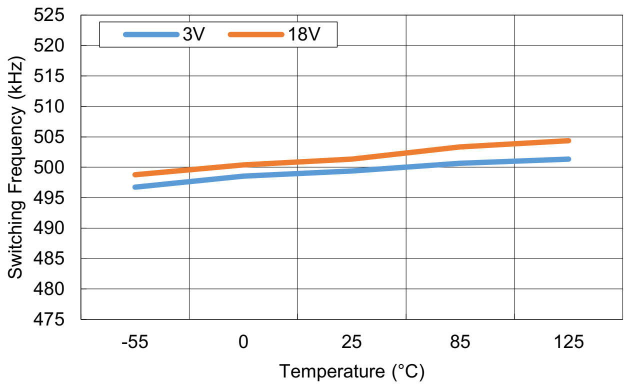


Figure 12. 100kΩ External 500kHz vs Temperature

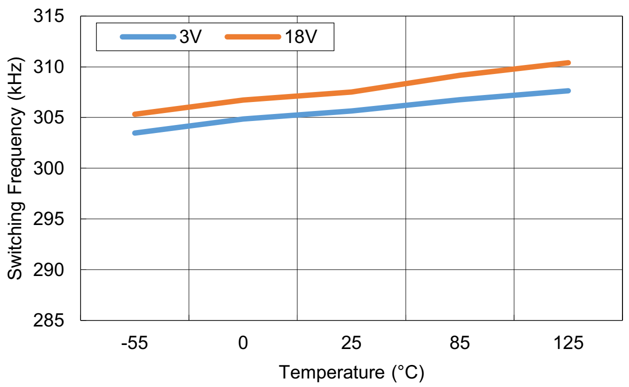


Figure 13. 174kΩ External 300kHz vs Temperature

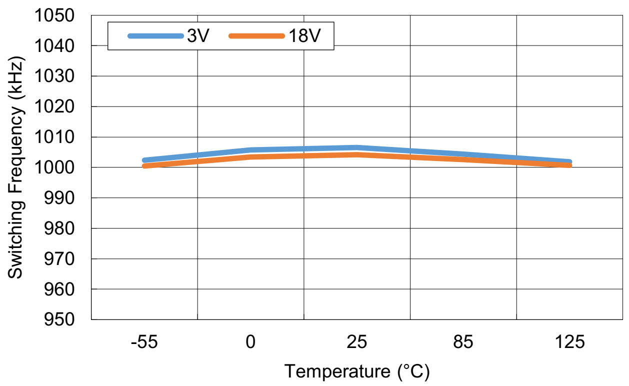


Figure 14. 42.7kΩ External 1000kHz vs Temperature

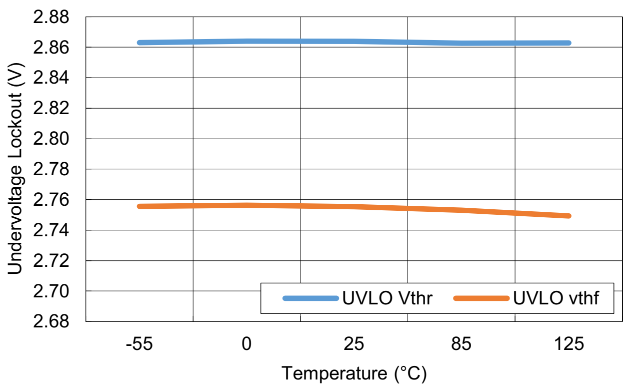


Figure 15. Undervoltage Lockout vs Temperature

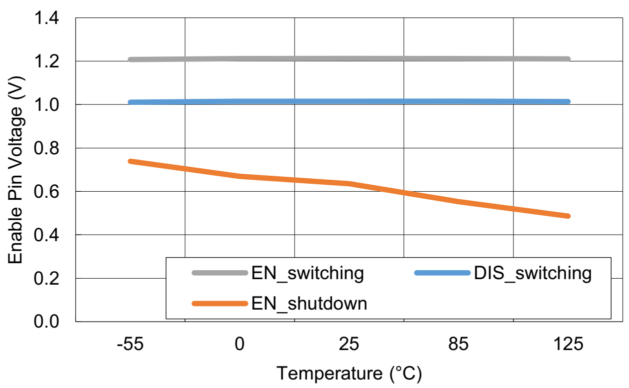


Figure 16. Enable Voltage Threshold vs Temperature

T_A = Room Ambient, unless otherwise noted (Cont.)

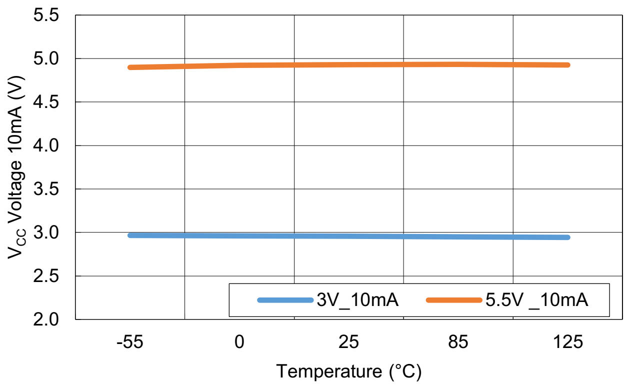


Figure 17. V_{CC} Voltage vs Temperature

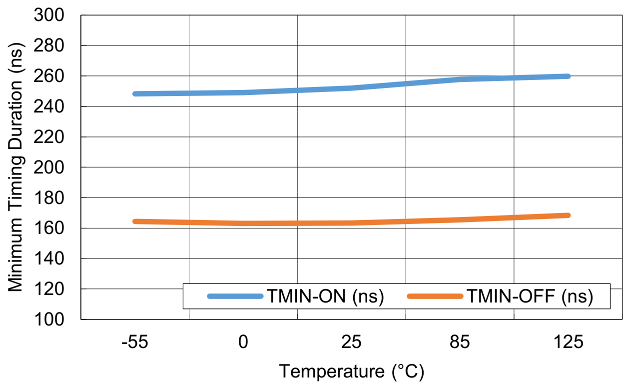


Figure 18. Minimum On-Time/Off-Time vs Temperature

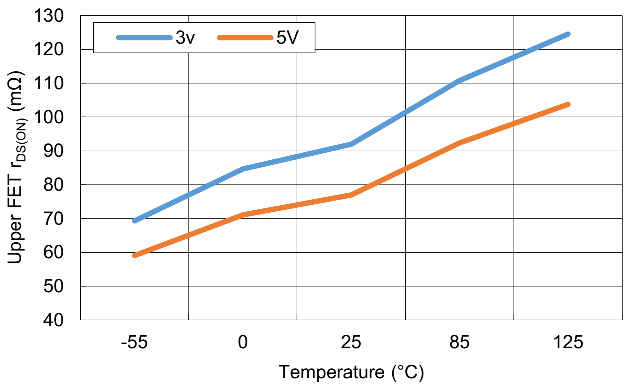


Figure 19. Upper FET $r_{DS(ON)}$ vs Temperature

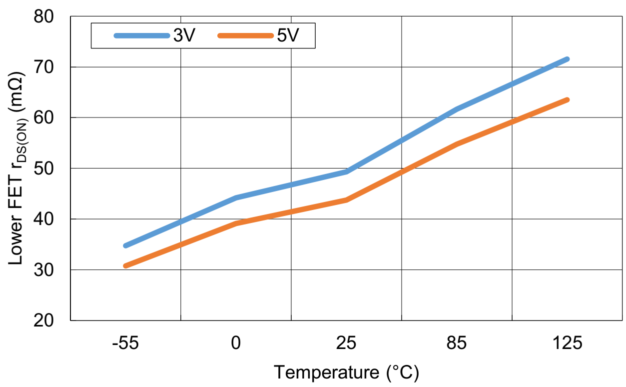


Figure 20. Lower FET $r_{DS(ON)}$ vs Temperature

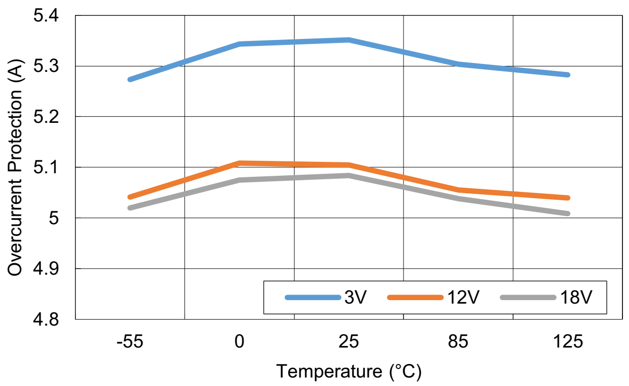


Figure 21. Overcurrent Protection vs Temperature

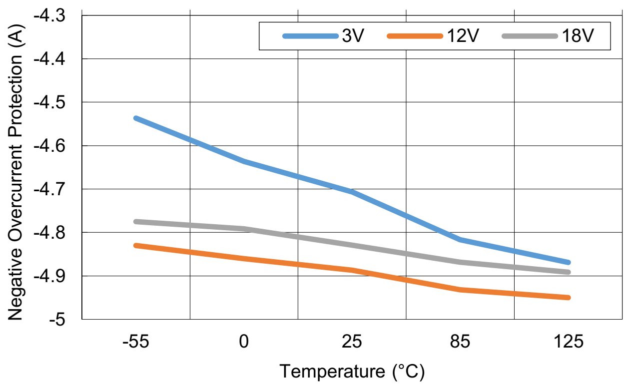


Figure 22. Negative Current Protection vs Temperature

T_A = Room Ambient, unless otherwise noted (Cont.)

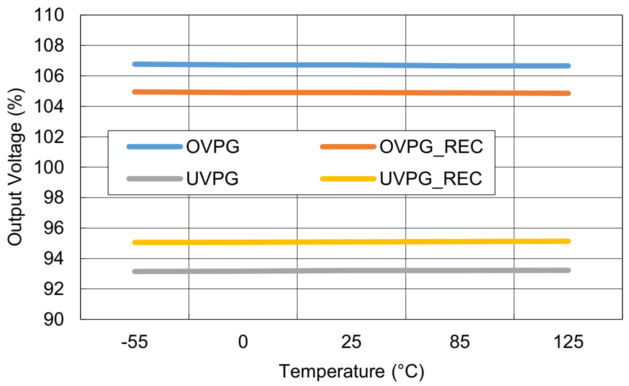


Figure 23. PGOOD Over/Undervoltage Threshold vs Temperature

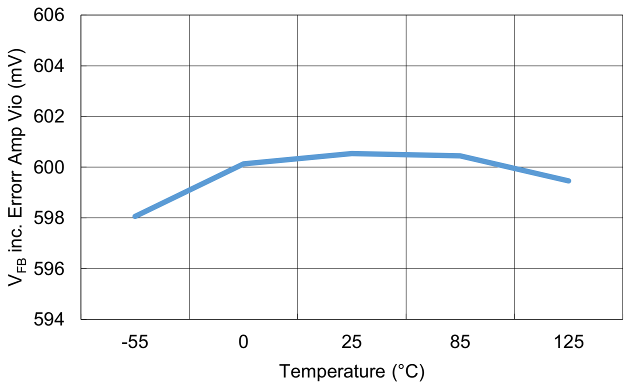


Figure 24. FB Voltage vs Temperature

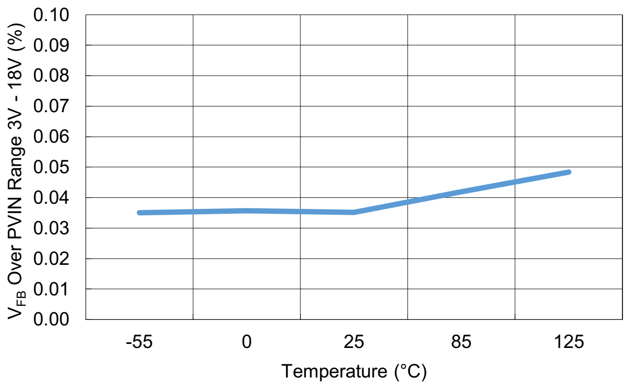


Figure 25. V_{FB} Over PVIN Range vs Temperature

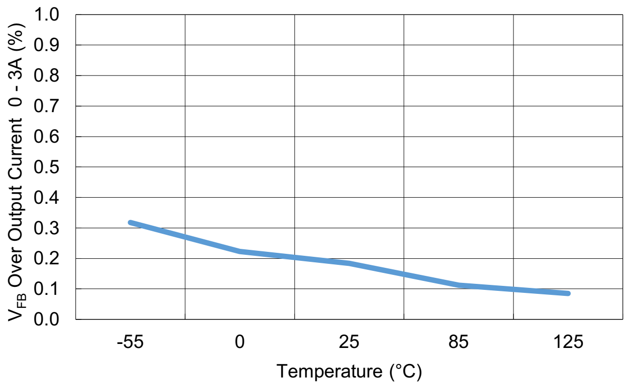


Figure 26. V_{FB} Over Output Current vs Temperature

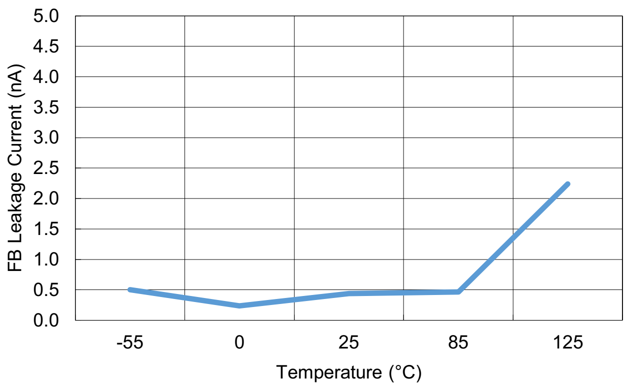


Figure 27. FB Leakage Current vs Temperature

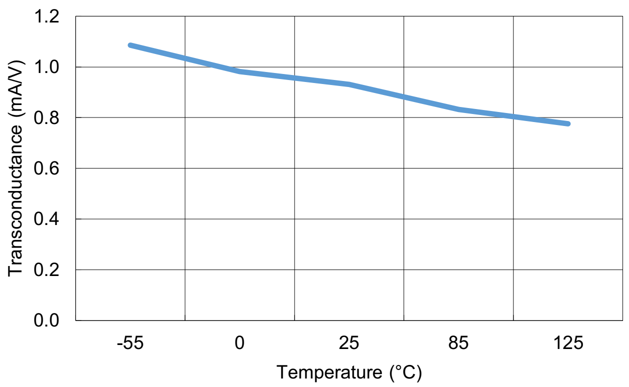


Figure 28. External Compensation Loop Error Amp Transconductance vs Temperature

T_A = Room Ambient, unless otherwise noted (Cont.)

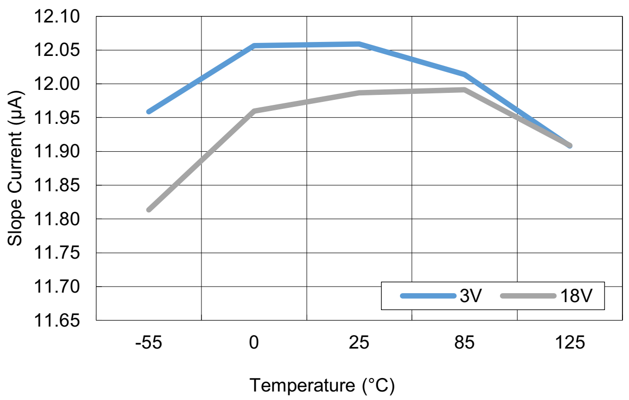


Figure 29. SLOPE Current vs Temperature

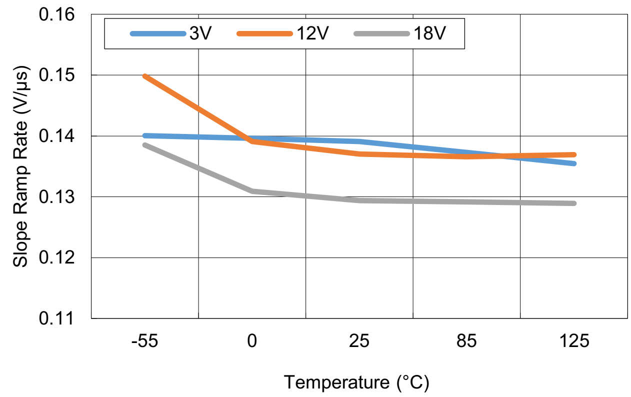


Figure 30. Internal Slope Ramp Rate vs Temperature

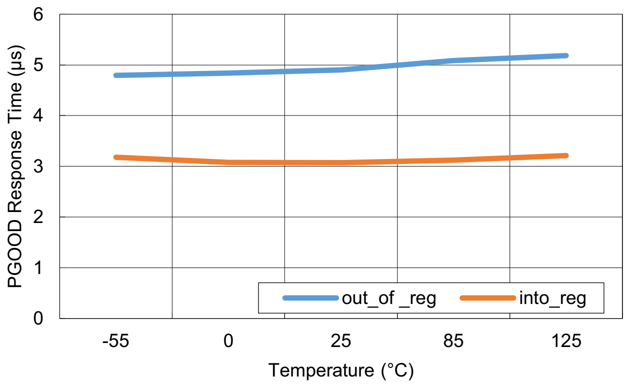


Figure 31. PGOOD Response Time vs Temperature

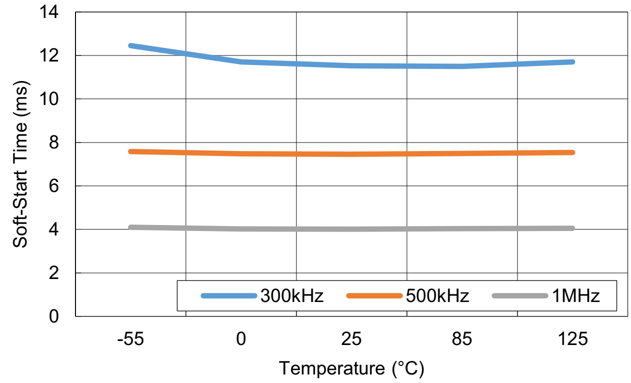


Figure 32. EN to PG Time vs Switching Frequency

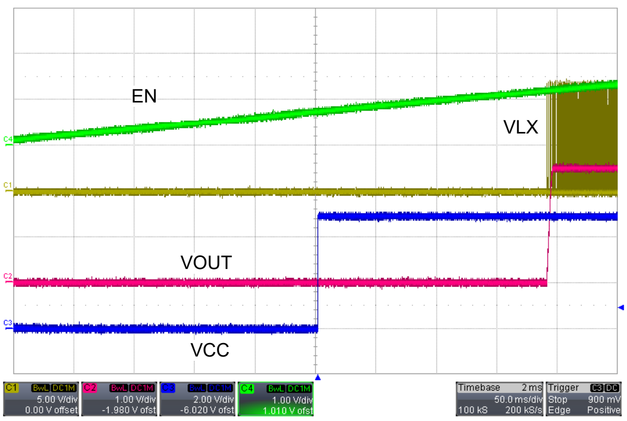


Figure 33. ENABLE to VCC to LX and VOUT Turn-On

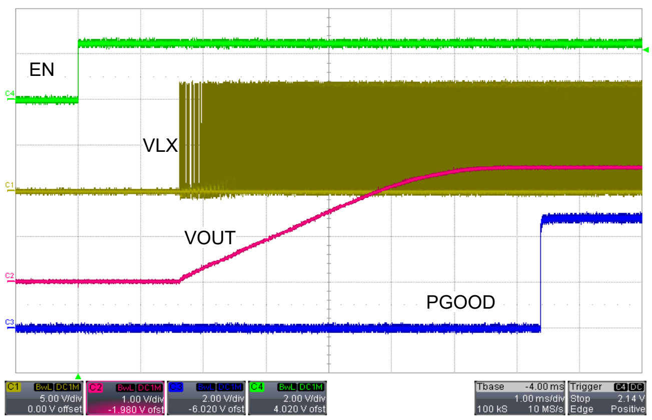


Figure 34. ENABLE to LX and VOUT to PGOOD Turn-On 500kHz

T_A = Room Ambient, unless otherwise noted (Cont.)

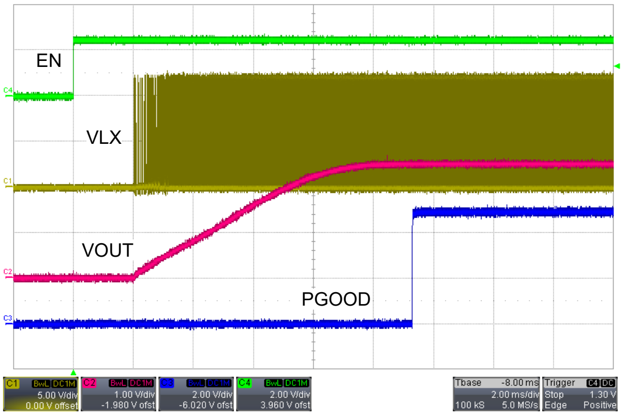


Figure 35. ENABLE to LX and VOUT to PGOOD Turn-On 300kHz

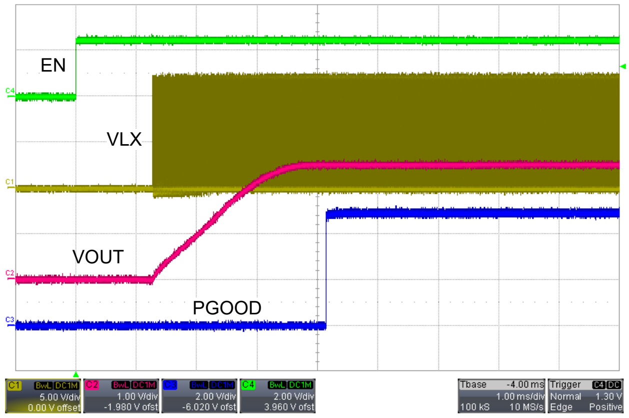


Figure 36. ENABLE to LX and VOUT to PGOOD Turn-On 1000kHz

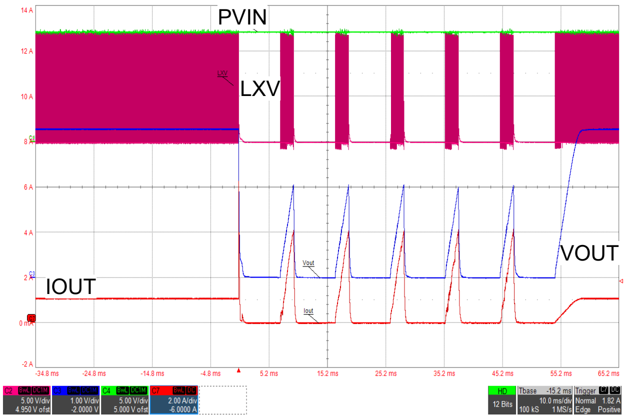


Figure 37. Positive Overcurrent Protection, Overcurrent Event, Restart Attempts into OC to Restart

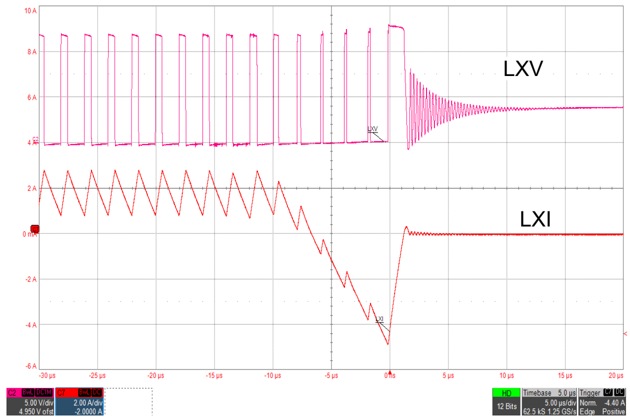


Figure 38. Negative Overcurrent Protection, Negative Overcurrent Event and Shutdown

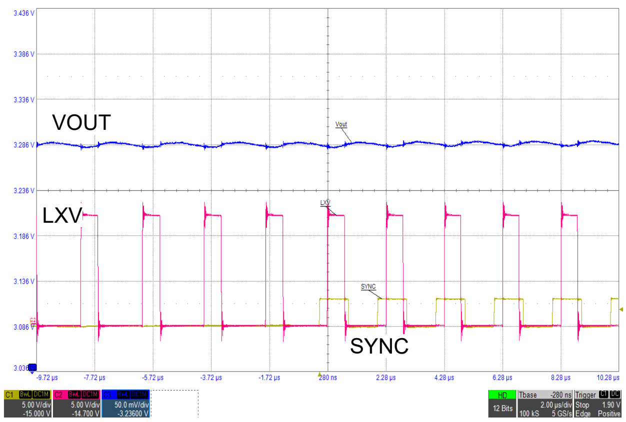


Figure 39. 500kHz SYNC Input Start

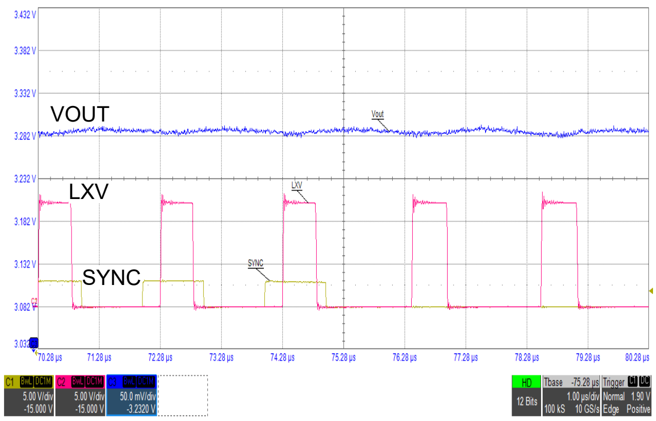


Figure 40. 500kHz SYNC Input Stop

T_A = Room Ambient, unless otherwise noted (Cont.)

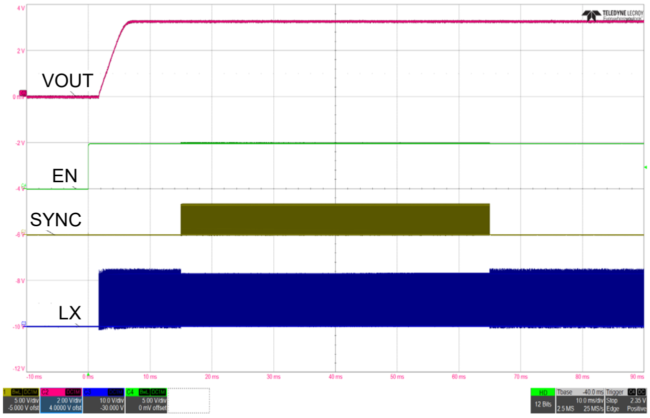


Figure 41. SYNC Turn-On after LX Switching

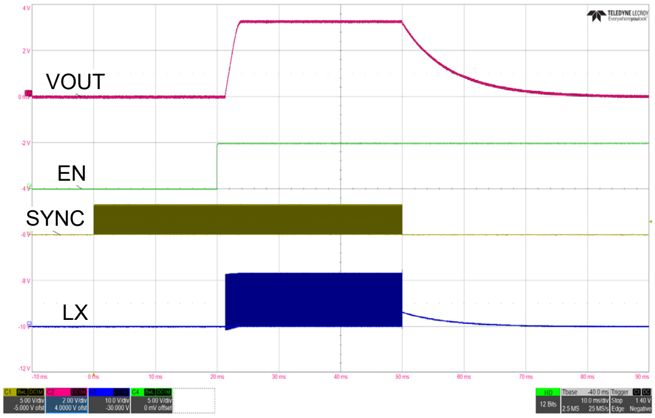


Figure 42. SYNC Turn-On before LX Switching

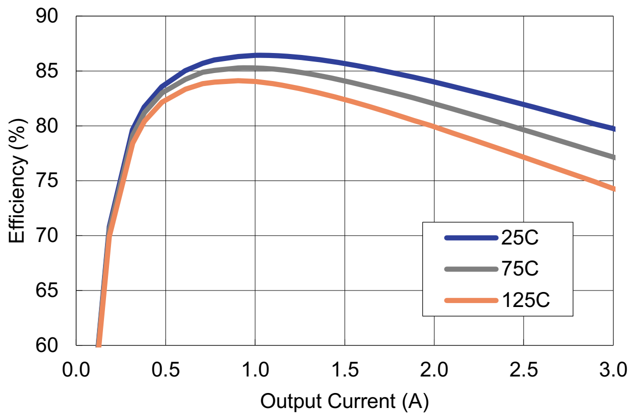


Figure 43. Efficiency 3.3V_{IN}, 1.2V_{OUT}, 1MHz vs Case Temp

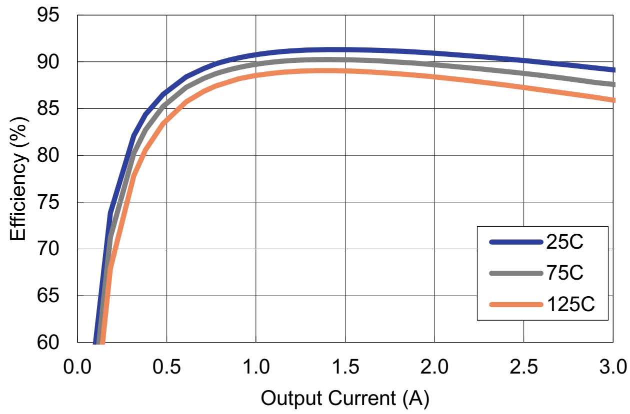


Figure 44. Efficiency 5V_{IN}, 2.5V_{OUT}, 1MHz vs Case Temp

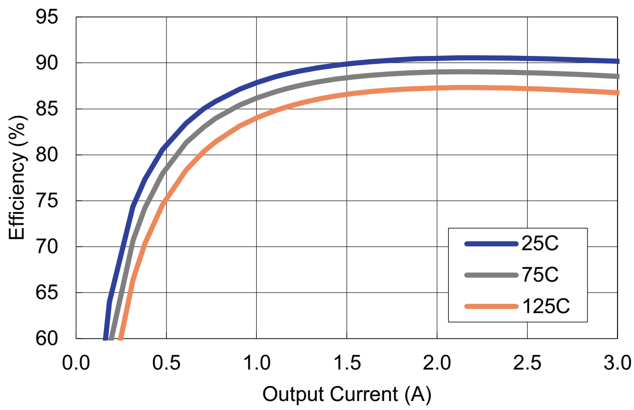


Figure 45. Efficiency 12V_{IN}, 3.3V_{OUT}, 500kHz vs Case Temp

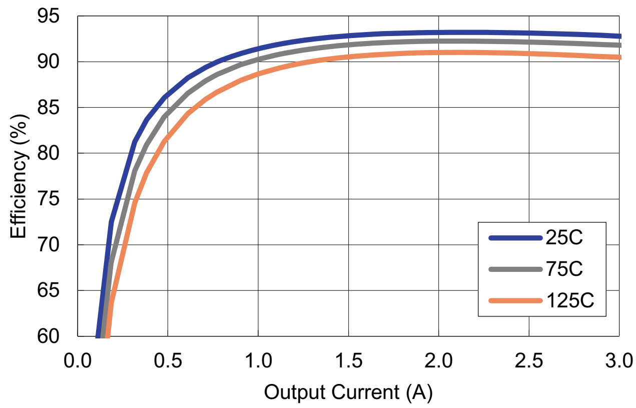


Figure 46. Efficiency 12V_{IN}, 5V_{OUT}, 500kHz vs Case Temp

T_A = Room Ambient, unless otherwise noted (Cont.)

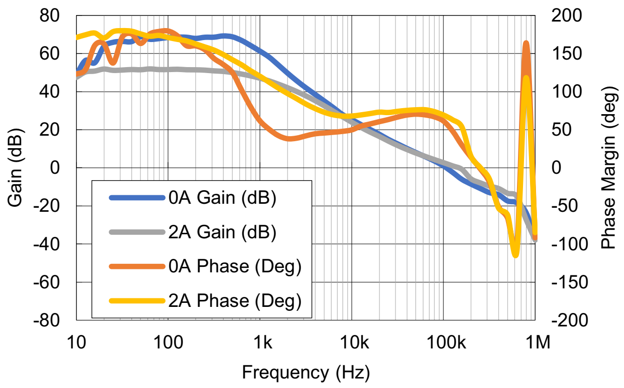


Figure 47. Ext Comp Gain/Phase BODE Plot, $3.3V_{IN}$, $1.0V_{OUT}$, 1MHz, R_{SLOPE} = 34.8kΩ, R_{COMP} = 14kΩ, C_{COMP} = 1200pF, L_{OUT} = 0.82μH, C_{OUT} = 172μF

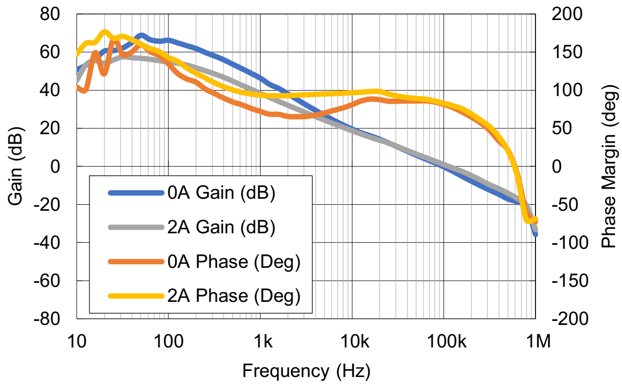


Figure 48. Int Comp Gain/Phase BODE Plot, $3.3V_{IN}$, $1.0V_{OUT}$, 1MHz, L_{OUT} = 0.82μH, C_{OUT} = 172μF

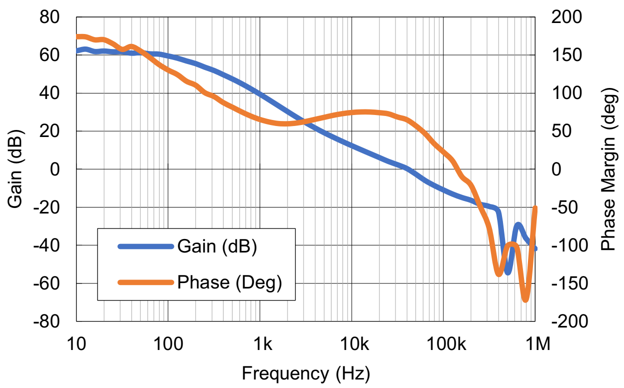


Figure 49. External Comp Gain/Phase BODE Plot, $12V_{IN}$, $3.3V_{OUT}$, 500kHz, I_{OUT} = 1.5A R_{SLOPE} = 44.2kΩ, R_{COMP} = 14kΩ, C_{COMP} = 3900pF, L_{OUT} = 4.7μH, C_{OUT}= 144μF

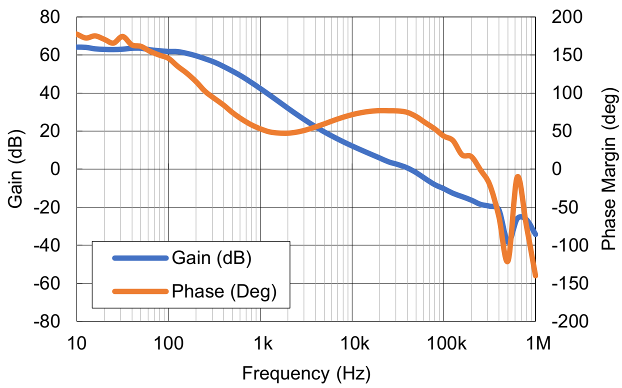


Figure 50. Internal Comp Gain/Phase BODE Plot, $12V_{IN}$, $3.3V_{OUT}$, 500kHz, I_{OUT} = 1.5A L_{OUT} = 4.7μH, C_{OUT} = 144μF

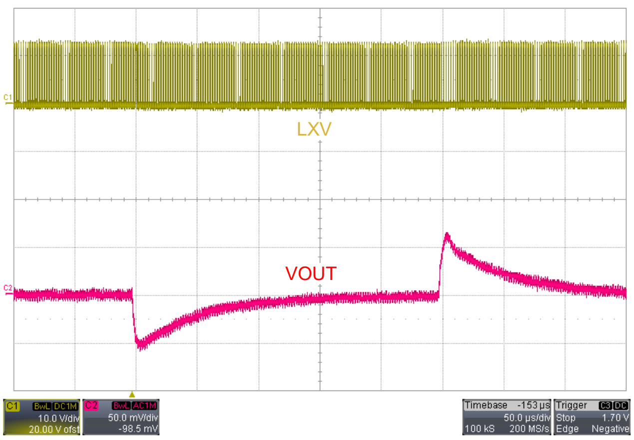


Figure 51. 12VIN, $3.3V_{OUT}$ 500kHz, 2A Load Transient R_{SLOPE} = 44.2kΩ, R_{COMP} = 14kΩ, C_{COMP} = 3900pF, L_{OUT} = 4.7μH, C_{OUT} = 144μF

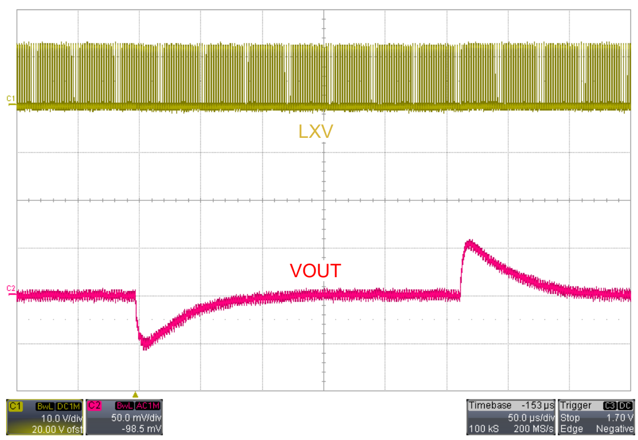


Figure 52. 12VIN, $3.3V_{OUT}$, 500kHz, 2A Load Transient (Internal Compensation), L_{OUT} = 4.7μH, C_{OUT} = 144μF

5. Theory of Operation

5.1 Description of Features

The ISL73007M is a Radiation Hardened by design buck converter using constant frequency peak current mode control architecture for fast loop transient response with a 3V to 18V input voltage regulating down to a minimum 0.6V output voltage adjusted using external resistors. The ISL73007M is capable of >90% efficiency from 1A to the 3A maximum output rated current.

The device operates at a default 500kHz switching frequency and can be resistor adjusted to operate from 300kHz to 1MHz. Implement a wider range of duty cycle operating points at the low end of the switching frequency range. At the high end of the switching frequency range, using smaller inductors and capacitors in the output filter results in a smaller implementation footprint. The V_{IN} to V_{OUT} step-down ratio is restricted by the minimum on and off times, making 1MHz a practical maximum switching frequency. The ISL73007M can be configured such that the switching frequency, the loop, and slope compensations can either be defaulted to internal attributes by tying pins to the VCC or be adjusted externally with passive components to meet particular design requirements and performance optimization. These features can be mixed externally or internally when implemented. This flexibility allows for a basic functional configuration with a minimal BOM or an optimized configuration for the POL task.

5.2 Output Voltage Setting

Use Equation 1 to calculate the required regulated output voltage. For greater voltage accuracy, Renesas recommends using 0.1% feedback resistors.

(EQ. 1) $$V_{OUT} = V_{REF} \times \left(1 + \frac{R_2}{R_1}\right)$$

- V_{OUT} is the required regulated output voltage.
- V_{REF} is the internal reference voltage on the VFB+ pin, which is 0.6V (typical).
- R_1 is the bottom resistor in the feedback divider.
- R_2 is the top resistor in the feedback divider.

5.3 Internal Configuration Summary

The ISL73007M switching frequency, loop compensation, and slope compensation can be configured entirely internally or partially internally with any combination of the three adjustable attributes. The corresponding FS, COMP, and SLOPE pins are connected to VCC to configure each of these internally. Tying FS to VCC invokes the default switching frequency of 500kHz. Tying COMP to VCC configures an internal compensation optimized for <2% transient response for the 1.5A current step.

Internal compensation has the additional benefit of significantly reducing Single Event Transients (SET) compared to external compensation.Tying SLOPE to VCC selects the internal slope compensation with 250mV/T slew rate ($T = 1/f_{SW}$).

5.4 External Configuration Summary

The ISL73007M allows for external configuration of each of the switching frequency, loop compensation, and slope compensation attributes. The switching frequency is externally set by connecting a resistor from the FS (R_{FS}) pin to ground. Renesas recommends selecting a switching frequency between 300kHz (174kΩ) to 1000kHz (42.7kΩ). The resulting frequency is within 10% of the nominal targeted frequency.

To program the external loop compensation, connect a Type II compensation network between the COMP pin and the neighboring SGND pin.

Select the external slope compensation by tying a resistor from the SLOPE pin to ground. The SLOPE pin forces 12µA of current into the R_{SLOPE} resistor (25kΩ ≤R_{SLOPE} ≤ 100kΩ), which sets the voltage reference for the internal slope. A 100kΩ resistor sets a maximum 250mV/T compensation slew rate, while a 25kΩ resistor sets a minimum 62.5mV/T slew rate.

5.5 Frequency Selection

The ISL73007M has a default 500kHz internal clock when the FS pin is tied to VCC. The user can program the switching frequency from 300kHz to 1MHz with a resistor (R_{FS}) from the FS pin to GND. Table 1 shows the resulting nominal switching frequency for the indicated FS to GND resistance used in production testing.

Table 1. Resulting Nominal Switching Frequency

FS to GND Resistor = 42.7kΩ	FS to GND Resistor = 100kΩ	FS to GND Resistor = 174kΩ
Switching Frequency = 1000kHz	Switching Frequency = 500kHz	Switching Frequency = 300kHz

The oscillator circuitry is SET hardened using a combination of redundant timing and reset paths and reset voter signals. Use Equation 2 to find the R_{FS} resistor for the required switching frequency.

(EQ. 2) $$R_{FS}[k\Omega] = \frac{57356}{f_{SW}(kHz)} - 14.53$$

5.6 External Source Frequency Synchronization

The ISL73007M SYNC input allows synchronization of the ISL73007M to an external clock frequency with a 0V to 3.5 to 5V logic level signal. External clock frequency must be a minimum of 15% above the internal oscillator frequency setting. The internal oscillator should not exceed 1000kHz when using external synchronization. The ISL73007M LX switching frequency is synchronized to the external clock frequency within 2 cycles of the internal oscillator. Within one switching cycle after external clock termination, switching frequency returns to the internal oscillator frequency, or terminates LX switching, depending on the operation mode. Figure 39 and Figure 40 show typical behavior for external clock start and stop operation.

The SYNC function has two operation modes determined by the EN and SYNC input sequencing. When the ISL73007M is enabled (EN pin logic high), and LX switching starts before the SYNC input is active, LX switching continues at the internal oscillator frequency after the SYNC signal is stopped (see Figure 41 for an example). When the external clock is applied to SYNC before the ISL73007M is enabled (EN pin logic low), LX switching stops after the SYNC clock is stopped (see Figure 42 for an example).

5.7 Time Constraints on DC/DC Voltage Conversion

The ISL73007M can operate across wide ranges of both input and output voltages; however, the step-down conversion has to adhere to the minimum off and minimum on timing requirements. Determine the down conversion suitability by comparing the t_{ON} and t_{OFF} specifications to the duty cycle high time and low time, respectively, for the intended switching frequency and duty cycle. The timing constraints mostly impact extremely high or low-duty cycle conversions where the minimum off and on times are infringed up. Lowering the switching frequency or changing PVIN are the simple methods to alleviate minimum on-time and off-time concerns.

5.8 Overcurrent Protection

Two levels of overcurrent protection (OCP) are provided for sourcing output current conditions. An accurate current-sensing pilot device parallel to the upper MOSFET is used for the peak current mode control signal and overcurrent protection. The ISL73007M implements cycle-by-cycle peak current limiting, terminating the upper FET on pulse when the FET current reaches the OCP threshold. An OCP fault is triggered if the OCP threshold is exceeded in four of the eight preceding switching periods. On the 4th current peak above the OCP threshold, the upper FET on pulse terminates, the lower FET turns on until the switching cycle is complete, then the device enters the fault state. When entering the fault state, LX output is forced to a Hi-Z state and the output is pulled low by the output loading. When the device attempts to restart, if the OCP occurs again, we go through another hiccup time and repeat until the OCP is not seen during soft-start. When the overcurrent condition goes away, the output soft starts into a regulated output voltage. The typical sourcing OCP threshold is ~5A, ~1.7x the rated output current of 3A, providing headroom for the peak ripple current. Be mindful during inductor selection, as an excessive ripple current lowers the DC output current capability due to OCP.

During the soft-start period, there is an additional level of overcurrent protection of a single instance at ~6A to protect against shorted or otherwise damaged loads. When invoked, this fault goes into hiccup restart cycling until a successful restart occurs.

5.9 Negative Overcurrent Protection (NOCP)

Negative overcurrent protection (NOCP) is provided for sinking output current conditions. If an external source drives current into the regulator output, the controller attempts to regulate the output voltage by reversing its inductor current to absorb the externally sourced current. If the external source is low-impedance, it might reverse the current to an unacceptable level, and the controller initiates its negative overcurrent limit protection. The negative overcurrent protection is realized by monitoring the current through the lower FET. When the valley point of the inductor current reaches the negative current limit of typically -4.8A, the NOCP fault is declared, and the LX out goes into a Hi-Z state. The IC enters into a hiccup mode to restart. There is no valley current counter on the NOCP function.

5.10 Power Good

Power-Good (PG) is the output of a window comparator that continuously monitors the buck regulator output voltage. The PG output is actively held low when EN is low and during the buck regulator soft-start period. After soft-start completes, the PG pin becomes high impedance as long as the output voltage is in nominal regulation of the output voltage. When VFB is typically beyond ±6% of the nominal regulation voltage for ~5µs, the device open drain output pulls the PG output low. Add an external resistor from PG to a maximum of the PVIN voltage for PG signaling purposes.

5.11 UVLO, Enable, Soft-start, Disable, and Soft-Stop

The regulator remains in shutdown mode until PVIN rises above the Undervoltage Lockout (UVLO) threshold of ~2.86V.

The ISL73007M Enable pin allows for three states of operation:

- In Shutdown Mode, the ISL73007M is disabled and draws a typical 105µA from PVIN. A transition to this shutdown state occurs when EN is below the Shutdown Enable Voltage.
- In Standby Mode, EN is above the Standby Enable Voltage and below the Enable Voltage Threshold. The VCC LDO is on, but switching is disabled.
- When EN is above the Enable Voltage Threshold, normal switching operation and soft-start begin.

During soft-start, the ISL73007M monitors for overvoltage (OV) and over-temperature (OT) faults and remains idle if either fault is active. The soft-start time is dependent on the operating switching frequency during startup (see Figure 32). There is a delay from enable active to LX activity during which the ISL73007M internal circuitry is biased. This delay time is frequency dependent, typically 2ms for 300kHz and 1.3ms for 1MHz (see Figure 34 and Figure 35).

The ISL73007M can seamlessly start into a pre-biased output, provided the pre-bias voltage is below the set regulation voltage. At the completion of sot-start the FB is monitored against VREF. If the pre-biased output exceeds the regulation set point, the ISL73007M does not initiate LX switching but turns on the lower FET at the end of the SS PGOOD time, pulling the output down. The lower FET stays on until VOUT is pulled down to the regulation point or the NOC point is hit. If the NOC point is hit, the part hiccups and repeats the start-up sequence until regulation can be achieved.

5.12 Thermal Protection

The device has integrated thermal protection. When the internal temperature reaches a typical value of +161°C, the regulator stops switching. After the internal temperature falls below a typical value of +148°C, the device resumes operation through soft-start. For continuous operation, do not exceed the +150°C junction temperature rating.

5.13 PWM Control and Compensation

The ISL73007M employs constant frequency peak current-mode pulse-width modulation (PWM) control for faster transient response and pulse-by-pulse current limiting. The current loop consists of the current-sensing circuit, slope compensation ramp, and PWM comparator.

Any regulator design starting point is knowing the operating conditions and design goals. These would include the input and output voltages, the switching frequency, the maximum transient current step, and the maximum transient output voltage tolerance. The following compensation equations guide completing an external slope and loop control compensation design. Switching frequency selection is discussed in Frequency Selection.

5.14 Slope Compensation

The ISL73007M offers user-adjustable slope compensation to allow for optimization of power supply performance and stability across the entire PWM duty-cycle range. Slope compensation is a technique in which the current feedback signal is modified by adding slope, that is, a linearly increasing voltage over time. Set the external slope compensation ramp with a resistor (R_{SLOPE}) from the SLOPE pin to ground.

For applications with a maximum duty cycle of less than 50%, slope compensation can improve noise immunity, particularly at lighter loads. For applications with a greater than 50% duty cycle, slope compensation is needed to prevent instability, seen as a sub-harmonic oscillation of the switching LX node. The minimum slope compensation typically required is shown in Equation 3.

(EQ. 3) $$\text{Min Slope Compensation} = \frac{-V_{OUT}}{2 \times L_{OUT}}$$

5.15 External Configuration Application Implementation Equations

This section guides the design for slope compensation, loop compensation and bandwidth, and load transient response. Use Equation 4 to set the inductor downslope.

(EQ. 4) $$S_L\left[\frac{A}{\mu s}\right] = \frac{V_{OUT}[V]}{L[\mu H]}$$

The compensation slope is:

(EQ. 5) $$S_{COMP}\left[\frac{A}{\mu s}\right] = 1.62\left(\frac{R_{SLOPE}[k\Omega]}{R_{FS}[k\Omega]}\right)$$

To increase noise immunity and account for inductor tolerances, Renesas recommends using $S_L = S_{COMP}$ (deadbeat control) so:

(EQ. 6) $$R_{SLOPE}[k\Omega] = 0.62R_{FS}[k\Omega]\frac{V_{OUT}[V]}{L[\mu H]}$$

Due to headroom issues, R_{SLOPE} value must be within $25k\Omega \le R_{SLOPE} \le 100k\Omega$.

Internal slope compensation is set to maximum slope compensation or:

(EQ. 7) $$S_{COMP}\left[\frac{A}{\mu s}\right] = \frac{162}{R_{FS}[k\Omega]}$$

The external R_{COMP} value is set by the transient response requirement on the output voltage, k, calculated using Equation 8, and the load step requirement.

(EQ. 8) $$k = \frac{\Delta V_{OUT}}{V_{OUT}}$$

The calculation also depends on external error amp transconductance (g_m = 0.923mA/V) and modulator transconductance (G_M = 12A/V, which means 250mV voltage step at COMP node causes 3A output current step). Calculate external R_{COMP} using Equation 9.

(EQ. 9) $$R_{COMP} = \frac{\Delta I_{OUT}}{kV_{REF}g_mG_M}$$

Internal compensation is set in such a way as to ensure ±2% V_{OUT} transient response for ±1.5A load current step.

The external C_{COMP} defines compensator zero frequency, f_z:

(EQ. 10) $$f_z = \frac{1}{2\pi R_{COMP}C_{COMP}}$$

Unity gain frequency, f_t, is typically recommended to target $f_{SW}/10$. Set f_z to $f_t/10$ to maximize phase margin. f_z impacts transient response recovery time. Reduce this time by increasing f_z (at the expense of the phase margin). In general, zero frequency should not exceed $f_t/3$ (12.7deg loss of phase margin).

After R_{COMP} is determined, use Equation 11 to calculate the output capacitance, where V_{REF} = 0.6V.

(EQ. 11) $$C_{OUT\_MIN} = \frac{V_{REF}g_mG_MR_{COMP}}{2\pi f_tV_{OUT}}$$

Equation 11 does not guarantee that transient response is met in all cases. The main reason is the nonlinear nature of the switching regulator. To derive equations, approximate the modulator with a simple (and linear) G_M stage, which means any fast dV/dt at the input of G_M produces equally fast dI/dt at the output. Because the output inductor (L) limits dI/dt (dI/dt = V/L), in some cases (typically extremely low D or extremely large D), the current slew rate dI/dt = V/L might get limited by V/L in which case transient response is going to be larger than expected. In those cases, reduce L to increase dI/dt or increase C_{OUT} to slow down dV/dt at the G_M input.

In the case of internal compensation (set for ±2% VOUT transient response with ±1.5A load current step), calculate C_{OUT_MIN} using Equation 12:

(EQ. 12) $$C_{OUT\_MIN} = \frac{V_{REF}A_{EAP}G_M}{2\pi f_tV_{OUT}}$$

Equations are derived for ideal C_{OUT}. Treat MLCCs as ideal capacitors because of small parasitic components (ESR and ESL). In cases where they cannot be used, carefully consider the ESR value. In the case of extremely fast transients (1A/ns for microprocessors), voltage drop (ESR x dI) appears extremely quickly, and the regulation loop cannot react that fast. In those cases, increase C_{OUT}. Transient response effectively has two components (ESR and C_{OUT}). The solution is to reduce C_{OUT} transient by the ESR x dI product value. For example, if 2% transient is required and ESR x dI causes 0.5% transient response, use 1.5% transient to determine the external R_{COMP}.

Regarding loop stability, ESR zero must be canceled by a pole created with C_{POLE} such that:

(EQ. 13) $$ESR \times C_{OUT} = R_{COMP}C_{POLE}$$

The temperature coefficient of the ESR can be significant and cause difficulty with this. Careful evaluation for wide temperature range operations is needed. Consider a combination of Tantalum and MLCC capacitors to achieve high total capacitance with lower ESR.

6. Typical Application

6.1 Typical Application Schematic

This section guides the design and component selection for a typical buck converter application using the ISL73007. A design calculator is available for download to support designers in component selection. The typical application schematic for an ISL73007 design using external compensation configuration is shown in Figure 53.

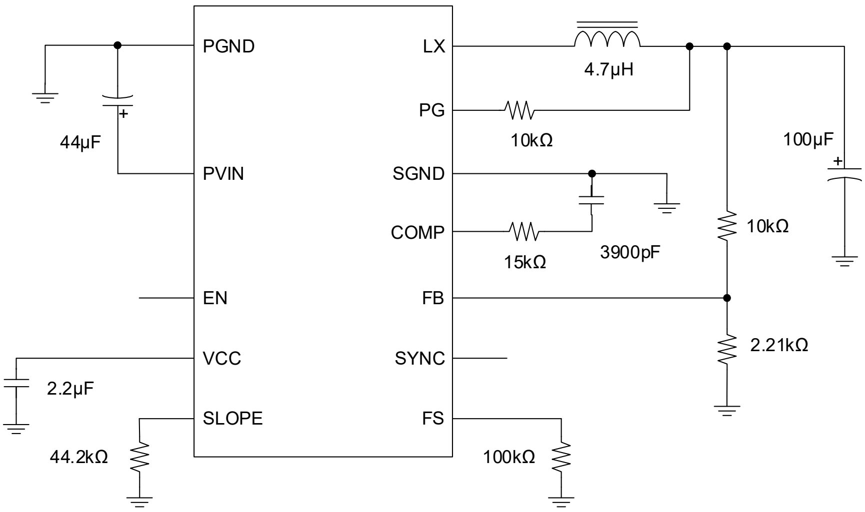


Figure 53. External Compensation Application Diagram for 12V to 3.3V, 500kHz

6.2 Design Requirements

Table 2 lists the design requirements for an example application using ISL73007 with external compensation configuration

Table 2. Design Requirements

Parameter	Min	Typ	Max	Units
Input Voltage	10.8	12	18	V
Output Voltage	-	3.3	-	A
Output Current	0	-	3	A
Output Voltage Transient Tolerance	-	-	2	%
Output Current Load Step	-	-	2	A
Switching Frequency	-	500	-	kHz

6.3 Set Output Voltage

The output voltage regulation point is set using the feedback resistor divider. Select an upper FB resistor (R2) value of 10kΩ. Rearrange Equation 1 to calculate the lower FB resistor (R1) value based on the required output voltage of 3.3V.

(EQ. 14) $$R_1 = \frac{R_2}{\frac{V_{OUT}}{V_{REF}} - 1}$$

$$R_1 = \frac{10k\Omega}{\frac{3.3V}{0.6V} - 1} = 2.22k\Omega$$

Select 2.21kΩ as a standard resistor value for R1.

6.3.1 Output Voltage Feedback Resistors When Using SYNC

In general applications, choosing the lower feedback resistor of 2kΩ for the ISL73007M is a good starting point. The upper feedback resistor ranges up to 14.7kΩ for V_{OUT} = 5V and 38kΩ for V_{OUT} = 12V, which is low enough impedance to not be susceptible to noise coupling. The 600mV across 2kΩ draws 300µA, keeping the application in a low operating current state.

However, for applications that use the SYNC pin for external clock synchronization, Renesas recommends decreasing the lower feedback resistor value to 200Ω. Because the FB and SYNC pins are next to each other, there is a coupling of clock switching noise from the SYNC pin to the FB pin. This coupling causes a small bi-modal modulation of the LX pulse width, producing a minor ripple component in V_{OUT}. Reducing the lower feedback resistor to 200Ω for setting VOUT minimizes the coupling of the SYNC to the FB pin. This reduction increases the feedback network current to 3mA, 0.1% of the 3A full load rated current. Figure 54 demonstrates how a lower feedback network resistance reduces coupling from SYNC to improve the output voltage ripple, when compared with Figure 55.

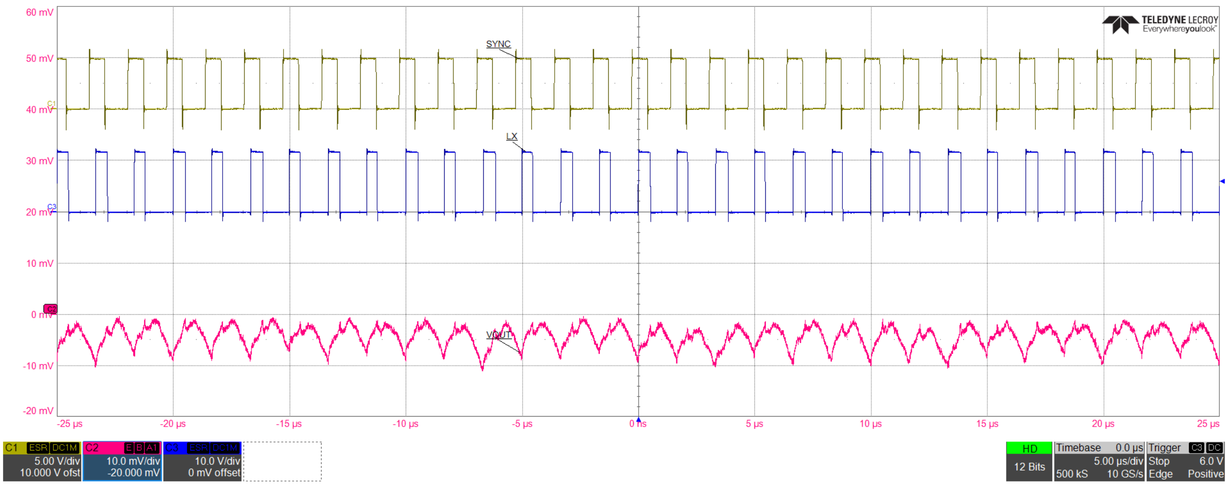


Figure 54. Output Voltage Ripple with External Clock (V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 3A, R1 = 221Ω, R2 = 1kΩ, $SYNC_{freq}$ = 600kHz)

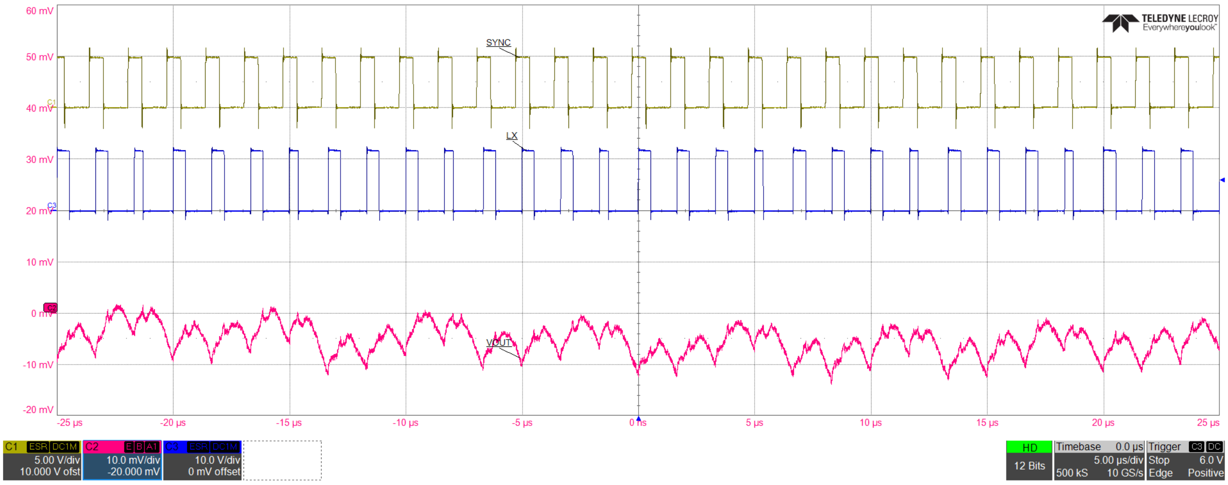


Figure 55. Output Voltage Ripple with External Clock (V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 3A, R1 = 2.21kΩ, R2 = 10kΩ, $SYNC_{freq}$ = 600kHz)

6.4 Set Switching Frequency

Substitute the target switching frequency into Equation 2 to calculate the required FS resistor.

(EQ. 15) $$R_{FS}[k\Omega] = \frac{57356}{500[kHz]} - 14.53 = 100.18[k\Omega]$$

Select 100kΩ as a standard resistor value for R_{FS}.

6.5 Input Capacitor Selection

Use a mix of input bypass capacitors to control the voltage overshoot and undershoot across the internal MOSFETs of the synchronous buck regulator. Use small low ESR ceramic capacitors for high-frequency decoupling and bulk capacitors to supply the current needed each time the upper MOSFET turns on. Place the small ceramic capacitors physically close to the IC between the PVIN and PGND pins.

The critical parameters for the bulk input capacitance are the voltage and RMS current ratings. For reliable operation, select bulk capacitors with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. Their voltage rating should be at least 1.5 times greater than the maximum input voltage, while a voltage rating of 2.5 times is a conservative guideline when considering voltage derating performance to 125°C. Consult the capacitor datasheets for temperature derating tables. For most cases, the RMS current rating requirement for the input capacitor of a buck regulator is approximately 1/2 the DC load current.

Use Equation 16 to closely approximate the maximum RMS current through the input capacitors.

(EQ. 16) $$I_{CINrms} = \sqrt{\frac{V_{OUT}}{V_{IN}} x \left(I_{OUT_{MAX}}{}^{2} x \left(1 - \frac{V_{OUT}}{V_{IN}}\right) + \frac{1}{12} x \left(\frac{V_{IN} - V_{OUT}}{Lxf_{OSC}} x \frac{V_{OUT}}{V_{IN}}\right)^{2}\right)}$$

The minimum recommended input capacitance for the ISL73007M is 44µF. Place these high-frequency, low-ESR capacitors close to the PVIN and PGND pins. These capacitors provide the instantaneous current into the buck regulator during the high-frequency switching transitions.

6.6 Output Capacitor Selection

An output capacitor is required to filter the inductor ripple current and supply the load transient current. The filtering requirements are a function of the switching frequency and the ripple current. The load transient requirements are a function of the slew rate (di/dt) and the magnitude of the transient load current. These requirements are generally achieved with a combination of bulk and decoupling capacitors with a careful layout.

High-frequency, low ESR ceramic capacitors initially supply the transient load current and reduce the current load slew rate seen by the bulk capacitors. The Effective Series Resistance (ESR) and voltage rating requirements generally determine the bulk filter capacitor values rather than actual capacitance requirements. Place high-frequency decoupling capacitors as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components.

The shape of the output voltage waveform during a load transient that represents the worst-case loading conditions ultimately determines the number of output capacitors and their type. When this load transient is applied to the regulator, most of the current required by the load is initially contributed by the output capacitors. This is due to the finite amount of time required for the inductor current to slew up or down to the level of the output current required by the load. This results in a momentary undershoot or overshoot in the output voltage. At the initial edge of the transient undershoot or overshoot, the Equivalent Series Inductance (ESL) of each capacitor induces a spike that adds on top of the voltage drop due to the ESR. After the initial spike, the output voltage dips down (load step on) or peaks up (load step off) as the output capacitor sources or sinks the transient load current until the output inductor current reaches the load current. Figure 56 shows a typical response of the output voltage to a transient load current.

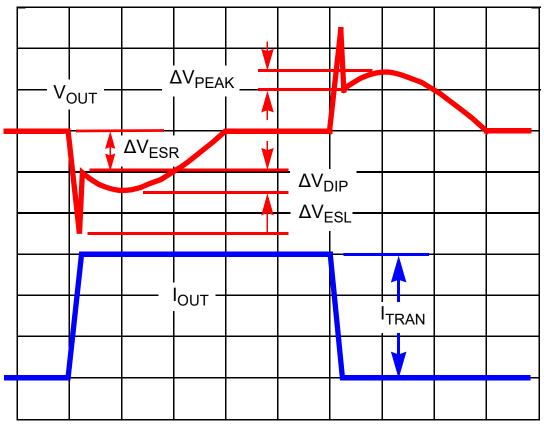


Figure 56. Typical Transient Response

Use Equation 17 to approximate the amplitudes of the voltage spikes caused by capacitor ESR and ESL, where I_{TRAN} = Output load current transient.:

(EQ. 17)

$$\Delta V_{ESR} = ESR \times I_{TRAN}$$

$$\Delta V_{ESL} = ESL \times \frac{dI_{TRAN}}{dt}$$

In a typical converter design, the ESR of the output capacitor bank impacts the transient response. The ESR and the ESL determine the number and types of output capacitors required to minimize the initial voltage spike at the output transient response. It may be necessary to place multiple output capacitors of both ceramic (to provide low ESR, ESL) and Tantalum (to provide the bulk capacitance in a small footprint) types in parallel to reduce the parasitic ESR and ESL to achieve minimize the magnitude of the output voltage spike during a load transient response.

The ESL of the capacitor is an important parameter and not usually listed in the datasheet. Use Equation 18 to approximate ESL if an Impedance vs Frequency curve is available, where f_{res} is the frequency where the lowest impedance is achieved (resonant frequency). The ESL of the capacitor becomes a concern when designing circuits that supply power to loads with high rates of change in the current.

(EQ. 18)
$$ESL = \frac{1}{C(2 \times \pi \times f_{res})^2}$$

If ΔV_{DIP} and/or ΔV_{PEAK} is too large for the output voltage limits, increasing the capacitance might be needed. A trade-off between output inductance and output capacitance might be necessary in this situation.

Calculate output impedance based on stability and transient response requirement.

Substituting into Equation 11 results in:

(EQ. 19)
$$C_{OUT\_MIN} = \frac{0.6V \times 0.923mA/V \times 12A/V \times 15k\Omega}{2\pi \times 50kHz \times 3.3V} = 96\mu F$$

Using a combination of ceramic and tantalum capacitors and allowing for additional margin, select 2x 22µF ceramic and 1x 100µF tantalum capacitors.

6.7 Output Inductor Selection

The inductor value determines the ripple current of the power supply. A reasonable starting target for inductor ripple current is ~33% of the total load current. The output inductor influences the response time of the regulator to a load transient. A smaller inductance value improves transient response but increases output voltage ripple. The inductor value determines the inductor ripple current, with the output voltage ripple being a function of the ripple current. Use Equation 20 to approximate the inductor ripple current and Equation 21 to approximate the output voltage ripple, where ESR is the output capacitor equivalent series resistance.

(EQ. 20)
$$I_{RIPPLE} = \frac{(V_{IN} - V_{OUT})}{f_{SW} \times L} \times \frac{V_{OUT}}{V_{IN}}$$

(EQ. 21)
$$V_{OUT\_RIPPLE} = I_{RIPPLE}\left(\frac{1}{8 \times C_{OUT} \times f_{SW}} + ESR\right)$$

Increasing inductance reduces the ripple current and output voltage ripple; however, the regulator response time to transient load increases.

One of the parameters limiting the regulator response to a load transient is the time required to change the inductor current. The response time is the time required to slew the inductor current from its initial level to the transient level. During this interval, the difference between the inductor and transient load current is sourced from or sunk into the output capacitor. Minimizing the response time reduces the amount of transient voltage overshoot and undershoot on the output capacitor.

The worst-case response time can be during either the load step on or off. Check for transient load response for both turn-on and turn-off at the minimum and maximum load current.

Based on Equation 20, a standard inductor value of 4.7µH results in the following inductor ripple current, which is near our starting target of 33%.

(EQ. 22)
$$I_{RIPPLE} = \frac{(12V - 3.3V)}{500kHz \times 4.7\mu H} \times \frac{3.3V}{12V} = 1.018A$$

6.8 Slope Compensation Resistor

Substitute the selected FS resistor and inductor values into Equation 6 to calculate the slope compensation resistor.

$$R_{SLOPE}[k\Omega] = 0.62 \times 100k\Omega \times \frac{3.3V}{4.7\mu H} = 43.5k\Omega$$

Select 44.2kΩ as a standard resistor value for R_{SLOPE}.

6.9 Compensation Resistor

The external compensation resistor depends on the target load transient response. For a 2% output voltage ripple requirement at a 2A load step, ΔV_{OUT} = 66mV:

(EQ. 23) $$k = \frac{0.066}{3.3} = 0.02$$

Substituting into Equation 9 results in the below compensation resistor value

$$R_{COMP} = \frac{2A}{0.02 \times 0.6V \times 0.923mA/V \times 12A/V} = 15.048k\Omega$$

Select 15kΩ as a standard resistor value for R_{COMP}.

6.10 Compensation Capacitor

Using Equation 10, a compensation capacitor value of 3.3nF results in the following compensator zero frequency:

(EQ. 24) $$f_z = \frac{1}{2\pi \times 15k\Omega \times 3.3nF} = 3.2kHz$$

7. Layout Considerations

Proper layout of the PCB for the switching converter is essential to ensure the switching converter works well to minimize EMI and noise and ensure first pass success of the design. Figure 57 shows the connections of the most critical top-layer components.

Note: Capacitors C_{IN} and C_{OUT} can each represent multiple physical capacitors.

Renesas recommends using a multilayer printed circuit board with buried GND planes. A critical connection is a thermal connection from the package thermal pad to the PCB PGND plane on the top layer. Additionally, connect the IC PGND pins to this GND plane. This connection of the GND pins to the system GND plane ensures a low-impedance path for all return currents and an excellent thermal path to dissipate heat. With this connection made, place the high-frequency ceramic input capacitor(s) across the PVIN and PGND pins. The bulk capacitance can be further away.

The power loop comprises the output inductor (L_{OUT}), the output capacitor (C_{OUT}), the LX pins, and the PGND pin. Make the power loop as short as possible and the connecting traces direct, short, and wide. The LX node connection to the output inductor is noisy due to high dV/dt switching waveforms. Ensure that the voltage feedback trace is kept away from this noisy area. Connect C_{OUT} tightly to L_{OUT} and directly as possible to the PGND pins.

If implemented, the external compensation loop should also be as short as possible, with the connecting traces to R_{COMP} and the C_{COMP} directly between the COMP and SGND pins. The SGND pin should be connected at one point to the PGND plane, out of the high current path of the ground plane. A convenient place is under the package to the thermal pad. If implementing internal compensation, tie the COMP pin to VCC as directly as possible, likewise for internal SLOPE and FS for the internal switching frequency selection. The two latter connections are not as critical and can be placed last.

The heat of the IC is mainly dissipated through the thermal pad. Maximizing the copper area connected to the thermal pad is preferable. In addition, a solid buried ground plane is helpful for better EMI performance with a cutout of the top-level LX shape to reduce coupling. Renesas recommends referencing TB499 for guidance about via ground connections within the pad for the best thermal relief.

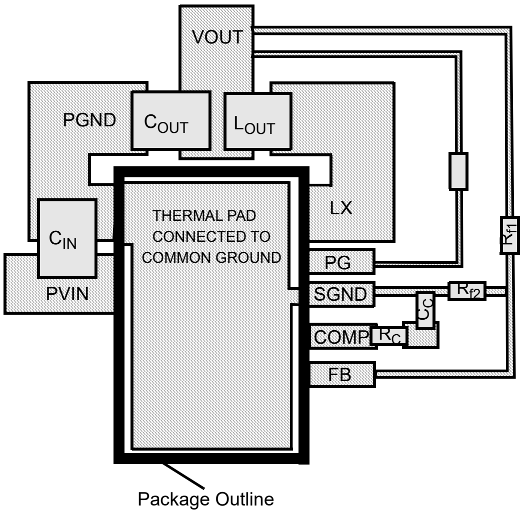


Figure 57. Layout Component Placement Suggestion

8. Radiation Tolerance

The ISL73007M is a radiation tolerant device for commercial space applications, Low Earth Orbit (LEO) applications, high altitude avionics, launch vehicles, and other harsh environments. This device response to Total Ionizing Dose (TID) radiation effects and Single Event Effects (SEE) has been measured, characterized, and reported in the following sections. The TID performance of the ISL73007MVZ is not guaranteed through radiation acceptance testing. The ISL73007M30VZ is radiation lot acceptance tested (RLAT) to 30krad(Si), and the ISL73007M50VZ is RLAT to 50krad(Si). The SEE characterized performance is not guaranteed.

8.1 Total Ionizing Dose (TID) Testing

8.1.1 Introduction

Total dose testing of the ISL73007M proceeded in accordance with the guidelines of MIL-STD-883 Test Method 1019. The experimental matrix consisted of 23 samples irradiated under bias, and 12 samples irradiated with all pins grounded (unbiased). Two control units were used. Figure 58 shows the bias configuration.

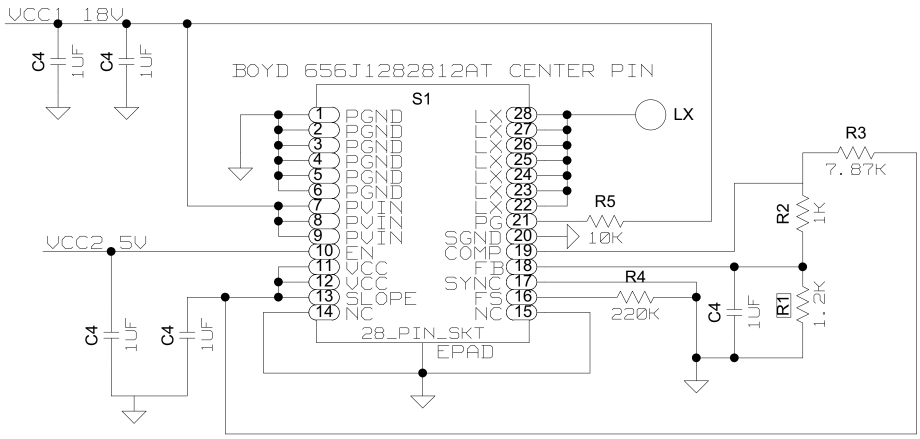


Figure 58. Irradiation Bias Configuration for the ISL73007M

Samples of the ISL73007M were drawn from wafer lots F6X591, F6X592, and F6X593, and were packaged in the production 28-lead HTSSOP. The samples were screened to datasheet limits at room temperature only before irradiation.

Total dose irradiations were performed using a Hopewell Designs N40 panoramic vault-type low dose rate ^{60}Co irradiator located in the Renesas Palm Bay, Florida Facility. The dose rate was 10mrad(Si)/s. PbAl spectrum hardening filters shielded the test board and devices under test against low energy secondary gamma radiation.

Downpoints for the testing were 0krad(Si), 10krad(Si), 30krad(Si), and 50krad(Si).

All electrical testing was performed outside the irradiator using production Automated Test Equipment (ATE) with data logging of all parameters at each downpoint. All downpoint electrical testing was performed at room temperature.

8.1.2 Results

Table 3 summarizes the attributes data. A Pass indicates a device that passes all the datasheet specification limits.

Table 3. ISL73007M Total Dose Test Attributes Data

Dose Rate mrad(Si)/s	Bias	Sample Size	Downpoints	Pass	Fail
10	Figure 58	23	Pre-Rad	23	0
			10krad(Si)	23	0
			30krad(Si)	23	0
			50krad(Si)	23	0
10	Grounded	12	Pre-Rad	12	0
			10krad(Si)	12	0
			30krad(Si)	12	0
			50krad(Si)	12	0

The plots in Figure 59 through Figure 65 show data for key parameters at all downpoints. The plots show the sample size average as a function of the total dose for each irradiation condition. All parts showed excellent stability over irradiation.

8.1.3 Typical Radiation Performance

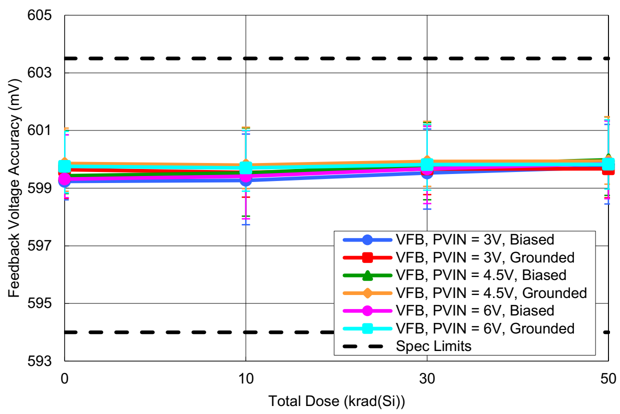


Figure 59. Voltage Feedback Accuracy

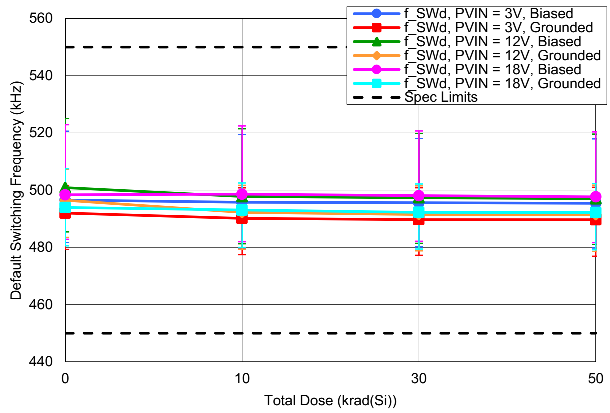


Figure 60. Default Switching Frequency

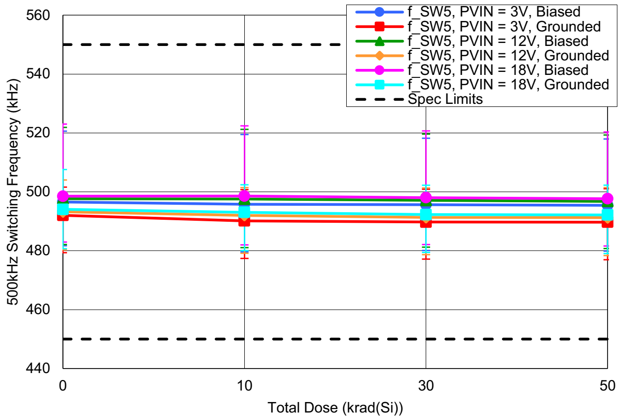


Figure 61. 500kHz Switching Frequency

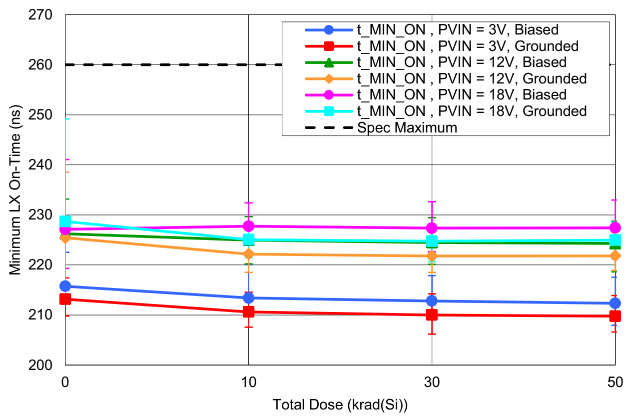


Figure 62. Minimum LX On-Time

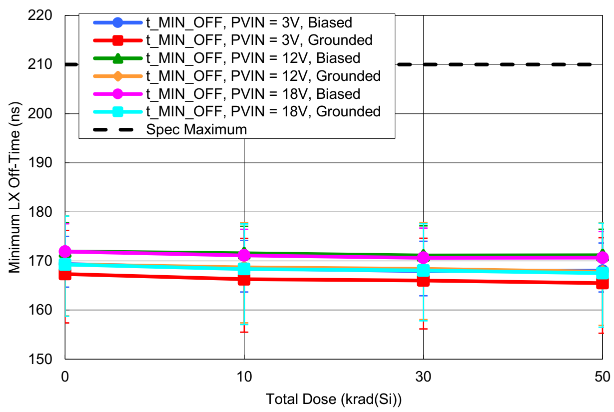


Figure 63. LX Minimum Off-Time

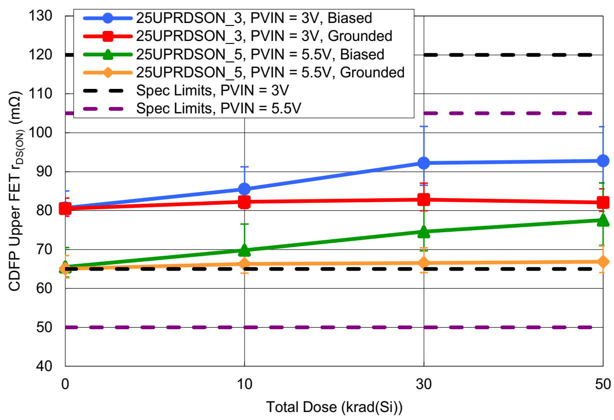


Figure 64. CDFP Upper FET $r_{DS(ON)}$

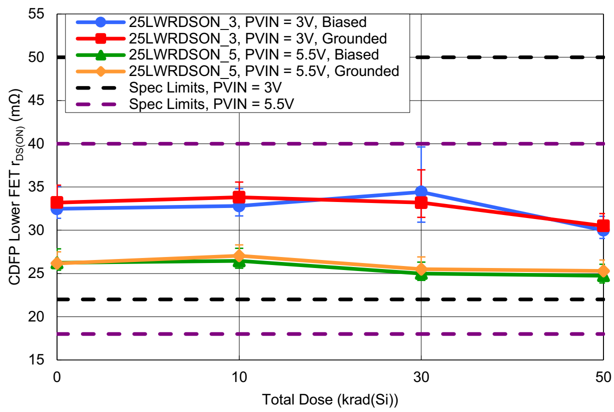


Figure 65. CDFP Lower FET $r_{DS(ON)}$

8.1.4 Conclusion

ATE characterization testing showed no rejects to the datasheet limits at all downpoints. Variables data for selected parameters are presented in Figure 59 through Figure 65. Table 4 shows the average of other key parameters with respect to total dose in tabular form. No differences between biased and unbiased irradiation were noted and the part is not considered bias sensitive.

Table 4. Response of Key Parameters vs TID

Parameter	Symbol	Irradiation Condition	Pre-Rad Value	10krad(Si)	30krad(Si)	50krad(Si)	Unit
Operating Supply Current	I_{PVIN_OPER}	Biased	36.02	35.97	36.40	36.49	mA
		Grounded	36.46	36.16	36.61	36.91	
		Limit -	28	28	28	28	
		Limit +	45	45	45	45	
Standby Supply Current with PVIN = 3V	I_{PVIN_SB}	Biased	1.37	1.36	1.35	1.34	mA
		Grounded	1.37	1.36	1.36	1.36	
		Limit -	1.1	1.1	1.1	1.1	
		Limit +	1.7	1.7	1.7	1.7	
Standby Supply Current with PVIN = 18V	I_{PVIN_SB}	Biased	1.30	1.30	1.29	1.29	mA
		Grounded	1.30	1.30	1.30	1.30	
		Limit -	1.1	1.1	1.1	1.1	
		Limit +	1.4	1.4	1.4	1.4	
Shutdown Supply Current PVIN = 3V	I_{PVIN_SD}	Biased	24.19	25.31	23.70	24.09	µA
		Grounded	23.92	24.91	24.05	23.96	
		Limit -	5	5	5	5	
		Limit +	40	40	40	40	
Shutdown Supply Current PVIN = 18V	I_{PVIN_SD}	Biased	128.61	129.74	126.83	127.86	µA
		Grounded	127.90	128.10	127.41	126.49	
		Limit -	50	50	50	50	
		Limit +	190	190	190	190	
Feedback Voltage Accuracy PVIN = 3V	VFB	Biased	599.24	599.27	599.53	599.73	mV
		Grounded	599.64	599.55	599.67	599.67	
		Limit -	594	594	594	594	
		Limit +	603.5	603.5	603.5	603.5	
Feedback Voltage Accuracy PVIN = 4.5V	VFB	Biased	599.43	599.53	599.79	599.98	mV
		Grounded	599.85	599.80	599.92	599.93	
		Limit -	594	594	594	594	
		Limit +	603.5	603.5	603.5	603.5	
Feedback Voltage Accuracy PVIN = 6V	VFB	Biased	599.32	599.42	599.67	599.85	mV
		Grounded	599.76	599.70	599.82	599.83	
		Limit -	594	594	594	594	
		Limit +	603.5	603.5	603.5	603.5	
Positive Peak Current Limit PVIN = 3V	$I_{IPLIMIT1}$	Biased	5.44	5.28	4.90	4.80	A
		Grounded	5.36	5.37	5.23	5.25	
		Limit -	3.8	3.8	3.8	3.8	
		Limit +	6.4	6.4	6.4	6.4	

Table 4. Response of Key Parameters vs TID (Cont.)

Parameter	Symbol	Irradiation Condition	Pre-Rad Value	10krad(Si)	30krad(Si)	50krad(Si)	Unit
Positive Peak Current Limit PVIN = 12V	$I_{IPLIMIT1}$	Biased	5.33	5.15	4.68	4.52	A
		Grounded	5.29	5.31	5.16	5.17	
		Limit -	3.8	3.8	3.8	3.8	
		Limit +	6.3	6.3	6.3	6.3	
Positive Peak Current Limit PVIN = 18V	$I_{IPLIMIT1}$	Biased	5.30	5.12	4.67	4.53	A
		Grounded	5.27	5.29	5.16	5.17	
		Limit -	3.8	3.8	3.8	3.8	
		Limit +	6.3	6.3	6.3	6.3	
Positive Peak Current Limit PVIN = 3V	$I_{IPLIMIT2}$	Biased	6.65	6.47	6.05	5.94	A
		Grounded	6.55	6.57	6.46	6.48	
		Limit -	5	5	5	5	
		Limit +	7.5	7.5	7.5	7.5	
Positive Peak Current Limit PVIN = 12V	$I_{IPLIMIT2}$	Biased	6.50	6.27	5.77	5.57	A
		Grounded	6.46	6.48	6.36	6.38	
		Limit -	5	5	5	5	
		Limit +	7.5	7.5	7.5	7.5	
Positive Peak Current Limit PVIN = 18V	$I_{IPLIMIT2}$	Biased	6.52	6.29	5.76	5.60	A
		Grounded	6.47	6.50	6.35	6.37	
		Limit -	5	5	5	5	
		Limit +	7.5	7.5	7.5	7.5	
Negative Peak Current Limit with PVIN = 3V	$-I_{IPLIMIT}$	Biased	-4.40	-4.28	-4.17	-4.17	A
		Grounded	-4.43	-4.41	-4.36	-4.38	
		Limit -	-5.7	-5.7	-5.7	-5.7	
		Limit +	-3.7	-3.7	-3.7	-3.7	
Negative Peak Current Limit with PVIN = 12V	$-I_{IPLIMIT}$	Biased	-4.60	-4.42	-4.30	-4.29	A
		Grounded	-4.63	-4.58	-4.52	-4.53	
		Limit -	-5.7	-5.7	-5.7	-5.7	
		Limit +	-3.7	-3.7	-3.7	-3.7	
Negative Peak Current Limit with PVIN = 18V	$-I_{IPLIMIT}$	Biased	-4.55	-4.36	-4.24	-4.23	A
		Grounded	-4.58	-4.52	-4.46	-4.47	
		Limit -	-5.8	-5.8	-5.8	-5.8	
		Limit +	-3.6	-3.6	-3.6	-3.6	
Default Switching Frequency with PVIN = 3V	f_{SWd}	Biased	496.53	495.75	495.61	495.40	kHz
		Grounded	491.99	490.14	489.72	489.67	
		Limit -	450	450	450	450	
		Limit +	550	550	550	550	
Default Switching Frequency with PVIN = 12V	f_{SWd}	Biased	500.88	497.78	497.35	497.02	kHz
		Grounded	496.46	492.21	491.51	491.46	
		Limit -	450	450	450	450	
		Limit +	550	550	550	550	

Table 4. Response of Key Parameters vs TID (Cont.)

Parameter	Symbol	Irradiation Condition	Pre-Rad Value	10krad(Si)	30krad(Si)	50krad(Si)	Unit
Default Switching Frequency with PVIN = 18V	f_{SWd}	Biased	498.35	498.60	498.05	497.66	kHz
		Grounded	493.94	493.04	492.26	492.18	
		Limit -	450	450	450	450	
		Limit +	550	550	550	550	
500kHz Switching Frequency with PVIN =3V	f_{SW5}	Biased	496.55	495.78	495.64	495.42	kHz
		Grounded	492.02	490.15	489.73	489.69	
		Limit -	450	450	450	450	
		Limit +	550	550	550	550	
500kHz Switching Frequency with PVIN =12V	f_{SW5}	Biased	497.66	497.53	497.08	496.75	kHz
		Grounded	493.23	492.00	491.31	491.23	
		Limit -	450	450	450	450	
		Limit +	550	550	550	550	
500kHz Switching Frequency with PVIN =18V	f_{SW5}	Biased	498.49	498.57	498.03	497.65	kHz
		Grounded	494.06	493.05	492.26	492.14	
		Limit -	450	450	450	450	
		Limit +	550	550	550	550	
VCC Output Voltage with PVIN = 3V and IOUT = 0mA	$VOUT_{3V,\ 0mA}$	Biased	2.995	2.995	2.994	2.994	V
		Grounded	2.995	2.995	2.995	2.995	
		Limit -	2.96	2.96	2.96	2.96	
		Limit +	3	3	3	3	
VCC Output Voltage with PVIN = 3V and IOUT = 10mA	$VOUT_{3V,\ 10mA}$	Biased	2.972	2.970	2.967	2.965	V
		Grounded	2.972	2.972	2.971	2.971	
		Limit -	2.93	2.93	2.93	2.93	
		Limit +	2.98	2.98	2.98	2.98	
VCC Output Voltage with PVIN = 5V and IOUT = 0mA	$VOUT_{5V,\ 0mA}$	Biased	4.95	4.95	4.95	4.95	V
		Grounded	4.95	4.94	4.95	4.95	
		Limit -	4.83	4.83	4.83	4.83	
		Limit +	5	5	5	5	
VCC Output Voltage with PVIN = 5V and IOUT = 10mA	$VOUT_{5V,\ 10mA}$	Biased	4.94	4.94	4.94	4.94	V
		Grounded	4.94	4.94	4.94	4.94	
		Limit -	4.82	4.82	4.82	4.82	
		Limit +	5	5	5	5	
Minimum LX On-Time with PVIN = 3V	tMIN_ON	Biased	215.75	213.39	212.81	212.34	ns
		Grounded	213.17	210.63	210.01	209.76	
		Limit -	-	-	-	-	
		Limit +	260	260	260	260	
Minimum LX On-Time with PVIN = 12V	tMIN_ON	Biased	226.23	224.98	224.49	224.29	ns
		Grounded	225.44	222.17	221.79	221.82	
		Limit -	-	-	-	-	
		Limit +	260	260	260	260	

Table 4. Response of Key Parameters vs TID (Cont.)

Parameter	Symbol	Irradiation Condition	Pre-Rad Value	10krad(Si)	30krad(Si)	50krad(Si)	Unit
Minimum LX On-Time with PVIN = 18V	tMIN_ON	Biased	227.12	227.74	227.35	227.42	ns
		Grounded	228.69	225.07	224.76	224.98	
		Limit -	-	-	-	-	
		Limit +	260	260	260	260	
Minimum LX Off-Time with PVIN = 3V	tMIN_OFF	Biased	169.39	168.49	167.93	168.03	ns
		Grounded	167.34	166.28	166.02	165.48	
		Limit -	-	-	-	-	
		Limit +	210	210	210	210	
Minimum LX Off-Time with PVIN = 12V	tMIN_OFF	Biased	171.94	171.58	171.12	171.18	ns
		Grounded	169.30	168.71	168.39	167.81	
		Limit -	-	-	-	-	
		Limit +	210	210	210	210	
Minimum LX Off-Time with PVIN = 18V	tMIN_OFF	Biased	171.91	171.13	170.63	170.66	ns
		Grounded	169.28	168.36	168.07	167.51	
		Limit -	-	-	-	-	
		Limit +	210	210	210	210	
CDFP Upper FET $r_{DS(ON)}$ with PVIN = 3V	$25UPR_{DS(ON)\_3}$	Biased	80.68	85.50	92.21	92.78	mΩ
		Grounded	80.50	82.23	82.81	82.07	
		Limit -	65	65	65	65	
		Limit +	120	120	120	120	
CDFP Upper FET $r_{DS(ON)}$ with PVIN = 5.5V	$25UPR_{DS(ON)\_5}$	Biased	65.52	69.82	74.59	77.56	mΩ
		Grounded	65.05	66.28	66.54	66.86	
		Limit -	50	50	50	50	
		Limit +	105	105	105	105	
CDFP Lower FET $r_{DS(ON)}$ with PVIN = 3V	$25LWR_{DS(ON)\_3}$	Biased	32.47	32.81	34.42	29.99	mΩ
		Grounded	33.20	33.81	33.19	30.50	
		Limit -	22	22	22	22	
		Limit +	50	50	50	50	
CDFP Lower FET $r_{DS(ON)}$ with PVIN = 5.5V	$25LWR_{DS(ON)\_5}$	Biased	26.23	26.46	25.00	24.74	mΩ
		Grounded	26.17	27.05	25.49	25.29	
		Limit -	18	18	18	18	
		Limit +	40	40	40	40	

8.2 Single-Event Effects Testing

8.2.1 Introduction

The intense proton and heavy ion environment encountered in space applications can cause a variety of Single Event Effects (SEE) in electronic circuitry, including Single Event Upset (SEU), Single Event Transient (SET), Single Event Functional Interrupt (SEFI), Single Event Gate Rupture (SEGR), and Single Event Burnout (SEB). SEE can lead to system-level performance issues, including disruption, degradation, and destruction. Individual electronic components should be characterized for predictable and reliable space system operation to determine their SEE response.

8.2.2 Test Facility

SEE Testing was performed at the Texas A&M University (TAMU) Radiation Effects Facility of the Cyclotron Institute heavy ion facility. This facility is coupled to a K500 super-conducting cyclotron that can generate a wide range of particle beams with the various energy, flux, and fluence levels needed for advanced radiation testing. The Devices Under Test (DUTs) were tested in air at 40mm from the Aramica window for the ion beam. SET testing was performed on April 12, 2024, with normal incidence silver ions for an LET of 45.8MeV·cm^2/mg at the surface of the device. The LET of the ions in the active silicon layer ranged from 47.9MeV·cm^2/mg to 49.8MeV·cm^2/mg. Signals were communicated to and from the DUT test fixture through 20ft cables connecting to the control room.

8.2.3 Destructive Single Event Effects (DSEE) Results

For DSEE testing, the die temperature was 125°C.

PVIN DSEE testing was completed with the output set to 3.3V and a load that switched between 0A and 3.3A, with a switching frequency of 100Hz and a 50% duty cycle. The output LC filter comprised a 4.7µH inductor and a 150µF bulk capacitor (ESR < 30mΩ). The internal SLOPE and COMP were invoked by connecting those pins to VCC.

For the VCC DSEE testing, the VCC supply was overdriven so the internal regulator from PVIN was inactive, and the VCC current could be monitored directly. Other than PVIN being 12V, the situation was for the PVIN DSEE testing.

Testing showed that the ISL73007M did not exhibit any DSEE events on PVIN up to 18V and VCC up to 6.2V.

8.2.4 SET and SEFI Results

For SET testing, the ambient temperature was 25°C. Oscilloscopes were set to capture events during which VOUT deviated by ±36mV, which represents a ±2% deviation of the nominal output voltage, or in which PG pulled below 1V to provide an estimate of the device's susceptibility to SETs and SEFIs, respectively. The ISL73007M was tested in the two test configurations (TCs) displayed in Table 5.

Table 5. Configurations used for SET and SEFI Testing of the ISL73007M

Configuration	COMP	SLOPE	FS	L_{OUT} (µH)	C_{OUT} (µF)	V_{OUT} (V)	PVIN (V)
1	Tied to VCC	Tied to VCC	Tied to VCC	1.8	150	1.8	3
2	Tied to VCC	Tied to VCC	Tied to VCC	1.8	150	1.8	6

Table 6 summarizes the results of the testing.

Table 6. Summary of SET and SEFI results at LET = 45.8MeV·cm^2/mg

Configuration	# of DUTs	Total Fluence (ions/cm^2)	SET		SEFI	
			# of Events	σ (µm^2)	# of Events	σ (µm^2)
1	4	4.00E+07	0	2.5	0	2.5
2	4	4.00E+07	1482	3,705	0	2.5

No SEFIs were captured during any of the runs. There were no SET captures in Configuration 1. In Configuration 2, there were triggers on VOUT deviations; however, VOUT never deviated beyond ±2% of the operating voltage as shown in Figure 66. The red lines in the figure indicate the ±2% window.

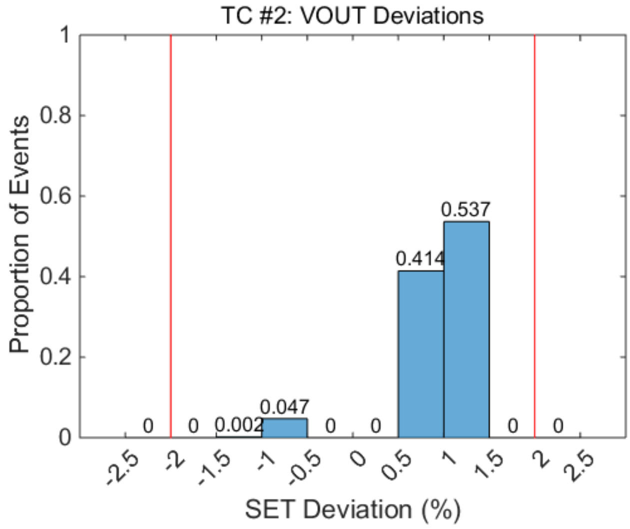


Figure 66. Test Condition #2: VOUT Deviation Size of SETs

The VOUT traces do no exhibit a well localized SET, and the LX do not show any anomalies. An example capture is shown in Figure 67. As VOUT and LX do not exhibit well localized SETs, the susceptibility of the ISL73007M to disruptive SETs is minimal.

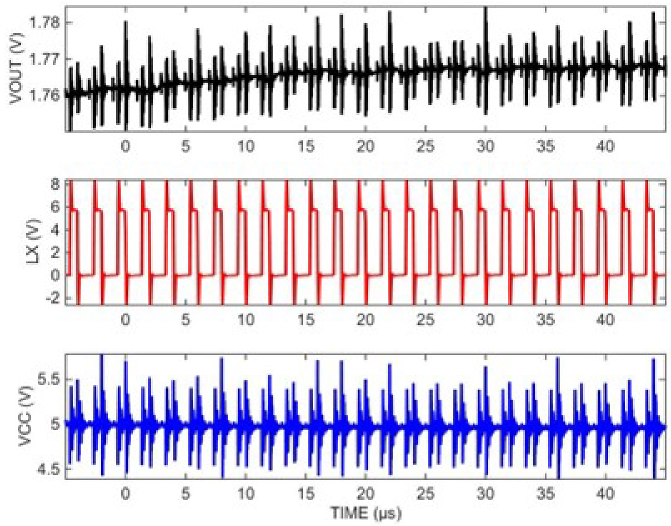


Figure 67. Typical SET Capture

8.2.5 Conclusion

Testing showed that the ISL73007M did not exhibit any DSEE events on PVIN up to 18V and VCC up to 6.2V at a die temperature of 125°C at an LET of 45.8MeV·cm^2/mg.

The ISL73007M did not exhibit any SEFIs at an LET of 45.8MeV·cm^2/mg.

The ISL73007M exhibited SETs at an LET of 45.8MeV·cm^2/mg. However, during the events, VOUT never exceeded the ±2% window, and LX do not show any anomalies. Therefore, there is low risk of the part exhibiting any disruptive SETs.

9. Package Outline Drawing

The package outline drawing is located at the end of this document and is accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

10. Ordering Information

Part Number[1][2]	Part Marking	Radiation Lot Acceptance Testing	Package Description[3] (RoHS Compliant)	Pkg. Dwg. #	Carrier Type	Temp. Range
ISL73007M30VEZ	ISL73007 MVEZ	LDR to 30krad(Si)	28 Ld HTSSOP	M28.173C	Tray	-55 to +125°C
ISL73007M30VEZ-T					Reel, 2.5k	
ISL73007M30VEZ-T7A					Reel, 250	
ISL73007M50VEZ	ISL73007 MVEZ	LDR to 50krad(Si)	28 Ld HTSSOP	M28.173C	Tray	-55 to +125°C
ISL73007M50VEZ-T					Reel, 2.5k	
ISL73007M50VEZ-T7A					Reel, 250	
ISL73007MEVAL1Z	Evaluation Board (Includes feature configuration jumpers, test points and transient load generator, optimized for 12VIN to 3.3V_{OUT} at 500kHz)					

1. These Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu-Ag plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. For Moisture Sensitivity Level (MSL), see the ISL73007M product page. For more information about MSL, see TB363.
3. For the Pb-Free Reflow Profile, see TB493.

11. Revision History

Revision	Date	Description
1.02	Jul 24, 2025	Updated Positive Peak Current maximum specification.
1.01	Jul 22, 2025	Added Output Voltage Feedback Resistors When Using SYNC section.
1.00	Jun 11, 2025	Initial release.

A. ECAD Design Information

This information supports the development of the PCB ECAD model for this device. It is intended to be used by PCB designers.

A.1 Part Number Indexing

Orderable Part Number	Number of Pins	Package Type	Package Code/POD Number
ISL73007M30VEZ	28	HTSSOP	M28.173C
ISL73007M50VEZ	28	HTSSOP	M28.173C

A.2 Symbol Pin Information

A.2.1 28-HTSSOP

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
1	PGND	Power	-
2	PGND	Power	-
3	PGND	Power	-
4	PGND	Power	-
5	PGND	Power	-
6	PGND	Power	-
7	PVIN	Power	-
8	PVIN	Power	-
9	PVIN	Power	-
10	EN	Input	-
11	VCC	Power	-
12	VCC	Power	-
13	SLOPE	Input	-
14	NC	Passive	-
15	NC	Passive	-
16	FS	Input	-
17	SYNC	Input	-
18	FB	Input	-
19	COMP	Output	-
20	SGND	Power	-
21	PG	Output	-
22	LX	Power	-
23	LX	Power	-
24	LX	Power	-
25	LX	Power	-
26	LX	Power	-
27	LX	Power	-
28	LX	Power	-
EPAD29	GND	Power	-

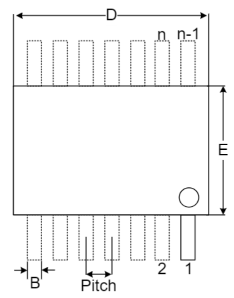
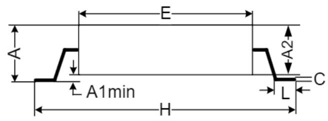
A.3 Symbol Parameters

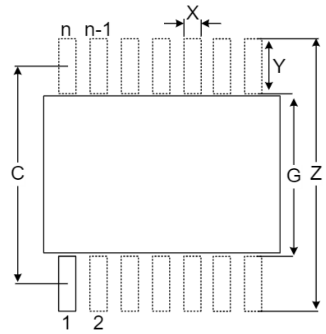
Orderable Part Number	Qualification	Radiation Qualification	RoHS	LDR	Mounting Type	Min Operating Temperature	Max Operating Temperature	Min Input Voltage	Max Input Voltage	Switching Frequency	Max Supply Current
ISL73007M30VEZ	Space	Radiation Tolerant	Compliant	30 krad(Si)	SMD	-55 °C	125 °C	3 V	18 V	1 MHz	38 mA
ISL73007M50VEZ	Space	Radiation Tolerant	Compliant	50 krad(Si)	SMD	-55 °C	125 °C	3 V	18 V	1 MHz	38 mA

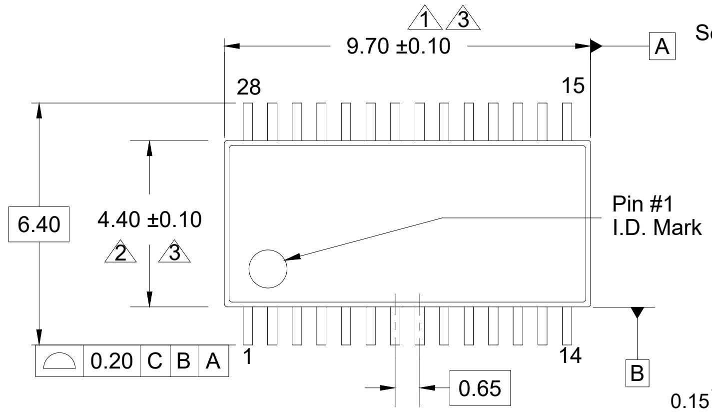
A.4 Footprint Design Information

A.4.1 28-HTSSOP

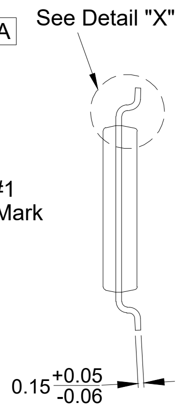
IPC Footprint Type	Package Code/ POD Number	Number of Pins
SOP	M28.173C	28

Description	Dimension	Value (mm)	Diagram
Minimum lead span	Hmin	6.20	 Bottom View
Maximum lead span	Hmax	6.60	
Minimum body span (pin1 side)	Dmin	9.60	
Maximum body span (pin1 side)	Dmax	9.80	
Minimum body span	Emin	4.30	
Maximum body span	Emax	4.50	
Minimum Lead Width	Bmin	0.19	
Maximum Lead Width	Bmax	0.30	
Minimum Lead Length	Lmin	0.45	
Maximum Lead Length	Lmax	0.75	
Maximum Height	Amax	1.20	 Side View
Minimum Standoff Height	A1min	0.05	
Minimum Lead Thickness	cmin	0.09	
Maximum Lead Thickness	cmax	0.20	
Total number of pin positions (including absent pins)	PinCount	28	
Distance between the center of any two adjacent pins	Pitch	0.65	
Minimum thermal pad size (pin1 side)	D2min	6.70	
Maximum thermal pad size (pin1 side)	D2max	6.90	
Minimum thermal pad size	E2min	2.70	
Maximum thermal pad size	E2max	2.90	

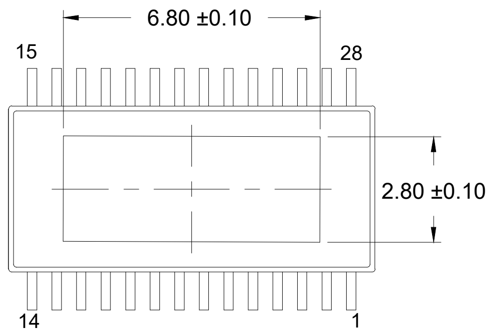
Recommended Land Pattern			
Description	**Dimension**	**Value (mm)**	**Diagram**
Distance between left pad toe to right pad toe.	Z	7.10	 PCB Top View
Distance between left pad heel to right pad heel.	G	4.2	
Row spacing. Distance between pad centers	C	5.65	
Pad Width	X	0.35	
Pad Length	Y	1.45	



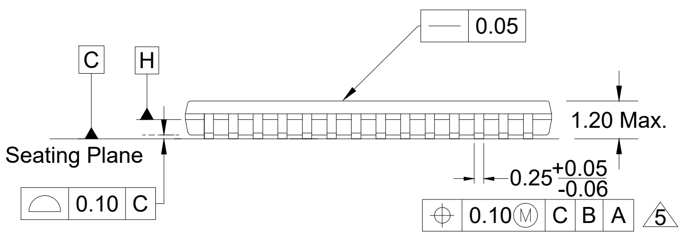
Top View



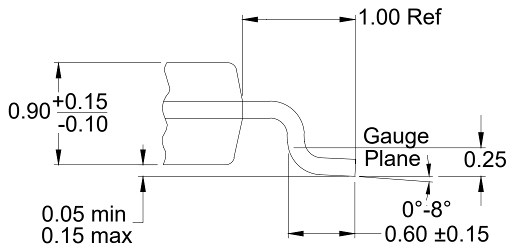
End View



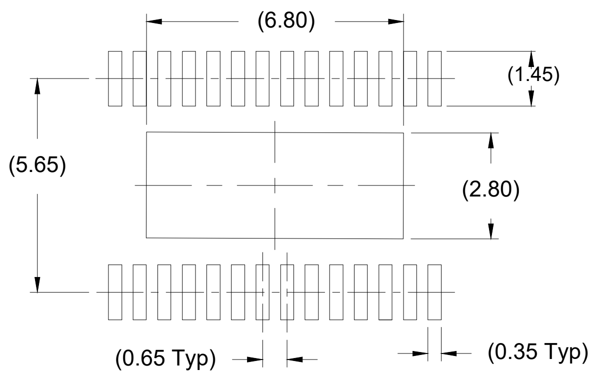
Bottom View



Side View



Detail X



Typical Recommended Land Pattern

Notes:

1. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
2. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
3. Dimensions are measured at datum plane H.

(4) Dimensioning and tolerancing per ASME Y14.5M-1994.

5. Dimension does not include dambar protrusion. Allowable protrusion shall be 0.08mm total in excess of dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm.

(6) Dimension in ( ) are for reference only.

(7) Conforms to JEDEC MO-153.

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