ISL73846M

Radiation Tolerant 2MHz Double Ended PWM Controller with Synchronous Rectification

Description

The ISL73846M is a radiation tolerant double-ended PWM controller, which can be used in high frequency switching power supplies in either voltage mode or current mode control configurations.

It features independent supplies for the control circuitry and driver output stage. The driver stage supply can be configured anywhere between 4.5V and 20V, allowing the part to drive either GaN FETs or MOSFETs directly.

The ISL73846M enables current sharing and supports synchronization to either an internal or external clock. It natively supports two-phase operation without additional ICs, while configurations requiring more than two phases can be expanded using the ISL74420M.

The ISL73846M offers enhanced design flexibility, allowing engineers to use the internal error amplifier or configure it as a buffer for custom feedback loops with an external error amplifier.

The ISL73846M is offered in a 64 Ld EP-TQFP that is fully specified across the temperature range of -55°C to +125°C.

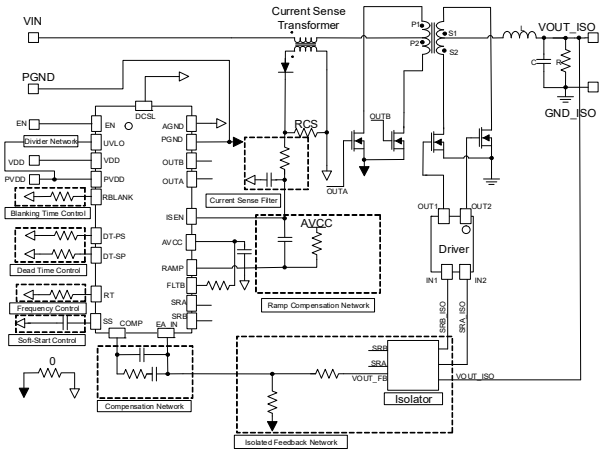


Figure 1. ISL73846 Typical Application (Push-Pull)

Features

- Qualified to Renesas Rad Tolerant Screening and QCI Flow (R34TB0004EU)
- VDD supply range 4.5V to 19V
  - Independent driver supply 4.5V to 19V
- Programmable switching frequency 20kHz to 2MHz
  - Internal or external clock source
  - Internal accuracy: ±5%
- 8MHz GBWP Error Amplifier
  - Support for external error amplifier
- Programmable UVLO
  - Low startup current <75µA for off-line power supply applications
- Max Duty Cycle Selectable (OUTA/B)
  - 50% (Out of phase)
  - 100% (Complementary)
  - 100% (In phase)
- TID Radiation Lot Acceptance Testing (RLAT) (LDR: ≤10mrad(Si)/s)
  - ISL73846M30NEZ: 30krad(Si)
  - ISL73846M50NEZ: 50krad(Si)
- SEE Characterization
  - No DSEE for VDD = 26.2V, PVDD = 19V, and AVCC = 5.8V at 46MeV•cm^2/mg
  - SEFI < 2.5µm^2 at 46MeV•cm^2/mg
  - Elongated or missing pulses only last for one pulse at 46MeV•cm^2/mg
  - VOUT SETs <2% at 46MeV•cm^2/mg

Applications

- Voltage or current mode control switching power supplies
- Power supplies with power stages using MOSFETs or GaNFETs
- Off-line isolated and non-isolated power supply

Contents

1. Overview

1.1 Block Diagram

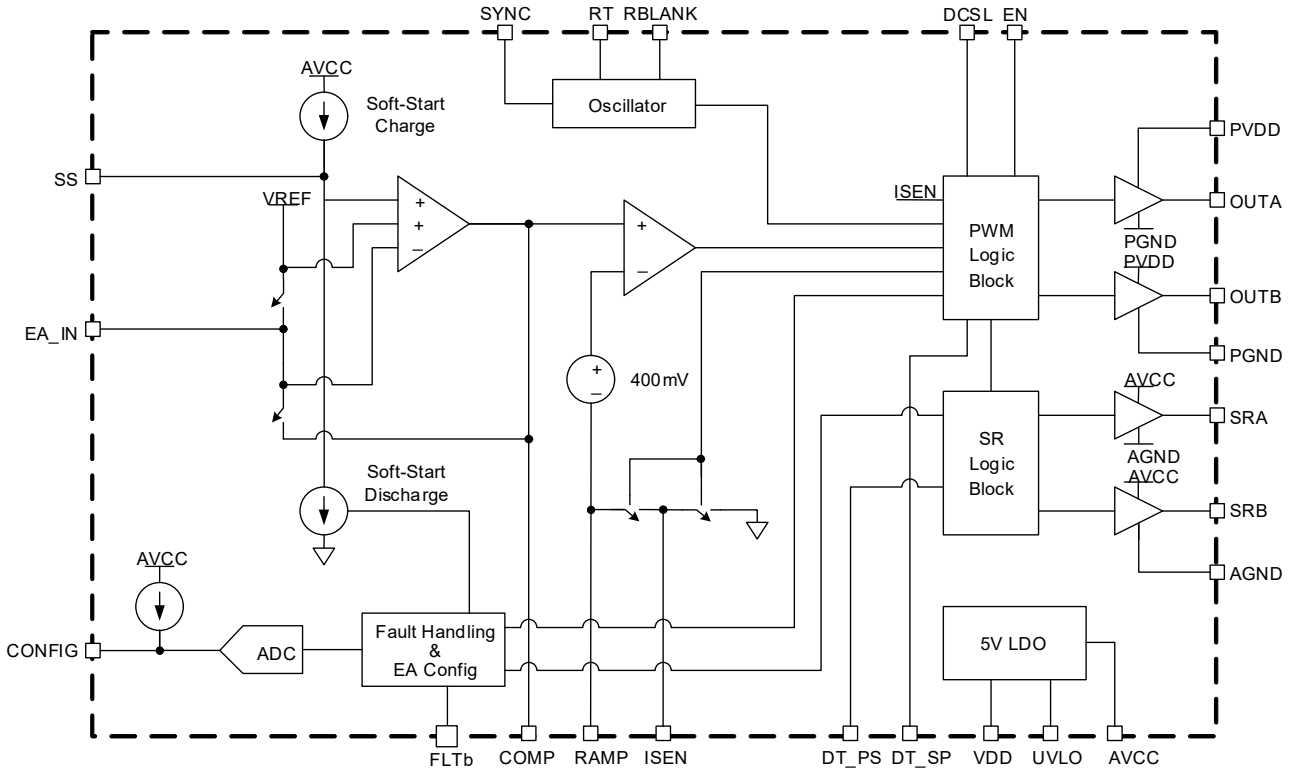


Figure 2. Block Diagram Configuration 1 (Internal Error Amplifier)

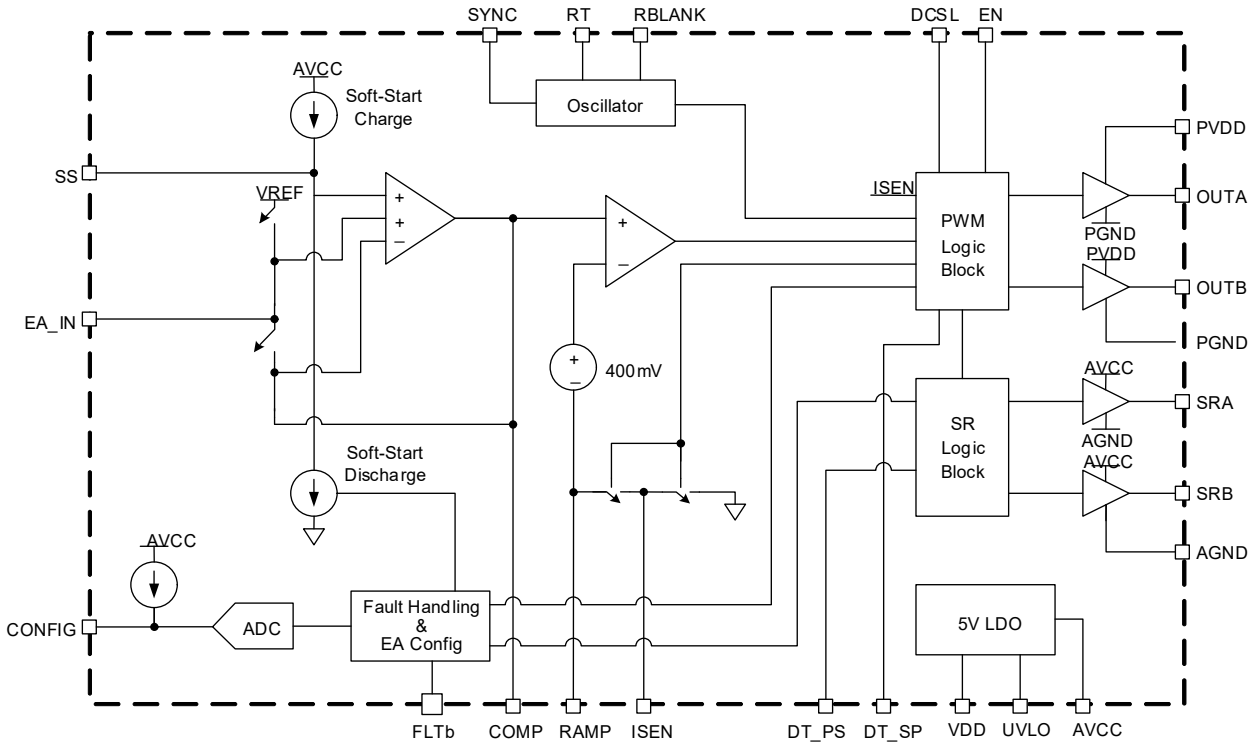


Figure 3. Block Diagram Configuration 2 (External Error Amplifier)

1.2 Typical Applications

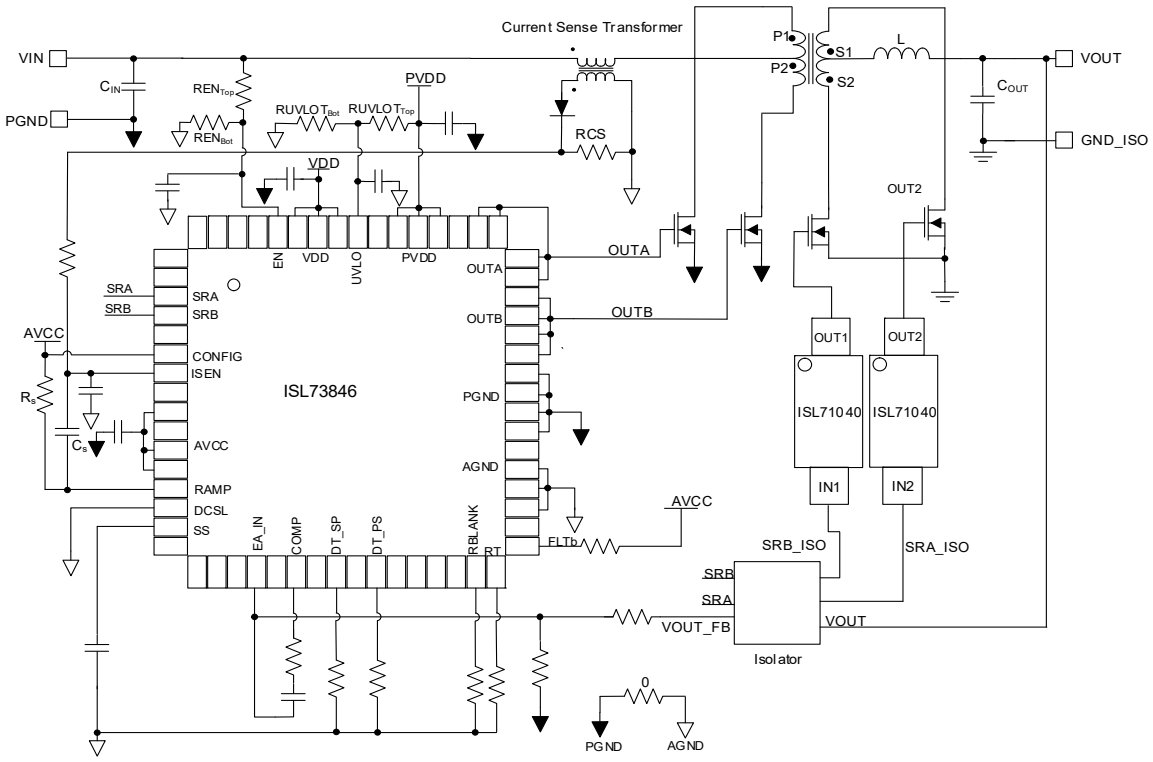


Figure 4. Push-Pull Converter with Synchronous Rectifiers

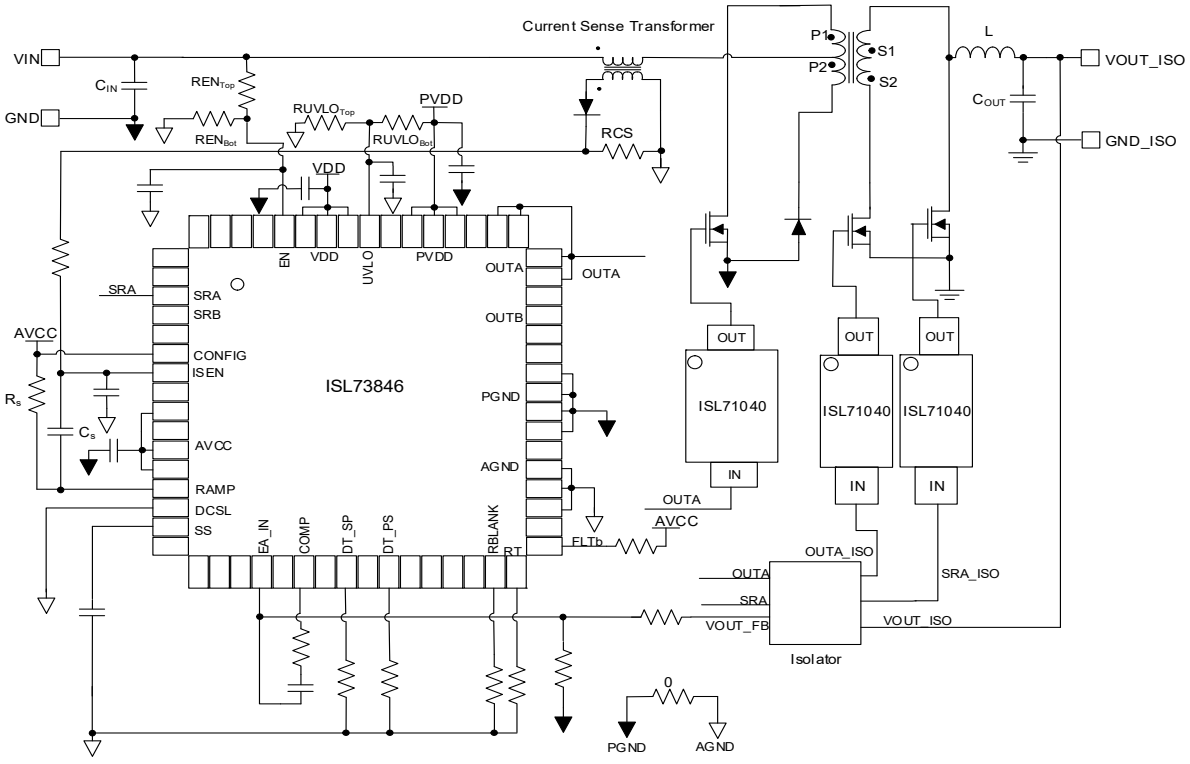


Figure 5. Forward Converter with Synchronous Rectifiers

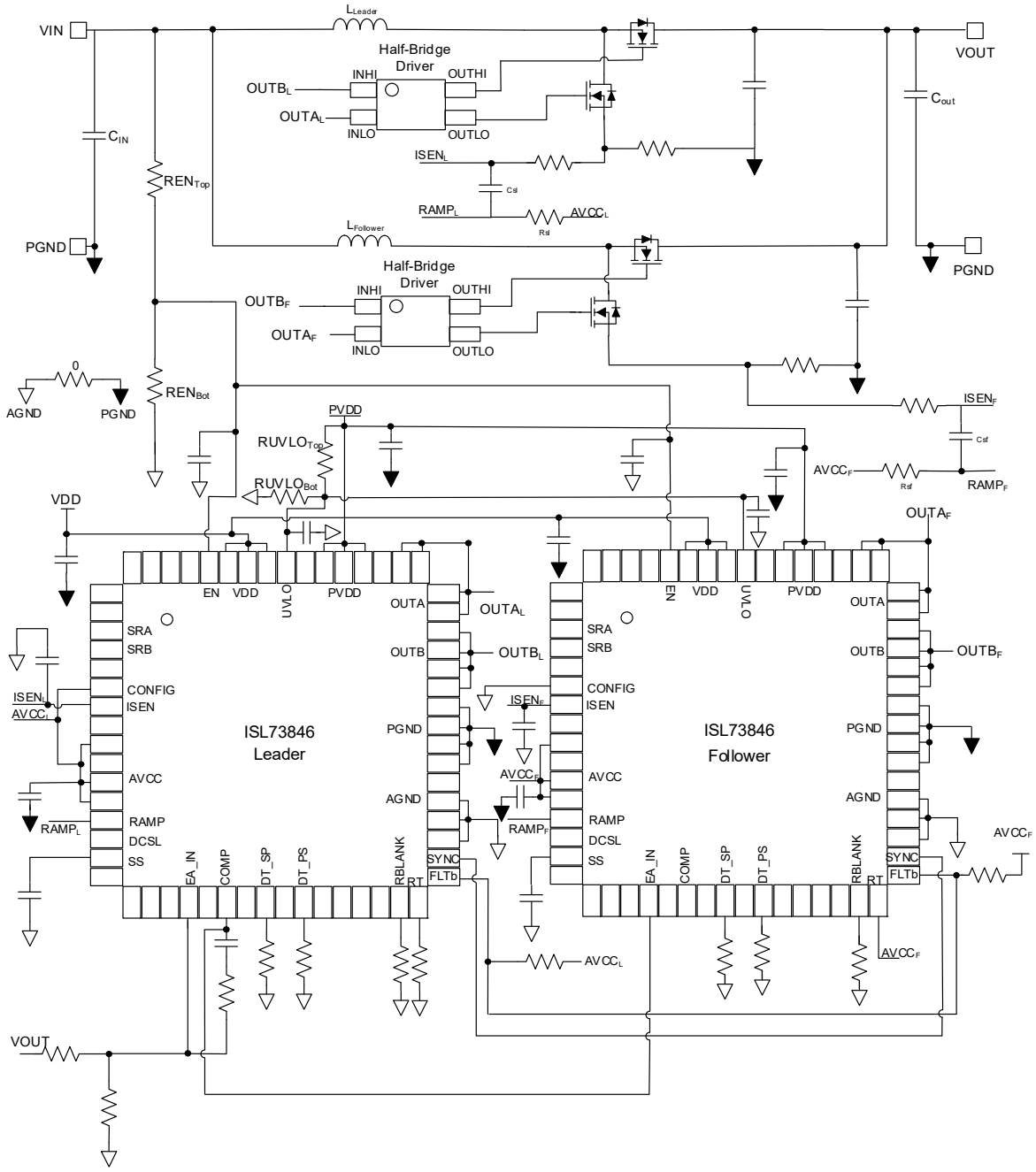


Figure 6. 2-Phase Synchronous Boost Converter

2. Pin Information

2.1 Pin Assignments

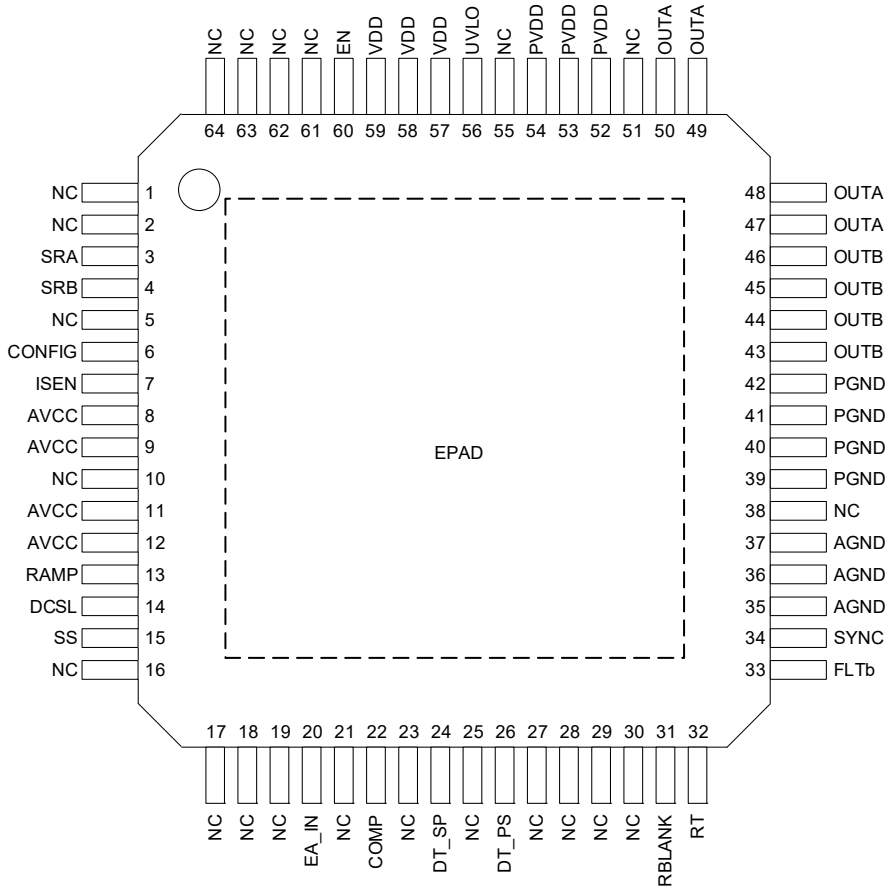
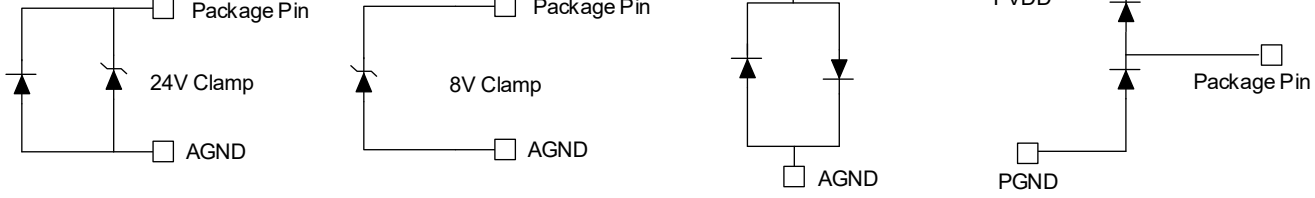


Figure 7. Pin Assignments - Top View

2.2 Pin Descriptions

Pin Number	Pin Name	ESD Circuit	Description
1, 2, 5, 10, 16, 17, 18, 19, 21, 23, 25, 27, 28, 29, 30, 38, 51, 55, 61, 62, 63, 64	NC	NA	No Connect
3	SRA	2	Synchronous rectification logic level output for OUTA.
4	SRB	2	Synchronous rectification logic level output for OUTB.
6	CONFIG	2	Configuration pin to set the overcurrent response and error amplifier configuration. Overcurrent response options are cycle-by-cycle current limit, hiccup or ignore. The error amplifier can be configured in a standard error amplifier configuration or as a buffer where an external error amplifier is preferred. Table 1 outlines the different states that are available.
7	ISEN	2	Input to the current limit comparator.
8, 9, 11, 12	AVCC	2	5V Analog supply rail generated from VDD for the internal control circuitry.
13	RAMP	2	Sawtooth input presented to the PWM comparator. For voltage mode, the R_{ff}/C_{ff} ramp is fed directly to this pin. In current mode control, the current sense information is summed with the R_s/C_s ramp and then fed to this pin.

Pin Number	Pin Name	ESD Circuit	Description
14	DCSL	2	Duty cycle select pin. ▪ DCSL = AGND: 50% duty (max); OUTA/B are out of phase ▪ DSCL = AVCC: 100% duty (max); OUTA/B are in phase ▪ DCSL = Float: 100% duty (max); OUTB is complement of OUTA
15	SS	2	Soft-start control pin. A capacitor from this pin to ground sets the soft-start interval between 2ms and 200ms according to the Equation 19.
20	EA_IN	2	Input to the error amplifier, configured with CONFIG pin.
22	COMP	2	Output of the error amplifier.
24	DT_SP	2	Secondary to Primary (SRx to OUTx) dead time control for the synchronous rectification outputs. Refer to Dead Time Control.
26	DT_PS	2	Primary to Secondary (OUTx to SRx) dead time control for the synchronous rectification outputs. Refer to Dead Time Control.
31	RBLANK	2	Minimum on and off time and leading edge blanking time control. A resistor from this pin to ground sets the timing interval.
32	RT	2	Oscillator frequency control pin. A resistor from this pin to AGND sets the switching frequency from 20kHz to 2MHz. The resistor range is between 1.07kΩ to 122kΩ. Refer to Equation 15. Tie this pin to AVCC to configure SYNC as an input. A resistor to ground configures SYNC as an output. Refer to 2-Phase Converter Operation (Leader-Follower Mode).
33	FLTb	2	Bi-directional open-drain fault input/output. Tie this pin to AVCC through10kΩ.
34	SYNC	2	Bi-directional clock pin. When RT is tied to AVCC, SYNC is configured as an input. When a resistor is present from RT to AGND, SYNC outputs the internal oscillator clock.If DCSL is tied to AVCC or left floating, the SYNC frequency is equal to OUTx frequency. If DCSL is tied to AGND, the SYNC frequency is twice the OUTx frequency.
35, 36, 37	AGND	3	Ground reference for the internal control circuitry.
39, 40, 41, 42	PGND	3	Ground reference for the OUTx drive stage circuitry and power supplies.
43, 44, 45, 46	OUTB	Self-Protecting	1.5 A sourcing and sinking driver output.
47, 48, 49, 50	OUTA	Self-Protecting	1.5 A sourcing and sinking driver output
52, 53, 54	PVDD	1	Power supply input for the driver stage circuitry.
56	UVLO	1	Undervoltage lockout input. Before the UVLO threshold is met (1.23V Typical), the part is in low power state, consuming <75µA current from VDD and PVDD.Refer to UVLO.
57, 58, 59	VDD	1	Power supply input for the control circuitry
60	EN	1	Enable control for outputs switching. Before EN threshold is met (but after UVLO pin threshold has been met), a 6µA current is sunk into the pin, which can be used with an external resistor divider to generate a hysteresis voltage. After the EN threshold of 2V is met, the OUTx and SRx outputs are enabled.
-	EPAD	-	The EPAD is connected to the die substrate. The die substrate is connected internally to AGND in the package. Solder the EPAD down to a PGND island using 25 vias on multiple layers for better thermal properties.



Circuit 1 Circuit 2 Circuit 3 Circuit 4

3. Specifications

3.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
VDD, UVLO, and EN	AGND - 0.3	AGND + 20	V
PVDD	PGND - 0.3	PGND + 0.3	V
AVCC	AGND - 0.3	AGND + 7	V
AGND - PGND	-0.3	+0.3	V
VDD[1]	AGND - 0.3	AGND + 20	V
PVDD[1]	PGND - 0.3	PGND + 19	V
AVCC[1]	AGND - 0.3	AGND + 5.8	V
Junction Temperature	-55	+150	°C
Storage Temperature	-65	+150	°C
Human Body Model (Tested per MIL-STD-883 TM3015.7)	-	2	kV
Charged Device Model (Tested per JS-002-2022)	-	1	kV
Latch-Up (Tested per JESD78E; Class 2, Level A)	-	±100	mA

1. Tested under a heavy ion environment at LET = 46MeV•cm^2/mg at +125°C (T_C) for SEB.

3.2 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
VDD, PVDD, UVLO, and EN	4.5	19	V
Switching Frequency	20	2000	kHz
Ambient Temperature	-55	+125	°C

3.3 Outgas Testing

Specification (Tested per ASTM E595, 1.5)	Value	Unit
Total Mass Loss[1]	0.05	%
Collected Volatile Condensible Material[1]	<0.01	%
Water Vapor Recovered	0.02	%

1. Outgassing results meet NASA requirements of total mass loss <1% and collected volatile condensible material <0.1%.

3.4 Thermal Specifications

Parameter	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance	64 Ld EP-TQFP Package	θ_{JA}[1]	Junction to ambient	23	°C/W
		θ_{JC}[2]	Junction to case	1.9	

1. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.
2. For θ_{JC}, the case temperature location is the center of the package underside.

3.5 Electrical Specifications

Unless otherwise noted, VDD = 4.5V, 12V, 19V, PVDD = 4.5V, 12V, 19V and C_{SS} = 33nF. **Boldface limits apply across the operating temperature range, -55°C to +125°C by characterization with production testing at +25°C; over a total ionizing dose of 30krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL73846M30NEZ); or over a total ionizing dose of 50krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL73846M50NEZ).**

Parameter	Symbol	Test Conditions	Temperature (°C)	Min	Typ[1]	Max	Unit
Supply Voltages and Currents							
Supply Voltage	VDD	-	-55 to +125	**4.5**	-	**19**	V
Drive Stage Supply Voltage	PVDD	-	-55 to +125	**4.5**	-	**19**	V
Internal Rail	AVCC	VDD = 4.5V	-55 to +125	-	4.5	-	V
		VDD = 5.5V	-55 to +125	**4.80**	4.94	**5.00**	V
		VDD = 12V	-55 to +125	**4.80**	4.94	**5.00**	V
		VDD = 19V	-55 to +125	**4.80**	4.94	**5.00**	V
AVCC Current Limit	$AVCC_{ILIM}$	UVLO = PVDD = VDD = 5V, AVCC = 4.3V	-55 to +125	**80**	107	**129**	mA
AVCC Fold-back Current Limit	$AVCC_{FBILIM}$	UVLO = PVDD = VDD = 5V, AVCC = 0V	-55 to +125	**54**	79	**100**	mA
AVCC Drop Out Voltage	$AVCC_{DO}$	VDD = 4.5V, I_{OUT} = 50mA	-55 to +125	**60**	131	**250**	mV
Startup Current	I_{QVDD}	EN = 0V, V_{UVLO} = 1.1V	-55 to +125	-	-	**75**	µA
Startup Current	I_{QPVDD}	VDD = PVDD = 12V & 19V EN = 0V, V_{UVLO} = 1.1V	-55 to +125	-	-	**1**	µA
Standby Current	$I_{STANDBY}$	EN = 1V, V_{UVLO} = 2V	-55 to +125	-	-	**7**	mA
		EN = 3V, V_{UVLO} = 2V	-55 to +125	-	-	**7**	mA
Operating Supply Current	I_{VDD}	VDD = 4.5V & 19V, f_{SW} = 20kHz, C_{LOAD} = Open OUTA, OUTB, SRA, SRB	-55 to +125	-	3.3	**4**	mA
		VDD = 4.5V & 19V, f_{SW} = 500kHz, C_{LOAD} = Open OUTA, OUTB, SRA, SRB	-55 to +125	-	7.3	**8**	mA
		VDD = 4.5V & 19V, f_{SW} = 1MHz, C_{LOAD} = Open OUTA, OUTB, SRA, SRB	-55 to +125	-	12	**14**	mA
		VDD = 4.5V & 19V, f_{SW} = 2MHz, C_{LOAD} = Open OUTA, OUTB, SRA, SRB	-55 to +125	-	20	**24**	mA
Operating Drive Stage Supply Current	I_{PVDD}	VDD = 4.5V & 19V, f_{SW} = 20kHz, C_{LOAD} = Open OUTA, OUTB, SRA, SRB	-55 to +125	-	0.6	**1.5**	mA
		VDD = 4.5V & 19V, f_{SW} = 500kHz, C_{LOAD} = Open OUTA, OUTB, SRA, SRB	-55 to +125	-	4.5	**7.0**	mA
		VDD = 4.5V & 19V, f_{SW} = 1MHz, C_{LOAD} = Open OUTA, OUTB, SRA, SRB	-55 to +125	-	8.0	**12.5**	mA
		VDD = 4.5V & 19V, f_{SW} = 2MHz, C_{LOAD} = Open OUTA, OUTB, SRA, SRB	-55 to +125	-	15.5	**25.0**	mA
Enable and Undervoltage Lockout							
Enable Pin Rising Threshold	$V_{Enable-R}$	UVLO = PVDD = VDD = 5V	-55 to +125	**1.95**	2.00	**2.09**	V

Unless otherwise noted, VDD = 4.5V, 12V, 19V, PVDD = 4.5V, 12V, 19V and C_{SS} = 33nF. **Boldface limits apply across the operating temperature range, -55°C to +125°C by characterization with production testing at +25°C; over a total ionizing dose of 30krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL73846M30NEZ); or over a total ionizing dose of 50krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL73846M50NEZ). (Cont.)**

Parameter	Symbol	Test Conditions	Temperature (°C)	Min	Typ[1]	Max	Unit
Enable Pin Hysteresis current	$I_{Enable-HYS}$	PVDD = VDD = 5V, EN = 1V, UVLO = 5V	-55 to +125	**5.00**	6	**7.00**	µA
UVLO Pin Rising Threshold	V_{UVLO-R}	EN = PVDD = VDD = 5V	-55 to +125	**1.15**	1.22	**1.29**	V
UVLO Pin Hysteresis sourcing current	$I_{UVLO-HYS}$	PVDD = VDD = 5V, UVLO = 2V	-55 to +125	**4.40**	4.8	**5.07**	µA
PVDD UVLO Rising Threshold	$V_{PVDD-UVLO-R}$	EN = UVLO = VDD = 5V	-55 to +125	**4.1**	4.2	**4.35**	V
PVDD UVLO Falling Threshold	$V_{PVDD-UVLO-F}$	EN = UVLO = VDD = 5V	-55 to +125	**3.9**	4.0	**4.15**	V
PVDD UVLO Hysteresis	$V_{PVDD-UVLO-H}$	EN = UVLO = VDD = 5V	-55 to +125	**150**	193	**235**	mV
VDD UVLO Rising Threshold	$V_{VDD-UVLO-R}$	EN = UVLO = PVDD = 5V	-55 to +125	**4.10**	4.2	**4.35**	V
VDD UVLO Falling Threshold	$V_{VDD-UVLO-F}$	EN = UVLO = PVDD = 5V	-55 to +125	**3.9**	4.0	**4.15**	V
VDD UVLO Hysteresis	$V_{VDD-UVLO-H}$	EN = UVLO = PVDD = 5V	-55 to +125	**150**	195	**235**	mV
AVCC UVLO Rising Threshold	$V_{AVCC-UVLO-R}$	EN = UVLO = PVDD = 5V	-55 to +125	**3.20**	3.70	**4.20**	V
AVCC UVLO Falling Threshold	$V_{AVCC-UVLO-F}$	EN = UVLO = PVDD = 5V	-55 to +125	**3.00**	3.50	**4.00**	V
AVCC UVLO Hysteresis	$V_{AVCC-UVLO-H}$	EN = UVLO = PVDD = 5V	-55 to +125	**74**	190	**267**	mV
Soft Start							
Soft-Start Charging Current	I_{SS}	V_{SS} = 0.3V	-55 to +125	-	10	-	µA
Soft-Start Pull-Down Resistance	$R_{SS-PULLDN}$	V_{SS} = 0.1V, FLTb = 0V	-55 to +125	**4.0**	11.0	**16.5**	Ω
Soft-Start Offset Voltage	$SS_{Voffset}$	CONFIG = 0V, EN Ramped to 5V	-55 to +125	**10**	43	**75**	mV
Oscillator							
Internal Oscillator Frequency	f_{SW}	RT = 122kΩ, VDD = 4.5V, 19V	-55 to +125	**19**	20	**21**	kHz
		RT = 4.7kΩ, VDD = 4.5V, 19V	-55 to +125	**475**	500	**525**	kHz
		RT = 2.26kΩ, VDD = 4.5V, 19V	-55 to +125	**950**	1000	**1050**	kHz
		RT = 1.07kΩ, VDD = 4.5V, 19V	-55 to +125	**1900**	2000	**2100**	kHz
SYNC Input High Level Threshold	$V_{SYNC-IH-TH}$	RT = AVCC	-55 to +125	**2.7**	3.1	**3.5**	V
SYNC Input Low Level Threshold	$V_{SYNC-IL-TH}$	RT = AVCC	-55 to +125	**1.5**	2.0	**2.3**	V
SYNC Input High Drive Voltage	$V_{SYNC-IH}$	Recommended drive voltage into SYNC pin guaranteed by $V_{SYNC-IH-TH}$	-55 to +125	**3.6**	-	-	V
SYNC Input Low Drive Voltage	$V_{SYNC-IL}$	Recommended drive voltage into SYNC pin guaranteed by $V_{SYNC-IL-TH}$	-55 to +125	-	-	**1.4**	V
SYNC Input Duty Cycle Range	$DC_{SYNC-IN}$	PVDD = VDD = UVLO = 12V EN = 5V	-55 to +125	**30**	-	**70**	%

Unless otherwise noted, VDD = 4.5V, 12V, 19V, PVDD = 4.5V, 12V, 19V and C_{SS} = 33nF. **Boldface limits apply across the operating temperature range, -55°C to +125°C by characterization with production testing at +25°C; over a total ionizing dose of 30krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL73846M30NEZ); or over a total ionizing dose of 50krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL73846M50NEZ). (Cont.)**

Parameter	Symbol	Test Conditions	Temperature (°C)	Min	Typ[1]	Max	Unit
SYNC Output High	$V_{SYNC-OH}$	VDD = 4.5V, I_{LOAD} = -500µA	-55 to +125	**4.40**	4.49	-	V
		VDD = 19V, I_{LOAD} = -500µA	-55 to +125	**4.80**	4.93	-	V
SYNC Output Low	$V_{SYNC-OL}$	I_{LOAD} = +500µA	-55 to +125	-	0.02	**0.20**	V
SYNC Output Rise Time	$t_{SYNC-OR}$	PVDD = VDD = UVLO = 12V EN = 5V C_{LOAD}=100pF	-55 to +125	-	8	**23**	ns
SYNC Output Fall Time	$t_{SYNC-OF}$	PVDD = VDD = UVLO = 12V EN = 5V C_{LOAD}=100pF	-55 to +125	-	5	**9**	ns
Voltage Reference							
Reference Voltage (Measured on COMP pin)	V_{REF}	EA_IN = COMP, CONFIG = AVCC.	-55	**592**	598	**604**	mV
		EA_IN = COMP, CONFIG = AVCC.	+25	**597**	600	**605**	mV
		EA_IN = COMP, CONFIG = AVCC.	+125	**594**	600	**606**	mV
Reference Voltage over Line (VDD)	$V_{REF-LINE}$	EA_IN = COMP, CONFIG = AVCC.	-55 to +125	**-0.7**	-	**0.7**	mV
Reference Voltage over Rad	$V_{REF-RAD}$	EA_IN = COMP, CONFIG = AVCC.	+25	**595**	601	**606**	mV
Error Amplifier							
Input Bias Current	$I_{BIAS\_EA\_IN}$	CONFIG = 0V, VCM = 0V, 2V	-55	**-10**	-	**17**	nA
			+25	**-17**	-	**17**	nA
			+125	**-50**	-	**23**	nA
		CONFIG = 0V VCM = 0V, 2V, Post Rad	+25	**-17**	-4	**17**	nA
Open Loop Gain[2]	AV_{OL-EA}	-	-55 to +125	**60**	-	-	dB
Common Mode Rejection Ratio[2]	CMRR	VCM = 0V, 2V	-55 to +125	**66**	71	**78**	dB
Gain Bandwidth Product[2]	GBWP	-	-55 to +125	**8**	13	-	MHz
Output Sink Current	I_{OL}	COMP = AVCC EA_IN = 650mV	-55 to +125	**48**	-	-	mA
Output Source Current	I_{OH}	COMP = AGND EA_IN = 580mV	-55 to +125	**35**	-	-	mA
Output High Voltage[2]	V_{OH}	I_{LOAD} = 200µA EA_IN = 550mV	-55 to +125	**AVCC-0.2**	-	-	V
Output Low Voltage	V_{OL}	I_{LOAD} = 200µA EA_IN = 650mV	-55 to +125	-	-	**AGND+20**	mV
Current Limit (ISEN)							
Current Limit Threshold	V_{CL-OC1}	-	-55 to +125	**563**	595	**625**	mV
Current Limit Delay	t_{CL-OC1}	-	-55 to +125	-	-	**161**	ns
Overcurrent Limit Threshold	V_{CL-OC2}	-	-55 to +125	**867**	901	**928**	mV
Overcurrent Limit Delay	t_{CL-OC2}	-	-55 to +125	-	-	**176**	ns

Unless otherwise noted, VDD = 4.5V, 12V, 19V, PVDD = 4.5V, 12V, 19V and C_{SS} = 33nF. **Boldface limits apply across the operating temperature range, -55°C to +125°C by characterization with production testing at +25°C; over a total ionizing dose of 30krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL73846M30NEZ); or over a total ionizing dose of 50krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL73846M50NEZ). (Cont.)**

Parameter	Symbol	Test Conditions	Temperature (°C)	Min	Typ[1]	Max	Unit
ISEN Input Bias Current	-	ISEN = 500mV	-55 to +125	**-40**	1	**40**	nA
Pulse Width Modulator (PWM) Comparator Section							
Max Duty Cycle	DC_{MAX}	DCSL = 0V, f_{SW} = 20kHz, OUTA,OUTB, R_{BLANK} = 1.05kΩ	-55 to +125	-	-	**49.95**	%
		DCSL = AVCC, f_{SW} = 20kHz, OUTA,OUTB, R_{BLANK} = 1.05kΩ	-55 to +125	-	-	**99.9**	%
		DCSL floating, f_{SW} = 20kHz, OUTA, R_{BLANK} = 1.05kΩ	-55 to +125	-	-	**99.9**	%
		DCSL = 0V, f_{SW} = 500kHz, OUTA,OUTB, R_{BLANK} = 1.05kΩ	-55 to +125	-	-	**48**	%
		DCSL = AVCC, f_{SW} = 500kHz, OUTA,OUTB, R_{BLANK} = 1.05kΩ	-55 to +125	-	-	**97**	%
		DCSL floating, f_{SW} = 500kHz, OUTA, R_{BLANK} = 1.05kΩ	-55 to +125	-	-	**97**	%
Min Duty Cycle	DC_{MIN}	DCSL floating, f_{SW} = 20kHz, OUTB, R_{BLANK} = 1.05kΩ	-55 to +125	**0.1**	-	-	%
		DCSL floating, f_{SW} = 500kHz, OUTB, R_{BLANK} = 1.05kΩ	-55 to +125	**3**	-	-	%
RAMP Offset	$RAMP_{VOS}$	VDD = PVDD = UVLO = 12V, EN = 5V, V_{COMP} = 0.5V to 2V	-55 to +125	**358**	402	**451**	mV
RAMP Input Bias Sourced Current	$I_{BIAS-RAMP}$	RAMP = 0V to 600mV	-55 to +125	**8**	10	**12**	µA
Primary and Synchronous Outputs							
Minimum On-Time	t_{MIN-ON}	R_{BLANK} = 1.05kΩ, VDD=12V	-55 to +125	**81**	109	**162**	ns
		R_{BLANK} = 10.5kΩ, VDD=12V	-55 to +125	**0.88**	1.00	**1.20**	µs
		R_{BLANK} = 105kΩ, VDD = 12V	-55 to +125	**9.55**	10.00	**10.60**	µs
Minimum Off-Time	$t_{MIN-OFF}$	R_{BLANK} = 1.05kΩ, VDD = 12V	-55 to +125	**87**	105	**123**	ns
		R_{BLANK} = 10.5kΩ, VDD = 12V	-55 to +125	**0.98**	1.00	**1.07**	µs
		R_{BLANK} = 105kΩ, VDD = 12V	-55 to +125	**9.10**	10.04	**12.15**	µs
Leading Edge Blanking Time	t_{BLANK}	R_{BLANK} = 1.05kΩ, VDD = 12V	-55 to +125	**58**	64	**71**	ns
		R_{BLANK} = 10.5kΩ, VDD = 12V	-55 to +125	**0.91**	0.97	**1.02**	µs
		R_{BLANK} = 105kΩ, VDD = 12V	-55 to +125	**9.45**	10.00	**11.10**	µs
Output Voltage High (OUTA,B)	V_{OH-OUT}	I_{LOAD} = -50mA	-55 to +125	**PVDD-0.25**	-	-	V
Output Voltage Low (OUTA,B)	V_{OL-OUT}	I_{LOAD} = +50mA	-55 to +125	-	-	**GND+250**	mV
Output Rise Time (OUTA,B)	$t_{RISE-OUT}$	C_{LOAD} = 1nF	-55 to +125	**4.65**	10	**17.40**	ns
Output Fall Time (OUTA,B)	$t_{FALL-OUT}$	C_{LOAD} = 1nF	-55 to +125	**2.2**	9.90	**17.0**	ns
SR Rise Time (SRA,B)	$t_{RISE-SR}$	C_{LOAD} = 200pF	-55 to +125	-	8	-	ns
SR Fall Time (SRA,B)	$t_{FALL-SR}$	C_{LOAD} = 200pF	-55 to +125	-	10	-	ns

Unless otherwise noted, VDD = 4.5V, 12V, 19V, PVDD = 4.5V, 12V, 19V and C_{SS} = 33nF. **Boldface limits apply across the operating temperature range, -55°C to +125°C by characterization with production testing at +25°C; over a total ionizing dose of 30krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL73846M30NEZ); or over a total ionizing dose of 50krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL73846M50NEZ). (Cont.)**

Parameter	Symbol	Test Conditions	Temperature (°C)	Min	Typ[1]	Max	Unit
Peak Switching Current (OUTA,B)[2]	$I_{OUTA/B}$	C_{LOAD} = 470nF	-55 to +125	**±1.5**	-	-	A
Output Voltage High (SRA,B)	V_{OH-SR}	PVDD = 4.5V, I_{LOAD} = -500µA	-55 to +125	**4.45**	4.48	**4.50**	V
Output Voltage High (SRA,B)	V_{OH-SR}	PVDD = 19V, I_{LOAD} = -500µA	-55 to +125	**4.80**	4.93	**5.00**	V
Output Voltage Low (SRA,B)	V_{OL-SR}	I_{LOAD} = +500µA	-55 to +125	-	9	**50**	mV
Clock to PWM Output Delay (OUTA,B)	$t_{PWM-PROP-OUT}$	PVDD = V_{VDD} = UVLO = 12V, EN = 5V SYNC to OUTA/B	-55 to +125	**99**	138	**179**	ns
CH to CH Skew	$t_{CH-CH-SKEW}$	-	-55 to +125	**-10**	1	**10**	ns
EDGE to EDGE Skew	$t_{EDGE-EDGE-SKEW}$	R_{DT} = Open or R_{DT} = AVCC	-55 to +125	**-9**	1	**8**	ns
		R_{DT} = 4kΩ	-55 to +125	**-11**	1	**10**	ns
		R_{DT} = 50kΩ	-55 to +125	**-14**	1	**15**	ns
		R_{DT} = 100kΩ	-55 to +125	**-22**	1	**21**	ns
OUTA/B Off to SRA/B On Dead Time	t_{DT-PS}	R_{DT} = Open or R_{DT} = AVCC	-55 to +125	-	4.8	-	ns
		R_{DT} = 4kΩ	-55 to +125	**14**	20	**27**	ns
		R_{DT} = 50kΩ	-55 to +125	**74**	88	**106**	ns
		R_{DT} = 100kΩ	-55 to +125	**138**	161	**203**	ns
SRA/B Off to OUTA/B On Dead Time	t_{DT-SP}	R_{DT} = Open or R_{DT} = AVCC	-55 to +125	-	6.3	-	ns
		R_{DT} = 4kΩ	-55 to +125	**12**	19.5	**29**	ns
		R_{DT} = 50kΩ	-55 to +125	**74**	87	**103**	ns
		R_{DT} = 100kΩ	-55 to +125	**138**	162	**203**	ns
Configuration and Fault Section							
Configuration Current	I_{CONFIG}	PVDD = VDD = UVLO =12V, CONFIG = 0V	-55 to +125	**18.6**	20	**21.4**	µA
Configuration 1	$V_{CONFIG1}$	-	-55 to +125	**0**	-	**0.47**	V
Configuration 2	$V_{CONFIG2}$	-	-55 to +125	**0.6**	-	**0.97**	V
Configuration 3	$V_{CONFIG3}$	-	-55 to +125	**1.1**	-	**1.47**	V
Configuration 4	$V_{CONFIG4}$	-	-55 to +125	**1.6**	-	**1.97**	V
Configuration 5	$V_{CONFIG5}$	-	-55 to +125	**2.1**	-	**2.47**	V
Configuration 6	$V_{CONFIG6}$	-	-55 to +125	**2.6**	-	**5**	V
FLTb Rising Threshold	V_{FLTb-R}	-	-55 to +125	**2.6**	3.0	**3.4**	V
FLTb Falling Threshold	V_{FLTb-F}	-	-55 to +125	**1.5**	1.9	**2.2**	V
FLTb Hysteresis	V_{FLTb-H}	-	-55 to +125	**0.8**	1.1	**1.4**	mV
FLTb Minimum Pulse	$t_{FLTb-PW-MIN}$	-	-55 to +125	**35**	-	-	ns
FLTb Reaction Time	t_{FLTb}	DCSL = 5V	-55 to +125	**84**	119	**160**	ns
FLTb Leakage	I_{FLTb}	VDD = PVDD = UVLO =12V, FLTb = 0 to 5V	-55 to +125	**-1**	-	**1**	µA
Overvoltage Rising Threshold	V_{OV-R}	-	-55 to +125	**675**	692	**706**	mV
Overvoltage Falling Threshold	V_{OV-F}	-	-55 to +125	**657**	674	**688**	mV

Unless otherwise noted, VDD = 4.5V, 12V, 19V, PVDD = 4.5V, 12V, 19V and C_{SS} = 33nF. **Boldface limits apply across the operating temperature range, -55°C to +125°C by characterization with production testing at +25°C; over a total ionizing dose of 30krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL73846M30NEZ); or over a total ionizing dose of 50krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL73846M50NEZ). (Cont.)**

Parameter	Symbol	Test Conditions	Temperature (°C)	Min	Typ[1]	Max	Unit
Overvoltage Hysteresis	V_{OV-HYS}	-	-55 to +125	**11.5**	18.1	**25**	mV
Undervoltage Rising Threshold	V_{UV-R}	-	-55 to +125	**511**	528	**542**	mV
Undervoltage Falling Threshold	V_{UV-R}	-	-55 to +125	**497**	511	**525**	mV
Undervoltage Hysteresis	V_{UV-HYS}	-	-55 to +125	**11.1**	16.8	**23**	mV
Thermal Shutdown							
Thermal Shutdown Rising	T_{OTR}	-	-	-	165	-	°C
Thermal Shutdown Falling	T_{OTF}	-	-	-	152	-	°C
Thermal Shutdown Hysteresis	T_{OT-HYS}	-	-	-	13	-	°C

1. Typical values are at 25°C and are not guaranteed.
2. Limits established by characterization and/or design analysis and are not production tested.

4. Typical Performance Graphs

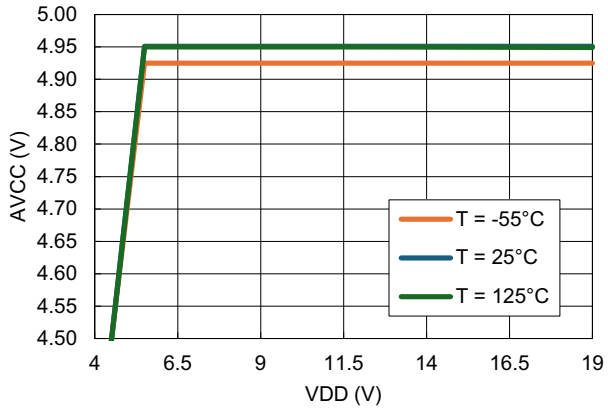


Figure 8. AVCC Voltage vs VDD with 0mA Load on AVCC at various Temperatures

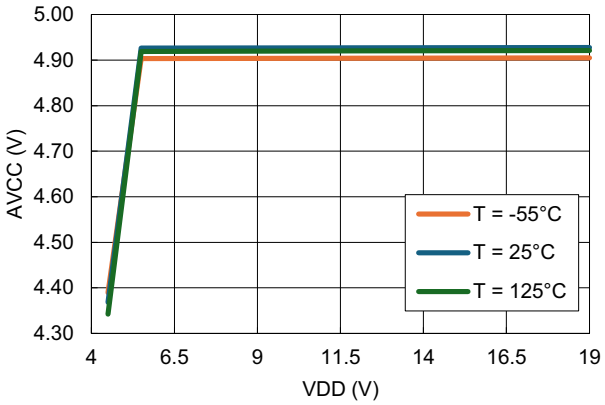


Figure 9. AVCC Voltage vs VDD with 50mA Load on AVCC at Various Temperatures

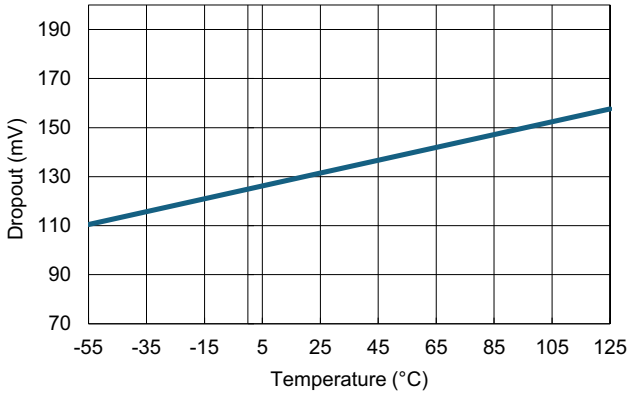


Figure 10. AVCC Dropout Voltage vs Temperature

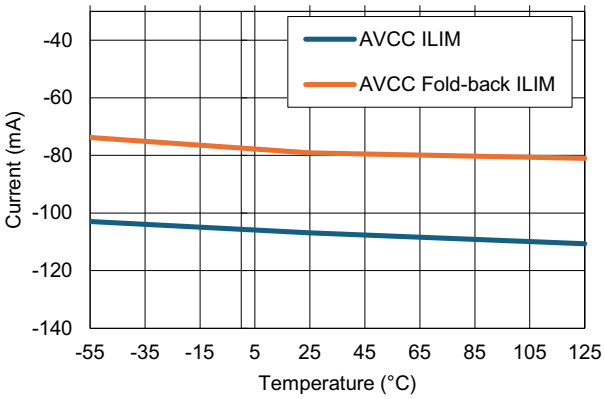


Figure 11. AVCC Current Limit and AVCC Fold-back Current Limit vs Temperature

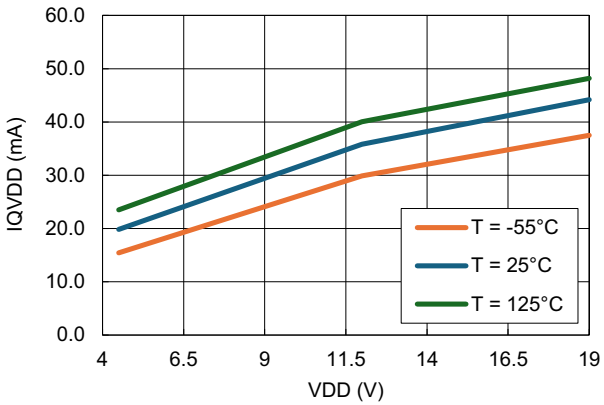


Figure 12. Startup Current IQVDD vs VDD Voltage at Various Temperatures

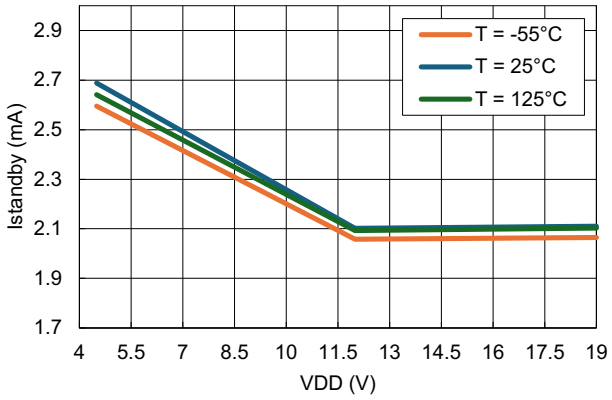


Figure 13. Standby Current vs VDD Voltage at Various Temperatures with EN < 2V, and UVLO = 2V

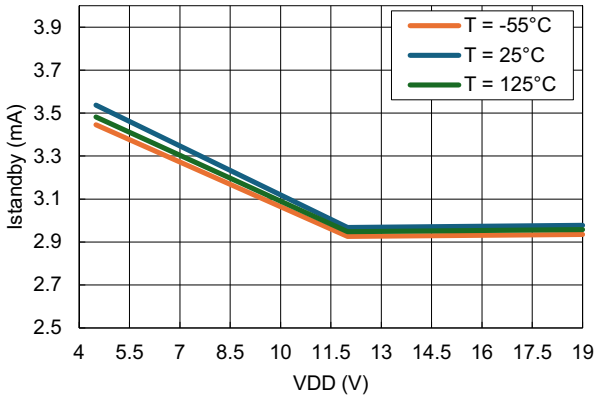


Figure 14. Standby Current vs VDD at various Temperatures with EN > 2V, and UVLO = 2V

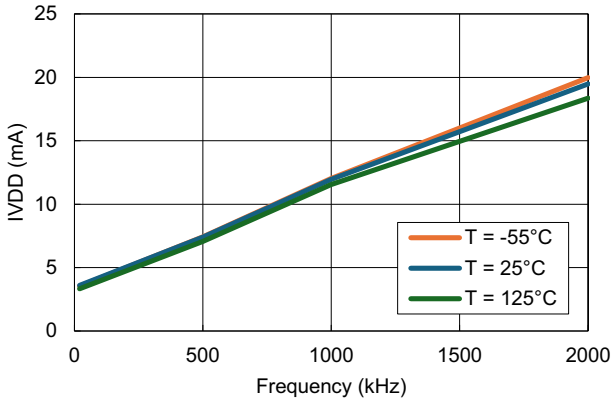


Figure 15. Operating Supply Current vs Frequency at Various Temperatures with VDD = PVDD = 4.5V

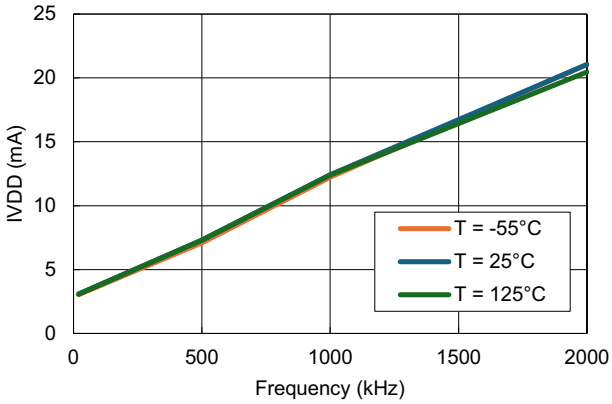


Figure 16. Operating Supply Current vs Frequency at Various Temperatures with VDD = PVDD = 19V

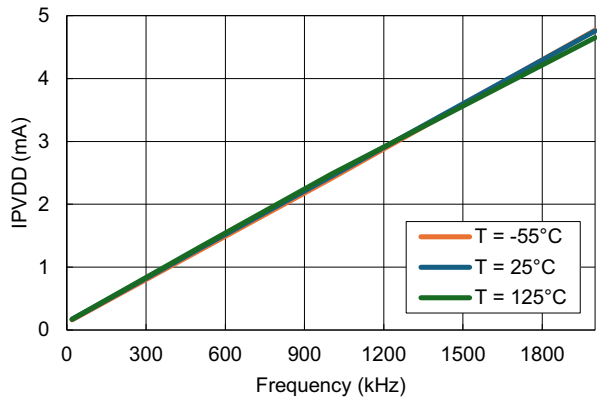


Figure 17. Operating Drive Stage Supply Current vs Frequency at Various Temperatures with VDD = 4.5V

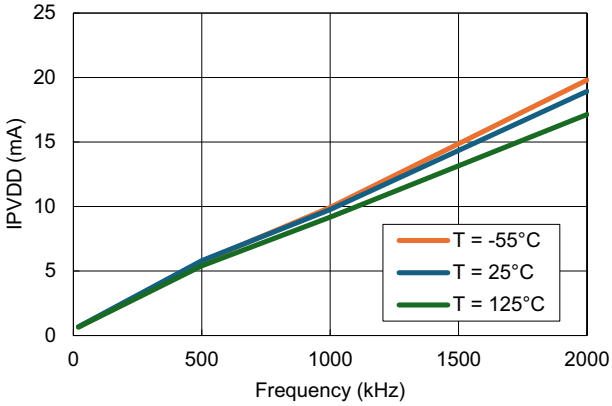


Figure 18. Operating Drive Stage Supply Current vs Frequency at Various Temperatures with VDD = 19V

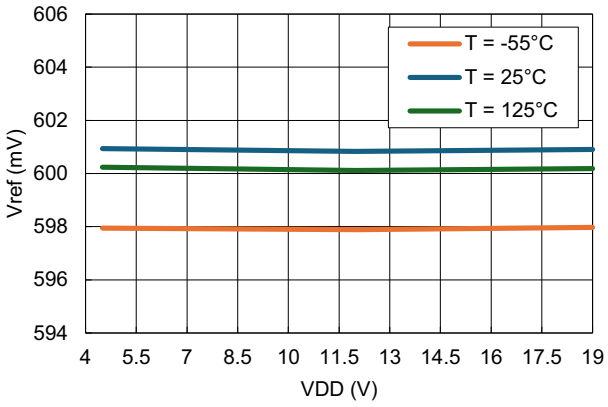


Figure 19. Reference Voltage vs VDD at Various Temperatures with EAIN = COMP

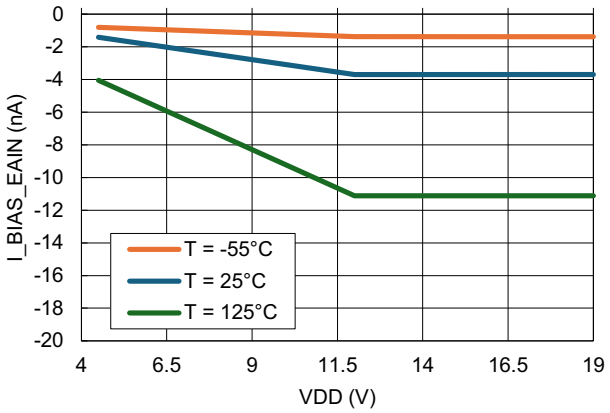


Figure 20. Error Amplifier Input Bias Current vs VDD at Various Temperatures with CONFIG = AVCC and VCM = 0V

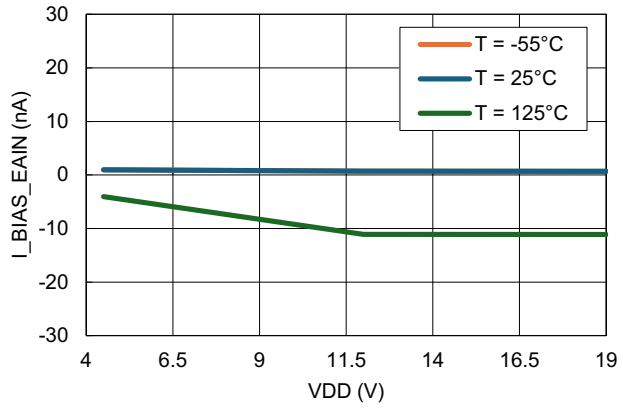


Figure 21. Error Amplifier Input Bias Current vs VDD at Various Temperatures with CONFIG = AVCC and VCM = 2V

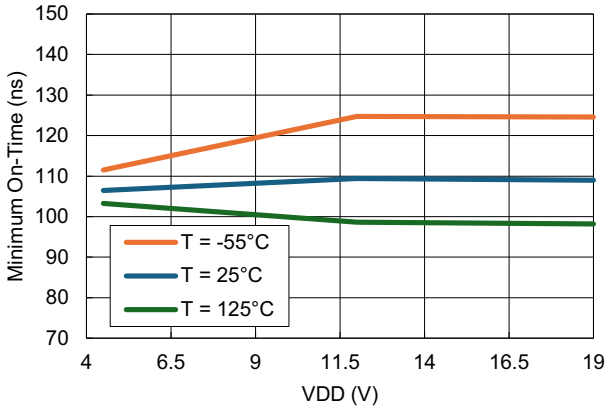


Figure 22. Minimum On-Time vs VDD at Various Temperatures with R_{BLANK} = 1.05K

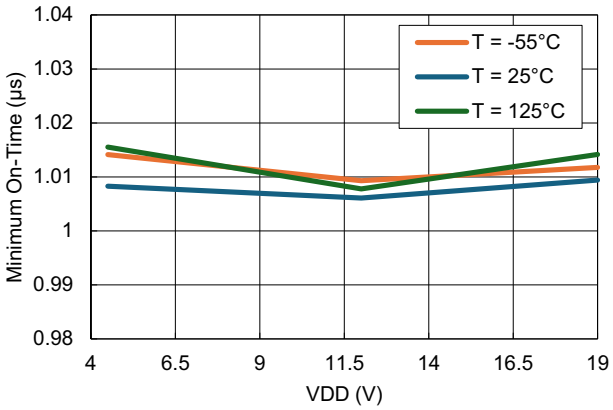


Figure 23. Minimum On-Time vs VDD at Various Temperatures with R_{BLANK} = 10.5K

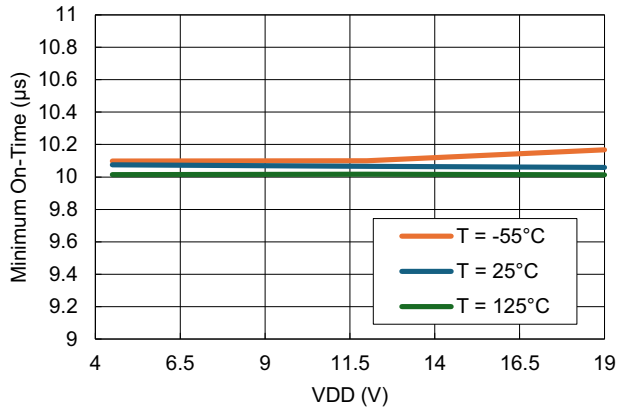


Figure 24. Minimum On-Time vs VDD at Various Temperatures with R_{BLANK} = 105K

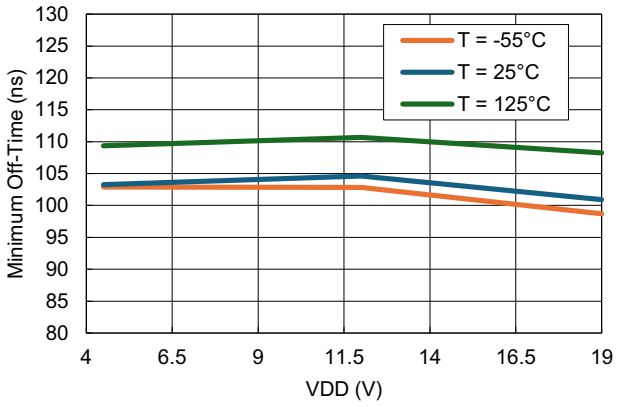


Figure 25. Minimum Off-Time vs VDD at Various Temperatures with R_{BLANK} = 1.05K

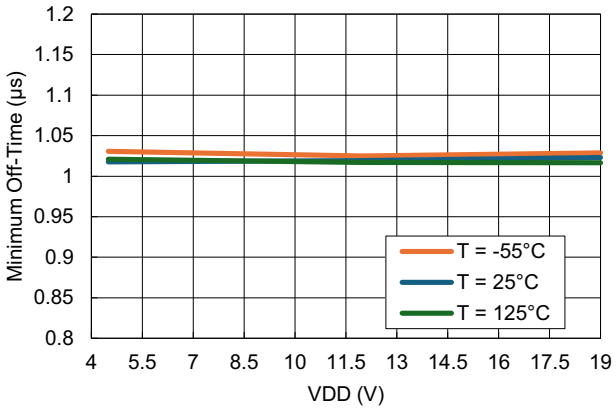


Figure 26. Minimum Off-Time vs VDD at Various Temperatures with R_{BLANK} = 10.5K

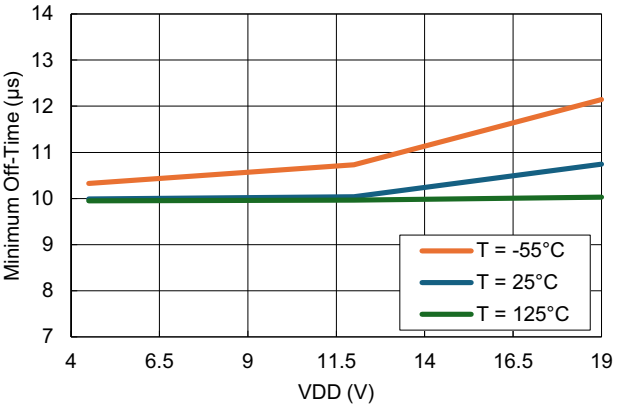


Figure 27. Minimum Off-Time vs VDD at Various Temperatures with R_{BLANK} = 105K

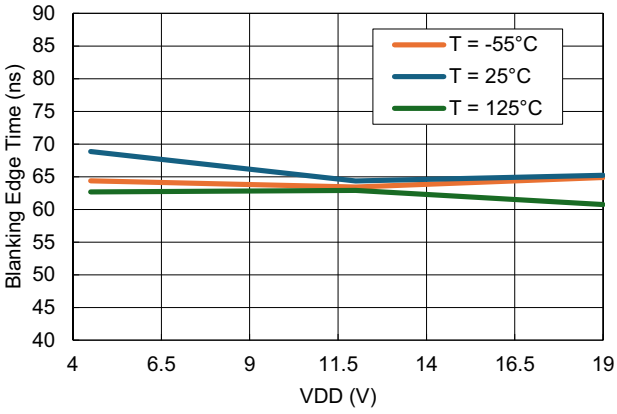


Figure 28. Leading Edge Blanking Time vs VDD at Various Temperatures with R_{BLANK} = 1.05K

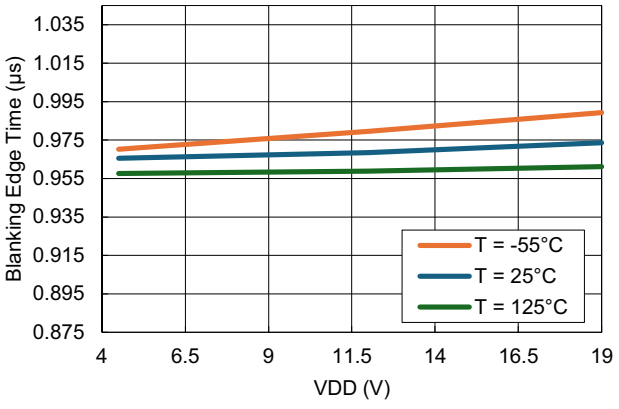


Figure 29. Leading Edge Blanking Time vs VDD at various Temperatures with R_{BLANK} = 10.5K

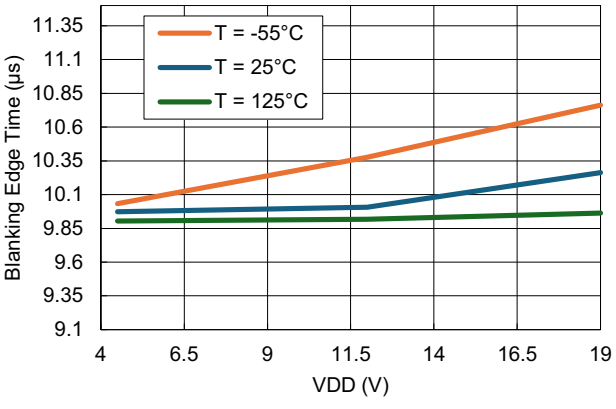


Figure 30. Leading Edge Blanking Time vs VDD at various Temperatures with R_{BLANK} = 105K

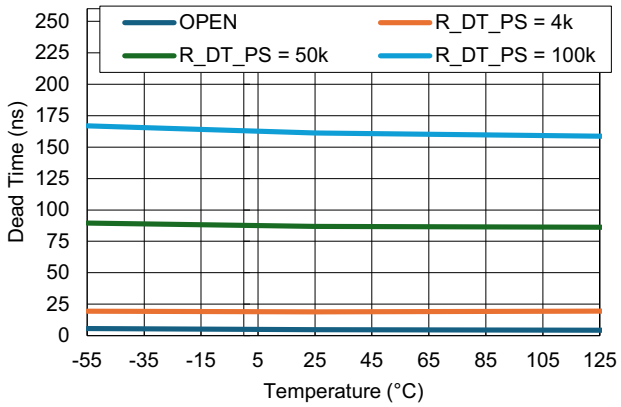


Figure 31. OUTA Falling to SRA Rising Dead Time vs Temperature at Various R_{DT_PS} Resistors with VDD = 4.5V

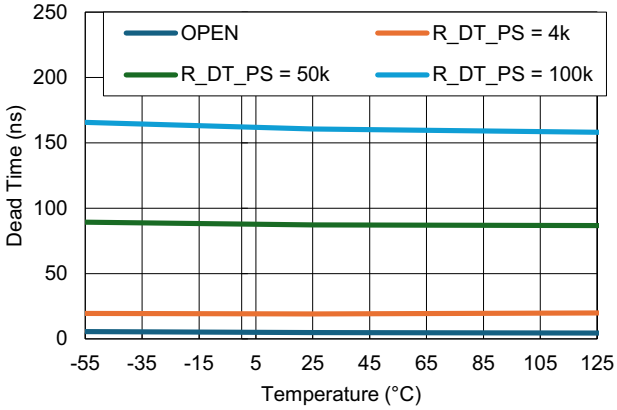


Figure 32. OUTA Falling to SRA Rising Dead Time vs Temperature at Various R_{DT_PS} Resistors with VDD = 12V

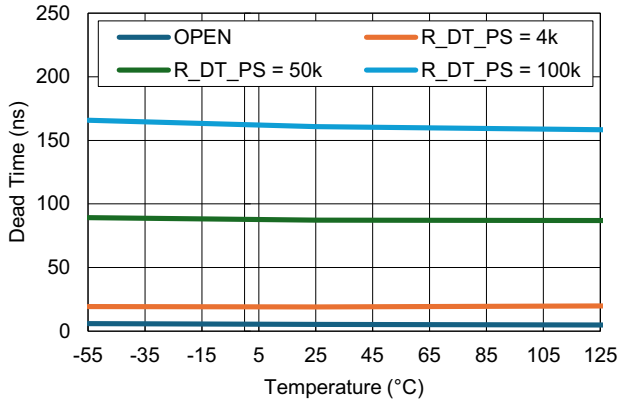


Figure 33. OUTA Falling to SRA Rising Dead Time vs Temperature at Various R_{DT_PS} Resistors with VDD = 19V

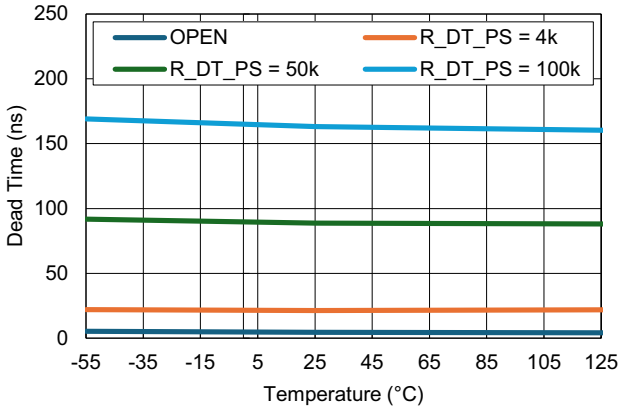


Figure 34. OUTB Falling to SRB Rising Dead Time vs Temperature at Various R_{DT_PS} Resistors with VDD = 4.5V

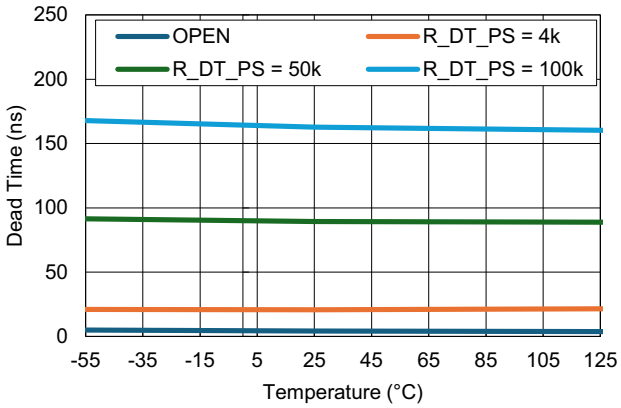


Figure 35. OUTB Falling to SRB Rising Dead Time vs Temperature at Various R_{DT_PS} Resistors with VDD = 12V

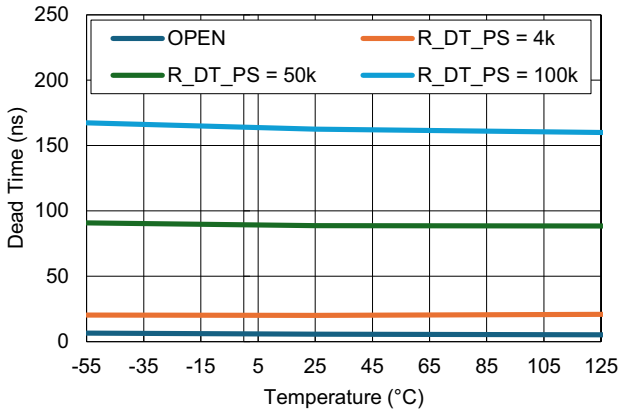


Figure 36. OUTB Falling to SRB Rising Dead Time vs Temperature at Various R_{DT_PS} Resistors with VDD = 19V

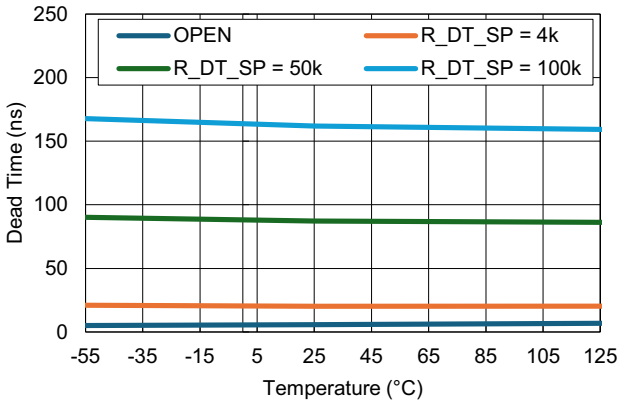


Figure 37. SRA Falling to OUTA Rising Dead Time vs Temperature at Various R_{DT_SP} Resistors with VDD = 4.5V

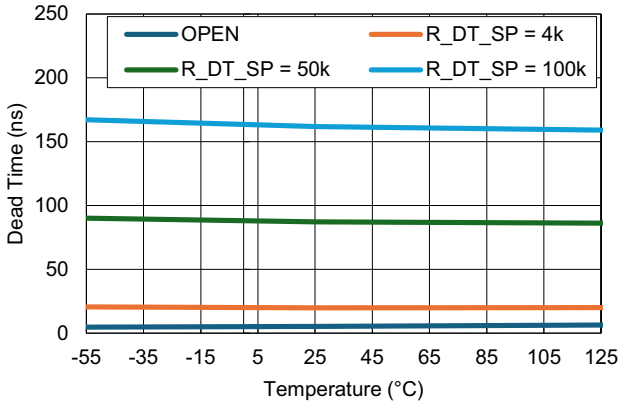


Figure 38. SRA Falling to OUTA Rising Dead Time vs Temperature at Various R_{DT_SP} Resistors with VDD = 12V

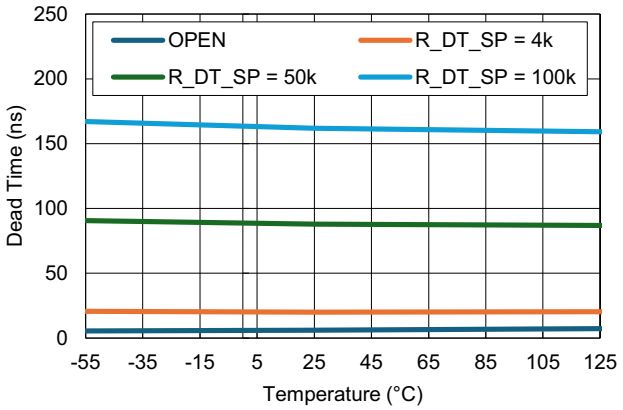


Figure 39. SRA Falling to OUTA Rising Dead Time vs Temperature at Various R_{DT_SP} Resistors with VDD = 19V

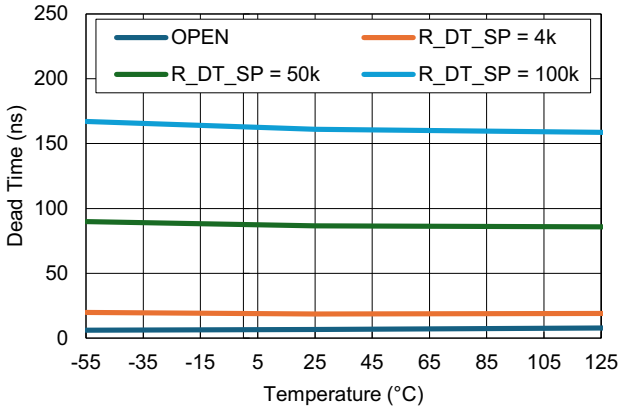


Figure 40. SRB Falling to OUTB Rising Dead Time vs Temperature at Various R_{DT_SP} Resistors with VDD = 4.5V

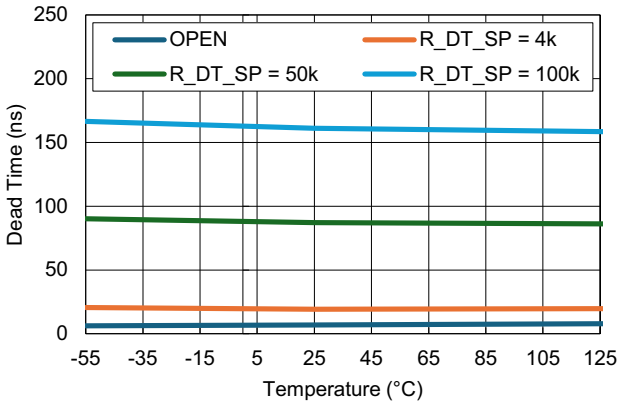


Figure 41. SRB Falling to OUTB Rising Dead Time vs Temperature at Various R_{DT_SP} Resistors with VDD = 12V

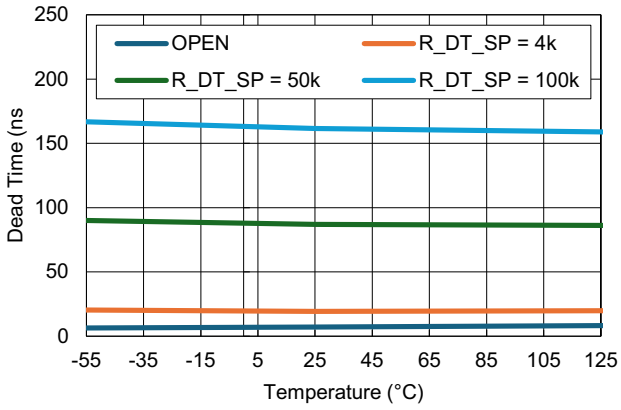


Figure 42. SRB Falling to OUTB Rising Dead Time vs Temperature at Various R_{DT_SP} Resistors with VDD = 19V

5. Functional Description

5.1 UVLO

The UVLO pin holds the ISL73846M in a low-power standby mode until the voltage presented to the UVLO pin crosses 1.22V (typical). The benefit of this feature can be seen in an off-line power supply where the ISL73846M is powered from an auxiliary winding. Maintaining a low power mode reduces the power dissipation in the startup circuit.

This pin can be tied to a resistor divider to generate a programmable hysteresis voltage with the 5µA current source that is turned on after the threshold is met. Choices for voltages to monitor can be the PVDD voltage, VDD (power supply input), or another rail that indicates when switching occurs (excluding AVCC). When the resistor divided version of the monitored rail crosses 1.22V (typical), the ISL73846M is allowed to power up and start switching provided the EN pin has met the rising threshold requirement.

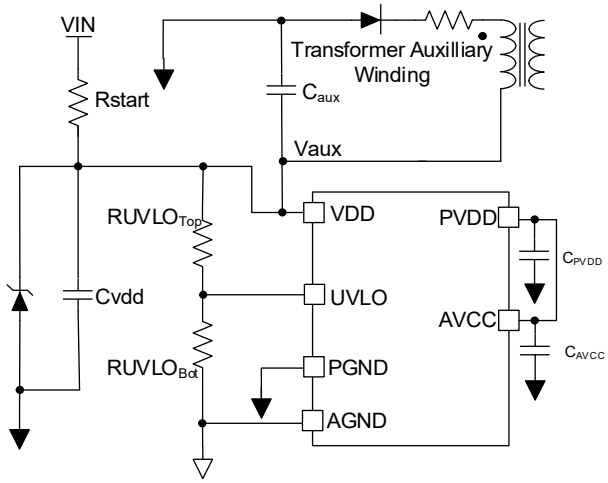


Figure 43. UVLO Pin Configuration Simplified Example Using Two External Resistors in Off-Line Startup Mode

The following are useful equations to calculate $RUVLO_{Top}$ and $RUVLO_{Bot}$ as shown in Figure 43.

VDD_R and VDD_F are the required rising and falling VDD threshold voltages

(EQ. 1) $$RUVLO_{Top} = \frac{VDD_R - VDD_F}{I_{UVLO-HYS}} \times 1000$$

(EQ. 2) $$RUVLO_{Bot} = \frac{V_{UVLO-R} \times RUVLO_{Top}}{VDD_R - V_{UVLO-R}}$$

where:

- VDD_R is the required VDD voltage where UVLO rising threshold is met in V.
- VDD_F is the required VDD voltage where UVLO falling threshold is met in V.
- $RUVLO_{Top}$ is the calculated top resistor for the UVLO voltage divider network in kΩ.
- $RUVLO_{Bot}$ is the calculated bottom resistor for the UVLO voltage divider network in kΩ.
- $I_{UVLO-HYS}$ is the UVLO hysteresis sourcing current in µA.
- V_{UVLO-R} is the UVLO pin rising threshold in V.

For example if the required VDD_R is 8V and VDD_F is 6V, $RUVLO_{Top}$= 400kΩ and $RUVLO_{Bot}$ = 81.3kΩ.

To calculate R_{start} in kΩ and C_{vdd} in µF for the off-line startup, consider the following:

- EN pin rising threshold is met.
- V_{aux} is available right after switching starts.
- I_{VDD} is the supply current of the device when the UVLO pin threshold is met.
- PVDD is tied to AVCC (5V), C_{AVCC} and C_{PVDD} are in µF.
- t_{SS} is the required soft-start time in ms.
- t_{uvlo} is the time delay from UVLO pin meeting its threshold to when the OUTx starts switching in ms.
- Q_{VDD} is the charge in µC the VDD capacitor needs to provide after the UVLO threshold is met until the part starts switching and V_{aux} is available.
- $C_{VDD,min}$ in µF is the minimum VDD capacitor required so the VDD voltage does not fall below VDD_F
- AVCC is the internal rail LDO in V.
- I_{QVDD} is the VDD pin standby current in µA.

(EQ. 3) $$t_{uvlo} \approx 2ms + t_{ss}$$

(EQ. 4) $$Q_{VDD} = AVCC \times (C_{PVDD} + C_{AVCC}) + I_{VDD} \times t_{uvlo}$$

(EQ. 5) $$Q_{VDD} = C_{VDD,\,min} \times (VDD_R - VDD_F)$$

By equating Equation 4 to Equation 5, Equation 6 is derived.

(EQ. 6) $$C_{VDD,\,min} = \frac{AVCC \times (C_{AVCC} + C_{PVDD}) + t_{uvlo} \times I_{VDD}}{VDD_R - VDD_F}$$

Note: Actual C_{VDD} capacitance required might be several times the $C_{VDD,min}$ calculated depending on time taken for V_{aux} to come up and additional power dissipation of the IC when the outputs start switching.

For adequate selection, R_{start} must be less than $R_{start,max}$ calculated in Equation 7.

(EQ. 7) $$R_{start,\,max} = \frac{VIN_{min} - VDD_R}{I_{QVDD}} \times 1000$$

5.2 Enable

The EN pin voltage is monitored and determines when the outputs start switching. When the EN voltage rises above the threshold voltage of 2.0V typical and the UVLO, VDD, and PVDD thresholds are met, the outputs start switching. The enable pin has a 6µA sinking hysteresis current that allows for the hysteresis voltage on the EN pin to be user-programmable with an external resistor divider.

Note: After the VDD and UVLO thresholds are met, the EN pin sinking current is applied before the EN pin threshold is met and released after the threshold is met to generate the hysteresis. A sinking current is used instead of a sourcing current so that if the pin is floating, it is pulled low.

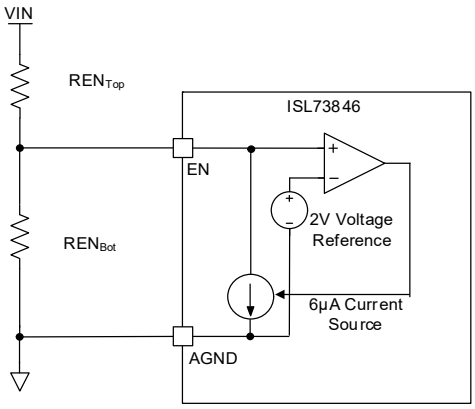


Figure 44. Example Enable Pin Configuration Using Two External Resistors

The following are useful equations to calculate REN_{Top} and REN_{Bot} from required rising and falling VIN voltage thresholds based on the example shown in Figure 44.

(EQ. 8) $$REN_{Top} = \frac{VIN_R - VIN_F}{I_{Enable-HYS}} \times 1000$$

(EQ. 9) $$REN_{Bot} = \frac{V_{Enable-R} \times REN_{Top}}{VIN_F - V_{Enable-R}}$$

Where:

- VIN_R is the required VIN voltage where EN rising threshold is met in V.
- VIN_F is the required VIN voltage where EN falling threshold is met in V.
- REN_{Top} is the calculated top resistor for the EN voltage divider network in kΩ.
- REN_{Bot} is the calculated bottom resistor for the EN voltage divider network in kΩ.
- $I_{Enable-HYS}$ is the Enable pin hysteresis sinking current in µA,
- $V_{Enable-R}$ is the Enable pin rising threshold in V.

For example, if the required VIN_R is 19V and VIN_F is 17V, REN_{Top}= 333.3 kΩ and REN_{Bot} = 44.4kΩ.

5.3 Overcurrent Response

The ISL73846M has two current limiting thresholds; current limit (OC1) when the ISEN pin reaches 600mV typical and overcurrent (OC2) when the ISEN pin reaches 900mV typical. The device can be programmed to handle OC1 and OC2 events in several ways using the CONFIG pin. The responses are summarized below.

- OC1
  - 4/8 Hiccup - The device enters Hiccup if the ISEN pin reaches the OC1 threshold during any four of the previous eight switching cycles. For example, if the ISEN pin reaches the OC1 threshold during four consecutive switching cycles, the device enters Hiccup. Or, if OC1 is not detected during four consecutive pulses but is detected four times within the previous eight switching cycles, the device enters Hiccup. OUTA and OUTB are internally monitored independently. For example, OC1 must be detected for four of the previous eight cycles on either OUTA or OUTB for the device to enter Hiccup.
  - CC - The device terminates the OUTx pulse when ISEN reaches the OC1 threshold but does not Hiccup in response to OC1 events. This allows the device to operate as a pulse-by-pulse constant current source (CC).

- Ignore - The device does not terminate OUTx pulses or enter Hiccup regardless of the voltage at the ISEN pin.

- OC2
  - 1/1 Hiccup - The device enters Hiccup when the ISEN pin reaches the OC2 threshold once.
  - Ignore - The device does not terminate OUTx pulses or enter Hiccup regardless of the voltage at the ISEN pin.

5.4 CONFIG Pin Functionality

The overcurrent response and error amplifier configuration of the ISL73846M can be controlled by the CONFIG pin. The behavior for a current limit (OC1) and Overcurrent (OC2) event can be configured using Table 1.

Table 1. Fault Behavior and Error Amp Configuration

CONFIG Pin State	Current Limit (OC1)	Overcurrent (OC2)	EA Configuration Figure 45
150kΩ to AGND	4/8 Hiccup	1/1 Hiccup	Configuration 1
114kΩ to AGND	CC	1/1 Hiccup	
87.5kΩ to AGND	Ignore	Ignore	
62.5kΩ to AGND	Ignore	Ignore	Configuration 2
37.5kΩ to AGND	CC	1/1 Hiccup	
Tied to AGND	4/8 Hiccup	1/1 Hiccup	

The error amplifier in the ISL73846M can be configured in two different ways. In configuration 1, the error amplifier is setup in a traditional configuration where the internal 600mV reference voltage is connected to the non-inverting input and the EA_IN pin is connected to the inverting input of the error amplifier. In configuration 2, the error amplifier is connected as a unity-gain buffer with the EA_IN pin connected to the input of the buffer. This configuration can be useful in applications where an external error amplifier is preferred over the internal one, such as 2-Phase Converter Operation (Leader-Follower Mode).

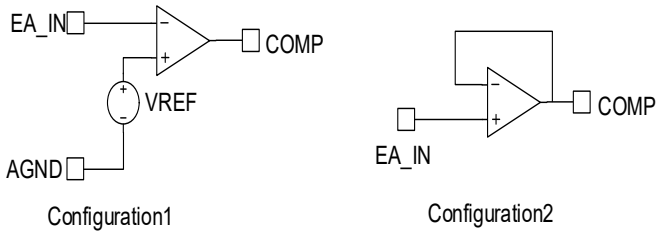


Figure 45. Error Amplifier Configuration

5.5 RAMP and ISEN Input

The RAMP pin on the ISL73846M is an input that expects a sawtooth waveform. This can be accomplished using a series RC network with the midpoint tied to the RAMP pin as shown in Figure 46. The CS/CFF capacitor is discharged on the rising edge of the clock.

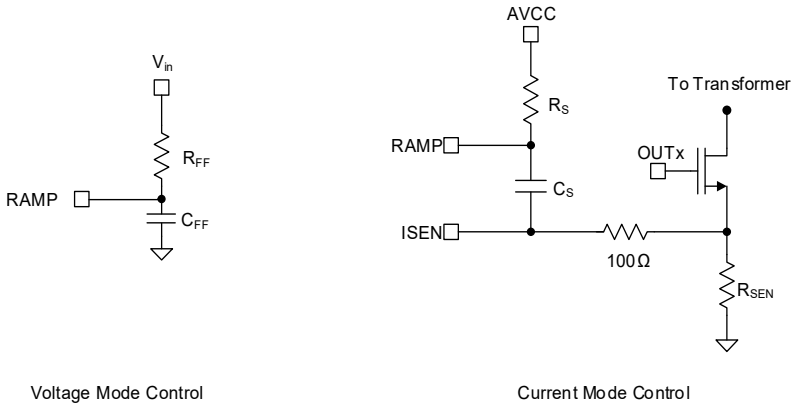


Figure 46. Voltage Mode vs Current Mode Setup

Use Equation 10 to calculate the modulator gain of $1/VRAMP_{max}$ for voltage mode control.

- V_{in} is the input voltage of the converter in V.
- f_{sw} is the converter switching frequency in kHz.
- C_{FF} is the ramp capacitor in nF.
- R_{FF} is the ramp resistor in kΩ.

Note: The ramp is reset on the falling edge of OUTx.

(EQ. 10) $$VRAMP_{max} = \frac{V_{in}}{f_{SW} \times C_{FF} \times R_{FF}}$$

Use Equation 11 through Equation 13 for current mode control considering the following:

- m_2 is the required artificial ramp slope in A/µs.

Note: Renesas recommends setting the slope compensation equal to the falling slope of the inductor current, for example for a buck converter take $m2 = V_{out}/L$.

- Cs is the ramp capacitor in nF. As a general rule, select this capacitance to be 10x the ISEN pin Filter capacitance. For example if C_{filter} is 100 pF, Cs should be 1nF.
- R_{sens} is the current sensing resistor in Ω.

Note: Renesas recommends placing R_{sens} in the primary side of the transformer windings in isolated topologies.

- dV_c/ dt in mV / µs is the rate of change of the Voltage across C_S and dV_{sens} /dt in mV / µs is the rate of change of the sensed voltage across R_{sens}. The two are set equal.
- I_C is the ramp capacitor (C_S) charging current in µA.
- AVCC = 5V(internal supply rail).
- R_S is calculated in kΩ Equation 13.

(EQ. 11) $$\frac{dv_{sens}}{dt} = m_2 \times R_{sens}$$

(EQ. 12) $$I_C = \frac{dV_C}{dt} \times C_S = m_2 \times R_{sens} \times C_S$$

(EQ. 13) $$R_S \approx \frac{AVCC \times 10^3}{I_C}$$

5.6 Dead Time Control

Dead time between OUTx and SRx can be controlled by placing a resistor from DT_PS and DT_SP to AGND. The resistor value range is between 4kΩ to 100kΩ. Use Equation 14 to achieve a specific dead time, where t_{DT} is the required dead time in ns and R_{DT} is the dead time setting resistor in kΩ.

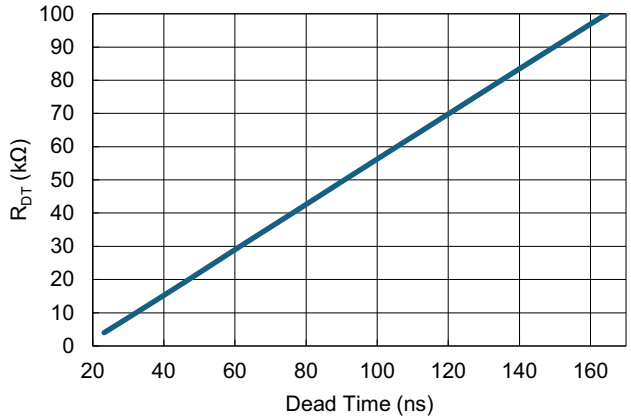


Figure 47. R_{DT} vs Dead Time

(EQ. 14) $$R_{DT} = 0.68 \times t_{DT} - 11.829$$

It is also possible to leave DT_PS and DT_SP either floating or tied to AVCC for a minimum dead time of 5ns for the respective edges. DT_PS controls the dead time from OUTx falling to SRx rising. DT_SP controls the dead time from SRx falling to OUTx rising.

The following summarizes the dead time control configuration. Refer to Table 2 for more details.

- RDT_PS, RDT_SP pins with resistor to ground – Dead time between OUTx and SRx controlled by resistor setting. SRx outputs are enabled after the SS pin reaches 900mV during startup.
- RDT_PS, RDT_SP pins tied to AVCC – If either the DT_PS or DT_SP pin is tied to AVCC, the SRx outputs are enabled at the beginning of soft-start. The minimum dead time (5ns typical) is applied to the corresponding edge of the dead time pin that is tied to AVCC. The SRx outputs are enabled after the first OUTx pulse at startup. *Note*: The user must generate dead time on their own using drivers capable of dead time control.
- RDT_PS, RDT_SP pins left floating – The minimum dead time (5ns typical) is applied to the corresponding edge of the dead time pin that is left floating. SRx outputs are enabled after the SS pin reaches 900mV during startup.

In all cases, after the SR outputs are enabled, the part keeps the SR outputs pulled down until the first OUTA or OUTB pulse, which is essential for pre-biased startup.

Table 2. DT Pin Settings, SR Enabling, and Associated Converter Topologies

Case	RDT_PS	RDT_SP	DT_PS	DT_SP	SRx Enable
1	R1 to GND	R2 to GND	Dead time programmed by R1	Dead time programmed by R2	After SS pin reaches 900mV
2	R1 to GND	Floating	Dead time programmed by R1	5ns	After SS pin reaches 900mV
3	Floating	R2 to GND	5ns	Dead time programmed by R2	After SS pin reaches 900mV

Table 2. DT Pin Settings, SR Enabling, and Associated Converter Topologies (Cont.)

Case	RDT_PS	RDT_SP	DT_PS	DT_SP	SRx Enable
4	Floating	Floating	5ns	5ns	After SS pin reaches 900mV
5	Tied to AVCC	R2 to GND	5ns	Dead time programmed by R2	Beginning of SS
6	Tied to AVCC	Floating	5ns	5ns	Beginning of SS
7	Floating	Tied to AVCC	5ns	5ns	Beginning of SS
8	Tied to AVCC	Tied to AVCC	5ns	5ns	Beginning of SS

5.7 Switching Frequency and Blanking Time

The switching frequency (f_{SW}) can be set by placing a resistor between RT and AGND. Figure 48 shows the relationship between R_T and f_{SW}.

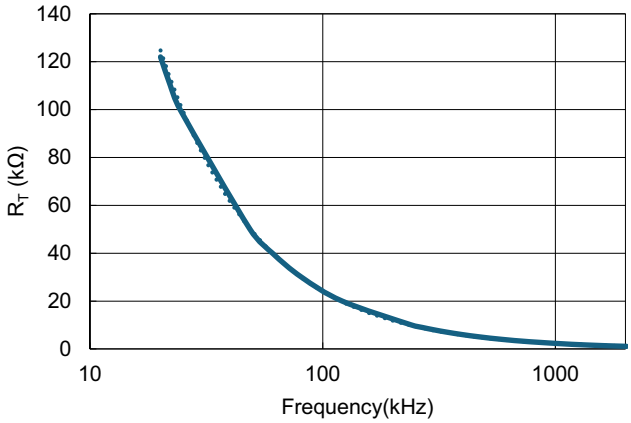


Figure 48. R_T vs Switching Frequency

Equation 15 is associated with Figure 48.

(EQ. 15) $$R_T = \frac{2447.3}{f_{sw}} - 0.1651$$

where

- f_{SW} is the oscillator switching frequency in kHz.
- R_T is the resistor value required in kΩ to achieve the required f_{SW}.

The RBLANK pin is responsible for programming minimum on-time, minimum off-time, and blanking time by placing a resistor between the RBLANK pin and AGND.

Use Equation 16 to determine the R_{BLANK} resistance value

(EQ. 16) $$R_{BLANK} = \frac{1.05 \times t_{MIN\_ON} - 1.9}{100}$$

where:

- t_{MIN_ON} is the required minimum on time in ns, which is equal to the minimum off time t_{MIN_OFF}.
- R_{BLANK} is the calculated resistor value in kΩ required to achieve the required t_{MIN_ON}.

The blanking time is the amount of time that the ISL73846M ignores faults related to the current sense feedback. A fault can be either a current limit fault or overcurrent fault. A current limit fault is when the V_{CL-LIM} threshold is

met four times in an 8-clock cycle window. An overcurrent fault is when the V_{CL-OC} is met in one clock cycle. The ISL73846M ignores both faults for the duration of the blanking time.

Use Equation 17 to estimate the blanking time where t_{BLANK} is the estimated blanking time in ns.

(EQ. 17) $$t_{BLANK} \approx t_{MIN\_ON} - 45ns$$

5.8 Soft Start

Soft-start time can be controlled by placing a capacitor between SS pin and AGND. Use Equation 18 to determine the soft-start capacitor value.The maximum programmable soft-start time is 120ms, which equates to a maximum capacitance value of 2.0µF.

(EQ. 18) $$C_{SS} = \frac{I_{SS} \times t_{SS}}{V_{ref}}$$

where:

- C_{SS} is the capacitor value in nanofarads (nF) required to achieve the required t_{SS}.
- t_{SS} is the required soft-start time (for SS pin to reach 600mV) in microseconds (µs).
- V_{ref} is the error amplifier voltage reference of 600mV.
- I_{SS} is the soft start pin charging current of 10µA.

Equation 18 can be further simplified into Equation 19.

(EQ. 19) $$C_{SS} = \frac{t_{SS}}{60}$$

5.9 FLTb

FLTb is a bidirectional open-drain pin that indicates the fault status of the ISL73846M. FLTb is low during startup and if a fault is encountered. FLTb is high after the EN threshold (2V typ) is met and if no faults are detected. Tie this pin to AVCC using a 10kΩ resistor.

5.10 Fault Response/HICCUP

If a fault is detected before switching is enabled, the FLTb pin is held low and OUTx and SRx outputs do not proceed to switching until the fault has been removed. If a fault is detected while the device is switching, the FLTb pin pulls low and the device enters hiccup. A fault can be detected at any point, with the exception of an undervoltage fault (UVFLT), which can only be detected after the SS voltage has surpassed 900mV.

The ISL73846M enters hiccup when a fault is detected. During hiccup, the OUTx and SRx outputs are pulled low and the SS pin voltage is discharged through an internal pull-down resistor ($R_{SS-PULLDN}$) for a period of 100µs. During this 100µs, the V_{SS} voltage decays with an RC time constant formed by C_{SS} and $R_{SS-PULLDN}$. When this period is complete, the SS pin sources a 10µA current, which charges the external SS capacitor until it reaches 900mV then discharges to GND. If a fault is no longer detected after the hiccup cycle, the device goes through a regular soft-start cycle.

The duration of the hiccup cycle is determined by the external SS capacitor and is calculated using Equation 20.

(EQ. 20) $$t_{HICCUP} = \frac{C_{SS} \times (900mV - V_{start})}{1000 \times I_{ss}}$$

where:

- C_{SS} is the capacitor value in nanofarads (F) required to achieve the required t_{SS}.
- I_{SS} is the soft start pin charging current of 10µA.

- V_{start} is the voltage of the SS pin after 100 µs discharge in mV.
- t_{HICCUP} is the calculated hiccup retry delay in ms.

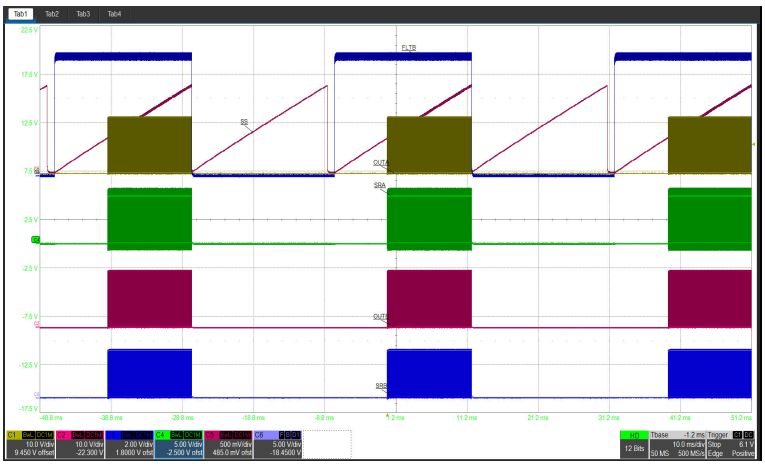


Figure 49. HICCUP Due to UV Fault

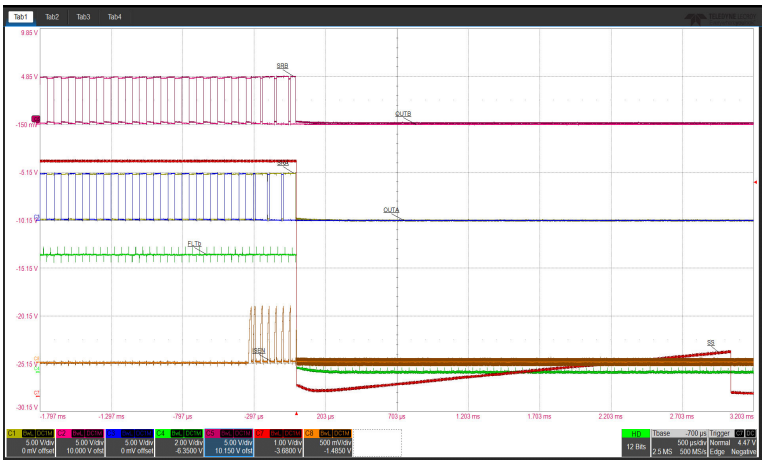


Figure 50. HICCUP Due to OC1 Fault

5.11 Duty Cycle Select

The DCSL pin configures the maximum duty cycle limit and phase of the outputs. Table 3 shows how to terminate the DCSL pin to change the maximum duty cycle and phase between OUTA and OUTB.

Table 3. Output Duty Cycle and Phase Control

DCSL State	Max Duty Cycle	Description
AGND	50%	OUTA and OUTB are 180° out of phase
Float	100%	OUTA and OUTB are complementary
AVCC	100%	OUTA and OUTB are identical and in phase

When the DCSL pin is low (Refer to Figure 51), OUTA and OUTB are completely non-overlapping. SRA, SRB are inverted versions of OUTA and OUTB (they have an overlap). Dead time between OUTx and SRx is controlled by the resistor setting.

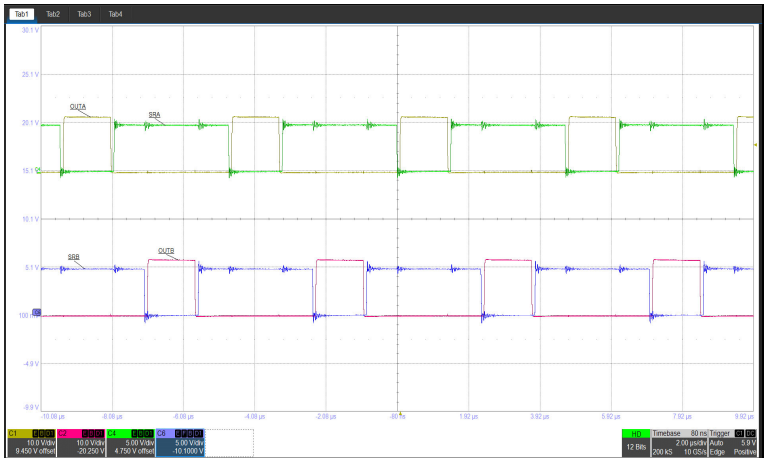


Figure 51. DCSL Tied to Ground PWM Outputs Waveforms

When the DCSL pin is floating (Refer to Figure 52), OUTB is inverted version of OUTA. Dead time between OUTA and OUTB is programmable. SRA is inverted OUTA with dead time. SRB is inverted OUTB with dead time. Essentially when SRx outputs are enabled, OUTA = SRB and OUTB = SRA (except for the voltage levels and drive strengths).

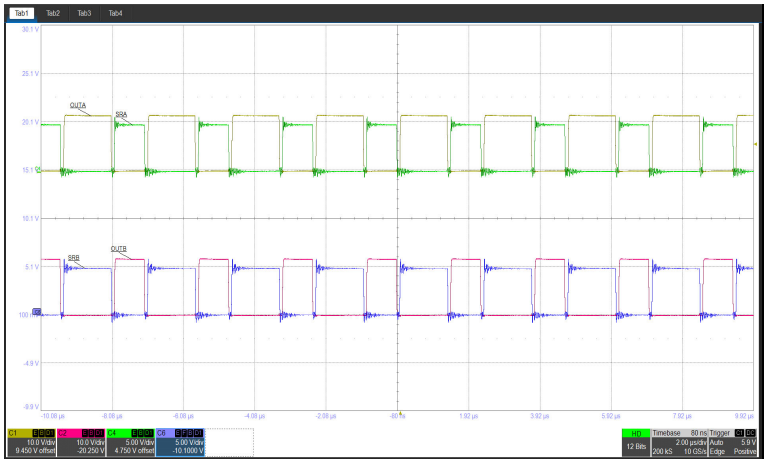


Figure 52. DCSL Floating PWM Outputs Waveforms

When the DCSL pin is high (Refer to Figure 53), OUTA and OUTB are completely overlapped. SRA and SRB are inverted versions of OUTA and OUTB (completely overlapped). Dead time between OUTx and SRx controlled by resistor setting.

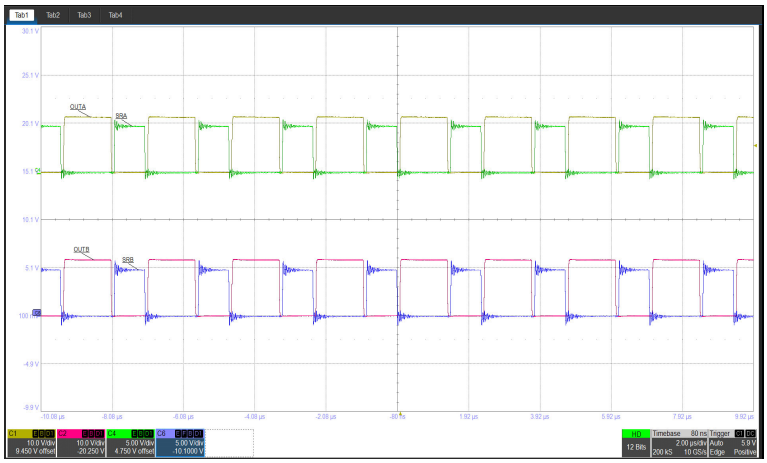


Figure 53. DCSL Tied to AVCC PWM Outputs Waveforms

Note the following:

- If the DCSL pin is tied to Ground, the frequency of OUTx is half of the Oscillator frequency f_{SW}.
- If the DCSL pin is left floating, $(t_{MIN\_ON}) – 2×(t_{DT\_SP})$ must be set to ≥ 100ns.
- If the DCSL pin is Tied to AVCC, $(t_{MIN\_ON}) – (t_{DT\_SP})$ must be set to ≥ 100ns.
- If the DCSL pin is tied to GND, $(t_{MIN\_ON}) – (t_{DT\_SP})$ must be set to ≥ 100ns.

5.12 SYNC

The SYNC pin can be configured as an input or an output based on how the RT pin is terminated. When the RT pin is tied to AGND through a resistor, the SYNC outputs a square wave signal with a 50% duty cycle. The frequency of the output signal is the same as the internal oscillator.

When the RT pin is tied to AVCC, the SYNC pin is configured as an input and expects a square wave signal at a given frequency. The acceptable duty cycle range for SYNC is between 30% and 70%.

Use this mode when using the ISL73846M in a parallel configuration or if synchronization to a primary system clock is required. Refer to 2-Phase Converter Operation (Leader-Follower Mode).

5.13 2-Phase Converter Operation (Leader-Follower Mode)

2-Phase operation using the ISL73846M controllers can be achieved by configuring two devices in a leader-follower mode as shown in Figure 54. The SYNC pins of both devices are connected together. The RT pin of the leader is tied to AGND through a resistor (calculated using Equation 15). The SYNC pin of the leader outputs a clock signal either equal to or twice the switching frequency depending on how the DCSL pin is

configured. This clock signal serves as the clock input to the SYNC pin of the follower controller, which operates in external synchronization mode.

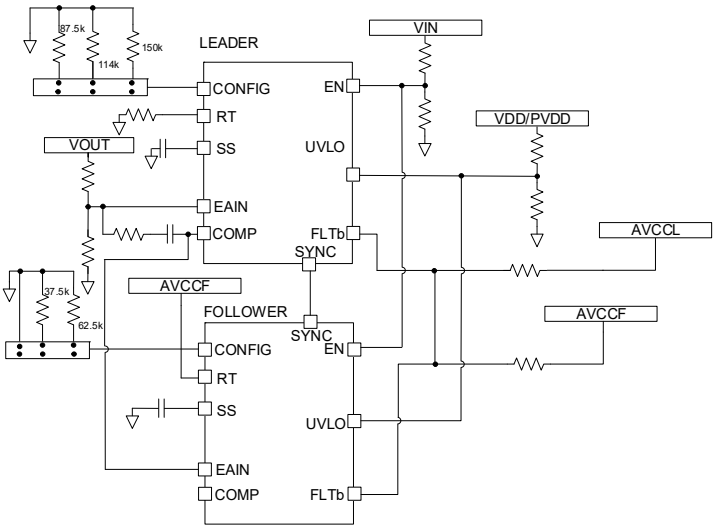


Figure 54. Leader-Follower Mode Configuration Using Two ISL73846

The RT pin of the follower device should be connected to the AVCC pin.The error amplifier of the leader is set to configuration 1 as mentioned in CONFIG Pin Functionality, while the error amplifier of the follower is set to configuration 2. The FLTb pin of the leader controller is connected to the FLTb pin of the follower controller and each tied to AVCC through a 10kΩ resistor. The SS pin of the leader and the follower should each have its own soft start capacitor of equal value. The OUTx of the leader and the follower are 180° phase shifted.

6. Layout

6.1 Layout Guidelines

To increase the reliability of the converter design using the ISL73846M, adhere to the following layout guidelines.

- Route the feedback trace away from any switching node on the printed circuit board (PCB).
- Route the feedback trace away from any existing magnetic component (Inductor and/or Transformer) on the printed circuit board (PCB).
- Ensure that a solid ground plane is present under the top layer and above the bottom layer.
- Minimize paths for high di/dt and dv/dt switching loops in the power stage to help reduce EMI.
- Separate analog ground (AGND) from power ground (PGND) of the power stage.
- Short analog ground (AGND) and power ground (PGND) at a point where PGND is the least noisy.
- Connect the sources of power semiconductor switches, the returns for bulk input capacitors of the power stage, and the output capacitor return to power ground (PGND).
- Shorten and widen all high current traces on the PCB.
- Place all filtering and decoupling capacitors for VDD, PVDD, AVCC, ISEN, UVLO, and EN close to the controller.
- Place the feedback voltage divider network near the EA_IN and COMP pins.
- Place external compensation components (surface mount preferred) near the COMP and EAIN pins of the controller.
- Route all traces that connect ISEN, COMP, EA_IN. DT_SP, DT_PS, RT, and RBLANK away from high dv/dt signals.

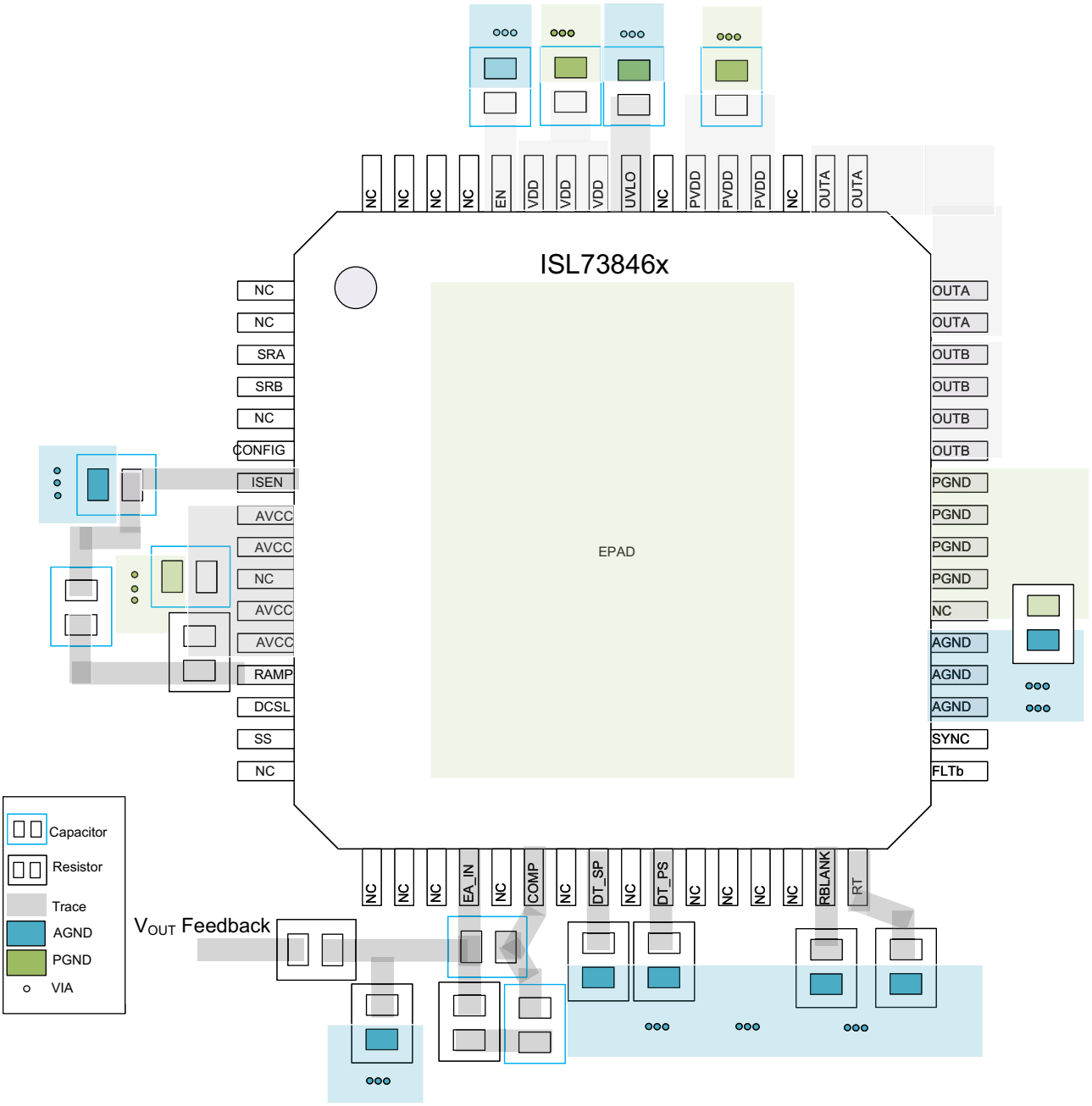


Figure 55. Layout Example

7. Radiation Tolerance

The ISL73846M is a radiation tolerant device for commercial space applications, Low Earth Orbit (LEO) applications, high altitude avionics, launch vehicles, and other harsh environments. This device's response to Total Ionizing Dose (TID) radiation effects and Single Event Effects (SEE) has been measured, characterized, and reported in the following sections. The ISL73846M30NEZ is radiation lot acceptance tested (RLAT) to 30krad(Si) and the ISL73846M50NEZ is RLAT to 50krad(Si).

7.1 Total Ionizing Dose (TID) Testing

7.1.1 Introduction

Total dose testing of the ISL73846M proceeded in accordance with the guidelines of MIL-STD-883 Test Method 1019. The experimental matrix consisted of 24 samples irradiated under bias and 24 samples irradiated with all pins grounded (unbiased). Three control units were used. Figure 56 shows the bias configuration. The samples were drawn evenly from wafer lots F6X785.6, F6X784.3, and F6X783.3. All samples were packaged in the production 64-Ld EP-TQFP production package.

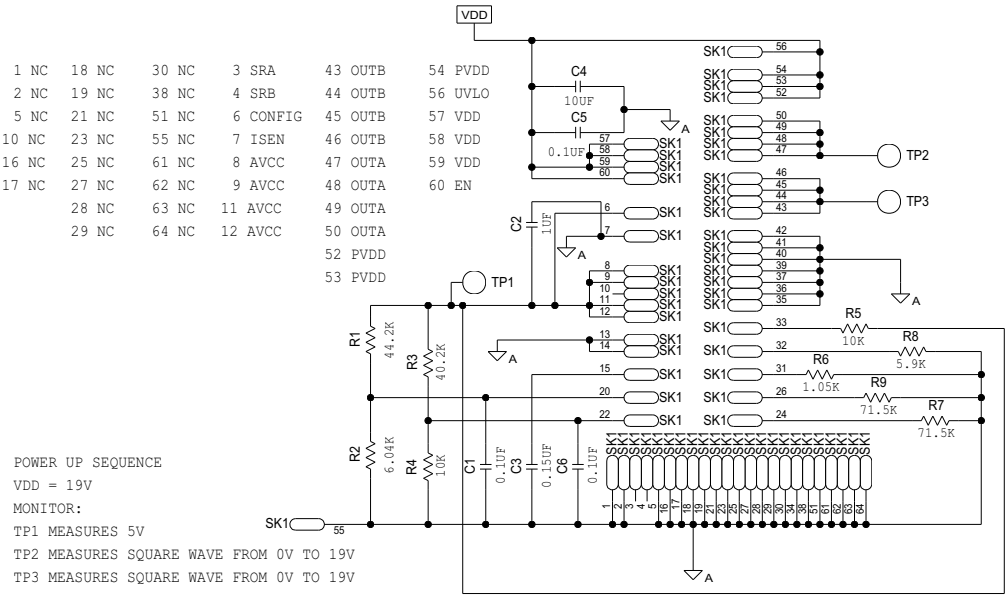


Figure 56. TID testing Bias Configuration

Samples were irradiated at a low dose rate (LDR) of 0.01rad(Si)/s using a Hopewell Designs N40 vault-type LDR irradiator located in the Palm Bay, Florida, Renesas Facility. A PbAl box was used to shield the text fixture and devices against low energy, secondary gamma radiation. All electrical testing was performed outside the irradiator using the production Automated Test Equipment (ATE) with data logging at each downpoint. Downpoint electrical testing was performed at room temperature. The planned irradiation downpoints were 0krad(Si), 10krad(Si), 30krad(Si), and 50krad(Si).

7.1.2 Results

Table 4 summarizes the attributes data.

Table 4. Attributes Data

Dose Rate (rad(Si)/s)	Condition	Sample Size	Downpoint	Pass[1]	Fail
0.01	Biased (Figure 56)	24	Pre-irradiation	24	0
			10krad(Si)	24	0
			30krad(Si)	24	0
			50krad(Si)	24	0
0.01	Grounded	24	Pre-irradiation	24	0
			10krad(Si)	24	0
			30krad(Si)	24	0
			50krad(Si)	24	0

1. A Pass indicates a device that passes all the datasheet specification limits.

The plots in Figure 57 through Figure 117 show data for key parameters at all downpoints. The plots show the sample size average as a function of the total dose for each irradiation condition. All parts showed excellent stability over irradiation.

7.1.3 Typical Radiation Performance

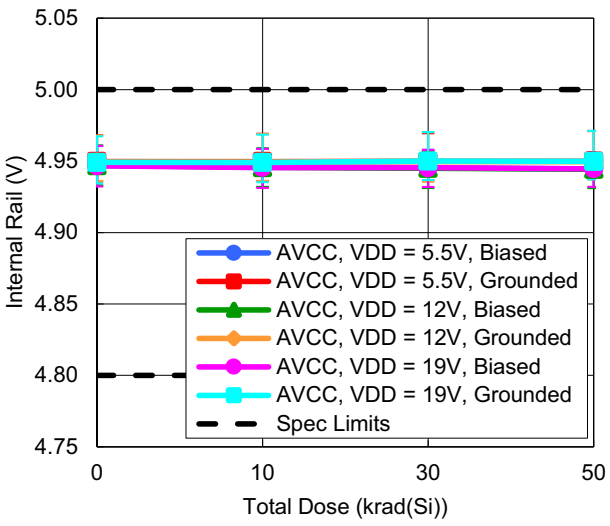


Figure 57. Internal Rail (AVCC) with I_{OUT} = 0mA vs TID

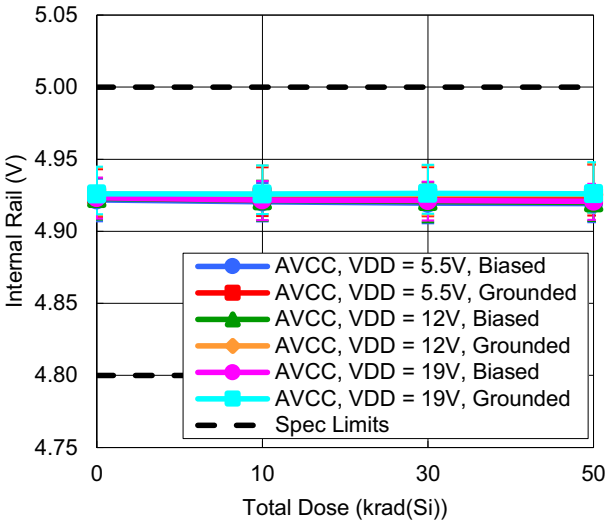


Figure 58. Internal Rail (AVCC) with I_{OUT} = 50mA vs TID

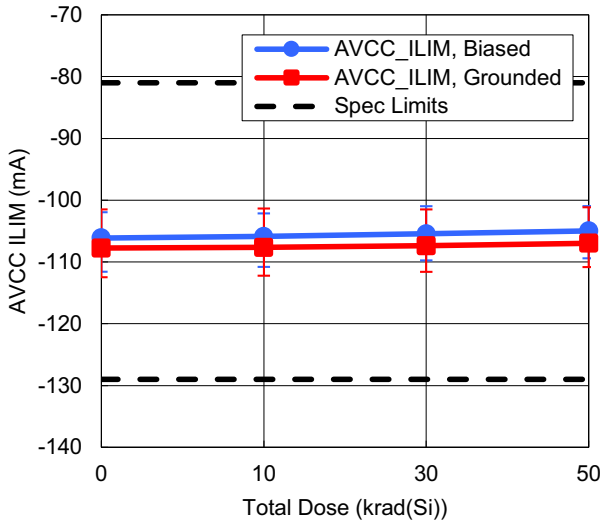


Figure 59. AVCC ILIM vs TID

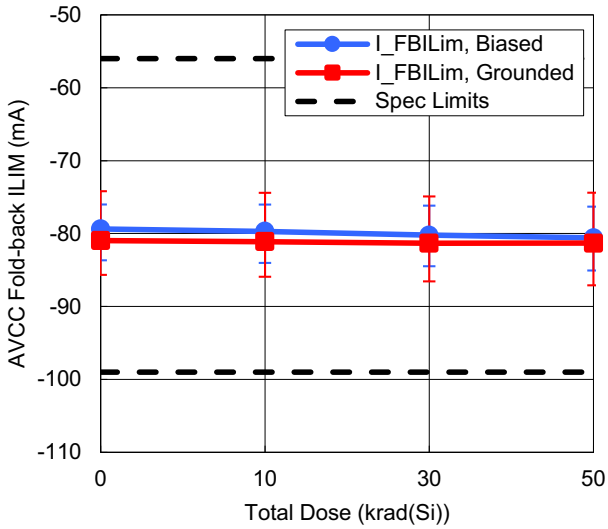


Figure 60. AVCC Fold-back ILIM vs TID

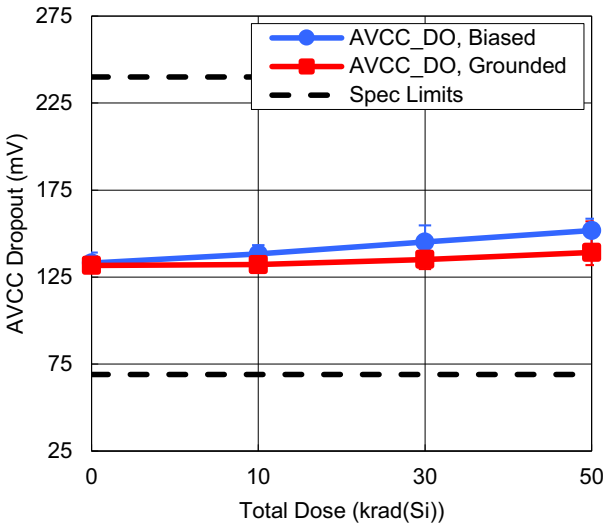


Figure 61. AVCC Dropout vs TID

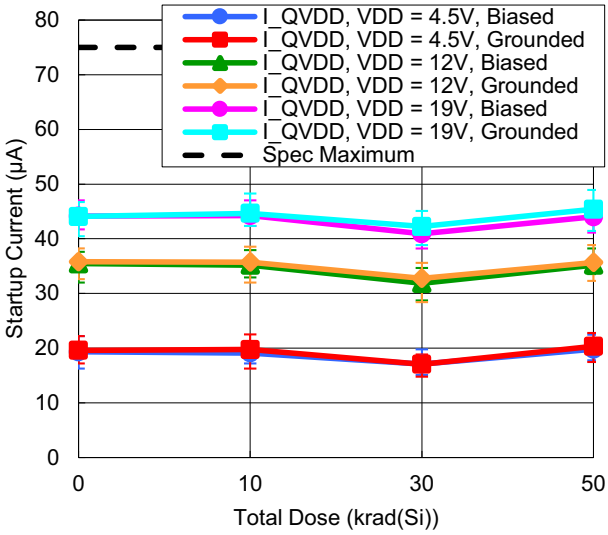


Figure 62. Startup Current (I_{QVDD}) vs TID

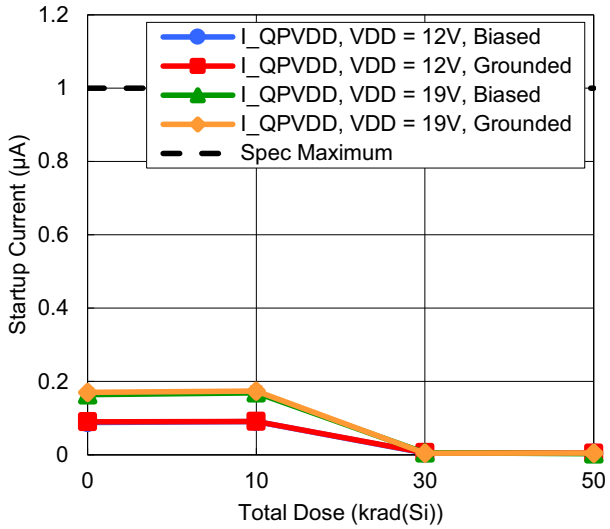


Figure 63. Startup Current (I_{QPVDD}) vs TID

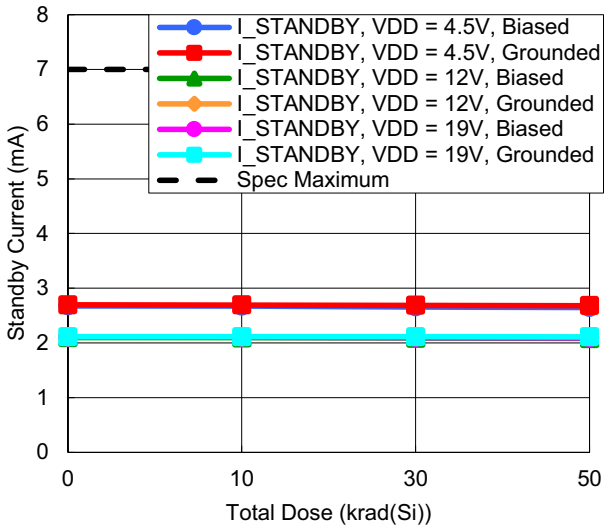


Figure 64. Standby Current with EN < 2V vs TID

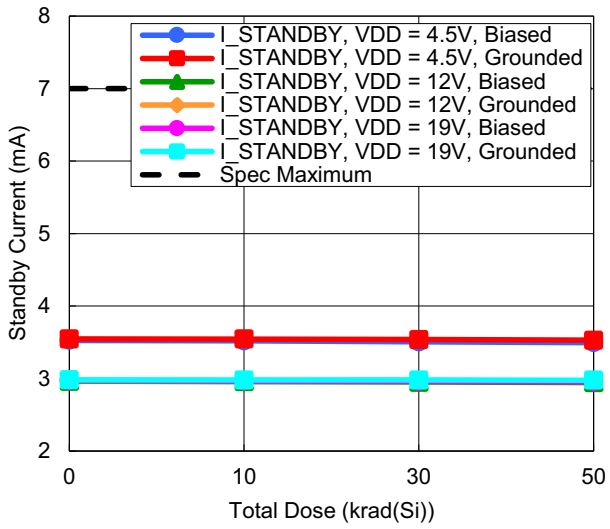


Figure 65. Standby Current with EN > 2V vs TID

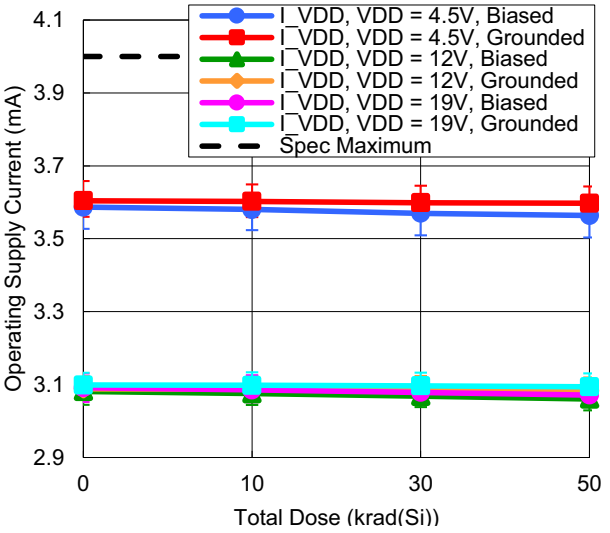


Figure 66. Operating Supply Current with f_{SW} = 20kHz vs TID

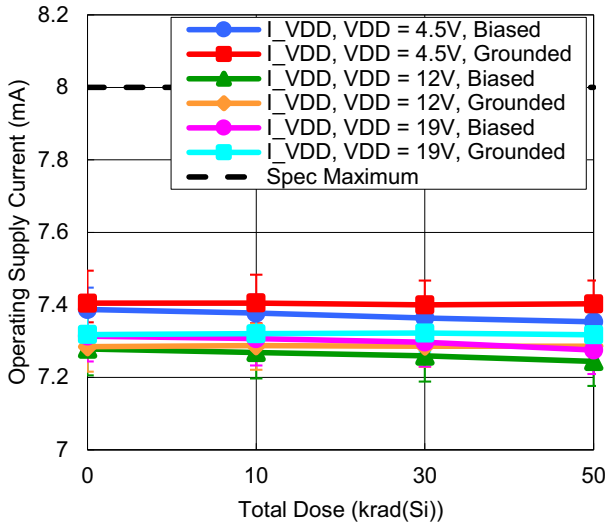


Figure 67. Operating Supply Current with f_{SW} = 500kHz vs TID

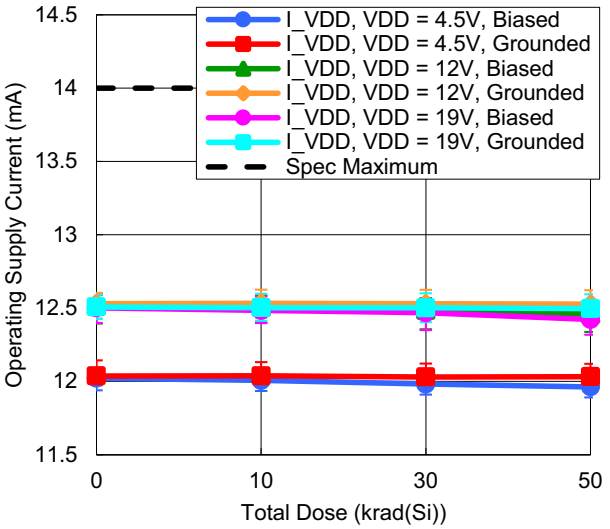


Figure 68. Operating Supply Current with f_{SW} = 1MHz vs TID

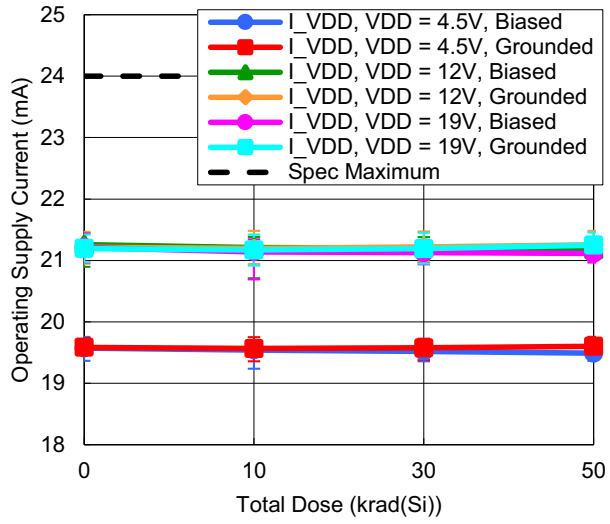


Figure 69. Operating Supply Current with f_{SW} = 2MHz vs TID

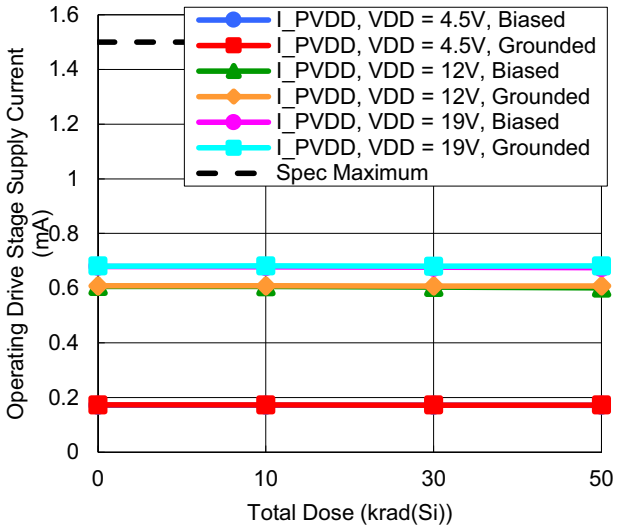


Figure 70. Operating Drive Stage Supply Current with f_{SW} = 20kHz vs TID

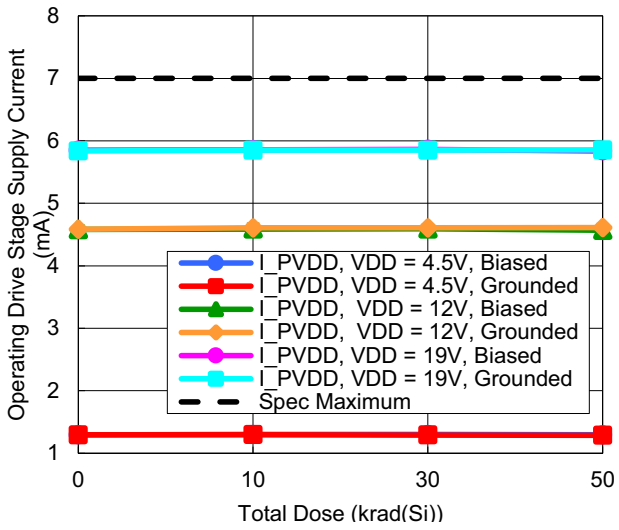


Figure 71. Operating Drive Stage Supply Current with f_{SW} = 500kHz vs TID

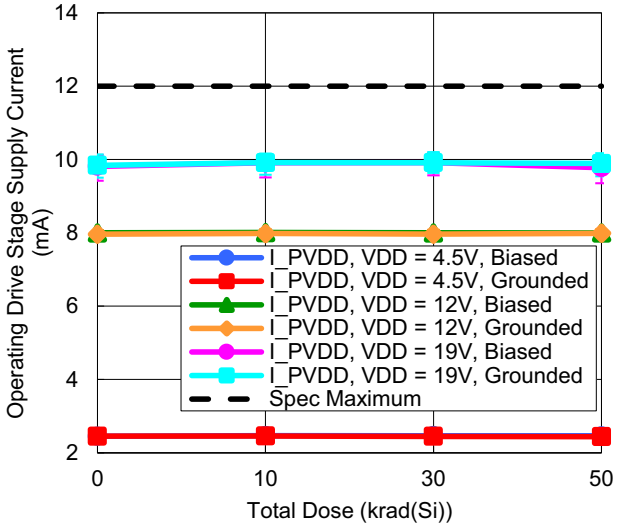


Figure 72. Operating Drive Stage Supply Current with f_{SW} = 1MHz vs TID

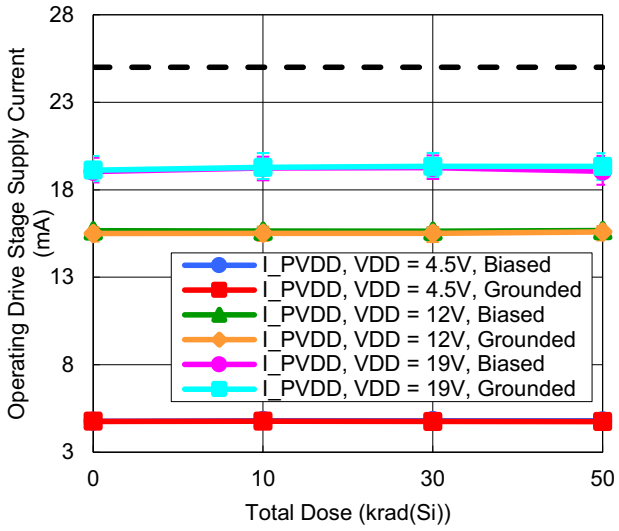


Figure 73. Operating Drive Stage Supply Current with f_{SW} = 2MHz vs TID

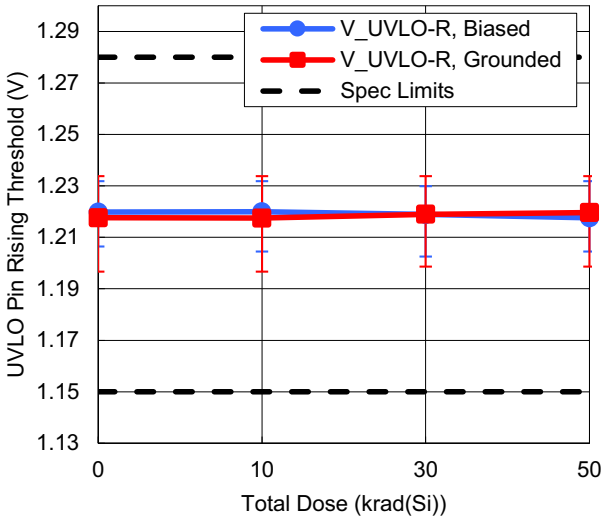


Figure 74. UVLO Pin Rising Threshold vs TID

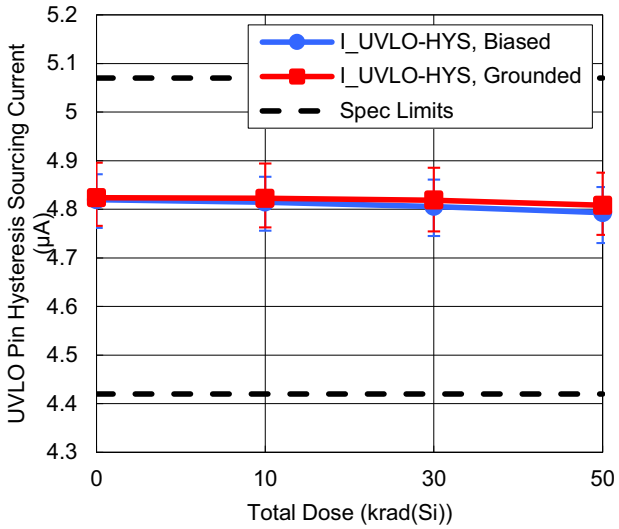


Figure 75. UVLO Pin Hysteresis Sourcing Current vs TID

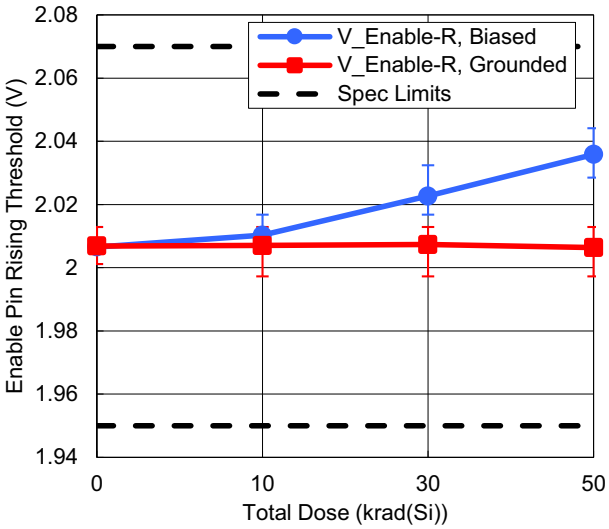


Figure 76. Enable Pin Rising Threshold vs TID

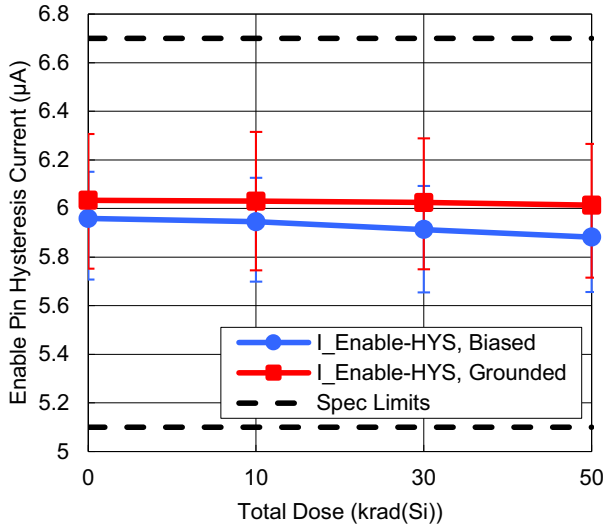


Figure 77. Enable Pin Hysteresis Current vs TID

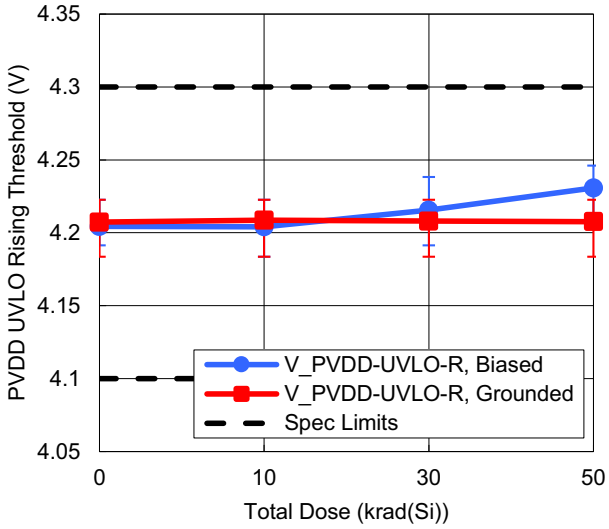


Figure 78. PVDD UVLO Rising Threshold vs TID

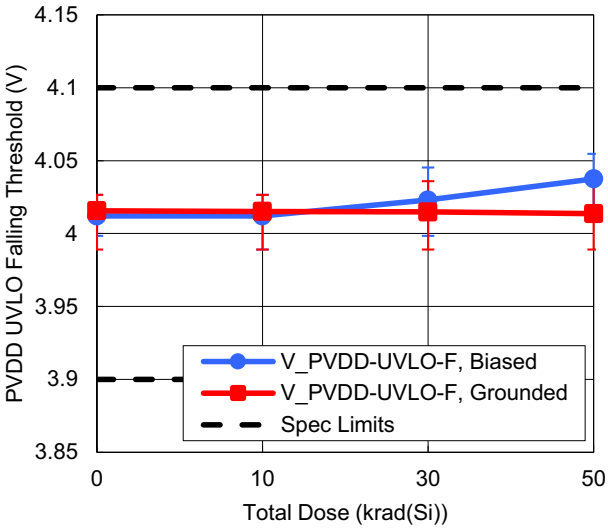


Figure 79. PVDD UVLO Falling Threshold vs TID

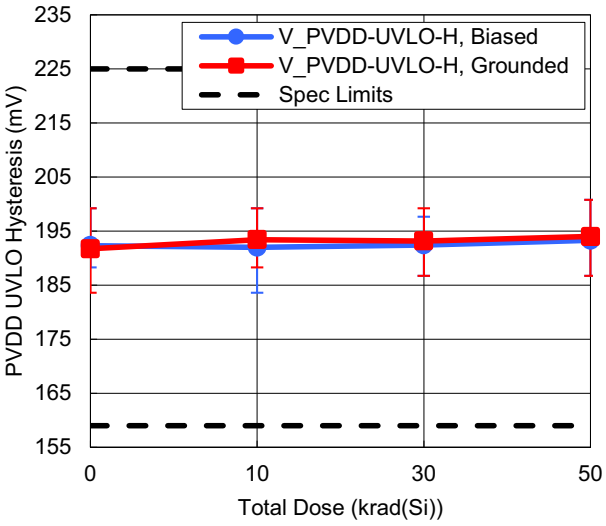


Figure 80. PVDD UVLO Hysteresis vs TID

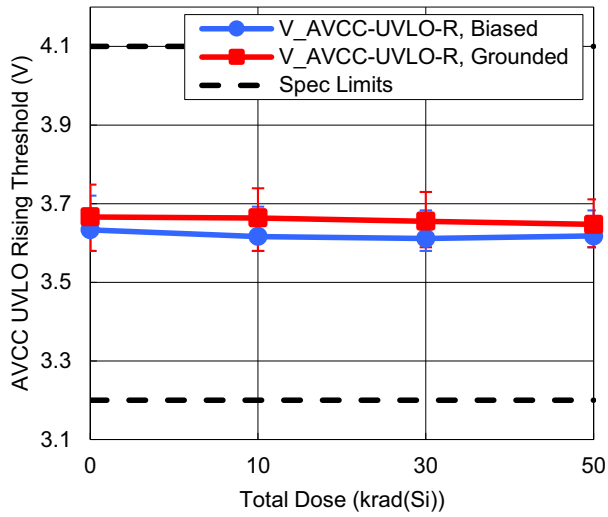


Figure 81. AVCC UVLO Rising Threshold vs TID

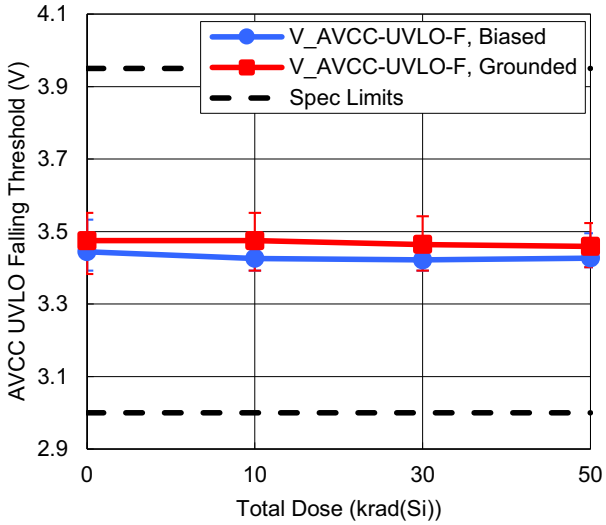


Figure 82. AVCC UVLO Falling Threshold vs TID

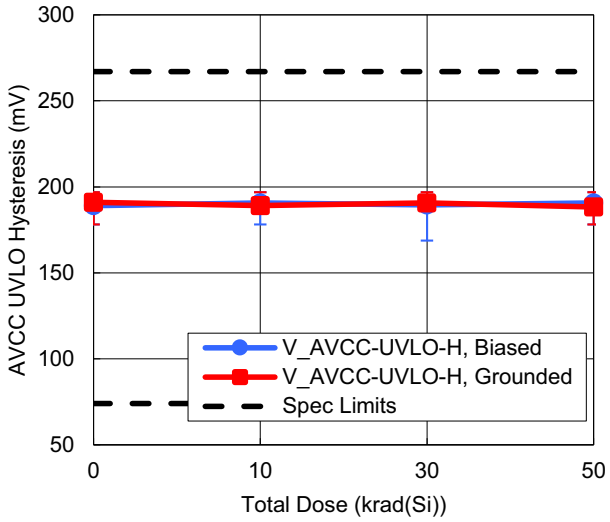


Figure 83. AVCC UVLO Hysteresis vs TID

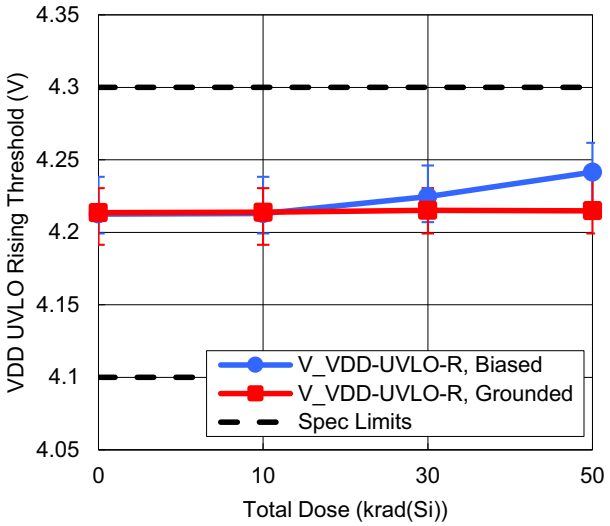


Figure 84. VDD UVLO Rising Threshold vs TID

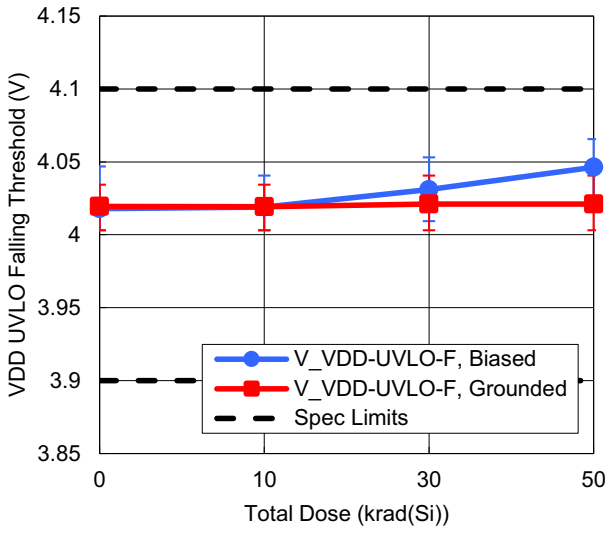


Figure 85. VDD UVLO Falling Threshold vs TID

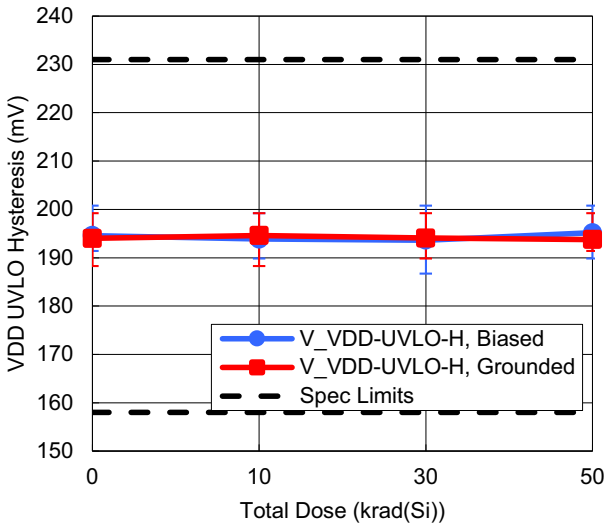


Figure 86. VDD UVLO Hysteresis vs TID

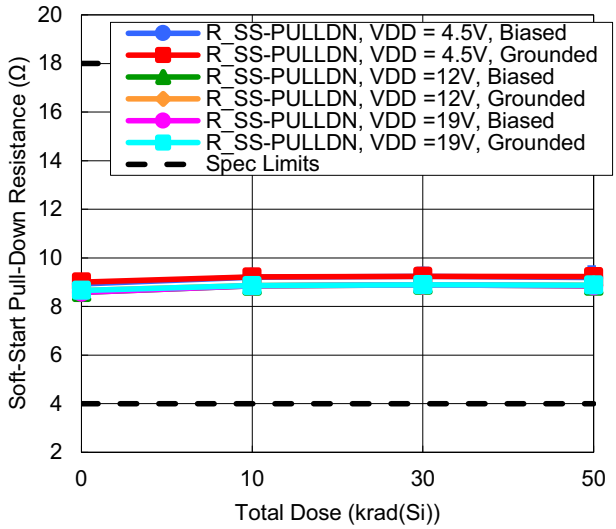


Figure 87. Soft-Start Pull-Down Resistance vs TID

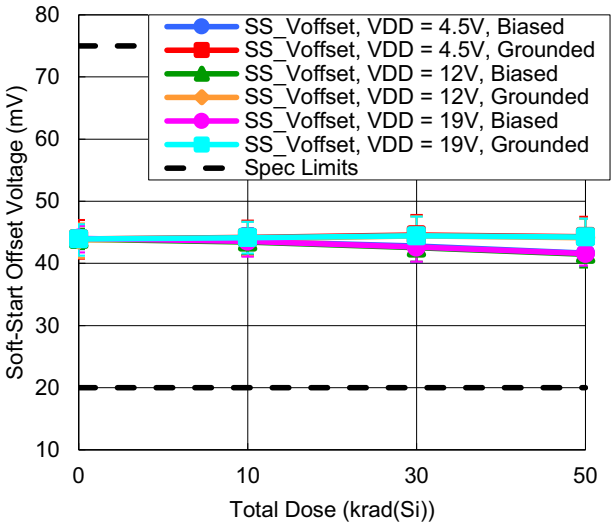


Figure 88. Soft-Start Offset Voltage vs TID

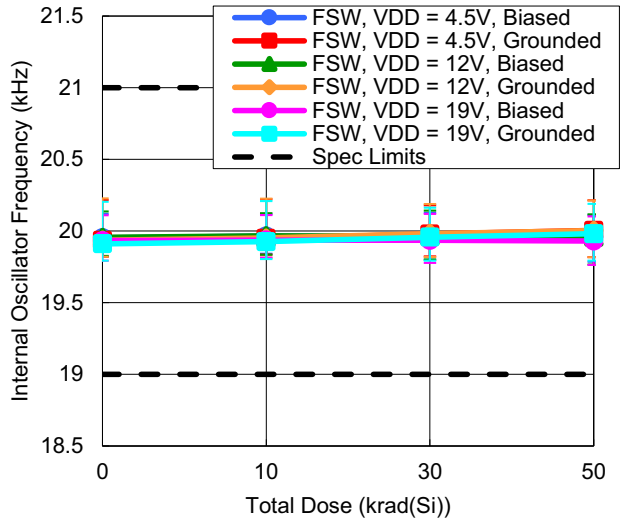


Figure 89. Internal Oscillator Frequency with RT = 122kΩ vs TID

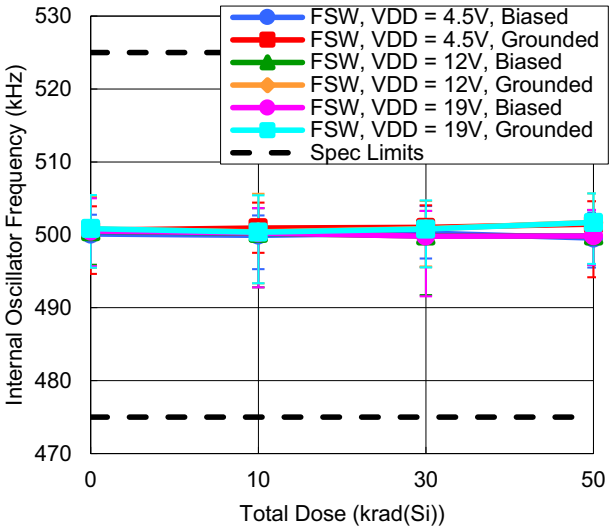


Figure 90. Internal Oscillator Frequency with RT = 4.7kΩ vs TID

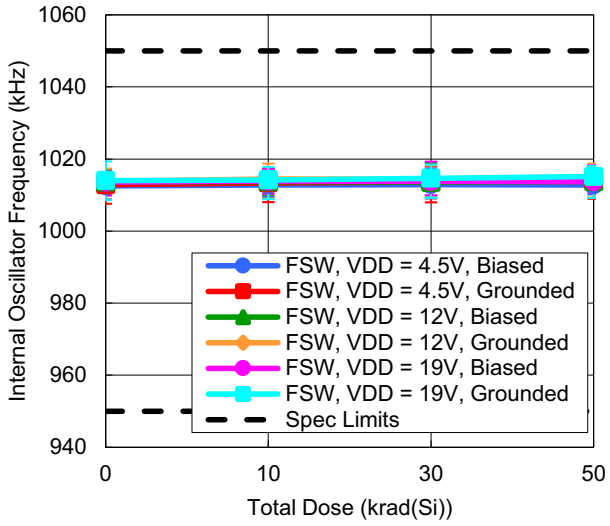


Figure 91. Internal Oscillator Frequency with RT = 2.26kΩ vs TID

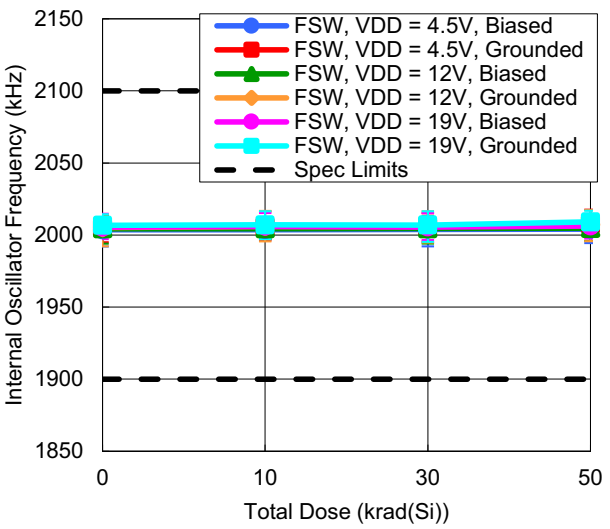


Figure 92. Internal Oscillator Frequency with RT = 1.07kΩ vs TID

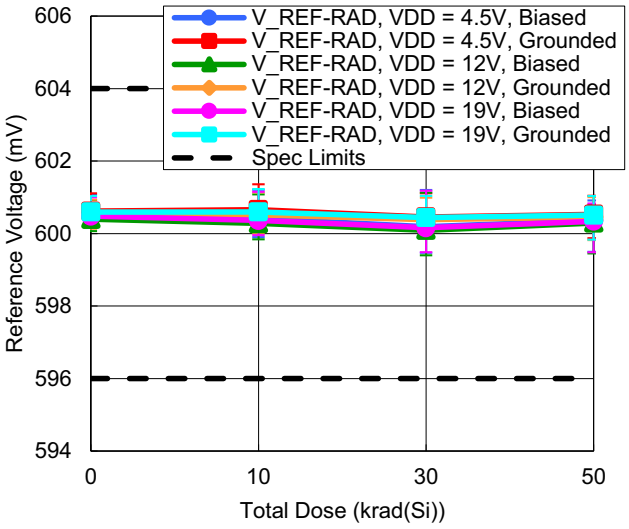


Figure 93. Reference Voltage vs TID

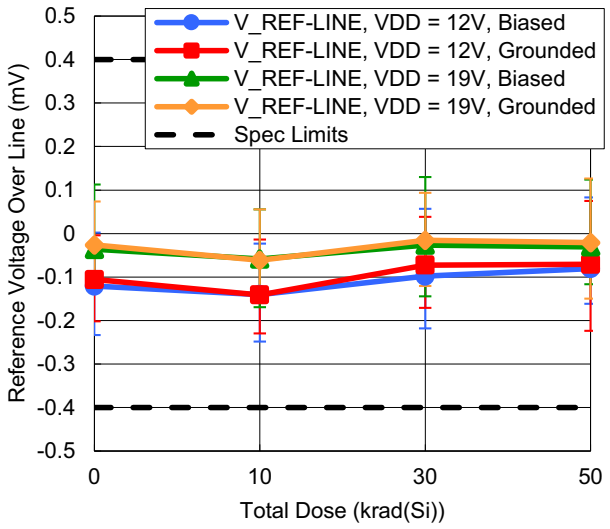


Figure 94. Reference Voltage Over Line vs TID

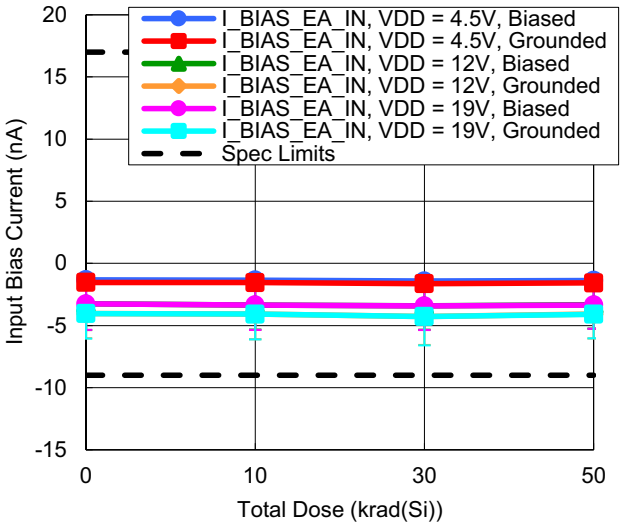


Figure 95. Input Bias Current with VCM = 0V vs TID

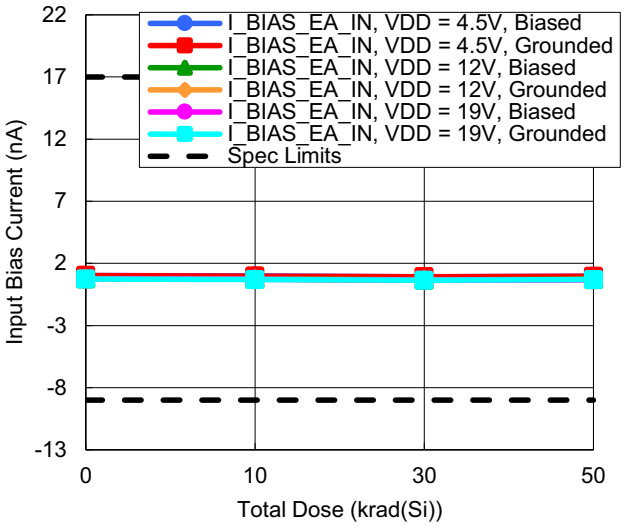


Figure 96. Input Bias Current with VCM = 2V vs TID

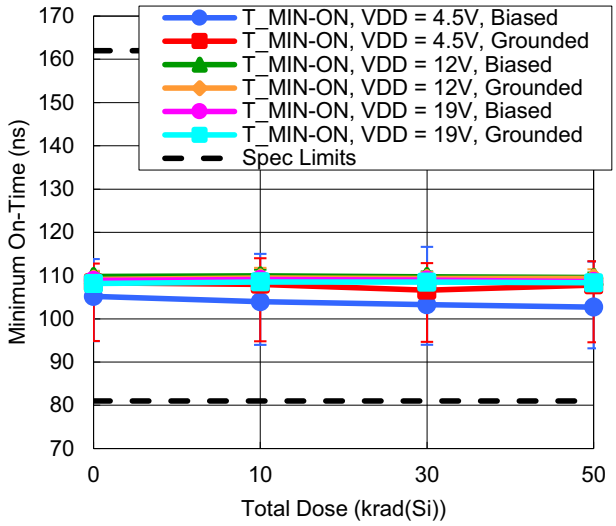


Figure 97. Minimum On-Time with R_{BLANK} = 1.05kΩ vs TID

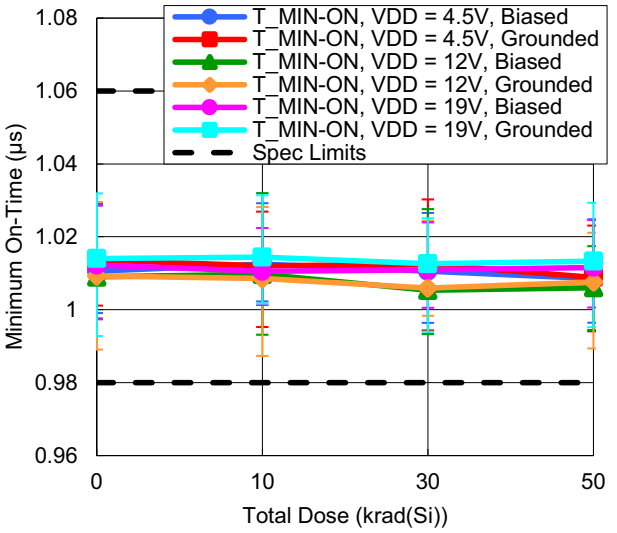


Figure 98. Minimum On-Time with R_{BLANK} = 10.5kΩ vs TID

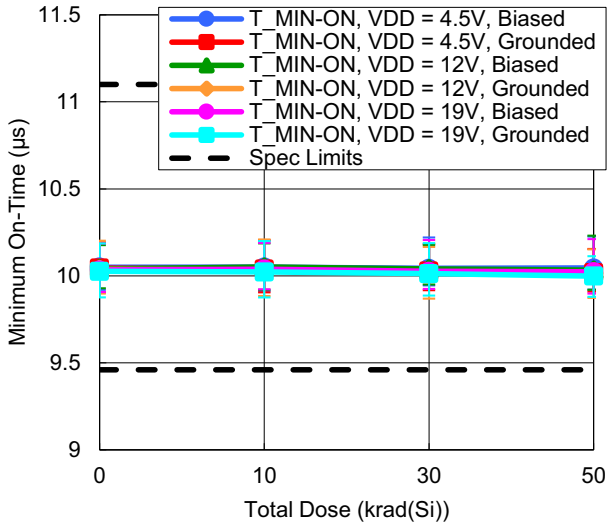


Figure 99. Minimum On-Time with R_{BLANK} = 105kΩ vs TID

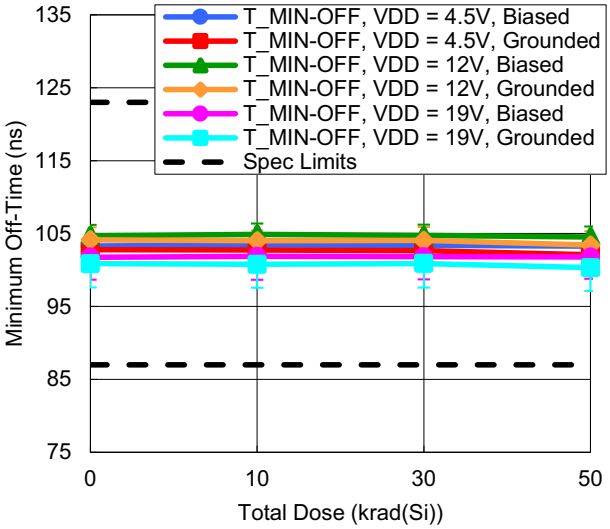


Figure 100. Minimum Off-Time with R_{BLANK} = 1.05kΩ vs TID

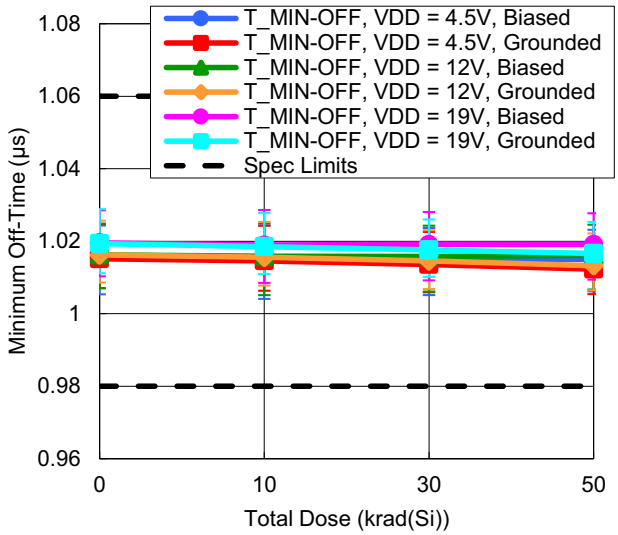


Figure 101. Minimum Off-Time with R_{BLANK} = 10.5kΩ vs TID

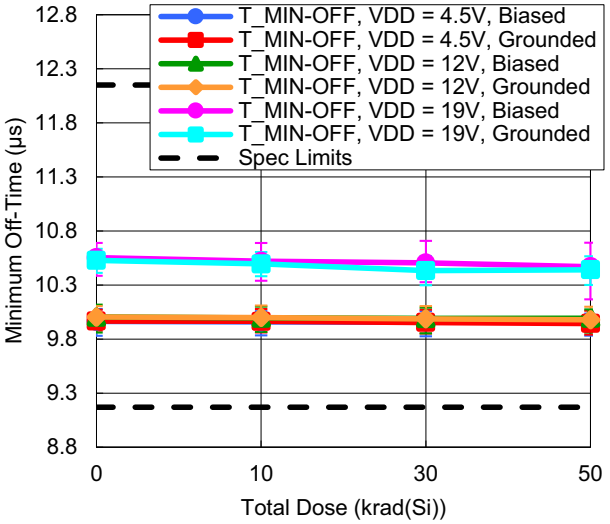


Figure 102. Minimum Off-Time with R_{BLANK} = 105kΩ vs TID

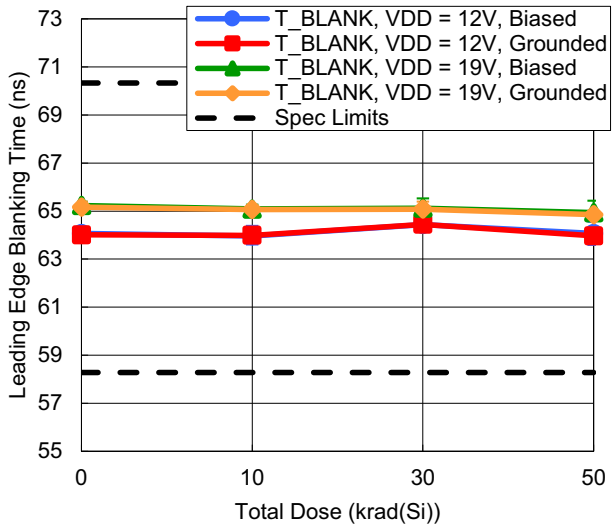


Figure 103. Leading Edge Blanking Time with R_{BLANK} = 1.05kΩ vs TID

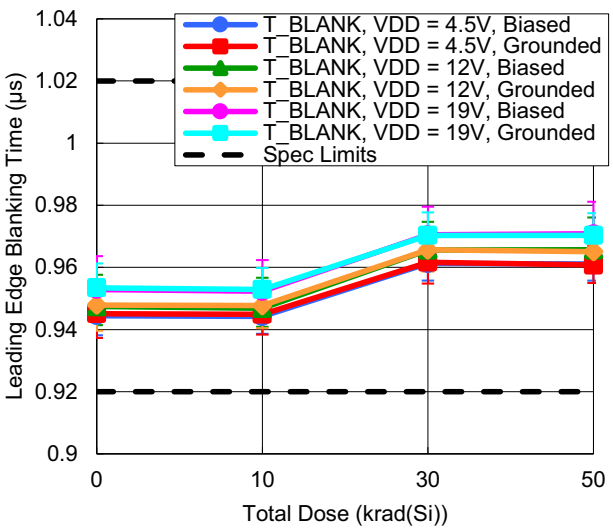


Figure 104. Leading Edge Blanking Time with R_{BLANK} = 10.5kΩ vs TID

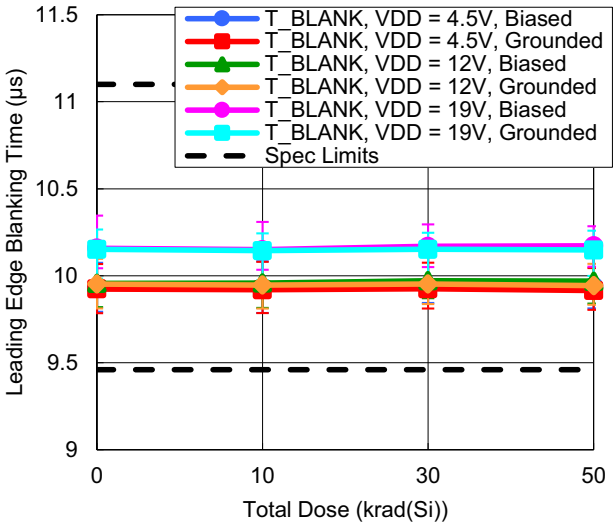


Figure 105. Leading Edge Blanking Time with R_{BLANK} = 105kΩ vs TID

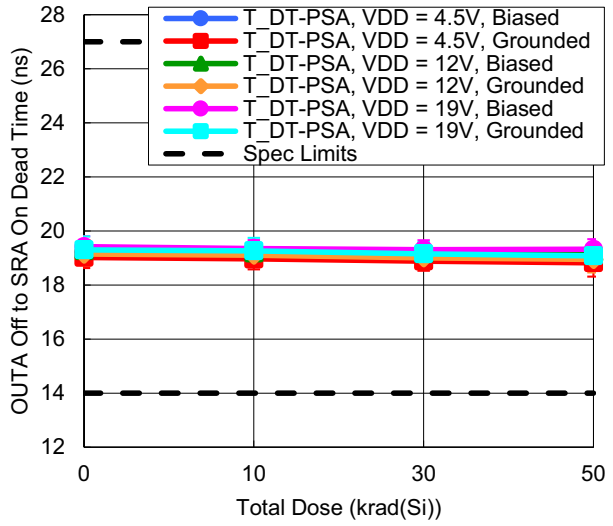


Figure 106. OUTA Off to SRA On Dead Time with R_{DT} = 4kΩ vs TID

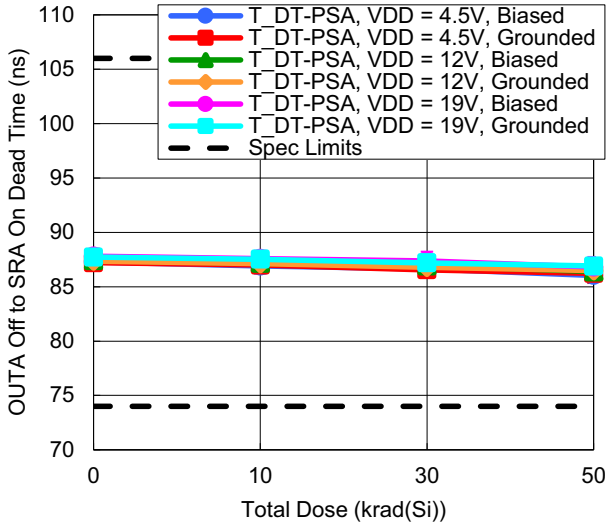


Figure 107. OUTA Off to SRA On Dead Time with R_{DT} 50kΩ vs TID

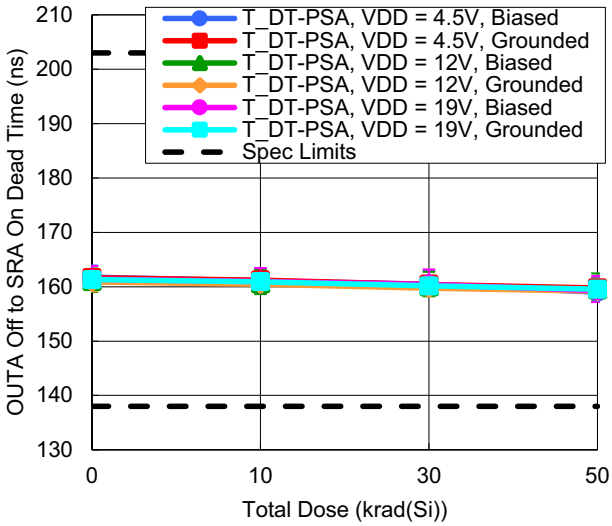


Figure 108. OUTA Off to SRA On Dead Time with R_{DT} = 100kΩ vs TID

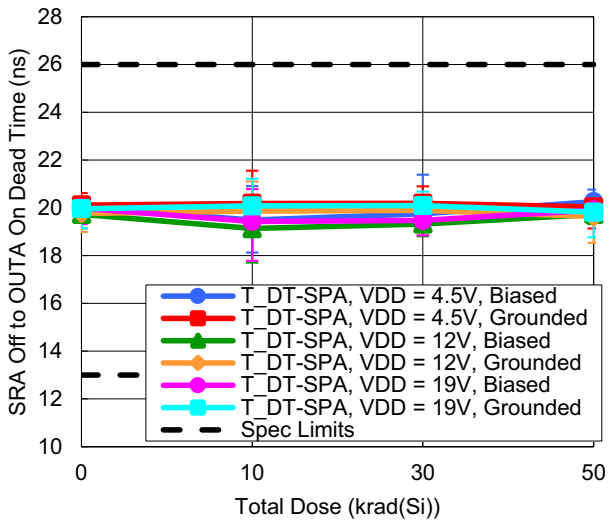


Figure 109. SRA Off to OUTA On Dead Time with R_{DT} = 4kΩ vs TID

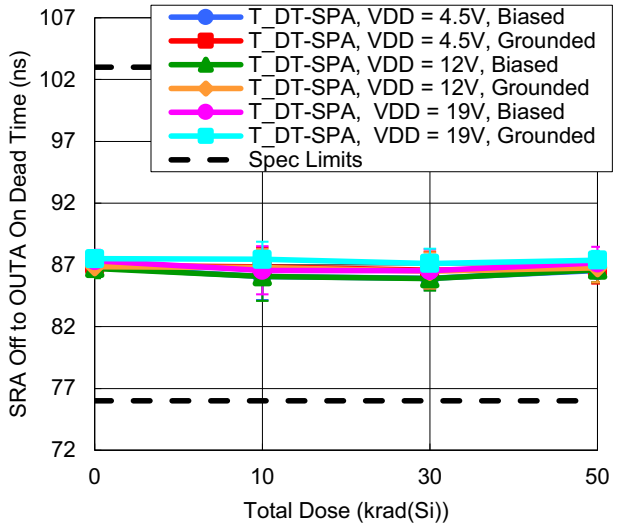


Figure 110. SRA Off to OUTA On Dead Time with R_{DT} = 50kΩ vs TID

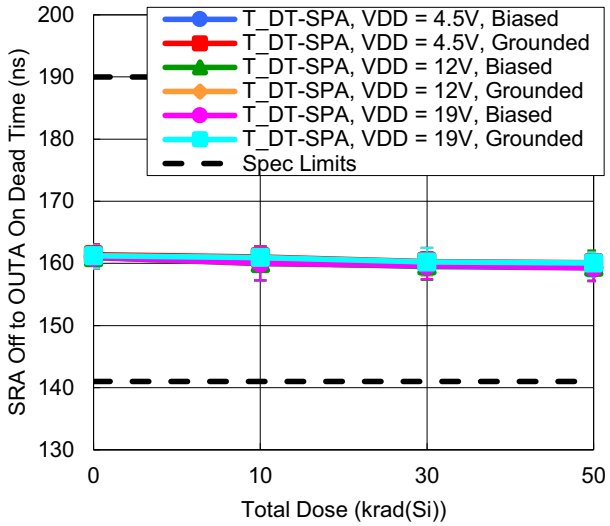


Figure 111. SRA Off to OUTA On Dead Time with R_{DT} = 100kΩ vs TID

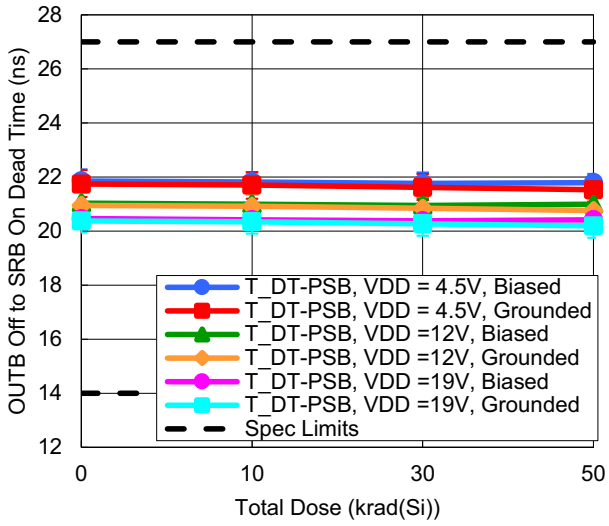


Figure 112. OUTB Off to SRB On Dead Time with R_{DT} = 4kΩ vs TID

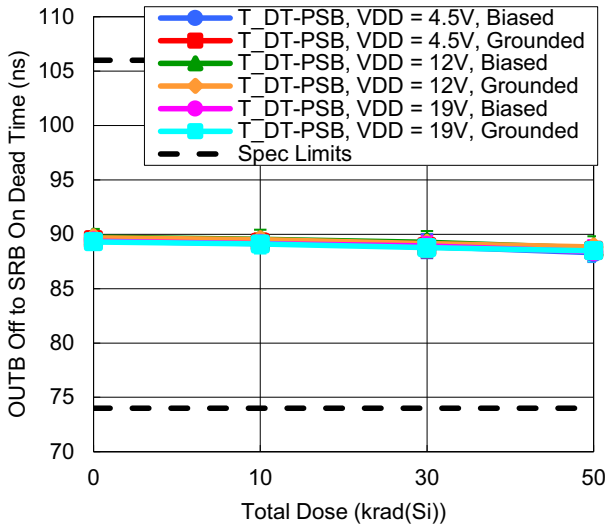


Figure 113. OUTB Off to SRB On Dead Time with R_{DT} 50kΩ vs TID

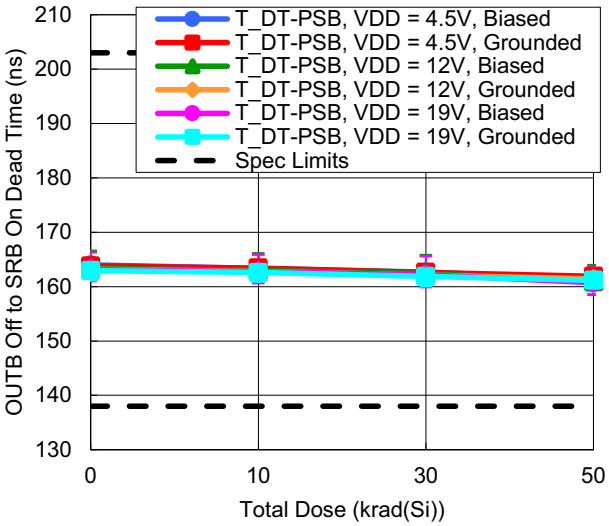


Figure 114. OUTB Off to SRB On Dead Time with R_{DT} 100kΩ vs TID

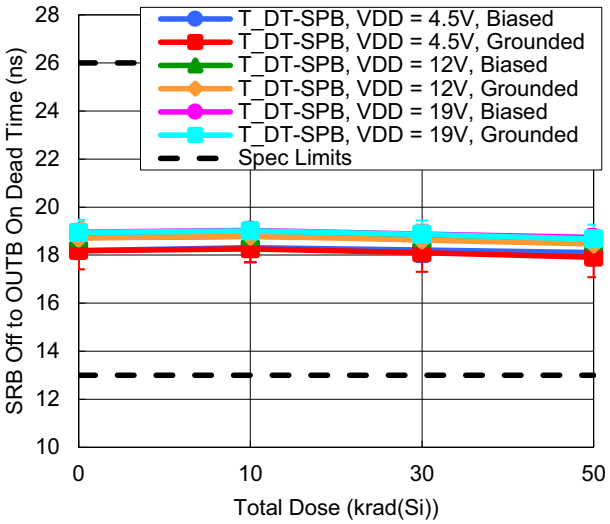


Figure 115. SRB Off to OUTB On Dead Time with R_{DT} 4kΩ vs TID

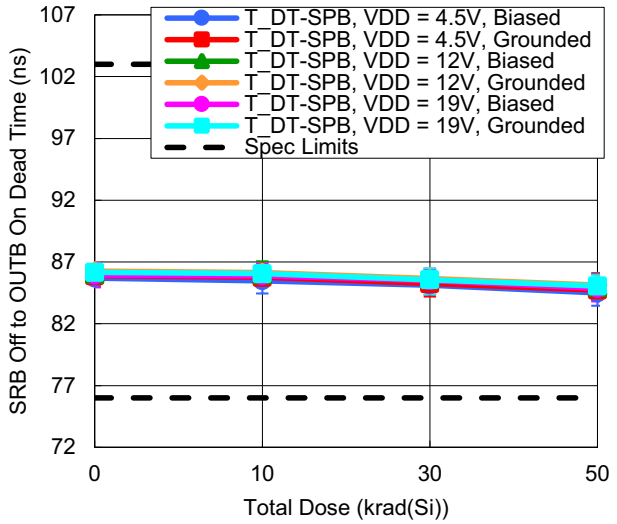


Figure 116. SRB Off to OUTB On Dead Time with R_{DT} 50kΩ vs TID

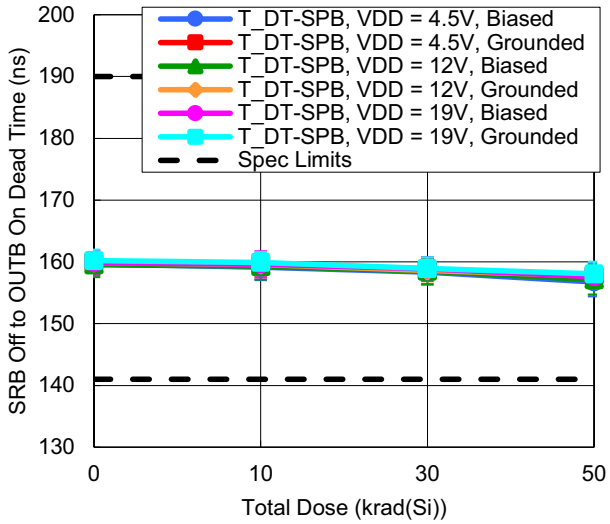


Figure 117. SRB Off to OUTB On Dead Time with R_{DT} 100kΩ vs TID

7.1.4 Conclusion

ATE characterization testing showed no rejects to the datasheet limits at all downpoints. Variables data for selected parameters are presented in Figure 57 to Figure 117. Some of the UVLO threshold levels (Figure 76, Figure 78, Figure 79, Figure 84, and Figure 85) showed a slight bias dependence, however all the parameters stayed within the specified limits.

7.2 Single Event Effects Testing

7.2.1 Introduction

The intense proton and heavy ion environment encountered in space applications can cause a variety of Single Event Effects (SEE) in electronic circuitry, including Single Event Upset (SEU), Single Event Transient (SET), Single Event Functional Interrupt (SEFI), Single Event Gate Rupture (SEGR), and Single Event Burnout (SEB). SEE can lead to system-level performance issues, including disruption, degradation, and destruction. Individual electronic components should be characterized for predictable and reliable space system operation to determine their SEE response. This section discusses the results of SEE testing on the ISL73846M PWM controller.

7.2.2 Test Facility

SEE testing was performed at the Texas A&M University (TAMU) Radiation Effects Facility of the Cyclotron Institute heavy ion facility. The facility is coupled to a K500 super-conducting cyclotron that can generate a wide range of particle beams with various energy, flux, and fluence levels required for advanced radiation testing. The Devices Under Test (DUTs) were in air at 40mm from the Aramica window for the ion beam. SET testing was performed on July 26, 2024 with normal incidence silver ions for an LET of 45.8MeV·cm^2/mg at the surface of the device. The LET of the ions in the active silicon layer ranged from 47.9MeV·cm^2/mg to 49.8MeV·cm^2/mg. The range to the Bragg peak was 105.1µm.

7.2.3 Destructive Single Event Effects (DSEE) Results

DSEE testing consisted of three components: VDD DSEE testing, PVDD DSEE testing, and AVCC DSEE testing. For all three components, the devices under test (DUTs) were set to operate in 500kHz push-pull operation with a 2A load. The DUT was enabled with 5V on the EN pin. VIN was set to 48V. The output voltage was 12V. For each test run, the DUT was exposed to fluence of 1E7ions/cm^2.

The purpose of the first component of DSEE testing was to find the maximum value of the power supply input for the control circuitry voltage (VDD) set by the onset of DSEEs at a die temperature of 125°C. For VDD DSEE testing, PVDD was set to 12V. VDD was initially set to 20.9V(18V+10% precision +95% derating), and was incremented after each run in steps of 5% derating up to a maximum voltage of 26.2V. Testing ended when the device exhibited a DSEE or when VDD reached 26.2V. The device was considered to have exhibited a DSEE if the output voltage changed by ±1% or the VDD current changed by ±2%.

The purpose of the second component of DSEE testing was to find the maximum value of the power supply input for the drive stage circuitry (PVDD) set by the onset of DSEEs at a die temperature of 125°C. For PVDD DSEE testing, VDD was set to 12V. PVDD was initially set 18V and was incremented after each run to a maximum voltage of 26.2V. Testing ended when the device exhibited a DSEE or when PVDD reached 26.2V. The device was considered to have exhibited a DSEE if the output voltage changed by ±1% or the PVDD current changed by ±1%.

The purpose of the third component of DSEE testing was to find the maximum value of the analog supply rail generated from VDD for the control circuitry (AVCC) set by the onset of DSEEs at a die temperature of 125°C. For AVCC DSEE testing, PVDD and VDD were set to 12V. Initially, AVCC was set to 5.5V and was incremented by 0.3V after each run to a maximum voltage of 6.9V. Testing ended when the device exhibited a DSEE or when AVCC reached 6.9V. The device was considered to have exhibited a DSEE if the output voltage changed by ±1% or the AVCC current changed by ±2%.

All four tested devices passed at the highest tested VDD voltage, VDD = 26.2V. Devices began to exhibit DSEE at PVDD = 20.9V, but all four tested devices passed testing at PVDD = 19V. Devices began exhibiting DSEE at AVCC = 6.1V, but all four tested devices passed at AVCC = 5.8V. Therefore, DSEE testing indicates that the device should be operated with the following maximum parameter set to be robust against DSEE at 46MeV·cm^2/mg: VDD = 26.2V, PVDD = 19V, and AVCC = 5.8V.

7.2.4 SET Results

The SET test board schematic is shown in Figure 118.

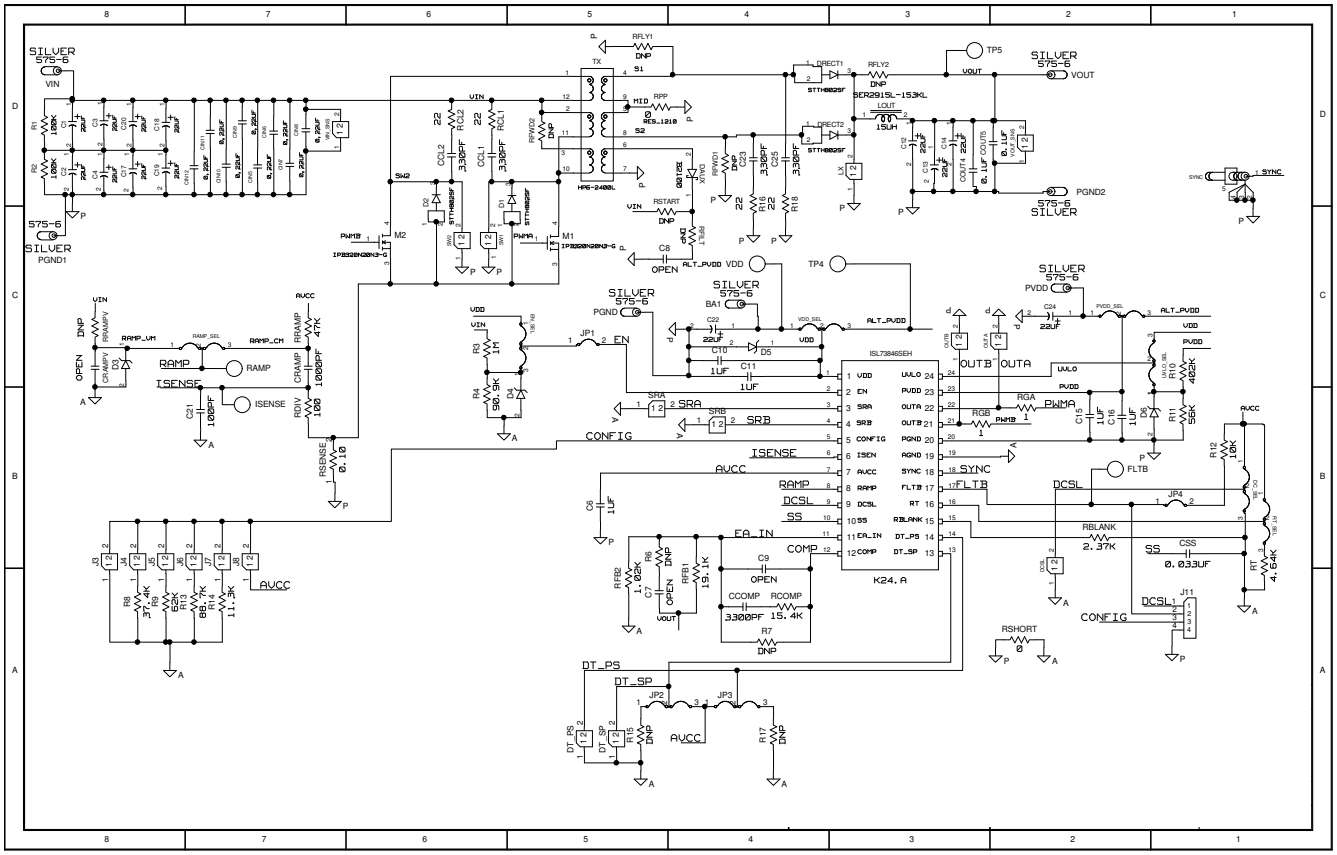


Figure 118. SET Test Board Schematic

For SET testing, devices were tested under four different test cases (TCs) as given in Table 5. For all conditions, the DUTs were set to operate in a 500kHz push-pull operation with a 2A load. The DUTs were enabled with 5V on the EN pin. PVDD was set to 15V. The ambient temperature was 25°C. An SET was defined as a deviation of the pulse width of the SRA or OUTB signals such that the pulse width of SRA extends beyond 5µs (SET1) or the separation between SRA pulses is outside of the range 0.2µs to 2µs (SET2) or the pulse width of OUTB is outside of the range of 0.2µs to 2µs (SET3) or the separation between OUTB pulses is longer than 5µs (SET4). A SEFI was defined as an event in which Soft-Start (SS) pin voltage fell below 4V. For each run, devices were irradiated to a fluence of 1E7ions/cm^2.

The results of SET testing for the ISL73846M are displayed in Table 5. The results are summarized in Table 6.

Table 5. ISL73846M SET Test Results at 46MeV·cm^2/mg

Test Case	VIN (V)	VDD (V)	DUT #	RUN #	# of SET1 SETs	# of SET2 SETs	# of SET3 SETs	# of SET4 SETs	# of SEFIs
#1	36	4.5	1	201	0	0	0	0	0
			2	205	2	0	3	0	0
			3	209	2	0	2	0	0
			4	213	2	0	2	0	0
#2	36	19	1	202	2	0	2	0	0
			2	206	1	0	1	0	0
			3	210	0	0	0	0	0
			4	214	10	0	2	0	0

Table 5. ISL73846M SET Test Results at 46MeV·cm²/mg

Test Case	VIN (V)	VDD (V)	DUT #	RUN #	# of SET1 SETs	# of SET2 SETs	# of SET3 SETs	# of SET4 SETs	# of SEFIs
#3	55	4.5	1	203	8	0	8	0	0
			2	207	4	0	4	0	0
			3	211	4	0	4	0	0
			4	215	3	0	11	0	0
#4	55	19	1	204	8	0	8	0	0
			2	208	6	0	6	0	0
			3	212	3	0	3	0	0
			4	216	0	0	0	0	0

Table 6. ISL73846M SET Test Results Summary at 46MeV·cm²/mg

Test Case	# of DUTs	Total Fluence (ions/cm²)	# of SET1 SETs	SET1 σ (µm²)	# of SET2 SETs	SET2 σ (µm²)	# of SET3 SETs	SET3 σ (µm²)	# of SET4 SETs	SET4 σ (µm²)	# of SEFIs	SEFI σ (µm²)
#1	4	4.0E7	6	15	0	2.5	7	17.5	0	2.5	0	2.5
#2	4	4.0E7	13	32.5	0	2.5	5	12.5	0	2.5	0	2.5
#3	4	4.0E7	19	47.5	0	2.5	27	67.5	0	2.5	0	2.5
#4	4	4.0E7	17	42.5	0	2.5	17	42.5	0	2.5	0	2.5
Worst Case				47.5		2.5		67.5		2.5		2.5

Figure 119 shows the scatter plot of the percent that VOUT deviates from the operating voltage versus the percent that the SRA pulse width deviates from the operating pulse width for all test cases. The SRA pulse width deviation was calculated as the percent difference between the SRA pulse width of the triggered pulse and the median SRA pulse width before the trigger. The SRA pulse width deviated by 58% to 65%. VOUT only deviated by -0.31% to -0.1%. TC 3 and TC 4 had similar SET responses. The pulse width deviation was consistently around 59%. TC 1 and TC 2 also seem to have a fairly similar response with a large clump of events having SRA pulse width deviations of approximately 64%.

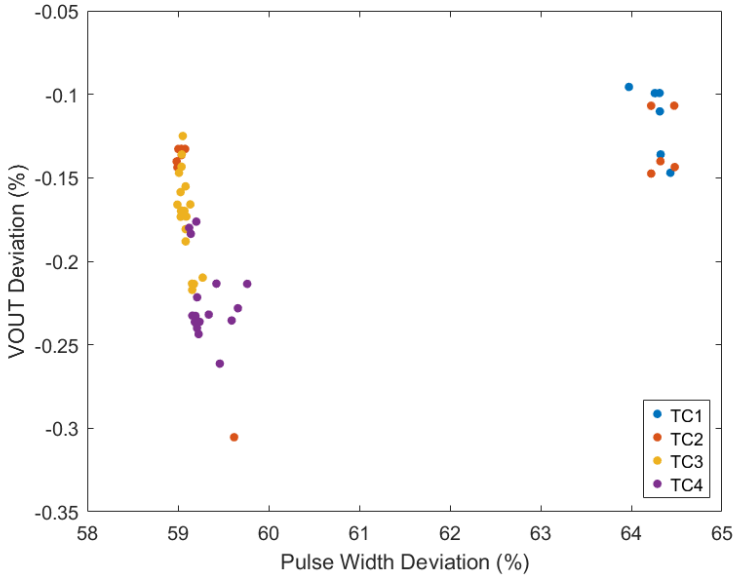


Figure 119. SET1: VOUT Deviation vs SRA Pulse Width Deviation at 46MeV·cm²/mg

Figure 120 shows the scatter plot of the percent that VOUT deviates from the operating voltage versus the percent that the OUTB pulse width deviates from the operating pulse width for all test cases. The OUTB pulse width deviation was calculated as the percent difference between the OUTB pulse width of the triggered pulse and the median OUTB pulse width before the trigger. The OUTB pulse width deviated by 55% to 61%; however, the deviations in OUTB pulse width did not translate to significant deviations in VOUT as VOUT only deviated by -0.31% to 0.17%. TC 3 and TC 4 had similar SET responses. The pulse width deviation was consistently around 56%. TC 1 and TC 2 also had similar SET responses with a pulse width deviation of approximately 60%.

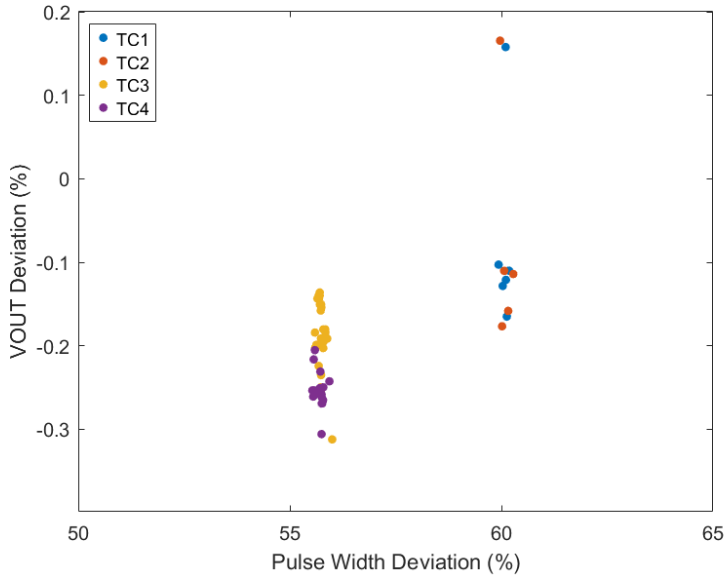


Figure 120. SET3: VOUT Deviation vs OUTB Pulse Width Deviation at 46MeV·cm^2/mg

The waveforms of the captured SET1s and SET3s were similar. Figure 121 shows a typical SRA pulse width deviation waveform. During the event, the SRA pulse at 0µs is elongated from the median pulse width of 3.35µs to 5.34µs. There is a similar elongation on SRB. OUTA and OUTB both show a missing pulse during the elongated SRA and SRB pulses. The elongation on SRA only lasts for one pulse. The pulse following the triggered pulse is slightly shortened as the part recovers, but operation is completely restored after this pulse. Despite the pulse width deviation, VOUT only deviates by as much as -0.24%.

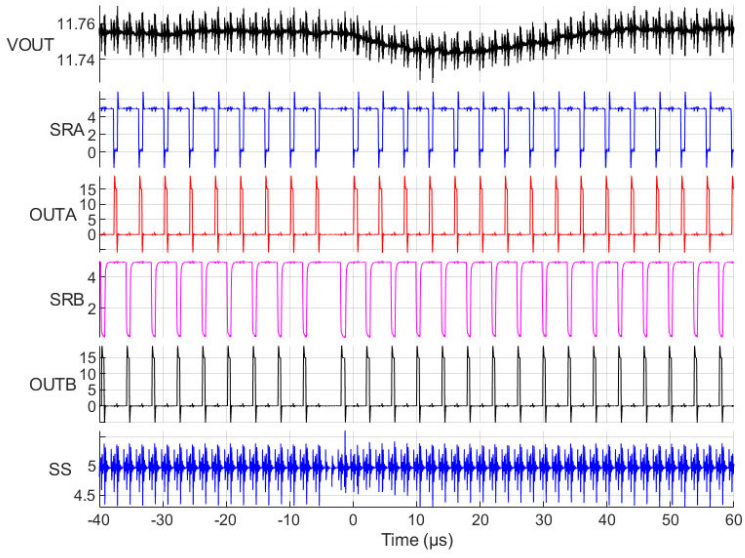


Figure 121. Typical SET1 Waveform in TC4 at 46MeV·cm^2/mg

7.2.5 Conclusion

The ISL73846M proved to be free from DSEE when operated with a maximum of VDD = 26.2V, PVDD = 19V, and AVCC = 5.8V at a die temperature of +125°C and an LET of 46MeV•cm^2/mg.

The ISL73846M exhibited SETs which elongated SRA and OUTB pulses at cross-sections <67.5µm^2. Although the pulses could be elongated by up to 65%, VOUT did not deviate by more than 0.31%. The elongation only lasted for one pulse. Therefore, these SETs pose a minimal threat, and the ISL73846M is an excellent choice for radiation tolerant applications.

8. Package Outline Drawing

The package outline drawing is located at the end of this document and is accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

9. Ordering Information

Part Number[1]	Part Marking	Rad Tolerance (Total Ionizing Dose)	Package Description[2] (RoHS Compliant)	Pkg. Dwg #	MSL Rating[3]	Carrier Type	Temp. Range
ISL73846M30NEZ	ISL73846MNZ	LDR to 30krad(Si)	64 Ld. EP-TQFP Plastic Packaged Device	Q64.10x10J	3	Tray	-55 to +125°C
ISL73846M30NEZ-T						Reel, k	
ISL73846M30NEZ-T7A						Reel, 250	
ISL73846M50NEZ	ISL73846MNZ	LDR to 50krad(Si)	64 Ld. EP-TQFP Plastic Packaged Device	Q64.10x10J	3	Tray	-55 to +125°C
ISL73846M50NEZ-T						Reel, k	
ISL73846M50NEZ-T7A						Reel, 250	
ISL73846MEV1Z[4]	N/A	N/A (For Evaluation Purposes)	Evaluation Board				

1. These Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu-Ag plate-e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. For the Pb-Free Reflow Profile, see TB493.
3. For more information about Moisture Sensitivity Level (MSL), see TB363.
4. Evaluation board uses devices that are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity.

10. Revision History

Revision	Date	Description
1.00	Jun 20, 2025	Initial Release

A. ECAD Design Information

This information supports the development of the PCB ECAD model for this device. It is intended to be used by PCB designers.

A.1 Part Number Indexing

Orderable Part Number	Number of Pins	Package Type	Package Code/POD Number
ISL73846M30NEZ	64	EP-TQFP	Q64.10x10J
ISL73846M30NEZ-T	64	EP-TQFP	Q64.10x10J
ISL73846M30NEZ-T7A	64	EP-TQFP	Q64.10x10J
ISL73846M50NEZ	64	EP-TQFP	Q64.10x10J
ISL73846M50NEZ-T	64	EP-TQFP	Q64.10x10J
ISL73846M50NEZ-T7A	64	EP-TQFP	Q64.10x10J

A.2 Symbol Pin Information

A.2.1 64-EP-TQFP

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
1	NC	Passive	-
2	NC	Passive	-
3	SRA	Output	-
4	SRB	Output	-
5	NC	Passive	-
6	CONFIG	Input	-
7	ISEN	Input	-
8	AVCC	Power	-
9	AVCC	Power	-
10	NC	Passive	-
11	AVCC	Power	-
12	AVCC	Power	-
13	RAMP	Input	-
14	DCSL	Input	-
15	SS	Input	-
16	NC	Passive	-
17	NC	Passive	-
18	NC	Passive	-
19	NC	Passive	-
20	EA_IN	Input	-
21	NC	Passive	-
22	COMP	Output	-
23	NC	Passive	-
24	DT_SP	Input	-
25	NC	Passive	-
26	DT_PS	Input	-
27	NC	Passive	-
28	NC	Passive	-
29	NC	Passive	-
30	NC	Passive	-
31	RBLANK	Input	-
32	RT	Input	-
33	FLTb	I/O	-
34	SYNC	I/O	-
35	AGND	Power	-
36	AGND	Power	-
37	AGND	Power	-
38	NC	Passive	-

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
39	PGND	Power	-
40	PGND	Power	-
41	PGND	Power	-
42	PGND	Power	-
43	OUTB	Output	-
44	OUTB	Output	-
45	OUTB	Output	-
46	OUTB	Output	-
47	OUTA	Output	-
48	OUTA	Output	-
49	OUTA	Output	-
50	OUTA	Output	-
51	NC	Passive	-
52	PVDD	Power	-
53	PVDD	Power	-
54	PVDD	Power	-
55	NC	Passive	-
56	UVLO	Input	-
57	VDD	Power	-
58	VDD	Power	-
59	VDD	Power	-
60	EN	Input	-
61	NC	Passive	-
62	NC	Passive	-
63	NC	Passive	-
64	NC	Passive	-
EPAD65	GND	Power	-

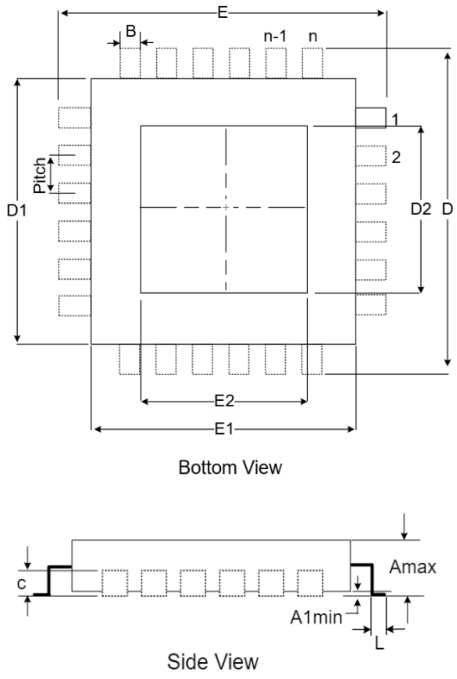
A.3 Symbol Parameters

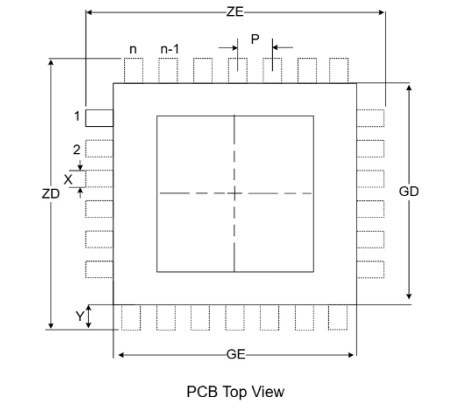
Orderable Part Number	Qualification	Radiation Qualification	LDR	Mounting Type	RoHS	Min Operating Temperature	Max Operating Temperature	Min Input Voltage	Max Input Voltage	Min Switching Frequency	Max Switching Frequency
ISL73846M30NEZ	Space	Radiation Tolerant	30 krad(Si)	SMD	Compliant	-55 °C	125 °C	4.5 V	19 V	20 kHz	2000 kHz
ISL73846M30NEZ-T	Space	Radiation Tolerant	30 krad(Si)	SMD	Compliant	-55 °C	125 °C	4.5 V	19 V	20 kHz	2000 kHz
ISL73846M30NEZ-T7A	Space	Radiation Tolerant	30 krad(Si)	SMD	Compliant	-55 °C	125 °C	4.5 V	19 V	20 kHz	2000 kHz
ISL73846M50NEZ	Space	Radiation Tolerant	50 krad(Si)	SMD	Compliant	-55 °C	125 °C	4.5 V	19 V	20 kHz	2000 kHz
ISL73846M50NEZ-T	Space	Radiation Tolerant	50 krad(Si)	SMD	Compliant	-55 °C	125 °C	4.5 V	19 V	20 kHz	2000 kHz
ISL73846M50NEZ-T7A	Space	Radiation Tolerant	50 krad(Si)	SMD	Compliant	-55 °C	125 °C	4.5 V	19 V	20 kHz	2000 kHz

A.4 Footprint Design Information

A.4.1 64-EP-TQFP

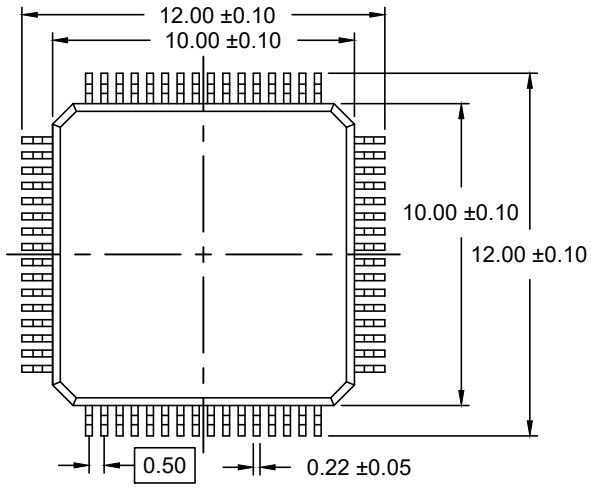
IPC Footprint Type	Package Code/ POD Number	Number of Pins
QFP	Q64.10x10J	64

Description	Dimension	Value (mm)	Diagram
Minimum lead span (vertical side)	Dmin	11.90	
Maximum lead span (vertical side)	Dmax	12.10	
Minimum lead span (horizontal side)	Emin	11.90	
Maximum lead span (horizontal side)	Emax	12.10	
Minimum body span (vertical side)	D1min	9.90	
Maximum body span (vertical side)	D1max	10.10	
Minimum body span (horizontal side)	E1min	9.90	
Maximum body span (horizontal side)	E1max	10.10	
Minimum Lead Width	Bmin	0.17	
Maximum Lead Width	Bmax	0.27	
Number of pins (vertical side)	PinCountD	16	
Number of pins (horizontal side)	PinCountE	16	
Distance between the center of any two adjacent pins	Pitch	0.50	
Location of pin 1; S2 = corner of D side, C1 = center of E side	Pin1	S2	
Minimum thermal pad size (vertical side)	D2min	7.15	
Maximum thermal pad size (vertical side)	D2max	7.45	
Minimum thermal pad size (horizontal side)	E2min	7.15	
Maximum thermal pad size (horizontal side)	E2max	7.45	
Minimum Lead Length	Lmin	0.45	
Maximum Lead Length	Lmax	0.75	
Maximum Height	Amax	1.20	
Minimum Standoff Height	A1min	0.05	
Minimum Lead Thickness	cmin	0.09	
Maximum Lead Thickness	cmax	0.20	

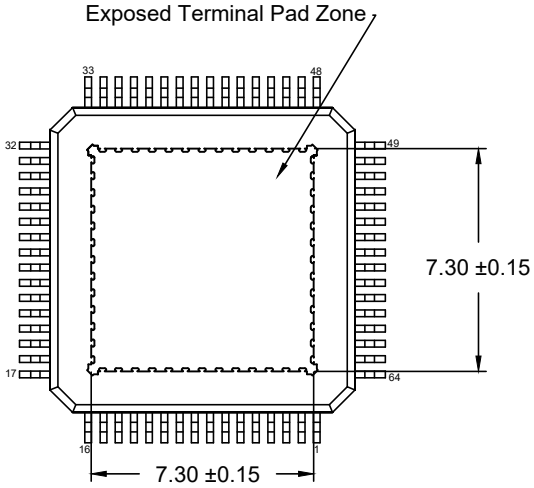
Recommended Land Pattern			
Description	**Dimension**	**Value (mm)**	**Diagram**
Distance between left pad toe to right pad toe (horizontal side)	ZE	12.60	
Distance between top pad toe to bottom pad toe (vertical side)	ZD	12.60	
Distance between left pad heel to right pad heel (horizontal side)	GE	10.20	
Distance between top pad heel to bottom pad heel (vertical side)	GD	10.20	
Pad Width	X	0.30	
Pad Length	Y	1.20	

Package Outline Drawing

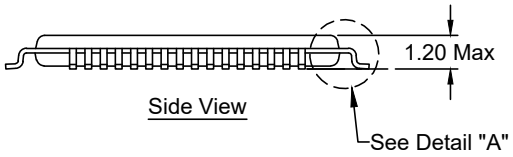
Q64.10x10J
PT0064AA
64-EPTQFP 10.0 x 10.0 x 1.2 mm Body, 0.5 mm Pitch
Rev01, Apr 1, 2025



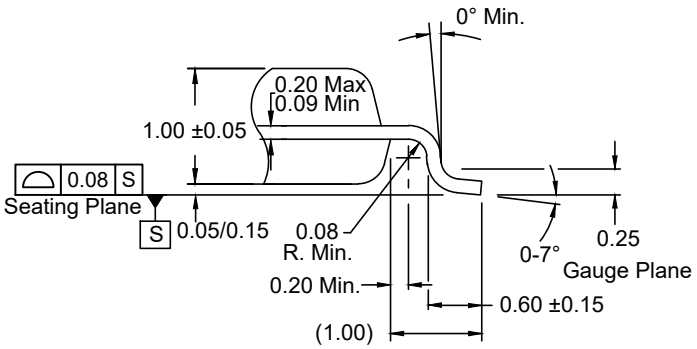
Top View



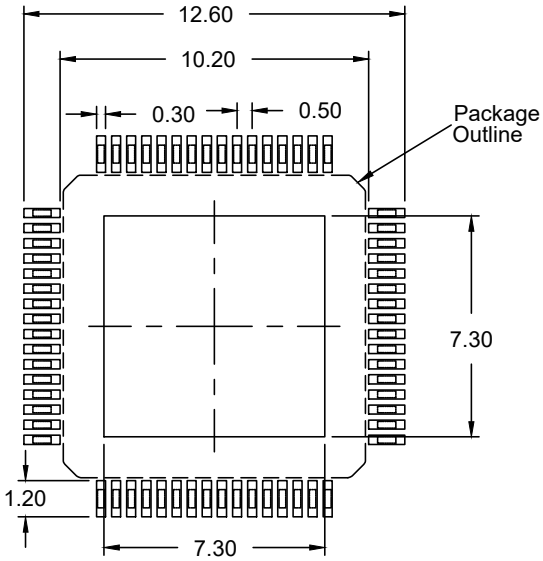
Bottom View



Side View



Detail A



Recommended Land Pattern
(PCB Top View, SMD Design)

Notes:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Foot length is measured at gauge plane 0.25 mm above seating plane.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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