ISL73849SLH

Radiation Hardened Single/Dual Phase Current Mode PWM Controller with PMBus & Telemetry

Description

The ISL73849SLH is a radiation-hardened PMBus-based synchronous buck controller that supports single- or dual-phase operation. It is designed to work with the ISL73041SEH (half-bridge GaN FET driver) to generate point-of-load voltage rails for commercial space applications.

The device operates from a 4.5V to 19V input and features a programmable switching frequency from 250kHz to 1.5MHz using a single resistor. The output can regulate voltages down to 200mV and is limited on the high end by minimum off-time and selected switching frequency.

The ISL73849SLH features built-in current sharing that enables 2-phase operation within a single device and 4-phase operation using two devices without requiring an external clock at frequencies up to 1.04MHz. For multi-phase configuration, the ISL74420M provides additional scalability. Current-mode control, remote sensing, PMBus control and telemetry, and robust fault protection enable a high-current, high-density power solution with minimal external components for FPGA cores and other general-purpose applications.

The ISL73849SLH operates across the military temperature range from -55°C to +125°C and is available in a 24 Ld hermetically sealed Ceramic Dual Flatpack (CDFP) package or die form.

Applications

- FPGA core power supply
- General purpose power supply

Features

- Qualified to Renesas Rad Hard QML-V Equivalent Screening and QCI Flow (R34TB0001EU)
  - All screening and QCI is in accordance with MIL-PRF-38535 Class-V
- Wide operating voltage range:
  - Input: 4.5V to 19V
  - Output: V_{REF} to PVIN×((T_{SW}-107ns)/T_{SW})
- Output switching frequency range
  - 250kHz to 1.5MHz
- Optional Droop regulation
- Current mode control provides
  - Excellent power supply rejection
  - Simplified control scheme
- Differential output remote sensing
- Programmable V_{REF} (0.2V to 1.2V) and soft start (0.5ms to 64ms)
- Hardware enable and software enable control
- Programmable UV, OV, OC fault levels
- Telemetry and fault reporting through PMBus
- TID Rad Hard Assurance (RHA) wafer-by-wafer testing
  - LDR (≤10mrad(Si)/s): 75krad(Si)
- SEE Characterization
  - No DSEE for, V_{DD} = 20V, V_{CC} = 6.1V, V_{ISEN} = 13.5V, and 86MeV•cm^2/mg
  - SEFI <2.5µm^2 at 86MeV•cm^2/mg
  - SET <3.55% on V_{OUT} at 86MeV•cm^2/mg

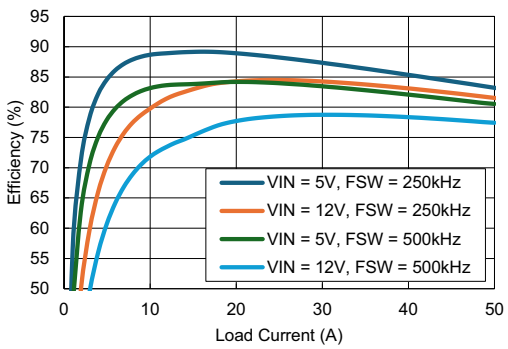


Figure 1. Conversion Efficiency (V_{OUT} = 1V, R_{SENSE} = 1mΩ)

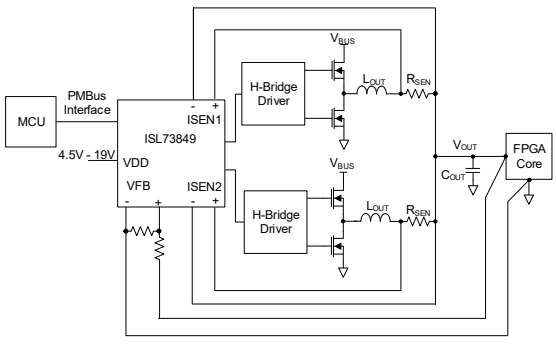


Figure 2. FPGA Core Power Supply Application

Contents

1. Overview

1.1 Typical Application Diagrams

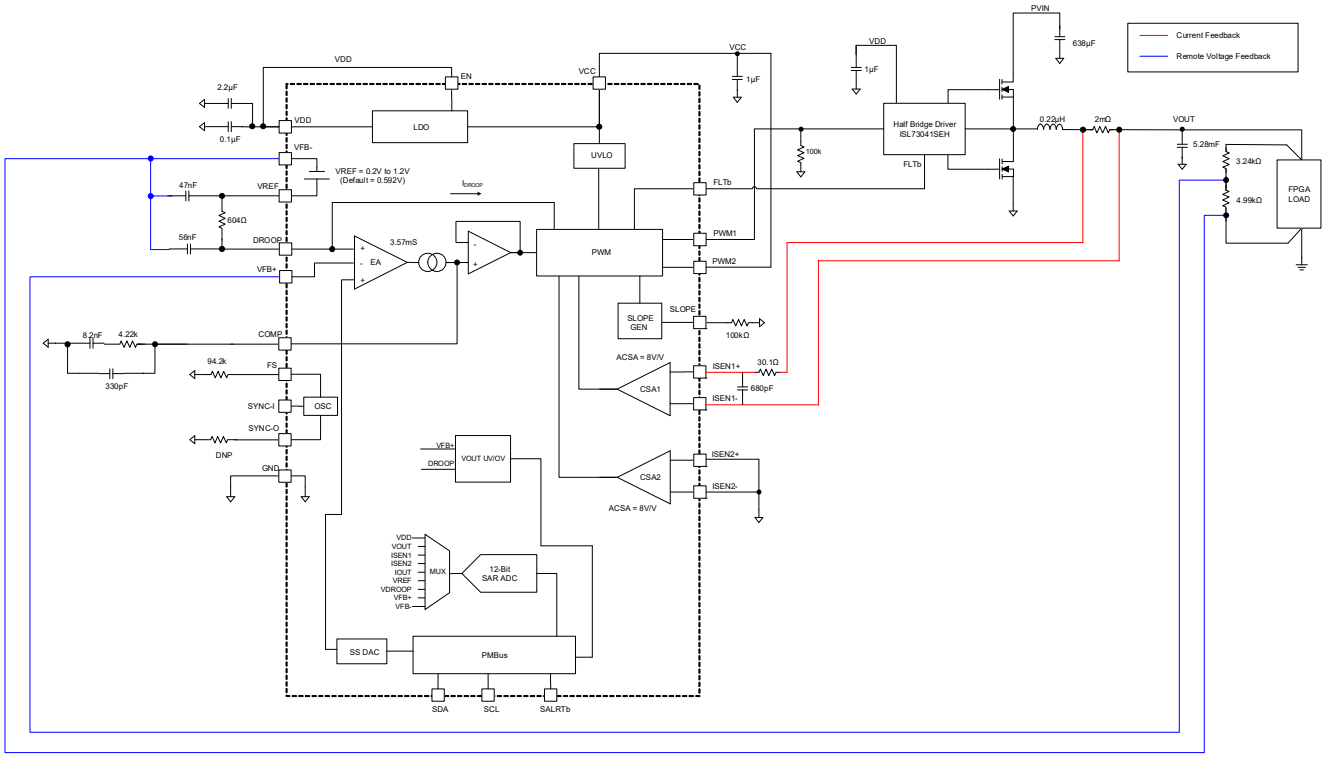


Figure 3. Typical Application (Single Phase) using One ISL73041SEH Half-Bridge Drivers

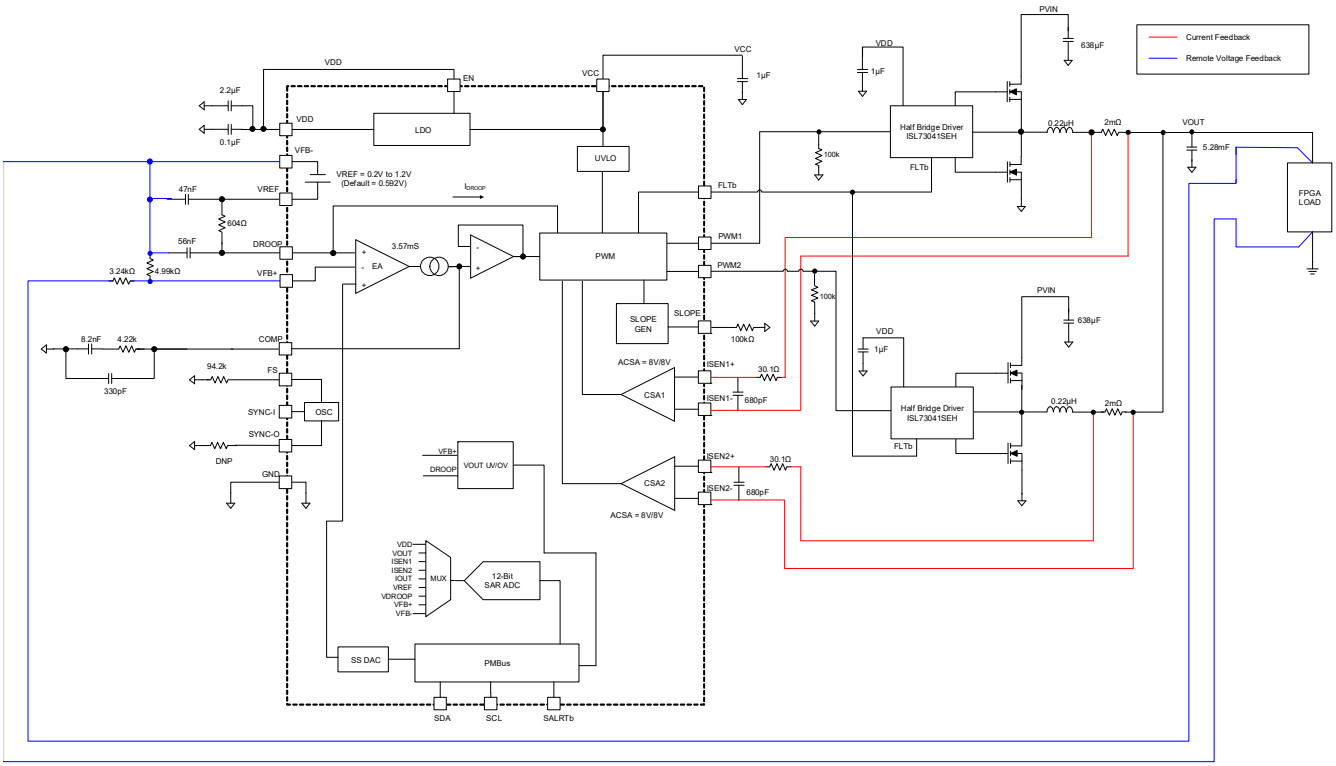


Figure 4. Typical Application (Dual-Phase) using Two ISL73041SEH Half-Bridge Drivers

1.2 Functional Block Diagram

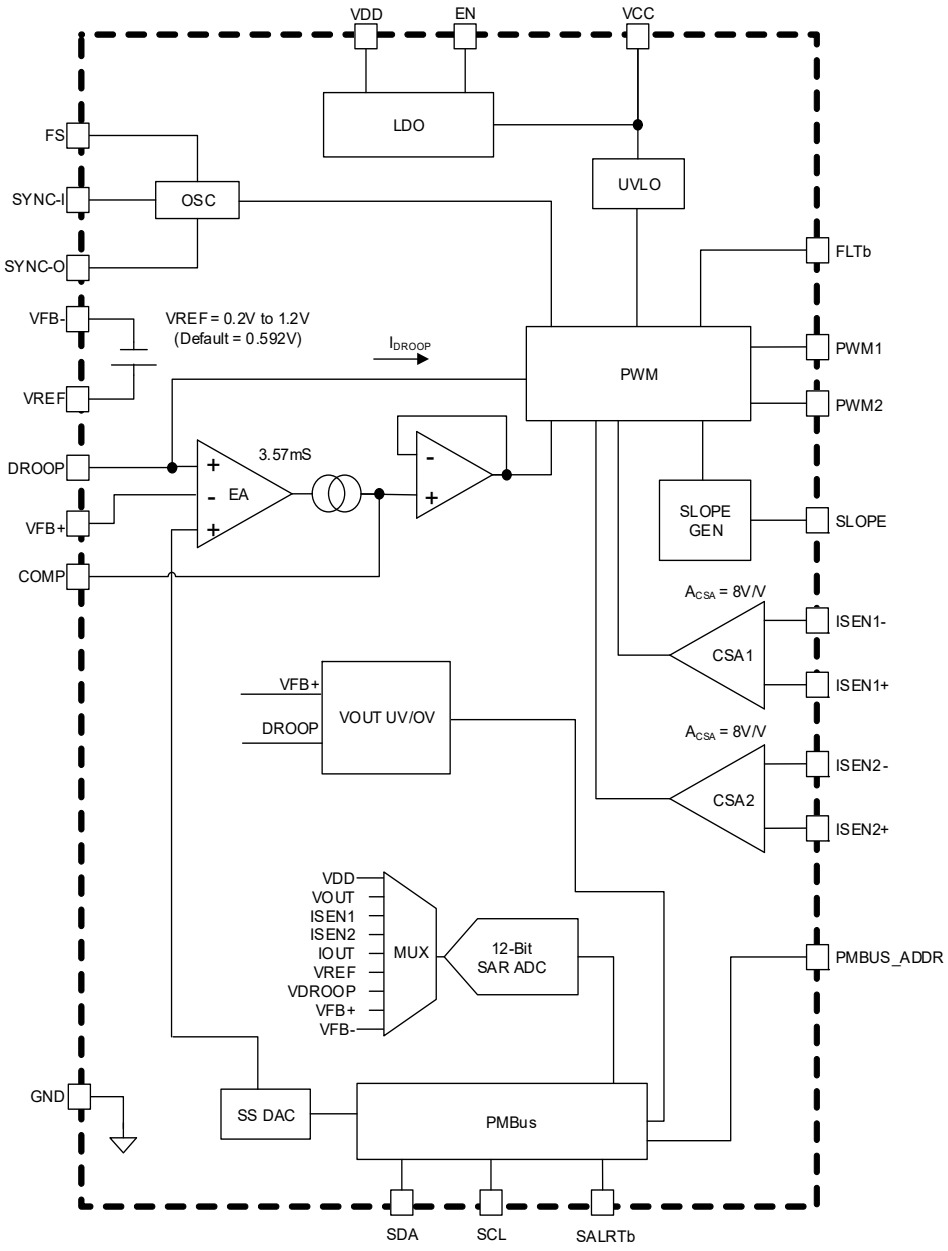


Figure 5. Block Diagram

2. Pin Information

2.1 Pin Assignments

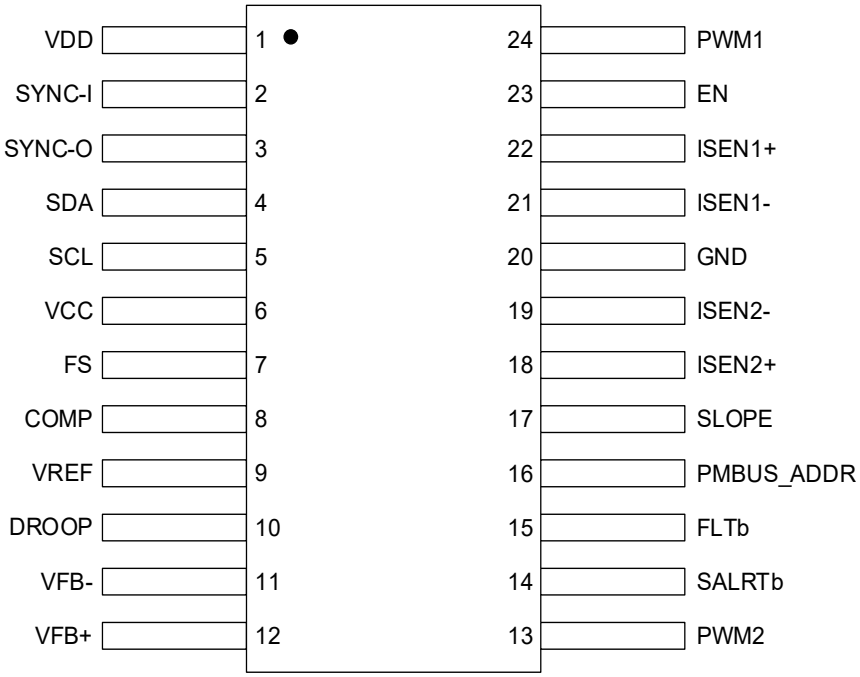


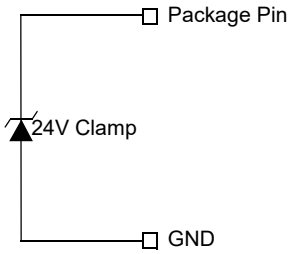
Figure 6. Pin Assignments 24Ld CDFP - Top View

2.2 Pin Descriptions

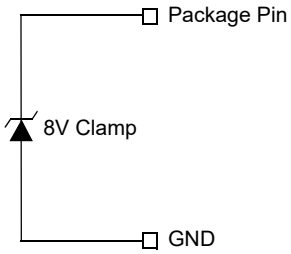
Pin Number	Pin Name	ESD Circuit	Description
1	VDD	1	The power supply input to the IC. The voltage range on this pin is 4.5V to 19V. Connect a 2.2µF and a 0.1µF ceramic capacitor from this pin to GND.
2	SYNC-I	2	This pin is an input that accepts 2x the required output switching frequency (regardless of single or dual phase). Internally the IC divides the clock down to get 2 clocks 180° from each other for each phase. *Note:* This pin has an internal pull-down, leave it floating if the SYNC function is not needed.
3	SYNC-O	2	This pin can output either 1x or 2x the output switching frequency depending on the loading present on the pin during power up (before soft start). When outputting 1x, the SYNC-O is 180° out of phase with phase 1 clock. The 2x SYNC-O output is in phase with the SYNC-I. ▪ Floating or 100kΩ to VCC: SYNC-O outputs 1x output switching frequency ▪ 100kΩ to GND: SYNC-O outputs 2x output switching frequency
4	SDA	2	PMBus Serial Data Bus
5	SCL	2	PMBus Serial Data Clock
6	VCC	2	5V Output of internal LDO for analog circuitry. Connect a 1µF ceramic capacitor from this pin to GND.
7	FS	2	This pin sets the frequency for the internal oscillator between 0.5MHz and 3MHz. This sets the PWM outputs between 0.25 MHz and 1.5MHz for each phase. When FS is tied to VCC the oscillator switching frequency (f_{OSC}) is 1MHz. To adjust the PWM outputs between 0.25MHz and 1.5MHz, use a 13.7kΩ to 205kΩ resistor between FS and GND. If SYNC-I is being used to sync to an external clock, FS must be set to a frequency 15% less than the external clock. Use Equation 4 to find which resistor value is needed for a specific frequency.
8	COMP	2	The output of error amplifier. Connect a resistor and capacitor in series to ground for type-2 compensation adjustment. For type-3 compensation add an additional capacitor in parallel with the type-2 series RC components.

Pin Number	Pin Name	ESD Circuit	Description
9	VREF	2	Output for the internal voltage reference. Connect a resistor between VREF and DROOP to enable droop regulation. Otherwise to disable droop regulation, short the VREF and DROOP pins together. Connect a 47nF ceramic capacitor from this pin to GND.
10	DROOP	2	This pin is a current mirrored version of the output of the current-sense amplifier output (sum of both phases). This output can be tied to the VREF pin through a resistor to enable droop regulation. The voltage created by the mirrored current and the resistor between VREF and DROOP sets the droop level.
11	VFB-	3	This pin is the negative input for differential voltage feedback.
12	VFB+	5	This pin is the positive input for differential voltage feedback.
13	PWM2	2	This pin is the PWM output for the secondary phase. Place a 100kΩ to GND on this pin.
14	SALRTb	2	This pin serves as the SALRTb pin for the PMBus. Pull up this pin to maximum of 5.5V via 10kΩ.
15	FLTb	2	This pin is used to sequence the startup between the ISL73849SLH and compatible drivers. On the ISL73849SLH, this pin operates as a bi-directional I/O during power up (before soft start) and as an input while switching (during and after soft start). A logic LOW on this pin indicates that either the ISL73849SLH or driver has encountered a fault or is not ready to start switching. A logic HIGH indicates that there is no faults for either device. Because FLTb is an open-drain output, use a 4.99kΩ typical pull-up resistor to VCC for a proper HIGH level.
16	PMBUS_ ADDR	2	This pin sets six unique PMBus addresses. When the PMBUS_ADDR pin is tied to GND, it is 0x11. The remaining addresses are set by using a resistor to GND: 0x12 (37.5kΩ), 0x13 (112.5kΩ), 0x14 (62.5kΩ), 0x16 (150kΩ) or 0x18 (87.5kΩ).
17	SLOPE	2	This pin is used to adjust the slope compensation of the ISL73849SLH. Place a resistor in the range of 25kΩ to 100kΩ to adjust slope compensation.
18	ISEN2+	4	This pin is the positive input for the secondary phase current-sense amplifier.
19	ISEN2-	1	This pin is the negative input for the secondary phase current-sense amplifier.
20	GND	-	This is the ground reference for the ISL73849SLH. This pin is tied to the package seal ring (lid).
21	ISEN1-	4	This pin is the negative input for the primary phase current-sense amplifier.
22	ISEN1+	1	This pin is the positive input for the primary phase current-sense amplifier.
23	EN	1	This pin is the chip enable for the ISL73849SLH.
24	PWM1	2	This pin is the PWM output for the primary phase. Place a 100kΩ to GND on this pin.

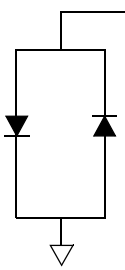
Pin Number	Pin Name	ESD Circuit	Description
-	Lid	-	The lid is electrically connected to pin 20 (GND).



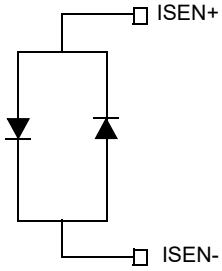
Circuit 1



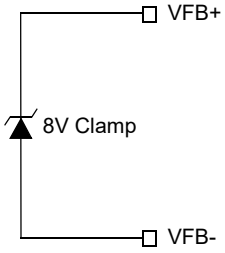
Circuit 2



Circuit 3



Circuit 4



Circuit 5

3. Specifications

3.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
VDD, ISENSx, EN	GND - 0.3	GND + 20.0	V
VDD, EN[1]	GND - 0.3	GND + 20.0	V
ISENSx[1]	GND - 0.3	GND + 13.5	V
VCC, SALRTb, SDA, SCL, FLTb	GND - 0.3	+6.5	V
VCC[1]	GND - 0.3	+6.3	V
VREF, DROOP, VFB+, VFB-, FS, COMP, SLOPE	GND - 0.3	VCC + 0.3	V
PWM1, PWM2, SYNC-I, SYNC-O	GND - 0.3	VCC + 0.3	V
Differential Voltage Across Current-Sense Inputs V(ISENx+) - V(ISENx-)[2]	-0.3	+0.3	V
Junction Temperature	-55	+150	°C
Storage Temperature	-65	+150	°C
Human Body Model (Tested per MIL-STD-883 TM3015.7)	-	2000	V
Charged Device Model (Tested per JS-002-2022)	-	750	V
Latch-Up (Tested per JESD78F; Class 2, Level A)	-	±100	mA

1. Tested under a heavy ion environment at LET = 86MeV•cm^2/mg at 125°C (T_C) for Single Event Burnout (SEB). Refer to the SEE Test Report for more details.
2. Maximum current through anti-parallel diodes show be ≤10mA.

3.2 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
VDD, EN	+4.5	+19	V
FLTb, SALRTb, SDA, SCL	GND	+5.5	V
SYNC-I, SYNC-O	GND	VCC	V
ISENx Common Mode Range	GND	19.0	V
Differential Voltage Across Current-Sense Inputs V(ISENx+) - V(ISENx-)	-83	111	mV
VCC	-	Limited by VCC dropout	V
PWM Output Switching Frequency	0.25	1.5	MHz
Regulated Output Voltage	VREF	PVIN×((T_{SW}-107ns)/T_{SW})	V
Ambient Temperature	-55	+125	°C

3.3 Thermal Specifications

Parameter	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance	24pin Ceramic Flatpack (CDFP) Package K24.B	θ_{JA}[1]	Junction to ambient	19.8	°C/W
		θ_{JC}[2]	Junction to case	0.9	°C/W

1. θ_{JA} is measured in free air with the component's ceramic base mounted with epoxy on a high-effective thermal conductivity test board with direct features. See TB379.
2. For θ_{JC}, the case temperature location is the center of the package underside.

3.4 Electrical Specifications

V_{DD} = 4.5V and 19V, EN = 3.3V, VREF = Float, DROOP = VFB+ = 0.6V, VFB- = 0V, C_{VREF} = 0.047µF, FS tied to VCC, FLTb = 5V, SYNC-I = 0V, SYNC-O = Float, PWM1 and PWM2 = Float, and T_A = +25°C; unless otherwise specified. **Boldface limits apply across the operating temperature range, -55°C to +125°C by production testing; over a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s.**

Parameter	Symbol	Test Conditions	Temp. (°C)	Min	Typ[1]	Max	Unit
Input Power Supply							
Supply Voltage Range	V_{DD}	-	-55 to +125	**4.5**	-	**19**	V
Rising VDD UVLO	$VDD_{UV(R)}$	EN = 3.3V	-55 to +125	**4.05**	4.2	**4.40**	V
Falling VDD UVLO	$VDD_{UV(F)}$	EN = 3.3V	-55 to +125	**3.85**	4.0	**4.10**	V
VDD UVLO Hysteresis	$VDD_{UV(HYS)}$	EN = 3.3V	-55 to +125	**150**	220	**300**	mV
Operating Supply Current	I_{DDO}	VDD = 4.5V, 12V, 19V EN = 3.3V, f_{SW} = 500kHz, C_L = 100pF	-55 to +125	**18**	22	**25**	mA
Shutdown Supply Current	I_{DDSD}	VDD = 19V, EN = GND	-55 to +125	-	11	**35**	µA
Internal LDO							
Output Range	V_{CC}	VDD = 6.0V, 19V I_{OUT} = 0mA, 20mA	-55 to +125	**4.7**	5.0	**5.3**	V
Dropout Voltage	VCC_{DO}	VDD = 4.5V, I_{OUT} = 50mA	-55 to +125	**85**	306	**476**	mV
Rising VCC UVLO	$VCC_{UV(R)}$	EN = 3.3V	-55 to +125	**3.39**	3.6	**3.70**	V
Falling VCC UVLO	$VCC_{UV(F)}$	EN = 3.3V	-55 to +125	**3.2**	3.3	**3.5**	V
VCC UVLO Hysteresis	$VCC_{UV(HYS)}$	EN = 3.3V	-55 to +125	**124**	202	**300**	mV
VCC Foldback Current	I_{CC-SC}	VDD = 19V, VCC = 0V, EN = 1.6V	-55 to +125	**40**	72	**90**	mA
VCC Overcurrent Limit	I_{CC-CL}	VDD = 19V, VCC = 4.3V, EN = 1.6V	-55 to +125	**75**	109	**135**	mA
Output Regulation							
Set Point Voltage[2]	VFB+	VREF = VDROOP VSEN1 = VSEN2 = 0mV, 50mV VOUT_COMMAND (21h) PMBus command set to 25dec for 0.2V	-55	0.196	0.2	0.206	V
			+25	0.195	0.2	0.205	V
			+125	0.193	0.2	0.203	V
			+25 (Post Rad)	0.190	0.2	0.206	V
		VREF = VDROOP VSEN1 = VSEN2 = 0mV, 50mV VOUT_COMMAND (21h) PMBus command left at default 74dec for 0.592V on power up or enable	-55	0.585	0.590	0.595	V
			+25	0.587	0.591	0.595	V
			+125	0.582	0.587	0.593	V
			+25 (Post Rad)	0.581	0.590	0.597	V
		VREF = VDROOP VSEN1 = VSEN2 = 0mV, 50mV VOUT_COMMAND (21h) PMBus command set to 75dec for 0.6V	-55	0.593	0.598	0.604	V
			+25	0.595	0.599	0.603	V
			+125	0.590	0.596	0.601	V
			+25 (Post Rad)	0.590	0.599	0.605	V
		VREF = VDROOP VSEN1 = VSEN2 = 0mV, 50mV VOUT_COMMAND (21h) PMBus command set to 150dec for 1.2V	-55	1.190	1.2	1.204	V
			+25	1.195	1.2	1.206	V
			+125	1.187	1.2	1.204	V
			+25 (Post Rad)	1.190	1.2	1.207	V
Set Point Accuracy Over Line Delta[2]	VFB+	VREF = VDROOP VSEN1 = VSEN2 = 0mV	-55 to +125	**-3.19**	0.2	**2.43**	mV

V_{DD} = 4.5V and 19V, EN = 3.3V, VREF = Float, DROOP = VFB+ = 0.6V, VFB- = 0V, C_{VREF} = 0.047µF, FS tied to VCC, FLTb = 5V, SYNC-I = 0V, SYNC-O = Float, PWM1 and PWM2 = Float, and T_A = +25°C; unless otherwise specified. **Boldface limits apply across the operating temperature range, -55°C to +125°C by production testing; over a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s. (Cont.)**

Parameter	Symbol	Test Conditions	Temp. (°C)	Min	Typ[1]	Max	Unit
Set Point Accuracy Over Load Delta[2]	VFB+	VREF = VDROOP VSEN1 = VSEN2 = 0mV, 50mV	-55 to +125	**-2.20**	0.53	**3.57**	mV
FB Input Bias Current Positive	$I_{FB-BIAS-P}$	V(FB+) = 0.6V, V(FB-) = 0V	-55 to +125	**-50**	-0.73	**50**	nA
FB Input Bias Current Negative	$I_{FB-BIAS-N}$	V(FB+) = 0.6V, V(FB-) = 0V	-55 to +125	**388**	449	**499**	µA
Soft-Start Time	T_{SS}	Time for the internal SS node to reach 0.9V when VREF = VDROOP = 0.6V. SS_CONFIG (E5h) PMBus command left at default 011b for 8ms on power-up and enable	-55 to +125	**7**	8	**10**	ms
VOUT Transition	-	Time for VREF = VDROOP to transition from 0.2V to 0.8V. Measurement is taken at 0.4V to 0.6V. VOUT_TRANSITION_RATE (27h) PMBus command left at default 100b on power-up and enable.	-55 to +125	**164**	201	**240**	mV/ms
Protection Features							
Peak Positive Current Limit	V_{POC1}	V_{CM} = 0.6V, 19V, OC_TH (E1h) PMBus command set to 000b	-55 to +125	**62.0**	72	**82.5**	mV
		V_{CM} = 0.6V, 19V, OC_TH (E1h) PMBus command set to 001b		**67.0**	77	**86.9**	
		V_{CM} = 0.6V, 19V, OC_TH (E1h) PMBus command set to 010b		**71.9**	82	**92.6**	
		V_{CM} = 0.6V, 19V, OC_TH (E1h) PMBus command set to 011b		**78.4**	88	**98.4**	
		V_{CM} = 0.6V, 19V, OC_TH (E1h) PMBus command set to 100b		**26.0**	35	**44.6**	
		V_{CM} = 0.6V, 19V, OC_TH (E1h) PMBus command set to 101b		**28.4**	37.5	**46.9**	
		V_{CM} = 0.6V, 19V, OC_TH (E1h) PMBus command set to 110b		**30.5**	40	**49.8**	
		V_{CM} = 0.6V, 19V, OC_TH (E1h) PMBus command set to 111b		**33.7**	43	**52.7**	
Peak Positive Overcurrent	V_{POC2}	V_{CM} = 0.6V, 19V, OC_TH (E1h) PMBus command set to 000b-011b	-55 to +125	**83.9**	97	**111**	mV
		V_{CM} = 0.6V, 19V, OC_TH (E1h) PMBus command set to 100b-111b		**35.9**	47	**60.2**	

V_{DD} = 4.5V and 19V, EN = 3.3V, VREF = Float, DROOP = VFB+ = 0.6V, VFB- = 0V, C_{VREF} = 0.047µF, FS tied to VCC, FLTb = 5V, SYNC-I = 0V, SYNC-O = Float, PWM1 and PWM2 = Float, and T_A = +25°C; unless otherwise specified. **Boldface limits apply across the operating temperature range, -55°C to +125°C by production testing; over a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s. (Cont.)**

Parameter	Symbol	Test Conditions	Temp. (°C)	Min	Typ[1]	Max	Unit
Peak Negative Overcurrent	V_{NOC}	V_{CM} = 0.6V, 19V, OC_TH (E1h) PMBus command set to 000b-011b	-55 to +125	**-83**	-72.7	**-61.7**	mV
		V_{CM} = 0.6V, 19V, OC_TH (E1h) PMBus command set to 100b-111b		**-47.5**	-35.1	**-23.0**	
Overvoltage Threshold Rising	$V_{(FB, OV)}$	VOUT_OV_LIMIT (E3h) PMBus command left at default 010b for 110% on power-up and enable	-55 to +125	**107**	110	**113**	%
Overvoltage Threshold Falling	$V_{(FB, OV)}$	VOUT_OV_LIMIT (E3h) PMBus command left at default 010b for 110% on power-up and enable	-55 to +125	**105**	107	**113**	%
Overvoltage Threshold Hysteresis	$V_{(FB, OV)}$	VOUT_OV_LIMIT (E3h) PMBus command left at default 010b for 110% on power-up and enable	-55 to +125	**1.4**	2.5	**3.6**	%
Overvoltage Severe Threshold	$V_{(FB, OV)}$	Internally set to 135% of VDROOP	-55 to +125	-	135	-	%
Undervoltage Threshold Rising	$V_{(FB, UV)}$	VOUT_UV_LIMIT (E4h) PMBus command left at default 101b for 90% on power-up and enable	-55 to +125	**87**	90	**93**	%
Undervoltage Threshold Falling	$V_{(FB, UV)}$	VOUT_UV_LIMIT (E4h) PMBus command left at default 101b for 90% on power-up and enable	-55 to +125	**87**	93	**95**	%
Undervoltage Threshold Hysteresis	$V_{(FB, UV)}$	VOUT_UV_LIMIT (E4h) PMBus command left at default 101b for 90% on power-up and enable	-55 to +125	**1.46**	2.6	**3.70**	%
Undervoltage Threshold Severe	$V_{(FB, UV)}$	Internally set to 65% of VDROOP	-55 to +125	-	65	-	%
UV/OV/Severe Propagation Delay	$t_{DEGLITCH}$	V(FB+, FB-) = 0.6V + Pulse to initiate the Severe UV/OV fault condition Measure the delay from fault to PWMx going mid-scale.	-55 to +125	**8**	11	**16**	µs
Hiccup Retry Delay	$t_{HIC-DLY}$	SS_CONFIG (E5h) PMBus command at default 011b for 8ms on power-up and enable.	-55 to +125	**9.6**	11	**14.0**	ms
FLTb Drive Current	I_{FLTb}	FLTb = 400mV	-55 to +125	**20**	50	**75**	mA
FLTb Rising Threshold Voltage	$V_{FLTbMID}$		-55 to +125	**2.4**	2.9	**3.3**	V
FLTb Falling Threshold Voltage	$V_{FLTbMID}$		-55 to +125	**1.6**	2.08	**2.55**	V
FLTb Leakage Current	$V_{FLTbLKG}$	FLTb = 5V	-55 to +125	**-2**	0	**2**	µA

V_{DD} = 4.5V and 19V, EN = 3.3V, VREF = Float, DROOP = VFB+ = 0.6V, VFB- = 0V, C_{VREF} = 0.047µF, FS tied to VCC, FLTb = 5V, SYNC-I = 0V, SYNC-O = Float, PWM1 and PWM2 = Float, and T_A = +25°C; unless otherwise specified. **Boldface limits apply across the operating temperature range, -55°C to +125°C by production testing; over a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s. (Cont.)**

Parameter	Symbol	Test Conditions	Temp. (°C)	Min	Typ[1]	Max	Unit
Error Amplifier							
Transconductance	g_{m-EA}	-	-55	3	4.1	4.5	mA/V
			+25	3	3.57	4	mA/V
			+125	2.5	3.04	3.5	mA/V
			+25 (Post Rad)	3	3.6	4	mA/V
DC Gain[3]	A_{V-EA}	-	-55 to +125	**66**	80	-	dB
Gain-Bandwidth Product[3]	GBW_{EA}	-		**15**	-	-	MHz
Output Voltage Range	$V_{COMP(RNG)}$	VDD = 4.5V		**0.4**	-	**4.1**	V
Output Voltage Range	$V_{COMP(RNG)}$	VDD = 19V		**0.4**	-	**4.6**	V
Output Slew Rate[3]	SR_{EA}			-	8.5	-	V/µs
Current-Sense Amplifier							
Droop Transconductance	$g_{m(CSA, DRP)}$	V(ISEN+ - ISEN-) = 10mV, 50mV V_{CM} = 0.6V, 19V DROOP = 0.6V	-55	0.369	0.399	0.436	µA/mV
			+25	0.372	0.400	0.425	
			+125	0.367	0.394	0.419	
			+25 (Post Rad)	0.364	0.396	0.424	
		V(ISEN+ - ISEN-) = 10mV, 50mV V_{CM} = 0.6V, 19V DROOP = 0.2V	-55	0.342	0.374	0.407	µA/mV
			+25	0.337	0.367	0.400	
			+125	0.304	0.340	0.385	
			+25 (Post Rad)	0.314	0.359	0.400	
		V(ISEN+ - ISEN-) =10mV, 50mV V_{CM} = 0.6V, 19V DROOP = 0.5V	-55	0.336	0.396	0.455	µA/mV
			+25	0.338	0.396	0.455	
			+125	0.340	0.393	0.445	
			+25 (Post Rad)	0.328	0.395	0.454	
		V(ISEN+ - ISEN-) =10mV, 50mV V_{CM} = 0.6V, 19V DROOP = 1.2V	-55	0.350	0.401	0.449	µA/mV
			+25	0.352	0.403	0.449	
			+125	0.346	0.397	0.442	
			+25 (Post Rad)	0.353	0.400	0.444	

V_{DD} = 4.5V and 19V, EN = 3.3V, VREF = Float, DROOP = VFB+ = 0.6V, VFB- = 0V, C_{VREF} = 0.047µF, FS tied to VCC, FLTb = 5V, SYNC-I = 0V, SYNC-O = Float, PWM1 and PWM2 = Float, and T_A = +25°C; unless otherwise specified. **Boldface limits apply across the operating temperature range, -55°C to +125°C by production testing; over a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s. (Cont.)**

Parameter	Symbol	Test Conditions	Temp. (°C)	Min	Typ[1]	Max	Unit
Droop Offset (Phase 1)	$Offset_{DRP}$	V(ISEN+,ISEN-) = 0mV, V_{CM} = 0.6V, 19V, DROOP = 0.6V	-55	-5.22	-0.07	4.87	µA
			+25	-3.73	-0.05	3.58	
			+125	-4.83	-0.21	4.32	
			+25 (Post Rad)	-10.83	-0.85	9.31	
		V(ISEN+,ISEN-) = 0mV, V_{CM} = 0.6V, 19V, DROOP = 0.2V	-55	-6.37	-1.6	3.27	µA
			+25	-5.69	-1.68	2.31	
			+125	-6.30	-2.17	2.09	
			+25 (Post Rad)	-11.88	-2.46	7.37	
		V(ISEN+,ISEN-) = 0mV, V_{CM} = 0.6V, 19V, DROOP = 0.5V	-55	-5.28	-0.26	4.78	µA
			+25	-4.33	-0.28	3.82	
			+125	-4.77	-0.38	4.08	
			+25 (Post Rad)	-10.78	-1.18	9.08	
		V(ISEN+,ISEN-) = 0mV, V_{CM} = 0.6V, 19V, DROOP = 1.2V	-55	-5.05	0.06	5.11	µA
			+25	-4.08	0.02	4.12	
			+125	-4.49	-0.04	4.44	
			+25 (Post Rad)	-10.5	-0.84	9.44	
Droop Offset (Phase 2)	$Offset_{DRP}$	V(ISEN+,ISEN-) = 0mV, V_{CM} = 0.6V, 19V, DROOP = 0.6V	-55	-4.83	0.16	5.11	µA
			+25	-3.58	0.08	3.78	
			+125	-4.04	-0.01	3.97	
			+25 (Post Rad)	-8.30	0.97	10.23	
		V(ISEN+,ISEN-) = 0mV, V_{CM} = 0.6V, 19V, DROOP = 0.2V	-55	-5.98	-1.31	3.50	µA
			+25	-5.39	-1.53	2.53	
			+125	-6.30	-2.12	2.37	
			+25 (Post Rad)	-10.81	-1.02	8.48	
		V(ISEN+,ISEN-) = 0mV, V_{CM} = 0.6V, 19V, DROOP = 0.5V	-55	-4.76	0.05	4.90	µA
			+25	-4.12	-0.09	3.98	
			+125	-4.83	-0.24	4.34	
			+25 (Post Rad)	-9.74	0.62	10.69	
		V(ISEN+,ISEN-) = 0mV, V_{CM} = 0.6V, 19V, DROOP = 1.2V	-55	-4.51	0.37	5.18	µA
			+25	-3.89	0.22	4.28	
			+125	-4.58	0.11	4.74	
			+25 (Post Rad)	-9.41	0.98	11.1	

V_{DD} = 4.5V and 19V, EN = 3.3V, VREF = Float, DROOP = VFB+ = 0.6V, VFB- = 0V, C_{VREF} = 0.047µF, FS tied to VCC, FLTb = 5V, SYNC-I = 0V, SYNC-O = Float, PWM1 and PWM2 = Float, and T_A = +25°C; unless otherwise specified. **Boldface limits apply across the operating temperature range, -55°C to +125°C by production testing; over a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s. (Cont.)**

Parameter	Symbol	Test Conditions	Temp. (°C)	Min	Typ[1]	Max	Unit
Droop Offset (Both Phases)	$Offset_{DRP}$	V(ISEN+,ISEN-) = 0mV, V_{CM} = 0.6V, 19V, DROOP = 0.6V	-55	-3.72	0.14	4.03	µA
			+25	-2.21	0.02	2.27	
			+125	-4.09	-0.19	3.79	
			+25 (Post Rad)	-9.2	0.29	7.5	
		V(ISEN+,ISEN-) = 0mV, V_{CM} = 0.6V, 19V, DROOP = 0.2V	-55	-6.35	-2.91	0.83	µA
			+25	-4.94	-3.21	-1.00	
			+125	-7.8	-4.23	-0.08	
			+25 (Post Rad)	-12.5	-3.36	4.50	
		V(ISEN+,ISEN-) = 0mV, V_{CM} = 0.6V, 19V, DROOP = 0.5V	-55	-3.92	-0.22	3.48	µA
			+25	-2.25	-0.38	1.59	
			+125	-4.67	-0.63	3.43	
			+25 (Post Rad)	-9.5	-0.36	7.0	
		V(ISEN+,ISEN-) = 0mV, V_{CM} = 0.6V, 19V, DROOP = 1.2V	-55	-3.30	0.42	4.16	µA
			+25	-1.65	0.24	2.23	
			+125	-4.01	0.06	4.13	
			+25 (Post Rad)	-9.0	0.32	8.0	
Gain from CSA Input to PWM Comparator Input	$A_{CSA-PWM}$	V(ISEN+, ISEN-) = 50mV	-55 to +125	**7.0**	8	**8.76**	mV/mV
Offset Voltage	$V_{OS(CSA)}$	V(ISEN+ - ISEN-) = 0mV V_{CM} = 0.6V, 19V	-55	-5.5	-0.34	4.78	mV
			+25	-2.87	-0.12	2.63	
			+125	-5.02	0.06	5.03	
			+25 (Post Rad)	-12	0.01	12	
Positive Input Leakage Current	$I_{LKG+(CSA)}$	EN = 0V, V_{CM} = 0.6V, 19V	-55 to +125	**-50**	4	**50**	nA
Negative Input Leakage Current	$I_{LKG-(CSA)}$	EN = 0V, V_{CM} = 0.6V	-55 to +125	-	-	**205**	nA
		EN = 0V, V_{CM} = 19V	-55 to +125	-	-	**2**	µA
HS CSA Supply Current per Phase (Current into ISENx- pin)	I_{CSA}	EN = 5V, V_{CM} = 2.7V	-55 to +125	-	13	**20**	µA
HS CSA Supply Current	I_{CSA}	EN = 5V, V_{CM} = 6V, VDD = 19V, V(ISEN+ - ISEN-) = 50mV	-55 to +125	**535**	643	**747**	µA
Transition from Low Side to High Side	$V_{CS(TRAN)}$	VDD = 4.5V	-55 to +125	**1.94**	2.11	**2.55**	V
Transition from Low Side to High Side	$V_{CS(TRAN)}$	VDD = 19V	-55 to +125	**2.2**	2.4	**2.55**	V
Gain-Bandwidth Product[3]	GBW_{CSA}	-	-55 to +125	**10**	-	-	MHz

V_{DD} = 4.5V and 19V, EN = 3.3V, VREF = Float, DROOP = VFB+ = 0.6V, VFB- = 0V, C_{VREF} = 0.047µF, FS tied to VCC, FLTb = 5V, SYNC-I = 0V, SYNC-O = Float, PWM1 and PWM2 = Float, and T_A = +25°C; unless otherwise specified. **Boldface limits apply across the operating temperature range, -55°C to +125°C by production testing; over a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s. (Cont.)**

Parameter	Symbol	Test Conditions	Temp. (°C)	Min	Typ[1]	Max	Unit
Oscillator / Slope Generator							
Default Oscillator Frequency	f_{SW-D}	FS = VCC, VDD = 4.5V, 19V	-55 to +125	**0.90**	1.00	**1.10**	MHz
Oscillator Frequency Range	$f_{SW-0.5M}$	R_{FS} = 205kΩ, EN = 5V, R_{SYNC-O} = 100kΩ to GND		**0.45**	0.5	**0.55**	MHz
	f_{SW-1M}	R_{FS} = 94.2kΩ, EN = 5V, R_{SYNC-O} = 100kΩ to GND		**0.90**	1.00	**1.10**	MHz
	f_{SW-2M}	R_{FS} = 37kΩ, EN = 5V, R_{SYNC-O} = 100kΩ to GND		**1.80**	2.00	**2.20**	MHz
	f_{SW-3M}	R_{FS} = 16.7kΩ, EN = 5V, R_{SYNC-O} = 100kΩ to GND		**2.70**	3.00	**3.30**	MHz
Slope Pin Current	I_{SLOPE}	V_{SLOPE} = 400mV, VDD = 4.5V, 19V	-55 to +125	**11.2**	12	**12.6**	µA
Default Slope Compensation Reference Voltage	V_{SCMP_DFLT}	-	-55 to +125	**1.14**	1.2	**1.26**	V
Ramp Slope	$V_{RAMP-SLOPE}$	V_{SLOPE} = 1.2V, VDD = 19V	-55	0.110	0.214	0.317	V/µs
			+25	0.145	0.253	0.361	V/µs
			+125	0.155	0.252	0.344	V/µs
			+25 (Post Rad)	0.110	0.210	0.361	V/µs
Ramp Valley	$V_{RAMP-VLY}$	-	-55 to +125	-	1.2	-	V
Enable							
Rising Enable Threshold (Gross)	$V_{IH-EN-G}$	-	-55 to +125	**0.9**	1.3	**1.6**	V
Falling Enable Threshold (Gross)	$V_{IL-EN-G}$	-	-55 to +125	**0.6**	1.0	**1.2**	V
Enable Threshold Hysteresis (Gross)	$V_{HYS-EN-G}$	-	-55 to +125	**200**	363	**500**	mV
Rising Enable Threshold (Fine)	$V_{IH-EN-G}$	-	-55 to +125	**1.74**	1.8	**1.85**	V
Falling Enable Threshold (Fine)	$V_{IL-EN-G}$	-	-55 to +125	**1.46**	1.5	**1.54**	V
Enable Threshold Hysteresis (Fine)	$V_{HYS-EN-G}$	-	-55 to +125	**260**	299	**320**	mV
EN rising to Boot Refresh Delay	t_{EN}	-	-55 to +125	**3.5**	4.7	**5.5**	ms
EN Pull-Down Resistance	R_{EN}	EN = 19V	-55 to +125	-	1	-	MΩ
EN Leakage	EN_{LK}	VDD = EN = 19V	-55 to +125	-	120	**280**	nA
PWM Outputs							
PWM Output High	VOH	VDD = 4.5V, I_{PWM} = -500µA	-55 to +125	**4**	-	-	V
PWM Output High	VOH	VDD = 19V, I_{PWM} = -500µA	-55 to +125	**4.5**	-	-	V
PWM Output Mid	VOZ	I_{PWM} = ±10µA	-55 to +125	**1.8**	2.0	**2.4**	V
PWM Output Low	VOL	I_{PWM} = +500µA	-55 to +125	-	0.05	**0.4**	V
Turn-On Blanking Time	$t_{MINONBLK}$	-	-55 to +125	**79**	100	**123**	ns
Turn-Off Blanking Time	$t_{MINOFFBLK}$	-	-55 to +125	**87**	112	**141**	ns

V_{DD} = 4.5V and 19V, EN = 3.3V, VREF = Float, DROOP = VFB+ = 0.6V, VFB- = 0V, C_{VREF} = 0.047µF, FS tied to VCC, FLTb = 5V, SYNC-I = 0V, SYNC-O = Float, PWM1 and PWM2 = Float, and T_A = +25°C; unless otherwise specified. **Boldface limits apply across the operating temperature range, -55°C to +125°C by production testing; over a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s. (Cont.)**

Parameter	Symbol	Test Conditions	Temp. (°C)	Min	Typ[1]	Max	Unit
Minimum Controllable ON-Time	$t_{MINCTRLON}$	-	-55 to +125	**81**	97	**135**	ns
Minimum Controllable OFF-Time	$t_{MINCTRLOFF}$	-	-55 to +125	**87**	107	**135**	ns
Passive Pull-Down	$R_{PWM-PLDN}$	-	-55 to +125	-	5	-	MΩ
Current Share between Phase 1 & 2[3]	$I_{PHSHARE}$	V_{CM} = 1V, 5V	-55 to +125	**-4**	-	**4**	mV
Boot Refresh Repeat Timer	t_{BOOT}	-	-55 to +125	**62**	71	**80**	µs
SYNC							
SYNC-I Input Voltage High	V_{SYNCH}	-	-55 to +125	**1.41**	-	-	V
SYNC-I Input Voltage Low	V_{SYNCL}	-	-55 to +125	-	-	**0.8**	V
Min SYNC-I Frequency (Referred to Internal Oscillator)	$f_{SYNC-MIN}$	R_{FS} = 16.7kΩ. HF capacitor on f_{SW}	-55 to +125	**15**	-	-	%
SYNC-I Input Leakage Current	$I_{SYNC-IN-LK}$	V_{SYNC} = 5V, VDD = 19V	-55 to +125	**2.5**	5	**7.0**	µA
SYNC-O Output Voltage High	$V_{SYNC-OH}$	VDD = 4.5V, ISYNC-O = -500µA	-55 to +125	**4.2**	-	-	V
SYNC-O Output Voltage High	$V_{SYNC-OH}$	VDD=19V, SYNC-O = -500µA	-55 to +125	**4.6**	-	-	V
SYNC-O Output Voltage Low	$V_{SYNC-OL}$	ISYNC-O = +500µA	-55 to +125	-	-	**0.4**	V
SYNC-I to PWMx Delay	$t_{SYNC-I-DEL}$	-		-	270	-	ns
SYNC-O to PWMx Delay	$t_{SYNC-O-DEL}$	-		-	32	-	ns
SYNC-I to SYNC-O Delay	$t_{SYNC-DLY}$	50% of SYNC-I to 50% of SYNC-O	-55 to +125	**217**	242	**275**	ns
PWM1 to PWM2 Phase Shift	$t_{PWM1-PWM2}$	Phase shift from PWM1 to PWM2	-55 to +125	**175**	178	**185**	°
PMBus Interface (SCL and SDA Input Pins)							
SCL Logic Input Voltage High	SCL	-	-55 to +125	**1.35**	-	-	V
SCL Logic Input Voltage Low	SCL	-	-55 to +125	-	-	**0.4**	V
SCL Hysteresis	SCL	-	-55 to +125	-	0.2	-	V
SDA Logic Input Voltage High	SDA	-	-55 to +125	**1.35**	-	-	V
SDA Logic Input Voltage Low	SDA	-	-55 to +125	-	-	**0.4**	V
SDA Hysteresis	SDA	-	-55 to +125	-	0.2	-	V
SDA Output Voltage Low	-	I_{OUT} = -4mA	-55 to +125	-	0.1	**0.4**	V
Input Current	-	5V	-55 to +125	**-0.08**	0.163	**0.42**	µA
		0V		**-2.98**	-2.47	**-1.88**	

V_{DD} = 4.5V and 19V, EN = 3.3V, VREF = Float, DROOP = VFB+ = 0.6V, VFB- = 0V, C_{VREF} = 0.047µF, FS tied to VCC, FLTb = 5V, SYNC-I = 0V, SYNC-O = Float, PWM1 and PWM2 = Float, and T_A = +25°C; unless otherwise specified. **Boldface limits apply across the operating temperature range, -55°C to +125°C by production testing; over a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s. (Cont.)**

Parameter	Symbol	Test Conditions	Temp. (°C)	Min	Typ[1]	Max	Unit
Input Capacitance	-	-	-55 to +125	-	5		pF
Clock Frequency	-	-	-55 to +125	-	-	**400**	kHz
SCL Falling Edge to SDA Valid Time	-	PMBus Frequency = 400kHz	-55 to +125	**100**	222	**300**	ns
SALRTb Pin Output							
Output Voltage Low	-	I_{OUT} = -4mA	-55 to +125	-	0.1	**0.4**	V
Output High Leakage Current	-	V_{SALERT} = 5.0V	-55 to +125	-	0	**1**	µA
PMBUS_ADDR							
PMBUS_ADDR Source Current	-	EN < 1V	-55 to +125	**17.6**	20	**21.6**	µA
PMBUS_ADDR Resistance Range	-	PMBus ADDR = 0x11	-55 to +125	-	-	21.84	kΩ
		PMBus ADDR = 0x12		27.36	-	44.95	kΩ
		PMBus ADDR = 0x14		55.56	-	68.00	kΩ
		PMBus ADDR = 0x18		83.46	-	91.29	kΩ
		PMBus ADDR = 0x13		111.85	-	114.08	kΩ
		PMBus ADDR = 0x16		140.33	-	-	kΩ
Internal 8-Bit DAC							
Minimum Output Voltage	-	LSB = 8mV	-55 to +125	-	8	-	mV
Maximum Output Voltage	-	LSB = 8mV	-55 to +125	-	2.048	-	V
Internal 12-Bit ADC (Sampling Voltages of TEMP, VDD, VOUT, IOUT, ISENSE1, ISENSE2, VDROOP, VREF, VFB+)							
Minimum Input Voltage	-	LSB = 500µV	-55 to +125	-	500	-	µV
Maximum Input Voltage	-	LSB = 500µV	-55 to +125	-	2.048	-	V
Telemetry Reading Accuracy (VDD, VOUT, IOUT, ISENSE1, ISENSE2, VDROOP, VREF, VFB+, TEMP)							
VDD Telemetry	-	V_{DD} = 19V	+25	6.16	6.19	6.24	mV/LSB
			-55 to +125 (+25 Post Rad)	6.12		6.24	
VOUT Telemetry	-	V_{DD} = 19V, V_{OUT} = 19V, VOUT1 (Phase 2 disabled) and VOUT2 (Phase 1 disabled)	+25	6.13	6.19	6.26	mV/LSB
			-55 to +125 (+25 Post Rad)	6.09		6.26	
ISENSE1 Telemetry	-	V_{CM} = 0.6V, V_{DD} = 19V, VSEN = 75mV	+25	36.2	38.9	41.8	µV/LSB
			-55 to +125 (+25 Post Rad)	34.1		45.0	
ISENSE2 Telemetry	-	V_{CM} = 0.6V, V_{DD} = 19V, VSEN = 75mV	+25	36.4	38.9	42.0	µV/LSB
			-55 to +125 (+25 Post Rad)	33.8		43.7	
I_{OUT} Telemetry	-	V_{CM} = 0.6V, V_{DD} = 19V, VSEN = 75mV	+25	36.2	38.9	41.8	µV/LSB
			-55 to +125 (+25 Post Rad)	33.5		45.0	
VREF Telemetry	-	V_{DD} = 19V, VREF = 1.2V	+25	0.493	0.498	0.503	mV/LSB
			-55 to +125 (+25 Post Rad)	0.490		0.503	

V_{DD} = 4.5V and 19V, EN = 3.3V, VREF = Float, DROOP = VFB+ = 0.6V, VFB- = 0V, C_{VREF} = 0.047µF, FS tied to VCC, FLTb = 5V, SYNC-I = 0V, SYNC-O = Float, PWM1 and PWM2 = Float, and T_A = +25°C; unless otherwise specified. **Boldface limits apply across the operating temperature range, -55°C to +125°C by production testing; over a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s. (Cont.)**

Parameter	Symbol	Test Conditions	Temp. (°C)	Min	Typ[1]	Max	Unit
DROOP Telemetry	-	V_{DD} = 19V, DROOP = 1.2V	+25	0.493	0.498	0.503	mV/LSB
			-55 to +125 (+25 Post Rad)	0.491	-	0.503	
VFB+ Telemetry	-	V_{DD} = 19V, VFB+ = 1.2V	+25	0.493	0.497	0.502	mV/LSB
			-55 to +125 (+25 Post Rad)	0.489	-	0.502	
VFB- Telemetry	-	V_{DD} = 19V, VFB- = 100mV	+25	0.524	0.578	0.643	mV/LSB
			-55 to +125 (+25 Post Rad)	0.500	-	0.705	
FOSC Telemetry[4]	-	FOSC = 3MHz	+25	-20.96	64k/Telemetry Value	21.13	%
			-55 to +125 (+25 Post Rad)	-25.97		27.51	

1. Typical values are at 25°C and are not guaranteed.
2. This test is conducted in a closed loop circuit (as shown in Figure 7) and includes the error amplifier offset.
3. Limits established by characterization and/or design analysis and are not production tested.
4. The min/max variation includes the variation of the internal oscillator itself.

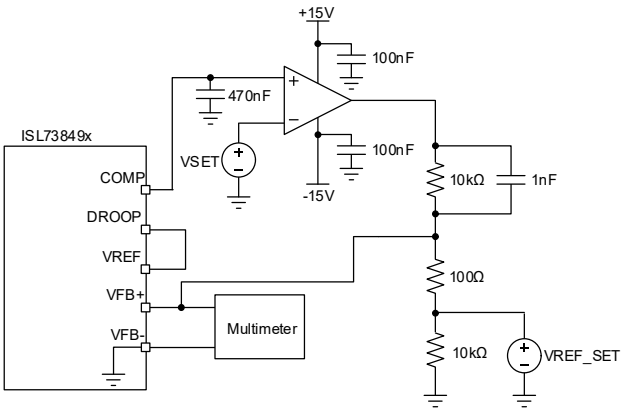


Figure 7. Closed-Loop Circuit

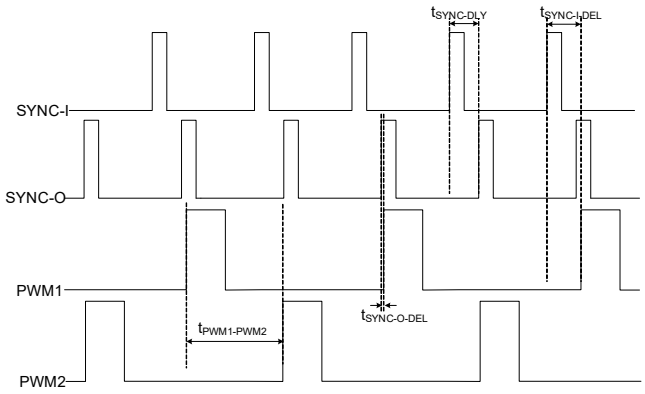


Figure 8. SYNC and PWM Timing

3.5 Operation Burn-In Deltas

Test Name	ATE Test Name	Min	Max	Unit
Shutdown Current 19V	Shutdown Current, 19V	-3.5	3.5	µA
Operating Current 19V	Operating Current, 19V	-1	1	mA
VCC Output Range VDD = 19V, I_{OUT} = 0mA	LDO Vout, 0mA, 19V	-0.15	0.15	V
VCC Dropout Voltage VDD = 4.5V, I_{OUT} = 50mA	LDO Dropout	10	10	mV
Setpoint Voltage, VDD = 19V, VREF = VDROOP = 600mV VSEN1 = VSEN2 = 0mV, 50mV	Setpoint Voltage 2V, 600mV, 19V	-3	3	mV
	Setpoint Voltage 1V, 600mV, 19V	-3	3	mV
	Setpoint Voltage 1V, 600mV,50mV, 19V	-3	3	mV
	Setpoint Voltage 2V, 600mV,50mV, 19V	-3	3	mV
Transconductance, gm-EA	EA Transconductance, 19V	-0.2	0.2	mA/V
PWM1Vol 19V	PWM1 Vol, 19V	-2	2	mV
PWM2Vol 19V	PWM2 Vol, 19V	-2	2	mV
Oscillator FS = VCC, 1.0MHz 19V	Osc FS 1M, 19V	-25	25	kHz

4. Typical Performance Graphs

4.1 General

Unless otherwise noted: V_{DD} = 4.5V and 19V, V_{OUT} = 1V, f_{SW} = 500kHz; L_{OUT}(XAL1010-221) = 220nH per phase, C_{OUT}(T530D227M010ATE006) = 2.64mF total per phase, C_{DROOP}= 56nF, C_{VREF} = 47nF, R_{DROOP} = 0Ω, FS tied to VCC, C_{COMP} = 8.2nF, R_{COMP} = 4.22kΩ, C_{POLE} = 330pF, C_{VCC} = 1µF, R_{SLOPE} = 100kΩ, R_{SENSE} = 2mΩ, RFIL=30.1Ω, C_{FIL} = 680pF, $R_{FB(TOP)}$ = 3.24kΩ, $R_{FB(BOT)}$ = 4.99kΩ

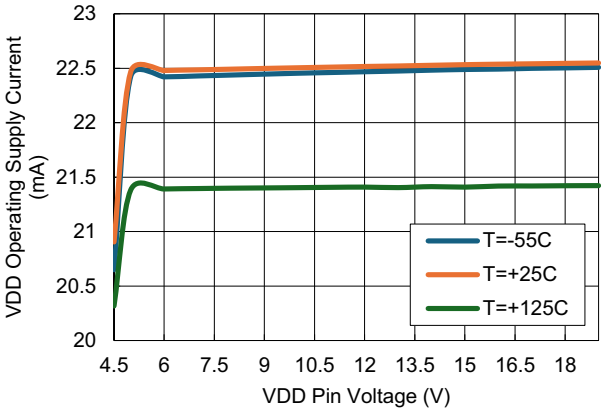


Figure 9. VDD Operating Supply Current (V_{EN} = 3.3V, f_{SW} = 500kHz, 100pF load on each PWM output)

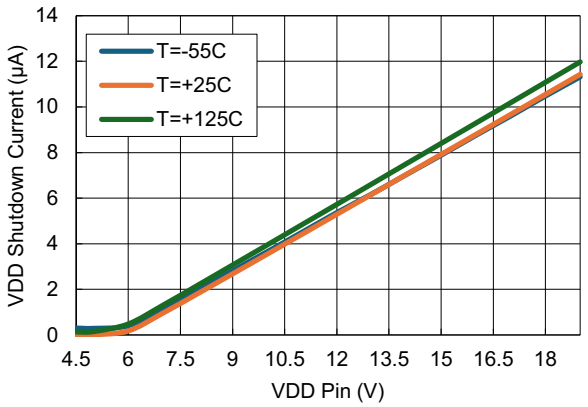


Figure 10. VDD Shutdown Current (V_{EN} = 0V, f_{SW} = 500kHz)

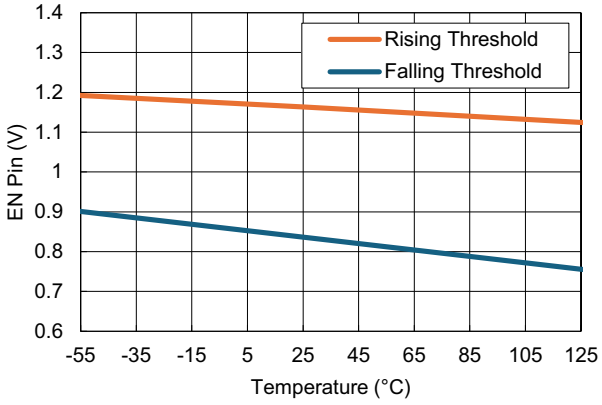


Figure 11. VEN Gross Thresholds vs Temperature (V_{DD} = 4.5V)

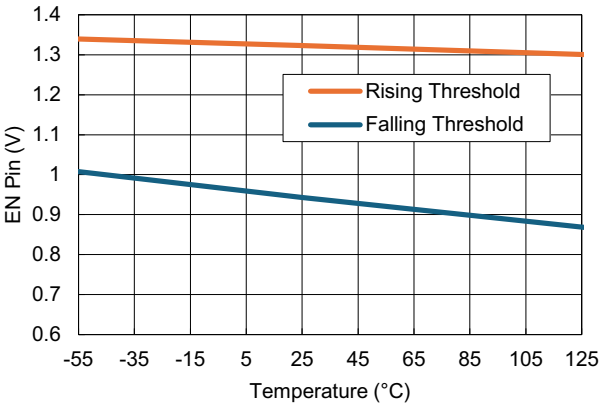


Figure 12. VEN Gross Thresholds vs Temperature (V_{DD} = 19V)

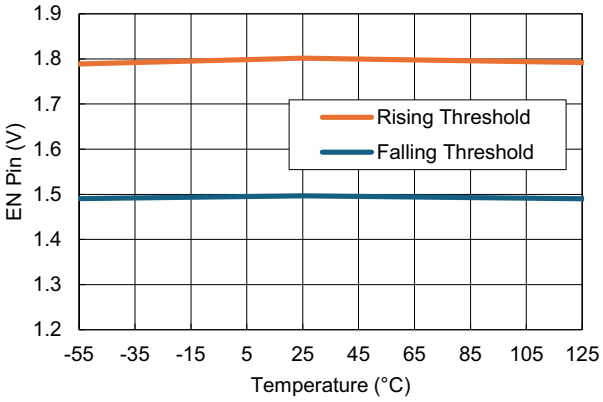


Figure 13. VEN Fine Thresholds vs Temperature

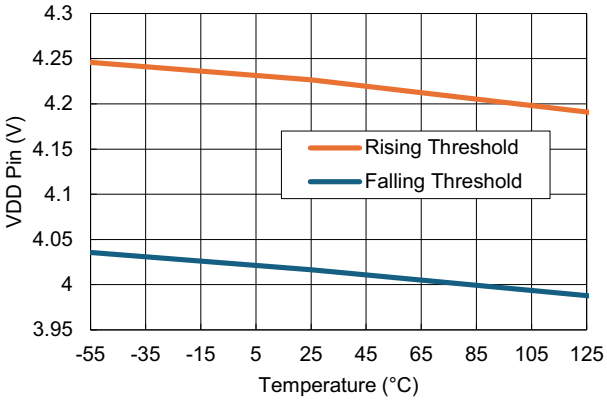


Figure 14. VDD UVLO Thresholds vs Temperature

Unless otherwise noted: V_{DD} = 4.5V and 19V, V_{OUT} = 1V, f_{SW} = 500kHz; L_{OUT}(XAL1010-221) = 220nH per phase, C_{OUT}(T530D227M010ATE006) = 2.64mF total per phase, C_{DROOP}= 56nF, C_{VREF} = 47nF, R_{DROOP} = 0Ω, FS tied to VCC, C_{COMP} = 8.2nF, R_{COMP} = 4.22kΩ, C_{POLE} = 330pF, C_{VCC} = 1µF, R_{SLOPE} = 100kΩ, R_{SENSE} = 2mΩ, RFIL=30.1Ω, C_{FIL} = 680pF, $R_{FB(TOP)}$ = 3.24kΩ, $R_{FB(BOT)}$ = 4.99kΩ (Cont.)

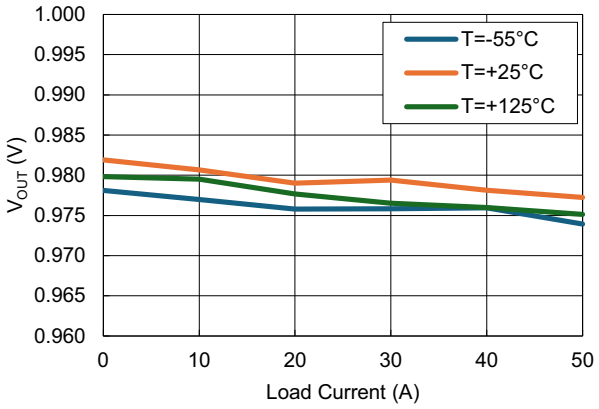


Figure 15. Load Regulation for Various Temperatures (V_{DD} = 5V, PVIN = 5V, V_{REF} = 0.6V)

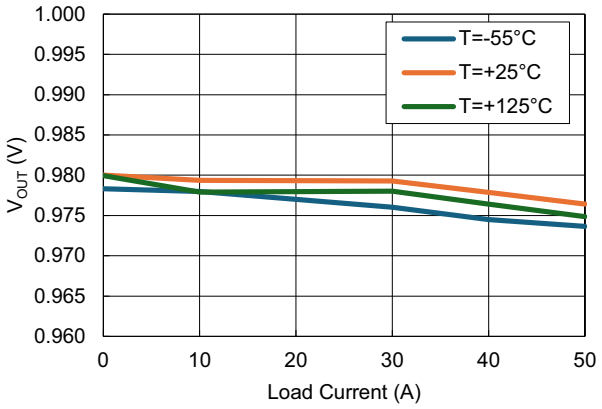


Figure 16. Load Regulation for Various Temperatures (V_{DD} = 12V, PVIN = 12V, V_{REF} = 0.6V)

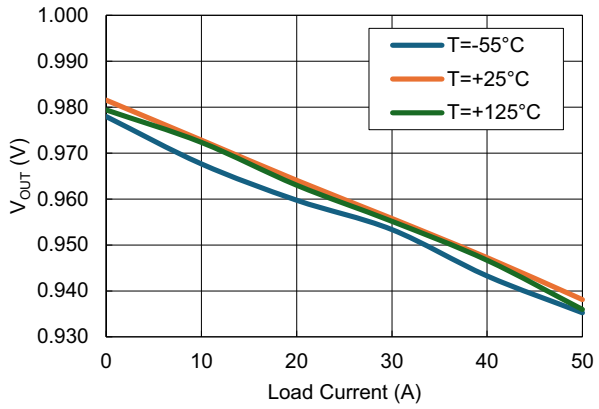


Figure 17. DROOP Regulation for Various Temperatures (V_{DD} = 5V, PVIN = 5V, V_{REF} = 0.6V, R_{DROOP} = 604Ω)

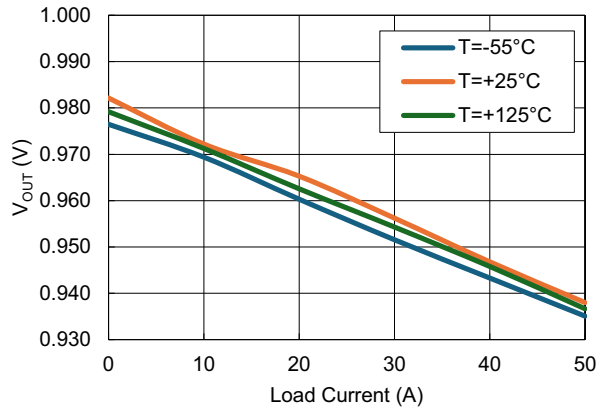


Figure 18. DROOP Regulation for Various Temperatures (V_{DD} = 12V, PVIN = 12V, V_{REF} = 0.6V, R_{DROOP} = 604Ω)

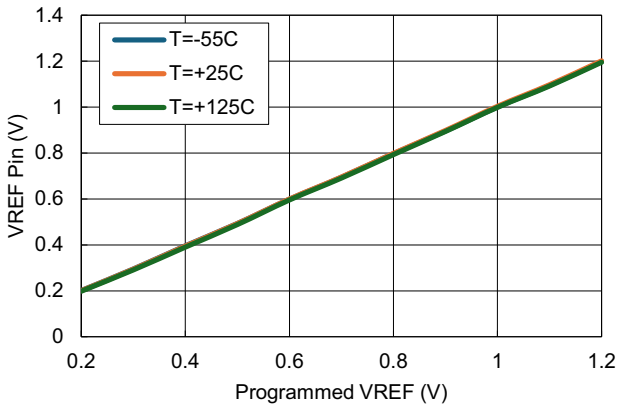


Figure 19. VREF Pin Voltage vs Programmed VREF value with VOUT_COMMAND

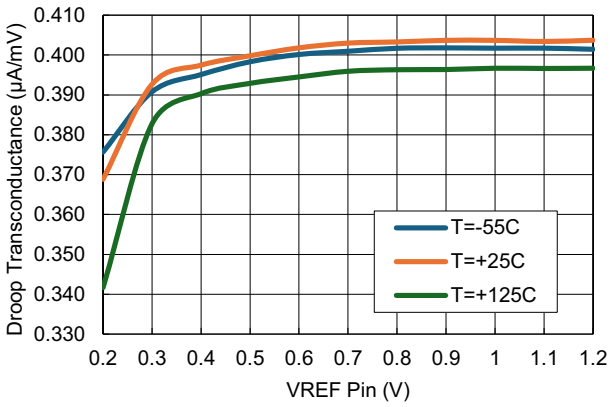


Figure 20. Droop Transconductance vs VREF Voltage

Unless otherwise noted: V_{DD} = 4.5V and 19V, V_{OUT} = 1V, f_{SW} = 500kHz; L_{OUT}(XAL1010-221) = 220nH per phase, C_{OUT}(T530D227M010ATE006) = 2.64mF total per phase, C_{DROOP}= 56nF, C_{VREF} = 47nF, R_{DROOP} = 0Ω, FS tied to VCC, C_{COMP} = 8.2nF, R_{COMP} = 4.22kΩ, C_{POLE} = 330pF, C_{VCC} = 1µF, R_{SLOPE} = 100kΩ, R_{SENSE} = 2mΩ, RFIL=30.1Ω, C_{FIL} = 680pF, $R_{FB(TOP)}$ = 3.24kΩ, $R_{FB(BOT)}$ = 4.99kΩ (Cont.)

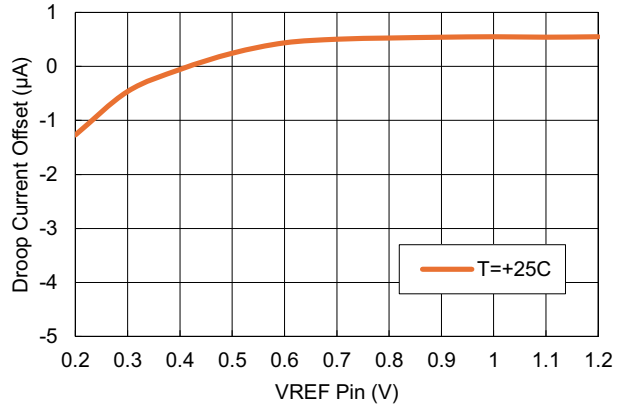


Figure 21. Droop Current Offset vs VREF Voltage (EN_PWM_PH = PH1 Only)

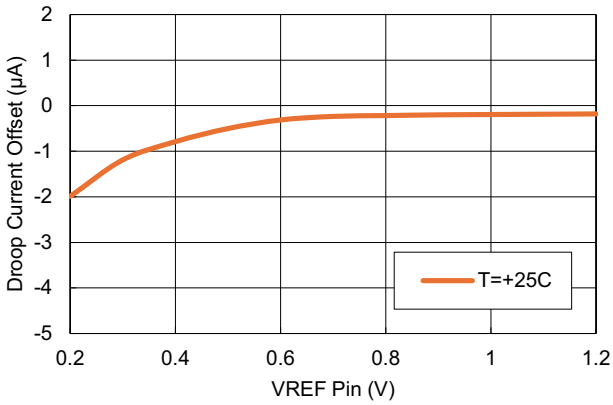


Figure 22. Droop Current Offset vs VREF Voltage (EN_PWM_PH = PH2 Only)

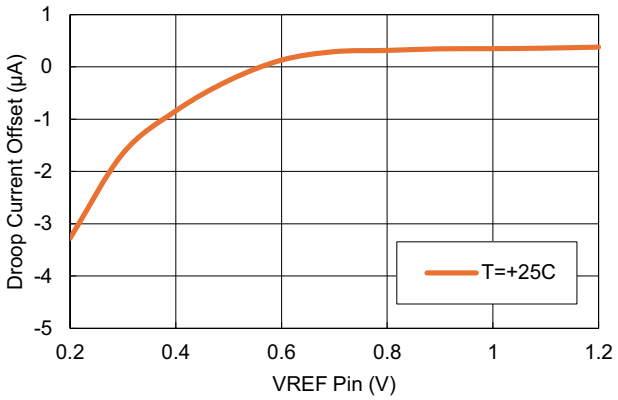


Figure 23. Droop Current Offset vs VREF Voltage (EN_PWM_PH = Both Phases)

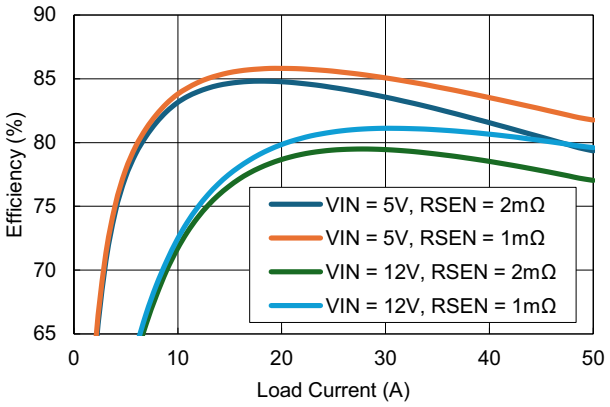


Figure 24. Conversion Efficiency (V_{OUT} = 1V, f_{SW} = 500kHz, RB080LAM-30 between PH and GND for each phase)

4.2 VCC LDO

Unless otherwise noted: f_{SW} = 500kHz

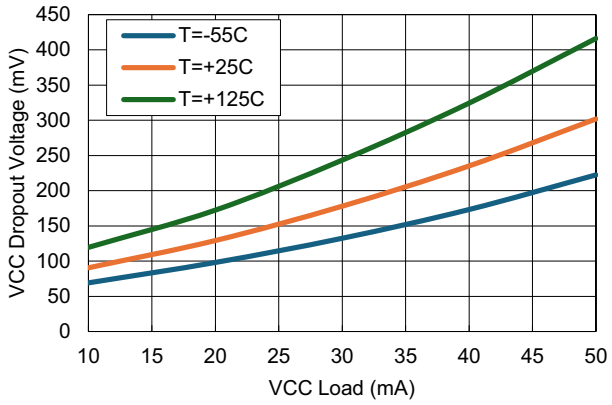


Figure 25. VCC Dropout Voltage (V_{DD} = 4.75V, V_{EN} = 3.3V)

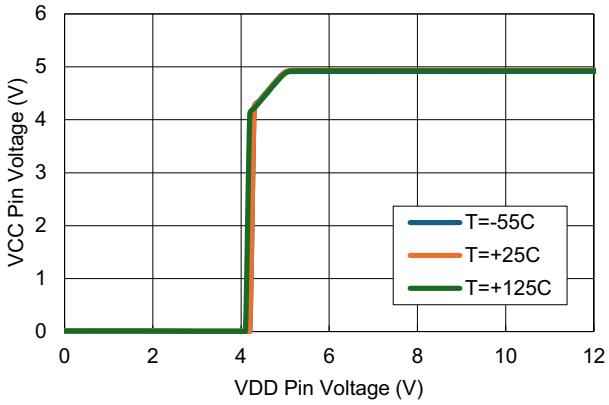


Figure 26. VCC Voltage vs VDD Voltage ($I_{CC(LOAD)}$ = 1mA)

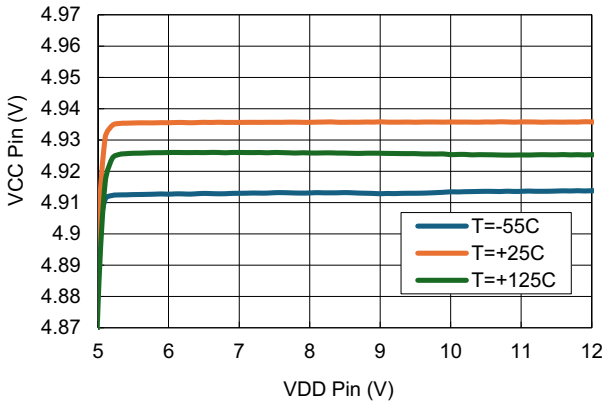


Figure 27. VCC Line Regulation Over Temperature ($I_{CC(LOAD)}$ = 1mA)

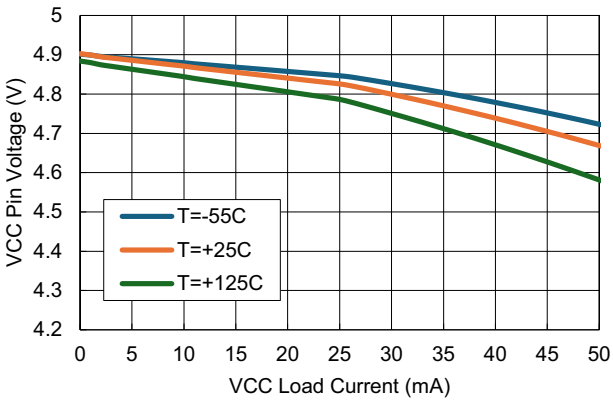


Figure 28. VCC Load Regulation Over Various Temperatures (V_{DD} = 5V)

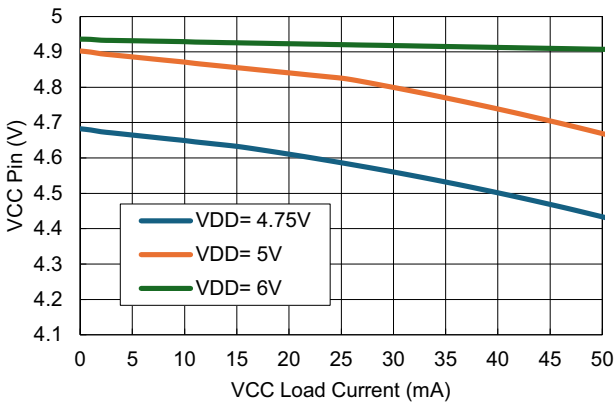


Figure 29. VCC Load Regulation Over Various VDD

4.3 VOUT OV/UV Protection

Unless otherwise noted: V_{DD} = 4.5V and 19V, V_{OUT} = 1V, f_{SW} = 500kHz; L_{OUT}(XAL1010-221) = 220nH per phase, C_{OUT}(T530D227M010ATE006) = 2.64mF total per phase, C_{DROOP}= 56nF, C_{VREF} = 47nF, R_{DROOP} = 0Ω, FS tied to VCC, C_{COMP} = 8.2nF, R_{COMP} = 4.22kΩ, C_{POLE} = 330pF, C_{VCC} = 1µF, R_{SLOPE} = 100kΩ, R_{SENSE} = 2mΩ, RFIL=30.1Ω, C_{FIL} = 680pF, $R_{FB(TOP)}$ = 3.24kΩ, $R_{FB(BOT)}$ = 4.99kΩ

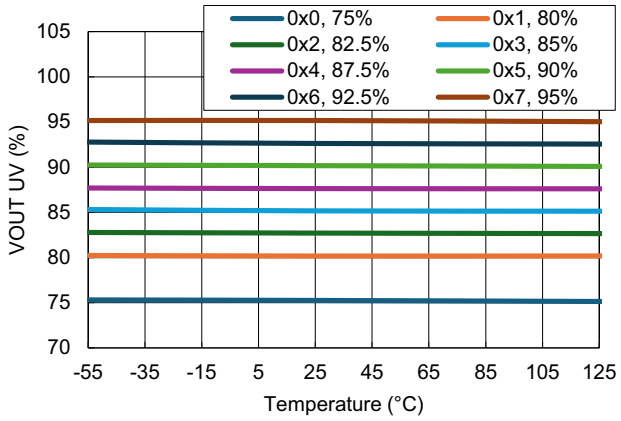


Figure 30. Programmable VOUT UV Falling Thresholds vs Temperature for Various VOUT_UV_LIMIT

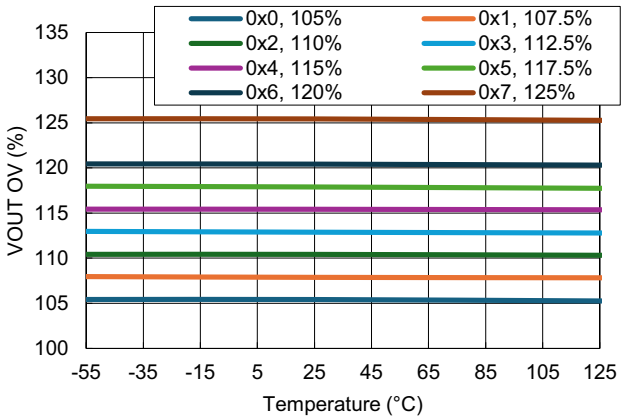


Figure 31. Programmable VOUT OV Falling Thresholds vs Temperature for Various VOUT_OV_LIMIT

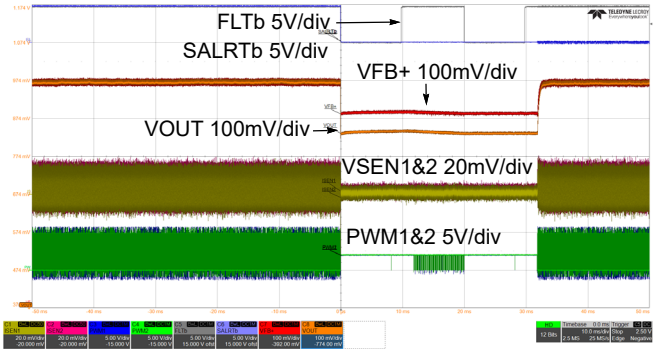


Figure 32. VOUT UV Fault Response into Hiccup Mode (VOUT_UV_LIMIT = 90%, FAULT_RESPONSE = UV Hiccup, Fault held for 25ms starting at time t = 0)

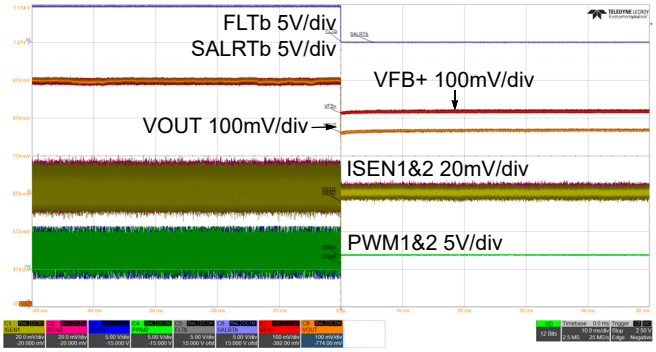


Figure 33. VOUT UV Fault Response into Latch-Off Mode (VOUT_UV_LIMIT = 90%, FAULT_RESPONSE = UV Latch-Off, Fault held for 25ms starting at time t = 0)

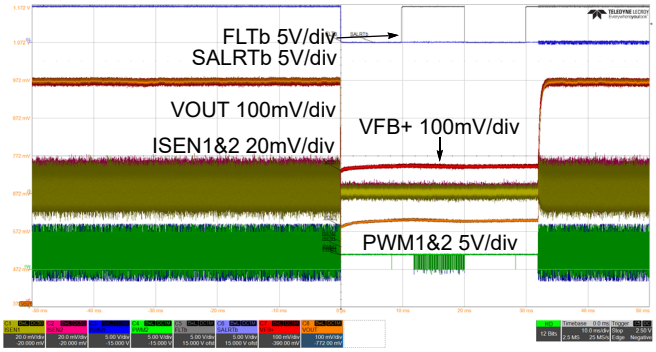


Figure 34. Severe VOUT UV Fault Response into Hiccup Mode (FAULT_MASK = UV, FAULT_RESPONSE = UV Severe Hiccup, Fault held for 25ms starting at time t = 0)

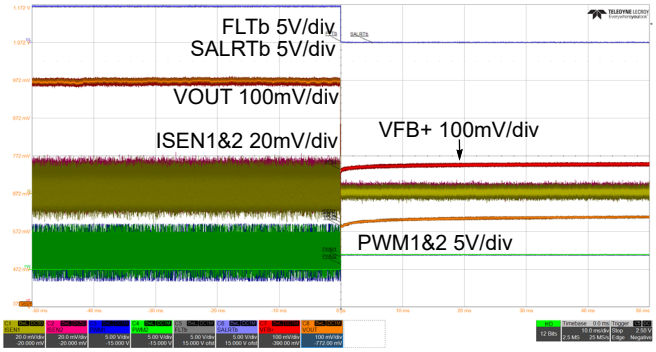


Figure 35. Severe VOUT UV Fault Response into Latch-Off Mode (FAULT_MASK = UV, FAULT_RESPONSE = UV Severe Latch-Off, Fault held for 25ms starting at time t = 0)

Unless otherwise noted: V_{DD} = 4.5V and 19V, V_{OUT} = 1V, f_{SW} = 500kHz; L_{OUT}(XAL1010-221) = 220nH per phase, C_{OUT}(T530D227M010ATE006) = 2.64mF total per phase, C_{DROOP}= 56nF, C_{VREF} = 47nF, R_{DROOP} = 0Ω, FS tied to VCC, C_{COMP} = 8.2nF, R_{COMP} = 4.22kΩ, C_{POLE} = 330pF, C_{VCC} = 1µF, R_{SLOPE} = 100kΩ, R_{SENSE} = 2mΩ, RFIL=30.1Ω, C_{FIL} = 680pF, $R_{FB(TOP)}$ = 3.24kΩ, $R_{FB(BOT)}$ = 4.99kΩ (Cont.)

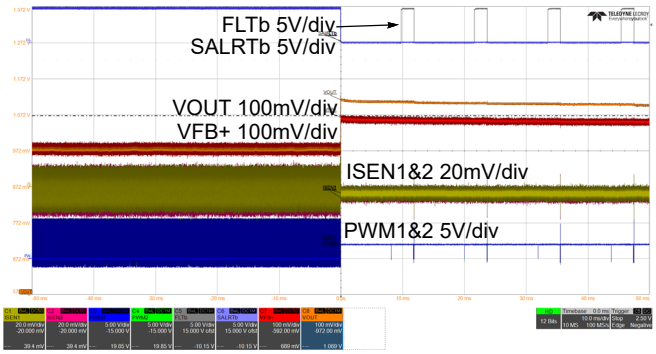


Figure 36. VOUT OV Fault Protection Response into Hiccup Mode (VOUT_OV_LIMIT = 110%, FAULT_RESPONSE = OV Hiccup)

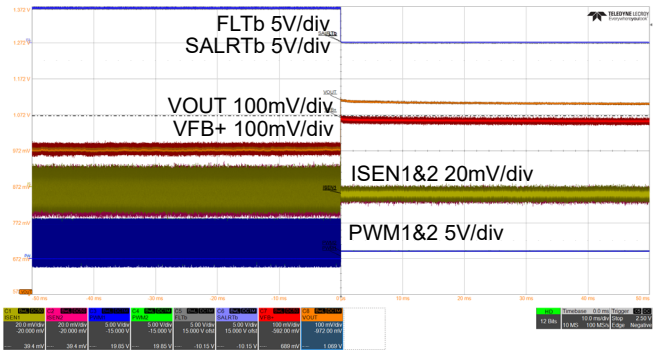


Figure 37. VOUT OV Fault Protection Response into Latch-Off Mode (VOUT_OV_LIMIT = 110%, FAULT_RESPONSE = OV Latch-Off)

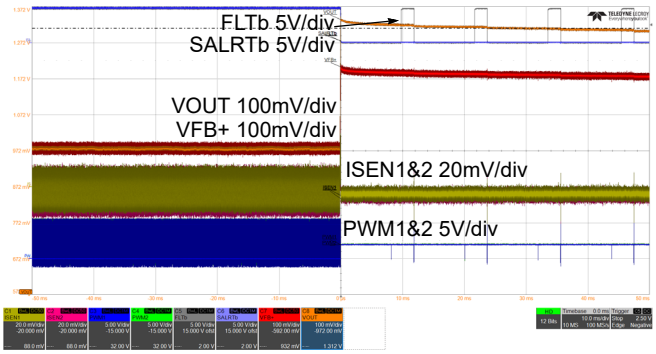


Figure 38. Severe VOUT OV Fault Protection Response into Hiccup Mode (FAULT_MASK = OV, FAULT_RESPONSE = OV Severe Hiccup)

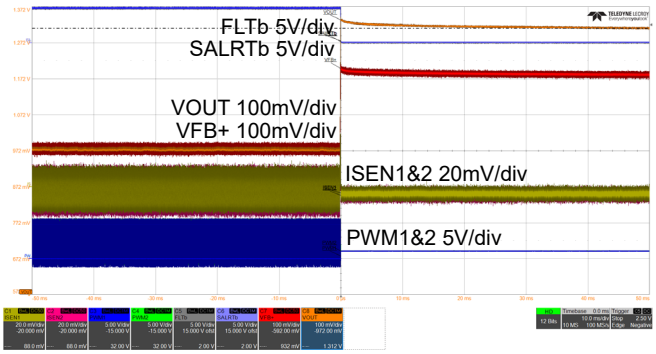


Figure 39. Severe VOUT UV Fault Protection Response into Latch-Off Mode (FAULT_MASK = OV, FAULT_RESPONSE = OV Severe Latch-Off)

4.4 OC Protection

Unless otherwise noted: V_{DD} = 4.5V and 19V, V_{OUT} = 1V, f_{SW} = 500kHz; L_{OUT}(XAL1010-221) = 220nH per phase, C_{OUT}(T530D227M010ATE006) = 2.64mF total per phase, C_{DROOP}= 56nF, C_{VREF} = 47nF, R_{DROOP} = 0Ω, FS tied to VCC, C_{COMP} = 8.2nF, R_{COMP} = 4.22kΩ, C_{POLE} = 330pF, C_{VCC} = 1µF, R_{SLOPE} = 100kΩ, R_{SENSE} = 2mΩ, RFIL=30.1Ω, C_{FIL} = 680pF, $R_{FB(TOP)}$ = 3.24kΩ, $R_{FB(BOT)}$ = 4.99kΩ

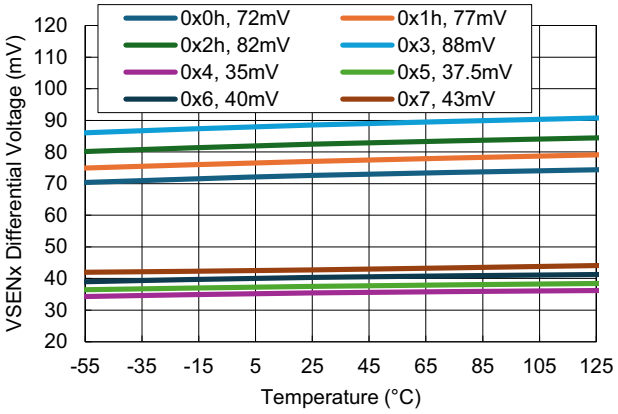


Figure 40. OC1 Thresholds vs Temperature for All Programmable OC_TH Levels

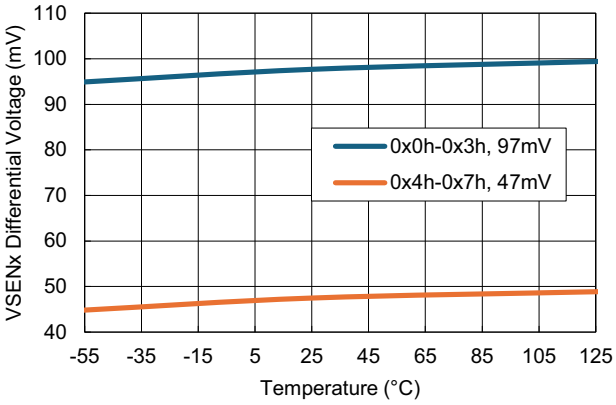


Figure 41. OC2 Thresholds vs Temperature for All Programmable OC_TH Levels

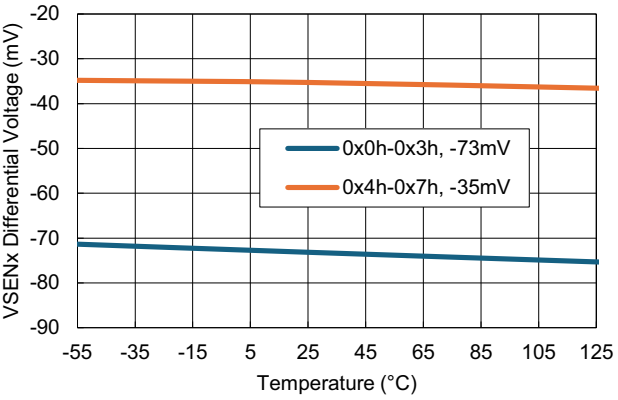


Figure 42. NOC Thresholds vs Temperature for All Programmable OC_TH Levels

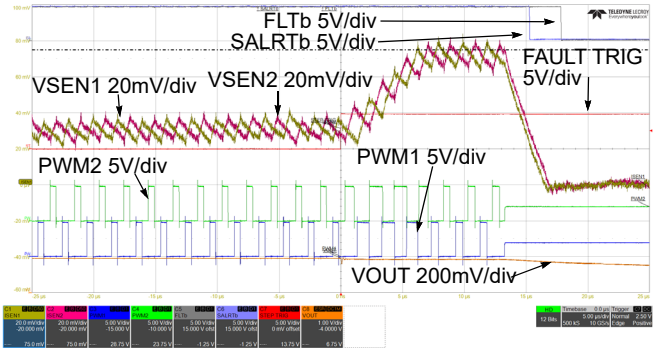


Figure 43. Default OC1 Fault Response (OC_TH = 72mV)

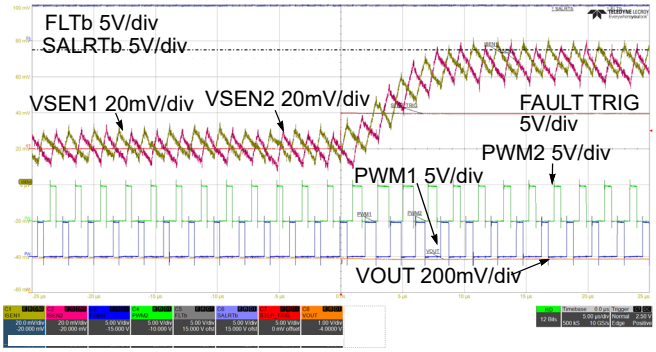


Figure 44. OC1 Fault Response with FAULT Masked (OC_TH = 72mV, FAULT_MASK = OC1)

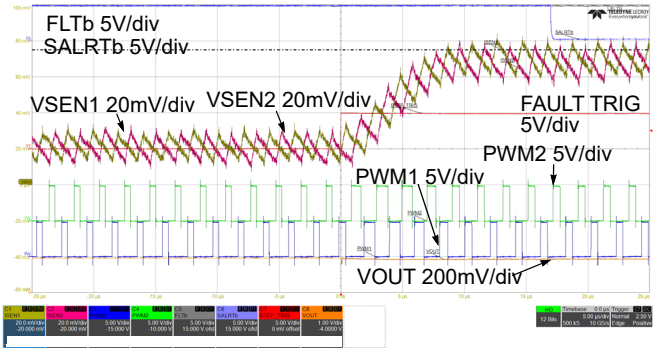


Figure 45. OC1 Fault Response with FAULT Masked and SALERT Unmasked (OC_TH = 72mV, FAULT_MASK = OC1, SALERT_MASK_OVERRIDE = OC1)

Unless otherwise noted: V_{DD} = 4.5V and 19V, V_{OUT} = 1V, f_{SW} = 500kHz; L_{OUT}(XAL1010-221) = 220nH per phase, C_{OUT}(T530D227M010ATE006) = 2.64mF total per phase, C_{DROOP}= 56nF, C_{VREF} = 47nF, R_{DROOP} = 0Ω, FS tied to VCC, C_{COMP} = 8.2nF, R_{COMP} = 4.22kΩ, C_{POLE} = 330pF, C_{VCC} = 1µF, R_{SLOPE} = 100kΩ, R_{SENSE} = 2mΩ, RFIL=30.1Ω, C_{FIL} = 680pF, $R_{FB(TOP)}$ = 3.24kΩ, $R_{FB(BOT)}$ = 4.99kΩ (Cont.)

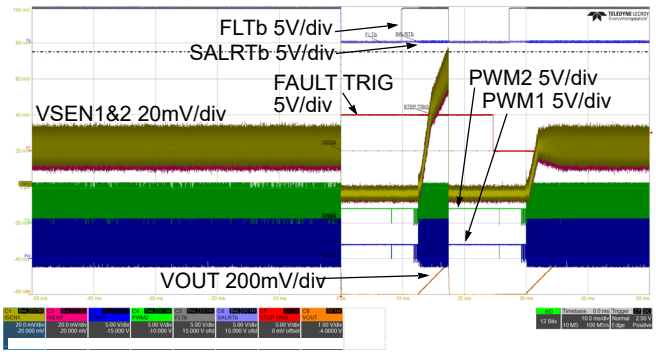


Figure 46. OC1 Fault Response into Hiccup Mode (OC_TH = 72mV, FAULT_RESPONSE = OC1 Hiccup, Fault held for 25ms starting from time t=0)

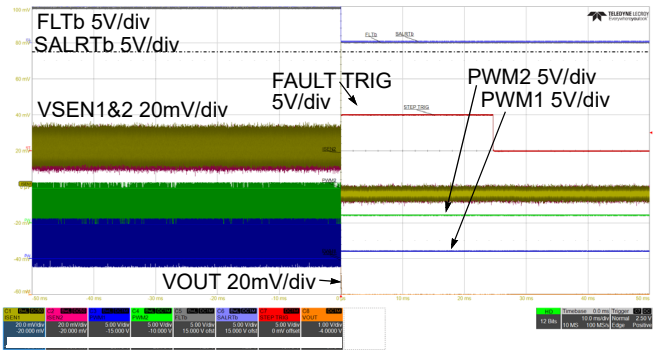


Figure 47. OC1 Fault Response into Latch-Off Mode (OC_TH = 72mV, FAULT_RESPONSE = OC1 Latch-Off, Fault held for 25ms starting from time t=0)

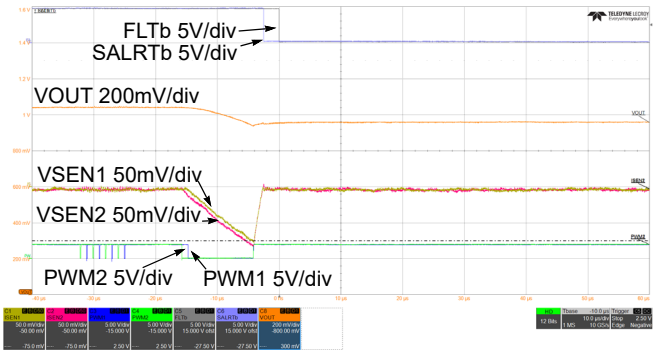


Figure 48. Default NOC Fault Response (OC_TH = -73mV)

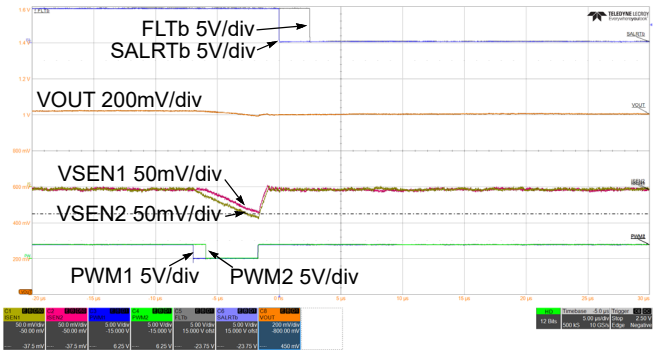


Figure 49. NOC Fault Response (OC_TH = -35mV)

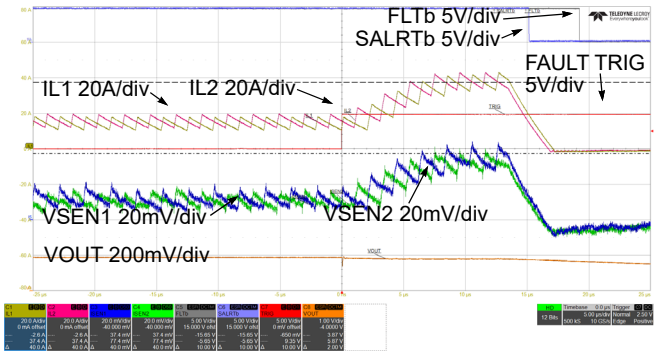


Figure 50. 1mΩ R_{SENSE} OC1 Fault Response (OC_TH = 35mV, R_{SENSE} = 1mΩ, R_{COMP} = 2.1kΩ, C_{COMP} = 22nF, C_{POLE} = 630pF)

4.5 1V Startup

Unless otherwise noted: V_{OUT} = 1V, f_{SW} = 500kHz; L_{OUT}(XAL1010-221) = 220nH per phase, C_{OUT}(T530D227M010ATE006) = 2.64mF total per phase, C_{DROOP}= 56nF, C_{VREF} = 47nF, R_{DROOP} = 0Ω, FS tied to VCC, C_{COMP} = 8.2nF, R_{COMP} = 4.22kΩ, C_{POLE} = 330pF, C_{VCC} = 1µF, R_{SLOPE} = 100kΩ, R_{SENSE} = 2mΩ, RFIL=30.1Ω, C_{FIL} = 680pF, $R_{FB(TOP)}$ = 3.24kΩ, $R_{FB(BOT)}$ = 4.99kΩ

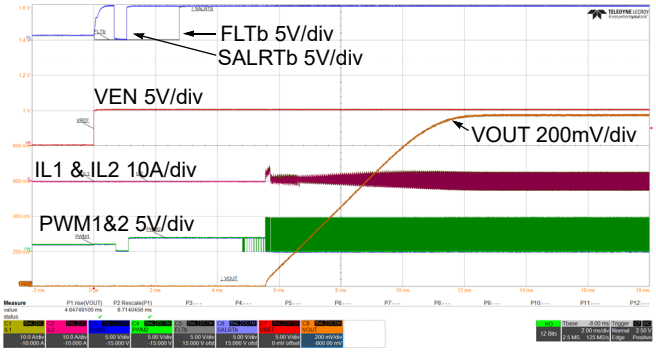


Figure 51. VEN Startup (V_{DD} = 5V, PVIN = 5V, V_{OUT} = 1V, V_{EN} = 0V to 5V, I_{LOAD} = 0A)

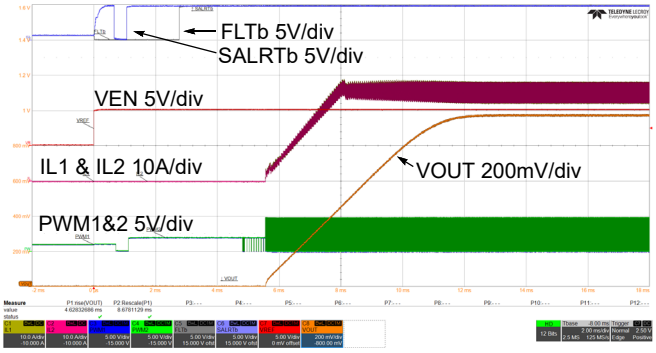


Figure 52. VEN Startup (V_{DD} = 5V, PVIN = 5V, V_{OUT} = 1V, V_{EN} = 0V to 5V, I_{LOAD} = 50A)

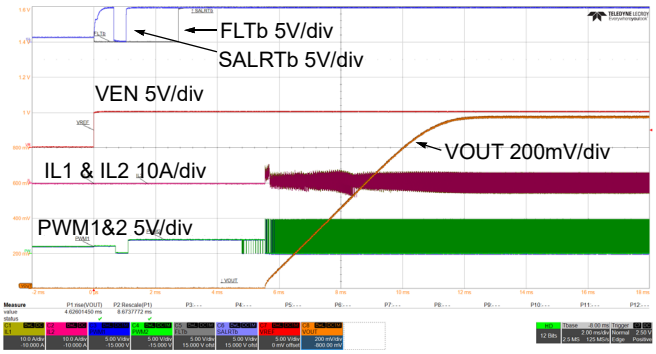


Figure 53. VEN Startup (V_{DD} = 19V, PVIN = 12V V_{OUT} = 1V, V_{EN} = 0V to 5V, I_{LOAD} = 0A)

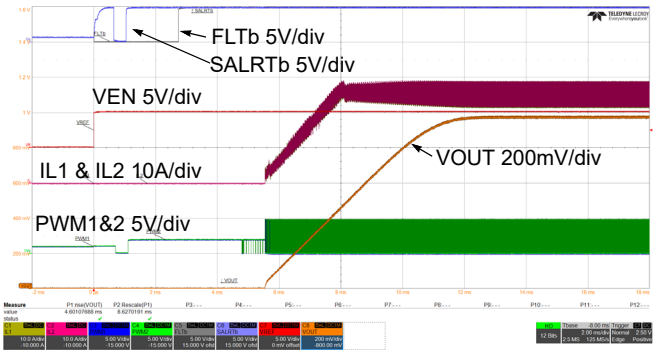


Figure 54. VEN Startup (V_{DD} = 19V, PVIN = 12V V_{OUT} = 1V, V_{EN} = 0V to 5V, I_{LOAD} = 50A)

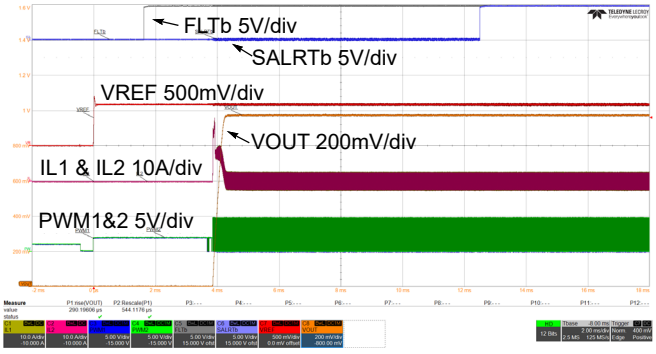


Figure 55. OPERATION Bit Startup (V_{DD} = 5V, PVIN = 5V, V_{OUT} = 1V, I_{LOAD} = 0A, OPERATION = 0x00h to 0x80h, SS_CONFIG = 0.5ms)

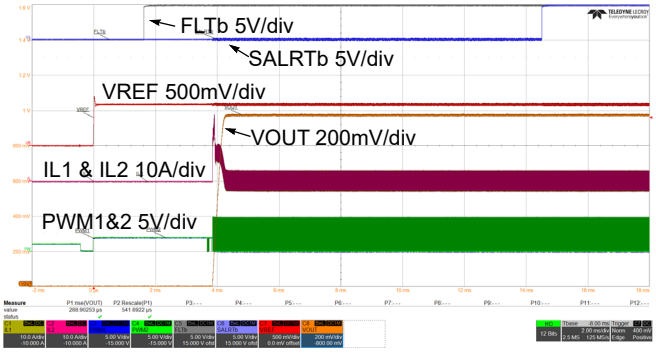


Figure 56. OPERATION Bit Startup (V_{DD} = 19V, PVIN = 12V, V_{OUT} = 1V, I_{LOAD} = 0A, OPERATION = 0x00h to 0x80h, SS_CONFIG = 0.5ms)

Unless otherwise noted: V_{OUT} = 1V, f_{SW} = 500kHz; L_{OUT}(XAL1010-221) = 220nH per phase, C_{OUT}(T530D227M010ATE006) = 2.64mF total per phase, C_{DROOP}= 56nF, C_{VREF} = 47nF, R_{DROOP} = 0Ω, FS tied to VCC, C_{COMP} = 8.2nF, R_{COMP} = 4.22kΩ, C_{POLE} = 330pF, C_{VCC} = 1µF, R_{SLOPE} = 100kΩ, R_{SENSE} = 2mΩ, RFIL=30.1Ω, C_{FIL} = 680pF, $R_{FB(TOP)}$ = 3.24kΩ, $R_{FB(BOT)}$ = 4.99kΩ (Cont.)

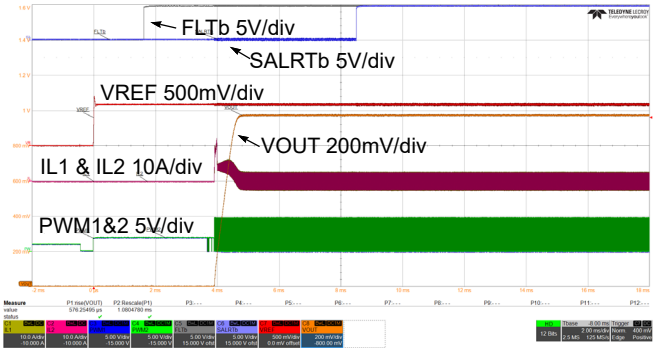


Figure 57. OPERATION Bit Startup (V_{DD} = 5V, PVIN = 5V, V_{OUT} = 1V, I_{LOAD} = 0A, OPERATION = 0x00h to 0x80h, SS_CONFIG = 1ms)

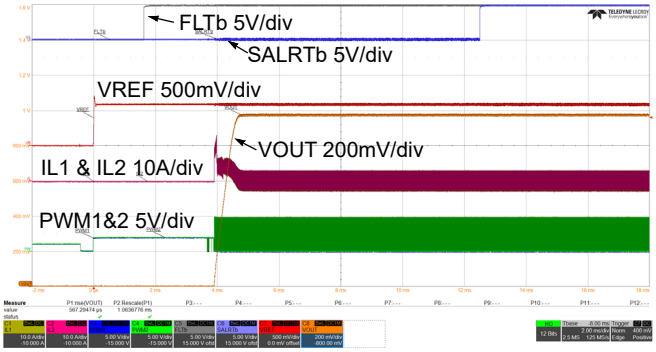


Figure 58. OPERATION Bit Startup (V_{DD} = 19V, PVIN = 12V, V_{OUT} = 1V, I_{LOAD} = 0A, OPERATION = 0x00h to 0x80h, SS_CONFIG = 1ms)

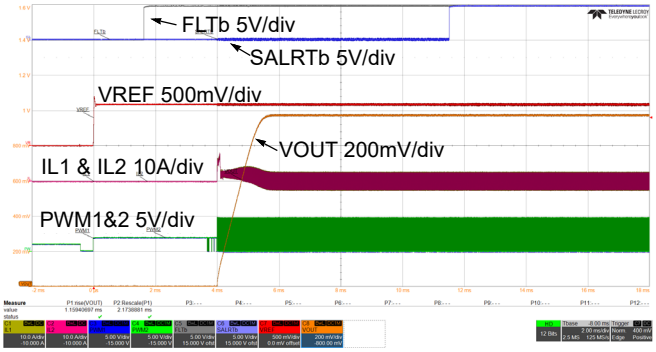


Figure 59. OPERATION Bit Startup (V_{DD} = 5V, PVIN = 5V, V_{OUT} = 1V, I_{LOAD} = 0A, OPERATION = 0x00h to 0x80h, SS_CONFIG = 2ms)

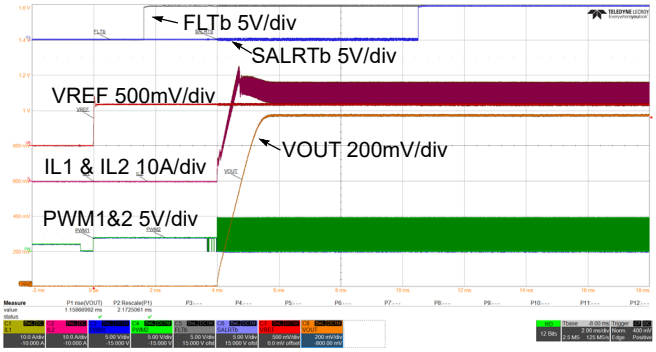


Figure 60. OPERATION Bit Startup (V_{DD} = 5V, PVIN = 5V, V_{OUT} = 1V, I_{LOAD} = 50A, OPERATION = 0x00h to 0x80h, SS_CONFIG = 2ms)

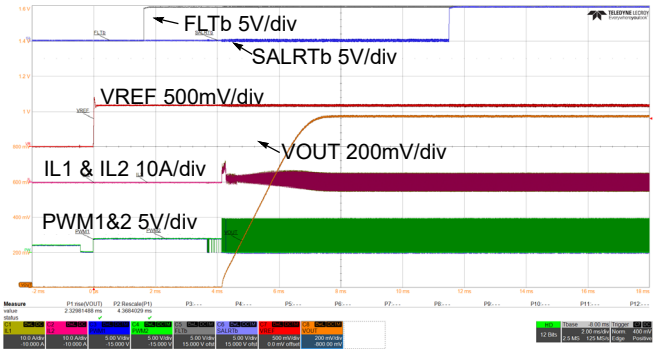


Figure 61. OPERATION Bit Startup (V_{DD} = 19V, PVIN = 12V, V_{OUT} = 1V, I_{LOAD} = 0A, OPERATION = 0x00h to 0x80h, SS_CONFIG = 2ms)

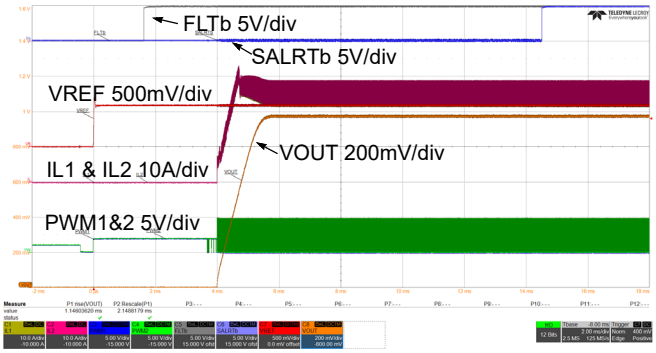


Figure 62. OPERATION Bit Startup (V_{DD} = 19V, PVIN = 12V, V_{OUT} = 1V, I_{LOAD} = 50A, OPERATION = 0x00h to 0x80h, SS_CONFIG = 2ms)

Unless otherwise noted: V_{OUT} = 1V, f_{SW} = 500kHz; L_{OUT}(XAL1010-221) = 220nH per phase, C_{OUT}(T530D227M010ATE006) = 2.64mF total per phase, C_{DROOP}= 56nF, C_{VREF} = 47nF, R_{DROOP} = 0Ω, FS tied to VCC, C_{COMP} = 8.2nF, R_{COMP} = 4.22kΩ, C_{POLE} = 330pF, C_{VCC} = 1µF, R_{SLOPE} = 100kΩ, R_{SENSE} = 2mΩ, RFIL=30.1Ω, C_{FIL} = 680pF, $R_{FB(TOP)}$ = 3.24kΩ, $R_{FB(BOT)}$ = 4.99kΩ (Cont.)

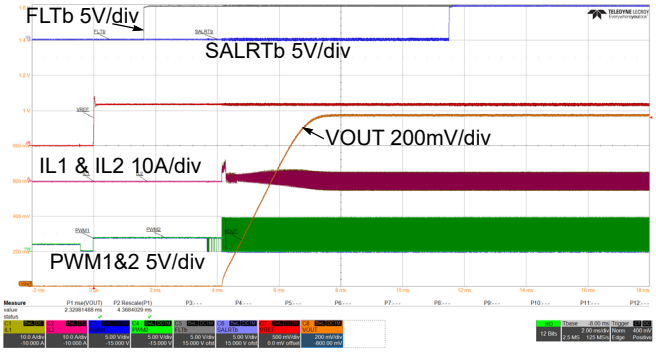


Figure 63. OPERATION Bit Startup (V_{DD} = 5V, PVIN = 5V, V_{OUT} = 1V, I_{LOAD} = 0A, OPERATION = 0x00h to 0x80h, SS_CONFIG = 4ms)

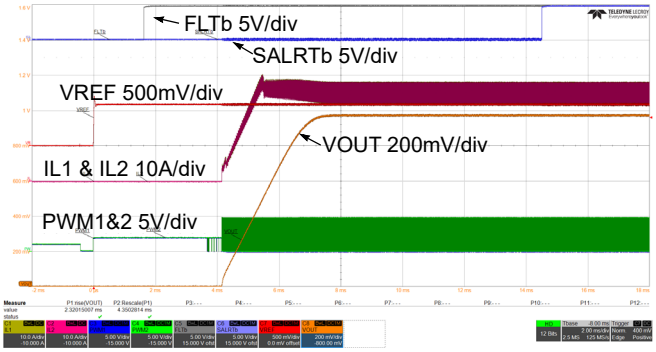


Figure 64. OPERATION Bit Startup (V_{DD} = 5V, PVIN = 5V, V_{OUT} = 1V, I_{LOAD} = 50A, OPERATION = 0x00h to 0x80h, SS_CONFIG = 4ms)

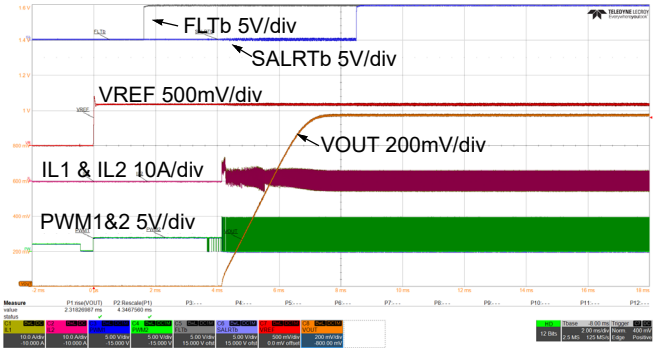


Figure 65. OPERATION Bit Startup (V_{DD} = 19V, PVIN = 12V, V_{OUT} = 1V, I_{LOAD} = 0A, OPERATION = 0x00h to 0x80h, SS_CONFIG = 4ms)

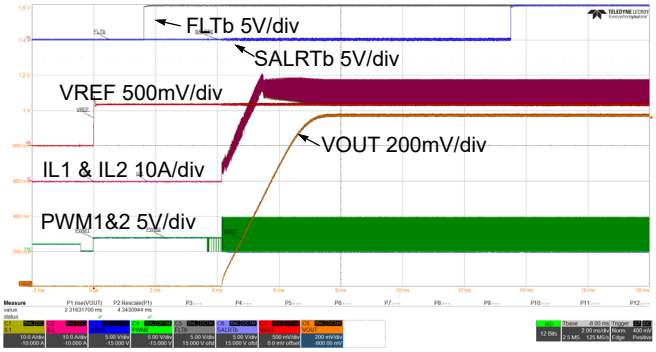


Figure 66. OPERATION Bit Startup (V_{DD} = 19V, PVIN = 12V, V_{OUT} = 1V, I_{LOAD} = 50A, OPERATION = 0x00h to 0x80h, SS_CONFIG = 4ms)

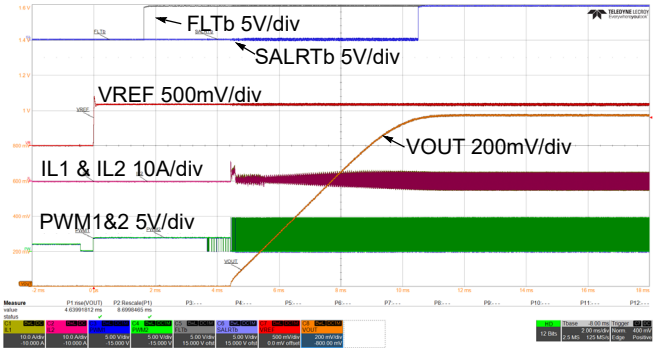


Figure 67. OPERATION Bit Startup (V_{DD} = 5V, PVIN = 5V, V_{OUT} = 1V, I_{LOAD} = 0A, OPERATION = 0x00h to 0x80h, SS_CONFIG = 8ms)

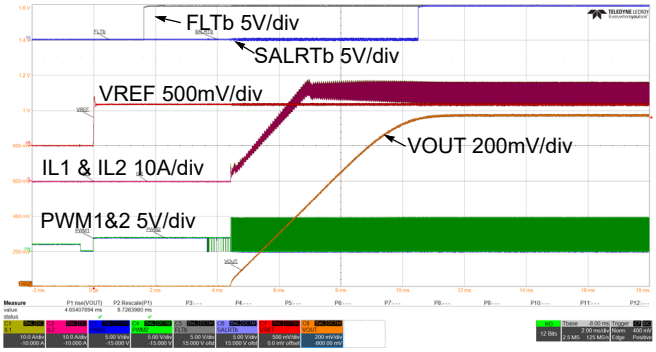


Figure 68. OPERATION Bit Startup (V_{DD} = 5V, PVIN = 5V, V_{OUT} = 1V, I_{LOAD} = 50A, OPERATION = 0x00h to 0x80h, SS_CONFIG = 8ms)

Unless otherwise noted: V_{OUT} = 1V, f_{SW} = 500kHz; L_{OUT}(XAL1010-221) = 220nH per phase, C_{OUT}(T530D227M010ATE006) = 2.64mF total per phase, C_{DROOP}= 56nF, C_{VREF} = 47nF, R_{DROOP} = 0Ω, FS tied to VCC, C_{COMP} = 8.2nF, R_{COMP} = 4.22kΩ, C_{POLE} = 330pF, C_{VCC} = 1µF, R_{SLOPE} = 100kΩ, R_{SENSE} = 2mΩ, RFIL=30.1Ω, C_{FIL} = 680pF, $R_{FB(TOP)}$ = 3.24kΩ, $R_{FB(BOT)}$ = 4.99kΩ (Cont.)

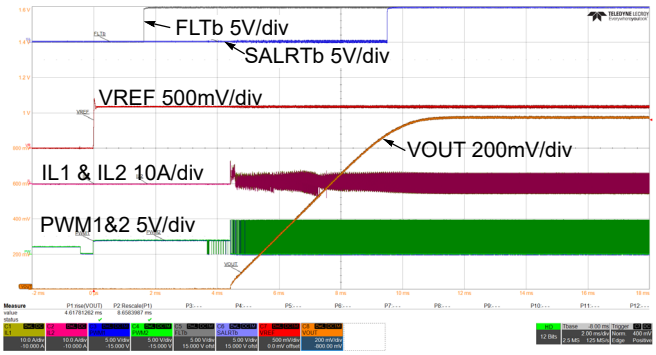


Figure 69. OPERATION Bit Startup (V_{DD} = 19V, PVIN = 12V, V_{OUT} = 1V, I_{LOAD} = 0A, OPERATION = 0x00h to 0x80h, SS_CONFIG = 8ms)

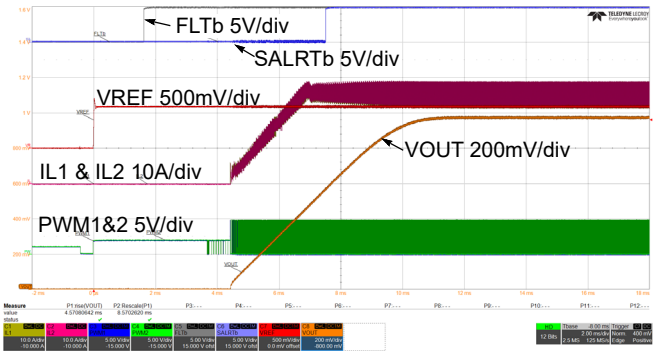


Figure 70. OPERATION Bit Startup (V_{DD} = 19V, PVIN = 12V, V_{OUT} = 1V, I_{LOAD} = 50A, OPERATION = 0x00h to 0x80h, SS_CONFIG = 8ms)

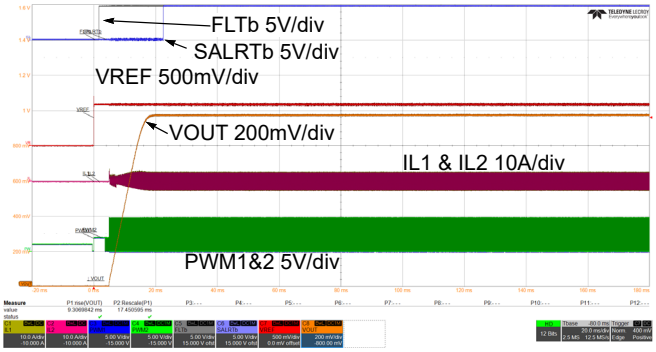


Figure 71. OPERATION Bit Startup (V_{DD} = 5V, PVIN = 5V, V_{OUT} = 1V, I_{LOAD} = 0A, OPERATION = 0x00h to 0x80h, SS_CONFIG = 16ms)

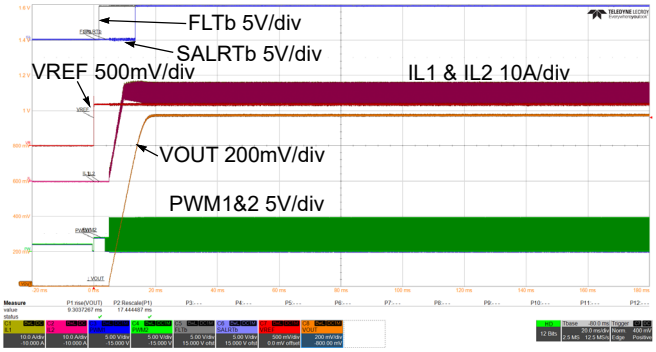


Figure 72. OPERATION Bit Startup (V_{DD} = 5V, PVIN = 5V, V_{OUT} = 1V, I_{LOAD} = 50A, OPERATION = 0x00h to 0x80h, SS_CONFIG = 16ms)

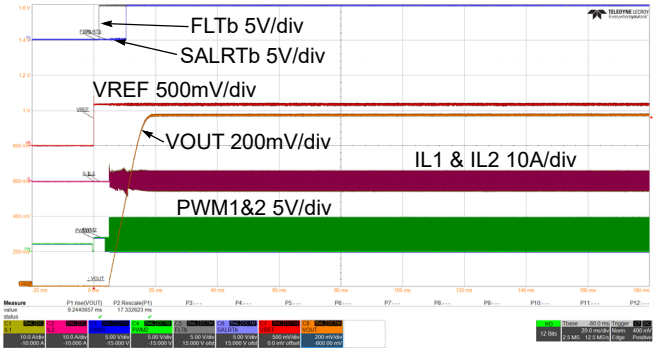


Figure 73. OPERATION Bit Startup (V_{DD} = 19V, PVIN = 12V, V_{OUT} = 1V, I_{LOAD} = 0A, OPERATION = 0x00h to 0x80h, SS_CONFIG = 16ms)

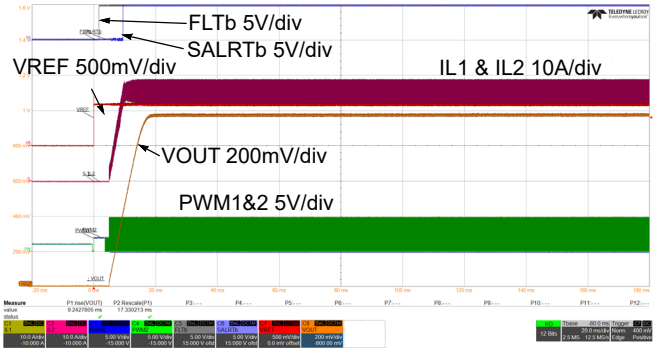


Figure 74. OPERATION Bit Startup (V_{DD} = 19V, PVIN = 12V, V_{OUT} = 1V, I_{LOAD} = 50A, OPERATION = 0x00h to 0x80h, SS_CONFIG = 16ms)

Unless otherwise noted: V_{OUT} = 1V, f_{SW} = 500kHz; L_{OUT}(XAL1010-221) = 220nH per phase, C_{OUT}(T530D227M010ATE006) = 2.64mF total per phase, C_{DROOP}= 56nF, C_{VREF} = 47nF, R_{DROOP} = 0Ω, FS tied to VCC, C_{COMP} = 8.2nF, R_{COMP} = 4.22kΩ, C_{POLE} = 330pF, C_{VCC} = 1µF, R_{SLOPE} = 100kΩ, R_{SENSE} = 2mΩ, RFIL=30.1Ω, C_{FIL} = 680pF, $R_{FB(TOP)}$ = 3.24kΩ, $R_{FB(BOT)}$ = 4.99kΩ (Cont.)

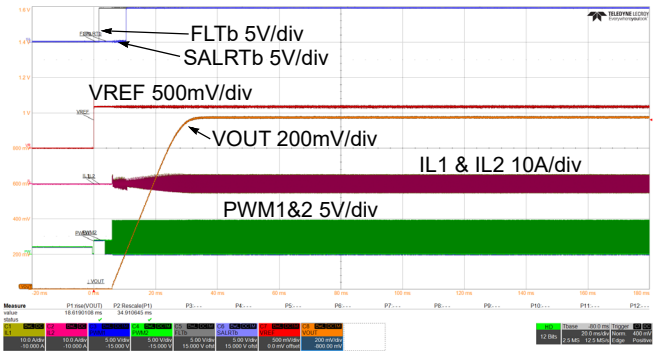


Figure 75. OPERATION Bit Startup (V_{DD} = 5V, PVIN = 5V, V_{OUT} = 1V, I_{LOAD} = 0A, OPERATION = 0x00h to 0x80h, SS_CONFIG = 32ms)

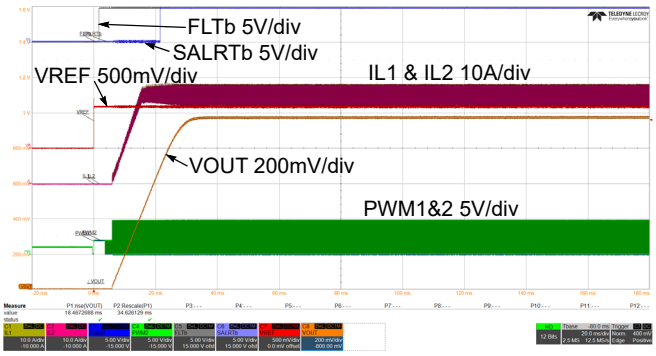


Figure 76. OPERATION Bit Startup (V_{DD} = 5V, PVIN = 5V, V_{OUT} = 1V, I_{LOAD} = 50A, OPERATION = 0x00h to 0x80h, SS_CONFIG = 32ms)

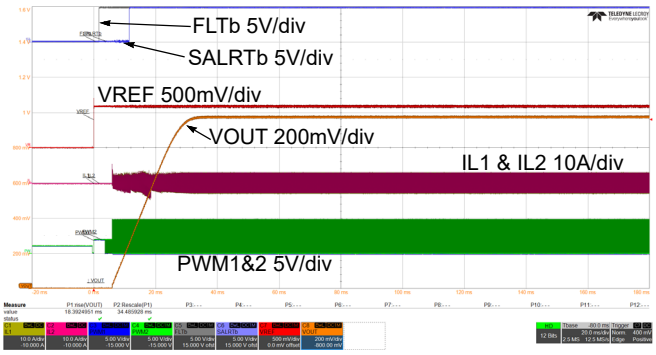


Figure 77. OPERATION Bit Startup (V_{DD} = 19V, PVIN = 12V, V_{OUT} = 1V, I_{LOAD} = 0A, OPERATION = 0x00h to 0x80h, SS_CONFIG = 32ms)

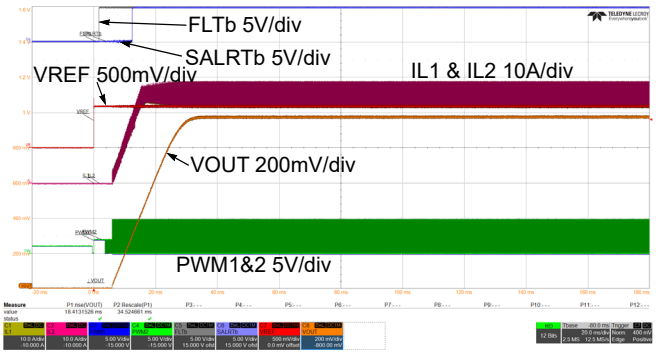


Figure 78. OPERATION Bit Startup (V_{DD} = 19V, PVIN = 12V, V_{OUT} = 1V, I_{LOAD} = 50A, OPERATION = 0x00h to 0x80h, SS_CONFIG = 32ms)

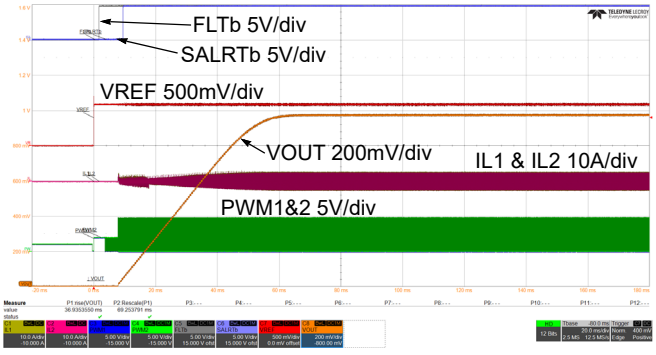


Figure 79. OPERATION Bit Startup (V_{DD} = 5V, PVIN = 5V, V_{OUT} = 1V, I_{LOAD} = 0A, OPERATION = 0x00h to 0x80h, SS_CONFIG = 64ms)

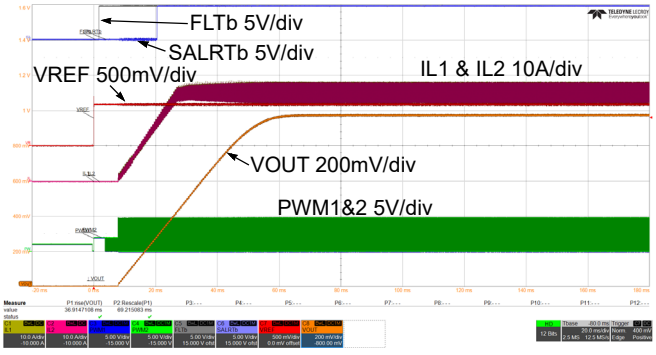


Figure 80. OPERATION Bit Startup (V_{DD} = 5V, PVIN = 5V, V_{OUT} = 1V, I_{LOAD} = 50A, OPERATION = 0x00h to 0x80h, SS_CONFIG = 64ms)

Unless otherwise noted: V_{OUT} = 1V, f_{SW} = 500kHz; L_{OUT}(XAL1010-221) = 220nH per phase, C_{OUT}(T530D227M010ATE006) = 2.64mF total per phase, C_{DROOP}= 56nF, C_{VREF} = 47nF, R_{DROOP} = 0Ω, FS tied to VCC, C_{COMP} = 8.2nF, R_{COMP} = 4.22kΩ, C_{POLE} = 330pF, C_{VCC} = 1µF, R_{SLOPE} = 100kΩ, R_{SENSE} = 2mΩ, RFIL=30.1Ω, C_{FIL} = 680pF, $R_{FB(TOP)}$ = 3.24kΩ, $R_{FB(BOT)}$ = 4.99kΩ (Cont.)

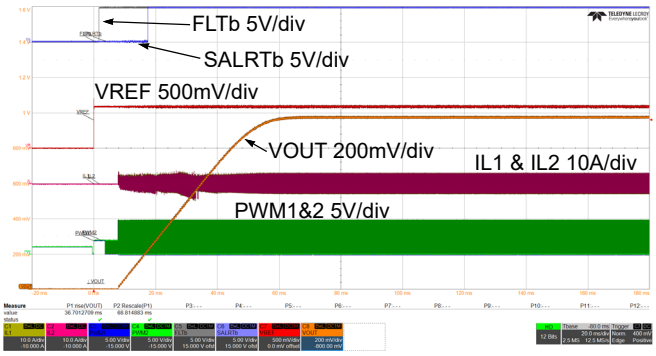


Figure 81. OPERATION Bit Startup (V_{DD} = 19V, PVIN = 12V, V_{OUT} = 1V, I_{LOAD} = 0A, OPERATION = 0x00h to 0x80h, SS_CONFIG = 64ms)

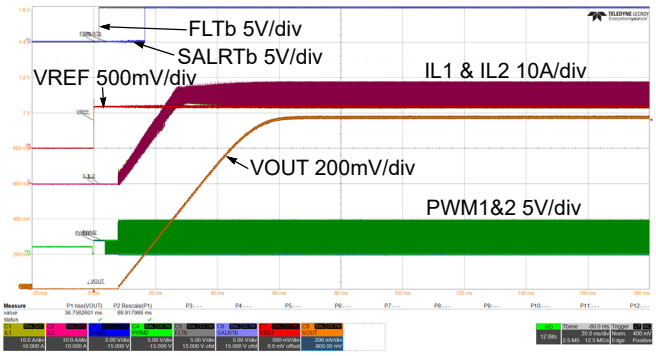


Figure 82. OPERATION Bit Startup (V_{DD} = 19V, PVIN = 12V, V_{OUT} = 1V, I_{LOAD} = 50A, OPERATION = 0x00h to 0x80h, SS_CONFIG = 64ms)

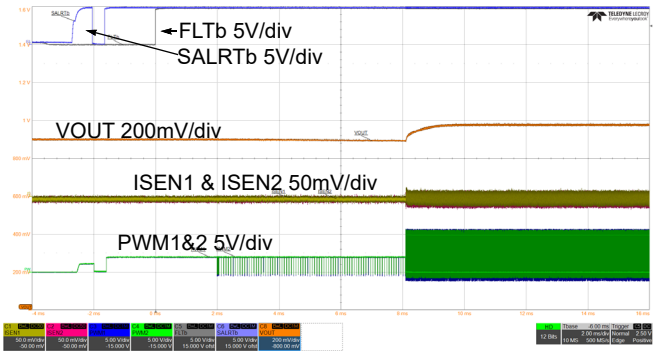


Figure 83. Pre-Biased Startup (V_{DD} = 5V, PVIN = 5V, V_{OUT} = 1V, I_{LOAD} = 0A, $V_{OUT(PRE-BIASED)}$ = 0.9V)

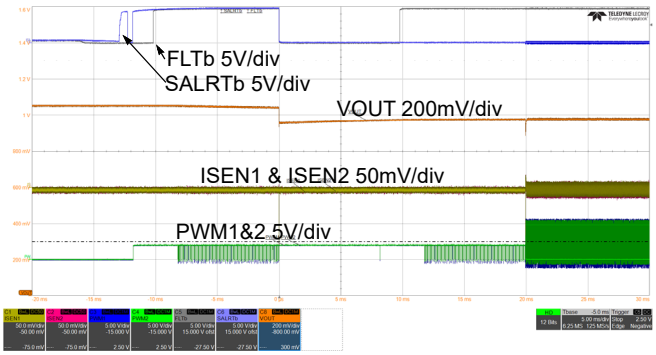


Figure 84. Pre-Biased Startup (V_{DD} = 5V, PVIN = 5V, V_{OUT} = 1V, I_{LOAD} = 0A, $V_{OUT(PRE-BIASED)}$ = 1.05V)

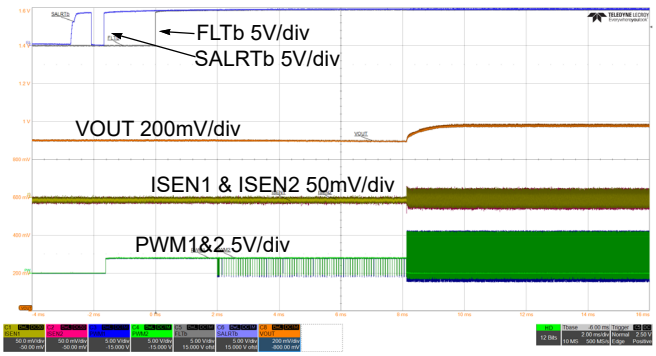


Figure 85. Pre-Biased Startup (V_{DD} = 19V, PVIN = 12V, V_{OUT} = 1V, I_{LOAD} = 0A, $V_{OUT(PRE-BIASED)}$ = 0.9V)

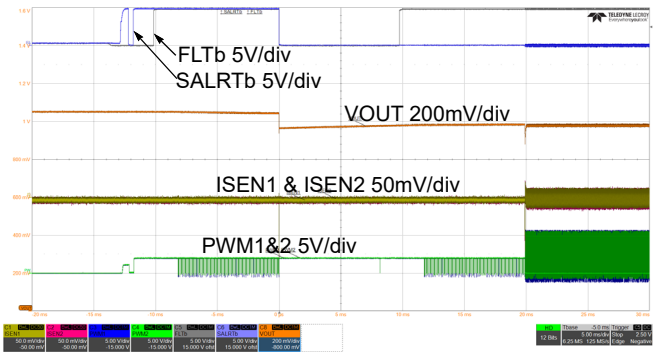


Figure 86. Pre-Biased Startup (V_{DD} = 19V, PVIN = 12V, V_{OUT} = 1V, I_{LOAD} = 0A, $V_{OUT(PRE-BIASED)}$ = 1.05V)

4.6 5V Startup

Unless otherwise noted: V_{DD} = 19V, PVIN = 12V, V_{OUT} = 5V, f_{SW} = 500kHz; $L_{OUT(XAL1010-682)}$ = 680nH per phase, $C_{OUT(T530D227M010ATE006)}$ = 440µF Total per Phase, C_{DROOP}= 56nF, C_{VREF} = 47nF, R_{DROOP} = 0Ω, FS tied to VCC, C_{COMP} = 8.2nF, R_{COMP} = 4.22kΩ, C_{POLE} = 330pF, C_{VCC} = 1µF, R_{SLOPE} = 100kΩ, R_{SENSE} = 2mΩ, RFIL=30.1Ω, C_{FIL} = 680pF, $R_{FB(TOP)}$ = 38.2kΩ, $R_{FB(BOT)}$ = 4.99kΩ

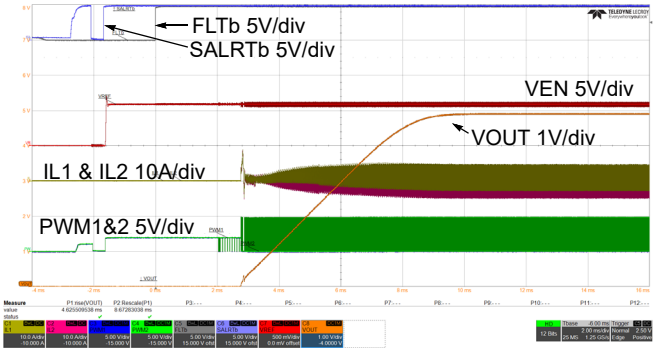


Figure 87. VEN Startup (V_{EN} = 0V to 5V, I_{LOAD} = 0A, V_{OUT} = 5V)

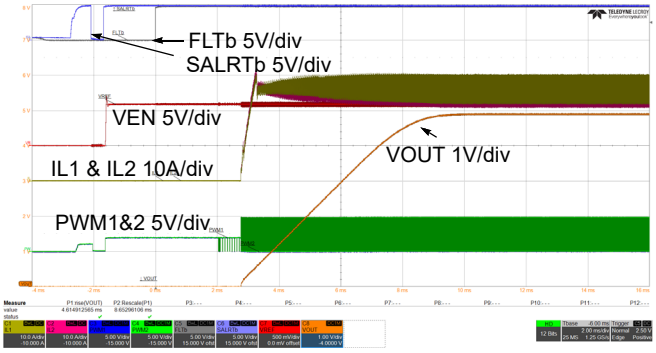


Figure 88. VEN Startup (V_{EN} = 0V to 5V, I_{LOAD} = 50A, V_{OUT} = 5V)

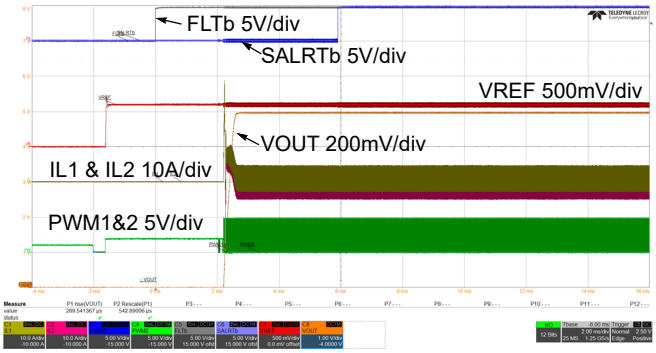


Figure 89. OPERATION Bit Startup (I_{LOAD} = 0A, V_{OUT} = 5V, OPERATION = 0x00h to 0x80h, SS_CONFIG = 0.5ms)

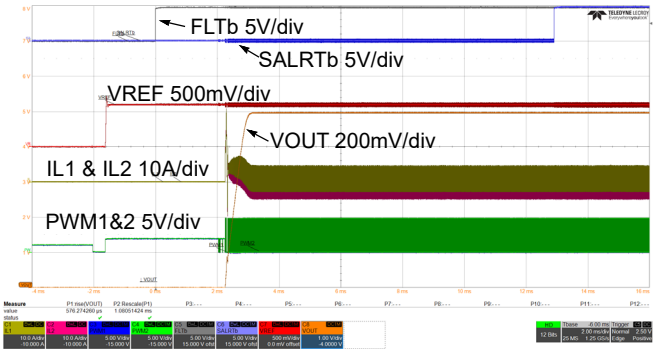


Figure 90. OPERATION Bit Startup (I_{LOAD} = 0A, V_{OUT} = 5V, OPERATION = 0x00h to 0x80h, SS_CONFIG = 1ms)

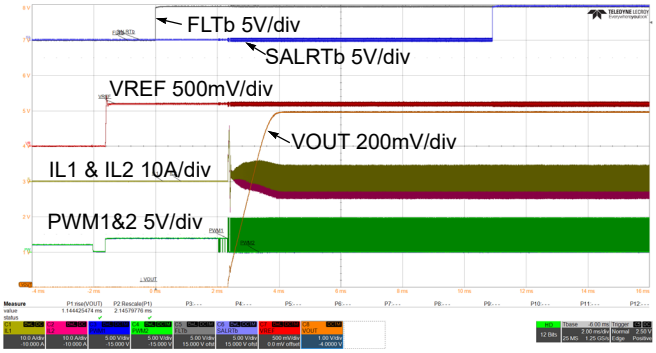


Figure 91. OPERATION Bit Startup (I_{LOAD} = 0A, V_{OUT} = 5V, OPERATION = 0x00h to 0x80h, SS_CONFIG = 2ms)

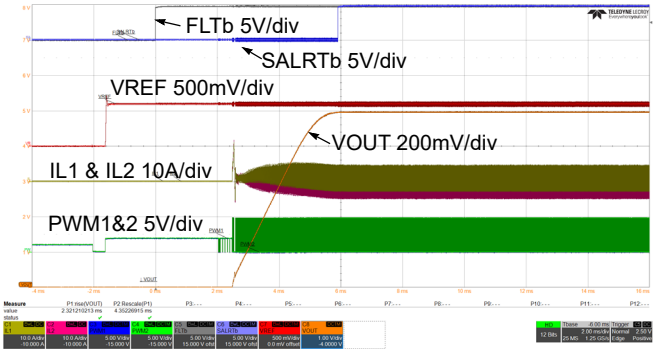


Figure 92. OPERATION Bit Startup (I_{LOAD} = 0A, V_{OUT} = 5V,OPERATION = 0x00h to 0x80h, SS_CONFIG = 4ms)

Unless otherwise noted: V_{DD} = 19V, PVIN = 12V, V_{OUT} = 5V, f_{SW} = 500kHz; $L_{OUT(XAL1010-682)}$ = 680nH per phase, $C_{OUT(T530D227M010ATE006)}$ = 440µF Total per Phase, C_{DROOP}= 56nF, C_{VREF} = 47nF, R_{DROOP} = 0Ω, FS tied to VCC, C_{COMP} = 8.2nF, R_{COMP} = 4.22kΩ, C_{POLE} = 330pF, C_{VCC} = 1µF, R_{SLOPE} = 100kΩ, R_{SENSE} = 2mΩ, RFIL=30.1Ω, C_{FIL} = 680pF, $R_{FB(TOP)}$ = 38.2kΩ, $R_{FB(BOT)}$ = 4.99kΩ

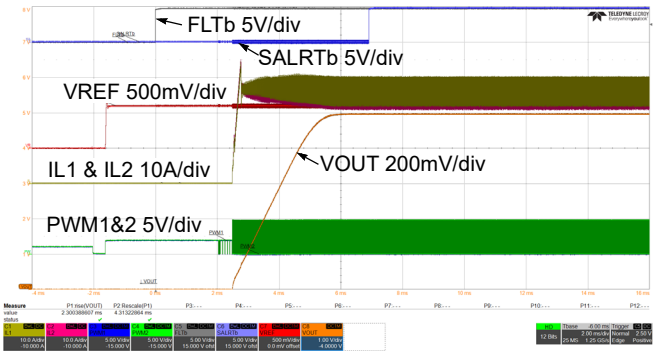


Figure 93. OPERATION Bit Startup (I_{LOAD} = 50A, V_{OUT} = 5V, OPERATION = 0x00h to 0x80h, SS_CONFIG = 4ms)

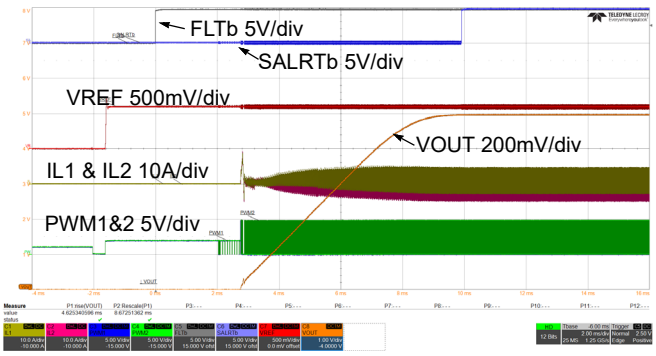


Figure 94. OPERATION Bit Startup (I_{LOAD} = 0A, V_{OUT} = 5V, OPERATION = 0x00h to 0x80h, SS_CONFIG = 8ms)

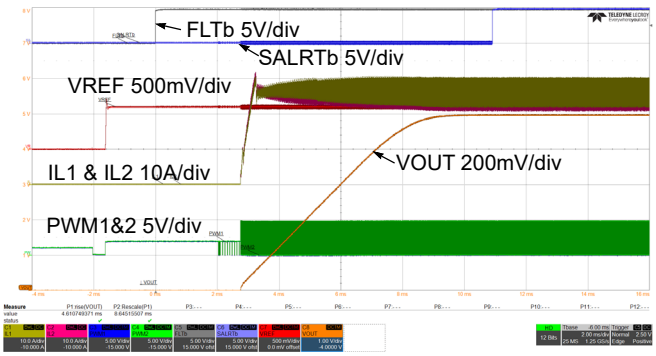


Figure 95. OPERATION Bit Startup (I_{LOAD} = 50A, V_{OUT} = 5V, OPERATION = 0x00h to 0x80h, SS_CONFIG = 8ms)

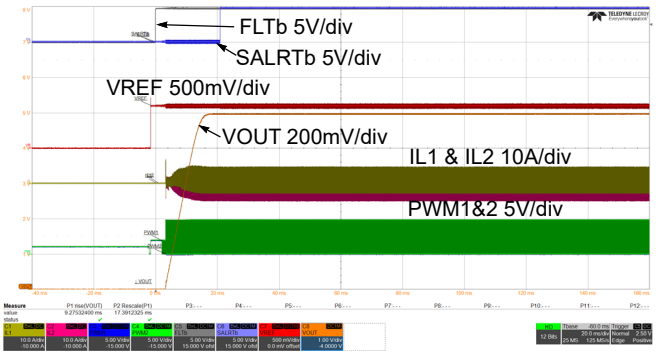


Figure 96. OPERATION Bit Startup (I_{LOAD} = 0A, V_{OUT} = 5V, OPERATION = 0x00h to 0x80h, SS_CONFIG = 16ms)

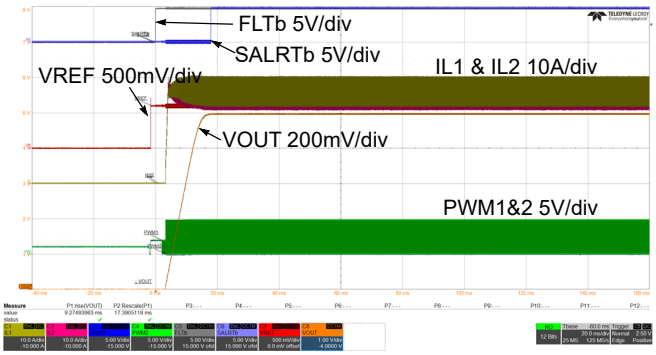


Figure 97. OPERATION Bit Startup (I_{LOAD} = 50A, V_{OUT} = 5V, OPERATION = 0x00h to 0x80h, SS_CONFIG = 16ms)

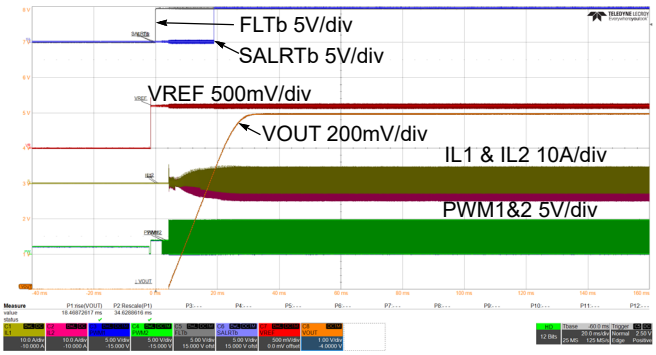


Figure 98. OPERATION Bit Startup (I_{LOAD} = 0A, V_{OUT} = 5V, OPERATION = 0x00h to 0x80h, SS_CONFIG = 32ms)

Unless otherwise noted: V_{DD} = 19V, PVIN = 12V, V_{OUT} = 5V, f_{SW} = 500kHz; $L_{OUT(XAL1010-682)}$ = 680nH per phase, $C_{OUT(T530D227M010ATE006)}$ = 440µF Total per Phase, C_{DROOP}= 56nF, C_{VREF} = 47nF, R_{DROOP} = 0Ω, FS tied to VCC, C_{COMP} = 8.2nF, R_{COMP} = 4.22kΩ, C_{POLE} = 330pF, C_{VCC} = 1µF, R_{SLOPE} = 100kΩ, R_{SENSE} = 2mΩ, RFIL=30.1Ω, C_{FIL} = 680pF, $R_{FB(TOP)}$ = 38.2kΩ, $R_{FB(BOT)}$ = 4.99kΩ

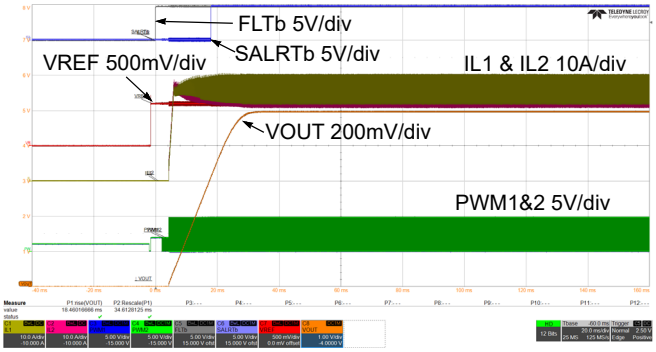


Figure 99. OPERATION Bit Startup (I_{LOAD} = 50A, V_{OUT} = 5V, OPERATION = 0x00h to 0x80h, SS_CONFIG = 32ms)

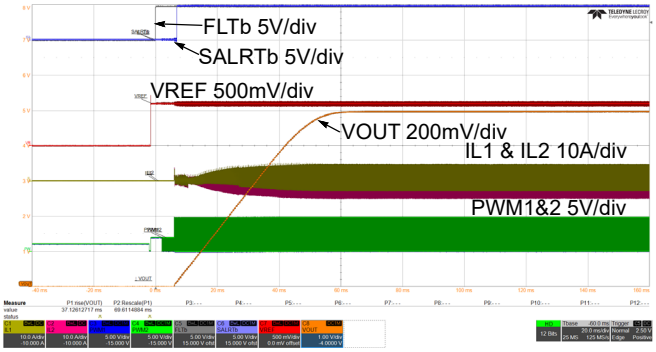


Figure 100. OPERATION Bit Startup (I_{LOAD} = 0A, V_{OUT} = 5V, OPERATION = 0x00h to 0x80h,SS_CONFIG = 64ms)

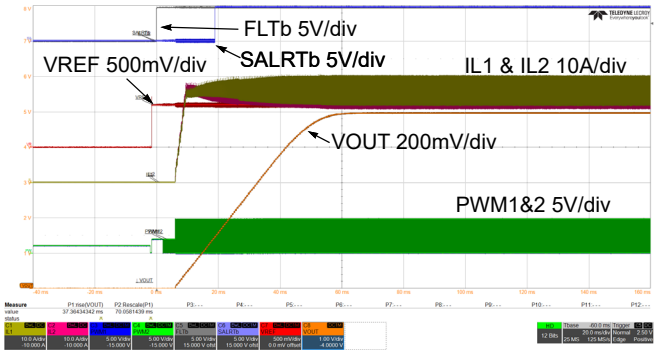


Figure 101. OPERATION Bit Startup (I_{LOAD} = 50A, V_{OUT} = 5V, OPERATION = 0x00h to 0x80h, SS_CONFIG = 64ms)

4.7 Shutdown

Unless otherwise noted: V_{DD} = 4.5V and 19V, V_{OUT} = 1V, f_{SW} = 500kHz; L_{OUT}(XAL1010-221) = 220nH per phase, C_{OUT}(T530D227M010ATE006) = 2.64mF total per phase, C_{DROOP}= 56nF, C_{VREF} = 47nF, R_{DROOP} = 0Ω, FS tied to VCC, C_{COMP} = 8.2nF, R_{COMP} = 4.22kΩ, C_{POLE} = 330pF, C_{VCC} = 1µF, R_{SLOPE} = 100kΩ, R_{SENSE} = 2mΩ, RFIL=30.1Ω, C_{FIL} = 680pF, $R_{FB(TOP)}$ = 3.24kΩ, $R_{FB(BOT)}$ = 4.99kΩ

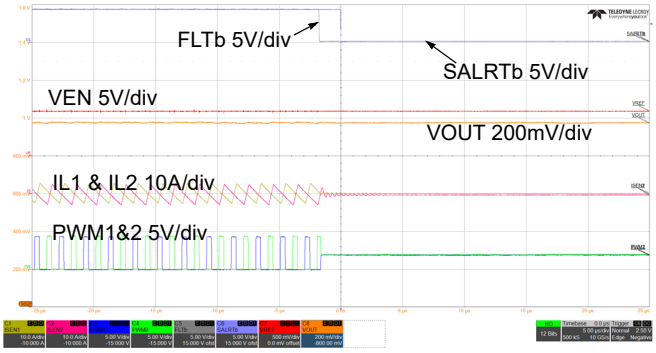


Figure 102. VEN Shutdown (V_{DD} = 5V, PVIN = 5V, V_{EN} = 5V to 0V, V_{OUT} = 1V, I_{LOAD} = 0A)

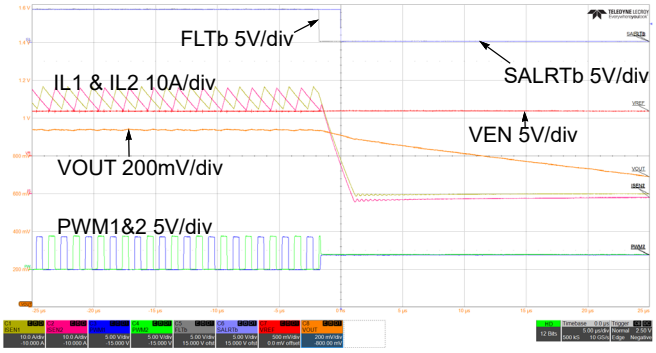


Figure 103. VEN Shutdown (V_{DD} = 5V, PVIN = 5V, V_{EN} = 5V to 0V, V_{OUT} = 1V, I_{LOAD} = 50A)

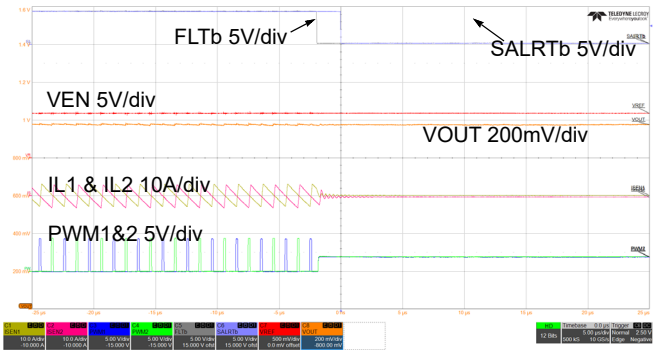


Figure 104. VEN Shutdown (V_{DD} = 19V, PVIN = 12V, V_{EN} = 5V to 0V, V_{OUT} = 5V, I_{LOAD} = 0A)

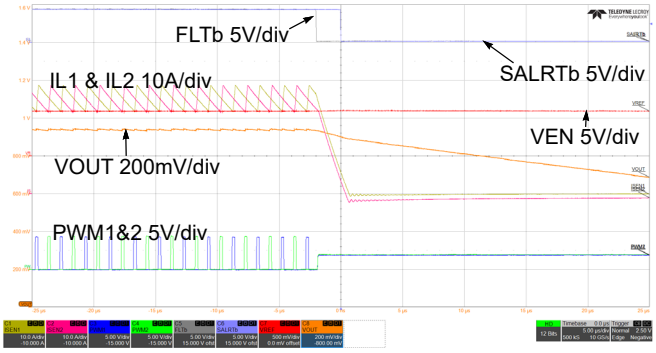


Figure 105. VEN Shutdown (V_{DD} = 19V, PVIN = 12V, V_{EN} = 5V to 0V, V_{OUT} = 5V, I_{LOAD} = 50A)

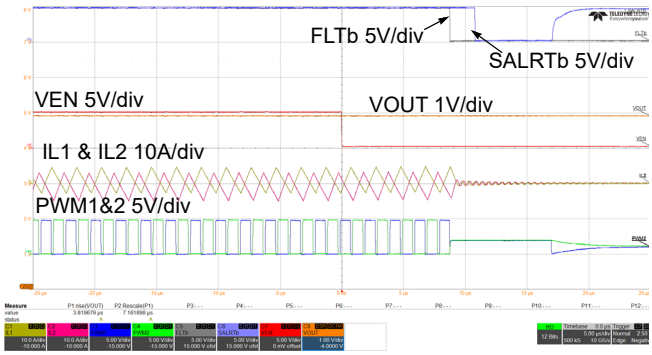


Figure 106. VEN Shutdown (V_{DD} = 19V, PVIN = 12V, V_{EN} = 5V to 0V, V_{OUT} = 5V, I_{LOAD} = 0A, V_{OUT} = 5V, $L_{OUT(XAL1010-682)}$ = 680nH per Phase, $R_{FB(TOP)}$ = 38.2kΩ, $C_{OUT(T530D227M010ATE006)}$ = 440µF Total per Phase)

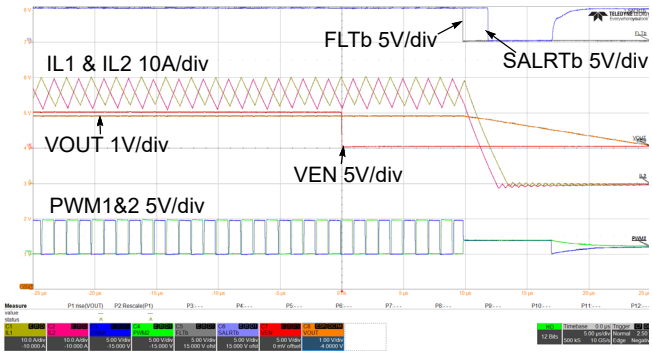


Figure 107. VEN Shutdown (V_{DD} = 19V, PVIN = 12V, V_{EN} = 5V to 0V, V_{OUT} = 5V, I_{LOAD} = 50A, V_{OUT} = 5V, $L_{OUT(XAL1010-682)}$ = 680nH per Phase, $R_{FB(TOP)}$ = 38.2kΩ, $C_{OUT(T530D227M010ATE006)}$ = 440µF Total per Phase)

Unless otherwise noted: V_{DD} = 4.5V and 19V, V_{OUT} = 1V, f_{SW} = 500kHz; L_{OUT}(XAL1010-221) = 220nH per phase, C_{OUT}(T530D227M010ATE006) = 2.64mF total per phase, C_{DROOP}= 56nF, C_{VREF} = 47nF, R_{DROOP} = 0Ω, FS tied to VCC, C_{COMP} = 8.2nF, R_{COMP} = 4.22kΩ, C_{POLE} = 330pF, C_{VCC} = 1µF, R_{SLOPE} = 100kΩ, R_{SENSE} = 2mΩ, RFIL=30.1Ω, C_{FIL} = 680pF, $R_{FB(TOP)}$ = 3.24kΩ, $R_{FB(BOT)}$ = 4.99kΩ (Cont.)

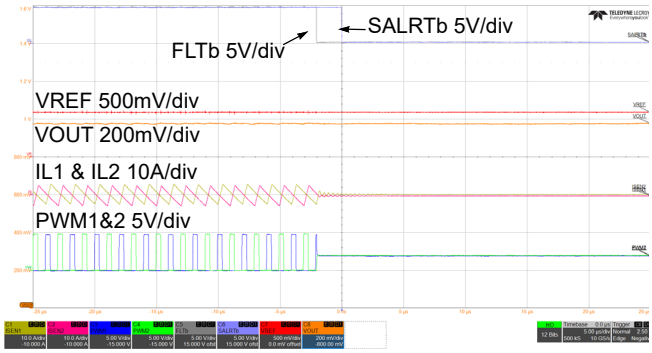


Figure 108. OPERATION Bit Shutdown (V_{DD} = 5V, PVIN = 5V, OPERATION = 0x80h to 0x00h, V_{OUT} = 1V, I_{LOAD} = 0A)

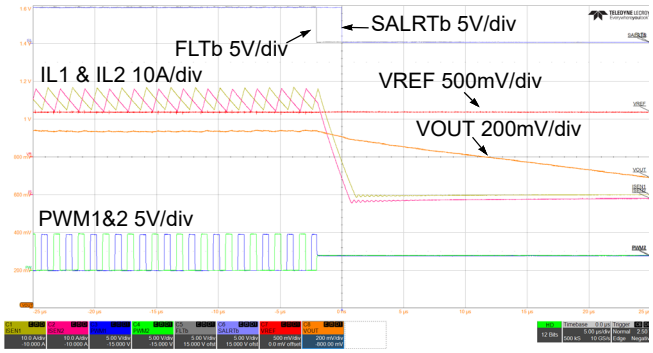


Figure 109. OPERATION Bit Shutdown (V_{DD} = 5V, PVIN = 5V, OPERATION = 0x80h to 0x00h, V_{OUT} = 1V, I_{LOAD} = 50A)

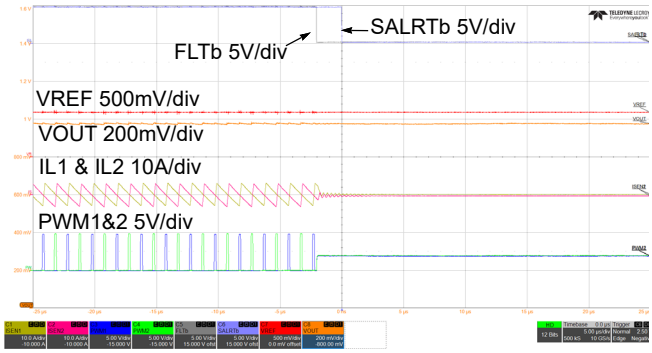


Figure 110. OPERATION Bit Shutdown (V_{DD} = 19V, PVIN = 12V, OPERATION = 0x80h to 0x00h, V_{OUT} = 1V, I_{LOAD} = 0A)

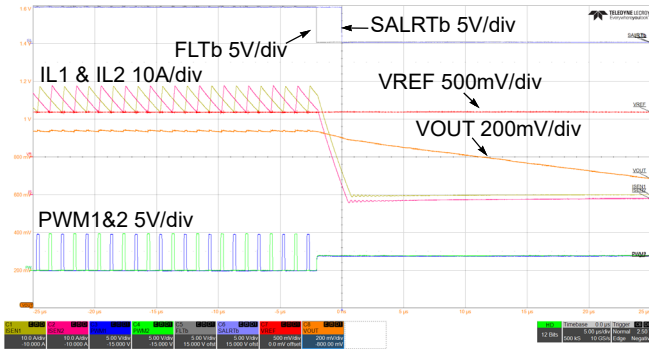


Figure 111. OPERATION Bit Shutdown (V_{DD} = 19V, PVIN = 12V, OPERATION = 0x80h to 0x00h, V_{OUT} = 1V, I_{LOAD} = 50A)

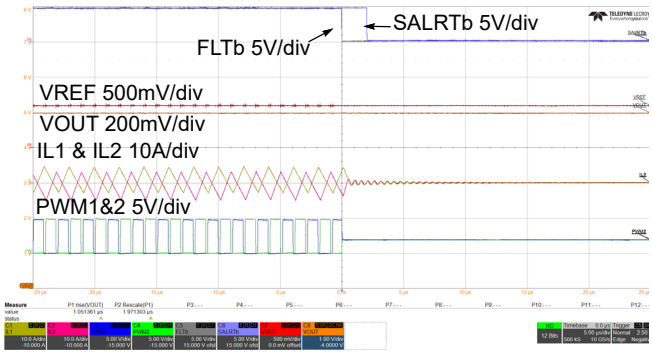


Figure 112. OPERATION Bit Shutdown (V_{DD} = 19V, PVIN = 12V, V_{EN} = 5V to 0V, I_{LOAD} = 50A, V_{OUT} = 5V, $L_{OUT(XAL1010-682)}$ = 680nH per Phase, $R_{FB(TOP)}$ = 38.2kΩ, $C_{OUT(T530D227M010ATE006)}$ = 440µF Total per Phase)

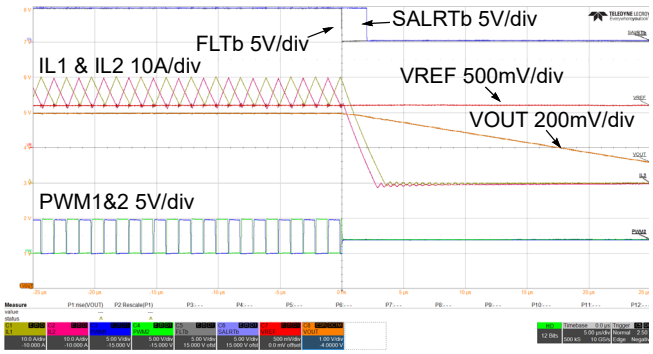


Figure 113. OPERATION Bit Shutdown (V_{DD} = 19V, PVIN = 12V, V_{EN} = 5V to 0V, I_{LOAD} = 50A, V_{OUT} = 5V, $L_{OUT(XAL1010-682)}$ = 680nH per Phase, $R_{FB(TOP)}$ = 38.2kΩ, $C_{OUT(T530D227M010ATE006)}$ = 440µF Total per Phase)

4.8 SYNC Frequency

Unless otherwise noted: V_{OUT} = 1V, f_{SW} = 500kHz; L_{OUT}(XAL1010-221) = 220nH per phase, C_{OUT}(T530D227M010ATE006) = 2.64mF total per phase, C_{DROOP}= 56nF, C_{VREF} = 47nF, R_{DROOP} = 0Ω, FS tied to VCC, C_{COMP} = 8.2nF, R_{COMP} = 4.22kΩ, C_{POLE} = 330pF, C_{VCC} = 1µF, R_{SLOPE} = 100kΩ, R_{SENSE} = 2mΩ, RFIL=30.1Ω, C_{FIL} = 680pF, $R_{FB(TOP)}$ = 3.24kΩ, $R_{FB(BOT)}$ = 4.99kΩ

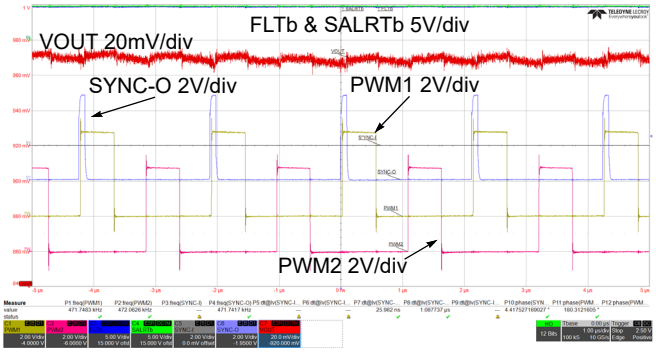


Figure 114. SYNC-O Outputs the PWM Frequency (V_{DD} = 5V, PVIN = 5V, R_{SYNC-O} = Floating, I_{LOAD} = 50A)

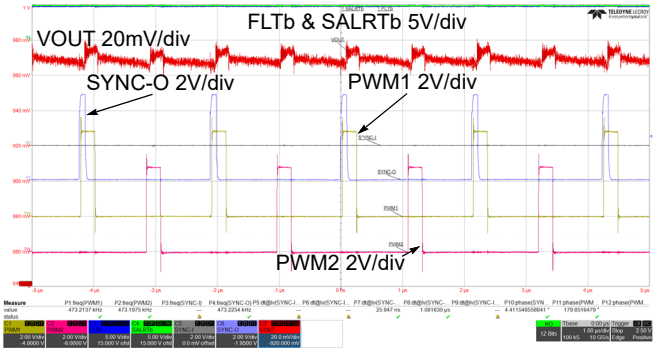


Figure 115. SYNC-O Outputs the PWM Frequency (V_{DD} = 19V, PVIN = 12V, R_{SYNC-O} = Floating, I_{LOAD} = 50A)

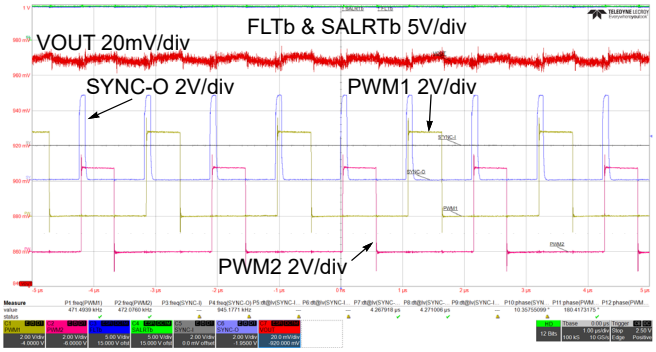


Figure 116. SYNC-O Outputs the Oscillator Frequency (V_{DD} = 5V, PVIN = 5V, R_{SYNC-O} = 100kΩ to GND, I_{LOAD} = 50A)

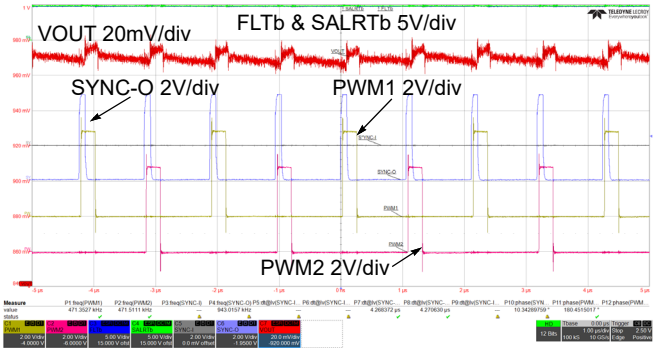


Figure 117. SYNC-O Outputs the Oscillator Frequency (V_{DD} = 19V, PVIN = 12V, R_{SYNC-O} = 100kΩ to GND, I_{LOAD} = 50A)

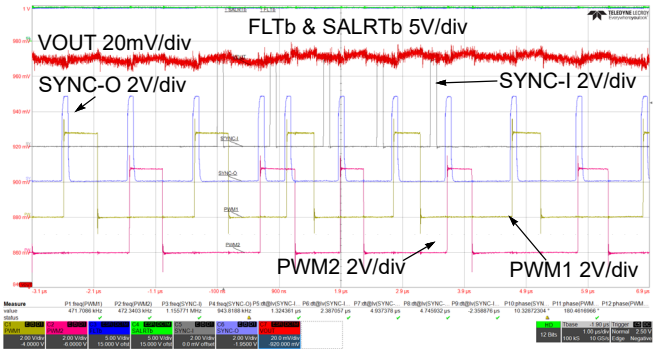


Figure 118. Synch and De-Synch Response with 5 External Clock Pulses (V_{DD} = 5V, PVIN = 5V, FS = VCC, R_{SYNC-O} = 100kΩ to GND, I_{LOAD} = 50A, SYNC-I = 1.15MHz)

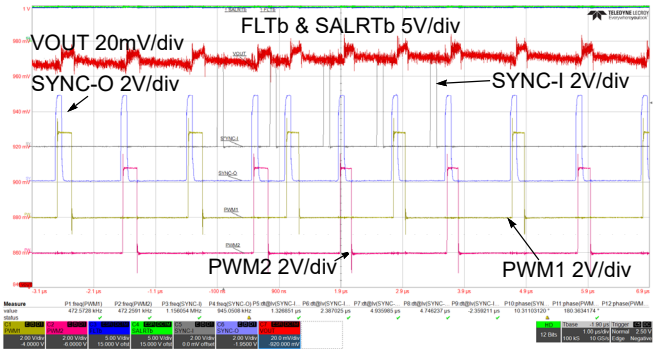


Figure 119. Synch and De-Synch Response with 5 External Clock Pulses (V_{DD} = 19V, PVIN = 12V, FS = VCC, R_{SYNC-O} = 100kΩ to GND, I_{LOAD} = 50A, SYNC-I = 1.15MHz)

Unless otherwise noted: V_{OUT} = 1V, f_{SW} = 500kHz; L_{OUT}(XAL1010-221) = 220nH per phase, C_{OUT}(T530D227M010ATE006) = 2.64mF total per phase, C_{DROOP}= 56nF, C_{VREF} = 47nF, R_{DROOP} = 0Ω, FS tied to VCC, C_{COMP} = 8.2nF, R_{COMP} = 4.22kΩ, C_{POLE} = 330pF, C_{VCC} = 1µF, R_{SLOPE} = 100kΩ, R_{SENSE} = 2mΩ, RFIL=30.1Ω, C_{FIL} = 680pF, $R_{FB(TOP)}$ = 3.24kΩ, $R_{FB(BOT)}$ = 4.99kΩ (Cont.)

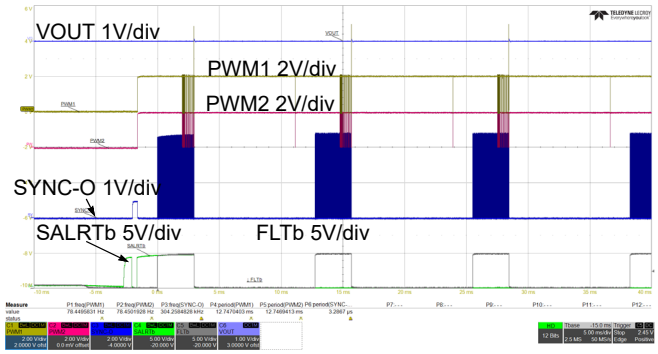


Figure 120. VDD Startup into ON_FAULT Hiccup Response (V_{DD} = 19V, PVIN = 12V, R_{FS} = 350kΩ)

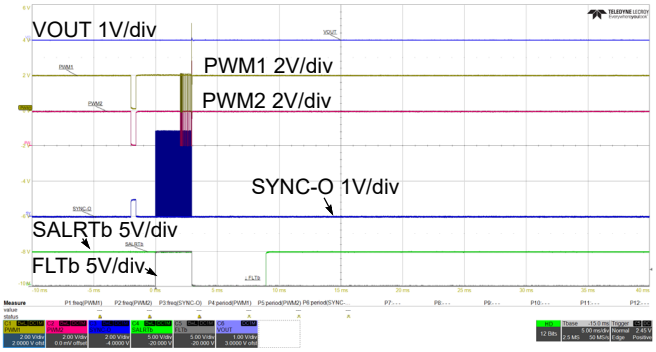


Figure 121. OPERATION Bit Startup into ON_FAULT Latch-Off Response (V_DD = 19V, PVIN = 12V, FAULT_RESPONSE = ON_FAULT Latch-Off, R_{FS} = 350kΩ))

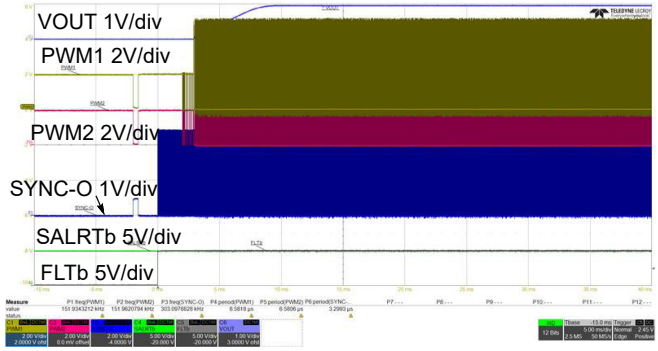


Figure 122. OPERATION Bit Startup with ON_FAULT Masked (V_{DD} = 19V, PVIN = 12V, I_{LOAD} = 50A, FAULT_MASK = ON_FAULT)

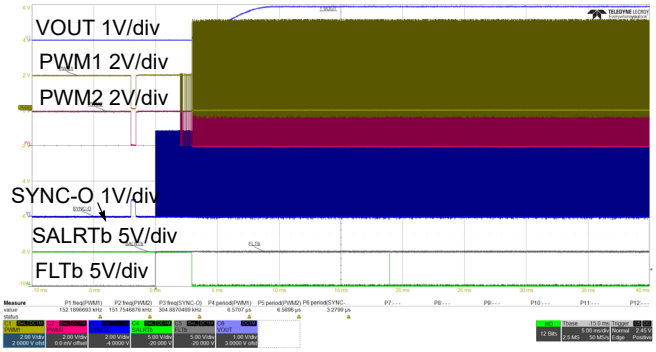


Figure 123. OPERATION Bit Startup with ON_FAULT Masked and SALERT Unmasked (V_{DD} = 19V, PVIN = 12V, I_{LOAD} = 50A, FAULT_MASK = ON_FAULT, SALERT_MASK_OVERRIDE = ON_FAULT)

4.9 Load Transient

Unless otherwise noted: V_{OUT} = 1V, f_{SW} = 500kHz; L_{OUT}(XAL1010-221) = 220nH per phase, C_{OUT}(T530D227M010ATE006) = 2.64mF total per phase, C_{DROOP} = 56nF, C_{VREF} = 47nF, R_{DROOP} = 0Ω, FS tied to VCC, C_{COMP} = 8.2nF, R_{COMP} = 4.22kΩ, C_{POLE} = 330pF, C_{VCC} = 1µF, R_{SLOPE} = 100kΩ, R_{SENSE} = 2mΩ, R_{FIL} = 30.1Ω, C_{FIL} = 680pF, $R_{FB(TOP)}$ = 3.24kΩ, $R_{FB(BOT)}$ = 4.99kΩ

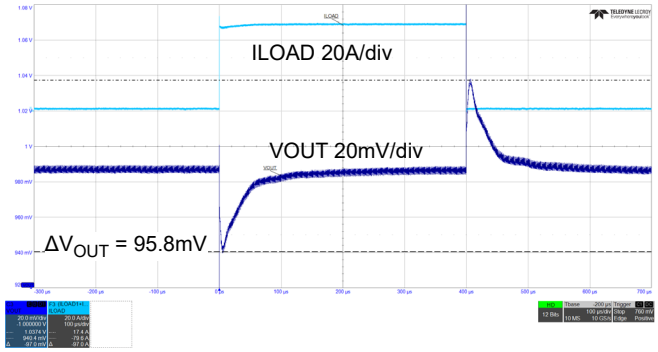


Figure 124. 1V Load Transient Response (V_{DD} = 5V, PVIN = 5V, ΔI_{LOAD} = 0A→50A→0A, R_{DROOP} = 0Ω, V_{REF} = 0.6V)

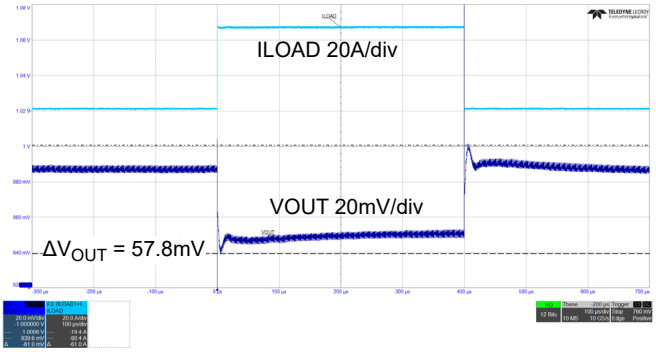


Figure 125. 1V Load Transient Response (V_{DD} = 5V, PVIN = 5V, ΔI_{LOAD} = 0A→50A→0A, R_{DROOP} = 604Ω, V_{REF} = 0.6V)

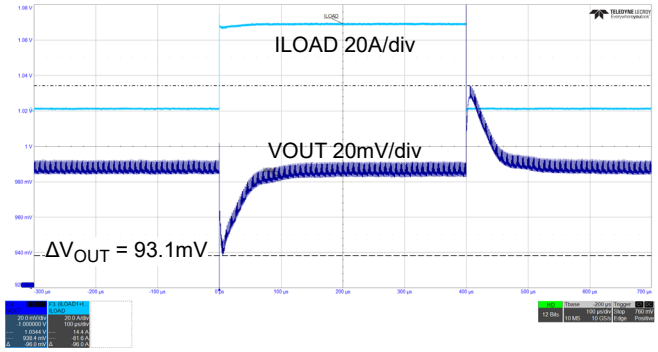


Figure 126. 1V Load Transient Response (V_{DD} = 19V, PVIN = 12V, ΔI_{LOAD} = 0A→50A→0A, R_{DROOP} = 0Ω, V_{REF} = 0.6V)

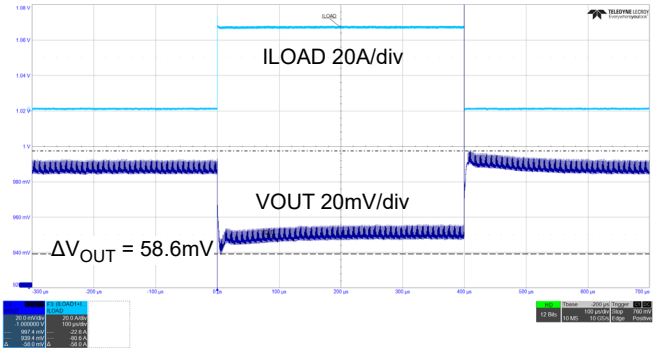


Figure 127. 1V Load Transient Response (V_{DD} = 19V, PVIN = 12V, ΔI_{LOAD} = 0A→50A→0, R_{DROOP} = 604Ω, V_{REF} = 0.6V)

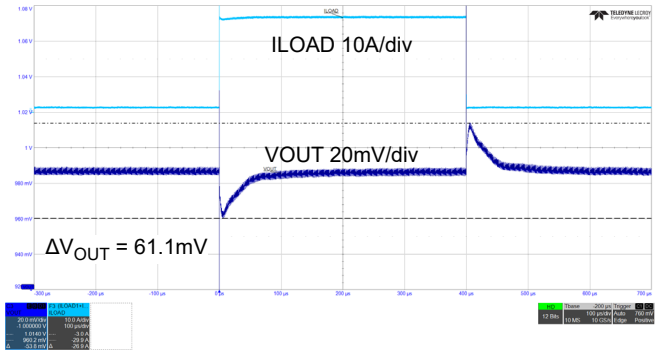


Figure 128. 1V Load Transient Response (V_{DD} = 5V, PVIN = 5V, ΔI_{LOAD} = 0A→25A→0A, R_{DROOP} = 0Ω, V_{REF} = 0.6V)

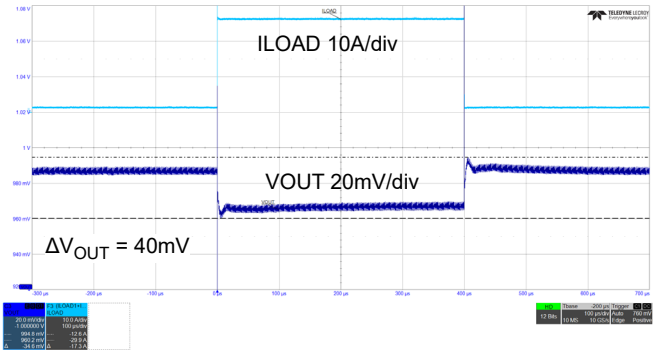


Figure 129. 1V Load Transient Response (V_{DD} = 5V, PVIN = 5V, ΔI_{LOAD} = 0A→25A→0A, R_{DROOP} = 604Ω, V_{REF} = 0.6V)

Unless otherwise noted: V_{OUT} = 1V, f_{SW} = 500kHz; L_{OUT}(XAL1010-221) = 220nH per phase, C_{OUT}(T530D227M010ATE006) = 2.64mF total per phase, C_{DROOP} = 56nF, C_{VREF} = 47nF, R_{DROOP} = 0Ω, FS tied to VCC, C_{COMP} = 8.2nF, R_{COMP} = 4.22kΩ, C_{POLE} = 330pF, C_{VCC} = 1µF, R_{SLOPE} = 100kΩ, R_{SENSE} = 2mΩ, R_{FIL} = 30.1Ω, C_{FIL} = 680pF, $R_{FB(TOP)}$ = 3.24kΩ, $R_{FB(BOT)}$ = 4.99kΩ (Cont.)

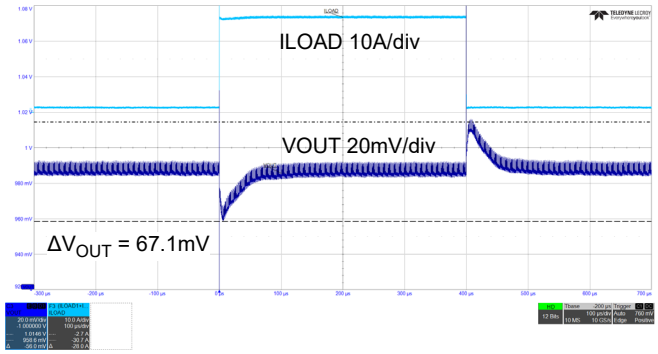


Figure 130. 1V Load Transient Response (V_{DD} = 19V, PVIN = 12V, ΔI_{LOAD} = 0A→25A→0A, R_{DROOP} = 0Ω, V_{REF} = 0.6V)

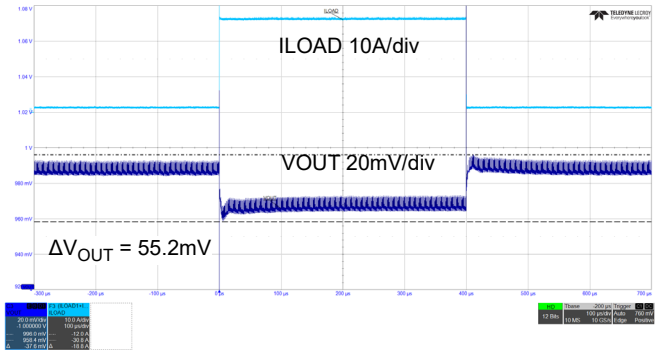


Figure 131. 1V Load Transient Response (V_{DD} = 19V, PVIN = 12V, ΔI_{LOAD} = 0A→25A→0A, R_{DROOP} = 604Ω, V_{REF} = 0.6V)

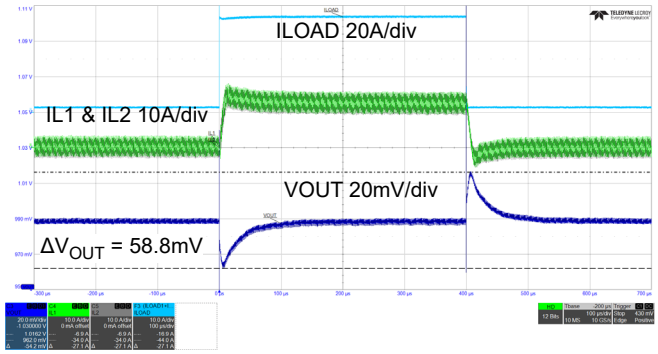


Figure 132. 1mΩ R_{SENSE} 1V Load Transient Response (V_{DD} = 5V, PVIN = 5V, ΔI_{LOAD} = 0A→25A→0A, R_{DROOP} = 0Ω, V_{REF} = 0.6V, R_{SENSE} = 1mΩ, R_{COMP} = 2.1kΩ, C_{COMP} = 2.2nF, C_{POLE} = 630pF)

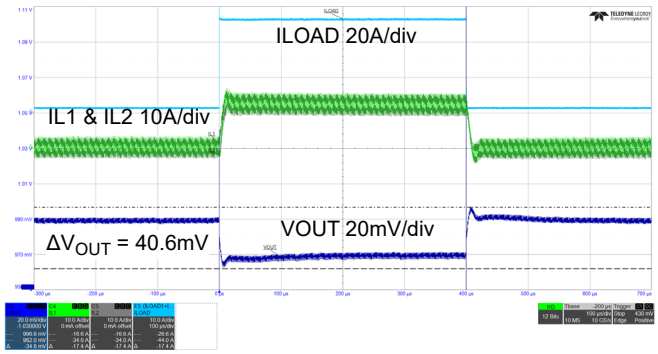


Figure 133. 1mΩ R_{SENSE} 1V Load Transient Response (V_{DD} = 5V, PVIN = 5V, ΔI_{LOAD} = 0A→25A→0A, R_{DROOP} = 604Ω, V_{REF} = 0.6V, R_{SENSE} = 1mΩ, R_{COMP} = 2.1kΩ, C_{COMP} = 2.2nF, C_{POLE} = 630pF)

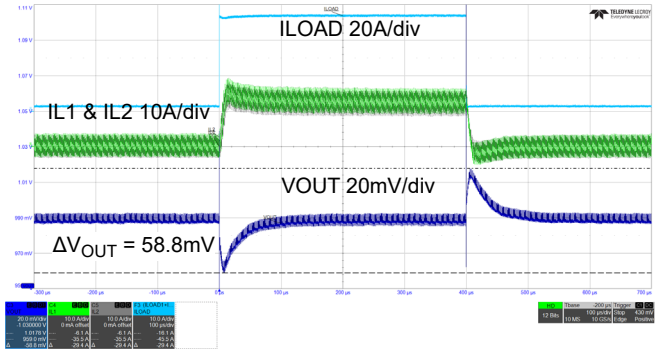


Figure 134. 1mΩ R_{SENSE} 1V Load Transient Response (V_{DD} = 19V, PVIN = 12V, ΔI_{LOAD} = 0A→25A→0A, R_{DROOP} = 0Ω, V_{REF} = 0.6V, R_{SENSE} = 1mΩ, R_{COMP} = 2.1kΩ, C_{COMP} = 2.2nF, C_{POLE} = 630pF)

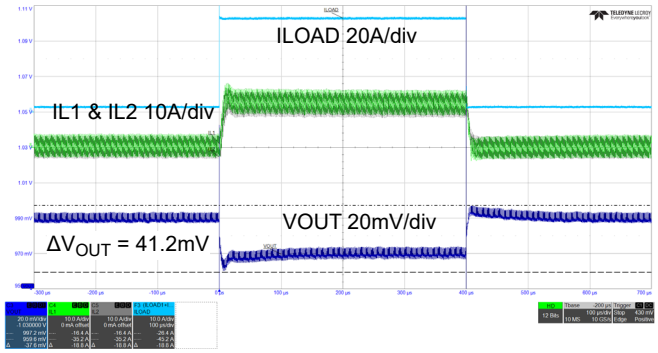


Figure 135. 1mΩ R_{SENSE} 1V Load Transient Response (V_{DD} = 19V, PVIN = 12V, ΔI_{LOAD}=0A→25A→0A, R_{DROOP} = 604Ω, V_{REF} = 0.6V, R_{SENSE} = 1mΩ, R_{COMP} = 2.1kΩ, C_{COMP} = 2.2nF, C_{POLE} = 630pF)

Unless otherwise noted: V_{OUT} = 1V, f_{SW} = 500kHz; L_{OUT}(XAL1010-221) = 220nH per phase, C_{OUT}(T530D227M010ATE006) = 2.64mF total per phase, C_{DROOP} = 56nF, C_{VREF} = 47nF, R_{DROOP} = 0Ω, FS tied to VCC, C_{COMP} = 8.2nF, R_{COMP} = 4.22kΩ, C_{POLE} = 330pF, C_{VCC} = 1µF, R_{SLOPE} = 100kΩ, R_{SENSE} = 2mΩ, R_{FIL} = 30.1Ω, C_{FIL} = 680pF, $R_{FB(TOP)}$ = 3.24kΩ, $R_{FB(BOT)}$ = 4.99kΩ (Cont.)

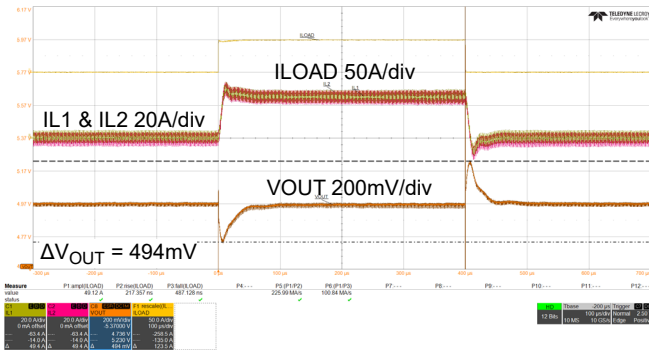


Figure 136. 5V Load Transient Response (V_{DD} = 19V, PVIN = 12V, ΔI_{LOAD} = 0A→50A→0A, R_{DROOP} = 0Ω, V_{REF} = 0.6V, V_{OUT} = 5V, $L_{OUT(XAL1010-682)}$ = 680nH per phase, $R_{FB(TOP)}$ = 38.2kΩ, $C_{OUT(T530D227M010ATE006)}$ = 440uF total per phase))

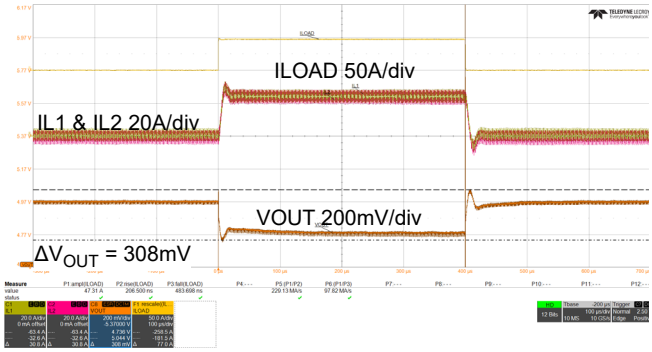


Figure 137. 5V Load Transient Response (V_{DD} = 19V, PVIN = 12V, ΔI_{LOAD} = 0A→50A→0A, R_{DROOP} = 604Ω, V_{REF} = 0.6V, V_{OUT} = 5V, $L_{OUT(XAL1010-682)}$ = 680nH per phase, $R_{FB(TOP)}$ = 38.2kΩ, $C_{OUT(T530D227M010ATE006)}$ = 440µF total per phase)

4.10 VOUT Transition

Unless otherwise noted: V_{DD} = 4.5V and 19V, V_{OUT} = 1V, f_{SW} = 500kHz; L_{OUT}(XAL1010-221) = 220nH per phase, C_{OUT}(T530D227M010ATE006) = 2.64mF total per phase, C_{DROOP}= 56nF, C_{VREF} = 47nF, R_{DROOP} = 0Ω, FS tied to VCC, C_{COMP} = 8.2nF, R_{COMP} = 4.22kΩ, C_{POLE} = 330pF, C_{VCC} = 1µF, R_{SLOPE} = 100kΩ, R_{SENSE} = 2mΩ, RFIL=30.1Ω, C_{FIL} = 680pF, $R_{FB(TOP)}$ = 3.24kΩ, $R_{FB(BOT)}$ = 4.99kΩ

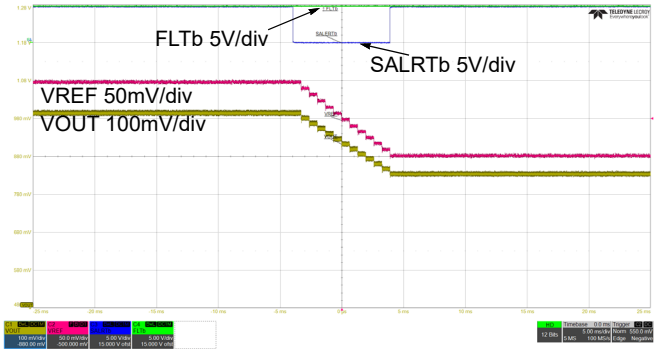


Figure 138. VOUT Transition (V_{DD} = PVIN = 12V, VOUT_COMMAND = 0.6V to 0.496V, VOUT_TRANSITION_RATE = 12.5mV/ms)

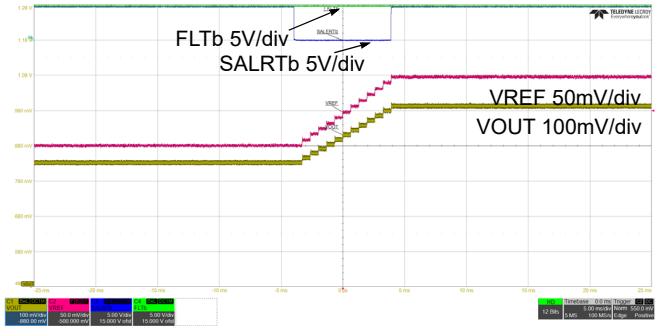


Figure 139. VOUT Transition (V_{DD} = PVIN = 12V, VOUT_COMMAND = 0.496V to 0.6V, VOUT_TRANSITION_RATE = 12.5mV/ms)

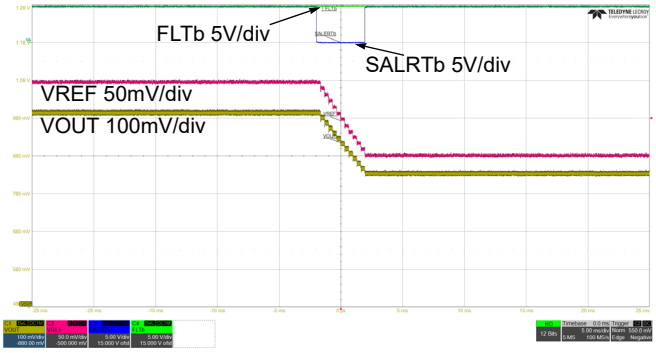


Figure 140. VOUT Transition (V_{DD} = PVIN = 12V, VOUT_COMMAND = 0.6V to 0.496V, VOUT_TRANSITION_RATE = 25mV/ms)

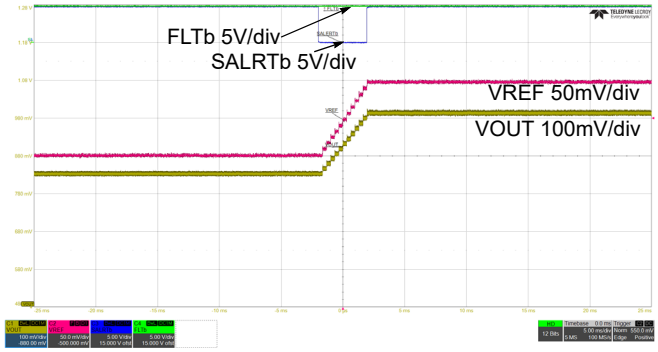


Figure 141. VOUT Transition (V_{DD} = PVIN = 12V, VOUT_COMMAND = 0.496V to 0.6V, VOUT_TRANSITION_RATE = 25mV/ms)

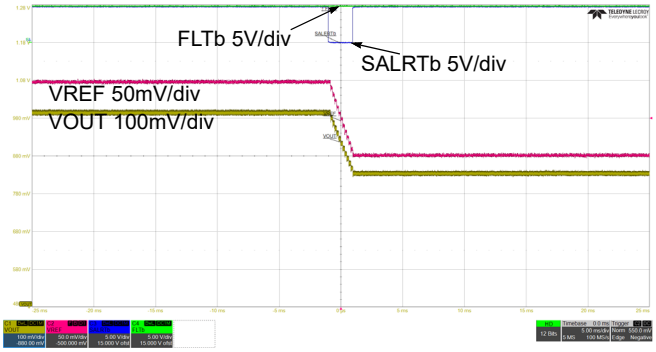


Figure 142. VOUT Transition (V_{DD} = PVIN = 12V, VOUT_COMMAND = 0.6V to 0.496V, VOUT_TRANSITION_RATE = 50mV/ms)

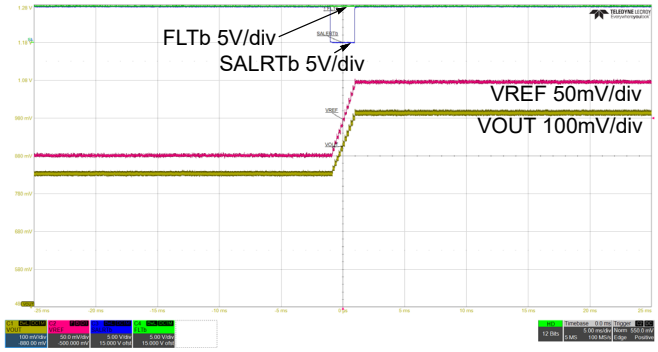


Figure 143. VOUT Transition (V_{DD} = PVIN = 12V, VOUT_COMMAND = 0.496V to 0.6V, VOUT_TRANSITION_RATE = 50mV/ms)

Unless otherwise noted: V_{DD} = 4.5V and 19V, V_{OUT} = 1V, f_{SW} = 500kHz; L_{OUT}(XAL1010-221) = 220nH per phase, C_{OUT}(T530D227M010ATE006) = 2.64mF total per phase, C_{DROOP}= 56nF, C_{VREF} = 47nF, R_{DROOP} = 0Ω, FS tied to VCC, C_{COMP} = 8.2nF, R_{COMP} = 4.22kΩ, C_{POLE} = 330pF, C_{VCC} = 1µF, R_{SLOPE} = 100kΩ, R_{SENSE} = 2mΩ, RFIL=30.1Ω, C_{FIL} = 680pF, $R_{FB(TOP)}$ = 3.24kΩ, $R_{FB(BOT)}$ = 4.99kΩ (Cont.)

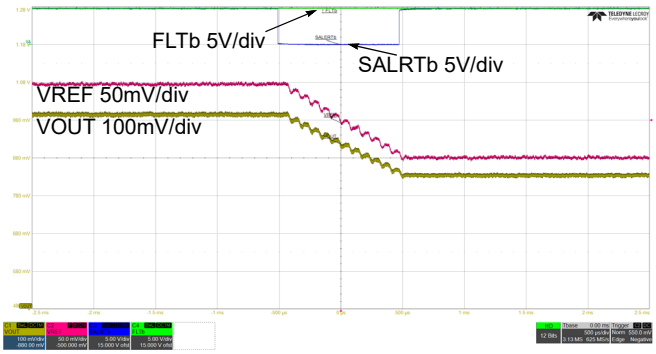


Figure 144. VOUT Transition (V_{DD} = PVIN = 12V, VOUT_COMMAND = 0.6V to 0.496V, VOUT_TRANSITION_RATE = 100mV/ms)

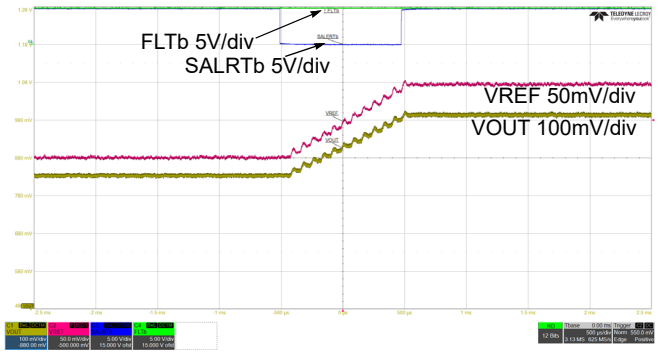


Figure 145. VOUT Transition (V_{DD} = PVIN = 12V, VOUT_COMMAND = 0.496V to 0.6V, VOUT_TRANSITION_RATE= 100mV/ms)

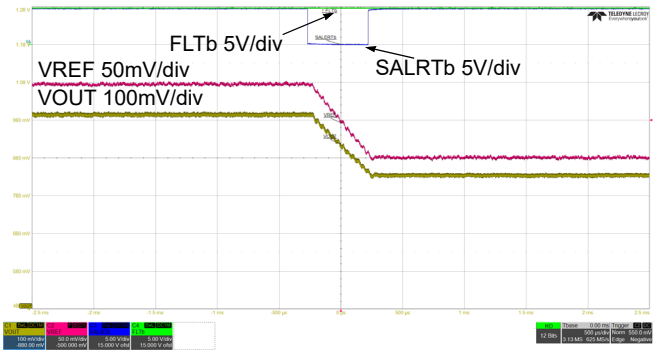


Figure 146. VOUT Transition (V_{DD} = PVIN = 12V, VOUT_COMMAND = 0.6V to 0.496V, VOUT_TRANSITION_RATE = 200mV/ms)

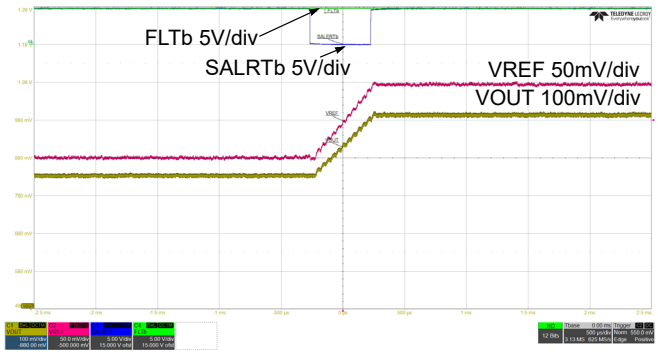


Figure 147. VOUT Transition (V_{DD} = PVIN = 12V, VOUT_COMMAND = 0.496V to 0.6V, VOUT_TRANSITION_RATE = 200mV/ms)

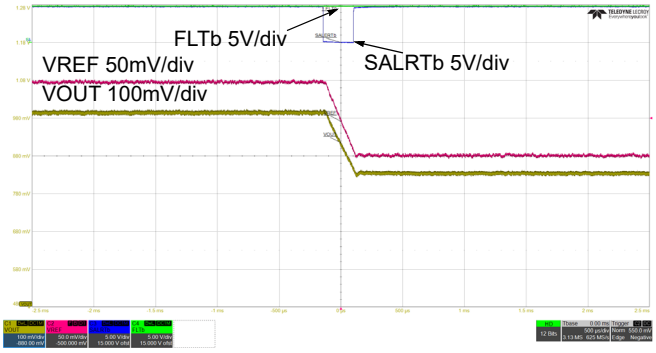


Figure 148. VOUT Transition (V_{DD} = PVIN = 12V, VOUT_COMMAND = 0.6V to 0.496V, VOUT_TRANSITION_RATE = 400mV/ms)

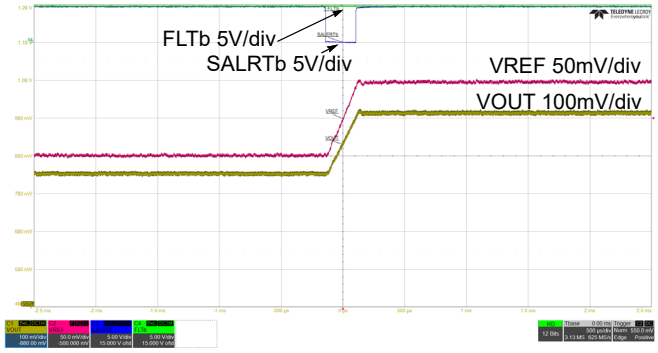


Figure 149. VOUT Transition (V_{DD} = PVIN = 12V, VOUT_COMMAND = 0.496V to 0.6V, VOUT_TRANSITION_RATE= 400mV/ms)

Unless otherwise noted: V_{DD} = 4.5V and 19V, V_{OUT} = 1V, f_{SW} = 500kHz; L_{OUT}(XAL1010-221) = 220nH per phase, C_{OUT}(T530D227M010ATE006) = 2.64mF total per phase, C_{DROOP}= 56nF, C_{VREF} = 47nF, R_{DROOP} = 0Ω, FS tied to VCC, C_{COMP} = 8.2nF, R_{COMP} = 4.22kΩ, C_{POLE} = 330pF, C_{VCC} = 1µF, R_{SLOPE} = 100kΩ, R_{SENSE} = 2mΩ, RFIL=30.1Ω, C_{FIL} = 680pF, $R_{FB(TOP)}$ = 3.24kΩ, $R_{FB(BOT)}$ = 4.99kΩ (Cont.)

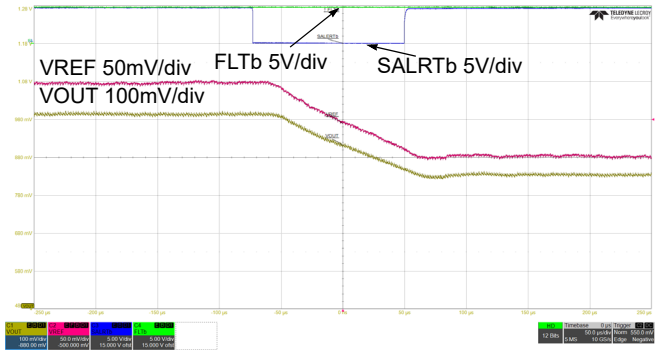


Figure 150. VOUT Transition (V_{DD} = PVIN = 12V, VOUT_COMMAND = 0.6V to 0.496V, VOUT_TRANSITION_RATE = 800mV/ms)

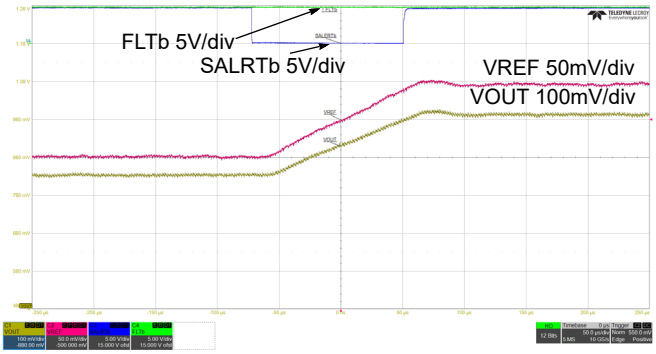


Figure 151. VOUT Transition (V_{DD} = PVIN = 12V, VOUT_COMMAND = 0.496V to 0.6V, VOUT_TRANSITION_RATE= 800mV/ms)

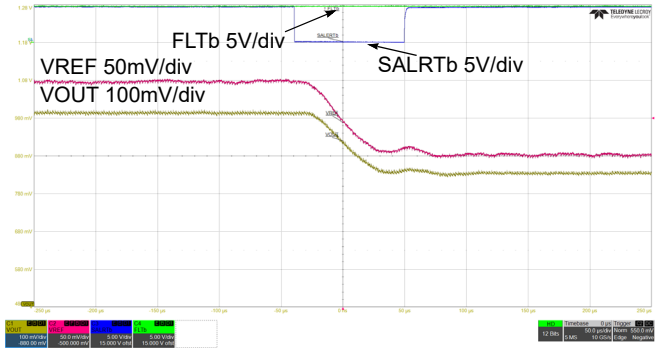


Figure 152. VOUT Transition (V_{DD} = PVIN = 12V, VOUT_COMMAND = 0.6V to 0.496V, VOUT_TRANSITION_RATE= 1600mV/ms)

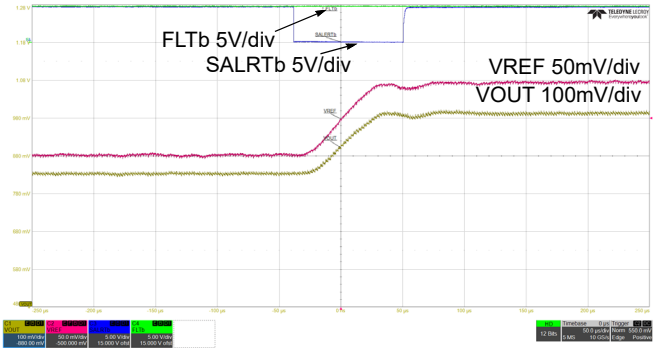


Figure 153. VOUT Transition (V_{DD} = PVIN = 12V, VOUT_COMMAND = 0.496V to 0.6V, VOUT_TRANSITION_RATE= 1600mV/ms)

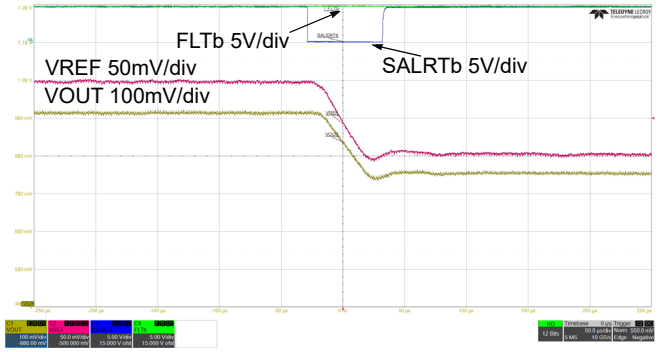


Figure 154. VOUT Transition (V_{DD} = PVIN = 12V, VOUT_COMMAND = 0.6V to 0.496V, VOUT_TRANSITION_RATE= 3200mV/ms)

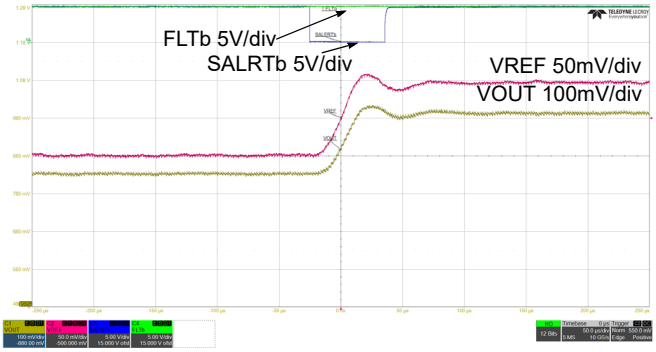


Figure 155. VOUT Transition (V_{DD} = PVIN = 12V, VOUT_COMMAND = 0.496V to 0.6V, VOUT_TRANSITION_RATE= 3200mV/ms)

Unless otherwise noted: V_{DD} = 4.5V and 19V, V_{OUT} = 1V, f_{SW} = 500kHz; L_{OUT}(XAL1010-221) = 220nH per phase, C_{OUT}(T530D227M010ATE006) = 2.64mF total per phase, C_{DROOP}= 56nF, C_{VREF} = 47nF, R_{DROOP} = 0Ω, FS tied to VCC, C_{COMP} = 8.2nF, R_{COMP} = 4.22kΩ, C_{POLE} = 330pF, C_{VCC} = 1µF, R_{SLOPE} = 100kΩ, R_{SENSE} = 2mΩ, RFIL=30.1Ω, C_{FIL} = 680pF, $R_{FB(TOP)}$ = 3.24kΩ, $R_{FB(BOT)}$ = 4.99kΩ (Cont.)

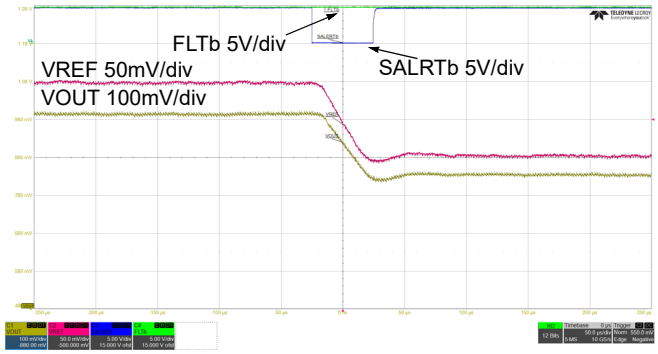


Figure 156. VOUT Transition (V_{DD} = PVIN = 12V, VOUT_COMMAND = 0.6V to 0.496V, VOUT_TRANSITION_RATE= 5333mV/ms)

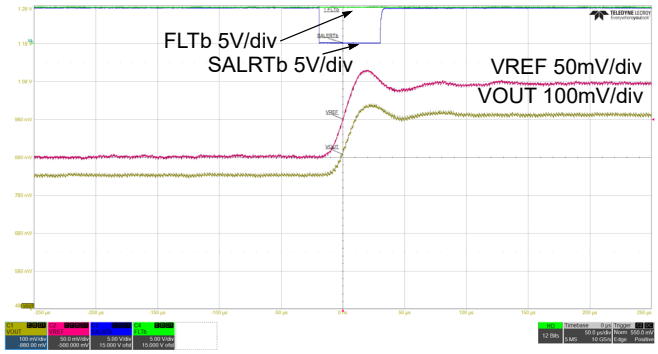


Figure 157. VOUT Transition (V_{DD} = PVIN = 12V, VOUT_COMMAND = 0.496V to 0.6V, VOUT_TRANSITION_RATE=5333mV/ms)

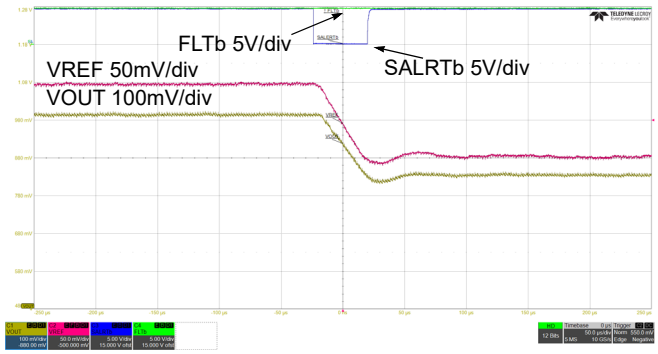


Figure 158. VOUT Transition (V_{DD} = PVIN = 12V, VOUT_COMMAND = 0.6V to 0.496V, VOUT_TRANSITION_RATE= 8000mV/ms)

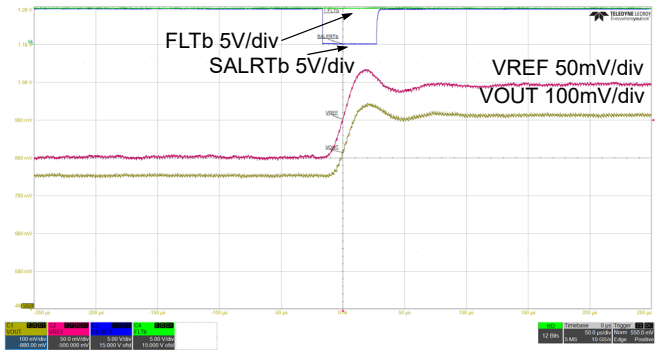


Figure 159. VOUT Transition (V_{DD} = PVIN = 12V, VOUT_COMMAND = 0.496V to 0.6V, VOUT_TRANSITION_RATE= 8000mV/ms)

4.11 Gain and Phase

Unless otherwise noted: V_{DD} = 4.5V and 19V, V_{OUT} = 1V, f_{SW} = 500kHz; L_{OUT}(XAL1010-221) = 220nH per phase, C_{OUT}(T530D227M010ATE006) = 2.64mF total per phase, C_{DROOP}= 56nF, C_{VREF} = 47nF, R_{DROOP} = 0Ω, FS tied to VCC, C_{COMP} = 8.2nF, R_{COMP} = 4.22kΩ, C_{POLE} = 330pF, C_{VCC} = 1µF, R_{SLOPE} = 100kΩ, R_{SENSE} = 2mΩ, RFIL=30.1Ω, C_{FIL} = 680pF, $R_{FB(TOP)}$ = 3.24kΩ, $R_{FB(BOT)}$ = 4.99kΩ

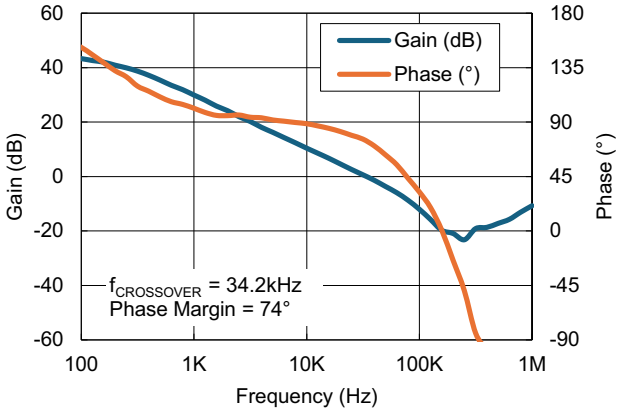


Figure 160. Gain and Phase vs Frequency (V_{DD} = PVIN = 5V, I_{LOAD} = 0A)

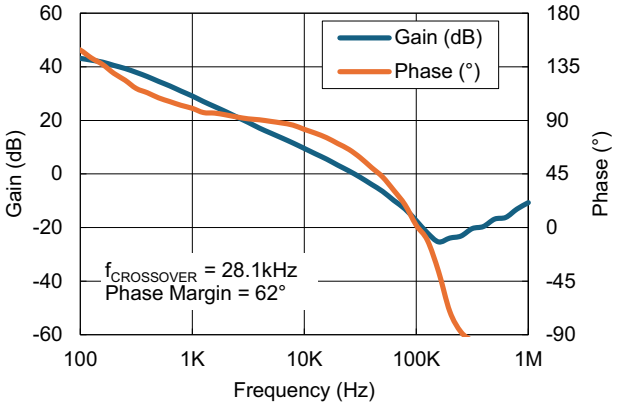


Figure 161. Gain and Phase vs Frequency (V_{DD} = PVIN = 12V, I_{LOAD} = 0A)

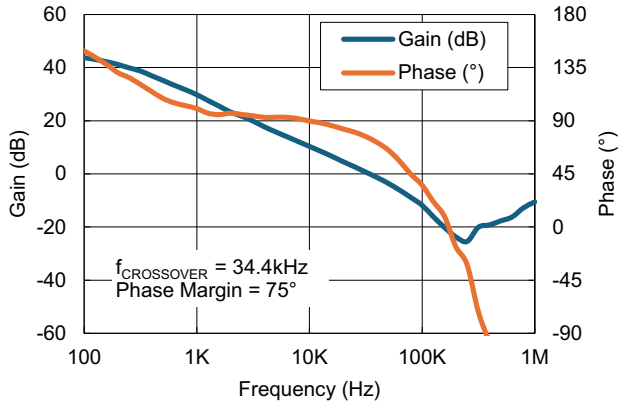


Figure 162. Gain and Phase vs Frequency (V_{DD} = PVIN = 5V, I_{LOAD} = 25A)

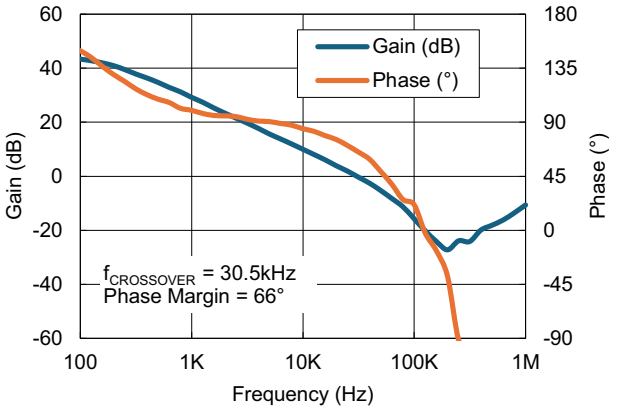


Figure 163. Gain and Phase vs Frequency (V_{DD} = PVIN = 12V, I_{LOAD} = 25A)

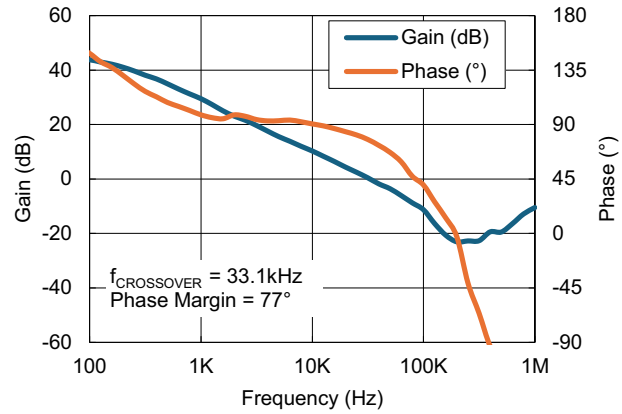


Figure 164. Gain and Phase vs Frequency (V_{DD} = PVIN = 5V, I_{LOAD} = 50A)

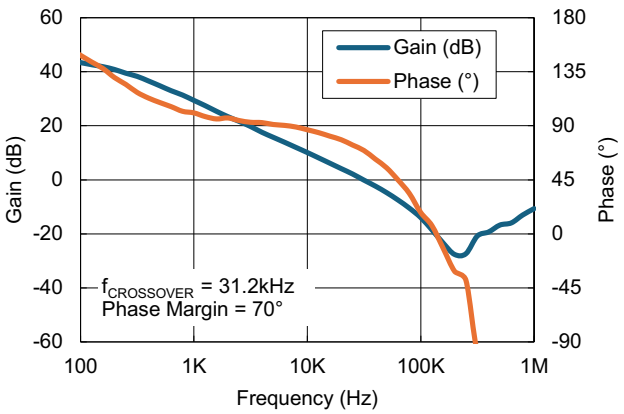


Figure 165. Gain and Phase vs Frequency (V_{DD} = PVIN = 12V, I_{LOAD} = 50A)

5. Operational Description

5.1 Dual-Phase Operation

The ISL73849SLH can operate in single-phase or dual-phase mode. The part is configured to work in dual-phase mode by default. To operate in single-phase mode, short the PWM output to VCC. Either PWM1 or PWM2 can be chosen for single-phase operation so long as the other is shorted to VCC. The flexibility of using either output in single phase can help during layout as it may be easier to route the current-sense feedback signals to one channel or the other.

5.2 Oscillator and Clock Synchronization

5.2.1 Oscillator

The switching frequency of the controller is determined by a resistor to ground on the FS pin (R_{FS}). The ISL73849SLH can operate with an oscillator frequency in the range of 500kHz to 3MHz. If the FS pin is shorted to ground while the device is operating, the ISL73849SLH reads this as a fault and stop switching. If the FS pin is shorted to ground and then the device is powered up, the ISL73849SLH does not switch and the PWM outputs sit at 2V midscale voltage. However, no fault is issued and SALRTb is not set LOW.

5.2.2 External Synchronization (SYNC-I)

The ISL73849SLH has a SYNC-I pin that allows the user to synchronize it to an external clock. It is necessary to set the internal oscillator to 15% less than the required external oscillator's frequency to use this functionality, ensuring that if the SYNC-I input frequency stops at any point in time, the internal oscillator takes over and continues operating. The allowable frequency range for the external clock is 588kHz to 3MHz. The SYNC-I frequency should be twice the required PWM switching frequency.

Note: The maximum SYNC-I frequency should not exceed the maximum oscillator frequency (3MHz).

5.2.3 Clock Output (SYNC-O)

The ISL73849SLH has a SYNC-O pin that can output either the oscillator frequency or the PWM switching frequency. Place a 100kΩ resistor on SYNC-O to ground to output the oscillator frequency. To get the PWM switching frequency leave the SYNC-O pin floating. The choice to use one or the other depends on what is receiving the clock pulse. If the clock output is being used to synchronize another ISL73849SLH, it expects a frequency that is twice the PWM switching frequency (load the pin with 100kΩ to ground). Other PWM regulators, such as the ISL7000x family of parts, switch at the same frequency as the incoming frequency (leave the pin floating). When SYNC-O is unloaded, it is in phase with PWM2. During a fault condition, the SYNC-O is asserted low.

5.2.4 Multi-Phase Operation

More phases can be added to the system by connecting multiple ISL73849SLH devices together in a single leader, multi-follower configuration. To synchronize the two or more controllers external clocks can be supplied to the SYNC-I inputs. The frequency of the clocks should be twice the target switching frequency. The phase relationship between the clocks depends on the number of controllers being synchronized. Use Equation 1 to calculate the recommended phase delay required between each SYNC-I clock depending on the number of controllers. The total phase delay should add up to 360°.

(EQ. 1) $$\text{Phase[deg]} = \frac{360}{\text{Controllers}}$$

A simple way to synchronize a 4-phase design is to use the SYNC-O of the leader controller to drive the SYNC-I of the follower controller as shown in Figure 166. The SYNC-O pin needs a 100kΩ to GND to output twice the switching frequency. Because the internal oscillator of the Follower must be set to 15% lower than the external clock, the RFS and RSLOPE resistors are different from the Leader. For a 1MHz switching frequency, the SYNC-O to PWMx delay from the Leader (typically 32ns) and the SYNC-I to SYNC-O delay of the Follower

(typically 242ns) create the 180° phase delay required to drive the SYNC-I of the Follower directly from the SYNC-O of the Leader. As shown, tie the DROOP pins together, tie all the VFB- pins together, and tie all the FLTb pins together. Tie the COMP pins of all controllers together and only install the compensation components on the leader. Lastly, tie the FB+ pin on each follower to its own DROOP pin.

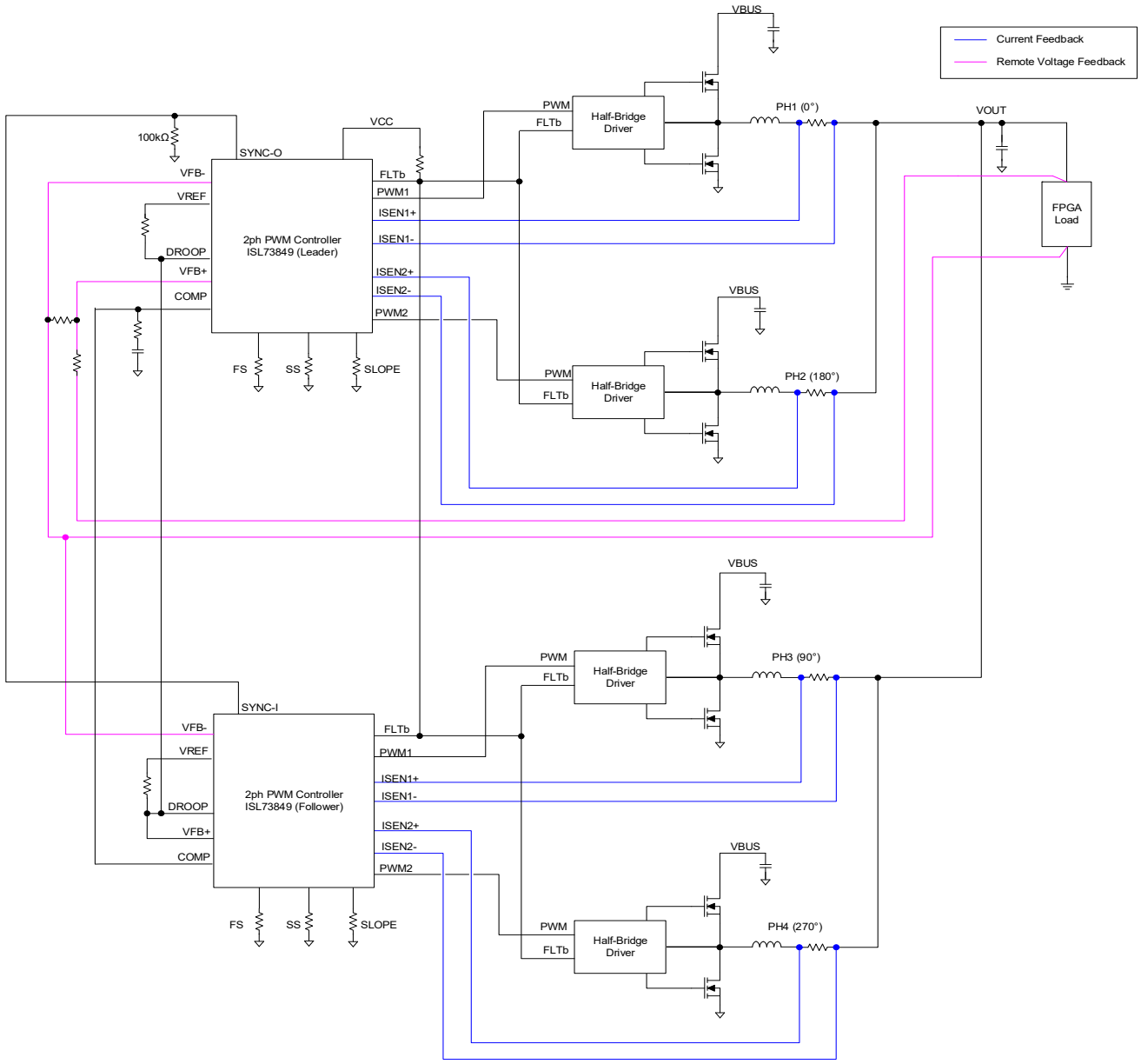


Figure 166. Leader-Follower Configuration for 1MHz 4-Phase Operation

Figure 167 is an oscilloscope capture where 86° phase separation is obtained between Phase 1 and Phase 3 by driving the SYNC-I of the follower with the SYNC-O of the leader directly with no extra delay circuit.

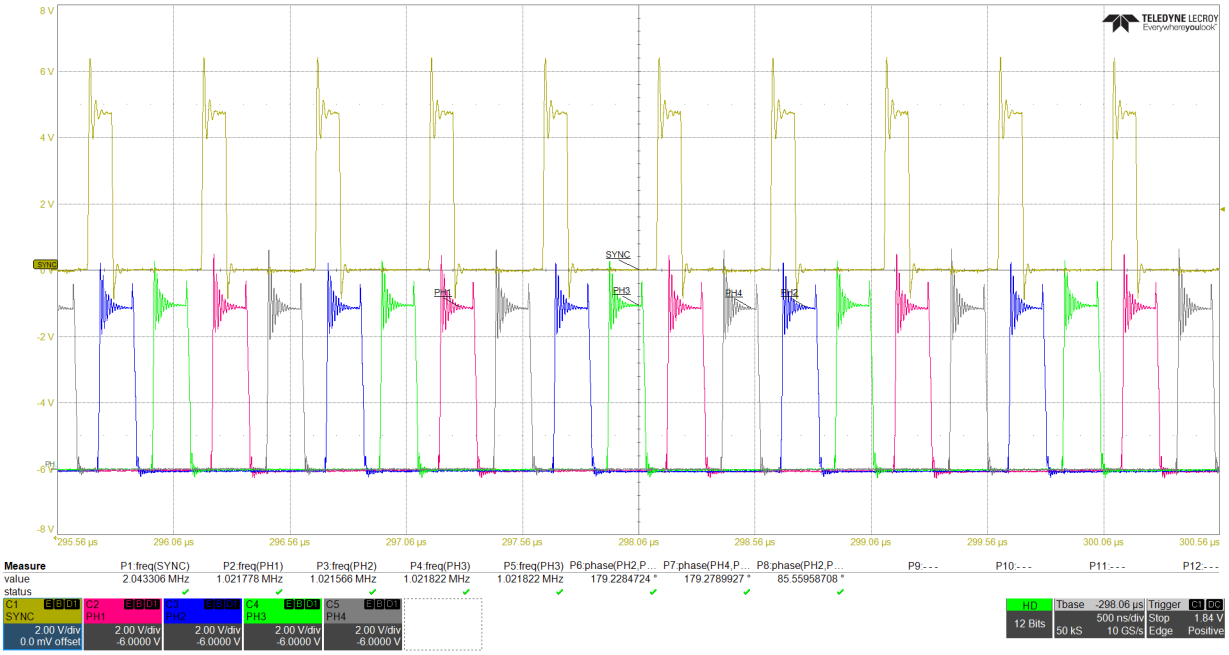


Figure 167. Using SYNC-O of Leader to drive SYNC-I of Follower Phase Shifting

For frequencies above 1MHz or phase counts over 4, an external delay circuit is required. This can be discreetly placed between the leader's SYNC-O and the follower's SYNC-I (Figure 168) or more flexibly with a smaller solution size using the ISL74420 (Figure 169).

Use Equation 2 to calculate the time delay from phase.

(EQ. 2) $$Delay = \frac{Phase}{(720 \times f_{SW})}$$

- Delay is the time delay in seconds.
- Phase is the phase delay in degrees.
- f_{SW} is the target switching frequency in Hertz.

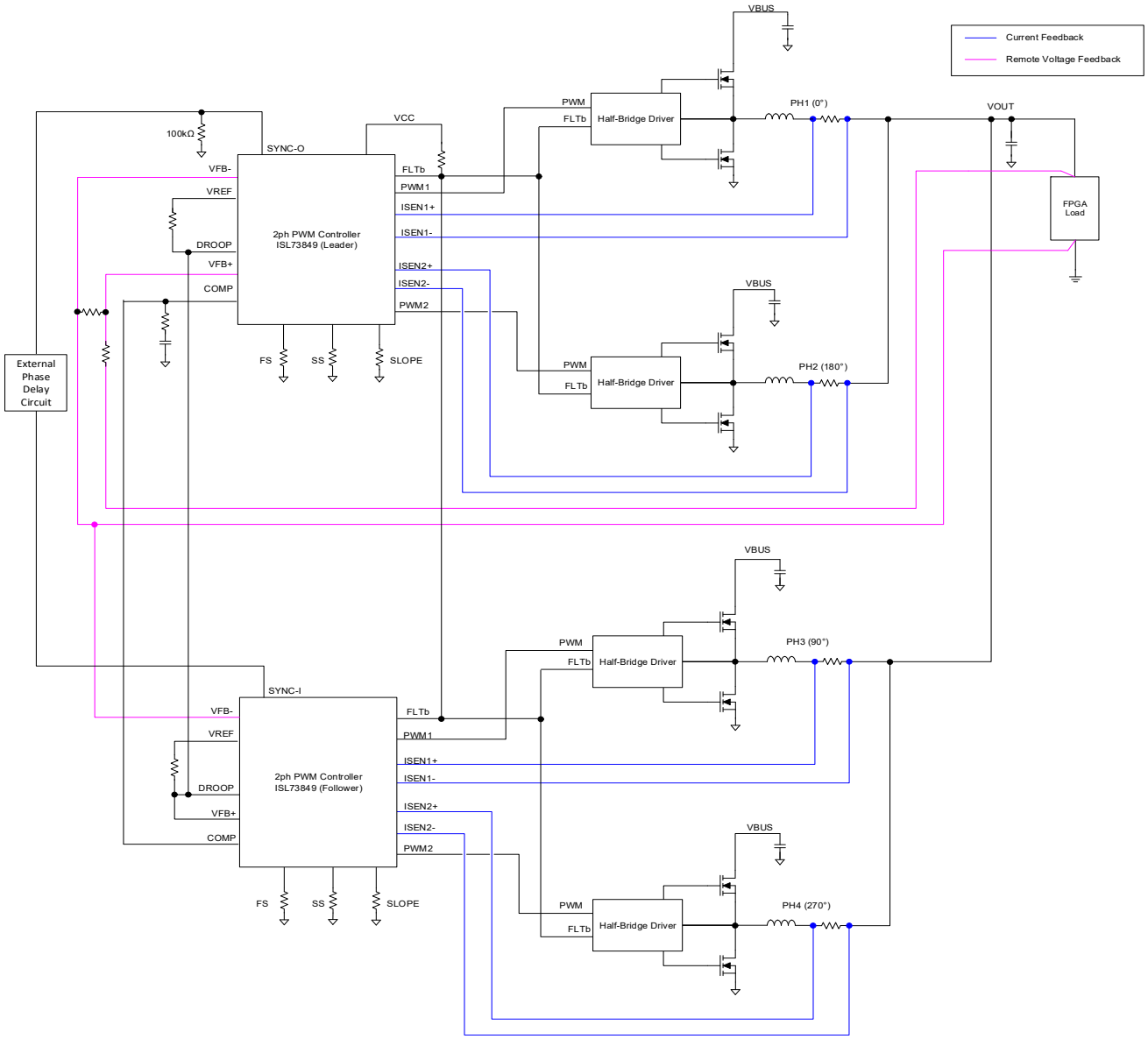


Figure 168. Leader-Follower Configuration for 4-Phase Operation

Another way to synchronize multiple ISL73849SLH devices is to use the ISL74420. Figure 169 is an example of a 4-phase using the ISL74420 to provide one clock to each controller. Both clocks are twice the converter switching frequency and 180° out-of-phase with each other for ideal multi-phase interleaving.

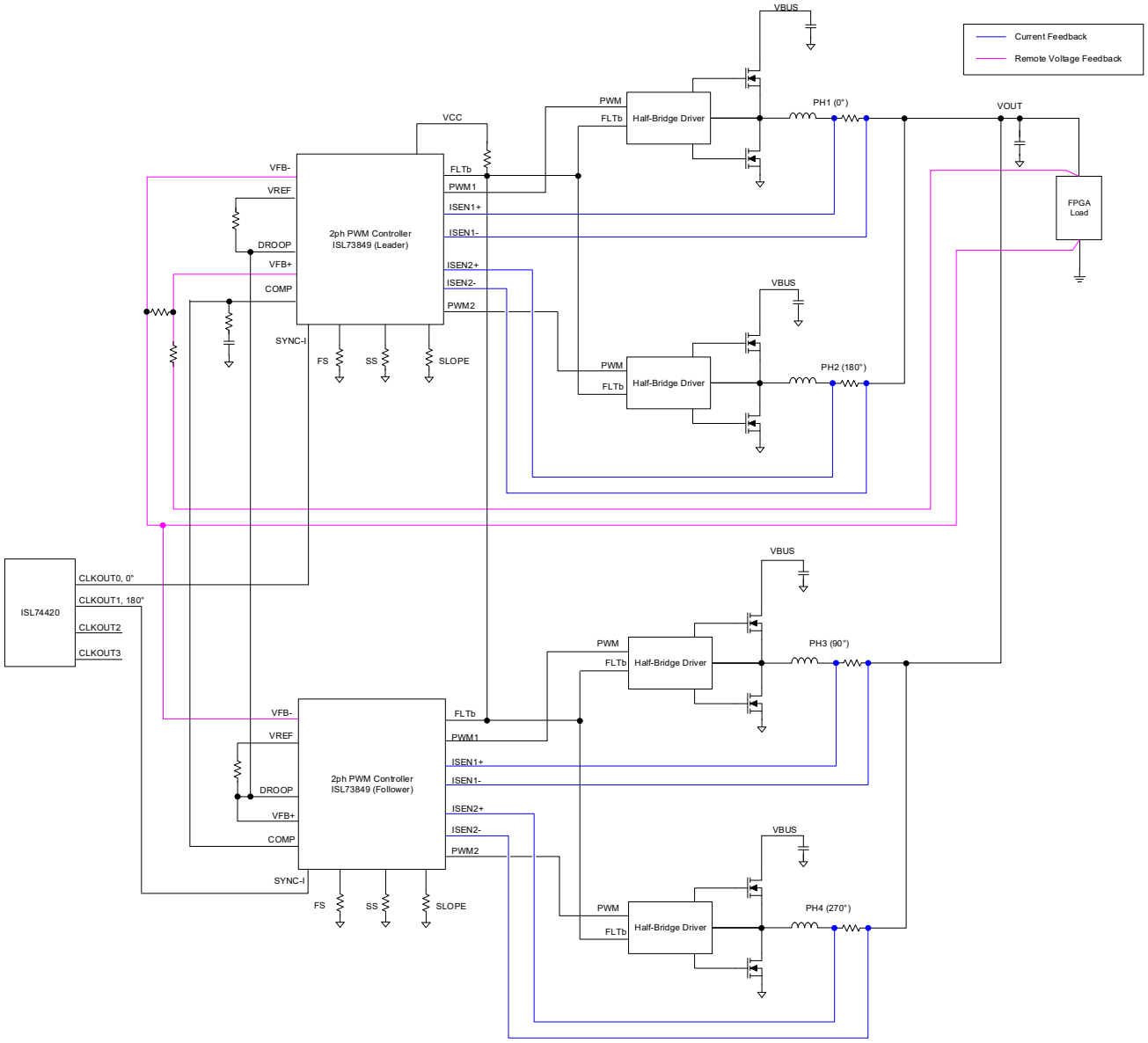


Figure 169. Leader-Follower Configuration for 4-Phase Operation

Figure 170 is an oscilloscope capture for a 4-phase, 1MHz, 5V to 0.8V, 100A reference design that uses the ISL74420 to output two 2MHz clocks, 180° out-of-phase for synchronization.

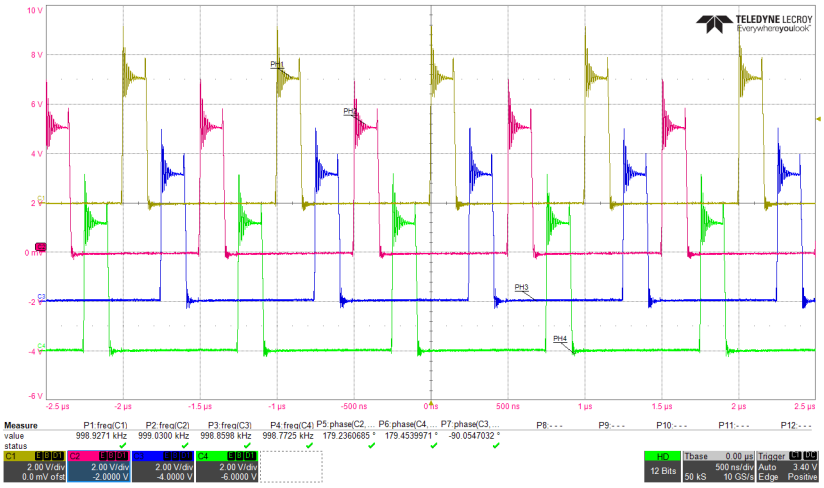


Figure 170. 4-Phase Clock Phase Shifting

5.3 Differential Remote Sensing

The ISL73849SLH can provide differential remote sensing. This allows for the power stage to reside close to the point of load, while having the controller further away to reduce the possibility of noise injection due to switching noise from the power stage. In this configuration, the remote sensing also allows the ISL73849SLH to compensate for any loss along the copper planes carrying large currents.

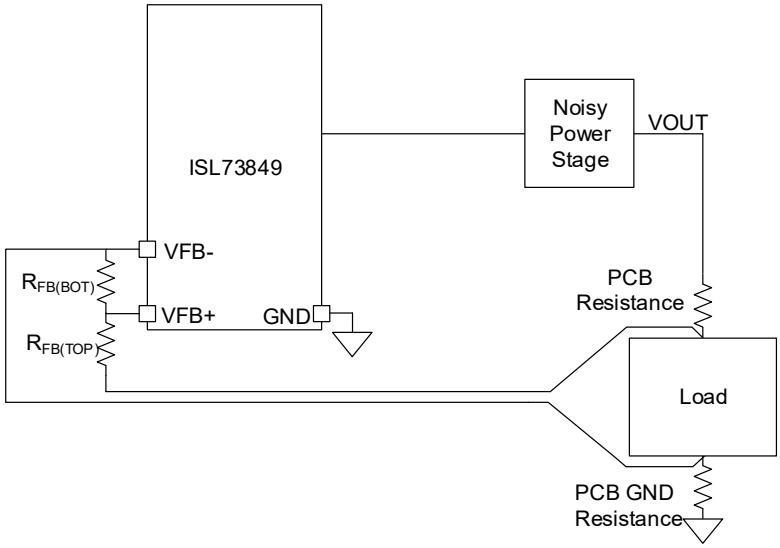


Figure 171. Differential Remote Sensing

5.4 Droop Regulation

Droop regulation can be used to minimize transient voltages on the regulated output during large load steps. It works by lowering the output voltage as the load current increases, effectively increasing the DC output impedance for the power supply.

Droop is tuned by adding a resistor between VREF and DROOP. The ISL73849SLH sinks a current on DROOP that is proportional to the sum of the differential voltage across both current-sense inputs. This current through the resistor between VREF and DROOP changes the reference voltage presented to the error amplifier and thereby

changes the DC regulation point. The larger the resistor, the larger the DROOP in regulated voltage with respect to load current.

5.5 Peak Current Mode Control

The ISL73849SLH uses a high-speed transconductance amplifier (minimum 10MHz bandwidth) to enable continuous peak current-mode control by accurately sensing the inductor current. For low common-mode voltages across ISEN+ and ISEN- the amplifier is set for low-side sensing. For higher common-mode voltages, the amplifier switches to high-side sensing. The transition from low-side sensing to high-side sensing is 2.11V to 2.4V typical for VDD of 4.5V to 19V. The low-side amplifier is supplied internally by VCC. The high-side amplifier is supplied by VCC when VOUT is less than VCC. The high-side amplifier switches its supply to VOUT when VOUT is greater than VCC. The device presents the current-sense signal directly to the PWM comparator. The PWM pulse is terminated when the current crosses the error amplifier output.

5.6 Tri-State PWM Control

The ISL73849SLH features a tri-level PWM output that can output a low, high and mid-level voltage. The high-level output is meant to turn on the high-side FET, while a low-level output is meant to turn on the low-side FET. The mid level output is meant to turn off both the high and low side FETs. This state is helpful during fault conditions where protecting any downstream devices and the power stage is required.

The ISL73849SLH works with drivers that accept a tri-level input, like the ISL73041SEH.

5.7 Boot Refresh

When the ISL73849SLH first powers up, prior to soft start, it issues a boot refresh command that consists of 32 mid to low transitions on the PWM output. This should allow sufficient time for the boot capacitor to charge up. The frequency of the boot refresh pulses is determined by the switching frequency and the pulse is equal to the minimum on time (t_{MINON}). Using the frequency and pulse widths, an appropriate boot capacitor value can be determined.

Whenever the ISL73849SLH is tri-stated it starts a analog timer that lasts 71µs (typical). Four additional boot refresh pulses are transmitted to ensure the boot voltage is replenished if the timer completes before the next high-level signal. This would be the case in a pre-biased startup, where there could be a significant amount of time between the boot refresh pulses and the first high-side turn on.

5.8 Adjustable Slope Compensation

The ISL73849SLH is a peak current mode controller whose nature makes it prone to subharmonic oscillations when the duty cycle is greater than 50%. By adding a compensating ramp equal to the down slope of the inductor, current can dampen any subharmonic oscillation within one switching cycle. If the nominal duty is under but close to 50%, Renesas recommends using adequate slope compensation as the duty cycle could cross 50% as the load increases. The slope compensation depends upon the SLOPE pin and the FS pin.

If slope compensation is not enough, the converter can experience subharmonic oscillation, which could result in noise emissions at half the switching frequency. However, too much slope compensation can deteriorate the phase margin therefore the slope compensation must be carefully considered.

5.9 Pulse Skipping

The ISL73849SLH can skip pulses if the feedback indicates that the minimum pulse width is excessive. One scenario where this could arise could be during a load release when operating close to the minimum on time. Pulse skipping reduces the overshoot during the unloading in a transient step.

5.10 VDD and VCC Range

The ISL73849SLH has an internal LDO that provides the bias for all internal circuitry. The LDO's input is VDD which accepts a range of 4.5V up to 19V. VCC is the output of the LDO which regulates 5V. When VDD is operating in the range of 4.5V to 5.0V, VCC tracks VDD minus the dropout.

5.11 Enable

The ISL73849SLH features a 2-stage enable. When enable is at 1.3V typical (gross threshold), the internal circuitry is biased (reference voltage, oscillator, logic) but switching is disabled. The ISL73849SLH can also be programmed with PMBus in this biased state. When the voltage of EN is at 1.8V typical (fine threshold), switching is enabled and the IC attempts a boot refresh and soft start. The EN pin has internal 80uS typical filter to mitigate Single Event Effects (SEE). The EN logic state (high or low) must persist for at least 80µs for the part to recognize it and respond. The EN pin has a pull-down that disables the part if the pin is not actively driven.

5.12 Initialization and Startup

When the ISL73849SLH first powers up, it goes through several states prior to boot refresh and soft-start. After VDD has crossed the rising UVLO threshold, the oscillator waits 128 clock cycles at 500kHz before allowing the digital core to enter its configuration state. The configuration state lasts 886 clock cycles at 500kHz. When the digital core completes it configuration, it signals the oscillator to switch to the frequency set by the FS pin or SYNC-I. After an additional 128 clock cycles at the new frequency, boot refresh pulses commence followed by soft start. Figure 172 and Figure 173 illustrate the start-up sequence.

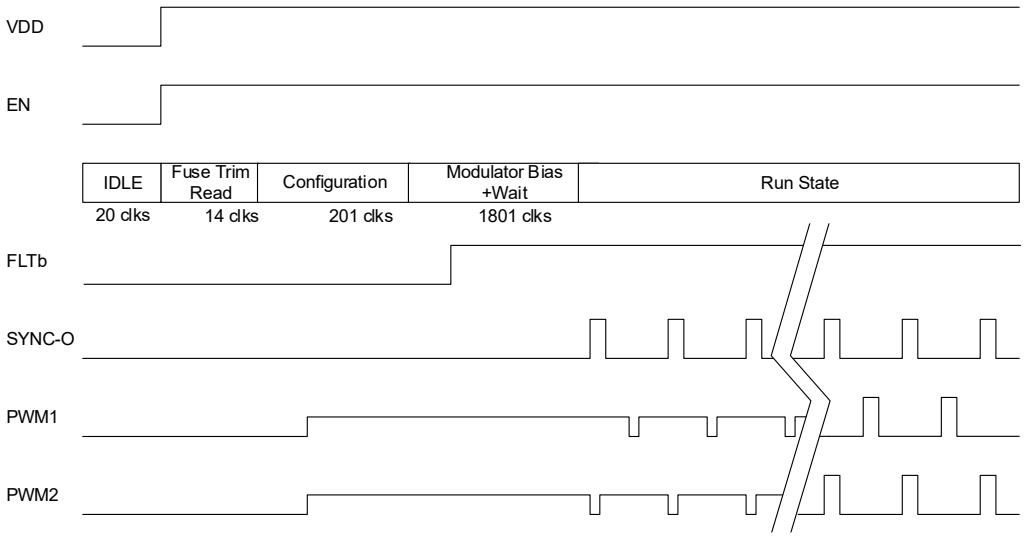


Figure 172. Start Up Timing Diagram (R_{SYNC-O} = OPEN)

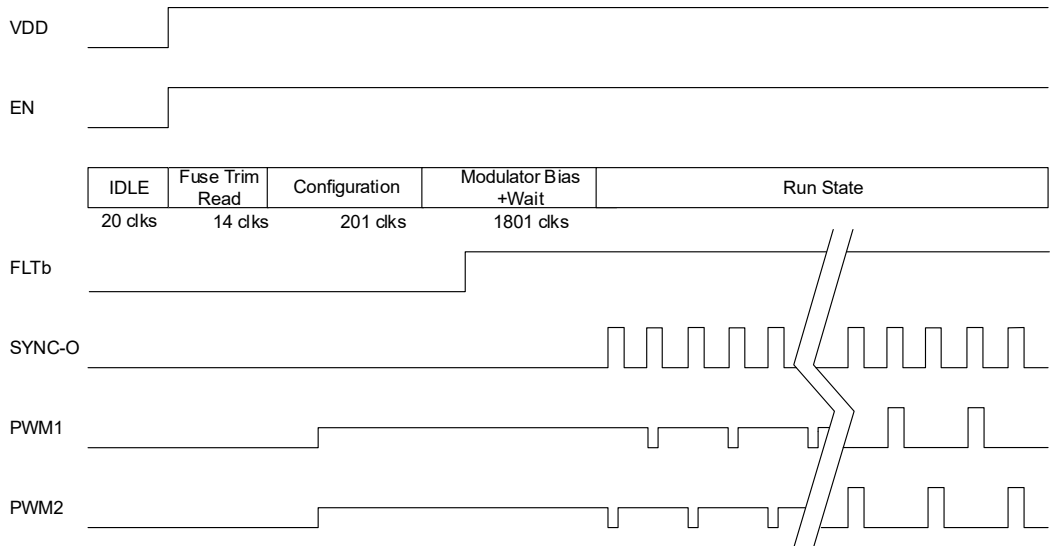


Figure 173. Start Up Timing Diagram (R_{SYNC-O} = 100kΩ)

During states A and C in Figure 172 and Figure 173, the oscillator blanks the clock signal to the digital core. This is done so that the oscillator has time to stabilize its frequency before entering the configuration state (B) or run state (D).

Important: During states A and C, because the digital core does not receive a clock, it is unable to detect a rising edge on EN. Rather, the EN signal must persist long enough so that the digital core can read it during states B and D. The ISL73849SLH reacts to a falling edge on EN regardless of what state the controller is in.

5.13 Fault Response

The ISL73849SLH can be programmed with PMBus to either respond to a fault by going into hiccup mode or latch-off mode. See FAULT_RESPONSE (D1h) for more information.

5.13.1 Hiccup Mode

By default, when the ISL73849SLH encounters a fault, it enters hiccup mode. During hiccup mode, the controller waits 1 soft-start cycle before attempting to start switching again. If the fault has not cleared after the dummy soft-start cycle has completed, the ISL73849SLH waits until it clears and then starts the PWM output switching. This would be the case if the fault that tripped was the driver pulling FLTb low due to an over temperature fault.

In the case of an output short, the part would hiccup, go through a dummy soft start cycle and attempt start up indefinitely until the output short is removed. In this case as soon as the part starts switching it would trip the overcurrent threshold and go back to hiccup. Once the output short is removed, normal operation resumes.

The fault response is set to hiccup mode by default on all faults. See FAULT_RESPONSE (D1h) for more information.

5.13.2 Latch-Off Mode

In latch-off mode the ISL73849SLH stops switching when it encounters a fault. To enable the system, the EN pin must be toggled or VDD must be power cycled.

5.14 Fault Handling

5.14.1 Cycle-by-Cycle Current Limit

The current flowing through the inductor is monitored through the current-sense inputs using a sense resistor or inductor DCR sensing. When the input reaches the current limit threshold (V_{PCL}), the PWM pulse is terminated to limit the peak current. A single cycle-by-cycle current limit event does not trigger hiccup but if there are four

current limit events in an eight clock cycle window, the ISL73849SLH enters hiccup. The current limit threshold levels can be programmed to other set values with PMBus. See OC_TH (E1h) for more information.

5.14.2 Inductor Peak Overcurrent Protection

If the output current increases even after triggering the cycle-by-cycle current limit, the ISL73849SLH has a second overcurrent protection (V_{POC} and V_{NOC}). If triggered, it drives the PWM outputs to mid-level (tri-state the power stage) and enter hiccup. If the initial fault continues to persist or another fault occurs during the next soft start, the cycle repeats indefinitely and stays in hiccup. The overcurrent protection protects against both positive and negative overcurrent conditions. The second overcurrent protection threshold levels can be programed to other set values with PMBus. See OC_TH (E1h) for more information.

5.14.3 Overvoltage and Undervoltage Fault

The ISL73849SLH has overvoltage and undervoltage protection that is triggered when the feedback overvoltage ($V_{(FB, OV)}$) or feedback undervoltage ($V_{(FB, UV)}$) threshold levels are exceeded. If the $V_{(FB, OV)}$ or $V_{(FB, UV)}$ levels are reached, the part enters hiccup. The overvoltage and undervoltage fault threshold levels can be programmed to other set values with the PMBus. See VOUT_OV_LIMIT (E3h) and VOUT_UV_LIMIT (E4h) for more information.

5.14.4 FLTb Pin

The FLTb pin (FLT stands for Fault) is a bi-directional communication pin between the ISL73849SLH controller and the ISL73041SEH driver. On the ISL73849SLH, the FLTb pin is low when the part is not ready (during start up) or when it encounters a fault. The ISL73041SEH uses this pin to communicate if it is not ready to accept an input or encountered a fault on its end. In either case, if the FLTb pin is pulled low by the ISL73041SEH, the ISL73849SLH tri-states the output (mid level) and enters hiccup or latches off depending on what the fault response is programmed as. See FAULT_RESPONSE (D1h) for more information.

5.14.5 Oscillator and Sync Input Fault

The ISL73849SLH can synchronize to an external frequency using SYNC-I. If the external clock is not present or if the internal frequency is not less than 15% of the required external clock frequency, the part reverts to the internal oscillator and continues operation. When the external SYNC-I input returns, the ISL73849SLH immediately switches back to the external clock as shown in Figure 174.

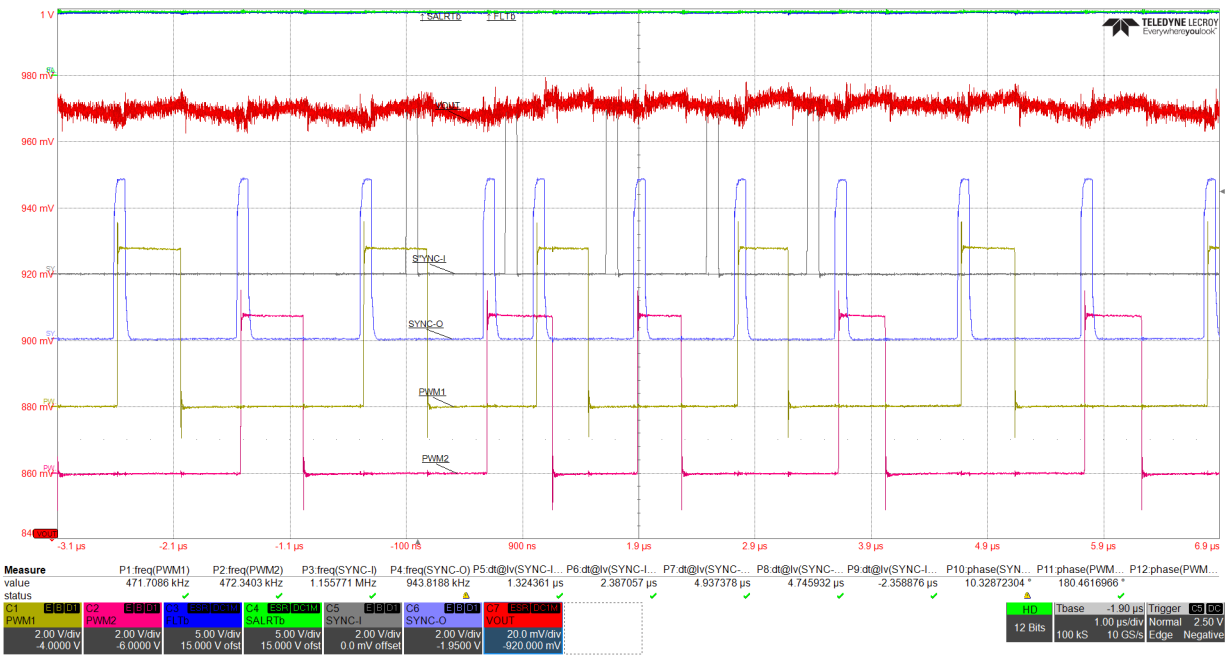


Figure 174. Switching between Internal Oscillator and External Oscillator on SYNC-I (External clock frequency changed from 1MHz to 1.15MHz)

While switching between the internal and external oscillator, there might be a glitch observed on the regulated output. This glitch depends on the frequency difference between the internal and external clock, output capacitance, and output loading.

The internal oscillator must be configured to operate 15% slower than the minimum external frequency applied to the SYNC-I pin to ensure that this fail-safe works. Setting the internal oscillator to a frequency that is too close to the external sync frequency can result in the clock output alternating between the internal and external clock, resulting in a beat frequency.

If the SYNC-I function is not needed, leave the pin floating as it has an internal pull-down. If whatever is driving the SYNC-I pin gets stuck in either a logic high or low, as long as there are no transitions the ISL73849SLH reverts back to the internal oscillator.

If the FS pin is inadvertently shorted to ground or floated while the controller is running, the controller detects and reports an ON_FAULT fault, causing FLTb to be pulled low and stop switching. If the controller is shut down and FS is shorted to ground or left floating when the controller is powered up, no switching occurs as shown in Figure 175 and Figure 176. However, the controller does not detect/report an ON-FAULT and does not pull FLTb low.

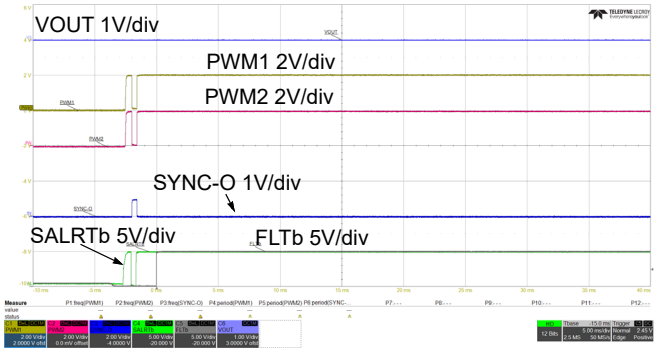


Figure 175. VDD Startup into ON_FAULT Hiccup Response (V_{DD} = 19V, PVIN = 12V, R_{FS} = 0Ω)

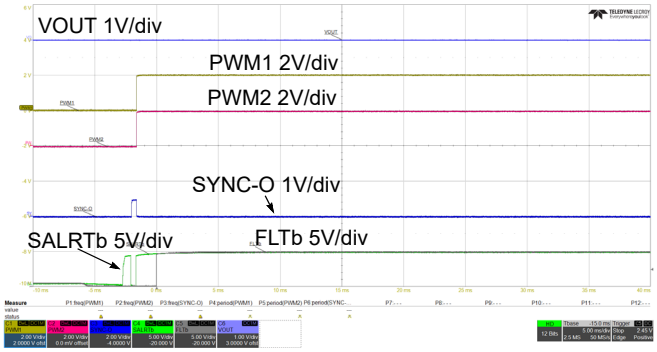


Figure 176. VDD Startup into ON_FAULT Hiccup Response (V_{DD} = 19V, PVIN = 12V, R_{FS} = DNP)

6. Dual-Phase Buck Applications Information

6.1 PWM Switching Frequency Selection

The PWM switching frequency is half the frequency of the internal oscillator or external SYNC-I frequency. The switching frequency is determined based on the requirements of transient response time, solution size, power dissipation, ripple voltage and input and output voltage range. Increasing the switching frequency improves the transient response and solution size but the trade off is increased switching losses. A balance must be reached between these parameters to decide the optimal switching frequency.

When the switching frequency is determined, the FS resistor (frequency setting resistor) can be determined by using Equation 3. where R_{FS} is in ohms (Ω) and f_{SW} is the internal oscillator frequency in hertz (this should be twice the PWM switching frequency). Renesas recommends using precision resistors to set the oscillator frequency as variations in the resistor increase the oscillator frequency spread.

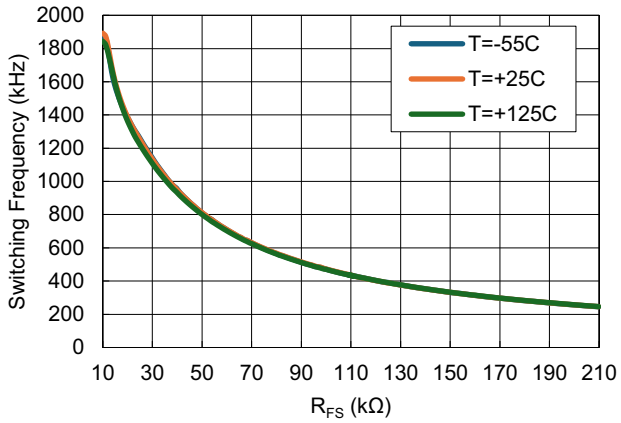


Figure 177. R_{FS} vs. Frequency

The switching frequency is determined by a resistor to ground on the FS pin.

(EQ. 3)
$$R_{FS}[k\Omega] = \frac{56497}{f_{SW}[kHz]} - 20.96$$

where

- R_{FS} is in kiloohms (kΩ)
- f_{SW} is the required switching frequency in kilohertz (kHz)

Important: Equation 3 approximates the real data presented in Figure 177. The data used for Figure 177 is typical and there is some variation due to temperature. This variation is shown in the electrical specifications table by providing 4 fixed resistors and the frequency and tolerance achieved with those resistors.

6.2 Output Voltage Setting

The output voltage can be set to the required regulated voltage by using the following Equation 4.

(EQ. 4)
$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_{FB(TOP)}}{R_{FB(BOT)}}\right)$$

where:

- V_{OUT} is the required regulated voltage.
- V_{REF} is the internal reference voltage on the VFB+ pin, which is 0.592V (default) but can be programmed 0.2V to 1.2V with PMBus.
- $R_{FB(BOT)}$ is the bottom resistor in the feedback divider.
- $R_{FB(TOP)}$ is the top resistor in the feedback divider.

6.3 Resistor Current Sensing and Monitoring Setting

The ISL73849SLH can sense current through a shunt resistor or DCR sensing. Use Equation 5 to determine the required shunt resistance or minimum DCR of the inductor. Depending on what PV_{IN}, V_{OUT}, and $I_{OUT(MAX)}$ are, DCR sensing might not be practical. For example, in a high current and low output voltage application, getting an inductor that meets both the minimum DCR requirement and the saturation current capability might not be possible. In this case, shunt resistance sensing is the only option.

(EQ. 5) $$R_{SEN} = \frac{V_{SEN} \times n}{I_{OUT(MAX)}}$$

- R_{SEN} is the sense resistor or DCR of the inductor.
- n is the number of phases (for the ISL73849SLH this is either 1 or 2).
- $I_{OUT(MAX)}$ is the max DC output current for all phases.
- V_{SEN} is the target current-sense amplifier ISEN voltage at full-load during steady-state operation.

The V_{SEN} can be changed for the needs of the application by programming the OC_TH (E1h) register. V_{SEN} is 1/1.5 of the OC_TH. For example, for a OC_TH of 37.5mV the V_{SEN} is 25mV. Using Equation 5, for a 2-phase 50A ISL73849SLH converter design R_{SEN} is 1mΩ. Lowering the sense resistance from 2mΩ to 1mΩ improves efficiency. For example, at V_{OUT} = 1V, 25mV smaller voltage drop represents 2.5% efficiency improvement. The disadvantage with using the lower 25mV current-sense option using PMBus is that the ±12mV CSA offset (post-rad) contributes a larger error to the current-sharing tolerance. At 50mV the current sharing is ±24% (±12mV/50mV) and increases with the 25mV current-sense option to ±48% (±12mV/25mV). Therefore, for better current-sharing accuracy Renesas recommends using the 50mV current-sense option.

It is necessary to add RC filters for sense resistor sensing and for DCR sensing. The RC filter on the sense resistor compensates for parasitic inductance. Use Equation 6 when the resistor value and parasitic inductance are known. The equation sets the RC pole to seven times the RL zero to prevent over filtering, which can cause instability near the controller minimum ON time. If the application design does not operate near the minimum ON time, set the RC pole equal to RL zero.

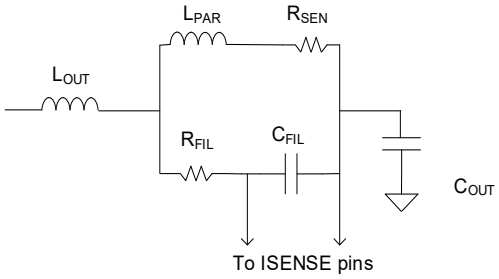


Figure 178. R_{SEN} Parasitic Inductance Compensation RC Circuit

(EQ. 6) $$\frac{L_{PAR}}{7 \times R_{SEN}} = R_{FIL} \times C_{FIL}$$

- R_{FIL} is the resistance of the RC filter resistor.
- C_{FIL} is the capacitance of the RC filter capacitor.
- R_{SEN} is the sense resistor from Equation 5.
- L_{PAR} is the parasitic inductance of R_{SEN}.

6.4 DCR Current Sensing

The DCR method of current sensing in a buck converter uses the DC resistance of the inductor winding as the current-sense element. This method eliminates the need for a sense resistor and improves efficiency. The

inductor DCR does vary based on the temperature coefficient of the selected winding material, such as Cu. However, these variations are not quite as wide as using a MOSFET for $r_{DS(ON)}$ sensing. This method is often used in low-output voltage converters, as any voltage drop on a sense resistor negates the low-output voltage. Keep in mind that DCR sensing is recommended for single-phase applications and not for current-sharing applications.

If the DCR = R_{SEN}, place an RC filter across the inductor. as shown in Figure 179.

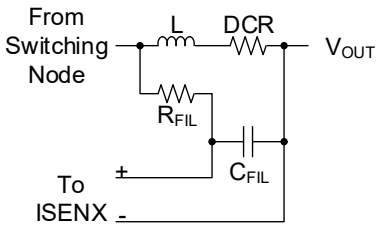


Figure 179. DCR Current Sensing when DCR = R_{SEN}

For DCR sensing, the RC filter has to be selected such that the voltage across the capacitor is proportional to the current through the inductor. Calculate the component values using Equation 7:

(EQ. 7) $$\frac{L}{DCR} = R_{FIL} \times C_{FIL}$$

- L is the output inductor value.
- DCR is the DC resistance of inductor winding.
- R_{FIL} is the resistor value selected for DCR sensing and filtering.
- C_{FIL} is the capacitor value selected for DCR sensing and filtering.

If DCR < R_{SEN}, a resistor can be added to get the required R_{SEN} as shown in Figure 180.

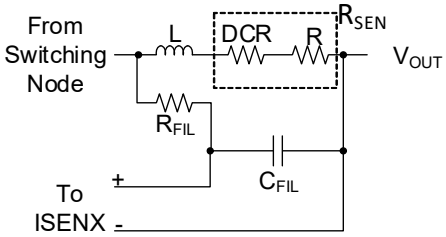


Figure 180. DCR Current Sensing when DCR < R_{SEN}

Calculate the component values using Equation 8. For example, if R_{SEN} is 2mΩ and the chosen inductor has a DCR of 1mΩ, a 25mV current-sense signal is produced instead of a 50mV signal. To fix this, add R = 1mΩ in series with the inductor to get a R_{SEN} = 2mΩ.

(EQ. 8) $$\frac{L}{DCR + R} = R_{FIL} \times C_{FIL}$$

- L is the output inductor value.
- DCR is the DC resistance of inductor winding.
- R is the added resistor in series with the inductor.
- R_{FIL} is the resistor value selected for DCR sensing and filtering.
- C_{FIL} is the capacitor value selected for DCR sensing and filtering.

If DCR > R_{SEN}, a voltage divider must be added so the equivalent resistance formed between the filter divider and the DCR is equal to R_{SEN} as shown in Figure 181.

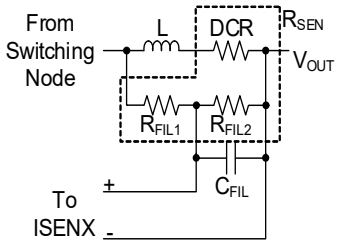


Figure 181. DCR Current Sensing when DCR > R_{SEN}

Calculate the component values using Equation 9. For example, if R_{SEN} is 2mΩ and the chosen inductor has a DCR of 3mΩ, a 75mV current-sense signal is produced instead of a 50mV signal. To fix this, use an R_{FIL1} = 1kΩ and R_{FIL2} = 2kΩ divider to reduce the 75mV current-sense signal to 50mV.

(EQ. 9) $$\frac{L}{DCR} = \frac{R_{FIL1} \times R_{FIL2}}{R_{FIL1} + R_{FIL2}} \times C_{FIL}$$

- L is the output inductor value.
- DCR is the DC resistance of inductor winding.
- R_{FIL1} and R_{FIL2} are the resistor values selected for DCR sensing and filtering.
- C_{FIL} is the capacitor value selected for DCR sensing and filtering.

6.5 Inductor Selection

To select the proper inductance value, determine the input voltage, output voltage, switching frequency, and inductor ripple current. Renesas recommends ensuring the inductor ripple current is 30%.

(EQ. 10) $$I_{OUT} = n \times I_{PHASE}$$

- n is the number of phases (for the ISL73849SLH this is either 1 or 2).
- I_{PHASE} is the phase current.

Designing with less ripple current reduces the output voltage ripple but comes at the expense of slower transient response. Therefore, the amount of acceptable ripple would need to be decided on a per-application basis.

Use Equation 11 to calculate a good first-pass estimate for the inductor size.

(EQ. 11) $$L_{SEL} = \frac{(V_{IN} - V_{OUT}) \times D \times n}{k_r \times f_{SW} \times I_{OUT}}$$

- L_{SEL} is the output inductance.
- V_{IN} is the input voltage to the power supply.
- V_{OUT} is the output voltage of the power supply.
- D is the duty cycle; for a buck converter, it is (V_{OUT}/V_{IN}).
- k_r is the inductor ripple to DC current ratio (k = 0.3 is recommended).
- n is the number of phases (for the ISL73849SLH this is either 1 or 2).
- f_{SW} is the switching frequency of the power supply.
- I_{OUT} is the output current of the regulator.

6.6 Slope Compensation

Use Equation 12 to calculate the slope compensation resistor:

(EQ. 12) $$R_{SLOPE} = \frac{R_{SEN} \times R_{FS} \times V_{OUT}}{k_s \times L_{SEL}}$$

$$25k\Omega \leq R_{SLOPE} \leq 100k\Omega$$

- R_{SLOPE} is the slope compensation resistor.
- R_{SEN} is the value of the current sensing resistor.
- R_{FS} is the value of the resistor that sets the switching frequency.
- V_{OUT} is the output voltage of the power supply.
- k_s is a constant, 25kV/s.
- L_{SEL} is the user-selected output inductance.

R_{SLOPE} must remain between 25kΩ and 100kΩ for proper operation. If the calculated R_{SLOPE} is < 25kΩ, decrease L_{SEL}, if it is > 100kΩ, increase L_{SEL}.

With the internal oscillator and the calculated R_{SLOPE}, the ISL73849SLH shows ≤1% PWM frequency jitter across 250kHz to 1.5MHz. To further reduce the jitter, set R_{SLOPE} to 100kΩ or tie SLOPE to VCC, overriding the calculated R_{SLOPE}. When synchronized to an external oscillator using SYNC-I, no jitter is observed and the calculated R_{SLOPE} can be used as is.

6.7 Error Amplifier Compensation and Output Capacitance

To calculate the output capacitor and compensation values, the transient response ΔV_{OUT} and transient current step ΔI_{OUT} must be known. With these two known values, use Equation 13 to calculate the equivalent load-line output impedance R_{LL}.

(EQ. 13) $$R_{LL} = \frac{\Delta V_{OUT}}{\Delta I_{OUT}}$$

As an example, if a regulator must meet a 5% transient specification for V_{OUT} = 1V and ΔI_{OUT} = 50A, ΔV_{OUT} is 50mV (1V×5%), which would make R_{LL} = 50mV/50A = 1mΩ.

The error amplifier is a transconductance amplifier that makes it much easier to compensate by placing a series resistor and capacitor to GND on the output of the amplifier (COMP pin). Use Equation 14 to determine the compensation resistor (R_{COMP}).

(EQ. 14) $$R_{COMP} = \frac{V_{OUT} \times R_{SEN} \times A_{CSA}}{n \times V_{REF} \times g_{m(EA)} \times R_{LL}}$$

- R_{COMP} is the COMP pin resistor.
- R_{SEN} is the sense resistor or minimum DCR of the inductor.
- A_{CSA} is the gain of the current-sense amplifier, which is 8mV/mV (typical).
- n is the number of phases (for the ISL73849SLH this is either 1 or 2).
- V_{REF} is the internal reference voltage on the VFB+ pin, which is 0.592V typical default on power up and can be programmed in the range of 0.2V to 1.2V.
- $g_{m(EA)}$ is the transconductance of the error amplifier, which is 3.57mA/V or 3.57mS (typical).
- R_{LL} is the equivalent load-line output impedance calculated with Equation 13.

Use Equation 15 to calculate $C_{OUT(MIN)}$.

(EQ. 15) $$C_{OUT(MIN)} = \frac{n \times R_{COMP} \times g_{m(EA)} \times V_{REF}}{2\pi \times f_{SW}/10 \times A_{CSA} \times R_{SEN} \times V_{OUT}}$$

- $C_{OUT(MIN)}$ is the minimum output capacitance needed for the required unity gain frequency of the regulator.
- R_{COMP} is the COMP pin resistor calculated in Equation 14.
- V_{REF} is the internal reference voltage on the VFB+ pin, which is 0.6V (typical).
- V_{OUT} is the output voltage of the power supply.
- R_{SEN} is the sense resistor or minimum DCR of the inductor.
- A_{CSA} is the gain of the current-sense amplifier, which is 8mV/mV (typical).

The output capacitance determines the unity gain frequency f_T. Renesas recommends setting the unity gain frequency a decade below the switching frequency ($f_T = f_{SW}/10$). Select $C_{OUT} \geq C_{OUT(MIN)}$ and f_T can be calculated after determining this value.

Equations for R_{COMP} and $C_{OUT(MIN)}$ are derived for an ideal case where the output capacitance has no parasitic ESR and ESL. The actual equivalent output capacitance has some parasitic ESR and ESL that impact the transient response. Use Equation 16 to approximate the total transient response.

(EQ. 16) $$\Delta V_{OUT(TOTAL)} = \Delta V_{OUT} + \Delta V_{ESR} + \Delta V_{ESL}$$

- ΔV_{OUT} is the value in Equation 13 used for calculating R_{LL}.
- ΔV_{ESR} is the output voltage deviation due to the equivalent parasitic ESR, calculated in Equation 17.

(EQ. 17) $$\Delta V_{ESR} = \Delta I_{OUT} \times ESR$$

- ΔV_{ESL} is the output voltage deviation due to the equivalent parasitic ESL, calculated in Equation 18, where di/dt is the slew rate of the transient step.

(EQ. 18) $$\Delta V_{ESL} = ESL \times di/dt$$

Note: Equation 16 is an estimate because these three components that affect the transient response never have maximum values simultaneously. Therefore, the ideal ΔV_{OUT} calculated in Equation 13 must be reduced to account for parasitic ESR and ESL in the output capacitors. For example, for a design goal of 5% total transient response, if both ΔV_{ESR} and ΔV_{ESL} are each causing 1% V_{OUT} disturbance each, the real ΔV_{OUT} used in Equation 13 should be 3% (5%-2%).

C_{COMP} sets the zero frequency of the error amplifier. To maximize the phase margin of the regulator, Renesas recommends setting the zero frequency formed by R_{COMP} and C_{COMP} a decade smaller than the actual unity gain frequency of the regulator calculated with actual output capacitance ($f_Z = f_T/10$). Use Equation 19 to calculate the C_{COMP} value.

(EQ. 19) $$C_{COMP} = \frac{1}{2\pi \times f_Z \times R_{COMP}}$$

- C_{COMP} is the compensation capacitance.
- R_{COMP} is the COMP pin resistor calculated in Equation 14.
- f_Z is the zero frequency set by R_{COMP} and C_{COMP}, based on the actual f_T calculated from the actual output capacitance.

6.8 Pole Capacitor

A pole capacitor must be added in parallel with R_{COMP} and C_{COMP} to cancel out the zero created by the equivalent ESR and C_{OUT}. To calculate C_{POLE} use Equation 20.

(EQ. 20) $$C_{POLE} = \frac{C_{OUT} \times ESR}{R_{COMP}}$$

6.9 Droop Regulation Setting

Droop regulation changes the DC regulation set point inversely to the output load current, improving the transient response. Place a resistor between the DROOP and VREF pins to use droop regulation. If droop regulation is unnecessary, short the DROOP and VREF pins together. Figure 182 shows the transient response with droop resistor = 0Ω, and Figure 183 shows the transient response with droop resistor = 604Ω. With droop regulation, the transient response is reduced by 40%, which could allow a reduction in output capacitance if there is margin in ΔV_{OUT}.

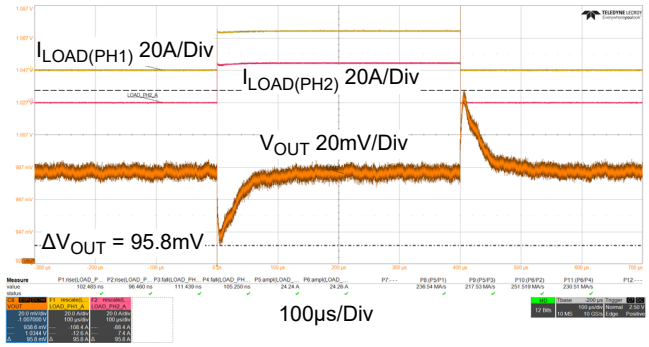


Figure 182. Transient Response without Droop Regulation

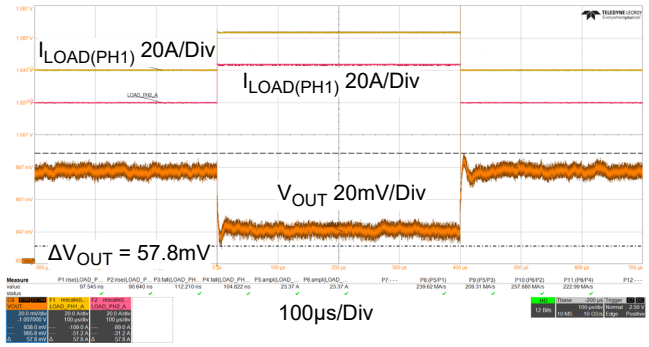


Figure 183. Transient Response with Droop Regulation

As the output loading increases, the current into the DROOP pin increases and generates a voltage across the resistor between the DROOP and VREF pins. This lowers the reference voltage presented to the error amplifier, effectively lowering the regulation point. The extent of the droop variation can be tuned by carefully selecting the droop resistor.

When using droop regulation, it is important to set the light load regulation point at the highest acceptable voltage using Equation 4. Then, calculate the percent deviation of the regulated voltage needed to achieve the lowest acceptable voltage at the maximum DC loading. When the percentage deviation ($DRP_{percent}$) is determined, use Equation 21 to calculate the resistance between VREF and DROOP.

(EQ. 21) $$R_{DROOP} = \frac{DRP_{percent} \times V_{REF}}{I_{DROOP} \times n}$$

- R_{DROOP} is the resistance between the VREF and DROOP pins.
- $DRP_{percent}$ is the percentage variation of V_{OUT} needed at full load in %.
- V_{REF} is the internal voltage reference, which is 0.592V typical default on power up. This can be programmed in the range of 0.2V to 1.2V using the PMBUS.
- I_{DROOP} is the current into the DROOP pin (also known as the ERROR_DRP in the EC Table), which is 19.9µA (typical).
- n is the number of phases (for the ISL73849SLH this is either 1 or 2).

Because I_{DROOP} follows the inductor current, it is necessary to average the signal to get the DC load current. Use Equation 22 to calculate the value of the capacitance:

(EQ. 22) $$C_{DROOP} = \frac{R_{COMP} \times C_{COMP}}{R_{DROOP}}$$

- C_{DROOP} is the droop capacitance.
- R_{DROOP} is the resistance between the VREF and DROOP pins.
- R_{COMP} is the resistor in the series RC on the COMP pin from Equation 14.
- C_{COMP} is the capacitor in the series RC on the COMP pin from Equation 14.

6.10 Layout

6.10.1 Layout Guidelines

The following are recommendations for the best performance on the ISL73849SLH:

- Place the VDD bulk and high-frequency capacitor as close as possible to the VDD pin.
- Place the feedback resistors as close as possible to the VFB+ and VFB- pins to minimize parasitic capacitance. Route the FB+ and FB- traces close together with no GND trace in between all the way from the load to the devices pins.
- Ensure that all feedback traces are routed away from noisy switching nodes.
- Place the R_{SENSE} RC filter as close to the ISENX+ and ISENX- pins as possible. Route the ISENSE+ and ISENSE- traces close together with no GND trace in between all the way from the load to the devices pins.
- Place C_{COMP}, R_{COMP}, and C_{POLE} as close as possible to the COMP pin.
- DROOP and V_{REF} capacitors should be referenced to VFB-.
- Ensure a good ground plane. Mount the package base with epoxy and drop an array of thermal vias below to the ground plane.
- Place bulk and high-frequency PVIN capacitors close to the ISL70020x FETS drain (Not drawn).
- Minimize the current loop area between the PVIN bulk capacitors and GND and phase node connections
- Connect the feedback traces to the load for point-of-load (POL) regulation.
- Ensure that the traces carrying high load currents are wide enough.

6.10.2 Layout Example

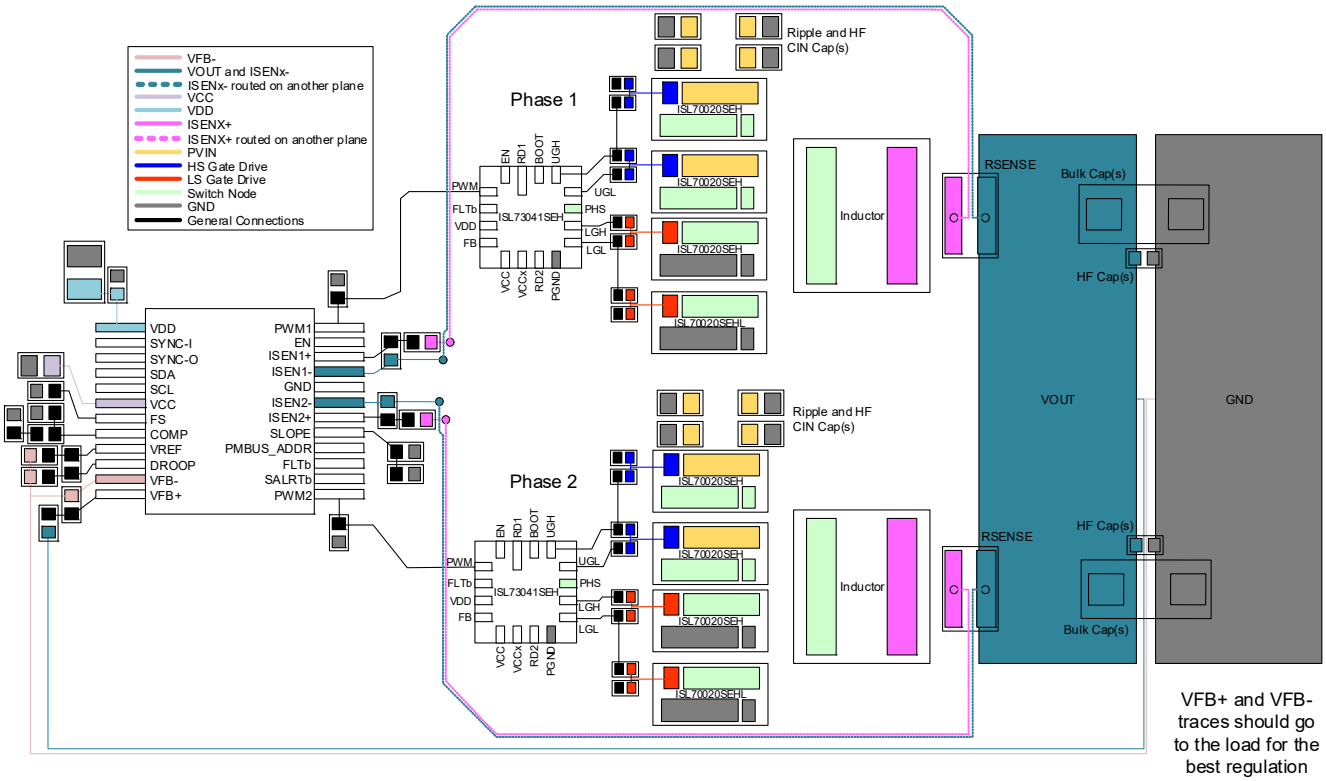


Figure 184. 24 Ld CDFP **Layout Recommendations**

7. PMBus Applications Information

7.1 PMBus User Guide

The ISL73849SLH is implemented with a PMBus digital interface for the user to monitor and change some operating parameters, allowing smart control of the switching converter.

The Power Management Bus (PMBus) is an open-standard digital power management protocol. It uses SMBus as its physical communication layer and includes support for the SMBus Alert (SALERT). In much the same way as SMBus defines the general means to manage portable power, PMBus defines the means to manage power subsystems.

PMBus and SMBus are I^2C derived bus standards that are generally electrically compatible with I^2C. They are more robust (Timeouts Force Bus Reset) and offer more features than I^2C, like SMBALERT(SALERT) line for interrupts, Packet Error Checking (PEC), and Host Notify Protocol.

The ISL73849SLH is compliant with the *PMBus Power System Management Protocol Specification Part I and II version 1.3*. These specification documents can be obtained from the PMBus website. These are required reading for complete understanding of the PMBus implementation. The maximum PMBus clock speed for the ISL73849SLH is 400kHz.

- Specification Part I – General Requirements Transport and Electrical Interface - Includes the general requirements, as well as defines the transport and electrical interface and timing requirements of hardwired signals.
- Specification Part II – Command Language - Describes the operation of commands, data formats, and fault management, as well as defines the command language used with the PMBus.

7.2 Accessing PMBus Registers

All PMBus registers on the ISL73849SLH are set to default values during the initialization period during power-on reset (POR). Most of the PMBus registers can be accessed when the device comes out of its initial POR. Some of the registers can only be changed when the device is disabled by writing a 00h to the OPERATION (01h) register.

To start up the system in a non-default condition such as with a different VREF or OC1 threshold level, there are three options to program the ISL73849SLH PMBus registers before starting up the output of the switching converter.

- Option 1 – Force FLTb LOW and then power up the device as normal; forcing FLTb LOW keeps the device disabled, while allowing access to the PMBus registers. Next, program the new configuration and release FLTb allowing it to go HIGH, causing the ISL73849SLH to start the soft-start process.
- Option 2 – Write an 00h to the OPERATION (01h) register after the first rising edge of SALRTb but before the PWM outputs start switching. This time interval is 2.5ms typical. Next, program the new PMBus configuration and write an 80h to the OPERATION register to enable the ISL73849SLH and begin the soft-start process.
- Option 3 – Keep the EN voltage greater than the gross threshold and lower than the fine threshold (see Enable for more details). Next, program the new configuration and fully enable the ISL73849SLH, which begins the soft-start process.

If the EN pin is set to a value lower than the gross threshold or VDD falls below its UVLO, the ISL73849SLH is disabled. This causes all the PMBus registers to be reset to their default values and they are no longer accessible through PMBus.

7.3 PMBus SDA and SCL Pull-Up Resistors

The SDA and SCL pull-up resistors must be connected to the ISL73849SLH VCC pin or a different voltage supply that is equal to or less than the V_{CC} = 5V voltage at all times.

While the PMBus specification allows these pins to be pulled to a supply bus separate from the power supply of the devices on the bus, the ISL73849SLH has the restrictions previously described. If the SDA and SCL pins are

pulled to a separate supply bus, the bus rail must be sequenced up after the ISL73849SLH VCC and down before the ISL73849SLH VCC.

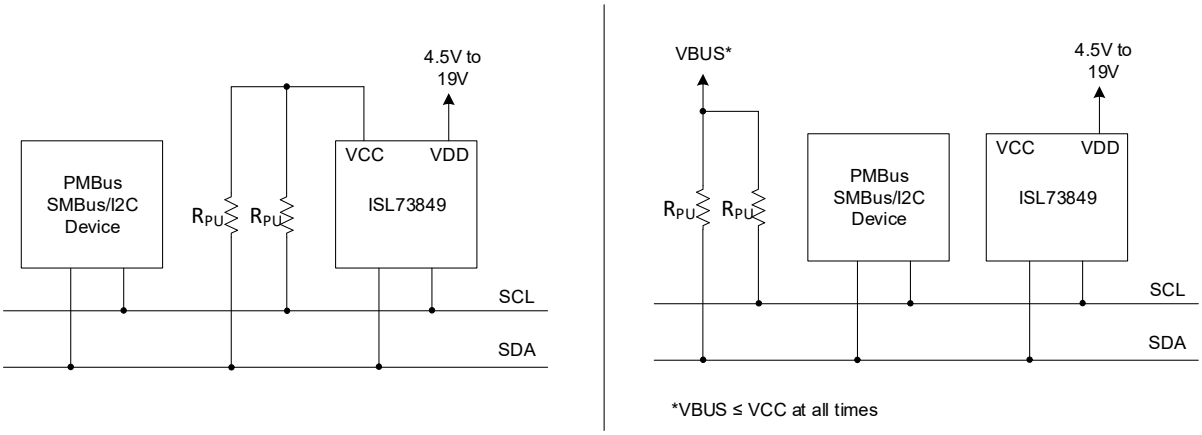


Figure 185. Allowed SDA/SCL PMBus Configurations for ISL73849SLH

7.4 I²C/PMBus Protocol Conventions

Data states on the SDA line must change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (see Figure 186). On power-up, the SDA pin is in the input mode.

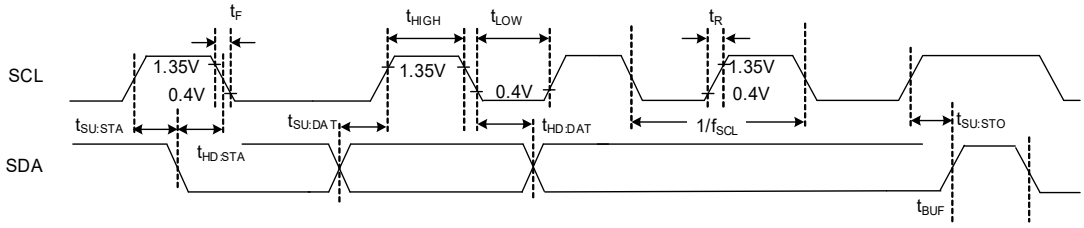


Figure 186. Valid Data Changes, START and STOP Conditions

All I²C/PMBus interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The ISL73849SLH continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (see Figure 186). A START condition is ignored during the power-up of the device.

All I²C/PMBus interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH (see Figure 186). A STOP condition at the end of a read operation, or at the end of a write operation, places the device in its standby mode.

An ACK, Acknowledge, is a software convention used to indicate a successful data transfer. The transmitting device, either controller or target, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data (see Figure 187).

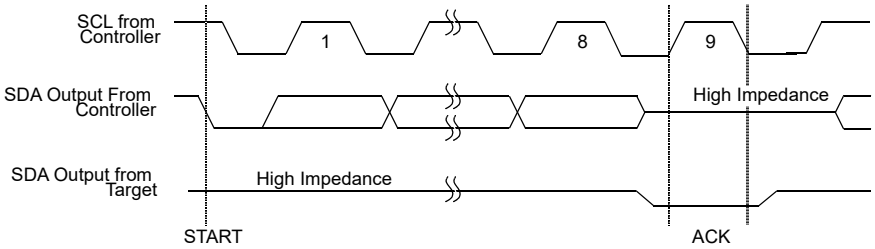


Figure 187. Acknowledge Response from Receiver

The ISL73849SLH responds with an ACK after recognition of a START condition followed by a valid Identification Byte, and once again after successful receipt of an Address Byte. The ISL73849SLH also responds with an ACK after receiving a Data Byte of a write operation. The controller must respond with an ACK after receiving a Data Byte of a read operation.

7.5 Target Device Identification Address

Following a START condition, the host controller must send Target Device Address Byte. A valid Target Address byte contains seven MSBs, which match the logic value associated with the PMBUS_ADDR pin configuration. The 7-bit address can be set to six different options as shown in Table 1. The LSB is the Read/Write bit. Its value is 1 for a Read operation, and 0 for a Write operation.

The ISL73849SLH serves as a target device on the PMBus. The 7-bit physical follower address can be set by the voltage presented to the PMBUS_ADDR pin. This is achieved by connecting the pin either to VCC or GND or by a resistor connected from the pin to GND.

Table 1. Target Device Identification Address Configuration

Option	Configuration	Target Address
0	GND	0x11
1	37.5kΩ	0x12
2	62.5kΩ	0x14
3	87.5kΩ	0x18
4	112.5kΩ	0x13
5	150kΩ	0x16

7.6 Send Byte

A Send Byte transaction issues a simple command to the device with no data. A Send Byte transaction requires a START condition, followed by a valid Target Device Address Byte with the R/W bit set to 0, a valid command Byte, and a STOP condition.

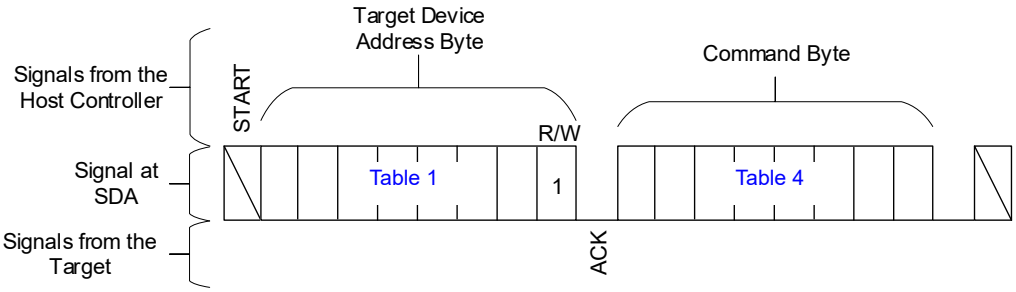


Figure 188. Send Byte

7.7 Write Byte

A Write Byte requires a START condition, followed by a valid Target Device Address Byte with the R/W bit set to 1, a valid command Byte, a data byte, and a STOP condition. After each of the three bytes the ISL73849SLH responds with an ACK.

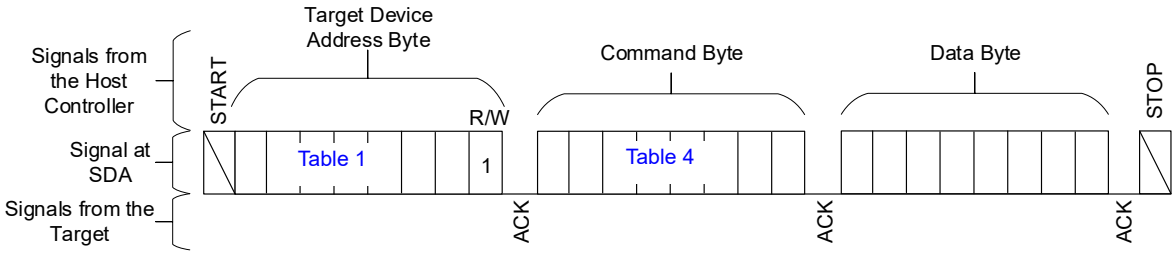


Figure 189. Write Byte

7.8 Write Word

The Write Word transaction sends a single word of data which is two bytes, a Low and High Data Byte. It is identical to the Write Byte except that after the 3rd ACK following the Low Data Byte, a High Data Byte is sent.

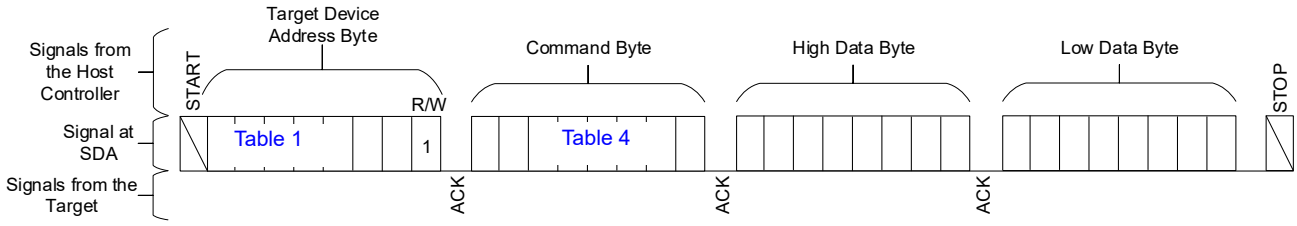


Figure 190. Write Word

7.9 Read Byte

A Read Byte transaction requires a START condition, the Target Device Address Byte with the R/W bit set to 0, a valid command byte, a second Start condition, and a second Target Device Address Byte with the R/W bit set to 1 which signals the device to return data for the specified command byte. After each of these three bytes, the ISL73849SLH responds with an ACK. The host controller terminates the read operation by issuing a NACK and a STOP condition.

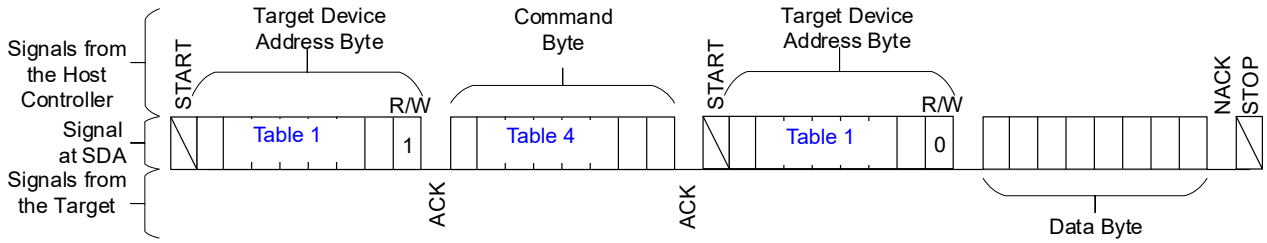


Figure 191. Read Byte

7.10 Read Word

The Read Word transaction reads a single word of data which is two bytes, a Low and High Data Byte. It is identical to the Read Byte transaction except that after receiving the Low Data Byte the host controller sends an ACK, receives the High Data Byte, then sends a NACK and a STOP condition.

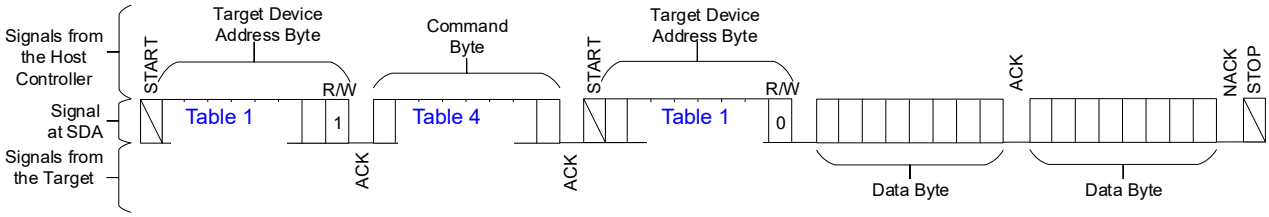


Figure 192. Read Word

7.11 Packet Error Checking (PEC)

The PMBus protocol requires devices to support Packet Error Checking or PEC for short. PEC is a way to ensure that the data transmitted between devices is valid. PEC is optional but highly recommended for data integrity in power-management systems. Transaction integrity is checked by using a cyclic redundancy check (CRC-8) algorithm.

For PMBus writes the host controller computes the PEC byte value and appends it to the end of its transaction before the STOP bit. If the sent PEC byte matches the target's internally computed PEC byte, the ISL73849SLH acknowledges the transaction, and the data is considered valid. If the data PEC bytes do not match, the ISL73849SLH NACKs the transaction, logs a CML fault in the FAULT_STATUS register, pulls SALRTb LOW, and does not act on the data received.

For PMBus reads, if the host does not send a stop bit after the last received data byte and continues to clock data, the ISL73849SLH returns an extra byte, which is the PEC byte it internally calculated. The host may compare its own computed PEC value with this PEC byte and then decide what to do.

7.12 Overview of PMBus Features

A system controller can monitor several ISL73849SLH operating parameters through the PMBus interface including the following:

- Input voltage (VDD pin)
- Output voltage (Sampled through ISEN1- if both phases are active or only Phase 1, or ISEN2- if only Phase 1 is active. Measurements are taken with respect to VFB-.)
- Total averaged inductor currents of the active phases
- Averaged inductor currents of each active phase
- Reference Voltage (VREF pin with respect to VFB-)
- Droop Voltage (VDROOP pin with respect to VFB-)
- VFB+ (VFB+ pin with respect to VFB-)
- VFB- (VFB- pin)
- Internal Oscillator Frequency

A system controller can change the ISL73849SLH operating parameters through the PMBus interface. Some of the commands include, but are not limited to:

- Enable or disable individual PWM operation
- Change the output voltage on-the-fly
- Change the output voltage transition slew rate
- Change the output overvoltage fault threshold
- Change the output undervoltage fault threshold

- Change the overcurrent limit thresholds
- Change the soft-start time
- Selectable fault hiccup mode or latch-off mode response for each individual fault
- Fault response masking and SALERT unmasking for each individual fault

7.13 SALRTb Pin and Fault Response

The SALRTb pin is analogous to the SMBALERT# pin as described in the PMBUS Part II (Rev 1.3) Section 10, Fault Management and Report. The main difference is that the source of the faults and fault masking for the ISL73849SLH does not come from the PMBus defined STATUS_BYTE/STATUS_WORD and SMBALERT_MASK registers. Instead, it comes from the user-defined FAULT_STATUS (D0h) and FAULT_MASK (D2h) as defined in the PMBus Command Summary. The ISL73849SLH supports 10 distinct fault conditions (see Table 2 for more details).

Table 3 lists the 10 types of faults that can be accessed through PMBus to:

- Monitor or clear each individual fault status bit of the FAULT_STATUS Register (D0h).
- Configure the FAULT_RESPONSE Register (D1h) to set each individual fault response to Hiccup or Latch-off.
- Configure the FAULT_MASK Register (D2h) to ignore or respond to each individual fault's protection.

See PMBus Command Details for details on each specific PMBus command.

Table 2. Registers to Monitor Fault Status and Configure Fault Response

Command Code	Register Name	Format	Access	Descriptions	Default Value
D0h	FAULT_STATUS (D0h)	Bit Field	R/W	0: No fault 1: Fault occurred	00h
D1h	FAULT_RESPONSE (D1h)	Bit Field	R/W	0: Hiccup Mode 1: Latch-off Mode	00h
D2h	FAULT_MASK (D2h)	Bit Field	R/W	0: Fault reaction is based on fault response 1: Fault is ignored	00h
E7h	SALERT_MASK_OVERRIDE (E7h)	Bit Field	R/W	0: With the corresponding bit in FAULT_MASK set to 1, the fault is ignored and SALERT# is unaffected. 1: With the corresponding bit in FAULT_MASK set to 1, the fault is ignored and SALERT# goes low.	00h

Table 3. Fault Names List for the Registers (with Default Values) in Table 2

Fault Name	Bit #	D0h Fault Status (Default Value = No Fault)	D1h Fault Response (Default Value = Hiccup Mode)	D2h Fault Status Mask (Default Value = No Mask)	Related Fault to be Monitored/Controlled
FLTb	0	0	0	0	FLTb
ON_FAULT	1	0	0	0	ON_FAULT
NOC_PH1	2	0	0	0	NOC_PH1
NOC_PH2	3	0	0	0	NOC_PH2
OC1_PH1	4	0	0	0	OC1_PH1
OC1_PH2	5	0	0	0	OC1_PH2
OC2_PH1	6	0	0	0	OC2_PH1

Table 3. Fault Names List for the Registers (with Default Values) in Table 2 (Cont.)

Fault Name	Bit #	D0h Fault Status (Default Value = No Fault)	D1h Fault Response (Default Value = Hiccup Mode)	D2h Fault Status Mask (Default Value = No Mask)	Related Fault to be Monitored/Controlled
OC2_PH2	7	0	0	0	OC2_PH2
VOUT_UV	8	0	0	0	VOUT_UV
VOUT_OV	9	0	0	0	VOUT_OV
VOUT_UV_SEVERE	10	0	0	0	VOUT_UV_SEVERE
VOUT_OV_SEVERE	11	0	0	0	VOUT_OV_SEVERE
CML	12	0	0	0	Communications warning (for unsupported command, PEC error)
VOUT_OOR	13	0	0	0	VOUT_OOR
VOUT_TRANSITION	14	0	0	0	VOUT_TRANSITION
FUSE PARITY	15	0	0	0	FUSE PARITY

7.13.1 Operation with No Fault Masking

If a fault occurs and its corresponding bit in the FAULT_STATUS_MASK register is 0, then:

- The corresponding bit of the FAULT_STATUS register is set to 1.
- The SALERT pin goes LOW.
- Depending on the bit set in the FAULT_RESPONSE register corresponding to the event, the fault disables PWM switching permanently (latch-off mode) or disables PWM switching and attempts to restart periodically (hiccup-mode).

When SALRT goes LOW, the PMBus Host can detect the LOW and then:

- Performs a transmission with the Alert Response Address to find which device is pulling SALERT LOW.
- The PMBus Host communicates with the device that is pulling SALERT LOW. The actions that the host performs next are up to the system designer.

7.13.2 Clearing Faults and PMBus Access after a Fault

Clearing each individual bit of the FAULT_STATUS register can only be done by a POR cycle, sending the CLEAR_FAULTS (03h) command, or writing a 1 to the corresponding bit that was set in the FAULT_STATUS register. The clearing of the fault indication from the SALRTb pin is only done by sending the CLEAR_FAULTS command.

If a fault causes the system to latch-off or hiccup, all the PMBus register values are accessible using PMBus, and the FAULT_STATUS register values are accessible for the host to diagnose the type of fault.

7.13.3 Operation when Fault is Masked

If a fault occurs and its corresponding bit in the FAULT_STATUS_MASK register is 1 then:

- The corresponding bit of the FAULT_STATUS register remains 0.
- The SALERT pin remains HIGH.
- No Fault Response occurs.

7.13.4 Operation when Fault is Masked and the SALRT Mask Override is Set

If a fault occurs and its corresponding bit in the FAULT_STATUS_MASK register and SALERT_MASK_OVERRIDE is 1 then:

- The corresponding bit of the FAULT_STATUS register is set to 1
- The SALERT pin goes LOW.
- No Fault Response occurs.

8. PMBus Command Summary

Table 4 lists all the command sets available for the ISL73849SLH. Refer to PMBus Command Details for details about each specific PMBus command.

Table 4. PMBus Command Summary

Command Code	Command Name (Code)	Access	# of Data Bytes	Data Format	Default Setting	Descriptions
01h	OPERATION (01h)	Read/Write Byte	1	Bit	80h	Enable/Disable the device – default is Enable
03h	CLEAR_FAULTS (03h)	Write Byte	0	N/A	N/A	Clears any fault bits in the FAULT_STATUS register that have been set
10h	WRITE_PROTECT (10h)	Read/Write Byte	1	Bit	00h	Protects against accidental changes – default is all registers are accessible
19h	CAPABILITY (19h)	Read Byte	1	Bit	B0h	Provides the way for a host system to determine some key capabilities of the ISL73849SLH as a PMBus device
21h	VOUT_COMMAND (21h)	Read/Write Word	2	CUS	4Ah	Sets the nominal reference voltage for the V_{OUT} set point, V_{REF} DAC = 0.592V as default
24h	VOUT_MAX (24h)	Read Word	2	CUS	0096h	Identifies the upper limit on the V_{REF} DAC the ISL73849SLH can be programmed to (V_{REF} = 1.2V)
27h	VOUT_TRANSITION_RATE (27h)	Read/Write Word	2	Bit	0004h	Sets the V_{REF} DAC transition rate during VOUT_COMMAND (21h) commands. 0000: 12.5mV/ms 0001: 25mV/ms 0010: 50mV/ms 0011: 100mV/ms 0100: 200mV/ms 0101: 400mV/ms 0110: 800mV/ms 0111: 1600mV/ms 1000: 3200mV/ms
2Bh	VOUT_MIN (2Bh)	Read	2	CUS	0019h	Identifies the lower limit on the V_{REF} DAC the ISL73849SLH can be programmed to (V_{REF} = 0.2V).
88h	READ_VIN (88h)	Read Word	2	CUS	N/A	Reports the input voltage measurement (VDD/12.4223). *Note*: This should be preceded by a TELEMETRY_REQ (F0h) command.

Table 4. PMBus Command Summary (Cont.)

Command Code	Command Name (Code)	Access	# of Data Bytes	Data Format	Default Setting	Descriptions
8Bh	READ_VOUT (8Bh)	Read Word	2	CUS	N/A	Reports the output voltage measurement (VOUT/12.4223) as measured from ISEN1- or ISEN2- with respect to VFB-. *Note*: This should be preceded by a TELEMETRY_REQ (F0h) command.
8Ch	READ_IOUT (8Ch)	Read Word	2	CUS	N/A	Reports the output current measurement. *Note*: This should be preceded by a TELEMETRY_REQ (F0h) command.
95h	READ_FREQUENCY (95h)	Read Word	2	CUS	N/A	Reports the oscillators frequency of the main power converter (2x the PWM frequency) *Note*: This should be preceded by a TELEMETRY_REQ (F0h) command.
98h	PMBUS_REVISION (98h)	Read Byte	1	CUS	33h	Reports the PMBus revision to which the ISL73849SLH is compliant (Revision 1.3 of both Parts 1 and 2 of spec).
ADh	IC_DEVICE_ID (ADh)	Read Word	2	CUS	3849h	Reports device identification information.
AEh	IC_DEVICE_REV (AEh)	Read Word	2	CUS	0B01h	Reports device revision information.
C4h	READ_FBN (C4h)	Read Word	2	CUS	N/A	Reports the value of the VFB- pin voltage. *Note*: This should be preceded by a TELEMETRY_REQ (F0h) command.
CAh	READ_VREF (CAh)	Read Word	2	CUS	N/A	Reports the value of the VREF pin voltage with respect to VFB-. *Note*: This should be preceded by a TELEMETRY_REQ (F0h) command.
CBh	READ_FBP (CBh)	Read Word	2	CUS	N/A	Reports the value of the VFB+ pin voltage with respect to VFB-. *Note*: This should be preceded by a TELEMETRY_REQ (F0h) command.
CCh	READ_ISEN1 (CCh)	Read Word	2	CUS	N/A	Reports the average value of the sensed PH1 current. *Note*: This should be preceded by a TELEMETRY_REQ (F0h) command.
CDh	READ_ISEN2 (CDh)	Read Word	2	CUS	N/A	Reports the average value of the sensed PH2 current. *Note*: This should be preceded by a TELEMETRY_REQ (F0h) command.
CEh	READ_VDROOP (CEh)	Read Word	2	CUS	N/A	Reports the value of the DROOP pin voltage with respect to VFB-. *Note*: This should be preceded by a TELEMETRY_REQ (F0h) command.

Table 4. PMBus Command Summary (Cont.)

Command Code	Command Name (Code)	Access	# of Data Bytes	Data Format	Default Setting	Descriptions
D0h	FAULT_STATUS (D0h)	Read/Write Word	2	Bit	0000h	Renesas defined register. Each bit records whether or not one specific fault or warning event occurred. Bit[15] - Fuse Parity Bit[14] – VOUT_TRANSITION Bit[13] – VOUT_OOR Bit[12] – CML Bit[11] – VOUT_OV_SEVERE Bit[10] – VOUT_UV_SEVERE Bit[9] – VOUT_OV Bit[8] – VOUT_UV Bit[7] – OC2_PH2 Bit[6] – OC2_PH1 Bit[5] – OC1_PH2 Bit[4] – OC1_PH1 Bit[3] – NOC_PH2 Bit[2] – NOC_PH1 Bit[1] – ON_FAULT Bit[0] – FLTb input Bit = 0: No Fault Bit = 1: Fault occurred Refer to SALRTb Pin and Fault Response for how to clear faults. FAULT_STATUS is not masked by FAULT_MASK (D2h) register.
D1h	FAULT_RESPONSE (D1h)	Read/Write Word	2	Bit	0000h	Renesas defined register. Bit[8:0] controls the response of a specific fault condition as listed below. Bits[15:9]: Reserved Bit[8]: VOUT_OV_SEVERE Bit[7]: VOUT_UV_SEVERE Bit[6]: VOUT_OV Bit[5]: VOUT_UV Bit[4]: OC2 Bit[3]: OC1 Bit[2]: NOC Bit[1]: ON_FAULT Bit[0]: FLTb Bit = 0: Hiccup Bit = 1: Latch-off

Table 4. PMBus Command Summary (Cont.)

Command Code	Command Name (Code)	Access	# of Data Bytes	Data Format	Default Setting	Descriptions
D2h	FAULT_MASK (D2h)	Read/Write Word	2	Bit	0000h	Renesas defined register. Bits[12:0] masks the respective fault response if set to 1. Bits[15:13]: Reserved Bit[12]: VOUT_TRANSITION Bit[11]: VOUT_OOR Bit[10]: CML Bit[9]: Mask All Faults Bit[8]: VOUT_OV_SEVERE Bit[7]: VOUT_UV_SEVERE Bit[6]: VOUT_OV Bit[5]: VOUT_UV Bit[4]: OC2 Bit[3]: OC1 Bit[2]: NOC Bit[1]: ON_FAULT Bit[0]: FLTb Bit = 0: Fault reaction is based on FAULT_RESPONSE (D1h) Bit = 1: Fault is ignored
DFh	SET_FOLLOWER (DFh)	Read/Write Byte	1	Bit	00h	Sets a controller to a leader or follower in multi-phase configurations. Bit = 0: Leader Bit = 1: Follower
E0h	VREF_STABLE (E0h)	Read Byte	1	Bit	00h	An indicator of when the internal VREF is changing due to a change in VOUT_COMMAND (21h)
E1h	OC_TH (E1h)	Read/Write Byte	1	Bit	00h	Programs the OC Limit Threshold: Bits[7:3]: Unused Bits[2:0]: Voltage Level of OC_TH 000: OC1 = 72mV, OC2 = 97mV, NOC = -73mV 001: OC1 = 77mV, OC2 = 97mV, NOC = -73mV 010: OC1 = 82mV, OC2 = 97mV, NOC = -73mV 011: OC1 = 88mV, OC2 = 97mV, NOC= -73mV 100: OC1 = 35mV, OC2 = 47mV, NOC = -35mV 101: OC1 = 37.5mV, OC2 = 47mV, NOC = -35mV 110: OC1 = 40mV, OC2 = 47mV, NOC = -35mV 111: OC1 = 43mV, OC2 = 47mV, NOC = -35mV These levels can not be modified when device is enabled/switching (See Accessing PMBus Registers for more details).

Table 4. PMBus Command Summary (Cont.)

Command Code	Command Name (Code)	Access	# of Data Bytes	Data Format	Default Setting	Descriptions
E2h	EN_PWM_PH (E2h)	Read/Write Byte	1	Bit	03h	Allows for enabling one or both phases for use during switching. Bits[7:2]: Unused Bit[1]: PWM2 Phase Enable Bit[0]: PWM1 Phase Enable Bit = 0: Disabled Bit = 1: Enabled This register cannot be modified when device is enabled/switching (See Accessing PMBus Registers for more details).
E3h	VOUT_OV_LIMIT (E3h)	Read/Write Byte	1	Bit	02h	Selects the OV fault level as a percentage of V_{DROOP}. Default set to 110%. Bits[7:3]: Unused Bits[2:0]: Percent of VDROOP 000: 105% 001: 107.5% 010: 110% 011: 112.5% 100: 115% 101: 117.5% 110: 120% 111: 125% This register cannot be modified when device is enabled/switching (See Accessing PMBus Registers for more details).
E4h	VOUT_UV_LIMIT (E4h)	Read/Write Byte	1	Bit	05h	Select the UV fault level as a percentage of V_{DROOP}. Default is set to 90%. Bits[7:3]: Unused Bits[2:0]: Percent of VDROOP 000: 75% 001: 80% 010: 82.5% 011: 85% 100: 87.5% 101: 90% 110: 92.5% 111: 95% This register cannot be modified when device is enabled/switching (See Accessing PMBus Registers for more details).

Table 4. PMBus Command Summary (Cont.)

Command Code	Command Name (Code)	Access	# of Data Bytes	Data Format	Default Setting	Descriptions
E5h	SS_CONFIG (E5h)	Read/Write Byte	1	Bit	03h	Set the soft-start time. Default is 8ms. Bits[7:3]: unused Bits[2:0]: Soft-Start 000: OSC/4 – 1ms 001: OSC/8 – 2ms 010: OSC/16 – 4ms 011: OSC/32 – 8ms 100: OSC/64 – 16ms 101: OSC/128 – 32ms 110: OSC/256 – 64ms 111: OSC/2 – 0.5ms System Clock = 500kHz SS time is approximately the time for the converter VOUT to reach 90% of its regulation point. This register cannot be modified when device is enabled/switching (See Accessing PMBus Registers for more details).
E6h	ADC_ACQ_TIME (E6h)	Read/Write Byte	1	Bit	0Ah	The ADC acquisition time sets the number of ADC clocks used to time the ADC data acquisition. Default is 40 clocks (ADC clock = 2MHz). Values written to this register must be greater than or equal to 4.
E7h	SALERT_MASK_OVERRIDE (E7h)	Read/Write Word	2	Bit	00h	Renesas defined register. Bits[12:0] controls SALERT fault mask. Bits[15:13]: Reserved Bit[12]: VOUT_TRANSITION Bit[11]: VOUT_OOR Bit[10]: CML Bit[9]: Mask All Faults Bit[8]: VOUT_OV_SEVERE Bit[7]: VOUT_UV_SEVERE Bit[6]: VOUT_OV Bit[5]: VOUT_UV Bit[4]: OC2 Bit[3]: OC1 Bit[2]: NOC Bit[1]: ON_FAULT Bit[0]: FLTb Bit = 0: SALRT stays HIGH during a fault and the corresponding FAULT_STATUS bit remains 0. Bit = 1: SALRT goes LOW during a fault and corresponding FAULT_STATUS bit changes to 1 Refer to SALRTb Pin and Fault Response for more information.
F0h	TELEMETRY_REQ (F0h)	Read/Write Byte	1	Bit	00h	Selects and starts ADC conversion for future telemetry reading.

9. PMBus Command Details

9.1 OPERATION (01h)

Definition: This command enables and disables the PWM regulating operation. Only Bit[7] is used for the ISL73849SLH. This command can also be monitored to read the operating state of the device on Bit[7]. Writing values other than 80h or 00h generates a Communication Fault (CML).

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 80h

Units: N/A

Can be Written to while Switching: Yes

Command	OPERATION (01h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See following table							
Default Value	1	0	0	0	0	0	0	0

Bit[7]	Bits[6:0]	Unit On or Off
0	Not Used	Immediately Off
1	Not Used	On, normal operation

9.2 CLEAR_FAULTS (03h)

Definition: This command clears all fault bits that are set in the FAULT_STATUS (D0h) register and releases the SALRTb pin (if asserted) simultaneously. If a fault condition still exists when the bit is cleared, the fault bit is immediately set again and the host is notified by the SALERT pin. This command does not affect the response of the ISL73849SLH that is in the middle of fault induced latch-off or hiccup. CLEAR_FAULT command writes are accepted when WRITE_PROTECT is set.

This command is write only. There is no data byte for this command.

Data Length in Bytes: 0 Byte

Data Format: N/A

Type: Write Only

Protectable: No

Default Value: N/A

Units: N/A

Can be Written to while Switching: Yes

Related Commands: FAULT_STATUS (D0h), WRITE_PROTECT (10h)

9.3 WRITE_PROTECT (10h)

Definition: This command controls writing to the ISL73849SLH. The intent of this command is to provide protection against accidental changes. This command is not intended to provide protection against deliberate changes to a device's configuration or operation. All supported commands may have their parameters read, regardless of the WRITE_PROTECT settings. A received data byte to the WRITE_COMMAND not listed in the following table is accepted. The device does not generate a CML fault or NACK so Renesas recommends reading back the register value to ensure it is set to a defined option.

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W Byte

Protectable: No

Default Value: 00h

Units: N/A

Can be Written to while Switching: Yes

Related Commands: CLEAR_FAULTS (03h), OPERATION (01h), VOUT_COMMAND (21h)

Command	WRITE_PROTECT (10h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See following table							
Default Value	0	0	0	0	0	0	0	0

Hex Value	Bit Value	Description
80h	10000000	Disable all writes except to the WRITE_PROTECT and CLEAR_FAULTS command
40h	01000000	Disable all writes except to the WRITE_PROTECT, OPERATION, and CLEAR_FAULTS commands
20h	00100000	Disable all writes except to the WRITE_PROTECT, OPERATION, VOUT_COMMAND, and CLEAR_FAULTS commands
00h	00000000	Enable writes to all commands

9.4 CAPABILITY (19h)

Definition: This command provides the way for a host system to determine some key capabilities of the ISL73849SLH.

Data Length in Bytes: 1

Data Format: Bit Field

Type: Read Only

Protectable: N/A

Default Value: B0h

Units: N/A

Command	CAPABILITY (19h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See following table							
Default Value	1	0	1	1	0	0	0	0

Bit Number	Description	Bit Value	Meaning
7	Packet Error Checking	1	Packet Error Checking is supported
6:5	Maximum Bus Speed	01	Maximum supported bus speed is 400kHz
4	SMBALERT#	1	The device does have a SALERT# pin and does support the SMBus Alert Response protocol
3	Numeric Format	0	Numeric data is not in LINEAR11, ULINEAR16, SLINEAR16, or DIRECT format
2	AVSBus Support	0	AVSBus not supported
1:0	Reserved	00	Reserved

9.5 VOUT_COMMAND (21h)

Definition: This command sets or reports V_{REF} DAC, which is the reference for the output voltage regulation as described in Output Voltage Setting.

The VOUT_COMMAND register has two data bytes. Bits[15:8] are not used. Bits[7:0] is an unsigned binary integer value, which is equal to the 8-bit V_{REF} DAC value with 1LSB = 8mV. Use Equation 23 to convert the 16Lu data's 8-bit [7:0] unsigned binary integer to V_{REF} DAC in volts. Next, use Equation 24 to convert V_{REF} DAC to V_{OUT}.

The range for programming the reference is 200mV (0x19h) to 1200mV (0x96h). If a value is written to VOUT_COMMAND that is less than 0.2V or greater than 1.2V a Communications (CML) fault is generated, the VOUT_COMMAND is not updated and a second write to VOUT_COMMAND with valid data is expected to take place.

When a VOUT_COMMAND is issued to change the output, the SALRTb pin is set LOW until the output voltage transitions to its new programmed value. The speed of the transition can be programmed with the VOUT_TRANSITION_RATE (27h) register. Any subsequent updates to VOUT_COMMAND that take place while the VREF is still transitioning are ignored and a CML fault is generated.

Data Length in Bytes: 2

Data Format: CUS

Type: R/W

Protectable: Yes

Default Value: 004Ah. With 004Ah = 74dec and 8mV/LSB, meaning V_{REF} DAC = 0.008×74 = 592mV

Units: Volts

Equations:

(EQ. 23) $$V_{REF\_DAC}[V] = 0.008 \times \text{VOUT\_COMMAND[dec]})$$

(EQ. 24) $$V_{OUT} = V_{REF\_DAC} \times \left(1 + \frac{R_{FB(TOP)}}{R_{FB(BOT)}}\right)$$

Range: 0.2V to 1.2V

Example: VOUT_COMMAND = 0096h = 200dec. Using Equation 23, V_{REF} DAC = 0.008×150 = 1.2V

With $R_{FB(BOT)}$ = 3.24kΩ and $R_{FB(TOP)}$ = 4.99kΩ, use Equation 24 to get V_{OUT} = 1V

Can be Written to while Switching: Yes

Related Commands: VOUT_MAX (24h), VOUT_MIN (2Bh)

Command	VOUT_COMMAND (21h)															
Format	CUS															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See following table															
Default Value	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	0

Bit Number	Meaning
7:0	Sets/reads the V_{REF} DAC voltage
15:8	Not used

9.6 VOUT_MAX (24h)

Definition: This command reports the maximum value that can be written to the VOUT_COMMAND (21h) register and therefore the maximum value the V_{REF} DAC can be set to. If an attempt is made to write a value larger than the value in the VOUT_COMMAND register then the write is ignored and VOUT_COMMAND remains unchanged. Furthermore, the VOUT_OOR Bit[11] in FAULT_STATUS (D0h) register is set and the SALRTb pin is set LOW.

Data Length in Bytes: 2

Data Format: CUS

Type: Read Only

Protectable: Yes

Default Value: 0096h. With 0096h = 150dec and 8mV/LSB, meaning V_{REF} DAC = 0.008×150 = 1.2V

Units: Volts

Related Commands: VOUT_COMMAND (21h), VOUT_MIN (2Bh)

Command	VOUT_MAX (24h)															
Format	CUS															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	See following table															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit Number	Meaning
7:0	Reports the maximum allowed VOUT_COMMAND value.
15:8	Not used

9.7 VOUT_TRANSITION_RATE (27h)

Definition: This command sets the rate in mV/ms at which the V_{REF} DAC changes and, correspondingly, sets the rate at which the output voltage changes when VOUT_COMMAND (21h) is changed. This rate does not apply on device start-up.

The VOUT_TRANSITION_RATE command has two data bytes formatted in bit field as shown in the table below. Bits [15:4] are not used. Bits [3:0] define the transition rate of the V_{REF} DAC with a default value of 0004h (200mV/ms) and eight other options ranging from 12.5mV/ms to 8000mV/ms.

Data Length in Bytes: 2

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 0004h (200mV/ms)

Units: mV/ms

Range: 12.5mV/ms to 1800mV/ms for V_{REF} DAC transition rate

Example: VOUT_TRANSITION_RATE = 0003h = 0000_0000_0000_0011b sets the V_{REF} DAC transition rate to be 100mV/ms.

Can be Written to while Switching: Yes

Related Commands: VOUT_COMMAND (21h)

Command	VOUT_TRANSITION_RATE (27h)															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See following table															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Hex Value	Bits[3:0]	Transition Rate of V_{REF} DAC (mV/ms)
0000h	0000	12.5
0001h	0001	25
0002h	0010	50
0003h	0011	100
0004h	**0100 (Default)**	**200**
0005h	0101	400
0006h	0110	800
0007h	0111	1600
0008h	1000	3200
0009h	1001	5333
000Bh	1011	8000

9.8 VOUT_MIN (2Bh)

Definition: This command reports the minimum value that can be written to the VOUT_COMMAND (21h) register and, therefore, the minimum value V_{REF} DAC can be set to. If an attempt is made to write a value smaller than the value in the VOUT_COMMAND register then the write is ignored and VOUT_COMMAND remains unchanged. Furthermore, the VOUT_OOR Bit[11] in FAULT_STATUS (D0h) register is set and the SALRTb pin is set LOW.

Data Length in Bytes: 2

Data Format: CUS

Type: Read Only

Protectable: Yes

Default Value: 0019h. With 0019h = 25dec and 8mV/LSB, meaning V_{REF} DAC = 0.008 × 25 = 0.2V

Units: Volts

Related Commands: VOUT_COMMAND (21h), VOUT_MAX (24h)

Command	VOUT_MIN (2Bh)															
Format	CUS															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	See following table															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit Number	Meaning
7:0	Reports the minimum allowed VOUT_COMMAND value
15:8	Not used

9.9 READ_VIN (88h)

Definition: This command returns a voltage reading of the VDD pin. The returned value contains the VIN voltage after it passes through an attenuator.

The READ_VIN command has two data bytes that contain a 16-bit 2's complement value. This value represents the VDD voltage value with 500µV/LSB with an additional attenuation factor. Use Equation 25 to convert the READ_VIN value (termed as COMMAND) to a voltage.

Data Length in Bytes: 2

Data Format: CUS

Type: Read Only

Protectable: N/A

Default Value: N/A

Units: Volts (use Equation 25 to convert from ADC code to Volts)

Equation:

(EQ. 25) $V_{IN\_ADC} = VIN\_COMMAND \times 6.19mV$

Range: 0V to 2.046V (post attenuator with 0.5mV/LSB)

Example:

READ_VIN = 0325h = 805dec Using Equation 25, V_{IN_ADC} = 6.19mV×805 = 4.98V

Related Commands: TELEMETRY_REQ (F0h)

Command	READ_VIN (88h)															
Format	CUS															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	See following table															
Default Value	N/A															

Bit Number	Meaning
15:0	Reports input voltage with 0.5mV/LSB and an attenuation factor.. Use Equation 25 to calculate the VIN.

9.10 READ_VOUT (8Bh)

Definition: This command returns a voltage reading of either the ISEN1- pin or the ISEN2- pin, depending on which of the phases is active. The returned value contains the VOUT voltage after it passes through an attenuator. *Note*: The value reported is also a derived value, a result of subtracting the converted value of the FB- pin from the ISENx- pin.

The READ_VOUT command has two data bytes formatted as 16-bit 2's complement value, representing the VOUT voltage value with 500µV/LSB and an additional attenuator factor. Use Equation 26 to convert the READ_OUT value (termed as COMMAND) to a voltage.

Data Length in Bytes: 2

Data Format: CUS

Type: Read Only

Protectable: N/A

Default Value: N/A

Units: Volts (see Equation 26 to convert from ADC code to Volts)

Equation:

(EQ. 26) $$V_{OUT\_ADC} = VOUT\_COMMAND \times 6.19mV$$

Range: 0V to 2.046V (post attenuator)

Example: READ_VOUT = 0325h = 805dec, V_{OUT_ADC}= 6.19mV×805 = 4.98V

Related Commands: TELEMETRY_REQ (F0h)

Command	READ_VOUT (8Bh)															
Format	2's Complement															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	See following table															
Default Value	N/A															

Bit Number	Meaning
15:0	Reports the output voltage with 500µV/LSB and an attenuation factor. Use Equation 26 to calculate the VOUT.

9.11 READ_IOUT (8Ch)

Definition: This command returns the total output current telemetry. The READ_IOUT command has two data bytes which contain a 16-bit 2's complement value. This value represents the V_{IOUT} value (termed as COMMAND) with 500µV/LSB. Use Equation 27 to convert the READ_IOUT value (termed as COMMAND) to a current for either a dual-phase or single-phase configuration.

Data Length in Bytes: 2

Data Format: CUS

Type: Read Only

Protectable: N/A

Default Value: N/A

Units: Amps (referred for V_{IOUT} with 500µV/LSB).
Range: 0 to 110A (V_{IOUT} = 0.14V to 1.155V)

Equation:

(EQ. 27) $$I_{OUT} = \frac{(0.0005 \times \text{COMMAND}) - 0.18}{10.5 \times R_{SEN}} \times N$$

- N is the number of phases (1 or 2).
- R_{SEN} is the sense resistor or DCR of the inductor.

Example: READ_IOUT = 07D0h = 2000dec, Using Equation 27, R_{SEN} = 2mΩ, N = 2, and I_{OUT} = 2×((0.0005×2000)-0.140)/(10.5×0.002) = 82A.

Related Commands: TELEMETRY_REQ (F0h)

Command	READ_IOUT (8Ch)															
Format	CUS															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	See following table															
Default Value	N/A															

Bit Number	Meaning
15:0	Reports the total output current information with 500µV/LSB. Use Equation 27 to calculate I_{OUT}.

9.12 READ_FREQUENCY (95h)

Definition: This command returns frequency information of the internally generated oscillator in a voltage value, which represents twice the PWM switching frequency set by the FS pin. The READ_FREQEUNCY register has two data bytes formatted as CUS where Bits[15:10] are not used and Bits[9:0] are used. Equation 28 can be used to convert the READ_FREQUENCY value (termed as COMMAND) to the internal switching frequency in kHz. Divide this value by two to derive the PWM switching frequency. The value read from this register is the only telemetry reading not generated from the ADC but instead is generated in a purely digital manner.

Data Length in Bytes: 2

Data Format: CUS

Type: Read Only

Protectable: N/A

Default Value: N/A

Units: Volts

Range: 68dec (44h) with a 500kHz PWM frequency to 18dec (12h) with a 1.5MHz PWM frequency.

Equation:

(EQ. 28) $$F_{OSC} = \frac{64000}{COMMAND}$$

Example: READ_FREQUENCY = 0043h = 67dec, using Equation 28, F_{OSC} = 64000/(67) = 955.2kHz

Related Commands: TELEMETRY_REQ (F0h)

Command	READ_FREQUENCY (95h)															
Format	CUS															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	See following table															
Default Value	N/A															

Bit Number	Meaning
9:0	Reports the frequency as a count of the 2MHz oscillator clock in an 8x switching clock (2x the PWM frequency) interval.
15:10	Not used

9.13 PMBUS_REVISION (98h)

Definition: This command returns the revision of the PMBus Specification to which the device is compliant.

Data Length in Bytes: 1

Data Format: Bit Field

Type: Read Only

Protectable: N/A

Default Value: 33h (Part 1 Revision 1.3, Part 2 Revision 1.3)

Units: N/A

Command	PMBUS_REVISION (98h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See following table							
Default Value	0	0	1	1	0	0	1	1

Bits[7:4]	Part 1 Revision	Bits[3:0]	Part 2 Revision
0011	1.3	0011	1.3

9.14 IC_DEVICE_ID (ADh)

Definition: This command reports device identification information. For the ISL73849SLH, this command is normal Read, and it returns the binary unsigned integer data with values representing the ISL73849SLH part number.

Data Length in Bytes: 2

Data Format: CUS

Type: Read Only

Protectable: N/A

Default Value: 3849h, which correlates to the ISL73849SLH part number

Units: N/A

Command	IC_DEVICE_ID (ADh)															
Format	CUS															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Returns IC ID as part number 3849h															
Default Value	0	0	1	1	1	0	0	0	0	1	0	0	1	0	0	1

9.15 IC_DEVICE_REV (AEh)

Definition: This command reports device revision information. For the ISL73849SLH, this command is normal Read, and it returns the binary unsigned integer data with values representing the revision 0B01h.

Data Length in Bytes: 2

Data Format: CUS

Type: Read Only

Protectable: N/A

Default Value: 0B01h (Initial Release)

Units: N/A

Command	IC_DEVICE_REV (AEh)															
Format	CUS															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Returns IC Revision information as “0B01h”															
Default Value	0	0	0	0	1	0	1	1	0	0	0	0	0	0	0	1

9.16 READ_FBN (C4h)

Definition: This command returns a voltage reading of the VFB- pin.

The READ_FBN command has two data bytes which contain a 16-bit 2's complement value. This value represents the FB- voltage value with 500µV/LSB. Use Equation 29 to convert the READ_FBN value (termed as COMMAND) to a voltage.

Data Length in Bytes: 2

Data Format: CUS

Type: Read Only

Protectable: N/A

Default Value: N/A

Units: Volts

Range: 0V to 1.2V

Equation:

(EQ. 29) $V_{FBN} = 0.0005 \times \text{COMMAND}$

Example: READ_FBN = 0014h = 20dec. With 500µV/LSB and Equation 29,

$V_{FBN} = 0.0005 \times 20 = 10\text{mV}$.

Related Commands: TELEMETRY_REQ (F0h)

Command	READ_FBN (C4h)															
Format	CUS															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	See following table															
Default Value	N/A															

Bit Number	Meaning
9:0	Reports the value of the VFB- pin voltage with 500µV/LSB. Use Equation 29 to calculate the VFB- voltage.
15:10	Not used

9.17 READ_VREF (CAh)

Definition: This command returns the voltage on the VREF pin. The value returned is a derived value, a result of subtracting the converted value of the FB- pin from the FB+ pin.

The READ_VREF command has two data bytes which contain a 16-bit 2's complement value. This value represents the VREF voltage value with 500µV/LSB. Use Equation 30 to convert the READ_VREF value (termed as COMMAND) to a voltage.

Data Length in Bytes: 2

Data Format: CUS

Type: Read Only

Protectable: N/A

Default Value: N/A

Units: Volts

Equation:

(EQ. 30) $V_{REF} = 0.0005 \times \text{COMMAND}$

Range: 0.2V to 1.2V

Example: READ_VREF = 0898h = 2200dec. With 500µV/LSB and Equation 30,

VREF = 0.0005 × 2200 = 1.1V.

Related Commands: TELEMETRY_REQ (F0h)

Command	READ_VREF(CAh)															
Format	CUS															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	See following table															
Default Value	N/A															

Bit Number	Meaning
7:0	Reports the value of the VREF pin voltage with 500µV/LSB. Use Equation 30 to calculate the VREF voltage.
15:8	Not used

9.18 READ_FBP (CBh)

Definition: This command returns a voltage reading of the FB+ pin. The value reported is a derived value, a result of subtracting the converted value of the FB- pin from the FB+ pin.

The READ_FBP command has two data bytes that contain a 16-bit 2's complement value. This value represents the VFB+ voltage value with 500µV/LSB. Use Equation 31 to convert the READ_FBP value (termed as COMMAND) to a voltage.

Data Length in Bytes: 2

Data Format: CUS

Type: Read Only

Protectable: N/A

Default Value: N/A

Units: Volts

Range: 0V to 1.2V

Equation:

(EQ. 31) $V_{FBP} = 0.0005 \times COMMAND$

Example: READ_FBP = 0640h = 1600dec. With 500µV/LSB and Equation 31,

$V_{FBP} = 0.0005 \times 1600 = 800mV$.

Related Commands: TELEMETRY_REQ (F0h)

Command	READ_FBP (CBh)															
Format	CUS															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	See following table															
Default Value	N/A															

Bit Number	Meaning
9:0	Reports the value of the VFB+ pin voltage with 500µV/LSB. Use Equation 31 to calculate the VFB+ voltage.
15:10	Not used

9.19 READ_ISEN1 (CCh)

Definition: This command returns a voltage reading of the internal ISEN1 signal which represents the output current of phase 1.

The READ_ISEN1 command has two data bytes which contain a 16-bit 2's complement value. This value represents the ISEN1 voltage value with 500µV/LSB. Equation 32 can be used to convert the READ_ISEN1 value (termed as COMMAND) to a current.

Data Length in Bytes: 2

Data Format: CUS

Type: Read Only

Protectable: N/A

Default Value: N/A

Units: Amps

Range: 0A to 55A

Equation:

(EQ. 32) $$I_{SEN1} = \frac{[(0.0005 \times COMMAND) - 0.18]}{10.5 \times R_{SEN1}}$$

R_{SEN1} is the sense resistor or DCR of the inductor in Phase 1

Example: READ_ISEN1 = 015Fh = 500dec. Using Equation 32 and R_{SEN1} = 2mΩ,

I_{SEN1} = [(0.0005×500)-0.18]/(10.5×0.002) = 3.33A.

Related Commands: TELEMETRY_REQ (F0h)

Command	READ_ISEN1 (CCh)															
Format	CUS															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	See following table															
Default Value	N/A															

Bit Number	Meaning
15:0	Reports the PH1 current . Use Equation 32 to convert to a current.

9.20 READ_ISEN2 (CDh)

Definition: This command returns a voltage reading of the internal ISEN2 signal which represents the output current of phase 2.

The READ_ISEN2 command has two data bytes which contain a 16-bit 2's complement value. This value represents the ISEN2 voltage value with 500µV/LSB. Equation 33 can be used to convert the READ_ISEN1 value (termed as COMMAND) to a current.

Data Length in Bytes: 2

Data Format: CUS

Type: Read Only

Protectable: N/A

Default Value: N/A

Units: Amps

Range: 0 to 55A

Equation:

(EQ. 33) $$I_{SEN2} = \frac{[(0.0005 \times COMMAND) - 0.18]}{10.5 \times R_{SEN2}}$$

R_{SEN2} is the sense resistor or DCR of the inductor in Phase 2

Example: READ_ISEN2 = 0015Fh = 500dec. Using Equation 33 and R_{SEN2} = 2mΩ,

I_{SEN2} = [(0.0005×500)-0.18]/(10.5×0.002) = 3.33A.

Related Commands: TELEMETRY_REQ (F0h)

Command	READ_ISEN2 (CDh)															
Format	CUS															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	See following table															
Default Value	N/A															

Bit Number	Meaning
9:0	Reports the PH2 current. Use Equation 33 to convert to a current.
15:10	Not used

9.21 READ_VDROOP (CEh)

Definition: This command returns a voltage reading of the DROOP pin. The value reported is a derived value, a result of subtracting the converted value of the FB- pin from the FB+ pin.

The READ_VDROOP command has two data bytes which contain a 16-bit 2's complement value. This value represents the VDROOP voltage value with 500µV/LSB. Equation 34 can be used to convert the READ_VDROOP value (termed as COMMAND) to VDROOP.

Data Length in Bytes: 2

Data Format: CUS

Type: Read Only

Protectable: N/A

Default Value: N/A

Units: Volts

Range: 0V to 1.2V

Equation:

(EQ. 34) $V_{DROOP} = 0.0005 \times COMMAND$

Example: READ_VDROOP = 0640h = 1600dec. Using Equation 34,

$V_{DROOP} = 0.0005 \times 1600 = 800mV$.

Related Commands: TELEMETRY_REQ (F0h)

Command	READ_VDROOP (CEh)															
Format	CUS															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	See following table															
Default Value	N/A															

Bit Number	Meaning
15:0	Reports the value of the DROOP pin voltage with 500µV/LSB. Use Equation 34 to get VDROOP.

9.22 FAULT_STATUS (D0h)

Definition: Renesas defined register. This command reports if a specific fault condition has ever been triggered. Each bit represents one specific fault condition (listed in the table below).

The bit value meanings are defined as follows:

- Bit = 1 means this fault occurred
- Bit = 0 means this fault did not occur.

Bits[11:0] control a total of eight fault conditions. Bits [14:12] give warning conditions that are PMBus related and Bits [15:13] are not used. All the faults can be cleared by writing a CLEAR_FAULTS (03h) command.

For more descriptions about this command and related commands, refer to SALRTb Pin and Fault Response.

Data Length in Bytes: 2

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 0000h

Units: N/A

Can be Written to while Switching: Yes

Related Commands: FAULT_STATUS (D0h), FAULT_MASK (D2h), CLEAR_FAULTS (03h), SALERT_MASK_OVERRIDE (E7h)

Command	FAULT_STATUS (D0h)															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See following table															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit Number	Fault Name	Default Value	Meaning
0	FLTb	0	FLTb input- real-time fault indicator
1	ON_FAULT	0	Indicates when internally generated oscillator period falls below 6µs.
2	NOC_PH1	0	Negative Overcurrent for Phase 1 (This threshold is programmable, see for more details)
3	NOC_PH2	0	Negative Overcurrent for Phase 2 (This threshold is programmable, see for more details)
4	OC1_PH1	0	Overcurrent 1 for Phase 1 (This threshold is programmable, see OC_TH (E1h) for more details)
5	OC1_PH2	0	Overcurrent 1 for Phase 2 (This threshold is programmable, see OC_TH (E1h) f for more details)
6	OC2_PH1	0	Overcurrent 2 for Phase 1 (This threshold is programmable, see OC_TH (E1h) f for more details)
7	OC2_PH2	0	Overcurrent 2 for Phase 2 (This threshold is programmable, see OC_TH (E1h) f for more details)
8	VOUT_UV	0	Output Undervoltage (This threshold is programmable, see VOUT_UV_LIMIT (E4h) for more details)
9	VOUT_OV	0	Output Overvoltage (This threshold is programmable, see VOUT_OV_LIMIT (E3h) for more details)

Bit Number	Fault Name	Default Value	Meaning
10	VOUT_UV_SEVERE	0	Output Undervoltage Severe (VOUT < 65%)
11	VOUT_OV_SEVERE	0	Output Overvoltage Severe (VOUT > 135%)
12	CML	0	Communications warning (for unsupported command or PEC error)
13	VOUT_OOR	0	VOUT_COMMAND was programmed out of range (see VOUT_COMMAND (21h) for more details).
14	VOUT_TRANSITION	0	Indicates that VREF/VOUT is changing due to a VOUT_COMMAND update and has not reached its final value (see VOUT_COMMAND (21h) for more details)
15	Not used	000000	Not used

9.23 FAULT_RESPONSE (D1h)

Definition: This command sets/reads the fault protection response which is either Hiccup or Latch-off.

- When bit = 0, the fault protection response is Hiccup mode (default)
- When bit = 1, the fault protection response is Latch-off mode

In Hiccup mode, the device stops switching when a fault condition is detected, and restarts from soft-start. This operation is repeated until the fault conditions are completely removed.

In Latch-off mode, the device stops switching when a fault condition is detected and PWM switching is disabled even after fault conditions are removed. In Latch-off, the internal LDO is active to maintain the VCC voltage, and the PMBus interface is accessible to monitor the type of fault triggered or other parameters. To restart the system toggle the EN pin or power-cycle VDD.

For more information about this command and related commands, see SALRTb Pin and Fault Response.

Data Length in Bytes: 2

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 0000h (Hiccup Mode)

Units: N/A

Can be Written to while Switching: Yes

Related Commands: FAULT_STATUS (D0h), FAULT_MASK (D2h)

Command	SET_FAULT_RESPOSE (D1h)															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See following table															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit Number	Fault Name	Default Value	Meaning
0	FLTb	0	Not used
1	ON_FAULT	0	Internally generated oscillator period falls below 6µs. Protection response is Hiccup when bit = 1, and Latch-off when bit = 0
2	NOC	0	Negative Overcurrent of Phase 1 and Phase 2. Protection response is Hiccup when bit = 1, and Latch-off when bit = 0
3	OC1	0	Overcurrent for Phase 1 and Phase 2. Protection response is Hiccup when bit = 1, and Latch-off when bit = 0

Bit Number	Fault Name	Default Value	Meaning
4	OC2	0	Overcurrent for Phase 1 and Phase 2. Protection response is Hiccup when bit = 1, and Latch-off when bit = 0
5	VOUT_UV	0	Output undervoltage fault Protection response is Hiccup when bit = 1, and Latch-off when bit = 0.
6	VOUT_OV	0	Output overvoltage fault Protection response is Hiccup when bit = 1, and Latch-off when bit = 0.
7	VOUT_UV_SEVERE	0	Output voltage undervoltage severe fault (VOUT < 65%). Protection response is Hiccup when bit = 1, and Latch-off when bit = 0
8	VOUT_OV_SEVERE	0	Output overvoltage severe fault (VOUT > 135%). Protection response is Hiccup when bit = 1, and Latch-off when bit = 0
15:9	Not used	000000	Not used

9.24 FAULT_MASK (D2h)

Definition: Renesas defined register. This command sets any specific fault protection to be masked (ignored) or not. Each bit (except Bit[9]) controls one specific fault condition to be ignored or not. If a bit is set to 1 the corresponding fault is masked (ignored), which means there is no fault protecting action taken by the device when that fault is triggered, and the ISL73849SLH keeps its normal PWM switching and operations.

The bit values meanings are defined as follows:

- When bit = 1, the fault is masked/ignored so no action is taken in response.
- When bit = 0, fault protection response is based on the FAULT_RESPONSE (D1h).

For more information about this command and related commands, see SALRTb Pin and Fault Response.

Data Length in Bytes: 2

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 00h (Respond to all faults)

Units: N/A

Can be Written to while Switching: Yes

Related Commands: FAULT_STATUS (D0h), FAULT_MASK (D2h), SALERT_MASK_OVERRIDE (E7h)

Command	FAULT_MASK (D2h)															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See following table															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit Number	Fault Mask Name	Default Value	Meaning
0	FLTb	0	Bit = 0: Respond to FLTb pin Bit = 1: No Response to FLTb pin
1	ON_FAULT	0	Bit = 0: Respond to ON_FAULT Bit = 1: No Response to ON_FAULT
2	NOC	0	Bit = 0: Respond to Negative Overcurrent Fault Bit = 1: No Response to Negative Overcurrent Fault

Bit Number	Fault Mask Name	Default Value	Meaning
3	OC1	0	Bit = 0: Respond to Overcurrent 1 Fault Bit = 1: No Response to Overcurrent 1 Fault
4	OC2	0	Bit = 0: Respond to Overcurrent 2 Fault Bit = 1: No Response to Overcurrent 2 Fault
5	VOUT_UV	0	Bit = 0: Respond to Output Undervoltage Fault Bit = 1: No Response to Output Voltage Undervoltage Fault
6	VOUT_OV	0	Bit = 0: Respond to Output Overvoltage Fault Bit = 1: No Response to Output Overvoltage Fault
7	VOUT_UV_SEVERE	0	Bit = 0: Respond to Output Undervoltage Severe Fault Bit = 1: No Response to Output Undervoltage Severe Fault
8	VOUT_OV_SEVERE	0	Bit = 0: Respond to Output Overvoltage Severe Fault Bit = 1: No Response to Output Overvoltage Severe Fault
9	MASK_ALL	0	Bit = 0: All the faults are responded to Bit = 1: Override the settings of bits[8:0] in the FAULT_MASK register setting them to 1 and masking all the faults controlled by this register.
10	CML	0	Bit = 0: Respond to communications warning (for unsupported command or PEC error) Bit = 1: No Response to communications warning
11	VOUT_OOR	0	Bit = 0: Respond to VOUT_COMMAND programmed out of range Bit = 1: No Response to out of range VOUT_COMMAND
12	VOUT_TRANSITION	0	Bit = 0: Respond to VREF/VOUT changing due to a VOUT_COMMAND update and not reaching its final value Bit = 1: No Response to VREF/VOUT not reaching its final value when VOUT_COMMAND is updated
15:13	Not used	000	Not used

9.25 SET_FOLLOWER (DFh)

Definition: Renesas defined register. This command sets the ISL73849SLH as a leader or follower when there are more than one device configured in a multi-phase setup (See Differential Remote Sensing for more information.) When Bit[0] is set to 1 the COMP pin is set to high-impedance and the device soft-start is set to 0.5ms, making the device a follower.

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: N/A

Default Value: 0h

Units: N/A

Can be Written to while Switching: Yes

Command	SET_FOLLOWER (DFh)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See following table							
Default Value	0	0	0	0	0	0	0	0

Bit Number	Bit Name	Meaning
0	SET_FOLLOWER	Bit = 1:The device is set to a follower Bit = 0: The device is set to a leader
7:1	Reserved	Not used

9.26 VREF_STABLE (E0h)

Definition: Renesas defined register. Provides a way for a host system to determine if the VREF has reached its new, final voltage after a change caused by a write to VOUT_COMMAND.

Data Length in Bytes: 1

Data Format: Bit Field

Type: Read Only

Protectable: N/A

Default Value: 00h

Units: N/A

Related Commands: VOUT_COMMAND (21h)

Command	VREF_STABLE (E0h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See following table							
Default Value	0	0	0	0	0	0	0	0

Bit Number	Bit Name	Meaning
0	VREF_STABLE	Bit = 0:The internal VREF signal is changing due to a change of VOUT_COMMAND. Bit = 1: The internal VREF has reached the new voltage based on VOUT_COMMAND.
7:1	Reserved	Not used

9.27 OC_TH (E1h)

Definition: Renesas defined register. This command programs the Overcurrent 1, Overcurrent 2, and Negative Overcurrent limit thresholds. These thresholds are in mV and represent the differential voltage across the ISENx± pins.

This register can only be updated during the system configuration period. The system configuration period is defined as the OPERATION (01h) register being set to 0x00 or the FLTb external pin being pulled low. Any attempt to change this value while outside of the system configuration period is ignored and a CML fault is generated (see Accessing PMBus Registers for more details).

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 00h (OC1 = 72mV, OC2 = 97mV, NOC= -73mV)

Units: mV

Can Be Written to while Switching: No

Command	OC_TH (E1h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See following table							
Default Value	0	0	0	0	0	0	0	0

Bit Number	Bit Name	Meaning
2:0	OC Limit Threshold	See the following table
7:3	Reserved	Not used

Hex Value	Bits[2:0]	OC1 (mV)	OC2 (mV)	NOC (mV)
00h	**000 (Default)**	**72**	**97**	**-73**
01h	001	77	97	-73
02h	010	82	97	-73
03h	011	88	97	-73
04h	100	35	47	-35
05h	101	37.5	47	-35
06h	110	40	47	-35
07h	111	43	47	-35

9.28 EN_PWM_PH (E2h)

Definition: Renesas defined register. This command enables and disables individual PWM phase switching operation. By default both phases are enabled.

This register can only be updated during the system configuration period. The system configuration period is defined as the OPERATION (01h) register being set to 0x00 or the FLTb external pin being pulled low. Any attempt to change this value while outside of the system configuration period is ignored and a CML fault is generated (see Accessing PMBus Registers for more details).

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 03h (Both PWM phases enabled)

Units: N/A

Can Be Written to while Switching: No

Command	EN_PWM_PH (E2h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See following table							
Default Value	0	0	0	0	0	0	1	1

Bit Number	Bits[7:2] (Not Used)	Unit On or Off
0	PWM1_EN	Bit = 0: PWM1 Switching disabled Bit = 1: PWM1 Switching enabled
1	PWM2_EN	Bit = 0: PWM2 Switching disabled Bit = 1: PWM2 Switching enabled
7:2	Reserved	Not used

9.29 VOUT_OV_LIMIT (E3h)

Definition: Renesas defined register. This command sets the OV fault level as a percentage of the VDROOP input. Their are eight options ranging from 105% to 125% of the reference voltage VDROOP. The default is 110% of VDROOP. The OV fault is generated by a comparator that compares the VFB+ pin voltage with the programmed OV fault level.

This register can only be updated during the system configuration period. The system configuration period is defined as the OPERATION (01h) register being set to 0x00 or the FLTb external pin being pulled low. Any attempt to change this value while outside of the system configuration period is ignored and a CML fault is generated. (See Accessing PMBus Registers for more details)

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 02h (110% of VDROOP)

Units: %

Can Be Written to while Switching: No

Command	VOUT_OV_LIMIT (E3h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See following table							
Default Value	0	0	0	0	0	1	0	0

Bit Number	Bit Name	Meaning
2:0	VOUT_OV_LIMIT	See following table
7:3	Reserved	Not used

Hex Value	Bits[2:0]	Threshold (%)
00h	000	105
01h	001	107.5
02h	**010 (Default)**	**110**
03h	011	112.5
04h	100	115
05h	101	117.5
06h	110	120
07h	111	125

9.30 VOUT_UV_LIMIT (E4h)

Definition: Renesas defined register. This command sets the UV fault level as a percentage of the VDROOP input. Their are eight options ranging from 75% to 95% of the reference voltage VDROOP. The default is 90% of VDROOP. The UV fault is generated by a comparator that compares the VFB+ pin voltage with the programmed UV fault level.

This register can only be updated during the system configuration period. The system configuration period is defined as the OPERATION (01h) register being set to 0x00 or the FLTb external pin being pulled low. Any attempt to change this value while outside of the system configuration period is ignored and a CML fault is generated (see Accessing PMBus Registers for more details).

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 05h (90% of VDROOP)

Units: N/A

Can Be Written to while Switching: No

Command	VOUT_UV_LIMIT (E4h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See following table							
Default Value	0	0	0	0	0	1	0	1

Bit Number	Bit Name	Meaning
2:0	VOUT_UV_LIMIT	See following table
7:3	Reserved	Not used

Hex Value	Bits[2:0]	Threshold (%)
00h	000	75
01h	001	80
02h	010	82.5
03h	011	85
04h	100	87.5
05h	**101 (Default)**	**90**
06h	110	92.5
07h	111	95%

9.31 SS_CONFIG (E5h)

Definition: Renesas defined register. This command sets the output soft-start time.

This register can only be updated during the system configuration period. The system configuration period is defined as the OPERATION (01h) register being set to 00h or the FLTb external pin being pulled low. Any attempt to change this value while outside of the system configuration period is ignored and a CML fault is generated (see Accessing PMBus Registers for more details).

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 03h (4.5ms)

Units: N/A

Can Be Written to while Switching: No

Command	SS_CONFIG (E5h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See following table							
Default Value	0	0	0	0	0	0	1	1

Bit Number	Bit Name	Meaning
2:0	SS_CONFIG	See following table
7:3	Reserved	Not used

Hex Value	Bits[2:0]	Soft-Start (ms)
00h	000	0.5
01h	001	1
02h	010	2
03h	**011 (Default)**	**4.5**
04h	100	9
05h	101	18
06h	110	36
07h	111	0.25

9.32 ADC_ACQ_TIME (E6h)

Definition: Renesas defined register. This command sets the ADC data acquisition time in terms of the number of ADC clocks. The default is 0Ah and this command assumes an 2MHz ADC clock, giving a default time of 5µs.

The value written to this register must be 4 or more for proper circuit operation. Any attempt to change this value to 3 or less is ignored and a CML fault is generated.

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 0Ah (5µs)

Units: N/A

Example: ADC_ACQ_TIME = 40h = 64dec. (1/2MHz)×64 = 32µs.

Command	ADC_ACQ_TIME (E6h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See following table							
Default Value	0	0	0	0	1	0	1	0

Bit Number	Bit Name	Meaning
6:0	ADC_ACQ_TIME	A value between 4 and 127 decimal, given a 2MHz ADC clock, gives data acquisition times between 2µs and 63.5µs.
7	Reserved	Not Used

9.33 SALERT_MASK_OVERRIDE (E7h)

Definition: Renesas defined register. This register overrides the setting of bits in the register in terms of the SALRTb pin. If a bit is set to 1 in the FAULT_MASK register and the corresponding bit in this SALERT_MASK_OVERRIDE register is set to 1, the ISL73849SLH does not react to a fault, but the corresponding bit in the FAULT_STATUS (D0h) register is set to 1 and the SALRTb pin is set LOW. This allows the system to know that a fault(s) has occurred without the ISL73849SLH responding.

The following are the bit values explanations:

- When bit = 1, if the corresponding bit is set in FAULT_MASK, even though the chip ignores the fault, the SALERT pin and the FAULT_STATUS register reacts to the fault.
- When bit = 0, if the corresponding bit is set in FAULT_STATUS_MASK, the SALERT pin and the FAULT_STATUS register is not affected if the fault occurs.

For more details about this command and related commands, see SALRTb Pin and Fault Response.

Data Length in Bytes: 2

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 00h

Units: N/A

Can Be Written to while Switching: Yes

Related Commands: FAULT_STATUS (D0h), FAULT_MASK (D2h)

Command	SALERT_MASK_OVERRIDE_MASK (E7h)															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See following table															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit Number	Fault Mask Name	Default Value	Meaning
0	FLTb	0	Bit = 0: Respond to FLTb pin Bit = 1: No Response to FLTb pin
1	ON_FAULT	0	Bit = 0: Respond to ON_FAULT Bit = 1: No Response to ON_FAULT
2	NOC	0	Bit = 0: Respond to Negative Overcurrent Fault Bit = 1: No Response to Negative Overcurrent Fault
3	OC1	0	Bit = 0: Respond to Overcurrent 1 Fault Bit = 1: No Response to Overcurrent 1 Fault
4	OC2	0	Bit = 0: Respond to Overcurrent 2 Fault Bit = 1: No Response to Overcurrent 2 Fault
5	VOUT_UV	0	Bit = 0: Respond to Output Voltage Undervoltage Fault Bit = 1: No Response to Output Voltage Undervoltage Fault
6	VOUT_OV	0	Bit = 0: Respond to Output Voltage Overvoltage Fault Bit = 1: No Response to Output Voltage Overvoltage Fault
7	VOUT_UV_SEVERE	0	Bit = 0: Respond to Output Undervoltage Severe Fault Bit = 1: No Response to Output Undervoltage Severe Fault
8	VOUT_OV_SEVERE	0	Bit = 0: Respond to Output Overvoltage Severe Fault Bit = 1: No Response to Output Overvoltage Severe Fault

Bit Number	Fault Mask Name	Default Value	Meaning
9	MASK_ALL	0	Bit = 0: All the faults are responded to Bit = 1: Override the settings of bits[8:0] in the FAULT_MASK register setting them to 1 and masking all the faults controlled by this register.
10	CML	0	Bit = 0: Respond to communications warning (for unsupported command or PEC error) Bit = 1: No Response to communications warning
11	VOUT_OOR	0	Bit = 0: Respond to VOUT_COMMAND programmed out of range (see VOUT_COMMAND (21h) for more details) Bit = 1: No Response to out of range VOUT_COMMAND
12	VOUT_TRANSITION	0	Bit = 0: Respond to VREF/VOUT changing due to a VOUT_COMMAND update and not reaching its final value Bit = 1: No Response to VREF/VOUT not reaching its final value when VOUT_COMMAND is updated
15:13	Not used	000	Not used

9.34 TELEMETRY_REQ (F0h)

Definition: Renesas defined register. This command selects one of the 10 possible ADC inputs for conversion and starts the ADC control logic. Setting this register to one of the 10 telemetry options connects the selected input to the ADC and starts controlling the ADC inputs to generate a conversion. A 8191dec or 1FFFhex is written to the telemetry registers during this operation. On the de-assertion of the BUSY signal from the ADC, the ADC control logic latches the converted data and updates the register with the telemetry value to make it available at the register address of the requested telemetry. If a telemetry read returns 8191dec or 1FFFhex, the ADC has likely not completed the conversion and/or has not updated the requested register. Repeat the read until a number in the range of 0-4095dec or 0-0FFFhex is obtained.

The VOUT, VREF, VDROOP, VFB+ telemetry requests also automatically generate a 2nd conversion of the FB- pin voltage, such that the difference between FB- and the highlighted pin is the returned telemetry value.

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 00h

Units: N/A

Can Be Written to while Switching: Yes

Related commands: READ_VIN (88h), READ_VOUT (8Bh), READ_IOUT (8Ch), READ_FREQUENCY (95h), READ_FBN (C4h), READ_VREF (CAh), READ_FBP (CBh), READ_ISEN1 (CCh), READ_ISEN2 (CDh), READ_VDROOP (CEh)

Command	TELEMETRY_REQ (F0h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See following table							
Default Value	0	0	0	0	0	0	0	0

Bit Number	Bit Name	Meaning
3:0	Telemetry Request	Pin/Internal Signal to be converted. See the following Table for more details
7:3	Reserved	Not used

Hex Value	Bits[3:0]	Telemetry	Description
00h	0000	VOUT	If both phases are active or just Phase 1, the MUX analog signal comes from ISEN1-. If only Phase 2 is active, the MUX analog signal comes from ISEN2-. Telemetry read returns the difference of ISENx- and VFB-
01h	0001	VREF	Telemetry read returns the difference of VREF pin and VFB-
02h	0010	VDROOP	Telemetry read returns the difference of VDROOP pin and VFB-
03h	0011	VFB+	Telemetry read returns the difference of VFB+ and VFB-
04h	0100	VDD	Telemetry read of the VDD pin
05h	0101	ISEN1	-
06h	0110	ISEN2	-
07h	0111	IOUT	-
08h	1000	FOSC	-
09h	1001	TEMP	Telemetry read of the TEMP pin
0Ah/0Fh	1010/1111	VFB-	Telemetry read of the FB- pin

10. Die and Assembly Information

Table 5. Die and Assembly Characteristics

Die Information	
Dimensions	6170µm × 8580µm (242.91 mils × 337.79 mils), Thickness: 483µm ±25µm (19mils ±1mil)
Interface Materials	
Glassivation	Type: Silicon dioxide and silicon nitride Thickness: 18.5kÅ ±10% dioxide; 6kÅ ±10% nitride
Top Metallization	Type: Al 99.5%, Cu 0.5% Thickness: 2.85µm ±15µm
Backside Finish	Silicon
Process	250nm BCD, Junction Isolated
Assembly Information	
Substrate Potential	Pin 20 = GND
Weight of Packaged Device	1.8 grams
Termination Finish	100% Au plate - e4
Lid Characteristics	Finish: Gold, Potential: Tied to Pin 20
Additional Information	
Worst Case Current Density	1.6e5A/cm^2
Transistor Count	250868

10.1 Metallization Mask Layout

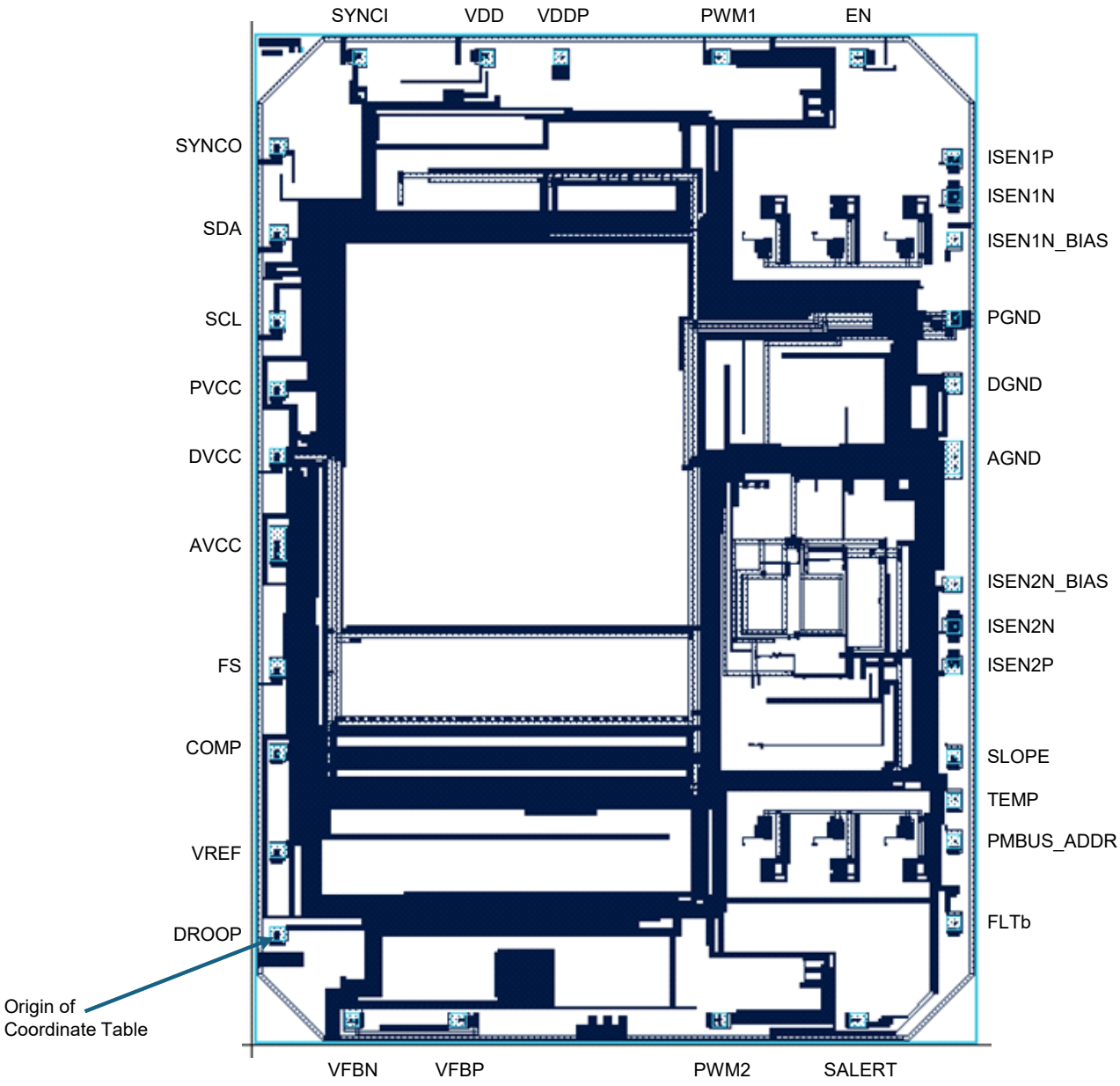


Table 6. Layout X-Y Coordinates (Centroid of bond pad)[1][2][3]

Pad Name	Pad Number	Pin Number	X-Coordinate (µm)	Y-Coordinate (µm)	Pad Size X (µm)	Pad Size Y (µm)	Bond Wire Diameter (0.001")
VDDP	1	1	2398.82	7400.28	117	117	1.25
VDD	2	1	1771.61	7400.28	117	117	1.25
SYNCI	3	2	697.27	7400.28	117	117	1.25
SYNCO	4	3	0	6648.15	117	117	1.25
SDA	5	4	0	5916.15	117	117	1.25
SCL	6	5	0	5169.94	117	117	1.25
PVCC	7	6	0	4598.26	117	117	1.25
DVCC	8	6	0	4032.84	117	117	1.25
AVCC	9	6	0	3293.27	117	280	1.25
FS	10	7	0	2242.18	117	117	1.25
COMP	11	8	0	1537.09	117	117	1.25
VREF	12	9	0.01	705.88	117	117	1.25
DROOP	13	10	0	0	117	117	1.25
VFBN	14	11	629.88	-729	117	117	1.25
VFBP	15	12	1533.18	-729	117	117	1.25
PWM2	16	13	3741.13	-729	117	117	1.25
SALERT	17	14	4905.33	-729	117	117	1.25
FLTb	18	15	5719.28	94.75	117	117	1.25
PWMBUS_ADDR	19	16	5719.28	777.74	117	117	1.25
TEMP	20	16	5719.28	1126.21	117	117	1.25
SLOPE	21	17	5719.28	1496.06	117	117	1.25
ISEN2P	22	18	5719.28	2254.27	117	117	1.25
ISEN2N	23	19	5719.28	2596.2	117	117	1.25
ISEN2N_BIAS	24	19	5719.28	2949.2	117	117	1.25
AGND	25	20	5719.29	4019.08	117	280	1.25
DGND	26	20	5719.28	4641.05	117	117	1.25
PGND	27	20	5719.28	5192.56	117	117	1.25
ISEN1N_BIAS	28	21	5719.28	5863.06	117	117	1.25
ISEN1N	29	21	5719.28	6214.06	117	117	1.25
ISEN1P	30	22	5719.28	6556.02	117	117	1.25
EN	31	23	4905.29	7400.28	117	117	1.25
PWM1	32	24	3744.63	7400.28	117	117	1.25

1. Origin of coordinates is the center of the DROOP pad.
2. Pad size for most pads are 117µm×117µm (two are 117µm×280µm), with an opening of +5µm on each side.
3. Bond wire size: 1.25 mils (0.00125 in).

11. Package Outline Drawing

The package outline drawing is located at the end of this document and is accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

12. Ordering Information

Part Number	Part Marking	Radiation Hardness (Total Ionizing Dose)	Package Description (RoHS Compliant)	Package Drawing	Carrier Type	Temp. Range
ISL73849SLHMF[1]	ISL73849 SLHMF	LDR to 75krad(Si)	24 Ld CDFP Packaged Device (Qualified)	K24.B	Tray	-55 to +125°C
ISL73849SLHF/PROTO[2]	ISL73849SLHF /PROTO	N/A	Packaged Device (For Evaluation Purposes)	K24.B	Tray	-55 to +125°C
ISL73849SLHMX[3]	-	LDR to 75krad(Si)	Bare Die (Qualified)	N/A	N/A	-55 to +125°C
ISL73849SLHX/SAMPLE[3][2]	-	N/A	Bare Die (For Evaluation Purposes)	N/A	N/A	-55 to +125°C
ISL73849SLHEV1Z[4]	2-Phase Evaluation Board (For Evaluation Purposes)					
ISL73849SLHEV3Z[4]	4-Phase Evaluation Board (For Evaluation Purposes)					

1. These Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
2. The /PROTO and /SAMPLE are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions across temperature specified in this datasheet and are in the same form and fit as the qualified device. The /SAMPLE parts are capable of meeting the electrical limits and conditions specified in the datasheet. The /SAMPLE parts do not receive 100% screening across temperature to the datasheet electrical limits. These part types do not come with a Certificate of Conformance (C of C) and have no accompanying data or documentation.
3. Die product tested at T_A = + 25°C. The wafer probe test includes functional and parametric testing sufficient to make the die capable of meeting the electrical performance outlined in Electrical Specifications.
4. Evaluation board uses the /PROTO parts and /PROTO parts are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity.

13. Revision History

Rev.	Date	Description
1.03	Mar 20, 2026	Updated Page 1 description. Updated last paragraph and Equation 6 in the Resistor Current Sensing and Monitoring Setting section.
1.02	Feb 6, 2026	Updated Burn-In Delta values for Shutdown Current spec.
1.01	Jan 13, 2026	▪ Updated Burn-In Delta values for Oscillator spec. ▪ Updated Ordering Information table.
1.00	Dec 11, 2025	Initial release

A. ECAD Design Information

This information supports the development of the PCB ECAD model for this device. It is intended to be used by PCB designers.

A.1 Part Number Indexing

This information supports the development of the PCB ECAD model for this device. It is intended to be used by PCB designers.

Orderable Part Number	Number of Pins	Package Type	Package Code/POD Number
ISL73849SLHMF	24	CDFP	K24.B

A.2 Symbol Pin Information

A.2.1 24-CDFP

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
1	VDD	Power	-
2	SYNC-I	Input	-
3	SYNC-O	Output	-
4	SDA	I/O	-
5	SCL	Input	-
6	VCC	Output	-
7	FS	Input	-
8	COMP	Input	-
9	VREF	Input	-
10	DROOP	Input	-
11	VFB-	Input	-
12	VFB+	Input	-
13	PWM2	Output	-
14	SALRTb	Output	-
15	FLTb	I/O	-
16	PMBUS_ADDR	Input	-
17	SLOPE	Input	-
18	ISEN2+	Input	-
19	ISEN2-	Input	-
20	GND	Power	-
21	ISEN1-	Input	-
22	ISEN1+	Input	-
23	EN	Input	-
24	PWM1	Output	-
EPAD25	GND	Power	-

A.3 Symbol Parameters

Orderable Part Number	Qualification	Radiation Qualification	LDR	Mounting Type	RoHS	Min Operating Temperature	Max Operating Temperature	Min Input Voltage	Max Input Voltage	Number of Outputs	Max Switching Frequency	Max Duty Cycle	Topology
ISL73849SLHMF	Space	QML-V Equivalent	75 krad(si)	SMD	Compliant	-55 °C	125 °C	4.5 V	19 V	2	1.5 MHz	97%	Buck

A.4 Footprint Design Information

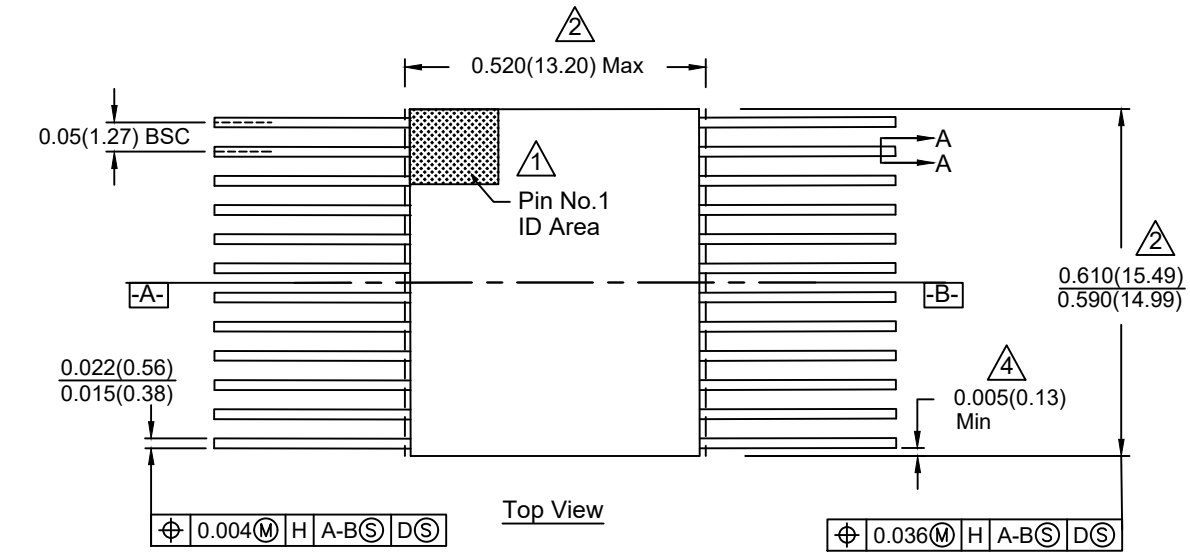
A.4.1 24-CDFP

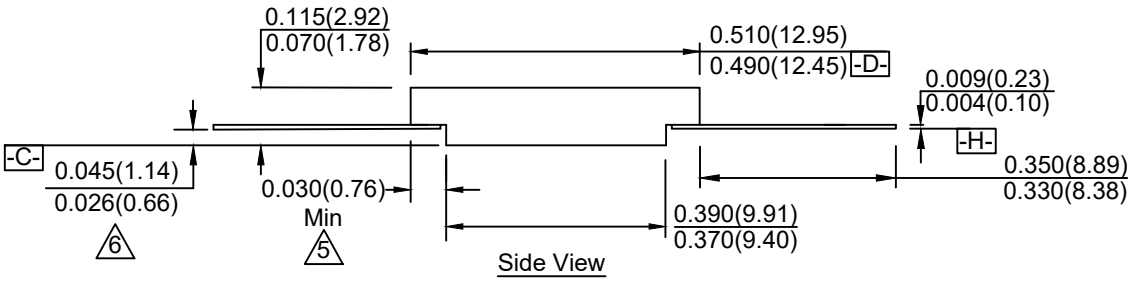
Follow the POD drawing for footprint generation of 24 Ld Ceramic Metal Seal Flatpack Package.

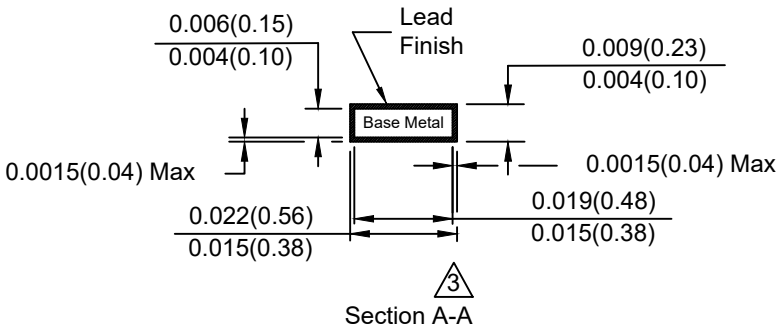
Package Outline Drawing

24 Lead Ceramic Metal Seal Flatpack

POD No: K24.B, Revision No: 01, Date Created:Jan 28, 2025







Notes:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacture's identification shall not be used as a pin one identification mark.
2. This dimension allows for off-center lid, meniscus, and glass overrun.
3. The maximum limits of lead dimensions (section A-A) shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate finish is applied.
4. Measure dimension at all four corners.
5. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
6. This dimension shall be measured at the point of exit (beyond the meniscus) of the lead from the body. This dimension's minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
7. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
8. Dimensions: Inch(mm). Controlling dimension: INCH.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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