ISL74420M

Radiation Tolerant Quad Clock Fanout IC

Description

The ISL74420M is a radiation tolerant quad output clock fanout IC with an optional internal oscillator. It provides synchronization clocks for any application and is particularly useful in multiphase power converters. Each of the four outputs can be set to a different frequency division and phase delay.

Multiple ISL74420M can be connected together to create more than four synchronized clocks.

The division and delay options can be set through selection pins or over an I²C/SMBus interface.

The ISL74420M can accept an external clock up to 50MHz or use its internal 48MHz oscillator that can be tuned ±10% with an external resistor.

The ISL74420M is offered in a 48 Lead TQFP-EP that is fully specified across the temperature range of -55°C to +125°C.

Applications

- Multiphase power converters
- Synchronizing multiple converters on one board to control EMI and crosstalk

Features

- Qualified to Renesas Rad Tolerant Screening and QCI Flow (R34TB0004EU)
- PVIN supply range 3V to 18V
  - Independent clock output supply 3V to 5.5V
- Programmable output frequency starting at 25kHz
  - Internal or external clock source
- Programmable phase delay as low as 15° increments
- I²C/SMBus Compatible
- I²C/SMBus or pin strapping to set frequency and phase
- TID Radiation Lot Acceptance Testing (LDR: ≤10mrad(Si)/s)
  - ISL74420M30NZ: 30krad(Si)
  - ISL74420M50NZ: 50krad(Si)
- SEE Characterization
  - No DSEE for PVIN = 20.7V, V_{CC} = 5.5V, and VCCEXT = 6.5V at 46MeV·cm²/mg
  - SEFI <10µm² at 46MeV·cm²/mg
  - No missing pulse SETs and Frequency Deviation SETs <3.6% on CLKOUTx at 46MeV·cm²/mg

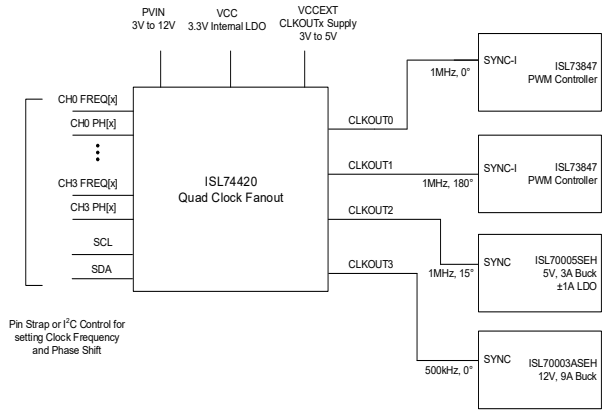


Figure 1. Typical Application

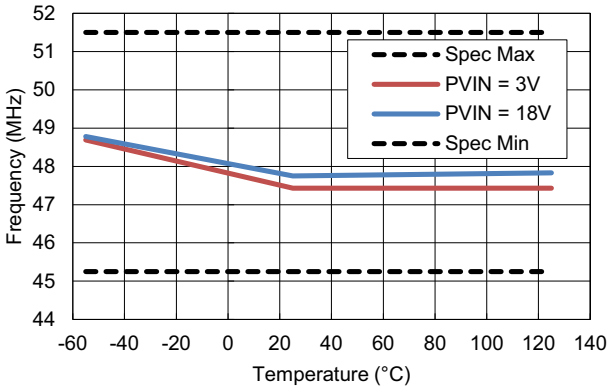


Figure 2. Internal Oscillator Nominal Frequency Accuracy Over Temp

Contents

1. Overview

1.1 Typical Application

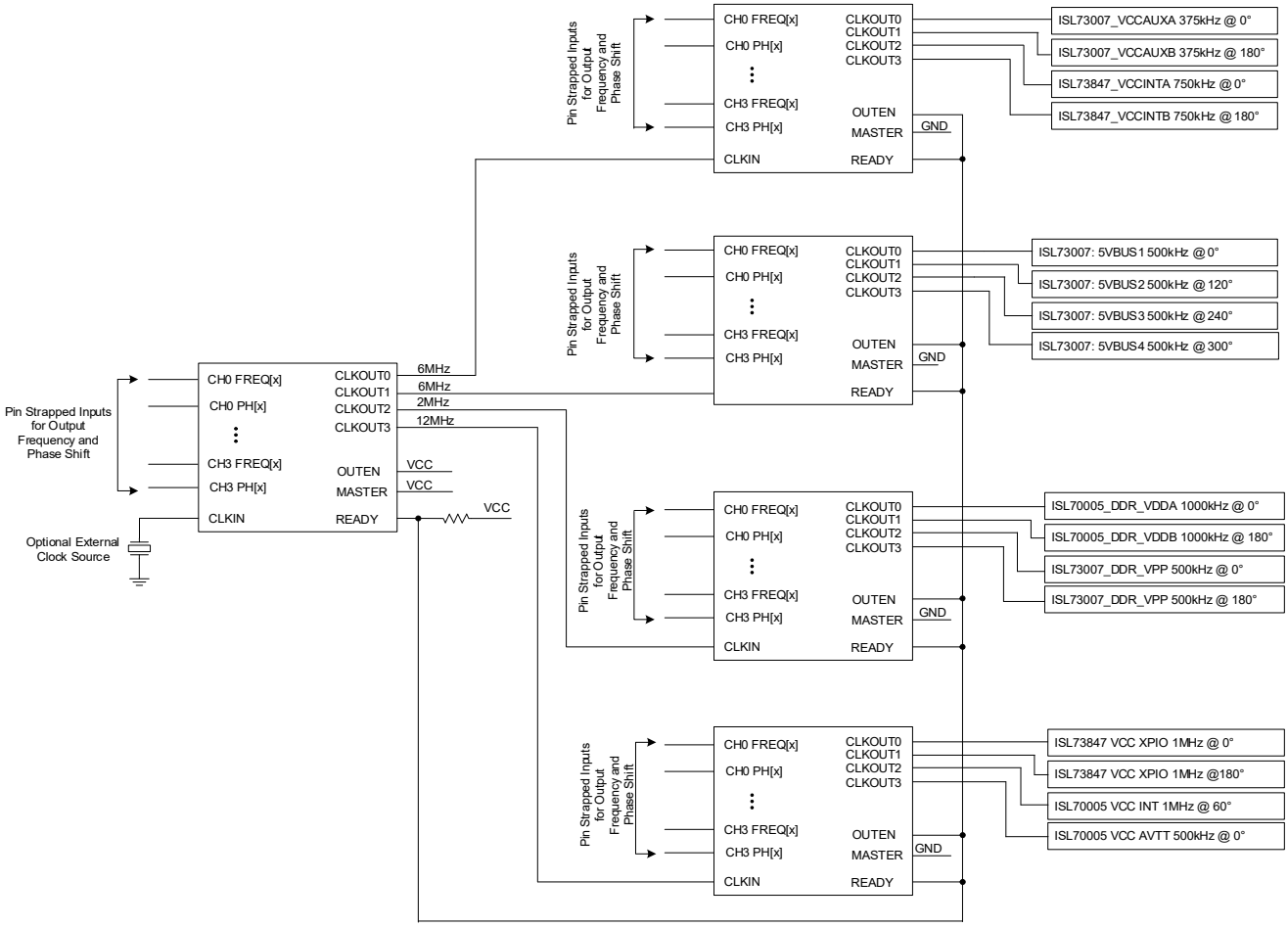


Figure 3. Leader-Follower Configuration for Multi-Channel Application

1.2 Block Diagram

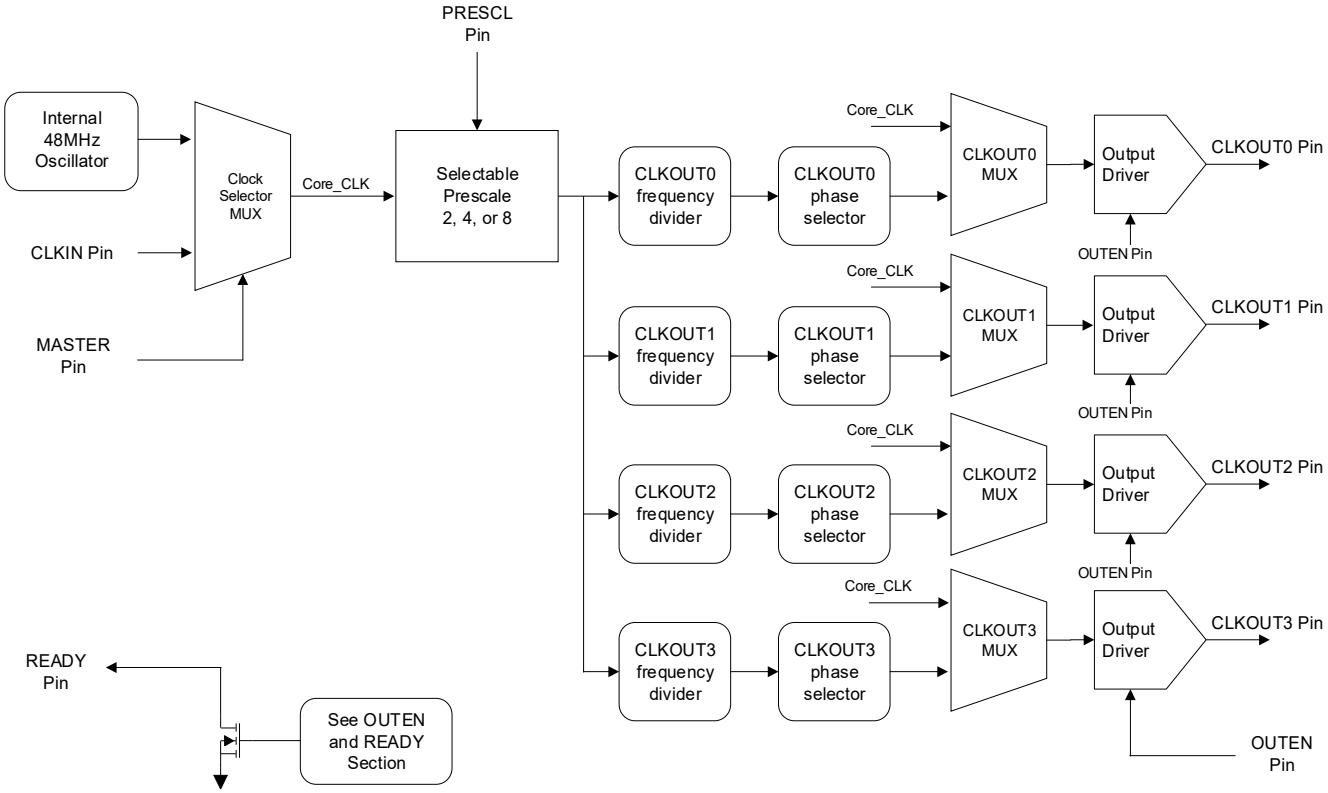


Figure 4. Block Diagram

2. Pin Information

2.1 Pin Assignments

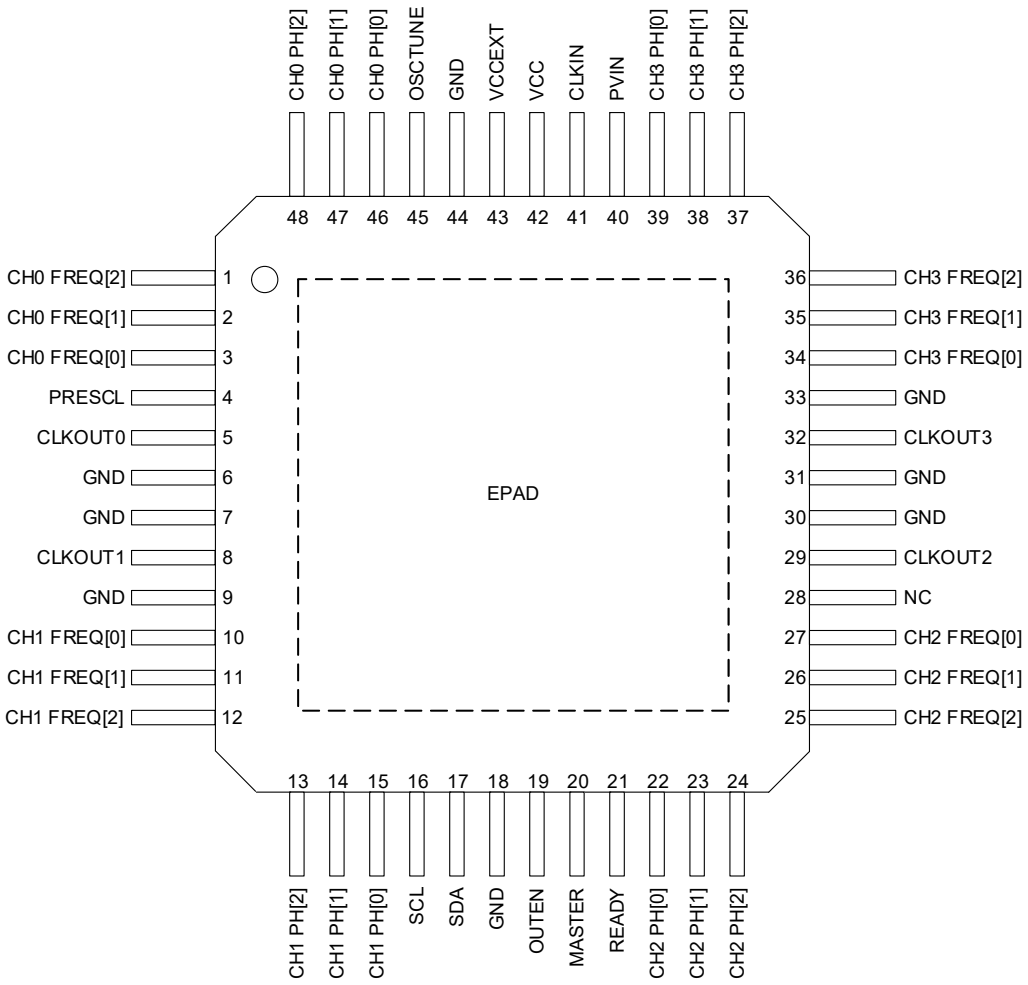


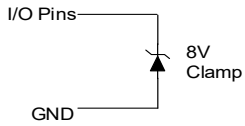
Figure 5. Pin Assignments - Top View

2.2 Pin Descriptions

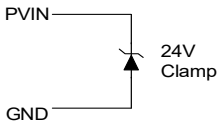
Pin Number	Pin Name	ESD Circuit	Description
1	CH0 FREQ[2]	1	3-level (tri-level) logic with 3-bit setting for frequency division selection on Channel 0.
2	CH0 FREQ[1]	1	
3	CH0 FREQ[0]	1	
4	PRESCL	1	3-level (tri-level) logic prescale selection for all channels.
5	CLKOUT0	3	Clock output pin for Channel 0.
6, 7, 9, 30, 31, 33, 44	GND	-	Connect these pins to the PCB ground.
8	CLKOUT1	3	Clock output pin for Channel 1

Pin Number	Pin Name	ESD Circuit	Description
10	CH1 FREQ[0]	1	3-level (tri-level) logic with 3-bit setting for frequency division selection on Channel 1
11	CH1 FREQ[1]	1	
12	CH1 FREQ[2]	1	
13	CH1 PH[2]	1	3-level (tri-level) logic with 3-bit setting for phase delay selection for Channel 1.
14	CH1 PH[1]	1	
15	CH1 PH[0]	1	
16	SCL	1	I^2C/SMBus clock input. SCL requires an external pull-up resistor for proper operation. Tie to VCC through a 4.7kΩ to 100kΩ resistor even if I^2C/SMBus is not going to be used.
17	SDA	1	I^2C/SMBus data input/output. SDA requires an external pull-up resistor for proper operation. Tie to VCC through a 4.7kΩ to 100kΩ resistor even if I^2C/SMBus is not going to be used.
18	GND	-	Connect this pin to the PCB ground.
19	OUTEN	1	Logic level input to enable the CLKOUTx pins.
20	MASTER	1	Logic level input to select if the part should use its internal oscillator when no external clock is present. A logic high enables Leader Mode and uses the internal 48MHz oscillator if no CLK-IN signal is present. A logic low enables Follower Mode and the internal oscillator is disabled, relying only on the CLK-IN input.
21	READY	1	Open-drain output to indicate if the part is ready to enable the CLKOUTx pins
22	CH2 PH[0]	1	3-level (tri-level) logic with 3-bit setting for phase delay selection for Channel 2.
23	CH2 PH[1]	1	
24	CH2 PH[2]	1	
25	CH2 FREQ[2]	1	3-level (tri-level) logic with 3-bit setting for frequency division selection on Channel 2.
26	CH2 FREQ[1]	1	
27	CH2 FREQ[0]	1	
28	NC	-	No internal connection. Renesas recommends connecting this pin to GND.
29	CLKOUT2	3	Clock output pin or Channel 2.
32	CLKOUT3	3	Clock output pin or Channel 3.
34	CH3 FREQ[0]	1	3-level (tri-level) logic with 3-bit setting for frequency division selection on Channel 3.
35	CH3 FREQ[1]	1	
36	CH3 FREQ[2]	1	
37	CH3 PH[2]	1	3-level (tri-level) logic with 3-bit setting for phase delay selection for Channel 3.
38	CH3 PH[1]	1	
39	CH3 PH[0]	1	
40	PVIN	2	The power supply input to the IC. This supplies power to the internal linear regulator. Locally bypass PVIN to GND with a 0.1µF or larger capacitor.
41	CLKIN	1	External clock input. Tie this pin to the ISL74420M GND with a short trace if not using CLKIN.
42	VCC	1	Output of the 3.3V internal linear regulator. The regulator can by bypassed by providing a 3.0V to 3.6V supply to both PVIN and VCC. Locally bypass VCC to GND with a 1µF capacitor.
43	VCCEXT	1	The power supply input for all of the CLKOUTx pins. This can be connected to VCC or supplied externally to level shift them to a different voltage. If supplied externally, locally bypass VCCEXT to GND with a 1µF or larger capacitor.
45	OSCTUNE	1	Connect a resistor between this pin and GND to adjust the internal oscillator.

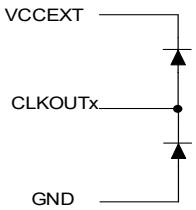
Pin Number	Pin Name	ESD Circuit	Description
46	CH0 PH[0]	1	3-level (tri-level) logic with 3-bit setting for phase delay selection for Channel 0.
47	CH0 PH[1]	1	
48	CH0 PH[2]	1	
-	EPAD	-	Connect to the PCB ground.



Circuit 1



Circuit 2



Circuit 3

3. Specifications

3.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
PVIN	GND - 0.3	GND + 20	V
PVIN[1]	GND - 0.3	GND + 20	V
VCC, VCCEXT	GND - 0.3	GND + 6.5	V
VCC[1], VCCEXT[1]	GND - 0.3	GND + 6.5	V
OSCTUNE	GND - 0.3	VCC	V
CLKIN	GND - 0.3	GND + 6.5	V
CLKOUTx	GND - 0.3	VCCEXT + 0.3; GND + 6.5	V
CHx PH[x], CHx FREQ[x]	GND - 0.3	GND + 6.5	V
SDA, SCL	GND - 0.3	GND + 6.5	V
READY	GND - 0.3	GND + 6.5	V
MASTER, OUTEN	GND - 0.3	GND + 6.5	V
Junction Temperature	-55	+150	°C
Storage Temperature	-65	+150	°C
Human Body Model (Tested per JS-001-2023)	-	2.0	kV
Charged Device Model (Tested per JS-002-2022)	-	750	V
Latch-Up (Tested per JESD78E; Class 2, Level A)	-	±100	mA

1. Tested under a heavy ion environment at LET = 46MeV•cm^2/mg at +125°C (T_C) for SEB.

3.2 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
PVIN	GND + 3.0	GND + 18	V
VCC	GND + 3.0	GND + 3.6	V
VCCEXT	GND + 3.0	GND + 5.5	V
CLKIN	GND	VCC	V
CLKOUTx	GND	VCCEXT	V
CHx PH[x], CHx FREQ[x]	GND	VCC	V
SDA, SCL	GND	VCC	V
READY	GND	GND + 5.5	V
MASTER, OUTEN	GND	VCC	V
Ambient Temperature	-55	+125	°C

3.3 Outgas Testing

Specification (Tested per ASTM E595, 1.5)	Value	Unit
Total Mass Lost[1]	0.04	%

Specification (Tested per ASTM E595, 1.5)	Value	Unit
Collected Volatile Condensible Material[1]	<0.01	%
Water Vapor Recovered	0.01	%

1. Outgassing results meet NASA requirements of total mass loss <1% and collected volatile condensible material <0.1%.

3.4 Thermal Specifications

Parameter	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance	48 Ld 7×7mm TQFP-EP Package	θ_{JA}[1]	Junction to ambient	26	°C/W
		θ_{JC}[2]	Junction to case	2.3	

1. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.
2. For θ_{JC}, the case temperature location is the center of the exposed metal pad on the package underside.

3.5 Electrical Specifications

Unless otherwise noted, PVIN = 3V, 18V, CVCC = 1µF, VCCEXT tied to VCC, OUTEN = VCC, ROSCTUNE = 12.7kΩ, C_{CLKOUT}[0:3] = 12pF, CLKIN = GND, MASTER = VCC, PRESCL = GND, frequency and phase options set using I^2C/SMBus mode. **Boldface limits apply across the operating temperature range, -55°C to +125°C by characterization with production testing at +25°C; over a total ionizing dose of 30krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL74420M30NZ); or over a total ionizing dose of 50krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL74420M50NZ).**

Parameter	Symbol	Test Conditions	Temp.	Min	Typ[1]	Max	Unit
Input Power Supply							
Supply Voltage	V_{PVIN_RANGE}	-	-55 to +125°C	**3.0**	-	**18**	V
UVLO Rising Threshold	V_{UVLO-R}	PVIN = VCC = VCCEXT	-55 to +125°C	-	2.91	**2.95**	V
UVLO Falling Threshold	V_{UVLO-F}	PVIN = VCC = VCCEXT	-55 to +125°C	**2.65**	2.79	-	V
PVIN Operating Supply Current - Leader Mode 48MHz out	I_{PVIN_OPER1}	PVIN = 12V, CH[0:3]FREQ = Option 0	-55 to +125°C	**29**	33	**36**	mA
PVIN Operating Supply Current - Leader Mode 48MHz out with CLKIN	I_{PVIN_OPER2}	PVIN = 12V, CH[0:3]FREQ = Option 0, MASTER = VCC, CLKIN = 48MHz	-55 to +125°C	**32**	36	**40**	mA
PVIN Operating Supply Current - Follower Mode	I_{PVIN_OPER3}	PVIN = 12V, CH[0:3]FREQ = Option 0, MASTER = GND, CLKIN = 48MHz	-55 to +125°C	**24**	27	**30**	mA
PVIN Operating Supply Current - Leader Mode 1MHz out	I_{PVIN_OPER4}	PVIN = 12V, CH[0:3]FREQ = Opt. 5 (1MHz), CH[0:3]PH = 0°, 90°, 180°, 270°	-55 to +125°C	**18**	22	**25**	mA
VCCEXT Supply Current	I_{VCCEXT_MAX}	PVIN = 12V, VCCEXT = 5.5V, CH[0:3]FREQ = Option 0	-55 to +125°C	**29**	35	**45**	mA
PVIN Standby Leader Mode Supply Current	I_{PVIN_SB1}	PVIN = 12V, OUTEN = GND, VCCEXT tied to VCC	-55 to +125°C	**12**	18	**20**	mA
PVIN Standby Follower Mode Supply Current	I_{PVIN_SB2}	PVIN = 12V, OUTEN = GND, MASTER = GND, CLKIN = GND, VCCEXT tied to VCC	-55 to +125°C	**0.5**	1.1	**2**	mA
VCC LDO							
VCC Voltage Tolerance (Accuracy)	V_{VCC}	PVIN = [3.5V, 5V, 12V, 18V], I_{LOAD} = 50mA	-55 to +125°C	**3**	3.3	**3.6**	V

Unless otherwise noted, PVIN = 3V, 18V, CVCC = 1µF, VCCEXT tied to VCC, OUTEN = VCC, ROSCTUNE = 12.7kΩ, C_{CLKOUT}[0:3] = 12pF, CLKIN = GND, MASTER = VCC, PRESCL = GND, frequency and phase options set using I^2C/SMBus mode. **Boldface limits apply across the operating temperature range, -55°C to +125°C by characterization with production testing at +25°C; over a total ionizing dose of 30krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL74420M30NZ); or over a total ionizing dose of 50krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL74420M50NZ). (Cont.)**

Parameter	Symbol	Test Conditions	Temp.	Min	Typ[1]	Max	Unit
VCC Dropout Voltage	VCC_{DO}	PVIN = 3.25V, I_{LOAD} = 50mA, VCCEXT = 3.3V, OUTEN = GND, MASTER = GND, CLKIN = GND	-55 to +125°C	**100**	160	**220**	mV
VCC Current Limit	$I_{AVCC-CL}$	PVIN = [5V, 12V, 18V], VCC = 2.9V, VCCEXT = 3.3V, OUTEN = GND, MASTER = GND, CLKIN = GND	-55 to +125°C	**75**	108	**130**	mA
VCC Foldback Current Limit	$I_{AVCC-SC}$	PVIN = [5V, 12V, 18V], VCC = GND, VCCEXT = 3.3V	-55 to +125°C	**40**	68	**90**	mA
Startup							
Time after Rising PVIN to READY Signal[2]	$T_{PVIN-READY}$	PVIN = step 2V to 4V, CH3FREQ = non-I^2C/SMBus Mode	-55 to +125°C	**1.7**	2.2	**2.7**	ms
Time after OUTEN to CLKOUT with Phase = 0°[3]	$T_{OUTEN-OUT}$	PVIN = 5V, CH[0:3]PH = 0°, OUTEN rising	-55 to +125°C	**70**	105	**180**	ns
		PVIN = 5V, MASTER = GND, CLKIN = 48MHz, CH[0:3]PH = 0°, OUTEN rising					
Clock Output Timing							
Internal Oscillator Nominal Frequency	InternalOsc_Nom	OSCTUNE = 12.7kΩ, PVIN = VCC = [3V, 3.6V] VCC regulating and PVIN = [5V, 12V, 18V]	-55°C	47.5	49.92	51.5	MHz
			+25°C	46.50	48.22	49.25	
			+125°C	45.25	47.59	49.0	
			+25°C (Post Rad)	46.25	47.72	49.25	
Internal Oscillator Minimum Frequency	InternalOsc_Min	PVIN = [5V, 12V, 18V], OSCTUNE = 26.7kΩ	-55 to +125°C	**41.0**	43.6	**46.2**	MHz
Internal Oscillator Minimum Frequency	InternalOsc_Min	PVIN = VCC = [3V, 3.6V], OSCTUNE = 26.7kΩ	-55 to +125°C	**41.0**	43.6	**46.2**	MHz
Internal Oscillator Maximum Frequency	InternalOsc_Max	PVIN = [5V, 12V, 18V], OSCTUNE = 8.2kΩ	-55 to +125°C	**49.5**	52.8	**56.5**	MHz
Internal Oscillator Maximum Frequency	InternalOsc_Max	PVIN = VCC = [3V, 3.6V], OSCTUNE = 8.2kΩ	-55 to +125°C	**48.5**	52.5	**56.5**	MHz
Allowed CLKIN frequency to Override Internal Oscillator in Leader Mode	CLKINFREQ_M	MASTER = VCC, CLKIN = [40%, 60%] duty cycle. CH[0:3]FREQ = Option 1	-55 to +125°C	**35**	-	**50**	MHz
Output Duty Cycle in Leader Mode with Internal Oscillator	M_int_Duty_Cycle	OSCTUNE = 8.2kΩ, CH[0:3]FREQ = Option 1	-55 to +125°C	**30**	42	**50**	%
Output Duty Cycle in Leader Mode with CLKIN	M_clkin_Duty_Cycle	OSCTUNE = 12.7kΩ, MASTER = VCC, CLKINfreq = 50MHz, CLKINduty = [40%, 60%] duty cycle, CH[0:3]FREQ = Option 1	-55 to +125°C	**30**	42	**50**	%

Unless otherwise noted, PVIN = 3V, 18V, CVCC = 1µF, VCCEXT tied to VCC, OUTEN = VCC, ROSCTUNE = 12.7kΩ, C_{CLKOUT}[0:3] = 12pF, CLKIN = GND, MASTER = VCC, PRESCL = GND, frequency and phase options set using I^2C/SMBus mode. **Boldface limits apply across the operating temperature range, -55°C to +125°C by characterization with production testing at +25°C; over a total ionizing dose of 30krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL74420M30NZ); or over a total ionizing dose of 50krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL74420M50NZ). (Cont.)**

Parameter	Symbol	Test Conditions	Temp.	Min	Typ[1]	Max	Unit
Allowed CLKIN Frequency for Follower Mode[4]	CLKINFREQ_S	VCCEXT = [VCC, 5.5V], MASTER = GND, CLKIN = [30%, 65%] duty cycle, CH[0:3]FREQ = Option 0	-55 to +125°C	**DC**	-	**30**	MHz
		VCCEXT = [VCC, 5.5V], MASTER = GND, CLKIN = [40%, 60%] duty cycle, CH[0:3]FREQ = Option 1		**DC**	-	**50**	
Output Duty Cycle in Follower Mode	S_Duty_Cycle	VCCEXT = [VCC, 5.5V] MASTER = GND, CLKINfreq = 30MHz, CLKIN duty = 30% duty cycle, CH[0:3]FREQ = Option 0	-55 to +125°C	**20**	30	**40**	%
		VCCEXT = [VCC, 5.5V] MASTER = GND, CLKINfreq = 30MHz, CLKIN duty = 65% duty cycle, CH[0:3]FREQ = Option 0		**55**	65	**75**	
		VCCEXT = [VCC, 5.5V] MASTER = GND, CLKINfreq = 50MHz, CLKINduty = [40%, 60%] duty cycle, CH[0:3]FREQ = Option 1		**30**	40	**50**	
Duty Cycle of a Divided Clock	div_Duty_Cycle	VCCEXT = [VCC, 5.5V]; CH[0:3]FREQ = Opt. 3 (4MHz)	-55 to +125°C	**47**	48.3	**50**	%
Output-to-Output Skew between CLKOUTx's with Equal Frequency and Phase	$CLKOUTx_{SKEW48M}$	MASTER = GND, CLKIN = 48MHz, CH[0:3]FREQ = Option 0	-55 to +125°C	**-1.5**	0.5	**1.5**	ns
Output-to-Output Skew between CLKOUTx's with Equal Frequency and Phase	$CLKOUTx_{SKEW1M}$	MASTER = GND, CLKIN = 48MHz, CH[0:3]FREQ = Opt. 5 (1MHz), equal phase	-55 to +125°C	**-6**	2	**6**	ns
Output-to-Output Skew Between CLKOUTx's with Equal Frequency and Different Phase	$CLKOUTx_{SKEW1M4P}$	MASTER = GND, CLKIN = 48MHz, CH[0:3]FREQ = Opt. 5 (1MHz), CH[0:3]PH = 0°, 90°, 180°, 270°	-55 to +125°C	**-7**	2	**7**	ns
CLKIN-to-CLKOUT Follower Mode Propagation Delay	$CLK_{PROPDELAY}$	MASTER = GND, CH[0:3]FREQ = Option 0, CLKIN = 1MHz	-55 to +125°C	**20**	29	**40**	ns
Internal Oscillator Phase Jitter, RMS (Random)[5][6]	tjitter (ϕ)	MASTER = VCC, CLKIN = GND, CH[0:3]FREQ = Option 1 24MHz, Period @ level >8k samples	-55 to +125°C	-	25	-	ps
Additive (Follower Mode) Phase Jitter, RMS (Random)[5][7]	tjitter (ϕ)	MASTER = GND, CLKIN = 48MHz, CH[0:3]FREQ = Option 1, 24MHz Period @ level >8k samples	-55 to +125°C	-	31	-	ps

Unless otherwise noted, PVIN = 3V, 18V, CVCC = 1µF, VCCEXT tied to VCC, OUTEN = VCC, ROSCTUNE = 12.7kΩ, C_{CLKOUT}[0:3] = 12pF, CLKIN = GND, MASTER = VCC, PRESCL = GND, frequency and phase options set using I^2C/SMBus mode. **Boldface limits apply across the operating temperature range, -55°C to +125°C by characterization with production testing at +25°C; over a total ionizing dose of 30krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL74420M30NZ); or over a total ionizing dose of 50krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL74420M50NZ). (Cont.)**

Parameter	Symbol	Test Conditions	Temp.	Min	Typ[1]	Max	Unit
Rise/Fall Times of the Outputs	T_{OUT_RF3p3}	PVIN = 12V, MASTER = GND, CLKIN = 1MHz, CH[0:3]FREQ = Option 0, VCCEXT = 3.3V, Measured 80%/20%	-55 to +125°C	-	1.9	**5**	ns
	T_{OUT_RF5}	PVIN = 12V, MASTER = GND, CLKIN = 1MHz, CH[0:3]FREQ = Option 0, VCCEXT = 5.5V, Measured 80%/20%		-	2.0	**5**	
Clock and Ready Outputs							
Output Voltage High	$CLKOUTx_{VOH}$	PVIN = 12V, MASTER = GND, CLKIN = 3.3V, CH[0:3]FREQ = Option 0, VCCEXT = 3.3V, I_{LOAD} = 1mA	-55 to +125°C	**3**	3.28	**3.3**	V
		PVIN = 12V, MASTER = GND, CLKIN = 3.3V, CH[0:3]FREQ = Option 0, VCCEXT = 3.3V, I_{LOAD} = 10mA		**2.7**	3.06	**3.3**	
		PVIN = 12V, MASTER = GND, CLKIN = 3.3V, CH[0:3]FREQ = Option 0, VCCEXT = 5.V, I_{LOAD} = 1mA		**4.5**	4.98	**5**	
		PVIN = 12V, MASTER = GND, CLKIN = 3.3V, CH[0:3]FREQ = Option 0, VCCEXT = 5V, I_{LOAD} = 10mA		**4**	4.81	**5**	
Output Voltage Low	$CLKOUTx_{VOL}$	PVIN = 12V, MASTER = GND, CLKIN = GND, CH[0:3]FREQ = Option 0, VCCEXT = 3.3V, I_{LOAD} = 1mA	-55 to +125°C	**0**	0.02	**0.3**	V
		PVIN = 12V, MASTER = GND, CLKIN = GND, CH[0:3]FREQ = Option 0, VCCEXT = 3.3V, I_{LOAD} = 10mA		**0**	0.2	**0.3**	
		PVIN = 12V, MASTER = GND, CLKIN = GND, CH[0:3]FREQ = Option 0, VCCEXT = 5V, I_{LOAD} = 1mA		**0**	0.02	**0.3**	
		PVIN = 12V, MASTER = GND, CLKIN = GND, CH[0:3]FREQ = Option 0, VCCEXT = 5V, I_{LOAD} = 10mA		**0**	0.15	**0.3**	
READY Voltage Low[3]	$READY_{VOL}$	I_{LOAD} = 1mA	-55 to +125°C	**0**	0.04	**0.3**	V
		I_{LOAD} = 10mA		**0**	0.15	**0.3**	
Input Thresholds							
OUTEN/MASTER Threshold High	$OUTEN/MASTER_{VIH}$	-	-55 to +125°C	**1.35**	1.65	**2**	V
OUTEN/MASTER Threshold Low	$OUTEN/MASTER_{VIL}$	-	-55 to +125°C	**0.8**	1.35	**1.65**	V
OUTEN/MASTER Voltage Hysteresis	$OUTEN/MASTER_{hyst}$	-	-55 to +125°C	**0.2**	0.3	**0.5**	V

Unless otherwise noted, PVIN = 3V, 18V, CVCC = 1µF, VCCEXT tied to VCC, OUTEN = VCC, ROSCTUNE = 12.7kΩ, C_{CLKOUT}[0:3] = 12pF, CLKIN = GND, MASTER = VCC, PRESCL = GND, frequency and phase options set using I^2C/SMBus mode. **Boldface limits apply across the operating temperature range, -55°C to +125°C by characterization with production testing at +25°C; over a total ionizing dose of 30krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL74420M30NZ); or over a total ionizing dose of 50krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL74420M50NZ). (Cont.)**

Parameter	Symbol	Test Conditions	Temp.	Min	Typ[1]	Max	Unit
CLKIN Voltage High Level	CLKIN_H	-	-55 to +125°C	**2**	-	-	V
CLKIN Voltage Low Level	CLKIN_L	-	-55 to +125°C	-	-	**0.8**	V

1. Typical values shown are not guaranteed.
2. CH3FREQ must be pin-configured for this test. The part holds READY low until the appropriate I^2C/SMBus command is received if it is configured for I^2C/SMBus mode.
3. Channels set to a phase of 0° transition to High after OUTEN is raised and CLKIN transitions high. A slower CLKIN adds to the apparent variation of this delay. Phase selections greater than 0° are delayed by some number of CLKIN pulses as their frequency division and phase selection demands.
4. A ISL74420M in Follower mode receiving a CLKIN of 48MHz or faster from another ISL74420M should not be set to frequency option 0. The duty cycle of high speed clock signals can degrade beyond the point that it is usable.
5. Limits established by characterization and/or design analysis and are not production tested.
6. Average of RMS Jitter values all four channels at 24MHz.
7. Average of RMS Jitter values all four channels at 24MHz, CLKIN RMS Jitter ~18ps.

3.6 I^2C/SMBus Interface Specifications

Unless otherwise noted, PVIN = 3V, 18V, CVCC = 1µF, VCCEXT tied to VCC, OUTEN = VCC, ROSCTUNE = 12.7kΩ, CCLKOUT[0:3] = 12pF, CLKIN = GND, MASTER = VCC, PRESCL = GND, frequency and phase options set using I^2C/SMBus mode.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SDA/SCL Pin Specifications						
Low-Level Input Voltage	V_{IL}	-	-	-	0.45	V
High-Level Input Voltage	V_{IH}	-	1.35	-	-	V
Low-Level Output Voltage	V_{OL}	4mA Sink into SDA/SCL pin	0	-	0.4	V
Low-level Output Current	I_{OL}	V_{OL} = 0.4V	4	-	-	mA
Output Fall Time from VIHmin to VILmax	t_F	From VIHmin to VILmax	-	-	250	ns
Input Current for each I/O Pin	Ii	0.1×VCC < VI < 0.9×VCCmax	-10	-	10	µA
Capacitance for each I/O Pin	Ci	Guaranteed by Design, not production tested	-	-	10	pF
SDA/SCL Timing Specifications						
SCL Clock Frequency	f_{SCL}	-	-	-	100	kHz
Hold Time (Repeated) START condition	$t_{HD;STA}$	After this period, the first clock pulse is generated.	4.0	-	-	µs
Setup Time for a Repeated START Condition	$t_{SU;STA}$	-	4.7	-	-	µs
Low Period of the SCL Clock	t_{LOW}	-	4.7	-	-	µs
High Period of the SCL Clock	t_{HIGH}	-	4.0	-	50	µs
Data Hold Time	$t_{HD;DAT}$	-	0	-	-	µs
Data Setup Time	$t_{SU;DAT}$	-	250	-	-	ns

Unless otherwise noted, PVIN = 3V, 18V, CVCC = 1µF, VCCEXT tied to VCC, OUTEN = VCC, ROSCTUNE = 12.7kΩ, CCLKOUT[0:3] = 12pF, CLKIN = GND, MASTER = VCC, PRESCL = GND, frequency and phase options set using I^2C/SMBus mode.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Setup Time for STOP Condition	$t_{SU;STO}$	-	4.0	-	-	µs
Bus-Free Time between a STOP and START Condition	t_{BUF}	-	4.7	-	-	µs

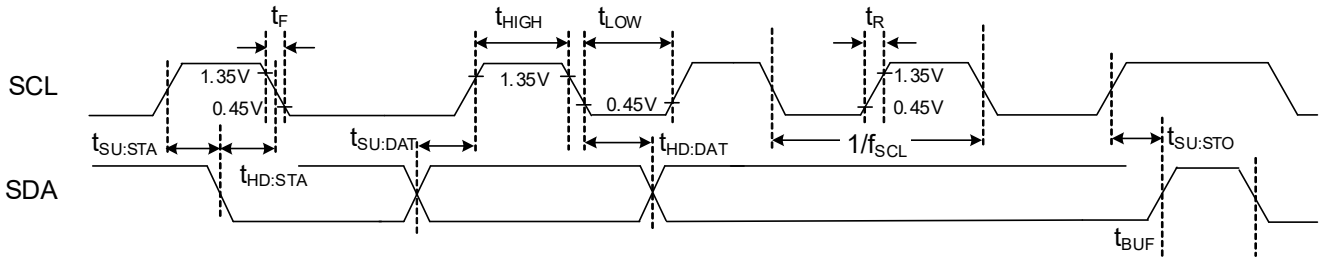


Figure 6. I^2C/SMBus SDA vs SCL Timing

4. Typical Performance Graphs

PVIN = 12V, CVCC = 1µF, VCCEXT tied to VCC, OUTEN = VCC, ROSCTUNE = 12.7kΩ, CCLKOUT[0:3] = 12pF, CLKIN = GND, MASTER = VCC, PRESCL = GND, unless otherwise stated.

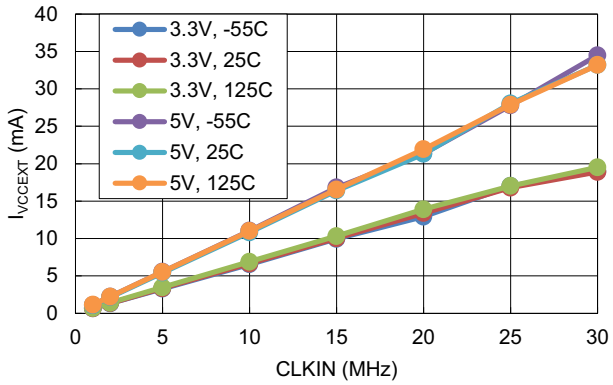


Figure 7. VCCEXT Supply Current vs CLKIN frequency and VCCEXT; MASTER = GND, CH[0:3]FREQ = Option 0

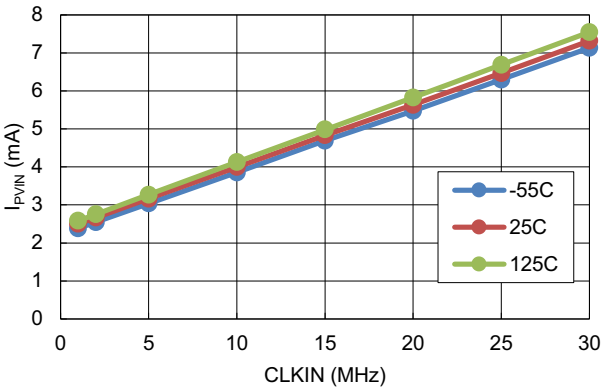


Figure 8. PVIN Supply Current vs CLKIN Frequency and Temperature; MASTER = GND

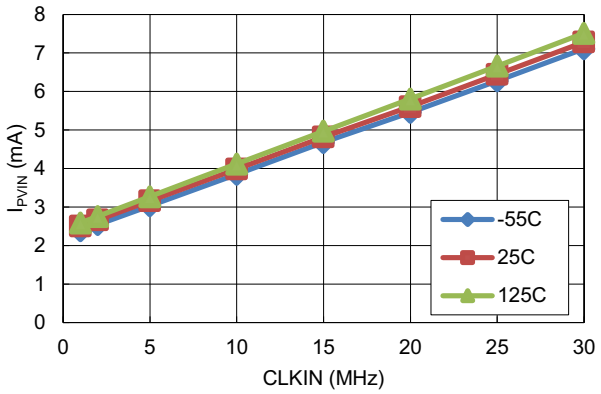


Figure 9. PVIN Supply Current with OUTEN Low vs CLKIN; MASTER = GND

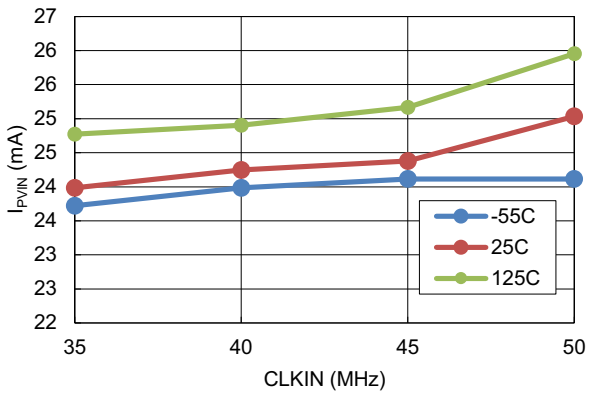


Figure 10. PVIN Supply Current vs CLKIN Frequency and Temperature; MASTER = VCC

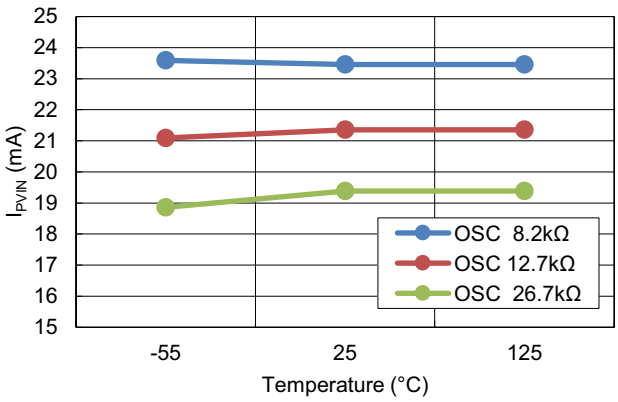


Figure 11. PVIN Supply Current vs OSCTUNE Resistor and Temperature; MASTER = VCC

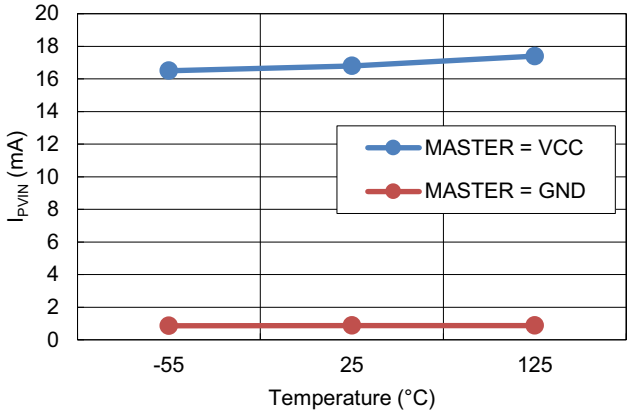


Figure 12. PVIN Shutdown Supply Current vs Temperature without CLKIN; OUTEN = LOW

PVIN = 12V, CVCC = 1µF, VCCEXT tied to VCC, OUTEN = VCC, ROSCTUNE = 12.7kΩ, CCLKOUT[0:3] = 12pF, CLKIN = GND, MASTER = VCC, PRESCL = GND, unless otherwise stated. (Cont.)

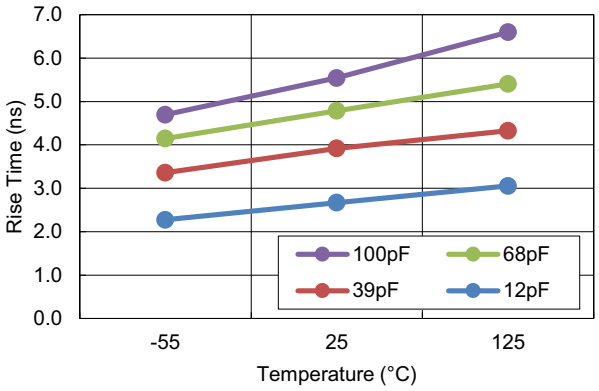


Figure 13. 20% to 80% Rise Time vs CLKOUT Load Capacitance

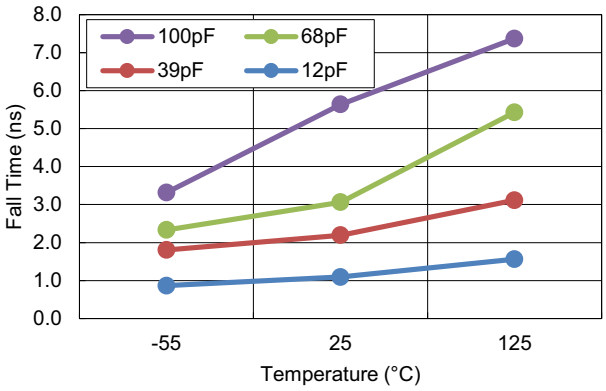


Figure 14. 80% to 20% Fall Time vs CLKOUT Load Capacitance

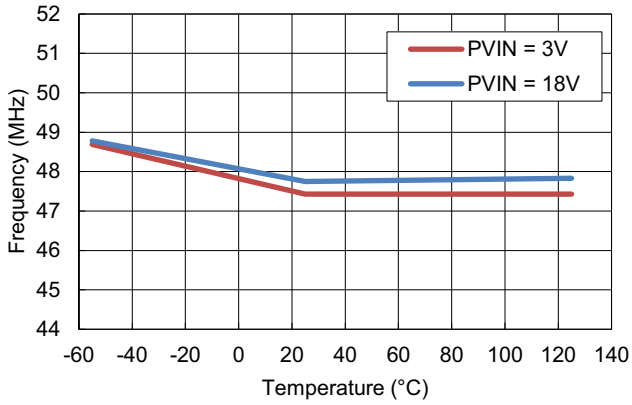


Figure 15. Internal Oscillator Nominal Frequency (OSCTUNE = 12.7kΩ) Accuracy Over Temp

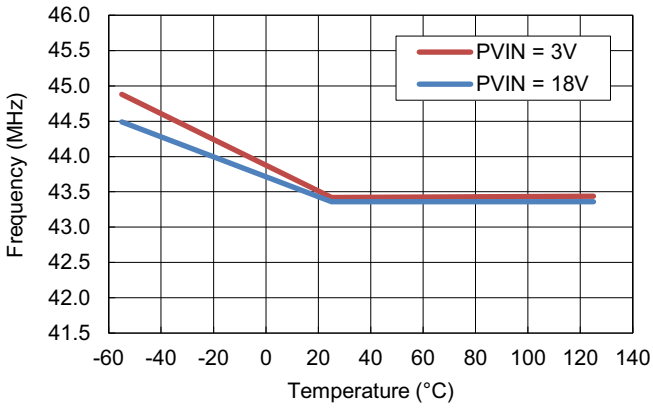


Figure 16. Internal Oscillator Minimum Frequency (OSCTUNE = 26.7kΩ) Accuracy Over Temp

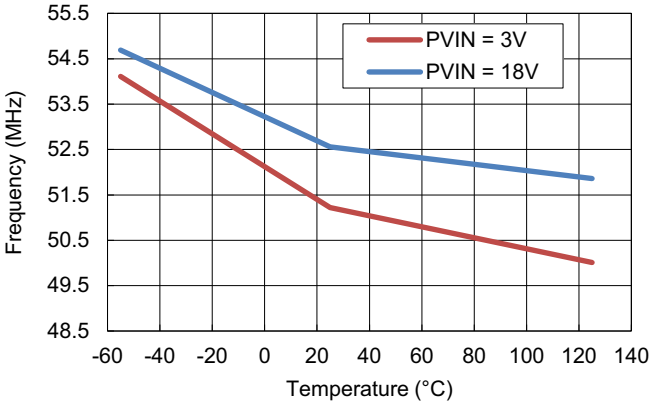


Figure 17. Internal Oscillator Maximum Frequency (With OSCTUNE = 8.2kΩ) Accuracy Over Temp

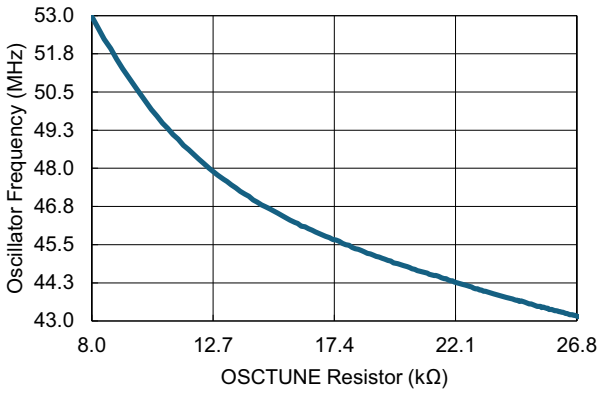


Figure 18. Internal Oscillator Frequency vs OSCTUNE Resistor

5. Operation

5.1 Frequency and I²C/SMBus Address Selection

Each channel of the ISL74420M can be configured to output a different frequency. All channels are subject to the prescale configuration. Ensure that all required frequencies are within the same frequency column of Table 1. If a wider variety of frequencies is required, multiple chips can be cascaded or driven from the same external clock.

Table 1. Frequency Selections

FREQ Option # (Hex)	CHx FREQ [2]	CHx FREQ [1]	CHx FREQ [0]	CLKOUT Frequency (Hz) PRESCL = LOW	CLKOUT Frequency (Hz) PRESCL = FLOAT	CLKOUT Frequency (Hz) PRESCL = HIGH	Supported Phase Options
0 (0x00)	Low	Low	Low	48M	48M	48M	0°
1 (0x01)	Low	Low	Float	24M	12M	6M	0°, 180°
2 (0x02)	Low	Low	High	12M	6M	3M	0°, 90°, 180°, 270°
3 (0x03)	Low	Float	Low	4M	2M	1M	0°, 60°, 120°, 180°, 240°, 300°
4 (0x04)	Low	Float	Float	2M	1M	500k	all 24 (every 15°)
5 (0x05)	Low	Float	High	1M	500k	250k	all 24
6 (0x06)	Low	High	Low	500k	250k	125k	all 24
7 (0x07)	Low	High	Float	400k	200k	100k	all 24
8 (0x08)	Low	High	High	333k	167k	83.3k	all 24
9 (0x09)	Float	Low	Low	250k	125k	62.5k	all 24
10 (0x0a)	Float	Low	Float	200k	100k	50k	all 24
11 (0x0b)	Float	Low	High	167k	83.3k	41.7k	all 24
12 (0x0c)	Float	Float	Low	125k	62.5k	31.3k	all 24
13 (0x0d)	Float	Float	Float	100k	50k	25k	all 24

The ISL74420M divides down a clock frequency to generate the various output frequency options. When operating with a CLKIN or internal oscillator tuned to a frequency other than 48MHz, derive the division ratio and use it instead of the frequency selection.

(EQ. 1) $$f_{OUT} = \frac{f_{CORE}}{48 \times 10^6 Hz} \times f_{OPTION}$$

- f_{CORE} is the CLKIN or internal oscillator frequency in Hz.
- f_{OPTION} is the selected frequency option from the table in Hz.
- f_{OUT} is the frequency that is provided on the CLKOUT pin in Hz.

Using this characteristic and chaining multiple ISL74420M together allows the generation of even lower frequency clocks. For example, feeding a 25kHz clock into a ISL74420M configured for the lowest frequency yields a 13Hz clock.

The frequency selection pins for Channel 3 (CH3_FREQ2, CH3_FREQ1, and CH3_FREQ0) also serve as I²C/SMBus address selection pins. When Option 19 through 26 is selected by the CH3_FREQ pins, the CLKOUT3 frequency defaults to Option 0 and must be overwritten with the required setting. The pin-selected frequencies and phases for all channels can be read and written using I²C/SMBus.

Table 2. CH3_FREQ Pin Configuration For Distinct I²C/SMbus Addresses

Option #	CH3_FREQ[2]	CH3_FREQ[1]	CH3_FREQ[0]	CLKOUT3 Frequency	7-Bit I²C/SMBus Address	8-Bit Read Address	8-Bit Write Address
0 - 13	Reference Table 1.			selected option	0x50	0xA1	0xA0
19	High	Low	Float	Write 0xD7 to set freq.	0x50	0xA1	0xA0
20	High	Low	High	Write 0xD7 to set freq.	0x51	0xA3	0xA2
21	High	Float	Low	Write 0xD7 to set freq.	0x52	0xA5	0xA4
22	High	Float	Float	Write 0xD7 to set freq.	0x53	0xA7	0xA6
23	High	Float	High	Write 0xD7 to set freq.	0x54	0xA9	0xA8
24	High	High	Low	Write 0xD7 to set freq.	0x55	0xAB	0xAA
25	High	High	Float	Write 0xD7 to set freq.	0x56	0xAD	0xAC
26	High	High	High	Write 0xD7 to set freq.	0x57	0xAF	0xAE

5.1.1 Internal Oscillator Tuning

The internal oscillator frequency can be tuned by varying the external resistance connected between the OSCTUNE pin and GND. For a nominal 48MHz, use the resistor value listed in the electrical specification table (12.7kΩ).

See Figure 18 or Table 3 to calculate the ideal OSCTUNE resistor for a particular internal oscillator frequency.

Table 3. OSCTUNE Resistor and Nominal Frequency

OSCTUNE Resistor (kΩ)	Oscillator Frequency (MHz)	Tuning Range (%)
8.2	52.8	110
10	50.4	105
12.7	48	100
17.8	45.6	95
26.7	43.6	91

Refer to Figure 15, Figure 16, or Figure 17 to estimate the variation of the oscillator across temperature. Performance with any PVIN greater than 3.5V is expected to match the PVIN = 18V performance due to the VCC regulator.

5.1.2 Leader and Follower Core Oscillator Configurations

The ISL74420M core clock (Core_CLK) passes into the frequency dividers. It can be sourced by the CLKIN pin or the internal oscillator. The state of the MASTER pin or the MISC_CTRL register controls whether the external CLKIN signal or the internal oscillator is used as the core clock.

In Follower Mode (MASTER pin = GND), the external CLKIN pin is enabled and is compatible with 3.3V CMOS clocks from 0Hz to 50MHz. The internal oscillator is disabled. This mode is commonly used when the CLKIN is sourced from another ISL74420M, a CMOS output crystal oscillator, an FPGA, or a microcontroller.

In Leader Mode (MASTER pin = VCC), both the external CLKIN pin and the internal oscillator are enabled. A Toggle Detection block decides which source drives the Core_CLK signal. If no active signal is present on the

CLKIN pin (CLKIN pin = GND), the internal oscillator drives the core clock. If the CLKIN pin receives a 35-50MHz clock with 40-60% duty cycle, that external clock drives the core clock. CLKIN signals outside of those specifications can cause unpredictable part operation, so they should be avoided. The external clock does not need to be specifically higher or lower than the internal oscillator, but it should be near the same frequency, so the output clocks do not experience substantial frequency changes between the two clock sources. Leader mode is commonly used in standalone operation without any CLKIN. It is also commonly used when the internal oscillator is required to start the system before the external clock is available or when the external clock is unreliable, so the internal oscillator is a failsafe.

When switching between the external clock and internal oscillator in Leader mode, it takes several core clock cycles to transition. This generally does not disrupt the output clocks if they are set to lower frequencies like those relevant to switching power converters.

5.1.3 CLKOUT Configuration Scenarios

The ISL74420M supports a wide variety of frequency configurations, but there are certain rules that must be followed. When the required output frequencies are selected, consider which of the following Scenarios matches the configuration. Then, ensure that the rules are followed for that scenario.

- Scenario 1 – All four outputs are at the same frequency
  - The phase configurations for each of the four output clocks are user configurable.
- Scenario 2 – Three outputs have the same frequency, 1 output at a different frequency
  - The three outputs with the same frequency must be on outputs CLKOUT0, CLKOUT1, and CLKOUT2.
  - The phase configurations for CLKOUT0, 1, and 2 are user configurable.
  - The different frequency must be on CLKOUT3.
  - The phase configuration for CLKOUT3 is ignored and defaults to 0°.
- Scenario 3 – Two outputs have the same frequency, the other two outputs are at a different but same frequency (such as, two outputs at 500kHz, two other outputs at 333kHz)
  - One pair of same frequencies must be on CLKOUT0 and CLKOUT1.
  - The other pair of frequencies must be on CLKOUT2 and CLKOUT3.
  - The phase relationship of CLKOUT0 and CLKOUT1 is user configurable.
  - The phase relationship of CLKOUT2 and CLKOUT3 is user configurable.
  - The phase relationship between outputs of different frequencies (such as, CLKOUT0 and CLKOUT3) is the result of frequencies selected.
- Scenario 4 – Two outputs have the same frequency, the other two outputs are at two different frequencies (there are three total different frequencies output)
  - The pair of same frequencies must be on CLKOUT0 and CLKOUT1.
  - The phase configurations for CLKOUT0 and CLKOUT1 are selectable.
  - The two different frequencies must be on CLKOUT2 and CLKOUT3
  - The phase configuration for CLKOUT2 and CLKOUT3 are ignored and default to 0°.
- Scenario 5 – All four outputs are at different frequencies
  - The frequencies can be in any order on any CLKOUTx channel.
  - The phase configuration for all CLKOUTx is ignored and defaults to 0°.

5.2 Phase Selection

Table 4 shows the different phase selection options. *Note*: Not every phase option is supported by every frequency option. Frequency options 0, 1, 2, and 3 each have a different reduced set of allowed phase selections. Frequency options 4-13 support all phase selections. The affected CLKOUT defaults to 0° if an unsupported phase delay is selected.

Table 4. Phase Selection

PHASE Option # (Hex)	CHx_PH[2]	CHx_PH[1]	CHx_PH[0]	Phase Selection (Degrees)	Frequency Selections that Support this Phase
0 (0x00)	Low	Low	Low	0	0-13 (all)
1 (0x01)	Low	Low	Float	15	4-13
2 (0x02)	Low	Low	High	30	4-13
3 (0x03)	Low	Float	Low	45	4-13
4 (0x04)	Low	Float	Float	60	3-13
5 (0x05)	Low	Float	High	75	4-13
6 (0x06)	Low	High	Low	90	2, 4-13
7 (0x07)	Low	High	Float	105	4-13
8 (0x08)	Low	High	High	120	3-13
9 (0x09)	Float	Low	Low	135	4-13
10 (0x0a)	Float	Low	Float	150	4-13
11 (0x0b)	Float	Low	High	165	4-13
12 (0x0c)	Float	Float	Low	180	1-13
13 (0x0d)	Float	Float	Float	195	4-13
14 (0x0e)	Float	Float	High	210	4-13
15 (0x0f)	Float	High	Low	225	4-13
16 (0x10)	Float	High	Float	240	3-13
17 (0x11)	Float	High	High	255	4-13
18 (0x12)	High	Low	Low	270	2, 4-13
19 (0x13)	High	Low	Float	285	4-13
20 (0x14)	High	Low	High	300	3-13
21 (0x15)	High	Float	Low	315	4-13
22 (0x16)	High	Float	Float	330	4-13
23 (0x17)	High	Float	High	345	4-13

5.3 I²C/SMBus Communication Device Registers

Table 5. I²C/SMBus Register Addresses and Descriptions

Command Code	Command Name	Comments
0xD0	STROBE_WR	A write of 1 to this register signals that the configuration using the I²C/SMBus interface is complete.
0xD1	OUT0_FREQ	Selects the output clock frequency for CLKOUT0.
0xD2	OUT0_PH	Selects the phase for CLKOUT0.
0xD3	OUT1_FREQ	Selects the output clock frequency for CLKOUT1.
0xD4	OUT1_PH	Selects the phase for CLKOUT1.
0xD5	OUT2_FREQ	Selects the output clock frequency for CLKOUT2
0xD6	OUT2_PH	Selects the phase for CLKOUT2.
0xD7	OUT3_FREQ	Selects the output clock frequency for CLKOUT3
0xD8	OUT3_PH	Selects the phase for CLKOUT3.
0xD9	MISC_CTRL	Sets the MASTER Pin Leader/Follower mode and Prescale setting

At startup, the ISL74420M reads its Frequency and Phase selection pins and populates its registers with the pin-selected options. The registers can be read to confirm that the pins were set correctly.

If the CH3 Frequency pins are configured for option 0 through 13, its register is populated with the pin-selected value and the STROBE_WR register is ignored. If the CH3 Frequency pins are configured for option 19 through 26, the OUT3_FREQ must be written with the required setting. In this mode, the part does not release the READY pin or allow outputs until a 1 is written to the STROBE_WR register.

STROBE_WR is not a lockout register. Therefore, it is possible to write new values at any point after startup. OUTEN should be lowered externally while writing any registers and should remain low for 20µs after the final I^2C/SMBus message to ensure reliable operation. The registers can be read back at any time with no disruption to the output clocks.

5.3.1 MISC_CTRL Register

Write the values to the MISC_CTRL register to select the corresponding operational mode.

When transitioning between Leader and Follower modes with the MISC_CTRL register, the internal oscillator requires some time to transition. Keep OUTEN low for 1ms after writing the MISC_CTRL register.

Table 6. MISC_CTRL Register

Register Value	Binary	Leader/Follower Mode	PRESCL Mode
8 (0x08)	1000	Follower	Divide-by-2 (PRESCL low)
9 (0x09)	1001	Follower	Divide-by-4 (PRESCL floating)
10 (0x0a)	1010	Follower	Divide-by-8 (PRESCL high)
11 (0x0b)	1011	Not supported	Not supported
12 (0x0c)	1100	Leader	Divide-by-2 (PRESCL low)
13 (0x0d)	1101	Leader	Divide-by-4 (PRESCL floating)
14 (0x0e)	1110	Leader	Divide-by-8 (PRESCL high)
15 (0x0f)	1111	Not supported	Not supported

5.3.2 I^2C/SMBus Communication Device Registers Access Support Tools

For interface control of the device registers, Renesas evaluation and demonstration boards provide connector access to the SCL / SDA communications signals. Ordering information for these boards are on the ISL74420M product page. There is also a USB Windows compatible HID hardware device that can be purchased. This USB HID device can be used with user supplied general purpose I^2C/SMBus control software. In addition, Renesas also supplies a software GUI specific to ISL74420M device. The ISL74420M product page provides a link for a Windows compatible installer of this GUI which is available for download.

5.4 OUTEN and READY

The OUTEN pin is an input that can be controlled externally to enable and disable the clock outputs. This also allows the synchronization of multi-phase clocks on different ISL74420M.

READY is an open-drain output that is released when the ISL74420M is ready to start providing clocks.

If CH3_FREQx is set to option 0 -13:

- In Leader mode, READY is released after the configuration pins are checked and the internal oscillator is running.
- In Follower mode, READY is released after the configuration pins are checked and the part is ready to buffer or divide clocks.

If CH3_FREQx is set to option 19 - 26:

- In Leader mode, READY is released after the configuration pins are checked, the internal oscillator is running, and the STROBE_WR register is written to a 1.

- In Follower mode, READY is released after the configuration pins are checked, the part is ready to buffer or divide clocks, and the STROBE_WR register is written to a 1.

5.4.1 Leader and Follower for More than Four Clocks

READY and OUTEN can be used together to synchronize the phase relationships of multiple ISL74420M as shown in Figure 3. All of the follower ISL74420Ms should have their READY and OUTEN pins tied together to a common bus. Tie the follower OUTEN to its VCC or controlled externally. Tie the leader READY pin to the common OUTEN/READY bus.

When first turned on, the leader ISL74420M starts up normally and begins producing clocks.

5.5 Clock Output Frequency Accuracy

The accuracy of the nominal 48MHz internal oscillator over supply voltage, temperature, radiation, and OSCTUNE resistor range is -5.7%/+7.3%. This accuracy translates to the clock outputs across the divided down frequencies. For example, when using the ISL74420M as a 500kHz clock signal to synchronize to DC/DC Switching Regulators, the 500kHz clock is -5.7%/+7.3% accurate.

6. I²C/SMBus Serial Interface

6.1 I²C/SMBus SDA and SCL Pull Up Resistors

The SDA and SCL pull up resistors must be connected to the ISL74420M VCC pin or a different voltage supply that is equal to or less than the VCC voltage at all times.

While the SMBus/I²C Specification allows these pins to be pulled to a supply bus separate from the power supply of the devices on the bus, ISL74420M has the restrictions described above.

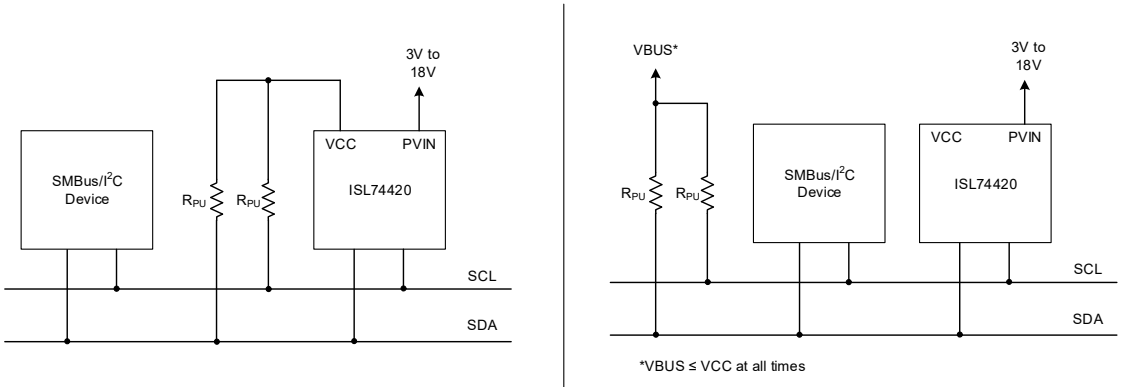


Figure 19. Allowed I²C/SMBus Pull Up Resistor Connection

6.2 I²C/SMBus Protocol Overview

The ISL74420M supports an I²C/SMBus bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a controller and the device being controlled is the target. The controller always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the ISL74420M operates as a target device in all applications. The ISL74420M operates as connections to the bus are made using the open-drain I/O lines SDA and SCL.

All communication over the I²C/SMBus interface is conducted by sending the MSB of each byte of data first.

6.3 I²C/SMBus Protocol Conventions

Data states on the SDA line must change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (see Figure 20). On ISL74420M power-up, the SDA pin is in the input mode.

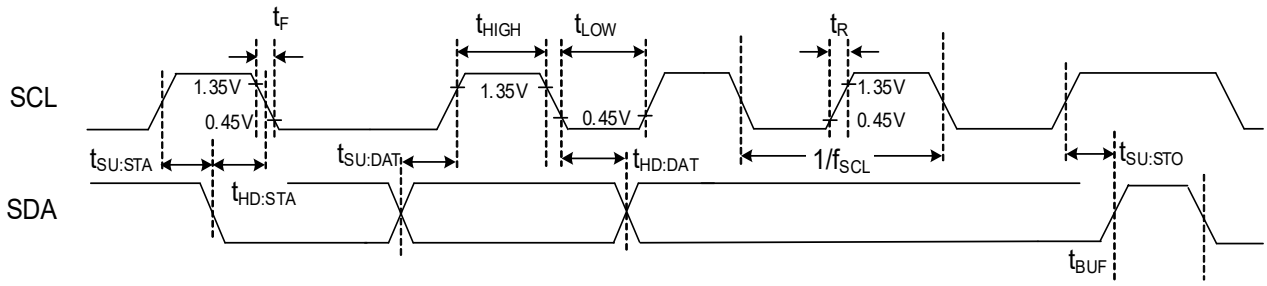


Figure 20. Valid Data Changes, START and STOP Conditions

All I²C/SMBus interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The ISL74420M continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (see Figure 20). A START condition is ignored during the power-up of the device.

All I²C/SMBus interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH (see Figure 20). A STOP condition at the end of a read operation, or at the end of a write operation places the device in its standby mode.

An ACK, Acknowledge, is a software convention used to indicate a successful data transfer. The transmitting device, either controller or target, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data (see Figure 21).

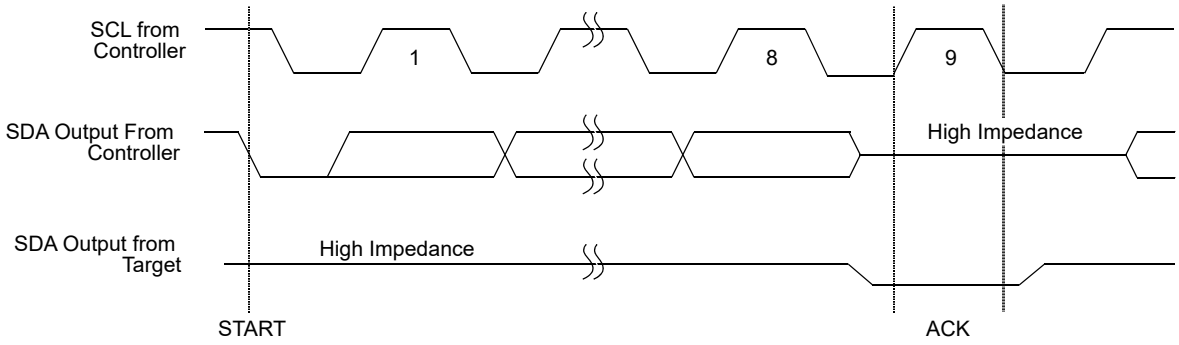


Figure 21. Acknowledge Response from Receiver

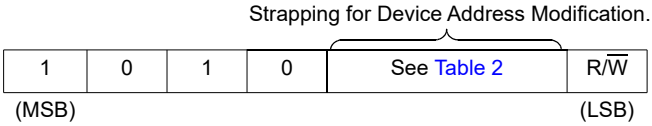
The ISL74420M responds with an ACK after recognition of a START condition followed by a valid Identification Byte, and once again after successful receipt of an Address Byte. The ISL74420M also responds with an ACK after receiving a Data Byte of a write operation. The controller must respond with an ACK after receiving a Data Byte of a read operation.

6.4 I²C/SMBus Target Device Addressing

Following a start condition, the controller must output a Target Device Address Byte. A valid Target Device Address Byte contains 1010 as the four MSBs and the following three bits matching the logic values present at CH3 input strapping (see Table 2). The LSB is the Read/$\overline{\text{Write}}$ bit. Its value is 1 for a Read operation, and 0 for a Write operation (see Table 7 and Figure 22).

After loading the entire Target Device Address Byte from the SDA bus, the ISL74420M compares the device identifier and device select bits. Upon a correct compare, the device outputs an acknowledge on the SDA line.

Table 7. Target Device Address Byte Format



6.5 I²C/SMBus Single Byte Write Operation

A Write operation requires a START condition, followed by a valid Target Device Address Byte, a valid Register Address Byte, a Data Byte, and a STOP condition. After each of the three bytes, the ISL74420M responds with an ACK.

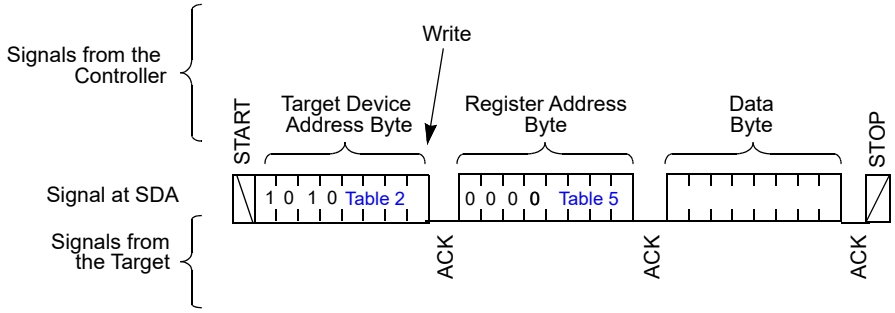


Figure 22. Byte Write Sequence

6.6 I²C/SMBus Single Byte Read Operation

A Read operation consist of a three byte instruction followed by one Data Byte (See Figure 23). The controller initiates the operation issuing the following sequence: a START, the Target Device Address Byte with the R/$\overline{W}$ bit set to 0, an Register Address Byte, a second START, and a second Target Device Address Byte with the R/$\overline{W}$ bit set to 1. After each of the three bytes, the ISL74420M responds with an ACK. The controller terminates the read operation (issuing a $\overline{ACK}$ and a STOP condition).

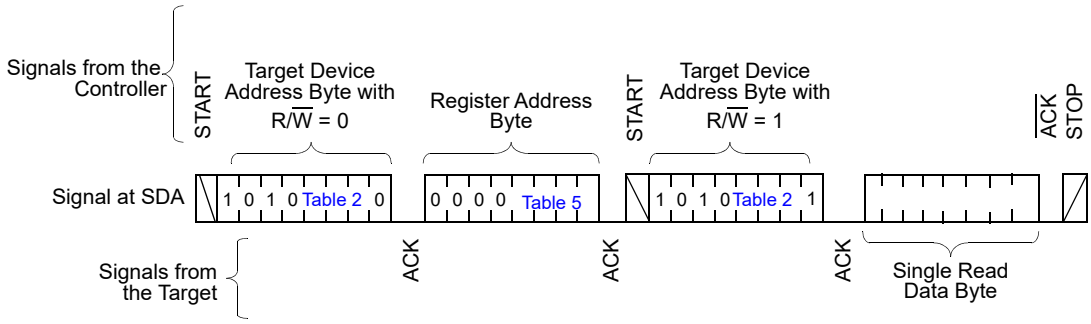


Figure 23. Single Byte Read Sequence

7. Application Information

7.1 Termination

CLKOUT and CLKIN signals may benefit from controlled impedance routing and termination to maintain clean signals over large distances. Refer to the *Termination Options for High-Speed LVCMOS Driver Clock Drivers* application note for termination recommendations.

Consider the ISL74420M VCC current limit, VOH level, and VOL level if adding a termination load resistor.

7.2 Current Consumption and Power Dissipation

The method used to estimate the current consumption and power dissipation of the ISL74420M varies depending on the PVIN, VCC, VCCEXT, and CLKOUT loading.

7.2.1 PVIN Current when VCCEXT is Tied to VCC

Estimating the current consumption and power dissipation of the ISL74420M can be simplified if VCCEXT is tied to VCC and the selected configuration is similar to one of the configurations listed in the Electrical Specifications table as I_{PVIN_OPER} configurations 1 through 4. Configurations 1, 2, and 3 represent the worst case PVIN current consumption in the three different operational modes. Renesas recommends using one of these three specification limits for the current and power budget.

Multiply the PVIN current consumption by the PVIN voltage to estimate the power dissipation of the ISL74420M.

7.2.2 PVIN Current when VCCEXT is Separate

Estimating current consumption becomes more complex when VCCEXT is supplied from a separate power supply. For this configuration, Renesas recommends using I_{PVIN_OPER4} as a starting point for the PVIN current. Although this configuration includes VCCEXT current, that current is small at 1MHz so the current consumption is still close. Subtract 6mA if operating in Follower mode and add 3mA if operating in Leader mode with a CLKIN signal.

Multiply the PVIN current and the PVIN voltage to estimate this portion of the power dissipation of the ISL74420M.

7.2.3 VCCEXT Current

Estimating VCCEXT supply current can be done two ways. The worst-case method is to use the specification I_{VCCEXT_MAX}. The actual VCCEXT supply current is not higher than that unless the CLKOUT pins have significant loads. When more granular current and power estimation is required, refer to Figure 7 to estimate the VCCEXT supply current. Look up the application's highest CLKOUT frequency on the X-axis, and use the measured VCCEXT current. This data was collected with all four outputs at the same frequency and VCCEXT = 5.5V, so the real-world consumption should be lower if the configuration has a combination of different CLKOUT frequencies.

Multiply the VCCEXT current and the VCCEXT voltage to estimate this portion of the power dissipation of the ISL74420M.

7.2.4 Additional Loading of the CLKOUT Pins

The specification table and performance graphs assume a small 12pF capacitive load on each CLKOUT pin. This is similar to the load that is imposed by a compact PCB layout and the SYNC or CLKIN of a typical IC. Additional loading beyond this causes additional supply current and should be considered.

For a capacitive load, use Equation 2 to calculate the average additional supply current for each CLKOUT where V_{VCCEXT} is the VCCEXT voltage, C_{LOADx} is the additional capacitive load on that CLKOUT pin, and $f_{CLKOUTx}$ is the frequency of that CLKOUT pin.

(EQ. 2) $$I_{load\_cap\_CLKOUTx} = V_{VCCEXT} \times C_{Loadx} \times f_{CLKOUTx}$$

Use Equation 3 to estimate the power dissipation due to additional capacitive loading where V_{src} is either PVIN (for applications where VCC is providing VCCEXT) or VCCEXT (when a separate VCCEXT is provided).

(EQ. 3) $$P_{load\_cap} = V_{src} \times \left(\sum_{X=0}^{3} I_{load\_cap\_CLKOUTx} \right)$$

Use Equation 4 to calculate the additional current consumption due to resistive loading of the CLKOUT pins that assumes a 50% duty cycle on any CLKOUT.

(EQ. 4) $$I_{load\_res\_CLKOUTx} = \frac{0.5 \times V_{VCCEXT}}{R_{LOADx}}$$

The additional power dissipation due to resistive loading of CLKOUT can generally be disregarded when a separate VCCEXT is supplied because the voltage drop between VCCEXT and CLKOUTx is low. However, the power dissipation can be significant if VCCEXT is supplied by VCC and the PVIN voltage is high.

(EQ. 5) $$P_{load\_res\_LDO} = (V_{PVIN} - CLKOUTx_{VOH}) \times \left(\sum_{X=0}^{3} I_{load\_res\_CLKOUTx} \right)$$

7.3 Leader and Follower Configuration

When driving ISL74420M as followers, there are often multiple options for the CLKIN frequency to provide the required output clock frequency. One way to determine the necessary input clock is to study Table 1. If all necessary frequencies occur in the PRESCL Float column, the ISL74420M can produce them with a 24MHz input clock. If all necessary frequencies occur in the PRESCL High column, it can produce them with a 12MHz input clock. Lower CLKIN frequencies are more resilient to signal degradation and can lower the power consumption of the ISL74420M.

In the example below, the system requires 2MHz 0°, 2MHz 180°, 1MHz, and 500kHz clock signals. All four of these are available in the PRESCL Low and PRESCL Float columns of the Table 8. 2MHz is not available in the PRESCL High column. Therefore, a 24MHz CLKIN signal can be used by setting the part up to divide-by-12, -24, and -48.

Table 8. Example 1

CLKOUT Channel	Required CLKOUT Frequency	FREQ option with 48MHz CLKIN			FREQ option with 24MHz CLKIN
		PRESCL Low	PRESCL Float	PRESCL High	PRESCL Low
0	2MHz 0°	4	3	x	3
1	2MHz 180°	4	3	x	3
2	1MHz	5	4	3	4
3	500kHz	6	5	4	5

In the next example, all four CLKOUT channels are set to 1MHz with 90° phase separation options. This can be produced by a ISL74420M set to option 2 (divide-by-4) with only a 4MHz input clock.

Table 9. Example 2

CLKOUT Channel	Required CLKOUT Frequency	FREQ Option with 48MHz CLKIN			FREQ Option with 4MHz CLKIN
		PRESCL Low	PRESCL Float	PRESCL High	PRESCL Low
0	1MHz 0°	5	4	3	2
1	1MHz 90°	5	4	x (phase)	2
2	1MHz 180°	5	4	3	2
3	1MHz 270°	5	4	x (phase)	2

7.4 Power Supply Biasing

The ISL74420M is biased from the PVIN pin and can accept a supply voltage of 3.0V to 18V. Although, the ISL74420M is fully specified down to 3.0V, providing a PVIN higher than 3.5V guarantees the best oscillator frequency performance across all operating conditions. Renesas recommends placing a local decoupling ceramic

capacitor of 0.1µF or larger near the PVIN and GND pins for high frequency filtering. The PVIN pin supplies power to the internal 3.3V LDO connected to the VCC pin. Renesas recommends placing a local 1µF ceramic capacitor near the VCC and GND pins. The VCC LDO is enabled when PVIN is above the UVLO threshold (2.91V typical).

7.4.1 3.3V Single Supply Applications

If only a 3.3V power supply is available, PVIN, VCC, and VCCEXT pins can all be tied together and driven from the same supply. This bypasses the internal LDO voltage regulation and its current limit.

7.4.2 Startup Sequence

After proper biasing of PVIN, the VCC LDO starts up and the ISL74420M runs through its startup routine. This routine varies based on the part configuration as described in OUTEN and READY. After the startup routine is complete, OUTEN is high and VCCEXT has an appropriate power supply connected, the ISL74420M begins to drive the CLKOUTx pins. The typical delay time from power-up to driving output clocks in non-I^2C/SMBus operation is 2.2ms.

7.5 VCCEXT - Clock Output Power Stage

The VCCEXT is the power supply for the CLKOUTx output drivers and can accept a supply voltage of 3.0V to 5.5V. The VCCEXT can be biased from the 3.3V LDO by connecting the VCC and VCCEXT pins together for 3.3V Clock output signals. The 3.3V VCC LDO current limit (75mA minimum) provides sufficient margin for driving the highest output frequency on the clock outputs. If VCCEXT is connected to an external supply, Renesas recommends placing a 1µF ceramic capacitor near the VCCEXT and GND pins. The CLKOUTx signals drive to a high level defined by the VCCEXT voltage. There is no power sequencing requirement for the PVIN and VCCEXT supplies.

7.6 Layout Recommendations

- Place the PVIN capacitor as close as possible to the PVIN pin.
- Place the VCC capacitor as close as possible to the VCC pin.
- Place the VCCEXT capacitor as close as possible to the VCCEXT pin.
- Place tightly coupled termination on CLKIN if the clock source requires it.
- Ensure that all CLKOUTx (0-3) traces are routed away from sensitive nets.
- Ensure that all CLKOUTx (0-3) traces are routed with equal length to achieve optimal phase matching between outputs.
- Place the OSCTUNE resistor as close as possible to the OSCTUNE pin.
- Ensure a good ground plane.
- Refer to the ISL74420M evaluation and demonstration boards for example PCB layouts.

When incorporating the ISL74420M into a system there are a few guidelines that can ensure optimal electrical and noise performance. Analog circuits can conduct noise through paths that connect it to the outside world. The most sensitive nets to the ISL74420M are VCC and OSCTUNE. Ensure these are kept away from known system noise sources.

When creating a new PCB design, Renesas recommends decoupling the power supply pins (PVIN, VCC and VCCEXT) for power supply filtering. If the traces to the supply lines are long, Renesas recommends using a larger 1µF capacitor at the point of entry for the supply and a smaller capacitor, like a 0.1µF, close to the part to reduce high-frequency perturbations. CLKOUTx (0-3) routing is especially important. Consider placing series termination resistors on the four clock outputs. Renesas recommends reviewing best practice documentation related to clock routing and termination options, see *Renesas Output Terminations Quick Guide*. Locate series Termination resistors or placeholders as close as possible to the driving device pin.

8. Radiation Tolerance

The ISL74420M is a radiation tolerant device for commercial space applications, Low Earth Orbit (LEO) applications, high altitude avionics, launch vehicles, and other harsh environments. This device's response to Total Ionizing Dose (TID) radiation effects and Single Event Effects (SEE) has been measured, characterized, and reported in the proceeding sections. The ISL74420M30NZ is radiation lot acceptance tested (RLAT) to 30krad(Si), and the ISL74420M50NZ is RLAT to 50krad(Si). The SEE characterized performance is not guaranteed.

8.1 Total Ionizing Dose (TID) Testing

8.1.1 Introduction

Total dose testing of the ISL74420M proceeded in accordance with the guidelines of MIL-STD-883 Test Method 1019. The experimental matrix consisted of 14 samples irradiated under bias, and 9 samples irradiated with all pins grounded (unbiased). Three control units were used. Figure 24 shows the bias configuration.

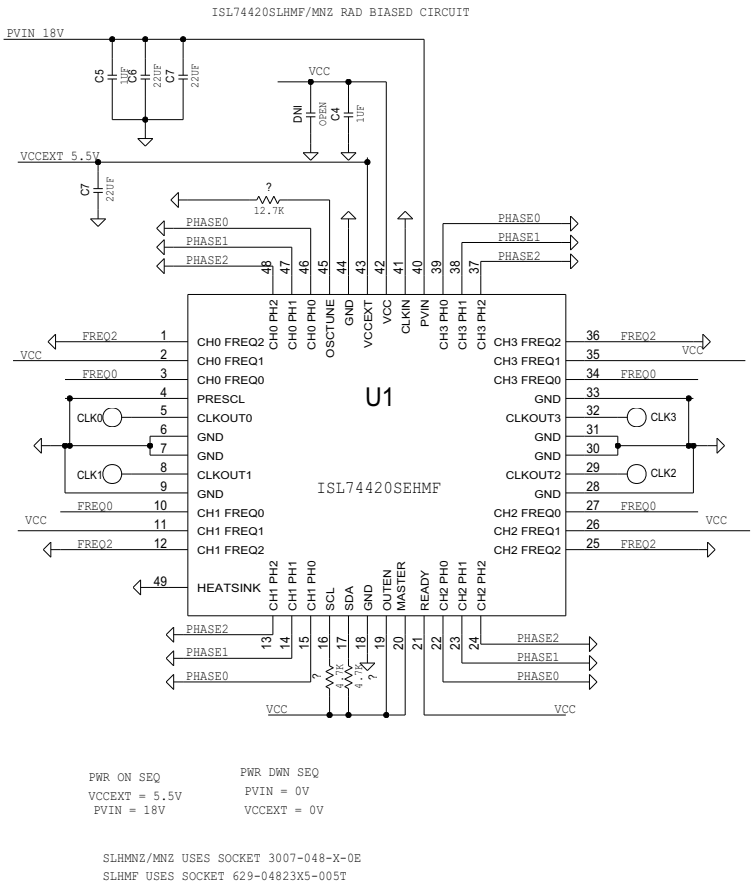


Figure 24. Irradiation Bias Configuration for the ISL74420M

Samples of the ISL74420M were drawn from wafer lot F6X588 and were packaged in the production 48-lead TQFP-EP. The samples were screened to datasheet limits at room temperature only before irradiation.

Total dose irradiations were performed using a Hopewell Designs N40 panoramic vault-type low dose rate ^{60}Co irradiator located in the Renesas Palm Bay, Florida Facility. The dose rate was 10mrad(Si)/s. PbAl spectrum hardening filters were used to shield the test board and devices under test against low energy secondary gamma radiation.

Down-points for the testing were 0krad(Si), 10krad(Si), 30krad(Si), and 50krad(Si).All electrical testing was performed outside the irradiator using production Automated Test Equipment (ATE) with data logging of all parameters at each down-point. All down-point electrical testing was performed at room temperature.

8.1.2 Results

Table 10 summarizes the attributes data.

Table 10. ISL74420M Total Dose Test Attributes Data

Dose Rate mrad(Si)/s	Bias	Sample Size	Downpoints	Pass[1]	Fail
10	Biased (Figure 24)	14	Pre-Rad	14	0
			10krad(Si)	14	0
			30krad(Si)	14	0
			50krad(Si)	14	0
10	Grounded	9	Pre-Rad	9	0
			10krad(Si)	9	0
			30krad(Si)	9	0
			50krad(Si)	9	0

1. A Pass indicates a device that passes all the datasheet specification limits.

The plots in Figure 25 through Figure 36 show data for key parameters at all downpoints. The plots show the sample size average as a function of the total dose for each irradiation condition. The error bars, if visible, indicate the minimum and maximum measured values. Some of the plotted parameters are denoted averages. This indicates that the plotted parameter is the average over all the channels. The error bars on these plots, if visible, indicate the minimum and maximum measured values across all channels. All parts showed excellent stability over irradiation.

8.1.3 Typical Radiation Performance

Parameters are measured using datasheet test conditions unless otherwise specified.

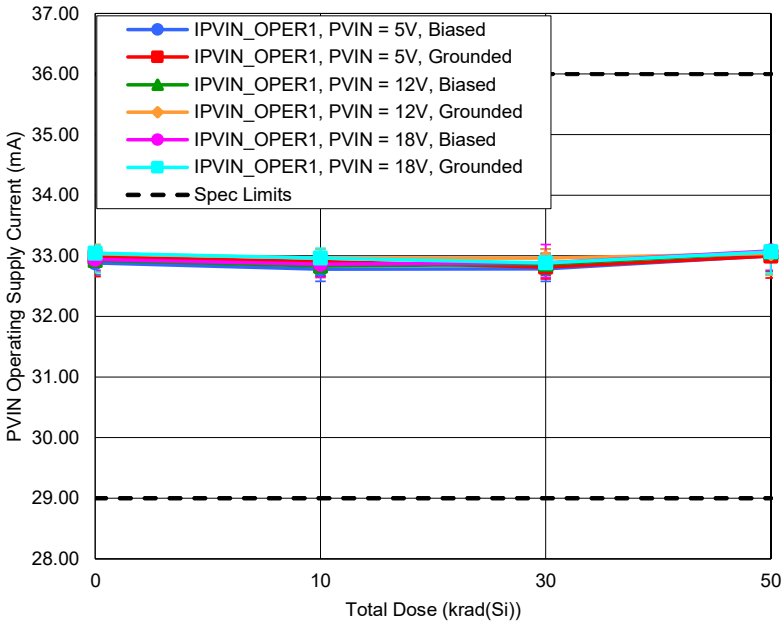


Figure 25. PVIN Operating Supply Current – Leader Mode 48MHz Out vs TID

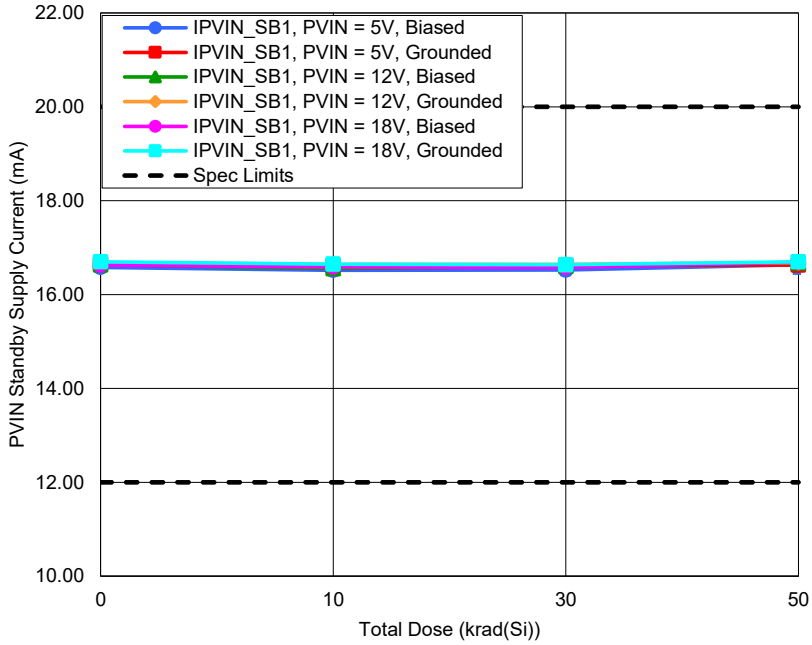


Figure 26. PVIN Standby Leader Mode Supply Current vs TID

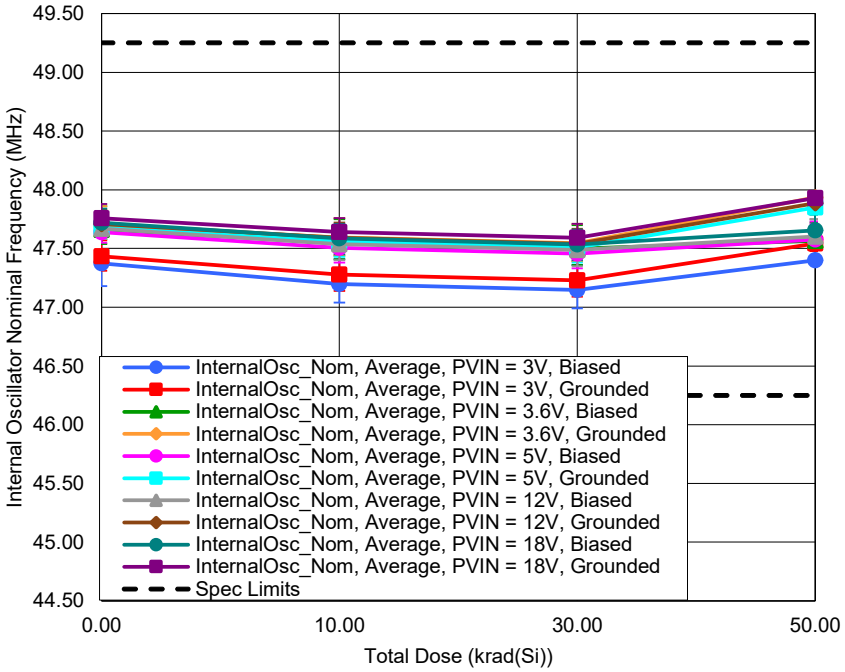


Figure 27. Internal Oscillator Nominal Frequency Averaged over all Channels vs TID

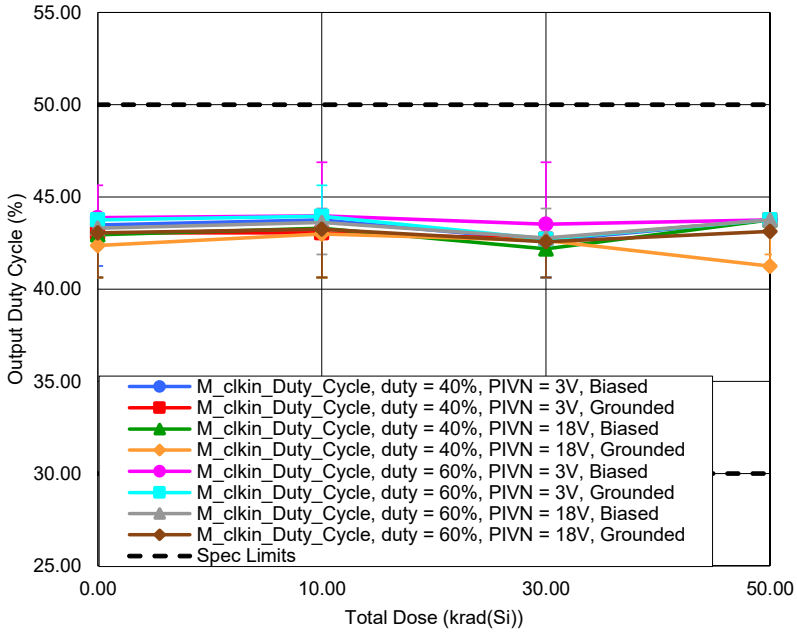


Figure 28. Output Duty Cycle in Leader Mode with CLKIN frequency = 50MHz vs TID

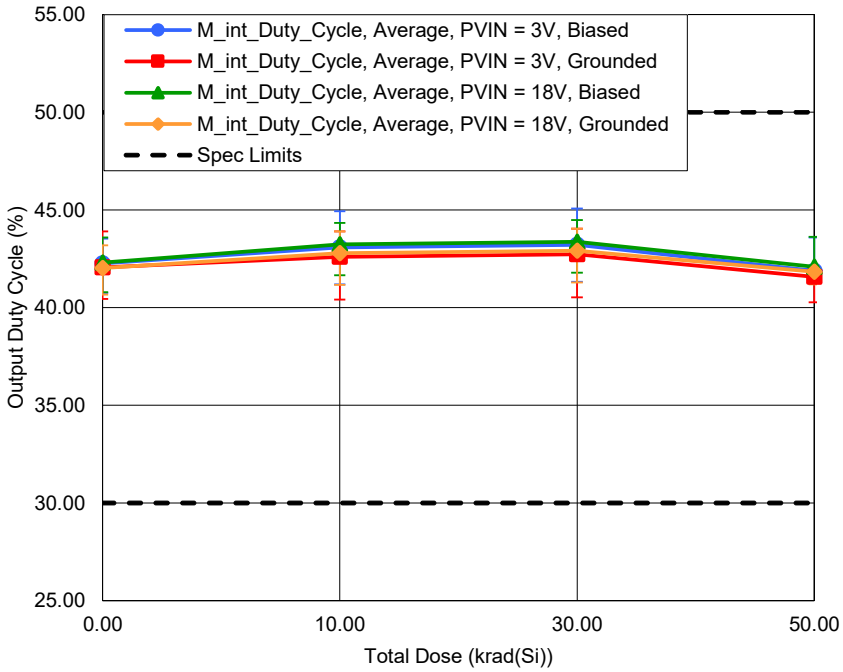


Figure 29. Output Duty Cycle in Leader Mode with Internal Oscillator vs TID

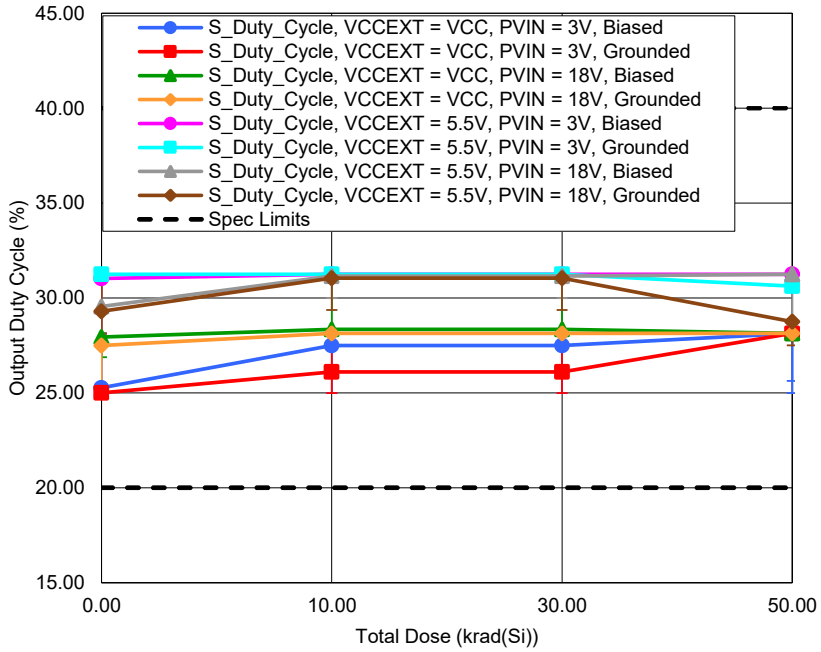


Figure 30. Output Duty Cycle in Follower Mode with CLKIN frequency = 30MHz and duty = 30% vs TID

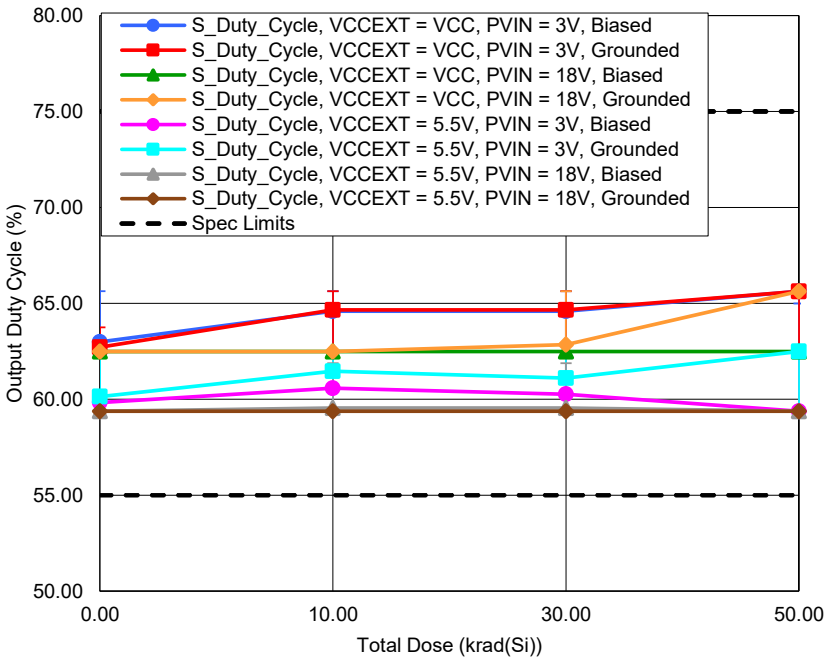


Figure 31. Output Duty Cycle in Follower Mode with CLKINfreq = 30MHz and duty = 65% vs TID

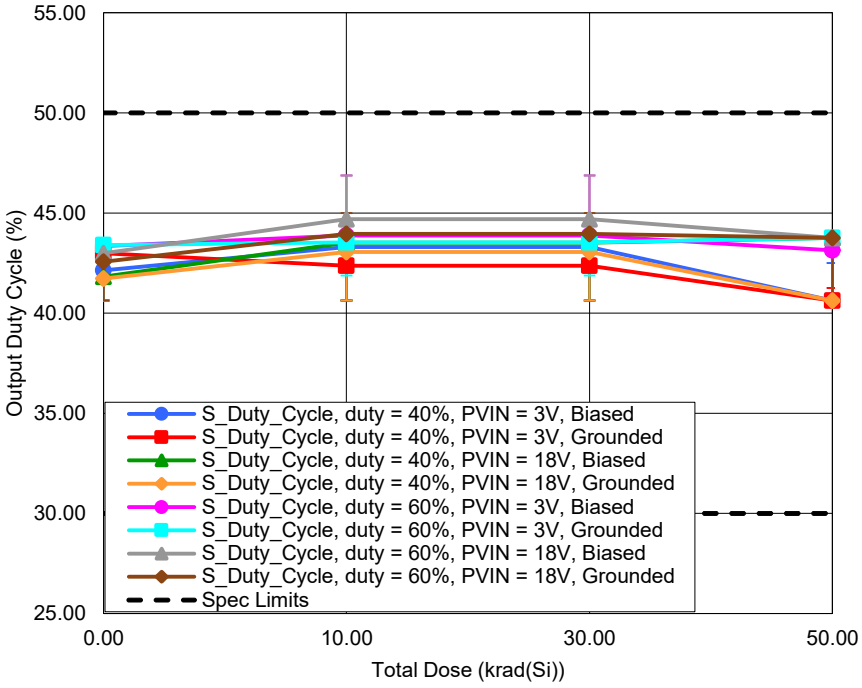


Figure 32. Output Duty Cycle in Follower Mode with CLKINfreq = 50MHz vs TID

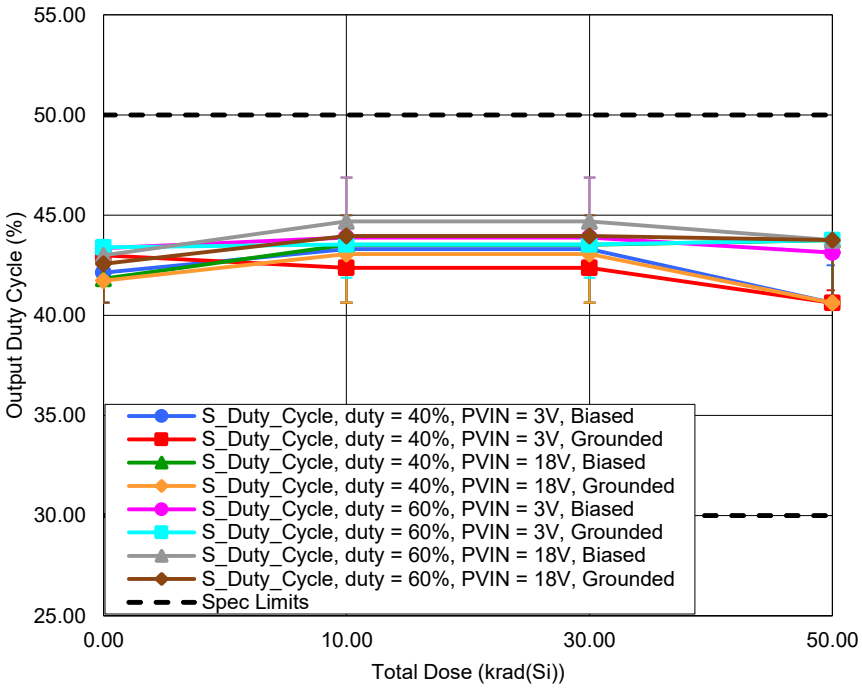


Figure 33. Duty Cycle of a Divided Clock vs TID

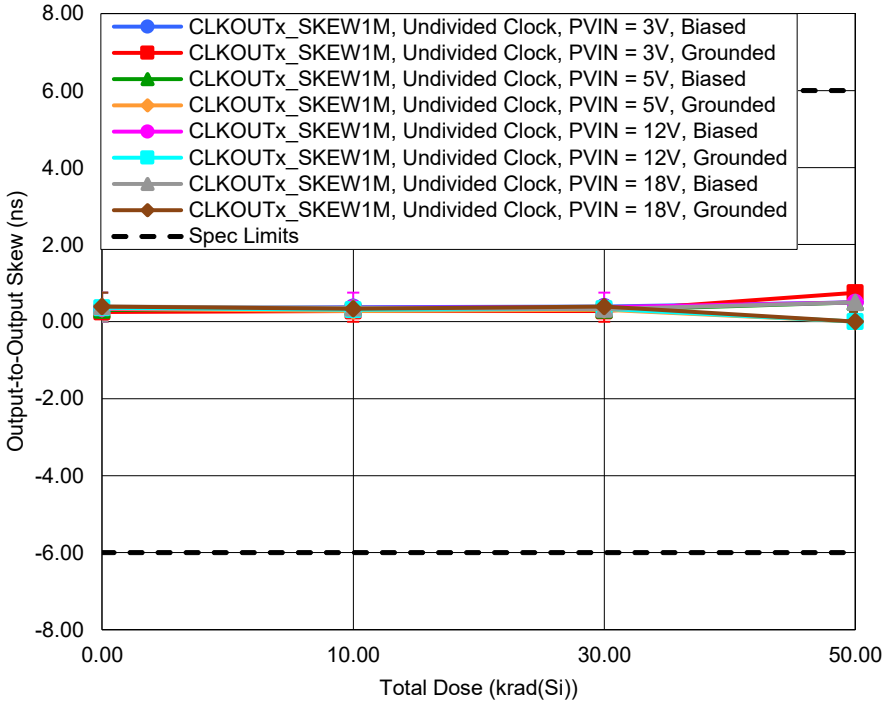


Figure 34. Output-to-Output Skew Between CLKOUTx's with Equal Frequency and Phase and with the Clock Divided vs TID

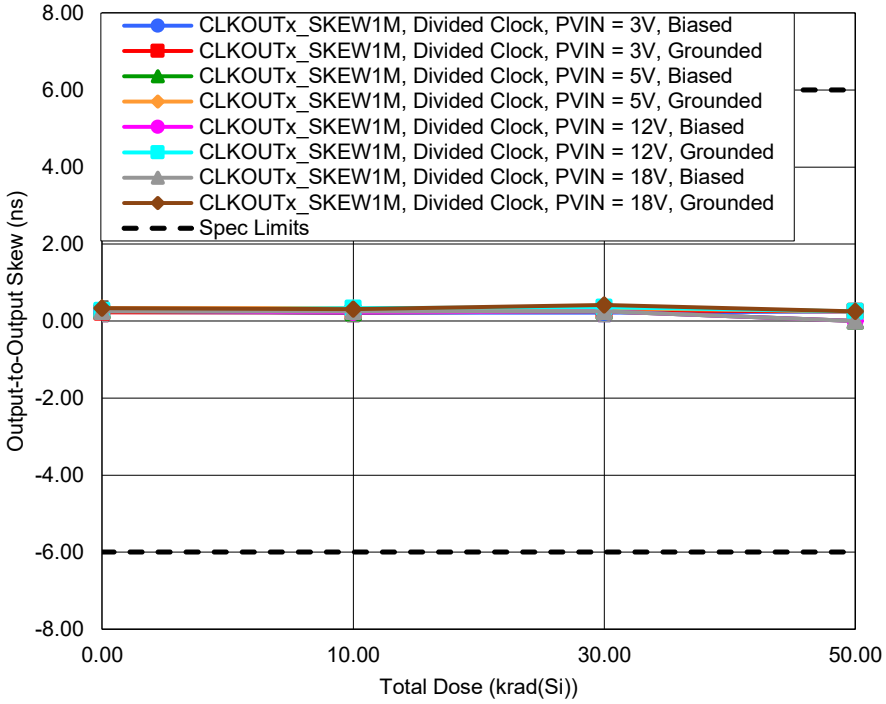


Figure 35. Output-to-Output Skew Between CLKOUTx's with Equal Frequency and Phase and with the Clock Undivided vs TID

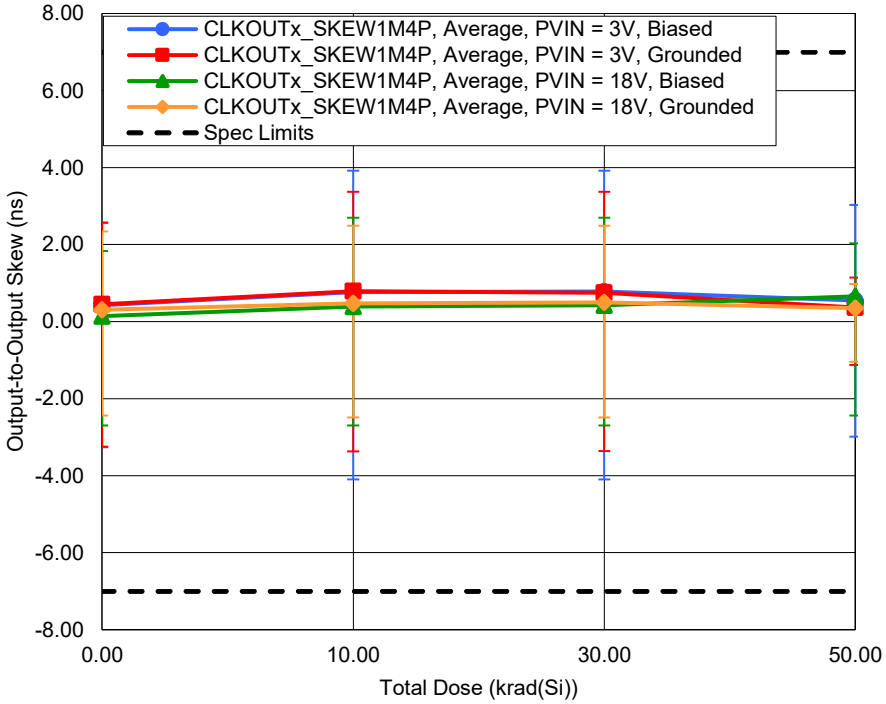


Figure 36. Output-to-Output Skew Between CLKOUTx's with Equal Frequency and Different Phase vs TID

8.1.4 Conclusion

ATE characterization testing showed no rejects to the datasheet limits at all downpoints. Variables data for selected parameters are presented in Figure 25 through Figure 36. Table 11 shows the average of the key parameters with respect to total dose in tabular form. Parameters are measured using datasheet test conditions unless otherwise specified. No differences between biased and unbiased irradiation were noted and the part is not considered bias sensitive.

Table 11. Response of Key Parameters vs TID

Parameter	Symbol	Irradiation Condition	Pre-Rad Value	10krad(Si)	30krad(Si)	50krad(Si)	Unit
PVIN Operating Supply Current – Leader Mode 48MHz out with PVIN = 5V	I_{PVIN_OPER1}	Biased (Figure 24)	32.88	32.78	32.78	33.00	mA
		Grounded	32.98	32.91	32.81	33.00	
		Limit -	29	29	29	29	
		Limit +	36	36	36	36	
PVIN Operating Supply Current – Leader Mode 48MHz out with PVIN = 12V	I_{PVIN_OPER1}	Biased (Figure 24)	32.93	32.83	32.86	33.06	mA
		Grounded	33.03	32.96	32.96	33.04	
		Limit -	29	29	29	29	
		Limit +	36	36	36	36	
PVIN Operating Supply Current – Leader Mode 48MHz out with PVIN = 18V	I_{PVIN_OPER1}	Biased (Figure 24)	32.94	32.86	32.88	33.08	mA
		Grounded	33.04	32.96	32.88	33.07	
		Limit -	29	29	29	29	
		Limit +	36	36	36	36	
PVIN Standby Leader Mode Supply Current with PVIN = 5V	I_{PVIN_SB1}	Biased (Figure 24)	16.58	16.52	16.52	16.63	mA
		Grounded	16.65	16.60	16.62	16.63	
		Limit -	12	12	12	12	
		Limit +	20	20	20	20	
PVIN Standby Leader Mode Supply Current with PVIN = 12V	I_{PVIN_SB1}	Biased (Figure 24)	16.64	16.56	16.61	16.68	mA
		Grounded	16.69	16.64	16.64	16.68	
		Limit -	12	12	12	12	
		Limit +	20	20	20	20	
PVIN Standby Leader Mode Supply Current with PVIN = 18V	I_{PVIN_SB1}	Biased (Figure 24)	16.63	16.59	16.58	16.69	mA
		Grounded	16.70	16.65	16.63	16.70	
		Limit -	12	12	12	12	
		Limit +	20	20	20	20	
Internal Oscillator Nominal Frequency Average of all Channels with PVIN = 3V	InternalOsc_Nom	Biased (Figure 24)	47.37	47.20	47.15	47.40	MHz
		Grounded	47.43	47.28	47.23	47.54	
		Limit -	46.25	46.25	46.25	46.25	
		Limit +	49.25	49.25	49.25	49.25	

Table 11. Response of Key Parameters vs TID (Cont.)

Parameter	Symbol	Irradiation Condition	Pre-Rad Value	10krad(Si)	30krad(Si)	50krad(Si)	Unit
Internal Oscillator Nominal Frequency Average of all Channels with PVIN = 3.6V	InternalOsc_Nom	Biased (Figure 24)	47.66	47.55	47.50	47.57	MHz
		Grounded	47.69	47.59	47.54	47.94	
		Limit -	46.25	46.25	46.25	46.25	
		Limit +	49.25	49.25	49.25	49.25	
Internal Oscillator Nominal Frequency Average of all Channels with PVIN = 5V	InternalOsc_Nom	Biased (Figure 24)	47.64	47.51	47.46	47.58	MHz
		Grounded	47.68	47.56	47.51	47.85	
		Limit -	46.25	46.25	46.25	46.25	
		Limit +	49.25	49.25	49.25	49.25	
Internal Oscillator Nominal Frequency Average of all Channels with PVIN = 12V	InternalOsc_Nom	Biased (Figure 24)	47.67	47.54	47.49	47.60	MHz
		Grounded	47.71	47.59	47.54	47.89	
		Limit -	46.25	46.25	46.25	46.25	
		Limit +	49.25	49.25	49.25	49.25	
Internal Oscillator Nominal Frequency Average of all Channels with PVIN = 18V	InternalOsc_Nom	Biased (Figure 24)	47.72	47.59	47.54	47.66	MHz
		Grounded	47.76	47.64	47.59	47.93	
		Limit -	46.25	46.25	46.25	46.25	
		Limit +	49.25	49.25	49.25	49.25	
Output Duty Cycle in Leader Mode with CLKIN with duty = 40% and PVIN = 3V	M_clkin_Duty_cycle	Biased (Figure 24)	43.48	43.75	42.63	43.75	%
		Grounded	43.06	43.06	42.71	43.75	
		Limit -	30	30	30	30	
		Limit +	50	50	50	50	
Output Duty Cycle in Leader Mode with CLKIN with duty = 40% and PVIN = 18V	M_clkin_Duty_cycle	Biased (Figure 24)	42.95	43.30	42.19	43.75	%
		Grounded	42.36	42.99	42.64	41.25	
		Limit -	30	30	30	30	
		Limit +	50	50	50	50	
Output Duty Cycle in Leader Mode with CLKIN with duty = 60% and PVIN = 3V	M_clkin_Duty_cycle	Biased (Figure 24)	43.88	43.97	43.53	43.75	%
		Grounded	43.75	43.96	42.71	43.75	
		Limit -	30	30	30	30	
		Limit +	50	50	50	50	
Output Duty Cycle in Leader Mode with CLKIN with duty = 60% and PVIN = 18V	M_clkin_Duty_cycle	Biased (Figure 24)	43.30	43.62	42.77	43.75	%
		Grounded	43.06	43.26	42.57	43.13	
		Limit -	30	30	30	30	
		Limit +	50	50	50	50	
Output Duty Cycle in Leader Mode with Internal Oscillator Average of all Channels with PVIN = 3V	M_clkin_Duty_cycle	Biased (Figure 24)	42.25	43.08	43.21	41.89	%
		Grounded	42.05	42.61	42.73	41.58	
		Limit -	30	30	30	30	
		Limit +	50	50	50	50	

Table 11. Response of Key Parameters vs TID (Cont.)

Parameter	Symbol	Irradiation Condition	Pre-Rad Value	10krad(Si)	30krad(Si)	50krad(Si)	Unit
Output Duty Cycle in Leader Mode with Internal Oscillator Average of all Channels with PVIN = 18V	M_clkin_Duty_cycle	Biased (Figure 24)	42.31	43.24	43.37	42.09	%
		Grounded	42.03	42.79	42.92	41.84	
		Limit -	30	30	30	30	
		Limit +	50	50	50	50	
Output Duty Cycle in Follower Mode with CLKINfreq = 30MHz, duty = 30%, VCCEXT = VCC, and PVIN = 3V	M_clkin_Duty_cycle	Biased (Figure 24)	25.27	27.50	27.50	28.13	%
		Grounded	25.00	26.11	26.11	28.13	
		Limit -	20	20	20	20	
		Limit +	40	40	40	40	
Output Duty Cycle in Follower Mode with CLKINfreq = 30MHz, duty = 30%, VCCEXT = VCC, and PVIN = 18V	S_Duty_Cycle	Biased (Figure 24)	27.95	28.35	28.35	28.13	%
		Grounded	27.50	28.13	28.13	28.13	
		Limit -	20	20	20	20	
		Limit +	40	40	40	40	
Output Duty Cycle in Follower Mode with CLKINfreq = 30MHz, duty = 30%, VCCEXT = 5.5V, and PVIN = 3V	S_Duty_Cycle	Biased (Figure 24)	31.03	31.25	31.25	31.25	%
		Grounded	31.25	31.25	31.25	30.63	
		Limit -	20	20	20	20	
		Limit +	40	40	40	40	
Output Duty Cycle in Follower Mode with CLKINfreq = 30MHz, duty = 30%, VCCEXT = 5.5V, and PVIN = 18V	S_Duty_Cycle	Biased (Figure 24)	29.55	31.16	31.16	31.25	%
		Grounded	29.31	31.04	31.04	28.75	
		Limit -	20	20	20	20	
		Limit +	40	40	40	40	
Output Duty Cycle in Follower Mode with CLKINfreq = 30MHz, duty = 65%, VCCEXT = VCC, and PVIN = 3V	S_Duty_Cycle	Biased (Figure 24)	62.99	64.60	64.60	65.63	%
		Grounded	62.71	64.65	64.65	65.63	
		Limit -	55	55	55	55	
		Limit +	75	75	75	75	
Output Duty Cycle in Follower Mode with CLKINfreq = 30MHz, duty = 65%, VCCEXT = VCC, and PVIN = 18V	S_Duty_Cycle	Biased (Figure 24)	62.50	62.50	62.50	62.50	%
		Grounded	62.50	62.50	62.85	65.63	
		Limit -	55	55	55	55	
		Limit +	75	75	75	75	
Output Duty Cycle in Follower Mode with CLKINfreq = 30MHz, duty = 65%, VCCEXT = 5.5V, and PVIN = 3V	S_Duty_Cycle	Biased (Figure 24)	59.82	60.58	60.27	59.38	%
		Grounded	60.14	61.46	61.11	62.50	
		Limit -	55	55	55	55	
		Limit +	75	75	75	75	
Output Duty Cycle in Follower Mode with CLKINfreq = 30MHz, duty = 65%, VCCEXT = 5.5V, and PVIN = 18V	S_Duty_Cycle	Biased (Figure 24)	59.38	59.55	59.55	59.38	%
		Grounded	59.38	59.38	59.38	59.38	
		Limit -	55	55	55	55	
		Limit +	75	75	75	75	

Table 11. Response of Key Parameters vs TID (Cont.)

Parameter	Symbol	Irradiation Condition	Pre-Rad Value	10krad(Si)	30krad(Si)	50krad(Si)	Unit
Output Duty Cycle in Follower Mode with CLKINfreq = 50MHz, duty = 40%, VCCEXT = VCC, and PVIN = 3V	S_Duty_Cycle	Biased (Figure 24)	42.14	43.30	43.30	40.63	%
		Grounded	42.99	42.36	42.36	40.63	
		Limit -	30	30	30	30	
		Limit +	50	50	50	50	
Output Duty Cycle in Follower Mode with CLKINfreq = 50MHz, duty = 40%, VCCEXT = VCC, and PVIN = 18V	S_Duty_Cycle	Biased (Figure 24)	41.83	43.53	43.53	43.75	%
		Grounded	41.74	43.06	43.06	40.63	
		Limit -	30	30	30	30	
		Limit +	50	50	50	50	
Output Duty Cycle in Follower Mode with CLKINfreq = 50MHz, duty = 60%, VCCEXT = VCC, and PVIN = 3V	S_Duty_Cycle	Biased (Figure 24)	43.35	43.88	43.88	43.13	%
		Grounded	43.40	43.54	43.54	43.75	
		Limit -	30	30	30	30	
		Limit +	50	50	50	50	
Output Duty Cycle in Follower Mode with CLKINfreq = 50MHz, duty = 60%, VCCEXT = VCC, and PVIN = 18V	S_Duty_Cycle	Biased (Figure 24)	42.99	44.69	44.69	43.75	%
		Grounded	42.57	43.96	43.96	43.75	
		Limit -	30	30	30	30	
		Limit +	50	50	50	50	
Duty Cycle of a Divided Clock with VCCEXT = VCC and PVIN = 3V	div_Duty_Cycle	Biased (Figure 24)	48.29	48.57	48.38	48.55	%
		Grounded	48.26	48.52	48.33	48.40	
		Limit -	47	47	47	47	
		Limit +	50	50	50	50	
Duty Cycle of a Divided Clock with VCCEXT = VCC and PVIN = 18V	div_Duty_Cycle	Biased (Figure 24)	48.22	48.51	48.30	48.57	%
		Grounded	48.18	48.45	48.24	48.21	
		Limit -	47	47	47	47	
		Limit +	50	50	50	50	
Duty Cycle of a Divided Clock with VCCEXT = 5.5V and PVIN = 3V	div_Duty_Cycle	Biased (Figure 24)	48.59	48.86	48.68	48.88	%
		Grounded	48.61	48.86	48.67	48.74	
		Limit -	47	47	47	47	
		Limit +	50	50	50	50	
Duty Cycle of a Divided Clock with VCCEXT = 5.5V and PVIN = 18V	div_Duty_Cycle	Biased (Figure 24)	48.76	49.05	48.83	49.01	%
		Grounded	48.75	49.01	48.79	48.79	
		Limit -	47	47	47	47	
		Limit +	50	50	50	50	
Output-to-Output Skew between CLKOUTx's with Equal Frequency and Phase with the Clock undivided and PVIN = 3V	$CLKOUTx_{SKEW1M}$	Biased (Figure 24)	0.34	0.37	0.39	0.50	ns
		Grounded	0.25	0.28	0.28	0.75	
		Limit -	-6	-6	-6	-6	
		Limit +	6	6	6	6	

Table 11. Response of Key Parameters vs TID (Cont.)

Parameter	Symbol	Irradiation Condition	Pre-Rad Value	10krad(Si)	30krad(Si)	50krad(Si)	Unit
Output-to-Output Skew between CLKOUTx's with Equal Frequency and Phase with the Clock undivided and PVIN = 5V	$CLKOUTx_{SKEW1M}$	Biased (Figure 24)	0.30	0.36	0.30	0.50	ns
		Grounded	0.33	0.28	0.31	0.00	
		Limit -	-6	-6	-6	-6	
		Limit +	6	6	6	6	
Output-to-Output Skew between CLKOUTx's with Equal Frequency and Phase with the Clock undivided and PVIN = 12V	$CLKOUTx_{SKEW1M}$	Biased (Figure 24)	0.34	0.36	0.37	0.50	ns
		Grounded	0.36	0.31	0.33	0.00	
		Limit -	-6	-6	-6	-6	
		Limit +	6	6	6	6	
Output-to-Output Skew between CLKOUTx's with Equal Frequency and Phase with the Clock undivided and PVIN = 18V	$CLKOUTx_{SKEW1M}$	Biased (Figure 24)	0.39	0.36	0.32	0.50	ns
		Grounded	0.39	0.33	0.39	0.00	
		Limit -	-6	-6	-6	-6	
		Limit +	6	6	6	6	
Output-to-Output Skew between CLKOUTx's with Equal Frequency and Phase with the Clock divided and PVIN = 3V	$CLKOUTx_{SKEW1M}$	Biased (Figure 24)	0.23	0.21	0.21	0.25	ns
		Grounded	0.22	0.22	0.28	0.25	
		Limit -	-6	-6	-6	-6	
		Limit +	6	6	6	6	
Output-to-Output Skew between CLKOUTx's with Equal Frequency and Phase with the Clock divided and PVIN = 5V	$CLKOUTx_{SKEW1M}$	Biased (Figure 24)	0.27	0.21	0.25	0.00	ns
		Grounded	0.33	0.33	0.33	0.25	
		Limit -	-6	-6	-6	-6	
		Limit +	6	6	6	6	
Output-to-Output Skew between CLKOUTx's with Equal Frequency and Phase with the Clock divided and PVIN = 12V	$CLKOUTx_{SKEW1M}$	Biased (Figure 24)	0.27	0.21	0.25	0.00	ns
		Grounded	0.28	0.33	0.36	0.25	
		Limit -	-6	-6	-6	-6	
		Limit +	6	6	6	6	
Output-to-Output Skew between CLKOUTx's with Equal Frequency and Phase with the Clock divided and PVIN = 18V	$CLKOUTx_{SKEW1M}$	Biased (Figure 24)	0.25	0.25	0.25	0.00	ns
		Grounded	0.33	0.31	0.42	0.25	
		Limit -	-6	-6	-6	-6	
		Limit +	6	6	6	6	
Output-to-Output Skew Between CLKOUTx's with Equal Frequency and Different Phase Average of all Channels with PVIN = 3V	$CLKOUTx_{SKEW1M4P}$	Biased (Figure 24)	0.42	0.76	0.78	0.55	ns
		Grounded	0.45	0.79	0.75	0.36	
		Limit -	-7	-7	-7	-7	
		Limit +	7	7	7	7	

Table 11. Response of Key Parameters vs TID (Cont.)

Parameter	Symbol	Irradiation Condition	Pre-Rad Value	10krad(Si)	30krad(Si)	50krad(Si)	Unit
Output-to-Output Skew Between CLKOUTx's with Equal Frequency and Different Phase Average of all Channels with PVIN = 3V	$CLKOUTx_{SKEW1M4P}$	Biased (Figure 24)	0.14	0.39	0.42	0.66	ns
		Grounded	0.31	0.48	0.50	0.35	
		Limit -	-7	-7	-7	-7	
		Limit +	7	7	7	7	

8.2 Single Event Effects Testing

8.2.1 Introduction

The intense proton and heavy ion environment encountered in space applications can cause a variety of Single Event Effects (SEE) in electronic circuitry, including Single Event Upset (SEU), Single Event Transient (SET), Single Event Functional Interrupt (SEFI), Single Event Gate Rupture (SEGR), and Single Event Burnout (SEB). SEE can lead to system-level performance issues, including disruption, degradation, and destruction. Individual electronic components should be characterized for predictable and reliable space system operation to determine their SEE response.

8.2.2 Test Facility

SEE Testing was performed at the Texas A&M University (TAMU) Radiation Effects Facility of the Cyclotron Institute heavy ion facility. This facility is coupled to a K500 super-conducting cyclotron that can generate a wide range of particle beams with the various energy, flux, and fluence levels needed for advanced radiation testing. SEE testing was performed with normal incidence silver ions for an LET of 45.8MeV·cm^2/mg at the surface of the device. The LET of the ions in the active silicon layer ranged from 47.9MeV·cm^2/mg to 49.8MeV·cm^2/mg. Signals were communicated to and from the DUT test fixture through 20ft cables connecting to the control room.

8.2.3 Destructive Single Event Effects (DSEE) Results

DSEE testing consisted of three components: PVIN DSEE testing, VCC DSEE testing, and VCCEXT DSEE testing. For all three components, PRESCL and CLKIN were grounded. SCL and SDA were pulled-up to VCC through a 4.7kΩ resistor provided by the I^2C dongle. OUTEN and MASTER were tied to VCC. OSCTUNE was tied to ground through as 12.7kΩ resistor setting the internal oscillator frequency to 48MHz. CLKOUT0 provided an undivided output of the internal oscillator, CLKOUT1 provided a 24MHz clock output, CLKOUT2 provided a 333.33kHz clock output, and CLKOUT3 provided a 100kHz clock output. The phases for all the clock output were set to 0°. The die temperature was +125°C.

For PVIN DSEE testing, VCC and VCCEXT were bypassed to ground through a 0.68µF capacitor.

For VCC DSEE testing, the VCC supply was overdriven so that the internal regulator from PVIN was inactive. PVIN was set to 13.2V, and VCCEXT was set to 3.3V.

For VCCEXT DSEE testing, PVIN was set to 13.2V and VCC was bypassed to ground with a 0.68µF capacitor.

A DSEE was defined as an event in which the part loses functionality or a ±10% change in I_{PVIN}, I_{VCCEXT}, or I_{VCC}.

Testing showed that the ISL74420M did not exhibit any DSEE events on PVIN up to 20.7V, VCC up to 5.5V, and VCCEXT up to 6.5V.

8.2.4 SET and SEFI Results

For SET testing, the ambient temperature was 25°C. The ISL74420M was tested for SETs and SEFIs in the three configurations shown in Table 12.

Table 12. ISL74420M SET Test Conditions: Clock Frequencies

Configuration	Number of Devices Tested	Operation Mode	CLKOUT0 (MHz)	CLKOUT1 (MHz)	CLKOUT2 (kHz)	CLKOUT3 (kHz)
#1	4	Leader Mode using Internal Oscillator	48	24	333.33	100
#2	4	Follower Mode	25	3.125	43.403	13.021
#3	4	Leader Mode using External Clock	50	25	347.222	104.167

A SET was defined to be when the frequency on one of the CLKOUT pins deviated beyond ±2% of its operating frequency. Additionally, SEFIs were events in which the READY signal pulled low. Oscilloscope triggers were set to capture events where READY pulled below 1V or the frequency on one of the CLKOUT channels deviated beyond ±2% of its operating frequency.

Additionally, the I^2C registers were continually read to monitor for SEUs.

The data is summarized in Table 13. No SEUs in the I^2C registers were observed.

Table 13. ISL74420M SET Test Results Summary

TC	# of DUTs	Total Fluence (ions/cm^2)	# of CLKOUT0 SETs	CLKOUT 0 SET σ (μm^2)	# of CLKOUT1 SETs	CLKOUT1 SET σ (μm^2)	# of CLKOUT2 SETs	CLKOUT 2 SET σ (μm^2)	# of CLKOUT 3 SETs	CLKOUT 3 SET σ (μm^2)	# of SEFIs
#1	4	4.0E7	111	277.5	2	5	0	2.5	0	2.5	0
#2	4	4.0E7	0	2.5	0	2.5	0	2.5	0	2.5	0
#3	4	4.0E7	0	2.5	0	2.5	0	2.5	0	2.5	0

SETs only occurred when the ISL74420M operated in leader mode using the internal oscillator. All 111 captures on CLKOUT0 were frequency deviations events during which the frequency of the CLKOUT pulse changed beyond the ±2% window. However, no pulses were missed during any of the events. Figure 37 shows a typical CLKOUT0 capture. There was not a localized SET event, and the pulses are visually indistinguishable.

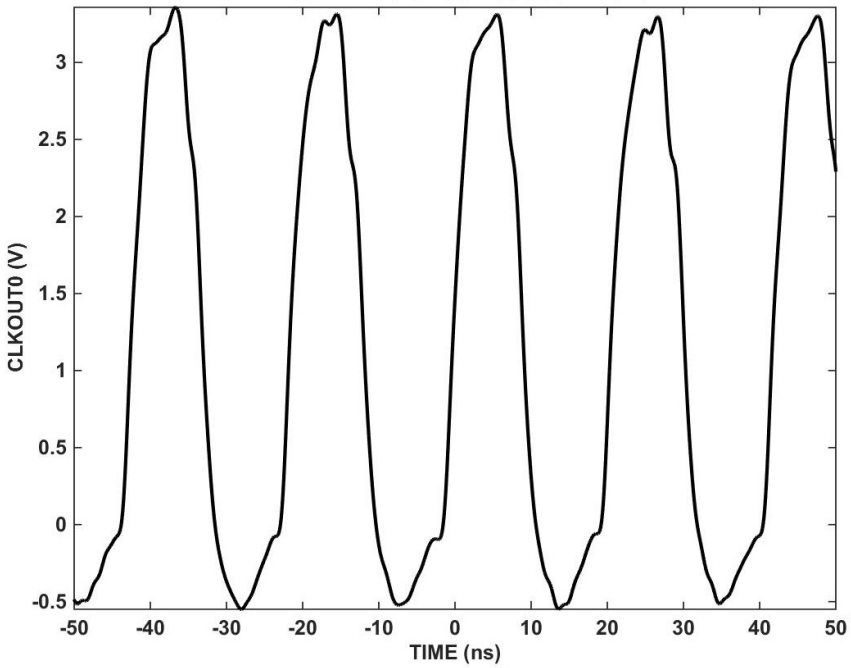


Figure 37. Typical SET capture on CLKOUT0

Figure 38 shows the distribution of the CLKOUT0 frequency deviations. The red lines indicate the ±2% window.

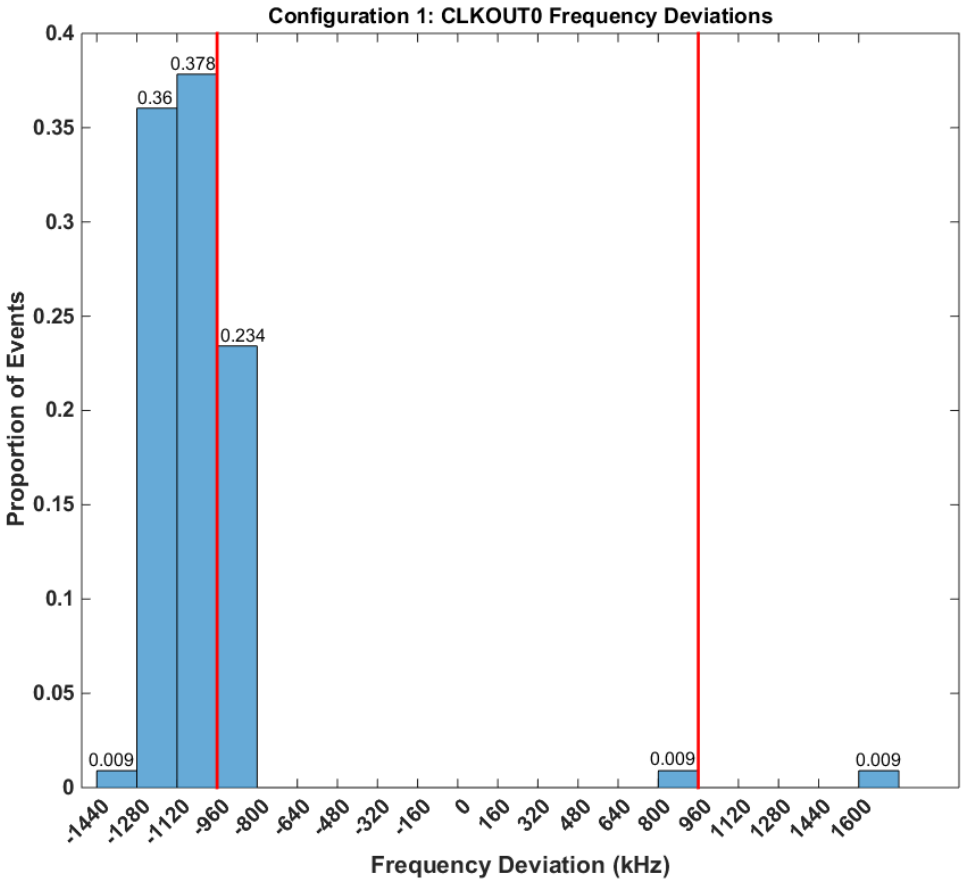


Figure 38. CLKOUT0 Frequency Deviations

All the frequency deviations on CLKOUT0 recovered by the next pulse.

The two captures on CLKOUT1 were also frequency deviations Figure 39 shows a typical capture on CLKOUT1. Similar to the captures on CLKOUT0, there was not a localized SET, and the pulses were visually indistinguishable.

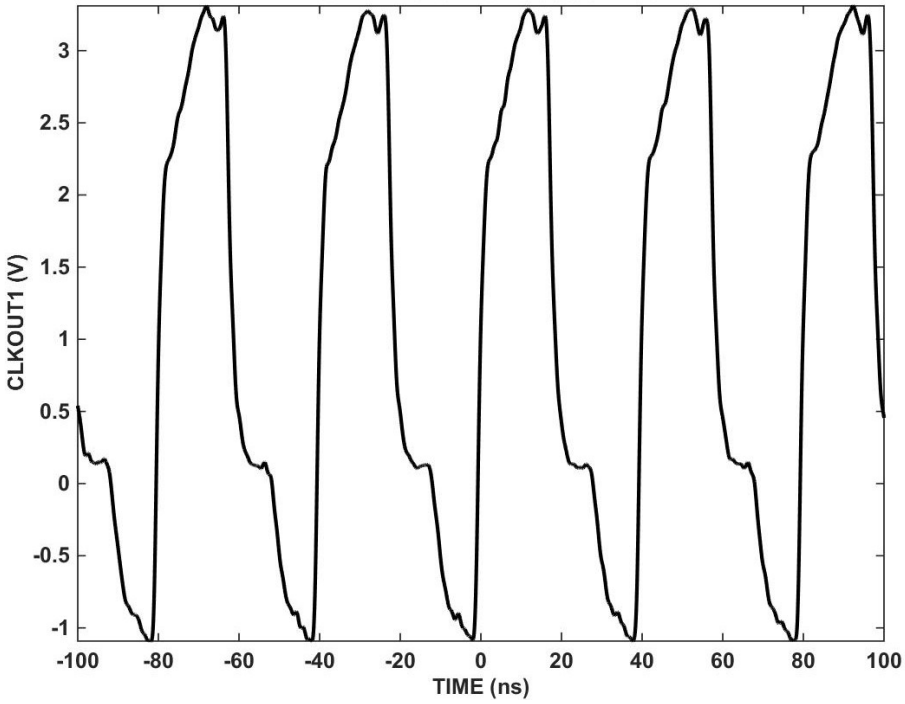


Figure 39. Typical SET capture on CLKOUT1

Figure 40 shows the distribution of the CLKOUT1 frequency deviations. The red lines indicate the ±2% window.

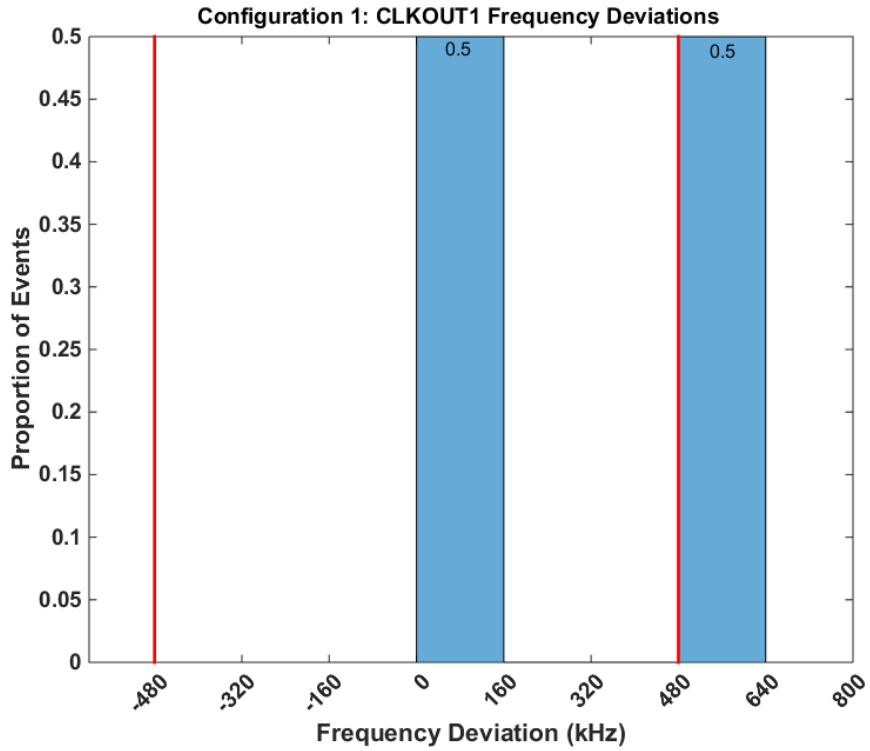


Figure 40. CLKOUT1 Frequency Deviations

One of the events had 12 pulses with frequency deviations beyond the ±2% window while the other had 13 pulses beyond the window.

CLKOUT2 and CLKOUT3 did not have any Sets. The ISL74420M did not exhibit any SEFIs.

8.2.5 Conclusion

Testing showed that the ISL74420M did not exhibit any DSEE events for PVIN = 20.7V, VCC = 5.5V, and VCCEXT = 6.5V at 46MeV•cm^2/mg.

The ISL74420M did not exhibit any missing pulse events or SEFIs. SEFI <10um2 at 46MeV•cm^2/mg.

The ISL74420M did exhibit frequency deviation SETs on CLKOUT0 (48MHz) and CLKOUT1 (24MHz) but did not exhibit SETs on CLKOUT2 (333kHz) or CLKOUT3 (100kHz) when operating in leader mode using the internal oscillator. However, given the rarity of the events, the immediate recovery on CLKOUT0, and the lack of a well-defined signature, the frequency deviation SETs are fairly innocuous. No missing pulse SETs and Frequency Deviation SETs < 3.6% on CLKOUTx at 46MeV•cm^2/mg.

9. Package Outline Drawing

The package outline drawing is located at the end of this document and is accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

10. Ordering Information

Part Number[1][2]	Part Marking	Radiation Lot Acceptance Testing	Package Description (RoHS Compliant)[3]	Pkg. Dwg #	Carrier Type	Temp. Range
ISL74420M50NZ	ISL74420 MNZ	LDR to 50krad(Si)	48Ld 7×7mm TQFP-EP	Q48.7x7C	Tray	-55 to +125°C
ISL74420M30NZ		LDR to 30krad(Si)				
ISL74420MEV1Z	Full-featured evaluation board with switch and jumper-configurable frequency and phase. Ideal for bench evaluation of the ISL74420M.					
ISL74420MDEMO1Z	Small form factor board with resistor-configurable frequency and phase. Ideal to provide clocks to switching power converter EVAL and DEMO boards.					

1. This Pb-free plastic packaged product employs special Pb-free material sets; molding compounds/die attach materials and NiPdAu-Ag plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. For Moisture Sensitivity Level (MSL), see the ISL74420M product page. For more information about MSL, see TB363.
3. For the Pb-Free Reflow Profile, see TB493.

11. Revision History

Revision	Date	Description
1.01	May 22, 2025	Updated page 1. Added Leader and Follower Core Oscillator configurations section. Added ECAD Information. Updated Q48.7x7C POD to the latest version; changes are as follows:. ▪ Overall: Applied the latest template. ▪ Top View: • Lead tip-to-tip tolerance changed from 0.20 to 0.10mm. • Pin #1 orientation moved from top left to bottom left. ▪ Side View: • Added Seating Plane ▪ Detail A: • Reversed the orientation; there was no dimension change. ▪ Recommended Land Pattern: • Recalculate all dimensions using the latest format.
1.00	Nov 18, 2024	Initial release

A. ECAD Design Information

This information supports the development of the PCB ECAD model for this device. It is intended to be used by PCB designers.

A.1 Part Number Indexing

Orderable Part Number	Number of Pins	Package Type	Package Code/POD Number
ISL74420M50NZ	48	TQFP-EP	Q48.7x7C
ISL74420M30NZ	48	TQFP-EP	Q48.7x7C

A.2 Symbol Pin Information

A.2.1 48-TQFP-EP

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
1	CH0 FREQ[2]	Input	-
2	CH0 FREQ[1]	Input	-
3	CH0 FREQ[0]	Input	-
4	PRESCL	Input	-
5	CLKOUT0	Output	-
6	GND	Power	-
7	GND	Power	-
8	CLKOUT1	Output	-
9	GND	Power	-
10	CH1 FREQ[0]	Input	-
11	CH1 FREQ[1]	Input	-
12	CH1 FREQ[2]	Input	-
13	CH1 PH[2]	Input	-
14	CH1 PH[1]	Input	-
15	CH1 PH[0]	Input	-
16	SCL	Input	-
17	SDA	I/O	-
18	GND	Power	-
19	OUTEN	Input	-
20	MASTER	Input	-
21	READY	Output	-
22	CH2 PH[0]	Input	-
23	CH2 PH[1]	Input	-
24	CH2 PH[2]	Input	-
25	CH2 FREQ[2]	Input	-
26	CH2 FREQ[1]	Input	-
27	CH2 FREQ[0]	Input	-
28	NC	Passive	-
29	CLKOUT2	Output	-
30	GND	Power	-
31	GND	Power	-
32	CLKOUT3	Output	-
33	GND	Power	-
34	CH3 FREQ[0]	Input	-
35	CH3 FREQ[1]	Input	-
36	CH3 FREQ[2]	Input	-
37	CH3 PH[2]	Input	-
38	CH3 PH[1]	Input	-
39	CH3 PH[0]	Input	-
40	PVIN	Power	-
41	CLKIN	Input	-
42	VCC	Power	-

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
43	VCCEXT	Power	-
44	GND	Power	-
45	OSCTUNE	Input	-
46	CH0 PH[0]	Input	-
47	CH0 PH[1]	Input	-
48	CH0 PH[2]	Input	-
EPAD49	GND	Power	-

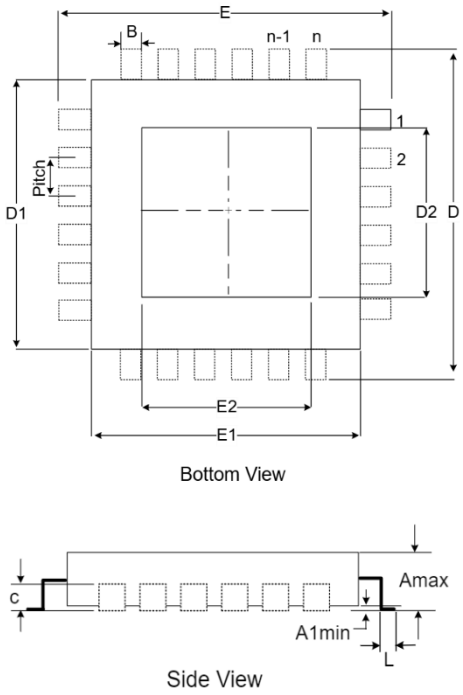
A.3 Symbol Parameters

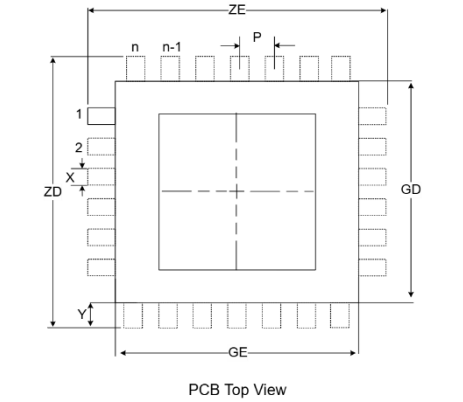
Orderable Part Number	Qualification	Radiation Qualification	LDR	Mounting Type	RoHS	Min Operating Temperature	Max Operating Temperature	Min Input Voltage	Max Input Voltage	Max Output Frequency	Output Type	Number of Output Channels	Interface	Phase Jitter	Core Frequency
ISL74420M30NZ	Space	Radiation Tolerant	30 krad(Si)	SMD	Compliant	-55 °C	125 °C	3 V	18 V	30 MHz	CMOS	4	I2C, SMBUS	25 ps	48 MHz
ISL74420M50NZ	Space	Radiation Tolerant	50 krad(Si)	SMD	Compliant	-55 °C	125 °C	3 V	18 V	30 MHz	CMOS	4	I2C, SMBUS	25 ps	48 MHz

A.4 Footprint Design Information

A.4.1 48-TQFP-EP

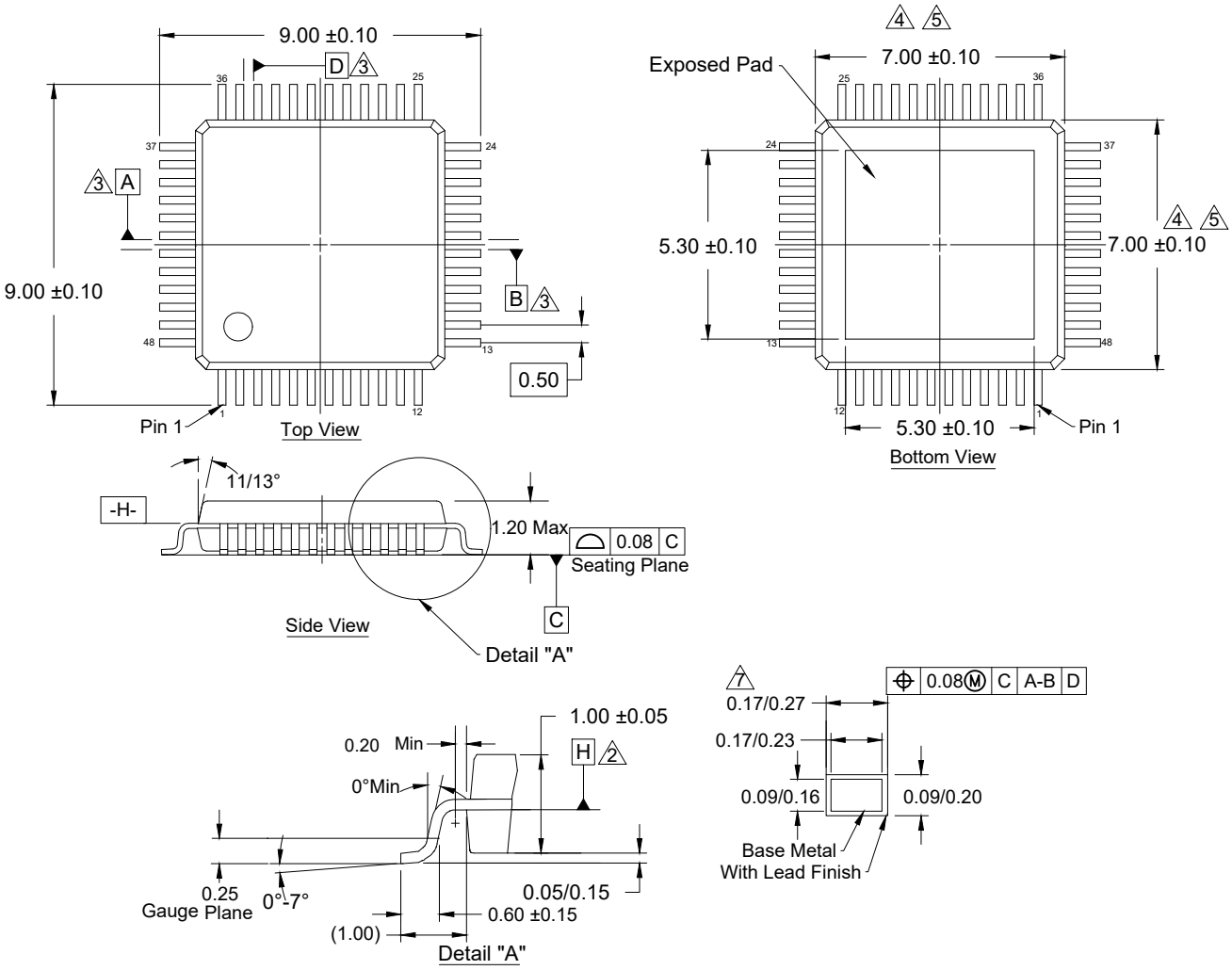
IPC Footprint Type	Package Code/ POD Number	Number of Pins
QFP	Q48.7x7C	48

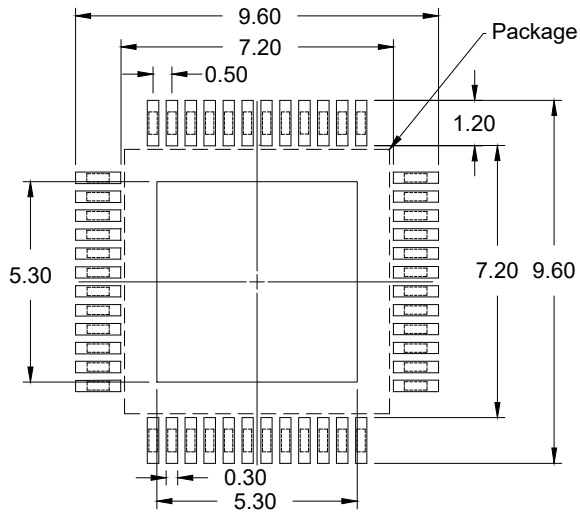
Description	Dimension	Value (mm)	Diagram
Minimum lead span (vertical side)	Dmin	8.90	
Maximum lead span (vertical side)	Dmax	9.10	
Minimum lead span (horizontal side)	Emin	8.90	
Maximum lead span (horizontal side)	Emax	9.10	
Minimum body span (vertical side)	D1min	6.90	
Maximum body span (vertical side)	D1max	7.10	
Minimum body span (horizontal side)	E1min	6.90	
Maximum body span (horizontal side)	E1max	7.10	
Minimum Lead Width	Bmin	0.17	
Maximum Lead Width	Bmax	0.27	
Number of pins (vertical side)	PinCountD	12	
Number of pins (horizontal side)	PinCountE	12	
Distance between the center of any two adjacent pins	Pitch	0.50	
Location of pin 1; S2 = corner of D side, C1 = center of E side	Pin1	S2	
Minimum thermal pad size (vertical side)	D2min	5.20	
Maximum thermal pad size (vertical side)	D2max	5.40	
Minimum thermal pad size (horizontal side)	E2min	5.20	
Maximum thermal pad size (horizontal side)	E2max	5.40	
Minimum Lead Length	Lmin	0.45	
Maximum Lead Length	Lmax	0.75	
Maximum Height	Amax	1.2	
Minimum Standoff Height	A1min	0.05	
Minimum Lead Thickness	cmin	0.09	
Maximum Lead Thickness	cmax	0.20	

Recommended Land Pattern			
Description	**Dimension**	**Value (mm)**	**Diagram**
Distance between left pad toe to right pad toe (horizontal side)	ZE	9.60	
Distance between top pad toe to bottom pad toe (vertical side)	ZD	9.60	
Distance between left pad heel to right pad heel (horizontal side)	GE	7.20	
Distance between top pad heel to bottom pad heel (vertical side)	GD	7.20	
Pad Width	X	0.30	
Pad Length	Y	1.20	

Package Outline Drawing

48 Thin Plastic Quad Flatpack Exposed Pad Packages (TQFP-EP)
POD Number: Q48.7x7C, Revision: 01, Date Created:May 6, 2025





Recommended Land Pattern

Notes:

1. All dimensioning and tolerancing conform to ANSI Y14.5-1982.
2. Datum plane H located at mold parting line and coincident with lead, where lead exits plastic body at bottom of parting line.
3. Datums A-B and D to be determined at centerline between leads where leads exit plastic body at datum plane H.
4. Dimensions do not include mold protrusion. Allowable mold protrusion is 0.254 mm .
5. These dimensions to be determined at datum plane H.
6. Package top dimensions are smaller than bottom dimensions and top of package does not overhang bottom of package.
7. Dimension does not include dambar protrusion. Allowable dambar protrusion is 0.08mm total in excess of the dimension at maximum material condition. Dambar cannot be located on the lower radius or the foot.
8. Controlling dimension: millimeter.
9. This outline conforms to jedec publication 95 registration MS-026, variation ABC-HD
10. DImensions in ( ) are for reference only.

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