ISL75052SEH, ISL73052SEH

1.5A, Radiation Hardened, Positive, High Voltage LDO

The ISL75052SEH and ISL73052SEH are radiation hardened, single output LDOs specified for an output current of 1.5A. The devices operate from an input voltage range of 4.0V to 13.2V and provide for output voltages of 0.6V to 12.7V. The output is adjustable based on a resistor divider setting. Dropout voltages as low as 75mV (at 0.5A) typical can be realized using the devices. This allows you to improve the system efficiency by lowering V_{IN} to nearly V_{OUT}.

The ENABLE feature allows the part to be placed into a low shutdown current mode of 165µA (typical). When enabled, the device operates with a low ground current of 11mA (typical), which provides for operation with low quiescent power consumption.

These devices have superior transient response and are designed keeping single event effects in mind. This results in reduction of the magnitude of SET seen on the output. There is no need for additional protection diodes and filters.

A COMP pin is provided to enable the use of external compensation. This is achieved by connecting a resistor and capacitor from COMP to ground. The device is stable with tantalum capacitors as low as 47µF (KEMET T525 series) and provides excellent regulation all the way from no load to full load. The programmable soft-start allows you to program the inrush current by means of the decoupling capacitor used on the BYP pin. The OCP pin allows the short-circuit output current limit threshold to be programmed by means of a resistor from OCP pin to GND. The OCP setting range is from 0.16A minimum to 3.2A maximum. The resistor sets the constant current threshold for the output under fault conditions. The thermal shutdown disables the output if the device temperature exceeds the specified value. It subsequently enters an ON/OFF cycle until the fault is removed.

Applications

- LDO regulator for space power systems
- DSP, FPGA, and µP core power supplies
- Post regulation of SMPS and down-hole drilling

Features

- **DLA SMD 5962-13220**
- **Input supply range 4.0V to 13.2V**
- **Output current up to 1.5A at T_J = +150°C**
- **Best in class accuracy ±1.5%**
  - **Over line, load, and temperature**
- **Ultra low dropout:**
  - **75mV dropout (typical) at 0.5A**
  - **225mV dropout (typical) at 1.5A**
- **Noise of 100µV_{RMS} (typical) between 300Hz to 300kHz**
- **SET mitigation with no added filtering/diodes**
- Shutdown current of 165µA (typical)
- Externally adjustable output voltage
- PSRR 65dB (typical) at 1kHz
- ENable and PGood feature
- Programmable soft-start/inrush current limiting
- Adjustable overcurrent protection
- Over-temperature shutdown
- Stable with 47µF minimum tantalum capacitor
- Radiation acceptance testing - ISL75052SEH
  - High dose rate (50-300rad(Si)/s). . . . . 100krad(Si)
  - Low dose rate (0.01rad(Si)/s) . . . . . .50krad(Si)
- Radiation acceptance testing - ISL73052SEH
  - Low dose rate (0.01rad(Si)/s) . . . . . .50krad(Si)
- SEE hardness (see SEE report for details)
  - No SEB/SEL LET_{TH}. . . . . .86MeV•cm^2/mg
  - SET (V_{OUT} within ±5% During Events) . .86MeV•cm^2/mg

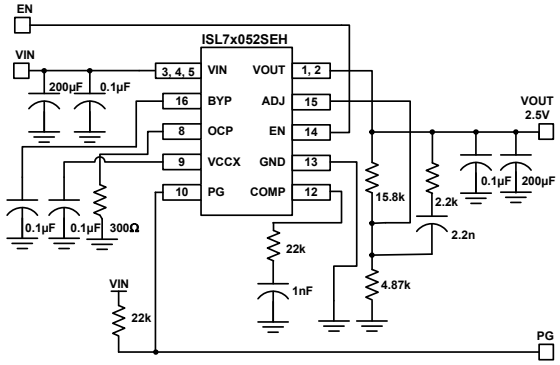


FIGURE 1. TYPICAL APPLICATION

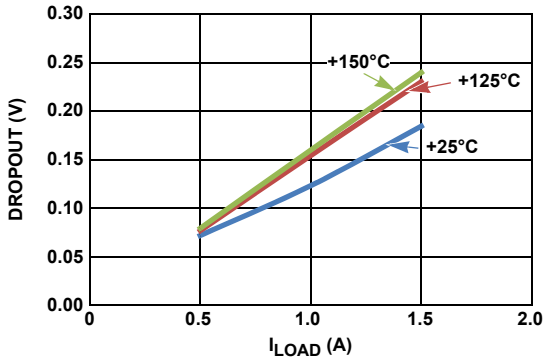


FIGURE 2. DROPOUT vs I_{OUT}

Block Diagram

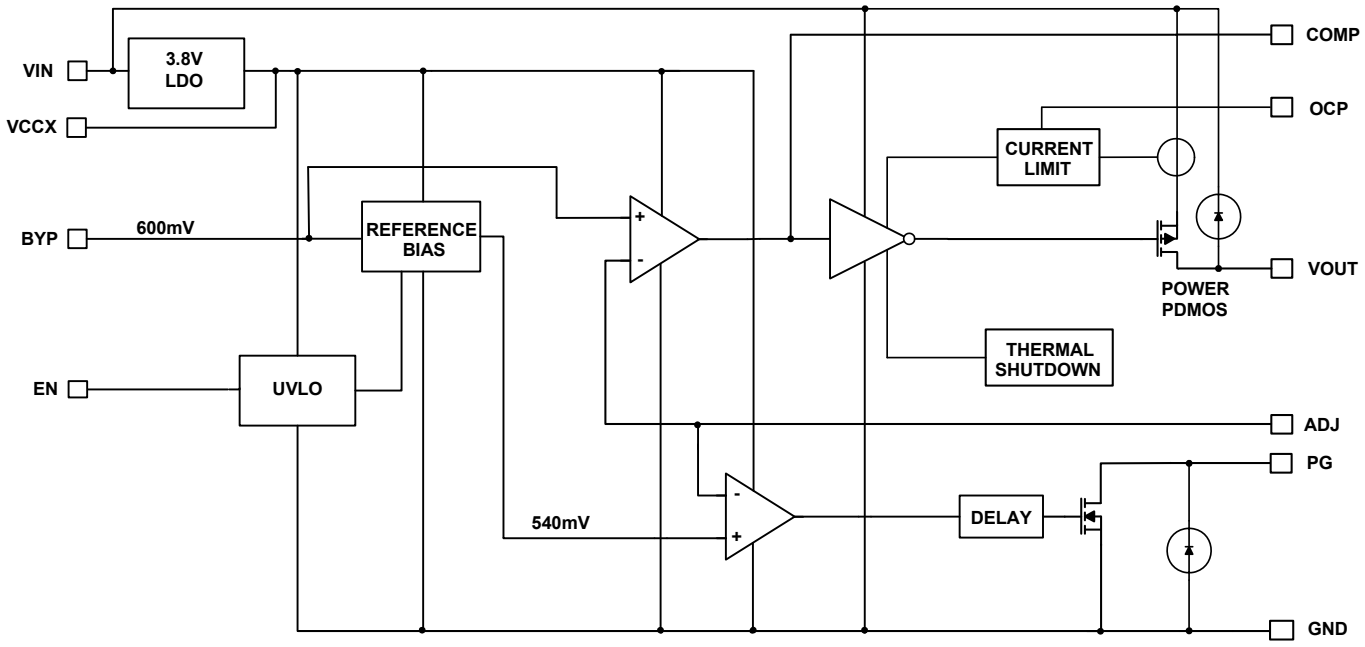


FIGURE 3. BLOCK DIAGRAM

Typical Application

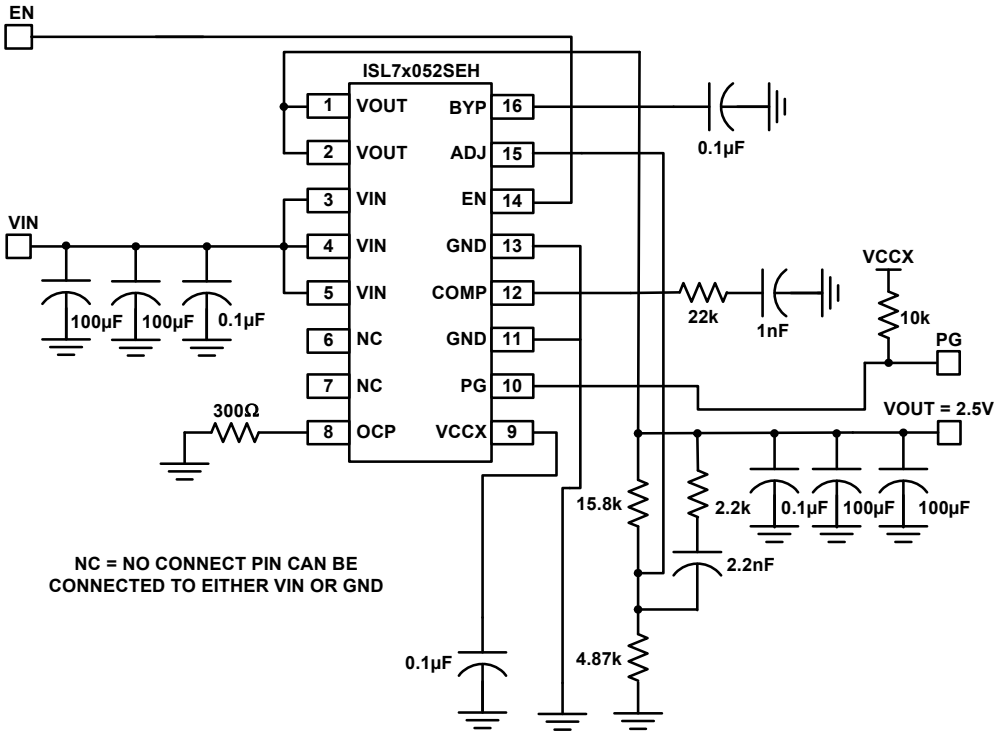


FIGURE 4. TYPICAL APPLICATION

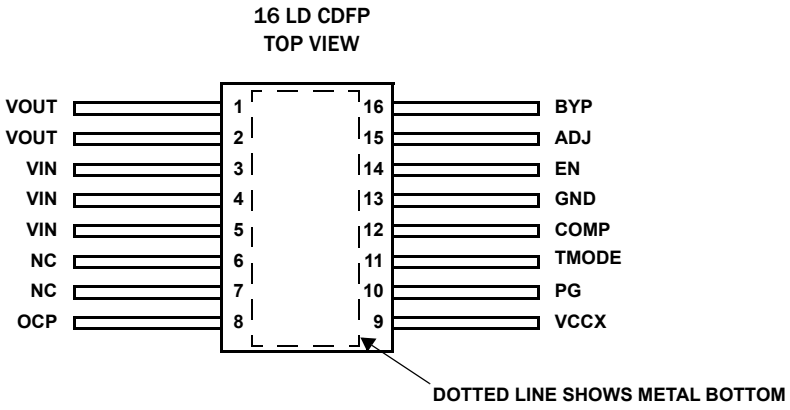
Ordering Information

ORDERING SMD NUMBER (Note 2)	PART NUMBER (Note 1)	RADIATION HARDNESS (Total Ionizing Dose)	PACKAGE (RoHS Compliant)	PKG DWG. #	TEMP RANGE
5962R1322001VXC	ISL75052SEHVFE	HDR to 100krad(Si) LDR to 50krad(Si)	16 Ld CDFP	K16.E	-55 to +125°C
5962R1322001V9A	ISL75052SEHVX (Note 3)		Die	-	
N/A	ISL75052SEHX/SAMPLE (Notes 3, 4)	N/A	Die Sample		
N/A	ISL75052SEHFE/PROTO (Note 4)	N/A	16 Ld CDFP	K16.E	
5962L1322002VXC	ISL73052SEHVFE	LDR to 50krad(Si)	16 Ld CDFP	K16.E	
5962L1322002V9A	ISL73052SEHVX (Note 3)		Die		
N/A	ISL73052SEHX/SAMPLE (Notes 3, 4)	N/A	Die Sample		
N/A	ISL73052SEHFE/PROTO (Note 4)	N/A	16 Ld CDFP	K16.E	
N/A	ISL75052SEHEVAL1Z (Note 5)	Evaluation Board			

NOTES:

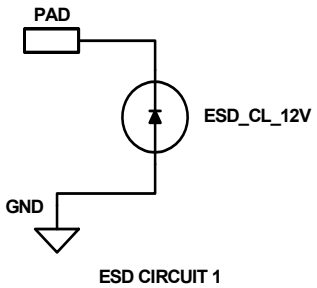
1. These Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
2. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed must be used when ordering.
3. Die product tested at T_A = + 25°C. The wafer probe test includes functional and parametric testing sufficient to make the die capable of meeting the electrical performance outlined in "Electrical Specifications" on page 5.
4. The /PROTO and /SAMPLE are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions across temperature specified in the DLA SMD and are in the same form and fit as the qualified device. The /SAMPLE parts are capable of meeting the electrical limits and conditions specified in the DLA SMD. The /SAMPLE parts do not receive 100% screening across temperature to the DLA SMD electrical limits. These part types do not come with a Certificate of Conformance because they are not DLA qualified devices.
5. Evaluation boards use the /PROTO parts and /PROTO parts are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity.

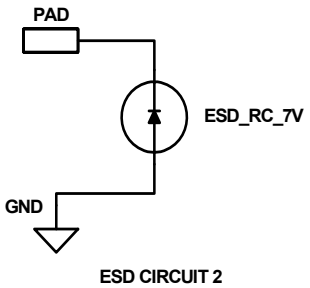
Pin Configuration



Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION	ESD CIRCUIT
1, 2	VOUT	Output voltage pins	Circuit 1
3, 4, 5	VIN	Input supply pins	Circuit 1
6, 7	NC	No connect. May be grounded if needed.	N/A
8	OCP	OCP pin allows the current limit to be programmed with an external resistor.	Circuit 2
9	VCCX	The 3.8V internal bus is pinned out to accept a decoupling capacitor. Connect a 0.1µF ceramic capacitor from VCCX pin to GND.	Circuit 2
10	PG	This pin is logic high when V_{OUT} is in regulation signal. A logic low defines when V_{OUT} is not in regulation.	Circuit 2
11	TMODE	Test Mode pin, must be connected to GND.	Circuit 2
12	COMP	Add compensation capacitor and resistor between COMP and GND.	Circuit 2
13	GND	GND pin. Pin 13 is also connected to the metal lid of the package.	Circuit 2
14	EN	V_{IN} independent chip enable. TTL and CMOS compatible.	Circuit 2
15	ADJ	ADJ pin allows V_{OUT} to be programmed with an external resistor divider.	Circuit 2
16	BYP	Connect a 0.1µF capacitor from BYP pin to GND, to filter the internal VREF.	Circuit 2
	Bottom Metalization	The metal surface on the bottom surface of the package is floating. For mounting instructions see "Bottom Metal Mounting Guidelines" on page 16.	Circuit 2





Absolute Maximum Ratings

VIN Relative to GND Without Ion Beam (Note 6) . . . . . -0.3 to +16.0V
VIN Relative to GND Under Ion Beam (Note 6) . . . . . -0.3 to +14.7V
VOUT Relative to GND (Note 6) . . . . . -0.3 to +14.7V
PG, EN, OCP/ADJ, COMP, REFIN,
REFOUT Relative to GND (Note 6) . . . . . -0.3 to +6.5V_{DC}
ESD Rating
Human Body Model (Tested per MIL-PRF-883 3015.7) 2kV
Machine Model (Tested per JESD22-A115-A) 200V
Charged Device Model (Tested per JESD22-C101D) 750V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
16 Ld CDFP Package (Notes 8, 9)	26	4.5

Storage Temperature Range . . . . . -65°C to +150°C
Junction Temperature (T_J) . . . . . +175°C

Recommended Operating Conditions (Note 7)

Ambient Temperature Range (T_A) . . . . . -55°C to +125°C
Junction Temperature (T_J) (Note 6) . . . . . +150°C
VIN Relative to GND . . . . . 4.0V to 13.2V
VOUT Range . . . . . 0.6V to 12.7V
PG, EN, OCP/ADJ Relative to GND . . . . . 0V to +5.5V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

NOTES:

6. Extended operation at these conditions may compromise reliability. Exceeding these limits results in damage. Recommended operating conditions define limits where specifications are established.
7. See "Bottom Metal Mounting Guidelines" on page 16.
8. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with direct attach features. See TB379.
9. For θ_{JC}, the case temperature location is the center of the exposed metal pad on the package underside.
10. Electromigration specification defined as lifetime average junction temperature of +150°C where maximum rated DC current = lifetime average current.

Electrical Specifications

Unless otherwise noted, $V_{IN} = V_{OUT} + 0.5V$, $V_{OUT} = 4.0V$, $C_{IN} = C_{OUT} = 2x100\mu F$ 60mΩ, KEMET type T541X107N025AH or equivalent, $T_J = +25°C$, $I_L = 0A$. Applications must follow thermal guidelines of the package to determine worst case junction temperature. See "Applications Information" on page 15 and TB379. **Boldface limits apply across the operating temperature range, -55°C to +125°C.** Pulse load techniques used by ATE to ensure $T_J = T_A$ defines established limits.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 11)	TYP	MAX (Note 11)	UNIT
DC CHARACTERISTICS						
DC Output Voltage Accuracy	V_{OUT}	V_{OUT} resistor adjust to: 2.5V and 5.0V				
		V_{OUT} = 2.5V, 4.0V < V_{IN} < 5.0V; 0A < I_{LOAD} < 1.5A, T_J = -55°C to +125°C	**-1.5**	0.2	**1.5**	%
		V_{OUT} = 2.5V, 4.0V < V_{IN} < 5.0V; 0A < I_{LOAD} < 1.5A, T_J = +25°C, post radiation	-2.0	0.2	2.0	%
		V_{OUT} = 5.0V, 5.5V < V_{IN} < 6.9V; 0A < I_{LOAD} < 1.5A, T_J = -55°C to +125°C	**-1.5**	0.2	**1.5**	%
		V_{OUT} = 5.0V, 5.5V < V_{IN} < 6.9V, 0A < I_{LOAD} < 1.5A, T_J = +25°C, post radiation	-2.0	0.2	2.0	%
		V_{OUT} resistor adjust to: 10.0V				
		V_{OUT} = 10.0V, 10.5V < V_{IN} < 13.2V, I_{LOAD} = 0A, T_J = -55°C to +125°C	**-1.5**	0.2	**1.5**	%
		V_{OUT} = 10.0V, 10.5V < V_{IN} < 13.2V, I_{LOAD} = 0A, T_J = +25°C, post radiation	-2.0	0.2	2.0	%
		V_{OUT} = 10.0V, V_{IN} = 10.5V, I_{LOAD} = 1.5A, V_{IN} = 13.2V, I_{LOAD} = 1.0A, T_J = -55°C to +125°C	**-1.5**	0.2	**1.5**	%
		V_{OUT} = 10.0V, V_{IN} = 10.5V; I_{LOAD} = 1.5A, V_{IN} = 13.2V, I_{LOAD} = 1.0A, T_J = +25°C, post radiation	-2.0	0.2	2.0	%
VCCX Pin	V_{VCCX}	T_J = -55°C to +125°C; 4V < V_{IN} < 13.2V; I_{LOAD} = 0A	**3.7**	3.9	**4.1**	V
ADJ Pin	V_{ADJ}	T_J = -55°C to +125°C	**591**	600	**609**	mV
ADJ Pin	V_{ADJ}	T_J = 25°C, post radiation	588	600	612	mV
BYP Pin	V_{BYP}	4.0V < V_{IN} < 13.2V; I_{LOAD} = 0A, T_J = -55°C to +125°C	**588**	600	**612**	mV

Electrical Specifications Unless otherwise noted, $V_{IN} = V_{OUT} + 0.5V$, $V_{OUT} = 4.0V$, $C_{IN} = C_{OUT} = 2x100\mu F$ 60mΩ, KEMET type T541X107N025AH or equivalent, $T_J = +25°C$, $I_L = 0A$. Applications must follow thermal guidelines of the package to determine worst case junction temperature. See "Applications Information" on page 15 and TB379. **Boldface limits apply across the operating temperature range, -55°C to +125°C.** Pulse load techniques used by ATE to ensure $T_J = T_A$ defines established limits. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 11)	TYP	MAX (Note 11)	UNIT
DC Input Line Regulation		$4.0V < V_{IN} < 13.2V$, $V_{OUT} = 2.5V$		1	**8**	mV
		$5.5V < V_{IN} < 13.2V$, $V_{OUT} = 5.0V$		1	**20**	mV
		$10.5V < V_{IN} < 13.2V$, $V_{OUT} = 10.0V$		1	**10**	mV
DC Output Load Regulation		$V_{OUT} = 2.5V$; $0A < I_{LOAD} < 1.5A$, $V_{IN} = 4.0V$		0.3	**9.0**	mV
		$V_{OUT} = 5.0V$; $0A < I_{LOAD} < 1.5A$, $V_{IN} = 5.5V$		1.3	**18.0**	mV
		$V_{OUT} = 10.0V$; $0A < I_{LOAD} < 1.5A$, $V_{IN} = 10.5V$		0.1	**36.0**	mV
ADJ Input Current		$V_{ADJ} = 0.6V$			1	µA
Ground Pin Current	I_Q	$V_{OUT} = 2.5V$; $I_{LOAD} = 0A$, $4.0V < V_{IN} < 13.2V$		6	**10**	mA
		$V_{OUT} = 2.5V$; $I_{LOAD} = 1.5A$, $4.0V < V_{IN} < 13.2V$		8	**12**	mA
		$V_{OUT} = 10.0V$, $I_{LOAD} = 0A$, $11.0V < V_{IN} < 13.2V$		15	**20**	mA
		$V_{OUT} = 10.0V$, $I_{LOAD} = 1.5A$, $11.0V < V_{IN} < 13.2V$		20	**25**	mA
Ground Pin Current in Shutdown	I_{SHDNL}	ENABLE pin = 0V, $V_{IN} = 4.0V$		70	**120**	µA
Ground Pin Current in Shutdown	I_{SHDNH}	ENABLE pin = 0V, $V_{IN} = 13.2V$		165	**300**	µA
Dropout Voltage (Note 13)	V_{DO}	$I_{LOAD} = 0.5A$, $V_{OUT} = 3.6V$ and 12.7V		75	**160**	mV
		$I_{LOAD} = 1.0A$, $V_{OUT} = 3.6V$ and 12.7V		150	**300**	mV
		$I_{LOAD} = 1.5A$, $V_{OUT} = 3.6V$ and 12.7V		225	**400**	mV
Output Short-Circuit Current for 16 Ld CDFP	ISCL	V_{OUT} SET = 4.0V, $V_{OUT} + 0.5V < V_{IN} < 13.2V$, $R_{SET} = 3k$, (Note 15)	0.16	0.24	0.32	A
Output Short-Circuit Current for 16 Ld CDFP	ISCH	V_{OUT} SET = 4.0V, $V_{OUT} + 0.5V < V_{IN} < 13.2V$, $R_{SET} = 300\Omega$, (Note 15)	1.6	2.4	3.2	A
Thermal Shutdown Temperature (Note 12)	TSD	$V_{OUT} + 0.5V < V_{IN} < 13.2V$	154	175	**196**	°C
Thermal Shutdown Hysteresis (Rising Threshold) (Note 12)	TSDn	$V_{OUT} + 0.5V < V_{IN} < 13.2V$			**25**	°C
AC CHARACTERISTICS						
Input Supply Ripple Rejection (Note 12)	PSRR	$V_{P-P} = 300mV$, f = 1kHz, $I_{LOAD} = 1.5A$; $V_{IN} = 4.9V$, $V_{OUT} = 4.0V$	**55**	65		dB
Input Supply Ripple Rejection (Note 12)	PSRR	$V_{P-P} = 300mV$, f = 120Hz, $I_{LOAD} = 5mA$; $V_{IN} = 4.9V$, $V_{OUT} = 2.5V$	**60**	70		dB
Input Supply Ripple Rejection (Note 12)	PSRR	$V_{P-P} = 300mV$, f = 100kHz, $I_{LOAD} = 1.5A$; $V_{IN} = 4.9V$, $V_{OUT} = 4.0V$	40	50		dB
Phase Margin (Note 12)	PM	$V_{OUT} = 2.5V$, 4.0V and 10V, $C_{OUT} = 2x100\mu F$, $R_{COMP} = 22k$, $C_{COMP} = 1nF$	**50**			°
Gain Margin (Note 12)	GM	$V_{OUT} = 2.5V$, 4.0V and 10V $C_{OUT} = 2x100\mu F$, $R_{COMP} = 22k$, $C_{COMP} = 1nF$	**10**			dB
Output Noise Voltage (Note 12)		$V_{IN} = 4.1V$, $V_{OUT} = 2.5V$, $I_{LOAD} = 10mA$, BW = 100Hz < f < 100kHz, BYPASS to GND capacitor = 0.2µF		100		μV_{RMS}

Electrical Specifications

Unless otherwise noted, $V_{IN} = V_{OUT} + 0.5V$, $V_{OUT} = 4.0V$, $C_{IN} = C_{OUT} = 2x100\mu F$ 60mΩ, KEMET type T541X107N025AH or equivalent, $T_J = +25°C$, $I_L = 0A$. Applications must follow thermal guidelines of the package to determine worst case junction temperature. See "Applications Information" on page 15 and TB379. **Boldface limits apply across the operating temperature range, -55°C to +125°C.** Pulse load techniques used by ATE to ensure $T_J = T_A$ defines established limits. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 11)	TYP	MAX (Note 11)	UNIT
DEVICE START-UP CHARACTERISTICS						
Enable Pin Characteristics						
Turn-On Threshold		$4.0V < V_{IN} < 13.2V$	**0.5**	0.8	**1.2**	V
Enable Pin Leakage Current		$V_{IN} = 13.2V$, EN = 5.5V			**1**	µA
Enable Pin Propagation Delay (EN step 1.2V to V_{OUT} = 100mV)		$V_{IN} = 4.5V$, $V_{OUT} = 4.0V$, $I_{LOAD} = 1.5A$, $C_{OUT} = 22\mu F$, $C_{BYP} = 0.2\mu F$		0.5	1.0	ms
Enable Pin Turn-On Delay (EN step 1.2V to PGOOD)		$V_{IN} = 4.5V$, $V_{OUT} = 4.0V$, $I_{LOAD} = 1.5A$, $C_{OUT} = 2x100\mu F$, $C_{BYP} = 0.2\mu F$		1.4	3.0	ms
Enable Pin Turn-On Delay (EN step 1.2V to PGOOD)		$V_{IN} = 4.5V$, $V_{OUT} = 4.0V$, $I_{LOAD} = 1.5A$, $C_{OUT} = 22\mu F$, $C_{BYP} = 0.2\mu F$		1.1	2.5	ms
Hysteresis (Falling Threshold)		$4.0V < V_{IN} < 13.2V$	**75**	170		mV
PG Pin Characteristics						
V_{OUT} Error Flag Rising Threshold			**83**	88	**94**	$\%V_{OUT}$
V_{OUT} Error Flag Falling Threshold			**80**	86	**91**	$\%V_{OUT}$
V_{OUT} Error Flag Hysteresis			**1.75**	2.50		$\%V_{OUT}$
Error Flag Low Voltage		$I_{SINK} = 1mA$		5	**100**	mV
Error Flag Low Voltage		$I_{SINK} = 10mA$		5	**400**	mV
Error Flag Leakage Current		$V_{IN} = 13.2V$, PG = 5.5V			**1**	µA

NOTES:

11. Parameters with bold face MIN and/or MAX limits are 100% tested at -55°C, +25°C and +125°C.
12. Limits established by characterization and are not production tested.
13. Dropout is defined by the difference in supply V_{IN} and V_{OUT} when the supply produces a 2% drop in V_{OUT} from its nominal value.
14. Refer to thermal package guidelines in "Bottom Metal Mounting Guidelines" on page 16.
15. OCP recovery overshoot should be within ±4% of the nominal V_{OUT} set point.
16. SET performance of <±5% at LET = 86MeV•cm2/mg has been evaluated at V_{OUT} = >2.5V with $C_{IN} = C_{OUT} = 2x100\mu F$ 10V 60mΩ in parallel with 0.1µF CDR04 X7R capacitor. Capacitor on BYP = 0.1µF CDR04 X7R.

High Dose Rate Post Radiation Characteristics

$T_A = +25°C$, unless otherwise noted. This data is typical test data post radiation exposure at a rate of 50 to 300rad(Si)/s (ISL75052SEH only). This data is intended to show typical parameter shifts due to high dose rate radiation (Note 17). These are not limits nor are they guaranteed.

ITEM#	DESCRIPTION	TEST CONDITIONS	0k RAD	100k RAD	UNIT
1	Enable Pin Leakage Current	$V_{IN} = 13.2V$, EN = 0V	-0.0375	-0.0409	µA
2	Enable Pin Leakage Current	$V_{IN} = 13.2V$, EN = 5.5V	-0.0006	0.0005	µA
3	ADJ Input Current	VADJ = 0.6V	-0.0007	-0.0010	µA
4	Ground Pin Current in Shutdown	EN pin = 0V, $V_{IN} = 4.0V$	68.0	67.5	µA
5	Ground Pin Current in Shutdown	EN pin = 0V, $V_{IN} = 13.2V$	162.7	163.1	µA
6	ADJ Pin	$V_{IN} = 4.0V$	0.60178	0.60489	V
7	BYP Pin	$V_{IN} = 4.0V$; $I_{LOAD} = 0A$	0.60075	0.60041	V
8	VCCX Pin	$V_{IN} = 4.0V$; $I_{LOAD} = 0A$	3.89156	3.87454	V
9	ADJ Pin	$V_{IN} = 13.2V$	0.60183	0.60495	V
10	BYP Pin	$V_{IN} = 13.2V$; $I_{LOAD} = 0A$	0.60105	0.60069	V
11	VCCX Pin	$V_{IN} = 13.2V$; $I_{LOAD} = 0A$	3.89260	3.87503	V
12	DC Output Voltage Accuracy	$V_{OUT} = 2.5V$, $V_{IN} = 4.0V$; $I_{LOAD} = 0A$, $T_A = +25°C$	2.51591	2.52880	V

High Dose Rate Post Radiation Characteristics

T_A = +25°C, unless otherwise noted. This data is typical test data post radiation exposure at a rate of 50 to 300rad(Si)/s (ISL75052SEH only). This data is intended to show typical parameter shifts due to high dose rate radiation (Note 17). These are not limits nor are they guaranteed. **(Continued)**

ITEM#	DESCRIPTION	TEST CONDITIONS	0k RAD	100k RAD	UNIT
13	DC Output Voltage Accuracy	V_{OUT} = 2.5V, V_{IN} = 4.0V; I_{LOAD} = 1.5A, = +25°C	2.51606	2.52893	V
14	DC Output Voltage Accuracy	V_{OUT} = 2.5V, V_{IN} = 5.0V; I_{LOAD} = 0A, = +25°C	2.51601	2.52879	V
15	DC Output Voltage Accuracy	V_{OUT} = 2.5V, V_{IN} = 5.0V; I_{LOAD} = 1.5A, = +25°C	2.51613	2.52894	V
16	DC Input Line Regulation	4.0V < V_{IN} < 13.2V, V_{OUT} = 2.5V	0.41881	0.43023	mV
17	DC Output Load Regulation	V_{OUT} = 2.5V; 0A < I_{LOAD} < 1.5A, V_{IN} = 4.0V	0.15429	0.13063	mV
18	DC Output Voltage Accuracy	V_{OUT} = 5.0V, V_{IN} = 5.5V; I_{LOAD} = 0A, = +25°C	5.02291	5.04849	V
19	DC Output Voltage Accuracy	V_{OUT} = 5.0V, V_{IN} = 5.5V; I_{LOAD} = 1.5A, = +25°C	5.02425	5.04984	V
20	DC Output Voltage Accuracy	V_{OUT} = 5.0V, V_{IN} = 6.9V; I_{LOAD} = 0A, = +25°C	5.02298	5.04900	V
21	DC Output Voltage Accuracy	V_{OUT} = 5.0V, V_{IN} = 6.9V; I_{LOAD} = 1.5A, = +25°C	5.02425	5.05003	V
22	DC Input Line Regulation	5.5V < V_{IN} < 13.2V, V_{OUT} = 5.0V	0.43559	0.71168	mV
23	DC Output Load Regulation	V_{OUT} = 5.0V; 0A < I_{LOAD} < 1.5A, V_{IN} = 5.5V	1.34488	1.34957	mV
24	DC Output Voltage Accuracy	V_{OUT} = 10.0V, V_{IN} = 10.5V; I_{LOAD} = 0A, = +25°C	10.05084	10.10237	V
25	DC Output Voltage Accuracy	V_{OUT} = 10.0V, V_{IN} = 10.5V; I_{LOAD} = 1.5A, = +25°C	10.04956	10.10146	V
26	DC Output Voltage Accuracy	V_{OUT} = 10.0V, V_{IN} = 13.2V; I_{LOAD} = 0A, = +25°C	10.05112	10.10158	V
27	DC Output Voltage Accuracy	V_{OUT} = 10.0V, V_{IN} = 13.2V; I_{LOAD} = 1.5A, = +25°C	10.05334	10.10470	V
28	DC Input Line Regulation	10.5V < V_{IN} < 13.2V, V_{OUT} = 10.0V	0.28300	-0.78996	mV
29	DC Output Load Regulation	V_{OUT} = 10.0V; 0A < I_{LOAD} < 1.5A, V_{IN} = 10.5V	-1.28285	-0.90861	mV
30	Ground Pin Current	V_{OUT} = 2.5V; I_{LOAD} = 0A, V_{IN} = 4.0V	5.4	5.3	mA
31	Ground Pin Current	V_{OUT} = 2.5V; I_{LOAD} = 1.5A, V_{IN} = 4.0V	7.1	7.1	mA
32	Ground Pin Current	V_{OUT} = 2.5V; I_{LOAD} = 0A, V_{IN} = 13.2V	5.6	5.6	mA
33	Ground Pin Current	V_{OUT} = 2.5V; I_{LOAD} = 1.5A, V_{IN} = 13.2V	5.6	5.6	mA
34	Ground Pin Current	V_{OUT} = 10.0V; I_{LOAD} = 0A, V_{IN} = 4.0V	13.5	13.4	mA
35	Ground Pin Current	V_{OUT} = 10.0V; I_{LOAD} = 1.5A, V_{IN} = 4.0V	13.8	13.8	mA
36	Ground Pin Current	V_{OUT} = 10.0V; I_{LOAD} = 0A, V_{IN} = 13.2V	11.7	11.7	mA
37	Ground Pin Current	V_{OUT} = 10.0V; I_{LOAD} = 1.5A, V_{IN} = 13.2V	13.3	13.6	mA
38	Dropout Voltage	I_{LOAD} = 0.5A, V_{OUT} = 3.6V	63.79	65.87	mV
39	Dropout Voltage	I_{LOAD} = 1.0A, V_{OUT} = 3.6V	130.74	134.93	mV
40	Dropout Voltage	I_{LOAD} = 1.5A, V_{OUT} = 3.6V	200.22	205.87	mV
41	Dropout Voltage	I_{LOAD} = 0.5A, V_{OUT} = 12.7V	67.06	69.05	mV
42	Dropout Voltage	I_{LOAD} = 1.0A, V_{OUT} = 12.7V	133.59	137.09	mV
43	Dropout Voltage	I_{LOAD} = 1.5A, V_{OUT} = 12.7V	202.13	207.74	mV
44	Error Flag Leakage Current	V_{IN} = 13.2V, PG = 5.5V	-0.0404	-0.0108	µA
45	Error Flag Low Voltage	I_{SINK} = 1mA	2.74	2.69	mV
46	Error Flag Low Voltage	I_{SINK} = 10mA	2.95	2.89	mV
47	V_{OUT} Error Flag Rising Threshold	V_{IN} = 13.2V	88.6	88.0	%
48	V_{OUT} Error Flag Falling Threshold	V_{IN} = 13.2V	86.1	85.5	%
49	V_{OUT} Error Flag Hysteresis	V_{IN} = 13.2V	2.5	2.5	%
50	V_{OUT} Error Flag Rising Threshold	V_{IN} = 4.0V	88.5	87.9	%

High Dose Rate Post Radiation Characteristics

T_A = +25°C, unless otherwise noted. This data is typical test data post radiation exposure at a rate of 50 to 300rad(Si)/s (ISL75052SEH only). This data is intended to show typical parameter shifts due to high dose rate radiation (Note 17). These are not limits nor are they guaranteed. **(Continued)**

ITEM#	DESCRIPTION	TEST CONDITIONS	0k RAD	100k RAD	UNIT
51	V_{OUT} Error Flag Falling Threshold	V_{IN} = 4.0V	86.0	85.4	%
52	V_{OUT} Error Flag Hysteresis	V_{IN} = 4.0V	2.5	2.5	%
53	Turn-On Threshold (Rising)	V_{IN} = 4.0V	0.930	0.928	V
54	Hysteresis	V_{IN} = 4.0V	163.8	163.3	mV
55	Turn-On Threshold (Rising)	V_{IN} = 13.2V	0.981	0.975	V
56	Hysteresis	V_{IN} = 13.2V	188.6	186.6	mV
57	Enable Pin Propagation Delay (EN step 1.2V to V_{OUT} = 100mV)	V_{IN} = 4.5V, V_{OUT} = 4.0V, I_{LOAD} = 1.5A, C_{OUT} = 22µF, C_{BYP} = 0.2µF	483.9	489.4	µs
58	Enable Pin Turn-On Delay (EN step 1.2V to PGOOD)	V_{IN} = 4.5V, V_{OUT} = 4.0V, I_{LOAD} = 1.5A, C_{OUT} = 22µF, C_{BYP} = 0.2µF	1007.6	984.1	µs
59	Enable Pin Turn-On Delay (EN step 1.2V to PGOOD)	V_{IN} = 4.5V, V_{OUT} = 4.0V, I_{LOAD} = 1.5A, C_{OUT} = 2x100µF, CBYP = 0.2µF	1312.8	1319.1	µs
60	Output Short-Circuit Current	V_{OUT} = 4.0V, V_{IN} = 4.5V, R_{SET} = 3k	0.235	0.234	A
61	Output Short-Circuit Current	V_{OUT} = 4.0V, V_{IN} = 13.2V, R_{SET} = 3k	0.240	0.239	A
62	Output Short-Circuit Current	V_{OUT} = 4.0V, V_{IN} = 4.5V, R_{SET} = 300	2.524	2.526	A
63	Output Short-Circuit Current	V_{OUT} = 4.0V, V_{IN} = 13.2V, R_{SET} = 300	2.538	2.540	A

Low Dose Rate Post Radiation Characteristics

T_A = +25°C, unless otherwise noted. This data is typical test data post radiation exposure at a rate of 10mrad(Si)/s. This data is intended to show typical parameter shifts due to low dose rate radiation (Note 17). These are not limits nor are they guaranteed (based on initial LDR characterization).

ITEM#	DESCRIPTION	TEST CONDITIONS	0k RAD	50k RAD	UNIT
1	Enable Pin Leakage Current	V_{IN} = 13.2V, EN = 0V	-0.0390	-0.0298	µA
2	Enable Pin Leakage Current	V_{IN} = 13.2V, EN = 5.5V	-0.0010	0.0092	µA
3	ADJ Input Current	V_{ADJ} = 0.6V	-0.0115	-0.0070	µA
4	Ground Pin Current in Shutdown	ENABLE Pin = 0V, V_{IN} = 4.0V	68.8	65.1	µA
5	Ground Pin Current in Shutdown	ENABLE Pin = 0V, V_{IN} = 13.2V	163.4	159.9	µA
6	ADJ Pin	V_{IN} = 4.0V	0.60162	0.60174	V
7	BYP Pin	V_{IN} = 4.0V; I_{LOAD} = 0A	0.60019	0.60048	V
8	VCCX Pin	V_{IN} = 4.0V; I_{LOAD} = 0A	3.88673	3.88170	V
9	ADJ Pin	V_{IN} = 13.2V	0.60168	0.60179	V
10	BYP Pin	V_{IN} = 13.2V; I_{LOAD} = 0A	0.60049	0.60057	V
11	VCCX Pin	V_{IN} = 13.2V; I_{LOAD} = 0A	3.88770	3.88246	V
12	DC Output Voltage Accuracy	V_{OUT} = 2.5V, V_{IN} = 4.0V; I_{LOAD} = 0A, T_A = +25°C	2.51577	2.51488	V
13	DC Output Voltage Accuracy	V_{OUT} = 2.5V, V_{IN} = 4.0V; I_{LOAD} = 1.5A, T_A = +25°C	2.51596	2.51508	V
14	DC Output Voltage Accuracy	V_{OUT} = 2.5V, V_{IN} = 5.0V; I_{LOAD} = 0A, T_A = +25°C	2.51598	2.51504	V
15	DC Output Voltage Accuracy	V_{OUT} = 2.5V, V_{IN} = 5.0V; I_{LOAD} = 1.5A, T_A = +25°C	2.51611	2.51520	V
16	DC Input Line Regulation	4.0V < V_{IN} < 13.2V, V_{OUT} = 2.5V	0.51044	0.44539	mV
17	DC Output Load Regulation	V_{OUT} = 2.5V; 0A < I_{LOAD} < 1.5A, V_{IN} = 4.0V	0.19541	0.20233	mV
18	DC Output Voltage Accuracy	V_{OUT} = 5.0V, V_{IN} = 5.5V; I_{LOAD} = 0A, T_A = +25°C	5.02321	5.02138	V
19	DC Output Voltage Accuracy	V_{OUT} = 5.0V, V_{IN} = 5.5V; I_{LOAD} = 1.5A, T_A = +25°C	5.02434	5.02257	V
20	DC Output Voltage Accuracy	V_{OUT} = 5.0V, V_{IN} = 6.9V; I_{LOAD} = 0A, T_A = +25°	5.02324	5.02155	V
21	DC Output Voltage Accuracy	V_{OUT} = 5.0V, V_{IN} = 6.9V; I_{LOAD} = 1.5A, T_A = +25°C	5.02443	5.02267	V
22	DC Input Line Regulation	5.5V < V_{IN} < 13.2V, V_{OUT} = 5.0V	0.10020	0.16807	mV
23	DC Output Load Regulation	V_{OUT} = 5.0V; 0A < I_{LOAD} < 1.5A, V_{IN} = 5.5V	1.13716	1.19041	mV

Low Dose Rate Post Radiation Characteristics

T_A = +25°C, unless otherwise noted. This data is typical test data post radiation exposure at a rate of 10mrad(Si)/s. This data is intended to show typical parameter shifts due to low dose rate radiation (Note 17). These are not limits nor are they guaranteed (based on initial LDR characterization). **(Continued)**

ITEM#	DESCRIPTION	TEST CONDITIONS	0k RAD	50k RAD	UNIT
24	DC Output Voltage Accuracy	V_{OUT} = 10.0V, V_{IN} = 10.5V; I_{LOAD} = 0A, T_A = +25°C	10.04951	10.04602	V
25	DC Output Voltage Accuracy	V_{OUT} = 10.0V, V_{IN} = 10.5V; I_{LOAD} = 1.5A, T_A = +25°C	10.04930	10.04583	V
26	DC Output Voltage Accuracy	V_{OUT} = 10.0V, V_{IN} = 13.2V; I_{LOAD} = 0A, T_A = +25°C	10.05009	10.04631	V
27	DC Output Voltage Accuracy	V_{OUT} = 10.0V, V_{IN} = 13.2V; I_{LOAD} = 1.5A, T_A = +25°C	10.05191	10.04823	V
28	DC Input Line Regulation	10.5V < V_{IN} < 13.2V, V_{OUT} = 10.0V	0.58653	0.29418	mV
29	DC Output Load Regulation	V_{OUT} = 10.0V; 0A < I_{LOAD} < 1.5A, V_{IN} = 10.5V	-0.20163	-0.18742	mV
30	Ground Pin Current	V_{OUT} = 2.5V; I_{LOAD} = 0A, V_{IN} = 4.0V	5.5	5.8	mA
31	Ground Pin Current	V_{OUT} = 2.5V; I_{LOAD} = 1.5A, V_{IN} = 4.0V	7.2	7.4	mA
32	Ground Pin Current	V_{OUT} = 2.5V; I_{LOAD} = 0A, V_{IN} = 13.2V	5.6	5.9	mA
33	Ground Pin Current	V_{OUT} = 2.5V; I_{LOAD} = 1.5A, V_{IN} = 13.2V	5.6	5.9	mA
34	Ground Pin Current	V_{OUT} = 10.0V; I_{LOAD} = 0A, V_{IN} = 4.0V	14.0	14.3	mA
35	Ground Pin Current	V_{OUT} = 10.0V; I_{LOAD} = 1.5A, V_{IN} = 4.0V	14.1	14.5	mA
36	Ground Pin Current	V_{OUT} = 10.0V; I_{LOAD} = 0A, V_{IN} = 13.2V	11.9	12.3	mA
37	Ground Pin Current	V_{OUT} = 10.0V; I_{LOAD} = 1.5A, V_{IN} = 13.2V	13.5	13.9	mA
38	Dropout Voltage	I_{LOAD} = 0.5A, V_{OUT} = 3.6V	67.19	68.88	mV
39	Dropout Voltage	I_{LOAD} = 1.0A, V_{OUT} = 3.6V	138.01	140.62	mV
40	Dropout Voltage	I_{LOAD} = 1.5A, V_{OUT} = 3.6V	210.09	213.41	mV
41	Dropout Voltage	I_{LOAD} = 0.5A, V_{OUT} = 12.7V	70.54	72.94	mV
42	Dropout Voltage	I_{LOAD} = 1.0A, V_{OUT} = 12.7V	140.61	143.23	mV
43	Dropout Voltage	I_{LOAD} = 1.5A, V_{OUT} = 12.7V	212.35	215.80	mV
44	Error Flag Leakage Current	V_{IN} = 13.2V, PG = 5.5V	-0.0581	-0.0364	µA
45	Error Flag Low Voltage	I_{SINK} = 1mA	2.72	2.81	mV
46	Error Flag Low Voltage	I_{SINK} = 10mA	2.92	2.97	mV
47	V_{OUT} Error Flag Rising Threshold	V_{IN} = 13.2V	88.6	88.5	%
48	V_{OUT} Error Flag Falling Threshold	V_{IN} = 13.2V	86.0	86.0	%
49	V_{OUT} Error Flag Hysteresis	V_{IN} = 13.2V	2.5	2.5	%
50	V_{OUT} Error Flag Rising Threshold	V_{IN} = 4.0V	88.4	88.4	%
51	V_{OUT} Error Flag Falling Threshold	V_{IN} = 4.0V	85.9	85.9	%
52	V_{OUT} Error Flag Hysteresis	V_{IN} = 4.0V	2.5	2.5	%
53	Turn-On Threshold (Rising)	V_{IN} = 4.0V	0.925	0.923	V
54	Hysteresis	V_{IN} = 4.0V	162.6	161.3	mV
55	Turn-On Threshold (Rising)	V_{IN} = 13.2V	0.975	0.972	V
56	Hysteresis	V_{IN} = 13.2V	186.9	185.0	mV
57	Enable Pin Propagation Delay (EN step 1.2V to V_{OUT} = 100mV)	V_{IN} = 4.5V, V_{OUT} = 4.0V, I_{LOAD} = 1.5A, C_{OUT} = 22µF, C_{BYP} = 0.2µF	531.5	531.8	µs
58	Enable Pin Turn-On Delay (EN step 1.2V to PGOOD)	V_{IN} = 4.5V, V_{OUT} = 4.0V, I_{LOAD} = 1.5A, C_{OUT} = 22µF, C_{BYP} = 0.2µF	1033.7	1031.8	µs
59	Enable Pin Turn-On Delay (EN step 1.2V to PGOOD)	V_{IN} = 4.5V, V_{OUT} = 4.0V, I_{LOAD} = 1.5A, C_{OUT} = 2x100µF, C_{BYP} = 0.2µF	1297.9	1305.7	µs
60	Output Short-Circuit Current	V_{OUT} = 4.0V, V_{IN} = 4.5V, R_{SET} = 3k	0.236	0.236	A
61	Output Short-Circuit Current	V_{OUT} = 4.0V, V_{IN} = 13.2V, R_{SET} = 3k	0.240	0.241	A
62	Output Short-Circuit Current	V_{OUT} = 4.0V, V_{IN} = 4.5V, R_{SET} = 300	2.575	2.564	A
63	Output Short-Circuit Current	V_{OUT} = 4.0V, V_{IN} = 13.2V, R_{SET} = 300	2.584	2.573	A

NOTE:

17. See the Radiation report.

Typical Operating Performance

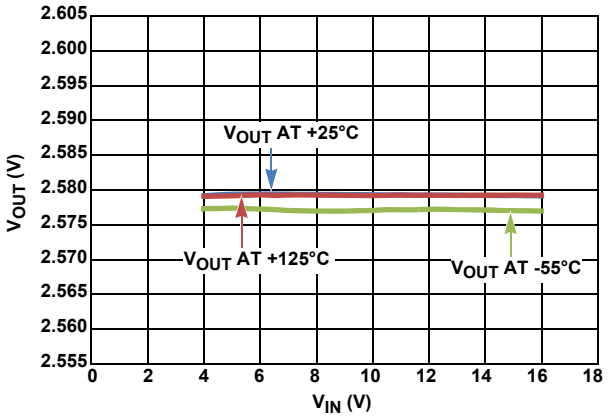


FIGURE 5. LINE REGULATION vs TEMPERATURE (°C), V_{OUT} = 2.579V, I_{OUT} = 0mA

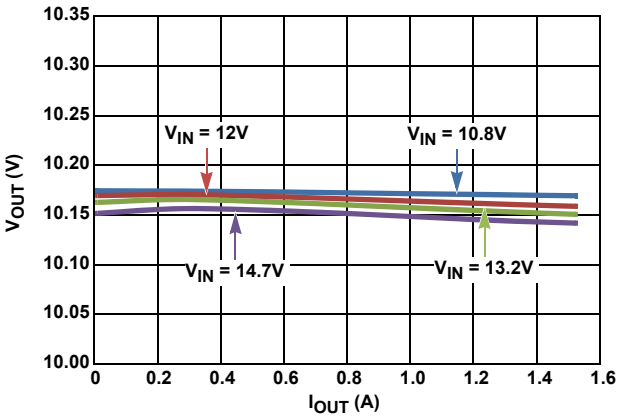


FIGURE 6. LOAD REGULATION V_{OUT} = 10.17V AT +25°C

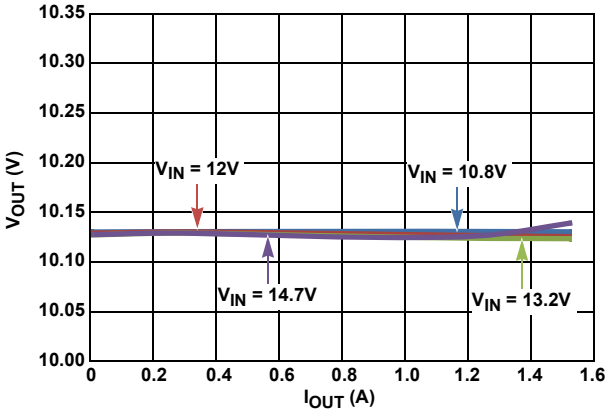


FIGURE 7. LOAD REGULATION V_{OUT} = 10.13V AT +125°C

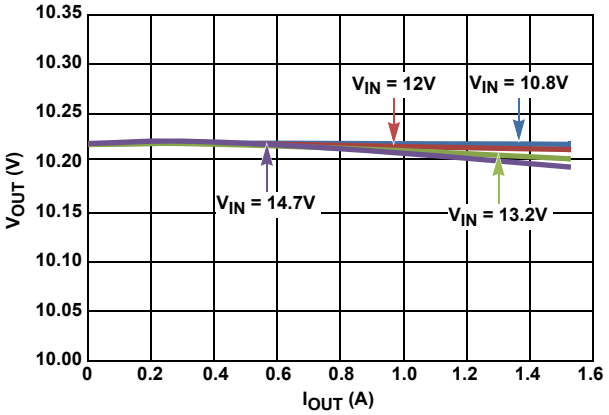


FIGURE 8. LOAD REGULATION V_{OUT} = 10.22V AT -55°C

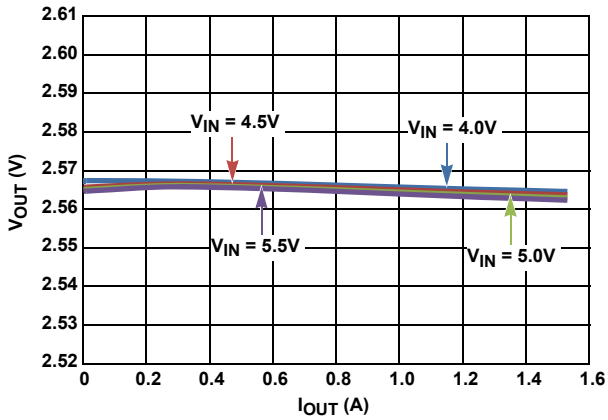


FIGURE 9. LOAD REGULATION V_{OUT} = 2.567V AT +25°C

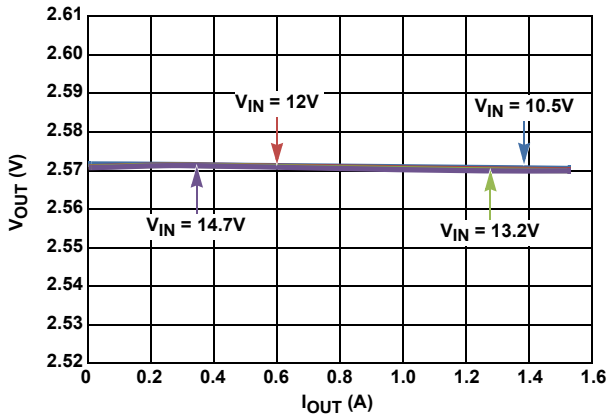


FIGURE 10. LOAD REGULATION V_{OUT} = 2.571V AT +125°C

Typical Operating Performance (Continued)

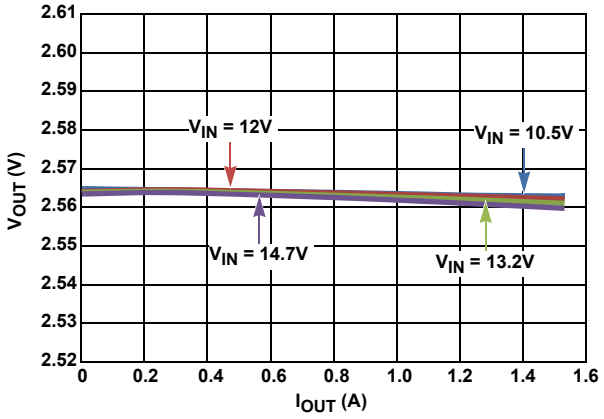


FIGURE 11. LOAD REGULATION V_{OUT} = 2.564V AT -55°C

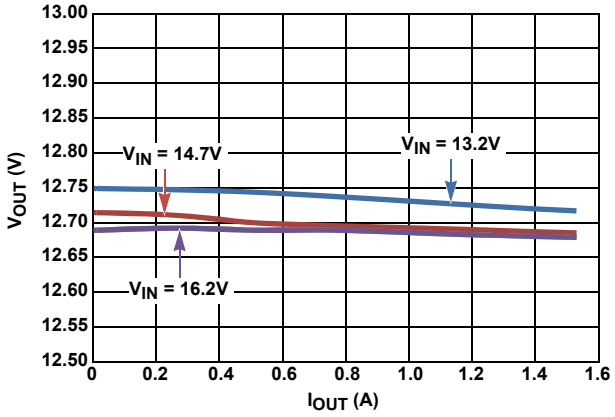


FIGURE 12. LOAD REGULATION V_{OUT} = 12.75V AT +25°C

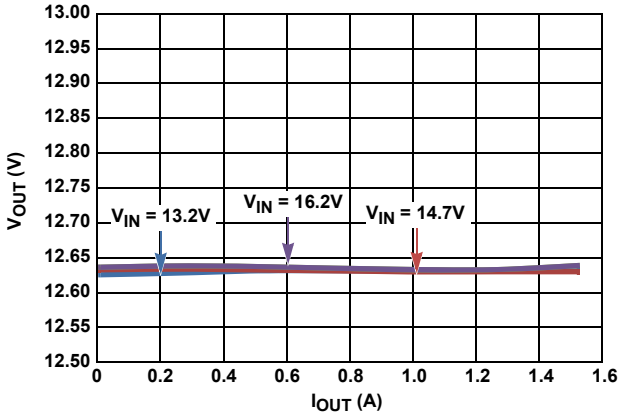


FIGURE 13. LOAD REGULATION V_{OUT} = 12.63V AT +125°C

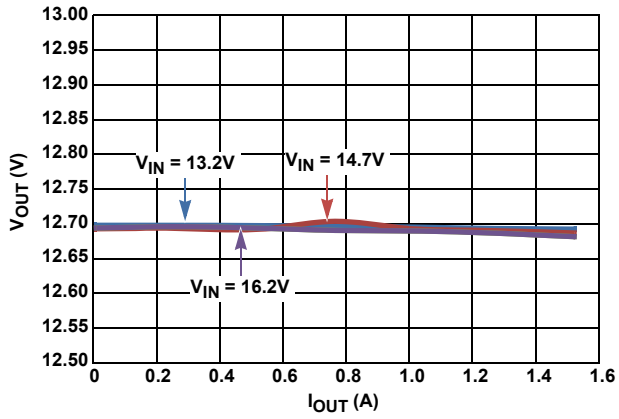


FIGURE 14. LOAD REGULATION V_{OUT} = 12.7V AT -55°C

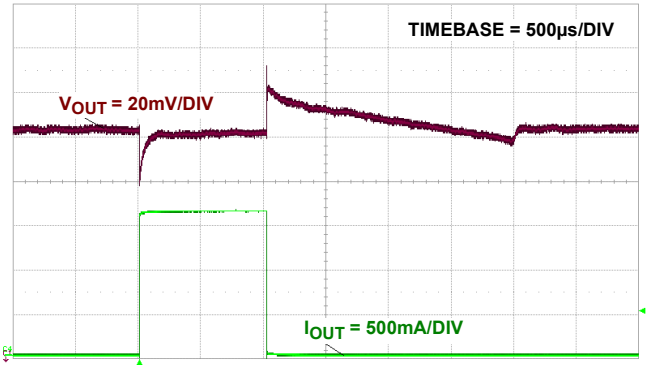


FIGURE 15. LOAD STEP RESPONSE +25°C, V_{IN} = 4.0V, V_{OUT} = 2.5V, I_{OUT} = 0A TO 1.6A, C_{OUT} = 200µF, 30mΩ

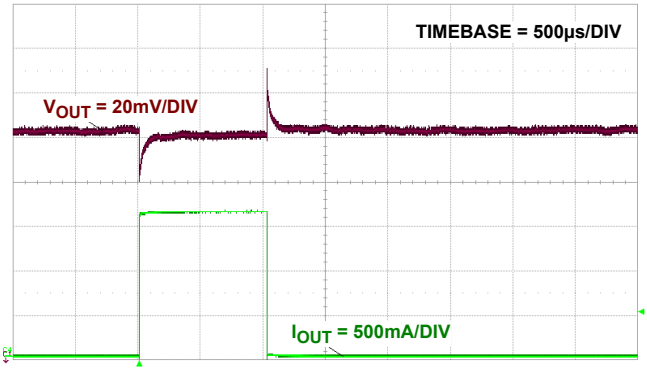


FIGURE 16. LOAD STEP RESPONSE, +25°C, V_{IN} = 4.0V, V_{OUT} = 2.5V, I_{OUT} = 0.15A TO 1.6A, C_{OUT} = 200µF, 30mΩ

Typical Operating Performance (Continued)

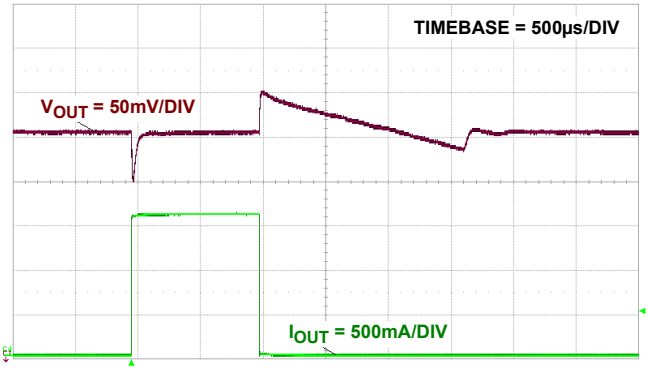


FIGURE 17. LOAD STEP RESPONSE, +25°C, V_{IN} = 13.2V, V_{OUT} = 10V, I_{OUT} = 0A TO 1.5A, C_{OUT} = 200µF, 30mΩ

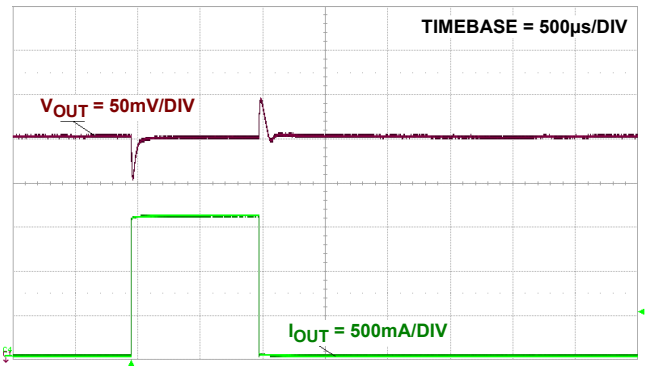


FIGURE 18. LOAD STEP RESPONSE, +25°C, V_{IN} = 13.2V, V_{OUT} = 10V, I_{OUT} = 0.15A TO 1.5A, C_{OUT} = 200µF, 30mΩ

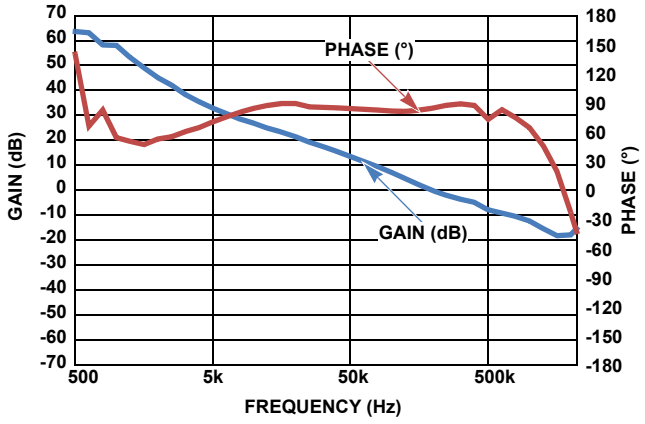


FIGURE 19. GAIN PHASE PLOTS, V_{IN} = 4V, V_{OUT} = 2.5V, I_{OUT} = 1.5A, R_{COMP} = 22k, C_{COMP} = 1nF, C_{OUT} = 200µF, 30mΩ, PHASE MARGIN = 98.68°, GAIN MARGIN = 23.01dB

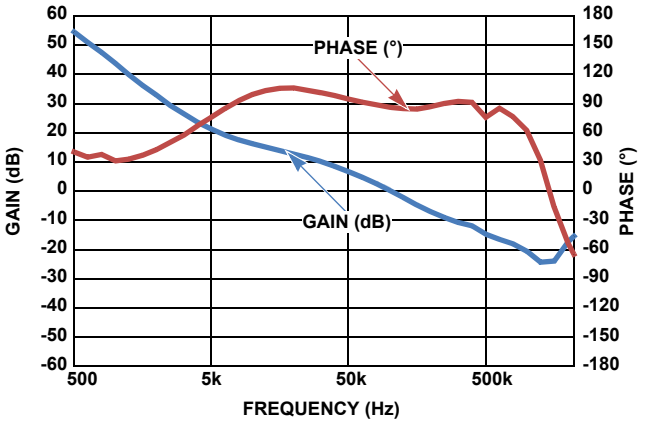


FIGURE 20. GAIN PHASE PLOTS, V_{IN} = 11V, V_{OUT} = 10V, I_{OUT} = 1.5A, R_{COMP} = 22k, C_{COMP} = 1nF, C_{OUT} = 200µF, 30mΩ, PHASE MARGIN = 84.56°, GAIN MARGIN = 18.06dB

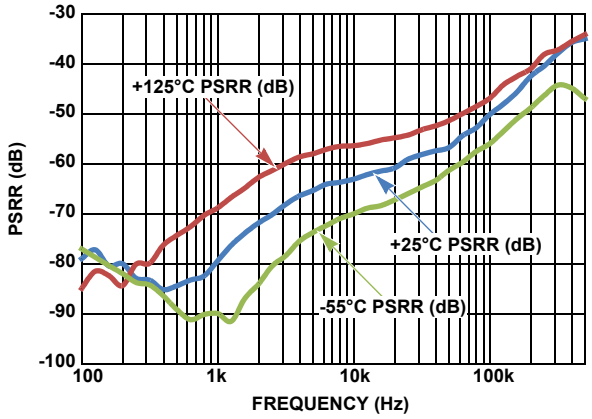


FIGURE 21. PSRR, V_{IN} = 4.9V, V_{OUT} = 4.0V, I_{OUT} = 1.5A, R_{COMP} = 22k, C_{COMP} = 1nF, C_{OUT} = 200µF, 30mΩ

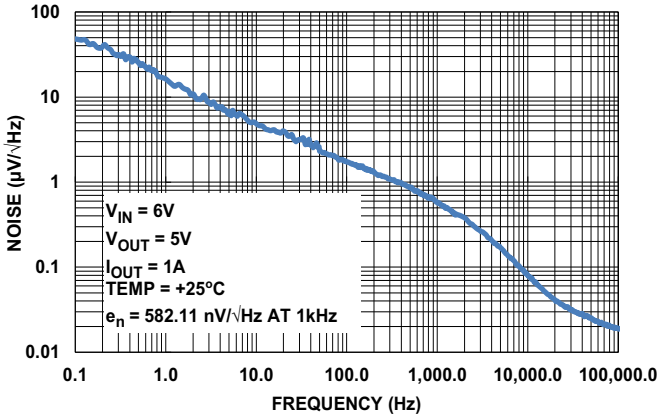


FIGURE 22. OUTPUT NOISE DENSITY

Typical Operating Performance (Continued)

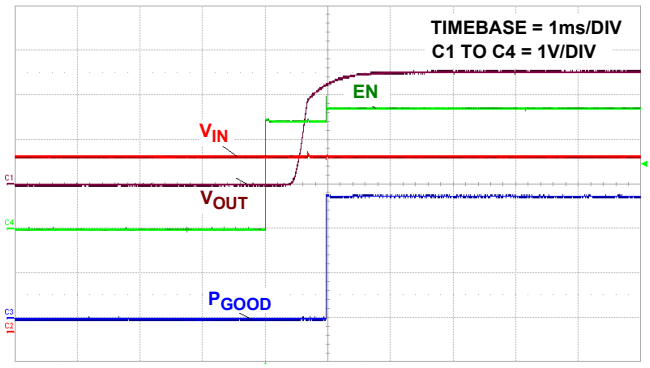


FIGURE 23. +25°C START-UP WITH ENABLE, V_{IN} = 4V, V_{OUT} = 2.5V, I_{OUT} = 0.1A

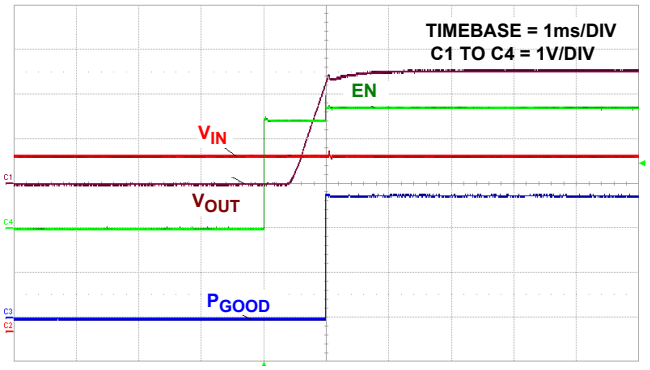


FIGURE 24. +25°C START-UP WITH ENABLE, V_{IN} = 4V, V_{OUT} = 2.5V, I_{OUT} = 1.5A

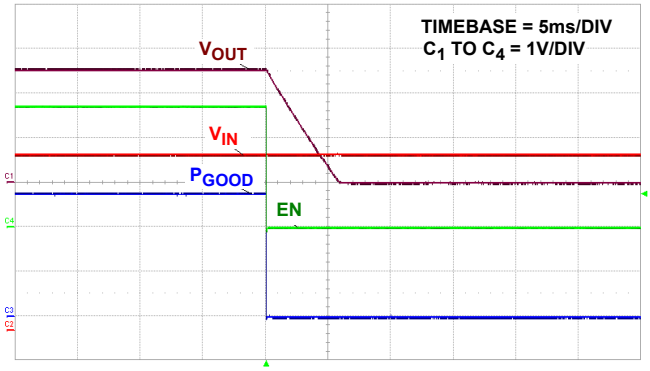


FIGURE 25. +25°C SHUTDOWN WITH ENABLE, V_{IN} = 4V, V_{OUT} = 2.5V, I_{OUT} = 0.1A

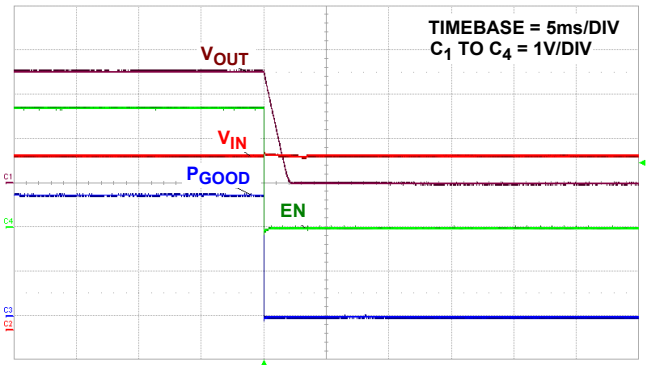


FIGURE 26. +25°C SHUTDOWN WITH ENABLE, V_{IN} = 4V, V_{OUT} = 2.5V, I_{OUT} = 1.5A

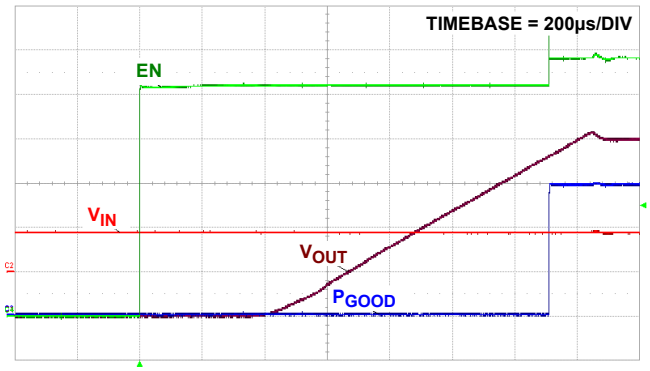


FIGURE 27. +25°C PROPAGATION DELAY, V_{IN} = 4.5V, V_{OUT} = 4V, I_{OUT} = 1.5A, EN 50% TO V_{OUT} 5%

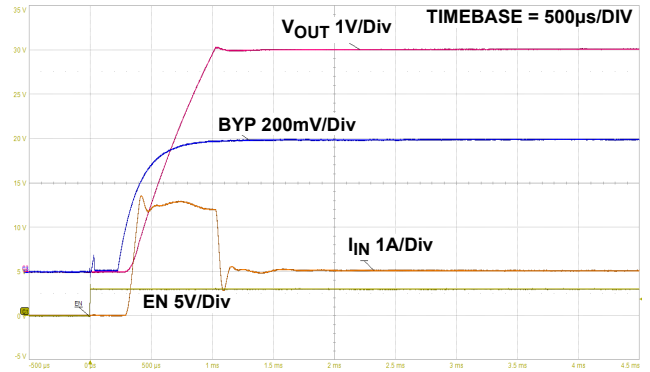


FIGURE 28. Soft-Start with BYP CAP = 0.2µF and EN to V_{OUT} Delay with VCCX CAP = 0.1µF, V_{IN} = 6.5V, V_{OUT} = 5V, R_L = 5Ω, C_{OUT} = 220µF, ROCP = 300Ω

Typical Operating Performance (Continued)

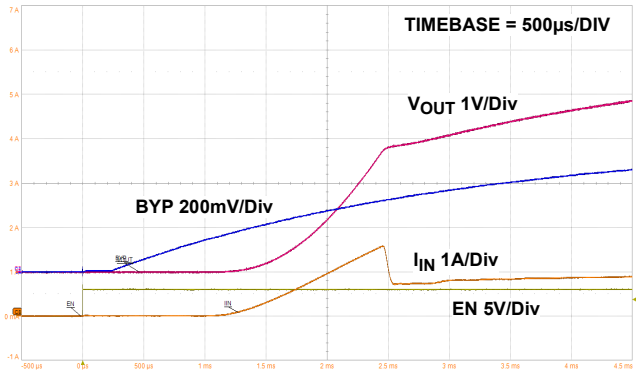


FIGURE 29. Soft-Start with BYP CAP = 1.9µF and EN to V_{OUT} Delay with VCCX CAP = 0.1µF, V_{IN} = 6.5V, V_{OUT} = 5V, RL = 5Ω, C_{OUT} = 220µF, ROCP = 300Ω

Applications Information

Input Voltage Requirements

This RH LDO works from a V_{IN} in the range of 4.0V to 13.2V. The input supply can have a tolerance of as much as ±10% for conditions noted in the specification table. The minimum assured input voltage is 4.0V. However, due to the nature of an LDO, V_{IN} must be some margin higher than the output voltage plus dropout at the maximum rated current of the application if active filtering (PSRR) is expected from V_{IN} to V_{OUT}. The Dropout specification of this family of LDOs has been generously specified in order to allow design for efficient operation.

External Capacitor Requirements

GENERAL GUIDELINES

External capacitors are required for proper operation. Careful attention must be paid to layout guidelines and selection of capacitor type and value to ensure optimal performance.

OUTPUT CAPACITORS

It is recommended to use a combination of tantalum and ceramic capacitors to achieve a good volume to capacitance ratio. The recommended combination is a 2x100µF 60mΩ rated, KEMET T541 series tantalum capacitor, in parallel with a 0.1µF MIL-PRF-49470 ceramic capacitor to be connected to V_{OUT} and ground pins of the LDO with PCB traces no longer than 0.5cm.

INPUT CAPACITORS

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Current Limit Protection

The RH LDO incorporates protection against overcurrent due to any short or overload condition applied to the output pin. The current limit circuit performs as a constant current source when the output current exceeds the current limit threshold, which can be adjusted by means of a resistor connected between the OCP pin and GND. If the short or overload condition is removed from V_{OUT}, then the output returns to normal voltage mode regulation. In the event of an overload condition, the LDO begins to cycle on and off due to the die temperature exceeding thermal fault condition. However, you may never witness thermal cycling if the heatsink used for the package can keep the die temperature below the limits specified for thermal shutdown. The R_{OCP} can be calculated using Equation 1:

$$R_{OCP} = \frac{762.8}{I_{OCP} - (1.382E\text{-}03 \bullet V_{IN}) - (2.629E\text{-}04 \bullet T_A) + 4.493E\text{-}02} \quad \text{(EQ. 1)}$$

where:

R_{OCP} = The OCP setting resistor in ohms.

V_{IN} = Supply voltage in volts.

I_{OCP} = The required OCP threshold in amps.

T_A = The ambient temperature in °C.

ESD Clamps

The ESD_CL_12V ESD clamps break down at nominally 17V. The ESD_RC_7V clamps break down at nominally 7.5V with a tolerance of ±10%. The PG pin has a diode to GND. The VOUT pin has a diode to VIN (see "Pin Descriptions" on page 4).

Soft-Start

Typically, soft-start is achieved by means of the charging time constant of the BYP pin. The capacitor value on the pin determines the time constant and can be calculated using Equation 2:

$$t_{SSbyp} = (3.3338E\text{-}6 \times C_{BYP}) + (9.5725E\text{-}8 \times T_A) - 9.2628E\text{-}6 \quad \text{(EQ. 2)}$$

where:

t_{SSbyp} = C_{BYP}-limited soft-start time in seconds.

C_{BYP} = Bypass capacitance in nF.

T_A = Ambient temperature in °C.

A low current limit and large output capacitance can cause startup to be slower than anticipated. Estimate the OCP-limited startup time with Equation 3. The actual startup time is either t_{SSbyp} or t_{SSOCP}, whichever is larger. See Figure 28 for an example of OCP-limited startup time. See Figure 29 for an example of C_{BYP} limited startup time.

$$t_{SSOCP} = C_{OUT}\frac{V_{OUT}}{I_{OCP} - I_{LOAD}} \quad \text{(EQ. 3)}$$

where:

t_{SSOCP} = OCP-limited startup time in microseconds

C_{OUT} = output capacitance in µF

V_{OUT} = target output voltage

I_{OCP} = The programmed OCP threshold in amps. (from Equation 1)

I_{LOAD} = Any load on VOUT in amps. If it is a resistive load, use $0.5*V_{OUT}/R_{LOAD}$.

COMP Pin

This pin helps compensate the device for various load conditions. For 4.0V < V_{IN} < 6.0V use R_{COMP} = 40k and C_{COMP} = 1nF. For 6V < V_{IN} < 13.2V use R_{COMP} = 40k and C_{COMP} = 4.7nF. The maximum current of the COMP pin when shorted to GND is 160µA.

Undervoltage Lockout

The undervoltage lockout function detects when VCCX exceeds 3.2V. When that level is reached, the LDO feedback loop is closed and the LDO can begin regulating. This is achieved by freeing the BYP net to charge up and act as a reference voltage to the EA. Prior to that happening, the LDO Power PMOS device is clamped off.

Bottom Metal Electrical Potential

The package bottom metal is electrically isolated and unbiased. The bottom metal may be electrically connected to any potential, which offers the best thermal path through conductive mounting materials (such as conductive epoxy or solder) or can be left unbiased through the use of electrically nonconductive mounting materials (nonconductive epoxy, Sil-pad, kapton film, etc.).

Bottom Metal Mounting Guidelines

The package bottom is a solderable metal surface. The following JESD51-5 guidelines can be used to mount the package:

- Place a thermal land on the PCB under the bottom metal.
- The land should be approximately the same size to 1mm larger than the 0.19inx0.41in bottom metal.
- Place an array of thermal vias below the thermal land.
- Via array size: ~4 x 9 = 36 thermal vias
- Via diameter: ~0.3mm drill diameter with plated copper on the inside of each via.
- Via pitch: ~1.2mm.

Vias should drop to and contact as much buried metal area as feasible to provide the best thermal path.

Thermal Fault Protection

If the die temperature exceeds +170°C (typical), the output of the LDO shuts down until the die temperature can cool down to +150°C (typical). The level of power combined with the thermal impedance of the package (θ_{JC} of 5°C/W for the 16 Ld CDFP package) determine if the junction temperature exceeds the thermal shutdown temperature specified in the specification table (see "Bottom Metal Mounting Guidelines" on page 16).

Package Characteristics

Weight of Packaged Device

0.59 Grams (typical)

Lid Characteristics

Finish: Gold
Potential: Connected to Pin 13 (GND)
Case Isolation to Any Lead: $20 \times 10^9 \Omega$ (minimum)

Die Characteristics

Die Dimensions

2819µm x 5638µm (111 mils x 222 mils)
Thickness: 304.8µm ±25.4µm (12.0 mils ±1 mil)

Interface Materials

GLASSIVATION

Type: Silicon Oxide and Silicon Nitride
Thickness: 0.3µm ±0.03µm to 1.2µm ±0.12µm

TOP METALLIZATION

Type: AlCu (99.5%/0.5%)
Thickness: 2.7µm ±0.4µm

SUSTRATE

Type: Silicon

BACKSIDE FINISH

Silicon

Assembly Related Information

SUBSTRATE POTENTIAL

Ground

Additional Information

WORST CASE CURRENT DENSITY

$< 2 \times 10^5$ A/cm^2

TRANSISTOR COUNT

1074

PROCESS

0.6µm BiCMOS Junction Isolated

Metallization Mask Layout

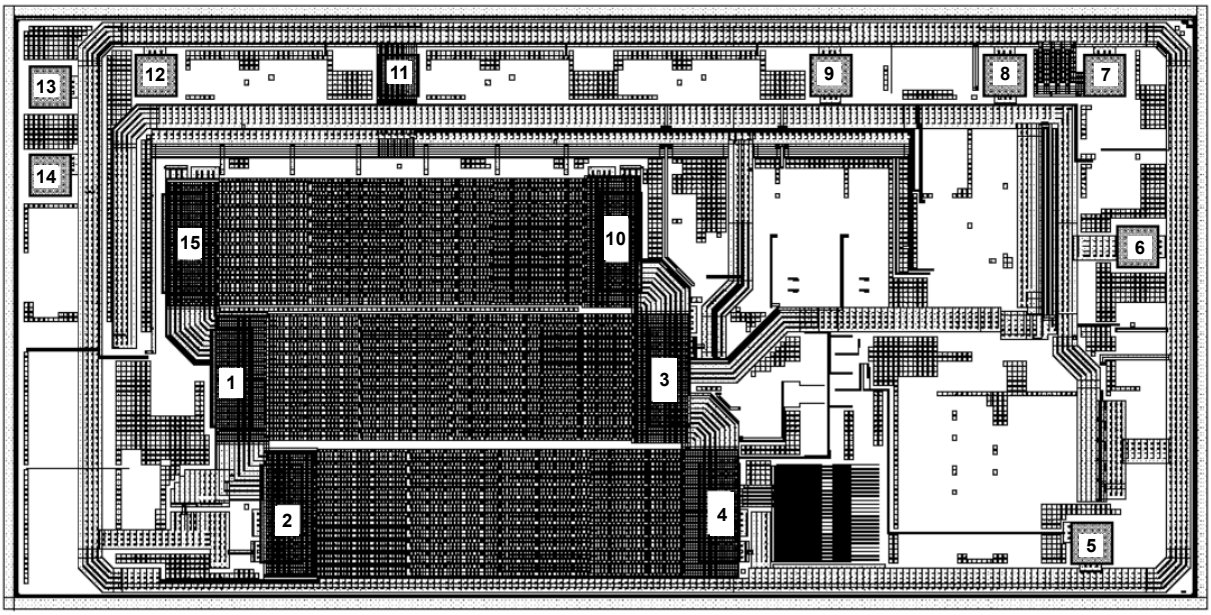


TABLE 1. DIE LAYOUT X-Y COORDINATES

PAD	X	Y	DX	DY	PIN NAME
1	1019	1021	185	450	VOUT
2	1249	390	185	449	VOUT
3	3070	1030	185	450	VIN
4	3300	399	185	450	VIN
5	5037	256	185	185	OCP
6	5253	1635	185	185	VCC
7	5099	2436	185	185	PG
8	4635	2436	185	185	TMODE
9	3824	2436	185	185	COMP
10	2840	1660	185	450	VIN
11	1799	2436	185	185	GND
12	668	2436	185	185	EN
13	168	2381	185	185	ADJ
14	168	1972	185	184	BYP
15	789	1652	185	450	VOUT

Revision History

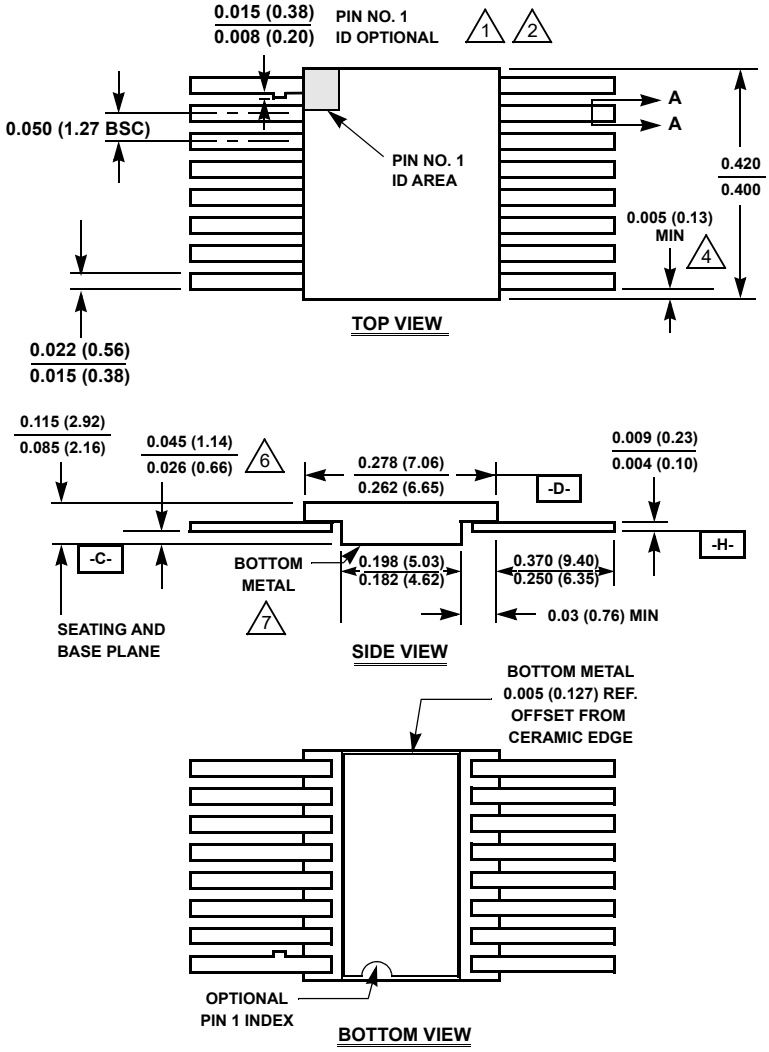
The revision history provided is for informational purposes only and is believed to be accurate, however, not warranted. Please go to the web to make sure that you have the latest revision.

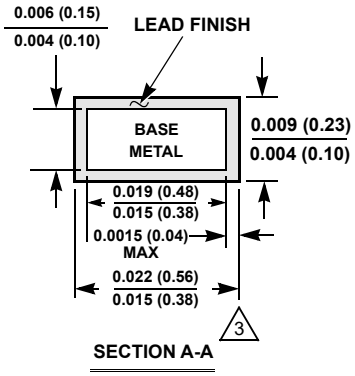
DATE	REVISION	CHANGE
Feb 9, 2023	8.03	Removed related literature section. Added Figures 28 and 29. Updated the Soft-start section.
Sep 17, 2020	8.02	Changed ESD Circuit in pin description table for Pin 6,7 from Circuit 2 to N/A.
Mar 19, 2020	8.01	Updated Pad 8 pin name in Table 1 (changed from NC to TMODE).
Jan 31, 2020	8.00	Reformatted Radiation Feature bullets. Updated Ordering information table by fixing part numbers, added radiation column, and updating Note 4 and adding Note 3. Removed Table 1. Removed Radiation Information section on page 5 along with Notes 7 and 11. Updated disclaimer.
Feb 11, 2019	7.00	Added ISL73052SEH part information throughout document. Updated Features note. Added Notes 3 and 4. Removed 100k RAD column from LDR Post Radiation Characteristics table on page 9. Removed About Intersil section. Updated Disclaimer.
Oct 25, 2016	6.00	Updated Related Literature section. Updated Ordering information table and Note 2. Added Figure 22 on page 13.
Nov 5, 2015	5.00	Updated Equation 1 on page 15.
Aug 31, 2015	4.00	Updated Equation 2 on page 16. Thermal Information table on page 5: Removed reference to TB493.
Dec 4, 2014	3.00	Updated Figure 1 for clarity. Added ESD Ratings to “Absolute Maximum Ratings” on page 5.
July 11, 2014	2.00	1) Pages 7 thru 10 - Added Radiation tables 2) Page 15 - Added paragraph for Soft Start: " The Soft-start is achieved by means of the charging time constant of the BYP pin. The capacitor value on the pin determines the time constant and can be calculated using Equation 2. Ts = (2961xCs) -121] EQ. 2 Where Ts = soft-start time in ms, and Cs = BYPASS capacitor in nF. 3) Page 15 - Changed in 1st paragraph, 2nd sentence “(θ_{JC} of 5°C/W....” to “(θ_{JC} of 4.5°C/W.....” 4) Page 17 - Rotated and changed pad numbers on Metallization Mask layout Updated Die layout X-Y Coordinates table
Sep19, 2013	1.00	Recommended operating conditions table on page 5, changed VOUT min from 2.5V to 0.6V, and added Note 12. Electrical spec on page 6, Output Noise Voltage, changed test conditions from I_{LOAD} = 10mA, BW = 300Hz < f <300 kHz, BYPASS to GND capacitor = 0.2µF to V_{IN} = 4.1V, V_{OUT} = 2.5V, I_{LOAD} = 10mA, BW = 100Hz < f <100 kHz, BYPASS to GND capacitor = 0.2µF. Figure 19 on page 11, changed the value from I_{OUT} = 0.2A to I_{OUT} = 1.5A. Figure 20 on page 11, changed the values from V_{IN} = 4V to V_{IN} = 11V and V_{OUT} = 2.5V to V_{OUT} = 10V.
May 29, 2013	0.00	Initial Release

Package Outline Drawing

For the most recent package outline drawing, see K16.E.

K16.E
16 Lead Ceramic Metal Seal Flatpack Package
Rev 1, 1/12





NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of the tab dimension do not apply.
3. The maximum limits of lead dimensions (section A-A) shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
4. Measure dimension at all four corners.
5. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
6. Dimension shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
7. The bottom of the package is a solderable metal surface.
8. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
9. Dimensions: INCH (mm). Controlling dimension: INCH.

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