ISL75055M

Radiation Tolerant 3A Source and Sink DDR Terminator/LDO with Buffered Reference

Description

The ISL75055M is a radiation tolerant 0.75V to 5.5V input, 3A sourcing and sinking low dropout linear regulator designed for powering the VTT termination rail of DDR memory modules. A buffered reference amplifier provides an accurate VREF reference supply for the DDR. Individual adjustable overcurrent protection (OCP) for sourcing and sinking allows the current limit of the LDO to be configured down to 300mA.

The ISL75055M features external error amplifier inputs to set VDDQ/2 as the reference voltage in DDR applications. It also features an internal 0.5V reference for standard LDO applications.

Separate VCC bias and LDO VIN pins, combined with a very low dropout allows minimal internal losses while maintaining highly accurate output regulation.

The ISL75055M is offered in a 48 lead Thin Plastic Quad Flatpack Exposed Pad Package (TQFP-EP) package and operates across the full military temperature range of -55°C to +125°C.

Applications

- DDR, DDR2, DDR3 and DDR4 memory VTT termination rail and buffered VREF reference
- Low noise supply rail for FPGA, DSP and ASIC
- General purpose LDO rails
- Two quadrant supply for sourcing or sinking up to 3A of current

Features

- Qualified to Renesas Rad Tolerant Screening and QCI Flow (R34TB0004EU)
- Separate 2.7V to 5.5V bias rail and 0.75V to 5.5V LDO input rail
- 3A sourcing and sinking low dropout regulator with 600µV dead band crossover
- Internal buffered reference amplifier provides VREF = VDDQ/2 for DDR applications
- Internal 0.5V voltage reference for standard LDO applications
- Low 122mV typical dropout at 3A sourcing in DDR4 configuration
- Individual OCP setting for source and sink from 300mA to 3A
- Optional LDO and buffer output discharge function
- Externally adjustable soft-start
- TID Radiation Lot Acceptance Testing (RLAT) (LDR: ≤10mrad(Si)/s)
  - ISL75055M30NEZ: 30krad(Si)
  - ISL75055M50NEZ: 50krad(Si)
- SEE Characterization
  - No DSEE for VIN = 6.2V, VCC = 6.9V at 46MeV•cm^2/mg
  - VOUT and BUF-OUT SET < 2% at 46MeV•cm^2/mg
  - |VOUT - BUF-OUT| SET < 40mV at 46MeV•cm^2/mg
  - SEFI < 0.18µm^2 at 46MeV•cm^2/mg

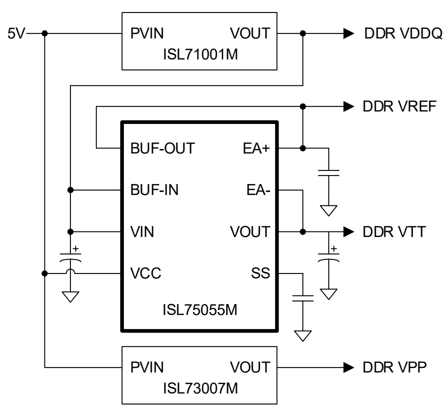


Figure 1. DDR4 Power Management Block Diagram

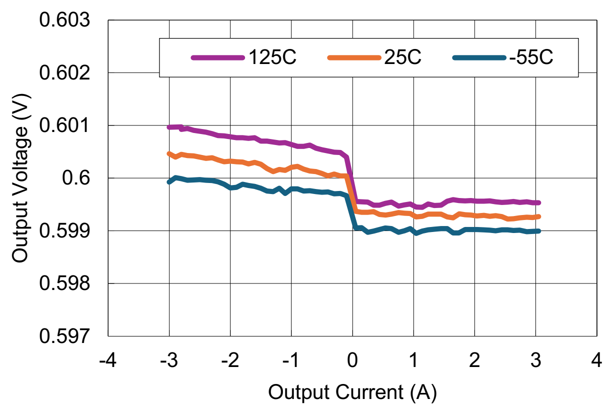


Figure 2. DDR4 Output Voltage Regulation

Contents

1. Overview

1.1 Typical Applications

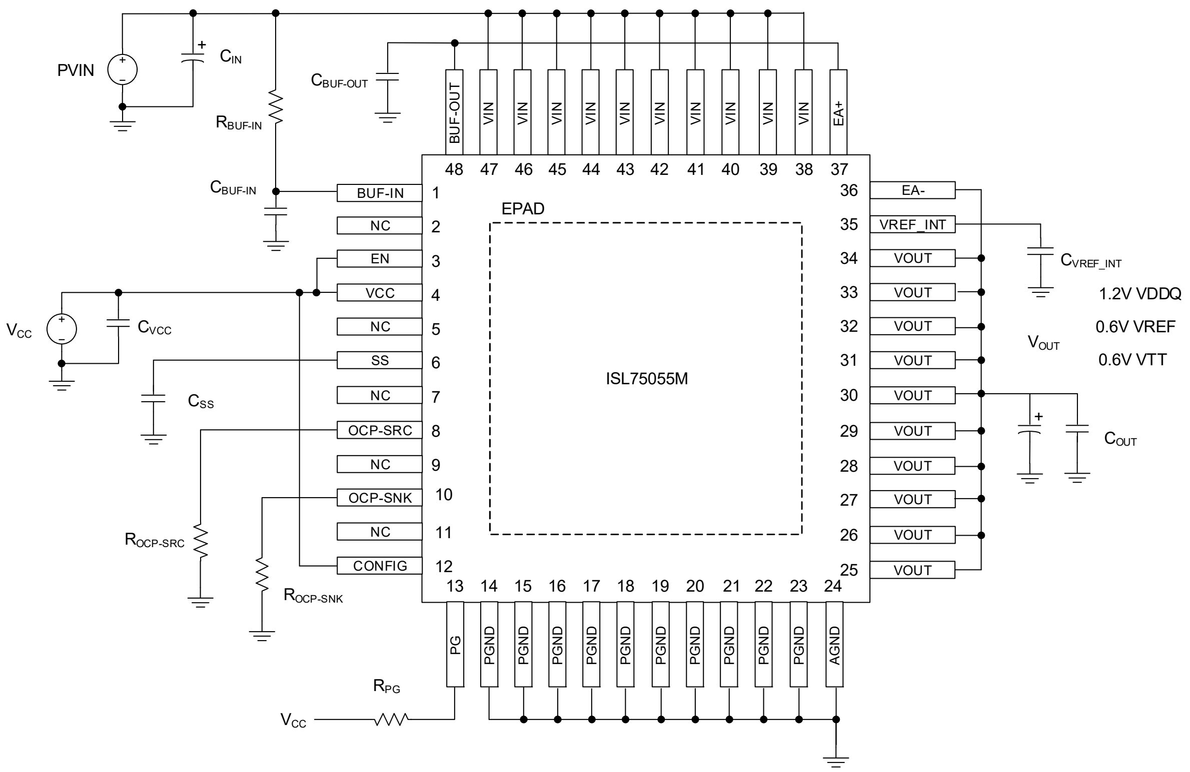


Figure 3. Typical Application Circuit: VTT Rail for DDR4 Memory Module

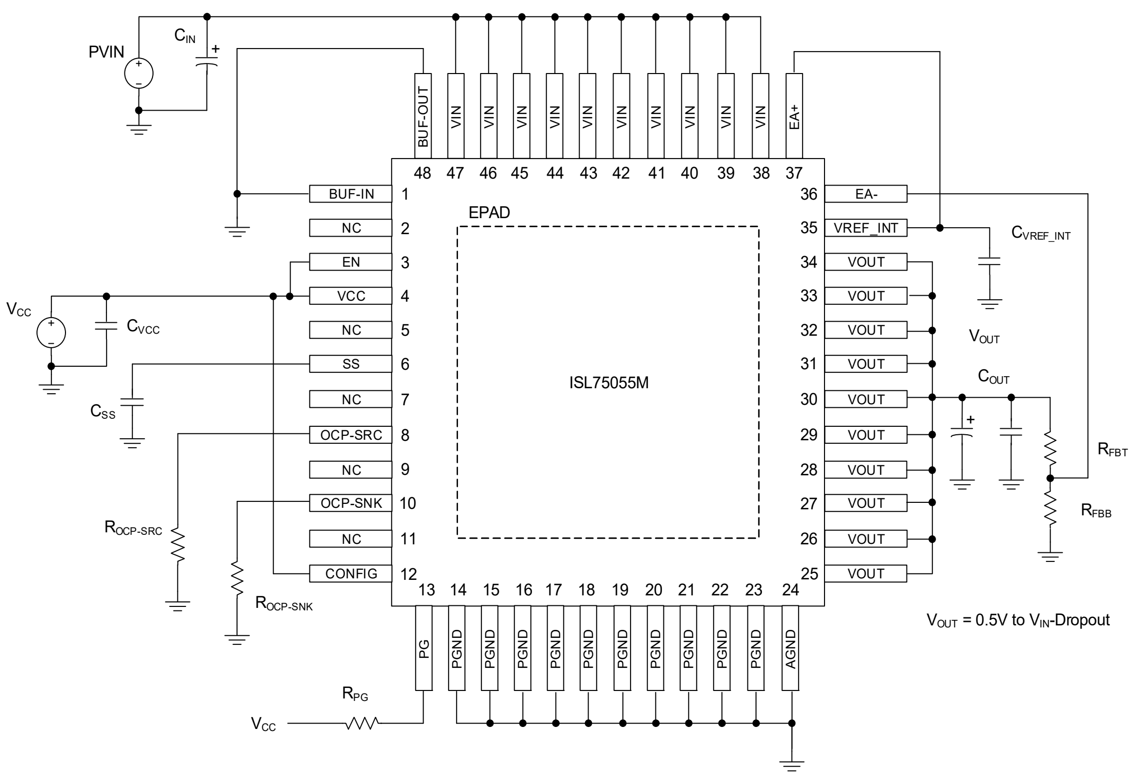


Figure 4. Typical Application Circuit: Standard LDO Output Applications

1.2 Block Diagram

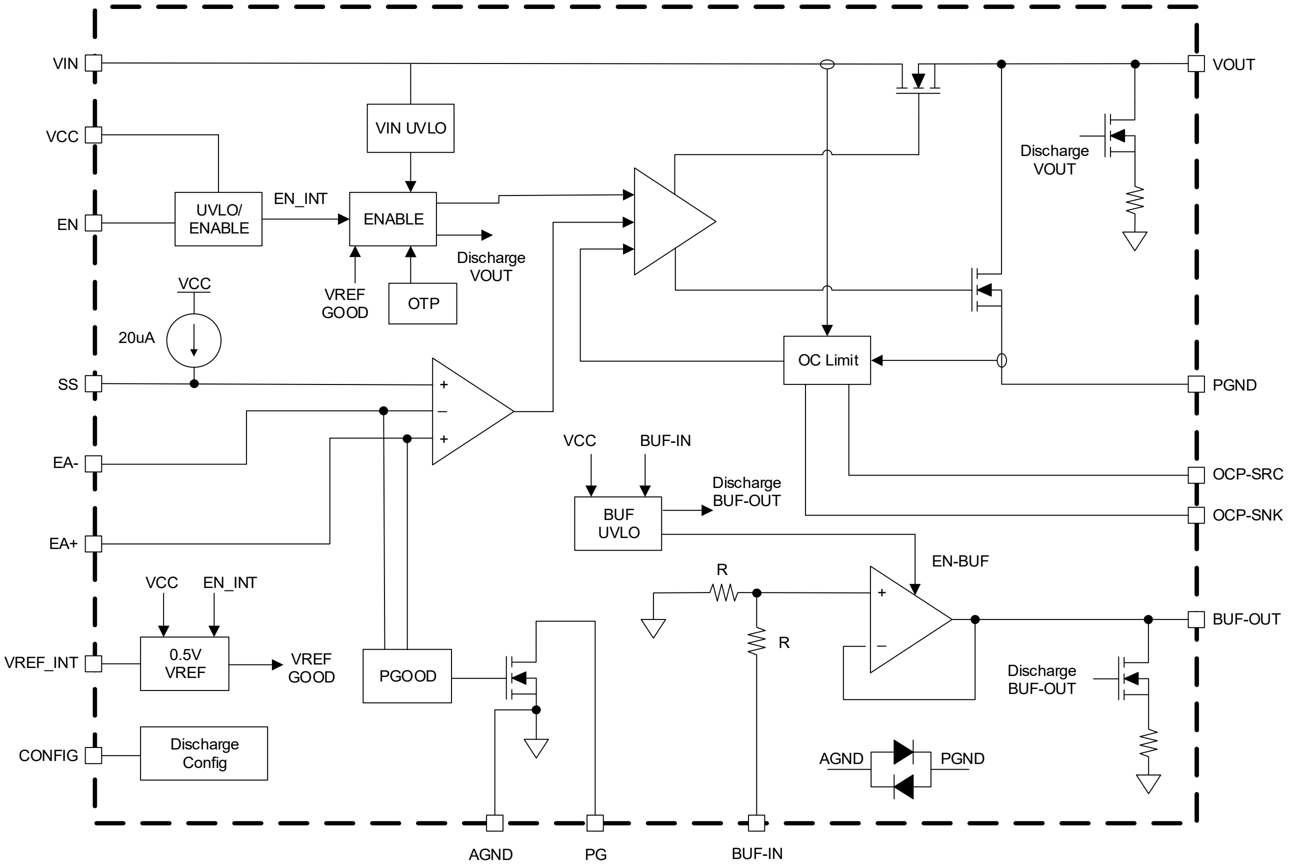
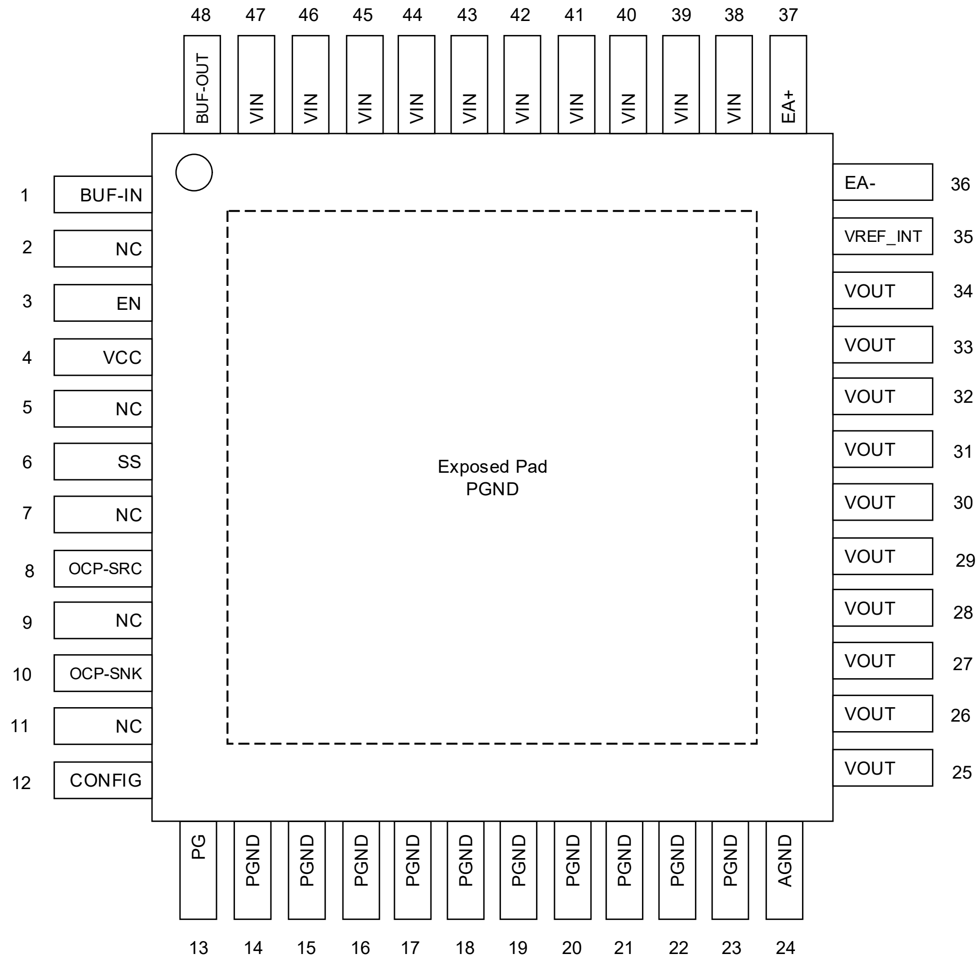


Figure 5. Functional Block Diagram

2. Pin Information

2.1 Pin Assignments



Note: Pin 1 indicator on package

Figure 6. Pin Assignments - Top View

2.2 Pin Descriptions

Pin Number	Pin Name	ESD Circuit	Description
1	BUF-IN	1	Buffered reference input voltage VDDQ for DDR applications. An internal voltage divider outputs 50% of the input signal (VDDQ/2) on BUF-OUT pin. When VIN directly supplies BUF-IN, a 1kΩ/1µF filter is recommended at the input of BUF-IN for SEE mitigation.
2	NC	-	No internal connection.
3	EN	2	Enable pin for the LDO output.
4	VCC	1	Analog bias input. Place a minimum 1µF capacitor on this pin to AGND for filtering.
5	NC	-	No internal connection.
6	SS	1	Soft-start pin. Place a capacitor on this pin for soft-start power up. A 20µA current source charges capacitor for ramping the reference of the error amplifier for a controlled start-up.

Pin Number	Pin Name	ESD Circuit	Description
7	NC	-	No internal connection.
8	OCP-SRC	1	Sourcing Overcurrent Protection setting pin. A resistor on this pin to AGND sets the Sourcing OCP level from 300mA to 3A. Short this pin to AGND for 4A typical sourcing OCP level.
9	NC	-	No internal connection.
10	OCP-SNK	1	Sinking Overcurrent Protection setting pin. A resistor on this pin to AGND sets the Sinking OCP level from 300mA to 3A. Short this pin to AGND for 4.1A typical sinking OCP level.
11	NC	-	No internal connection.
12	CONFIG	1	LDO VOUT and BUF-OUT discharge control pin. When low, discharge function disabled. When high, discharge function enabled. Internal switch discharges VOUT when EN = low. Internal switch discharges BUF-OUT when BUF-IN is below BUF-IN UVLO threshold.
13	PG	1	Open-drain power-good indicator pin. Place a resistor from PG to VCC. When VOUT is in overvoltage or undervoltage, PG pin pulls low.
14 15 16 17 18 19 20 21 22 23	PGND	3	LDO power ground connection. Connect common to AGND pin.
24	AGND	3	Analog ground pin.
25 26 27 28 29 30 31 32 33 34	VOUT	1	LDO output pin. Refer to Output Capacitance for more information on output capacitor selection.
35	VREF_INT	1	Internal 500mV reference. Place a 0.1µF ceramic capacitor on this pin to AGND.
36	EA-	1	Inverting input to the error amplifier.
37	EA+	1	Non-inverting input to the error amplifier. Connect to VREF_INT for the 500mV internal reference or connect to BUF-OUT for DDR applications.

Pin Number	Pin Name	ESD Circuit	Description
38	VIN	1	LDO input voltage. A single 150µF tantalum capacitor and 2x 10µF ceramic capacitor is recommended close to VIN and PGND connections.
39			
40			
41			
42			
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44			
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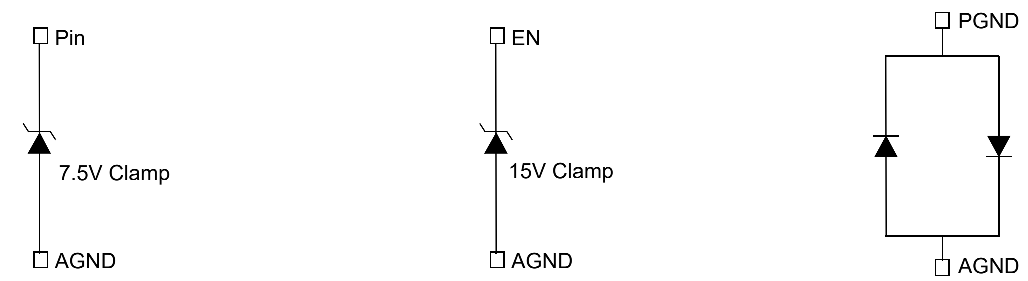
46			
47			
48	BUF-OUT	1	Buffered reference output. Provides a voltage equalt to 50% of BUF-IN (VDDQ/2) for DDR applications. This pin can source or sink up to 10mA. Output is stable across a capacitance range of 100nF to 2.2µF. A minimum of 1uF to AGND is recommended for SEE mitigation. Buffered reference output is independent of EN input and active when BUF-IN is above 0.78V.
EPAD	PGND	3	The EPAD is connected to the substrate of the die. Tie EPAD common to the PGND connection. Connect EPAD to PCB on multiple layers with thermal vias underneath the EPAD to maximize thermal performance.



Circuit 1 Circuit 2 Circuit 3

3. Specifications

3.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
VCC to AGND	-0.3	+6.5	V
VCC to AGND[1]	-0.3	+6.5	V
VIN to PGND	-0.3	+6.5	V
VIN to PGND[1]	-0.3	+6.2	V
VOUT to PGND	- 0.3	VIN + 0.3	V
AGND to PGND	-0.3	+0.3	V
All Other Pins	AGND - 0.3	VCC + 0.3	V
Junction Temperature	-55	+150	°C
Storage Temperature	-65	+150	°C
Human Body Model (Tested per MIL-STD-883 TM3015.7)	-	2	kV
Charged Device Model (Tested per JS-002-2022)	-	1	kV
Latch-Up (Tested per JESD-78E; Class 2, Level A) at 125°C	-	±100	mA

1. Tested under a heavy ion environment at LET = 46MeV•cm^2/mg at 125°C.

3.2 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
VCC Voltage	+2.7	+5.5	V
VIN Voltage	+0.75	+5.5	V
BUF-IN	+1.0	+3.3	V
EN, CONFIG, PG	0	VCC	V
VOUT voltage	0	Limited by VIN-VOUT and VCC-VOUT Dropout Specifications	V
EA+ voltage	0	+1.65	V
Current on VOUT	-3	+3	A
Ambient Temperature	-55	+125	°C

3.3 Plastic Package Outgas Testing

Specification (Tested per ASTM E595, 1.5)	Value	Unit
Total Mass Lost[1]	0.04	%
Collected Volatile Condensible Material[1]	<0.01	%
Water Vapor Recovered	0.01	%

1. Outgassing results meet NASA requirements of total mass loss <1% and collected volatile condensible material <0.1%.

3.4 Thermal Information

Parameter	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance	48Ld Plastic eTQFP	θ_{JA}[1]	Junction to ambient	25	°C/W
		θ_{JC}[2]	Junction to case	2.0	°C/W

1. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.
2. For θ_{JC}, the case temperature location is the center of the metal exposed pad on the package underside.

3.5 Electrical Specifications

3.5.1 DC Electrical Specifications

Unless otherwise specified: V_{CC} = 2.7V to 5.5V; V_{IN} = 0.75V to 5.5V; EN = V_{CC}; C_{OUT} = 150µF + 2x 10µF; OCP_SRC and OCP_SNK = AGND; T_A = 25°C. **Boldface limits apply across the operating temperature range, -55°C to +125°C by characterization with production testing at +25°C; over a total ionizing dose of 30krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL75055M30NEZ); or over a total ionizing dose of 50krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL75055M50NEZ).**

Parameter	Symbol	Test Conditions	Temperature	Min	Typ[1]	Max	Unit
Power Supply							
VCC Internal UVLO Rising Threshold	VCC_{UVLO_R}	V_{IN} = 3.3V; V_{OUT} = 0.5V; I_{OUT} = 0A	-55 to +125°C	**2.54**	2.62	**2.69**	V
VCC Internal UVLO Falling Threshold	VCC_{UVLO_F}	V_{IN} = 3.3V; V_{OUT} = 0.5V; I_{OUT} = 0A	-55 to +125°C	**2.44**	2.5	**2.6**	V
VCC UVLO Hysteresis	VCC_{UVLO_H}	-	-55 to +125°C	**90**	115	**140**	mV
VCC Enabled Supply Current	I_{VCC}	V_{CC} = 2.7V, V_{IN} = 0.75V, I_{OUT} = 0A; V_{CC} = 5.5V, V_{IN} = 5.5V, -3A < I_{OUT} < 3A; EA+ = VREF_INT; BUF-IN = 1V	-55 to +125°C	**2.7**	5	**7**	mA
VCC Disabled Supply Current	I_{VCC_SHDN1}	EN = 0V; V_{CC} = 5.5V; BUF-IN = 0V; EA+ = VREF_INT	-55 to +125°C	**120**	210	**300**	µA
	I_{VCC_SHDN2}	EN = 0V; V_{CC} = 5.5V; BUF-IN = 1V; EA+ = VREF_INT	-55 to +125°C	**310**	690	**1000**	µA
VIN Supply Current	I_{VIN}	EN = V_{CC}; V_{IN} = 3.3V; I_{OUT} = 0A; EA+ = VREF_INT	-55 to +125°C	**-**	5	**-**	µA
VIN UVLO Rising	VIN_{UVLO_R}	V_{CC} = 2.7V; BUF-IN = 1V; I_{OUT} = 0A	-55 to +125°C	**450**	472	**490**	mV
VIN UVLO Falling	VIN_{UVLO_F}	V_{CC} = 2.7V; BUF-IN = 1V; I_{OUT} = 0A	-55 to +125°C	**400**	425	**450**	mV
VIN UVLO Hysteresis	VIN_{UVLO_H}	-	-55 to +125°C	**10**	47	**70**	mV

Unless otherwise specified: V_{CC} = 2.7V to 5.5V; V_{IN} = 0.75V to 5.5V; EN = V_{CC}; C_{OUT} = 150µF + 2x 10µF; OCP_SRC and OCP_SNK = AGND; T_A = 25°C. **Boldface limits apply across the operating temperature range, -55°C to +125°C by characterization with production testing at +25°C; over a total ionizing dose of 30krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL75055M30NEZ); or over a total ionizing dose of 50krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL75055M50NEZ).** (Cont.)

Parameter	Symbol	Test Conditions	Temperature	Min	Typ[1]	Max	Unit
Reference Voltage							
VREF_INT Voltage	V_{REF}	V_{IN} = 3.3V; EA+ = VREF_INT Established by Total Output Accuracy specifications	-55°C	495	500	505	mV
			+25°C	495	500	505	mV
			+125°C	492.5	500	507.5	mV
			+25°C (Post Rad)	492.5	500	507.5	mV
Error Amplifier							
Error Amplifier VOS	EA_VOS	(EA- to EA+); V_{CC} = 3.3V; V_{IN} = 0.8V; EA+ = VREF_INT; I_{OUT} = 0A	+25°C	-2.2	0	2.2	mV
		(EA- to EA+); 2.7V<V_{CC}<5.5V; 0.75V<V_{IN}<5.5V; EA+ = VREF_INT; -3A<I_{OUT}<3A; Includes Regulator Dead-Band	-55 to +125°C	**-2.2**	0	**2.2**	mV
Regulator Dead-Band	DBand	Change in Error Amp VOS from I_{OUT} = -1mA to I_{OUT} = 1mA	-55°C	250	600	850	µV
			+25°C	300	600	900	µV
			+125°C	300	600	1000	µV
			+25°C (Post Rad)	300	600	900	µV
EA+; EA- Input Bias Current	I_EA+; I_EA-	EA+ = EA- = 0.5V; V_{CC} = 3.3V; V_{IN} = 3.3V	-55 to +125°C	-	-	**0.35**	µA
LDO VOUT							
Output Accuracy	VOUT%	0.75V < V_{IN} < 5.5V; EA+ = VREF_INT; V_{OUT} = 0.5V, 1.2V, 1.8V, 3.3V; -3A < I_{OUT} < 3A; V_{OUT} < V_{CC}-1.5V; V_{OUT}< V_{IN}-0.25V for V_{OUT} = 0.5V; V_{OUT}< V_{IN}-0.3V for all other V_{OUT}	-55°C	-1	-	1	%
			+25°C	-1	-	1	%
			+125°C	-1.5	-	1.5	%
			+25°C (Post Rad)	-1.5	-	1.5	%
Line Regulation	$VOUT_{LINE}$	0.75V < V_{IN} < 5.5V; EA+ = VREF_INT; V_{OUT} = 0.5V, 1.2V, 1.8V, 3.3V; I_{OUT} = 0A; V_{OUT}< V_{CC}-1.5V; V_{OUT} < V_{IN}-0.25V for V_{OUT} = 0.5V; V_{OUT} < V_{IN}-0.3V for all other V_{OUT}	-55 to +125°C	**-0.16**	-	**0.16**	%/V
Sourcing Load Regulation	V_{OUT_LOAD1}	V_{IN} = 0.75V and 5.5V; EA+ = VREF_INT; V_{OUT} = 0.5V, 1.2V, 1.8V, 3.3V; 0A < I_{OUT} < 3A; V_{OUT} < V_{CC}-1.5V; V_{OUT} < V_{IN}-0.25V for V_{OUT} = 0.5V; V_{OUT} < V_{IN}-0.3V for all other V_{OUT}	-55 to +125°C	**-0.15**	-	-	%/A
Sinking Load Regulation	V_{OUT_LOAD2}	V_{IN} = 0.75V and 5.5V; EA+ = VREF_INT; V_{OUT} = 0.5V, 1.2V, 1.8V, 3.3V; -3A < I_{OUT} < 0A; V_{OUT} < V_{CC}-1.5V; V_{OUT} < V_{IN}-0.25V for V_{OUT} = 0.5V; V_{OUT} < V_{IN}-0.3V for all other V_{OUT}	-55 to +125°C	-	-	**0.20**	%/A

Unless otherwise specified: V_{CC} = 2.7V to 5.5V; V_{IN} = 0.75V to 5.5V; EN = V_{CC}; C_{OUT} = 150µF + 2x 10µF; OCP_SRC and OCP_SNK = AGND; T_A = 25°C. **Boldface limits apply across the operating temperature range, -55°C to +125°C by characterization with production testing at +25°C; over a total ionizing dose of 30krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL75055M30NEZ); or over a total ionizing dose of 50krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL75055M50NEZ).** (Cont.)

Parameter	Symbol	Test Conditions	Temperature	Min	Typ[1]	Max	Unit
Output Accuracy DDR Configuration	V_DDR	V_{CC} = 2.75 - 5.5V; V_{IN} = BUF-IN = 2.5V; BUF-OUT = EA+; V_{OUT} = EA-; I_{OUT} = 0A, $I_{BUF-OUT}$ = 0mA	-55 to +125°C	**1.237**	1.25	**1.263**	V
		V_{CC} = 2.75 - 5.5V; V_{IN} = BUF-IN = 2.5V; BUF-OUT = EA+; V_{OUT} = EA-; I_{OUT} = -1A to +1A, $I_{BUF-OUT}$ = 0mA	-55 to +125°C	**1.237**	1.25	**1.263**	V
		V_{CC} = 2.75 - 5.5V; V_{IN} = BUF-IN = 2.5V; BUF-OUT = EA+; V_{OUT} = EA-; I_{OUT} = -3A to +3A, $I_{BUF-OUT}$ = 0mA	-55 to +125°C	**1.237**	1.25	**1.263**	V
	V_DDR2	V_{IN} = BUF-IN = 1.8V; BUF-OUT = EA+; V_{OUT} = EA-; I_{OUT} = 0A, $I_{BUF-OUT}$ = 0mA	-55 to +125°C	**0.891**	0.9	**0.909**	V
		V_{IN} = BUF-IN = 1.8V; BUF-OUT = EA+; V_{OUT} = EA-; I_{OUT} = -1A to +1A, $I_{BUF-OUT}$ = 0mA	-55 to +125°C	**0.891**	0.9	**0.909**	V
		V_{IN} = BUF-IN = 1.8V; BUF-OUT = EA+; V_{OUT} = EA-; I_{OUT} = -3A to +3A, $I_{BUF-OUT}$ = 0mA	-55 to +125°C	**0.891**	0.9	**0.909**	V
	V_DDR3	V_{IN} = BUF-IN = 1.5V; BUF-OUT = EA+; V_{OUT} = EA-; I_{OUT} = 0A, $I_{BUF-OUT}$ = 0mA	-55 to +125°C	**0.742**	0.75	**0.758**	V
		V_{IN} = BUF-IN = 1.5V; BUF-OUT = EA+; V_{OUT} = EA-; I_{OUT} = -1A to +1A, $I_{BUF-OUT}$ = 0mA	-55 to +125°C	**0.742**	0.75	**0.758**	V
		V_{IN} = BUF-IN = 1.5V; BUF-OUT = EA+; V_{OUT} = EA-; I_{OUT} = -3A to +3A, $I_{BUF-OUT}$ = 0mA	-55 to +125°C	**0.742**	0.75	**0.758**	V
	V_DDR3L	V_{IN} = BUF-IN = 1.35V; BUF-OUT = EA+; V_{OUT} = EA-; I_{OUT} = 0A, $I_{BUF-OUT}$ = 0mA	-55 to +125°C	**0.668**	0.675	**0.682**	V
		V_{IN} = BUF-IN = 1.35V; BUF-OUT = EA+; V_{OUT} = EA-; I_{OUT} = -1A to +1A, $I_{BUF-OUT}$ = 0mA	-55 to +125°C	**0.668**	0.675	**0.682**	V
		V_{IN} = BUF-IN = 1.35V; BUF-OUT = EA+; V_{OUT} = EA-; I_{OUT} = -3A to +3A, $I_{BUF-OUT}$ = 0mA	-55 to +125°C	**0.668**	0.675	**0.682**	V

Unless otherwise specified: V_{CC} = 2.7V to 5.5V; V_{IN} = 0.75V to 5.5V; EN = V_{CC}; C_{OUT} = 150µF + 2x 10µF; OCP_SRC and OCP_SNK = AGND; T_A = 25°C. **Boldface limits apply across the operating temperature range, -55°C to +125°C by characterization with production testing at +25°C; over a total ionizing dose of 30krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL75055M30NEZ); or over a total ionizing dose of 50krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL75055M50NEZ).** (Cont.)

Parameter	Symbol	Test Conditions	Temperature	Min	Typ[1]	Max	Unit
Output Accuracy DDR Configuration (cont.)	V_DDR4	V_{IN} = BUF-IN = 1.2V; BUF-OUT = EA+; V_{OUT} = EA-; I_{OUT} = 0A, $I_{BUF-OUT}$ = 0mA	-55 to +125°C	**0.594**	0.6	**0.606**	V
		V_{IN} = BUF-IN = 1.2V; BUF-OUT = EA+; V_{OUT} = EA-; I_{OUT} = -1A to +1A, $I_{BUF-OUT}$ = 0mA	-55 to +125°C	**0.594**	0.6	**0.606**	V
		V_{IN} = BUF-IN = 1.2V; BUF-OUT = EA+; V_{OUT} = EA-; I_{OUT} = -3A to +3A, $I_{BUF-OUT}$ = 0mA	-55 to +125°C	**0.594**	0.6	**0.606**	V
	BUF3V3	V_{IN} = BUF-IN = 3.3V; BUF-OUT = EA+; V_{OUT} = EA-; I_{OUT} = 0A, $I_{BUF-OUT}$ = 0mA	-55 to +125°C	**1.633**	1.65	**1.667**	V
		V_{IN} = BUF-IN = 3.3V; BUF-OUT = EA+; V_{OUT} = EA-; I_{OUT} = -1A to +1A, $I_{BUF-OUT}$ = 0mA	-55 to +125°C	**1.633**	1.65	**1.667**	V
		V_{IN} = BUF-IN = 3.3V; BUF-OUT = EA+; V_{OUT} = EA-; I_{OUT} = -3A to +3A, $I_{BUF-OUT}$ = 0mA	-55 to +125°C	**1.633**	1.65	**1.667**	V
	BUF1V0	V_{IN} = BUF-IN = 1.0V; BUF-OUT = EA+; V_{OUT} = EA-; I_{OUT} = 0A, $I_{BUF-OUT}$ = 0mA	-55 to +125°C	**0.495**	0.5	**0.505**	V
		V_{IN} = BUF-IN = 1.0V; BUF-OUT = EA+; V_{OUT} = EA-; I_{OUT} = -1A to +1A, $I_{BUF-OUT}$ = 0mA	-55 to +125°C	**0.495**	0.5	**0.505**	V
		V_{IN} = BUF-IN = 1.0V; BUF-OUT = EA+; V_{OUT} = EA-; I_{OUT} = -3A to +3A, $I_{BUF-OUT}$ = 0mA	-55 to +125°C	**0.495**	0.5	**0.505**	V
VCC Dropout Voltage[2]	VCC_DO	I_{OUT} = 3A; V_{OUT} = 3.3V; V_{IN} = 3.6V; V_{CC} = 0.99 x V_{OUT} + VCC_DO; BUF-IN = 1V; EA+ = VREF_INT	-55 to +125°C	-	-	**1.38**	V
VIN-VOUT Dropout Voltage LDO Configuration	VIN_DO	I_{OUT} = 1A; V_{OUT} = V_{IN} - VIN_DO; 2.7V<V_{CC}<5.5V; V_{IN} = 0.5V	-55°C	-	33	42	mV
			+25°C	-	40	50	mV
			+125°C	-	49	60	mV
			+25°C (Post Rad)	-	40	50	mV
		I_{OUT} = 2A; V_{OUT} = V_{IN} - VIN_DO; 2.7V<V_{CC}<5.5V; V_{IN} = 0.5V	-55°C	-	65	84	mV
			+25°C	-	80	100	mV
			+125°C	-	99	120	mV
			+25°C (Post Rad)	-	80	100	mV
		I_{OUT} = 3A; V_{OUT} = V_{IN} - VIN_DO; 2.7V<V_{CC}<5.5V; V_{IN} = 0.5V	-55°C	-	98	126	mV
			+25°C	-	121	145	mV
			+125°C	-	149	180	mV
			+25°C (Post Rad)	-	121	145	mV

Unless otherwise specified: V_{CC} = 2.7V to 5.5V; V_{IN} = 0.75V to 5.5V; EN = V_{CC}; C_{OUT} = 150µF + 2x 10µF; OCP_SRC and OCP_SNK = AGND; T_A = 25°C. **Boldface limits apply across the operating temperature range, -55°C to +125°C by characterization with production testing at +25°C; over a total ionizing dose of 30krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL75055M30NEZ); or over a total ionizing dose of 50krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL75055M50NEZ).** (Cont.)

Parameter	Symbol	Test Conditions	Temperature	Min	Typ[1]	Max	Unit
VIN-VOUT Dropout Voltage DDR Configuration	VIN_{DODDRA}	V_{CC} = 2.75V; BUF-IN = 2.5V; V_{IN} = 1.25V; V_{OUT} = V_{IN} - VIN_{DODDR}; I_{OUT} = 1A	-55°C	-	36	52	mV
			+25°C	-	44	60	mV
			+125°C	-	54	70	mV
			+25°C (Post Rad)	-	44	60	mV
	VIN_{DODDRB}	V_{CC} = 2.75V; BUF-IN = 2.5V; V_{IN} = 1.25V; V_{OUT} = V_{IN} - VIN_{DODDR}; I_{OUT} = 2A	-55°C	-	72	94	mV
			+25°C	-	88	110	mV
			+125°C	-	107	130	mV
			+25°C (Post Rad)	-	88	110	mV
	VIN_{DODDRC}	V_{CC} = 2.75V; BUF-IN = 2.5V; V_{IN} = 1.25V; V_{OUT} = V_{IN} - VIN_{DODDR}; I_{OUT} = 3A	-55°C	-	108	136	mV
			+25°C	-	132	155	mV
			+125°C	-	161	190	mV
			+25°C (Post Rad)	-	132	155	mV
	$VIN_{DODDR2A}$	V_{CC} = 2.7V; BUF-IN = 1.8V; V_{IN} = 0.9V; V_{OUT} = V_{IN} - VIN_{DODDR}; I_{OUT} = 1A	-55°C	-	34	52	mV
			+25°C	-	42	60	mV
			+125°C	-	52	70	mV
			+25°C (Post Rad)	-	42	60	mV

Unless otherwise specified: V_{CC} = 2.7V to 5.5V; V_{IN} = 0.75V to 5.5V; EN = V_{CC}; C_{OUT} = 150µF + 2x 10µF; OCP_SRC and OCP_SNK = AGND; T_A = 25°C. **Boldface limits apply across the operating temperature range, -55°C to +125°C by characterization with production testing at +25°C; over a total ionizing dose of 30krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL75055M30NEZ); or over a total ionizing dose of 50krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL75055M50NEZ).** (Cont.)

Parameter	Symbol	Test Conditions	Temperature	Min	Typ[1]	Max	Unit
VIN-VOUT Dropout Voltage DDR Configuration	$VIN_{DODDR2B}$	V_{CC} = 2.7V; BUF-IN = 1.8V; V_{IN} = 0.9V; V_{OUT} = V_{IN} - VIN_{DODDR}; I_{OUT} = 2A	-55°C	-	68	94	mV
			+25°C	-	83	110	mV
			+125°C	-	103	130	mV
			+25°C (Post Rad)	-	83	110	mV
	$VIN_{DODDR2C}$	V_{CC} = 2.7V; BUF-IN = 1.8V; V_{IN} = 0.9V; V_{OUT} = V_{IN} - VIN_{DODDR}; I_{OUT} = 3A	-55°C	-	102	136	mV
			+25°C	-	125	155	mV
			+125°C	-	155	190	mV
			+25°C (Post Rad)	-	125	155	mV
	$VIN_{DODDR3A}$	V_{CC} = 2.7V; BUF-IN = 1.5V; V_{IN} = 0.75V; V_{OUT} = V_{IN} - VIN_{DODDR}; I_{OUT} = 1A	-55°C	-	33	52	mV
			+25°C	-	41	60	mV
			+125°C	-	51	70	mV
			+25°C (Post Rad)	-	41	60	mV
	$VIN_{DODDR3B}$	V_{CC} = 2.7V; BUF-IN = 1.5V; V_{IN} = 0.75V; V_{OUT} = V_{IN} - VIN_{DODDR}; I_{OUT} = 2A	-55°C	-	67	94	mV
			+25°C	-	82	110	mV
			+125°C	-	102	130	mV
			+25°C (Post Rad)	-	82	110	mV
	$VIN_{DODDR3C}$	V_{CC} = 2.7V; BUF-IN = 1.5V; V_{IN} = 0.75V; V_{OUT} = V_{IN} - VIN_{DODDR}; I_{OUT} = 3A	-55°C	-	100	136	mV
			+25°C	-	124	155	mV
			+125°C	-	153	190	mV
			+25°C (Post Rad)	-	124	155	mV
	$VIN_{DODDR3LA}$	V_{CC} = 2.7V; BUF-IN = 1.35V; V_{IN} = 0.675V; V_{OUT} = V_{IN} - VIN_{DODDR}; I_{OUT} = 1A	-55°C	-	33	52	mV
			+25°C	-	41	60	mV
			+125°C	-	51	70	mV
			+25°C (Post Rad)	-	41	60	mV
	$VIN_{DODDR3LB}$	V_{CC} = 2.7V; BUF-IN = 1.35V; V_{IN} = 0.675V; V_{OUT} = V_{IN} - VIN_{DODDR}; I_{OUT} = 2A	-55°C	-	66	94	mV
			+25°C	-	82	110	mV
			+125°C	-	101	130	mV
			+25°C (Post Rad)	-	82	110	mV

Unless otherwise specified: V_{CC} = 2.7V to 5.5V; V_{IN} = 0.75V to 5.5V; EN = V_{CC}; C_{OUT} = 150µF + 2x 10µF; OCP_SRC and OCP_SNK = AGND; T_A = 25°C. **Boldface limits apply across the operating temperature range, -55°C to +125°C by characterization with production testing at +25°C; over a total ionizing dose of 30krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL75055M30NEZ); or over a total ionizing dose of 50krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL75055M50NEZ).** (Cont.)

Parameter	Symbol	Test Conditions	Temperature	Min	Typ[1]	Max	Unit
VIN-VOUT Dropout Voltage DDR Configuration	$VIN_{DODDR3LC}$	V_{CC} = 2.7V; BUF-IN = 1.35V; V_{IN} = 0.675V; V_{OUT} = V_{IN} - VIN_{DODDR}; I_{OUT} = 3A	-55°C	-	100	136	mV
			+25°C	-	123	155	mV
			+125°C	-	152	190	mV
			+25°C (Post Rad)	-	123	155	mV
	$VIN_{DODDR4A}$	V_{CC} = 2.7V; BUF-IN = 1.2V; V_{IN} = 0.6V; V_{OUT} = V_{IN} - VIN_{DODDR}; I_{OUT} = 1A	-55°C	-	33	52	mV
			+25°C	-	41	60	mV
			+125°C	-	50	70	mV
			+25°C (Post Rad)	-	41	60	mV
	$VIN_{DODDR4B}$	V_{CC} = 2.7V; BUF-IN = 1.2V; V_{IN} = 0.6V; V_{OUT} = V_{IN} - VIN_{DODDR}; I_{OUT} = 2A	-55°C	-	66	94	mV
			+25°C	-	81	110	mV
			+125°C	-	100	130	mV
			+25°C (Post Rad)	-	81	110	mV
	$VIN_{DODDR4C}$	V_{CC} = 2.7V; BUF-IN = 1.2V; V_{IN} = 0.6V; V_{OUT} = V_{IN} - VIN_{DODDR}; I_{OUT} = 3A	-55°C	-	99	136	mV
			+25°C	-	122	155	mV
			+125°C	-	151	190	mV
			+25°C (Post Rad)	-	122	155	mV
Adjustable OCP; Sourcing	$OCP+_{HIGH}$	V_{OUT} = 0V; V_{IN} = 2V; V_{CC} = 2.7V; $R_{OCP-SRC}$ = 3kΩ	-55 to +125°C	**2.7**	3.0	**3.5**	A
	$OCP+_{LOW}$	V_{OUT} = 0V; V_{IN} = 2V; V_{CC} = 2.7V; $R_{OCP-SRC}$ = 30kΩ	-55 to +125°C	**0.15**	0.3	**0.6**	A
Adjustable OCP; Sinking	$OCP-_{HIGH}$	V_{OUT} = 1V; V_{IN} = 2V; V_{CC} = 2.7V; $R_{OCP-SNK}$ = 3kΩ	-55 to +125°C	**-3.5**	-3.0	**-2.7**	A
	$OCP-_{LOW}$	V_{OUT} = 1V; V_{IN} = 2V; V_{CC} = 2.7V; $R_{OCP-SNK}$ = 30kΩ	-55 to +125°C	**-0.6**	-0.3	**-0.15**	A
Internal OCP; Sourcing	OCP+	V_{OUT} = 0V; V_{IN} = 2V; V_{CC} = 2.7V; $R_{OCP-SRC}$ = 0Ω	-55 to +125°C	**3.3**	4	**5.0**	A
Internal OCP; Sinking	OCP-	V_{OUT} = 1V; V_{IN} = 2V; V_{CC} = 2.7V; $R_{OCP-SNK}$ = 0Ω	-55 to +125°C	**-5.0**	-4.1	**-3.3**	A
Over-Temperature Protection; Rising	OTP_R	-	-	-	165	-	°C
Over-Temperature Recovery; Hysteresis	OTP_H	-	-	-	10	-	°C
Buffered Reference							
Buffer Input Voltage	BUF-IN	-	-55 to +125°C	**1.0**	-	**3.3**	V
Buffer Input Resistance	BUF_R	BUF-IN = 1V	-55 to +125°C	**1.5**	-	**2.5**	MΩ
Buffer Input UVLO; Rising	BUF_{UVLOR}	V_{CC} = 2.7V; V_{IN} = 3.3V; CONFIG = V_{CC}	-55 to +125°C	**0.75**	0.78	**0.82**	V

Unless otherwise specified: V_{CC} = 2.7V to 5.5V; V_{IN} = 0.75V to 5.5V; EN = V_{CC}; C_{OUT} = 150µF + 2x 10µF; OCP_SRC and OCP_SNK = AGND; T_A = 25°C. **Boldface limits apply across the operating temperature range, -55°C to +125°C by characterization with production testing at +25°C; over a total ionizing dose of 30krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL75055M30NEZ); or over a total ionizing dose of 50krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL75055M50NEZ).** (Cont.)

Parameter	Symbol	Test Conditions	Temperature	Min	Typ[1]	Max	Unit
Buffer Input UVLO; Falling	BUF_{UVLOF}	V_{CC} = 2.7V; V_{IN} = 3.3V; CONFIG = V_{CC}	-55 to +125°C	**0.72**	0.76	**0.78**	V
Buffer Input UVLO; Hysteresis	BUF_{UVLOH}	-	-55 to +125°C	**10**	23	**50**	mV
Buffer Output Voltage	BUF-OUT	As a percentage of BUF-IN; 1.0V < BUF-IN < 3.3V; -10mA < $I_{BUF-OUT}$ < 10mA	-55 to +125°C	**49.5**	50	**50.5**	%
BUF-OUT Voltage Tolerance to BUF-IN	$BUFOUT_{TOL}$	1.0V < BUF-IN < 3.3V; -10mA < $I_{BUF-OUT}$ < 10mA	-55 to +125°C	**-5**	-	**5**	mV
Buffer Output Current Limit; Sourcing	BUF_{OUT+}	BUF-OUT = 0V; V_{IN} = V_{CC} = 2.7V; BUF-IN = 1.2V; V_{IN} = V_{CC} = 5.5V; BUF-IN = 3.3V	-55 to +125°C	**15**	20	**27**	mA
Buffer Output Current Limit; Sinking	BUF_{OUT-}	BUF-OUT = V_{CC}; V_{IN} = V_{CC} = 2.7V; BUF-IN = 1.2V; V_{IN} = V_{CC} = 5.5V; BUF-IN = 3.3V	-55 to +125°C	**-27**	-20	**-15**	mA
ENABLE Pin							
Enable Threshold; Rising	EN_R	VREF_INT rising (200mV); V_{IN} = V_{CC} = 3.3V	-55 to +125°C	**1.05**	1.1	**1.15**	V
Enable Threshold; Falling	EN_F	VREF_INT falling (200mV); V_{IN} = V_{CC} = 3.3V	-55 to +125°C	**0.9**	0.98	**1.1**	V
Enable Threshold; Hysteresis	EN_H	-	-55 to +125°C	**10**	128	**160**	mV
Enable Propagation Delay; Rising	EN_PDR	EN = 0V to 5V; EN rising edge to VREF_INT = 450mV; V_{IN} = V_{CC} = 3.3V; C_{VREF_INT} = 100nF	-55 to +125°C	**60**	105	**130**	µs
Enable Propagation Delay; Falling	EN_PDF	EN = 5V to 0V; EN falling edge to VREF_INT = 450mV; V_{IN} = V_{CC} = 3.3V; C_{VREF_INT} = 100nF	-55 to +125°C	**4**	6.2	**8**	µs
Enable Input Leakage	I_EN	EN = 5.5V	-55 to +125°C	-	0.5	**1**	µA
Soft-Start							
Soft-Start Current	I_SS	SS = 0V; V_{IN} = V_{CC} = 3.3V	-55 to +125°C	**17**	20	**25**	µA
Soft-Start Done Threshold	SS_Done	V_{IN} = V_{CC} = 3.3V; PG = 2V	-55 to +125°C	**1.65**	2.08	**2.6**	V
Soft-Start Clamp Voltage	SS_Clamp	V_{IN} = V_{CC} = 3.3V	-55 to +125°C	**2.5**	3	**3.5**	V
SS Pin Discharge Resistance	R_SS	SS = 1V; EN = 0; V_{IN} = V_{CC} = 3.3V	-55 to +125°C	**8**	15	**22**	Ω

Unless otherwise specified: V_{CC} = 2.7V to 5.5V; V_{IN} = 0.75V to 5.5V; EN = V_{CC}; C_{OUT} = 150µF + 2x 10µF; OCP_SRC and OCP_SNK = AGND; T_A = 25°C. **Boldface limits apply across the operating temperature range, -55°C to +125°C by characterization with production testing at +25°C; over a total ionizing dose of 30krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL75055M30NEZ); or over a total ionizing dose of 50krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL75055M50NEZ).** (Cont.)

Parameter	Symbol	Test Conditions	Temperature	Min	Typ[1]	Max	Unit
Power Good							
PG Overvoltage Threshold; Rising	PG_OVR	V_{IN} = V_{CC} = 3.3V; EA- as a % of EA+; EA+ = 0.5V (Ramp EA-, PG = 2V falling, R_{PG} =10kΩ)	-55 to +125°C	**107**	111	**114**	%
PG Overvoltage Hysteresis	PG_OVH	V_{IN} = V_{CC} = 3.3V; EA- as a % of EA+; EA+ = 0.5V	-55 to +125°C	**1.5**	3.9	**5**	%
PG Undervoltage Threshold; Falling	PG_UVF	V_{IN} = V_{CC} = 3.3V; EA- as a % of EA+; EA+ = 0.5V (Ramp EA-, PG = 2V falling, R_{PG} =10kΩ)	-55 to +125°C	**87**	89	**91**	%
PG Undervoltage Hysteresis	PG_UVH	V_{IN} = V_{CC} = 3.3V; EA- as a % of EA+; EA+ = 0.5V	-55 to +125°C	**1.5**	4.2	**5**	%
PG Output Low Voltage	PG_LOW	I_PG = 1mA; V_{IN} = V_{CC} = 2.7V; EN = 0V	-55 to +125°C	-	0.03	**0.4**	V
PG Leakage Current	PG_LEAK	V_{IN} = V_{CC} =5.5V; PG = 5.5V; V_{OUT} in regulation	-55 to +125°C	-	-	**0.01**	µA
PG Delay; Rising	PG_PDR	V_{IN} = V_{CC} = 2.7V; EA- rising edge (0.5V) to PG Rising (89% of V_{CC})	-55 to +125°C	**5**	6.4	**8**	µs
PG Delay; Falling	PG_PDF	V_{IN} = V_{CC} = 2.7V; EA- falling edge (0.4V) to PG Falling (89% of V_{CC})	-55 to +125°C	**0.75**	1.04	**1.25**	µs
CONFIG Pin - VOUT and BUF-OUT Discharge							
CONFIG Pin Threshold	CFIG_R	V_{IN} = V_{CC} = 2.7V; EN=0V; Rising Threshold when V_{OUT} falls to 0.8V	-55 to +125°C	**1.05**	1.1	**1.15**	V
CONFIG Pin Hysteresis	CFIG_H	-	-55 to +125°C	**90**	106	**140**	mV
BUF-OUT Discharge Resistance	$BUF\text{-}OUT_{\_R}$	BUF-IN = 0.5V; V_{IN} = V_{CC} = CONFIG = 2.7V; BUF-OUT sinking current = 10mA	-55 to +125°C	**9**	17	**29**	Ω
VOUT Discharge Resistance	VOUT_R	EN = 0V; V_{IN} = V_{CC} = CONFIG = 2.7V; VOUT sinking current = 20mA	-55 to +125°C	**3**	6.5	**12**	Ω

1. Typical values are at 25°C and are not guaranteed.
2. VCC dropout is defined by the difference V_{CC}-V_{OUT} where the regulated V_{OUT} voltage produces a 1% drop in V_{OUT} from its nominal value established when V_{CC}-V_{OUT}>V_{CC_DO}.

3.5.2 AC Electrical Specifications

Unless otherwise specified: EN = V_{CC}; C_{OUT} = 2x150µF + 0.1µF; T_A = 25°C.

Parameter	Symbol	Test Conditions	Min	Typ[1]	Max	Unit
VOUT PSRR						
VCC PSRR; Sourcing	$PSSR_{VCC+}$	V_{CC} = 3.3V; V_{IN} = 1.5V; V_{OUT} = 0.5V; I_{OUT} = 3A V_{RIPPLE}(VCC) = 150mV_{P-P}; Frequency = 100kHz	-	66	-	dB
VCC PSRR; Sinking	$PSSR_{VCC-}$	V_{CC} = 3.3V; V_{IN} = 1.5V; V_{OUT} = 0.5V; I_{OUT} = -3A V_{RIPPLE}(VCC) = 150mV_{P-P}; Frequency = 100kHz	-	71	-	dB
VIN PSRR; Sourcing	$PSSR_{VIN+}$	V_{CC} = 3.3V; V_{IN} = 1.5V; V_{OUT} = 0.5V; I_{OUT} = 3A V_{RIPPLE}(VIN) = 150mV_{P-P}; Frequency = 100kHz	-	60	-	dB

Unless otherwise specified: EN = V_{CC}; C_{OUT} = 2x150µF + 0.1µF; T_A = 25°C. **(Cont.)**

Parameter	Symbol	Test Conditions	Min	Typ[1]	Max	Unit
VIN PSRR; Sinking	$PSSR_{VIN-}$	V_{CC} = 3.3V; V_{IN} = 1.5V; V_{OUT} = 0.5V; I_{OUT} = -3A V_{RIPPLE}(VIN) = 150mV_{P-P}; Frequency = 100kHz	-	87	-	dB
VOUT Noise						
VOUT RMS Noise		V_{CC} = 3.3V; V_{IN} = 1.5V; V_{OUT} = 0.5V; I_{OUT} = 3A; BW = 10Hz < f < 100kHz; EA- = OUT	-	22.8	-	µV_{RMS}

1. Typical values are at 25°C and are not guaranteed.

4. Typical Performance Graphs

V_{CC} = 3.3V, V_{IN} = 3.3V, C_{OUT} = 2x150µF Tantalum, 0.1µF ceramic, C_{SS} = 10nF, C_{BUF-IN} = 1µF, R_{BUF-IN} = 1kΩ, T_A = +25°C, unless otherwise stated.

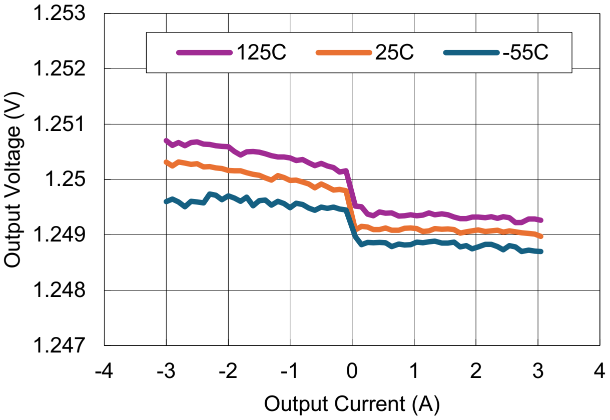


Figure 7. Output Voltage vs Output Current; DDR (BUF-IN = 2.5V)

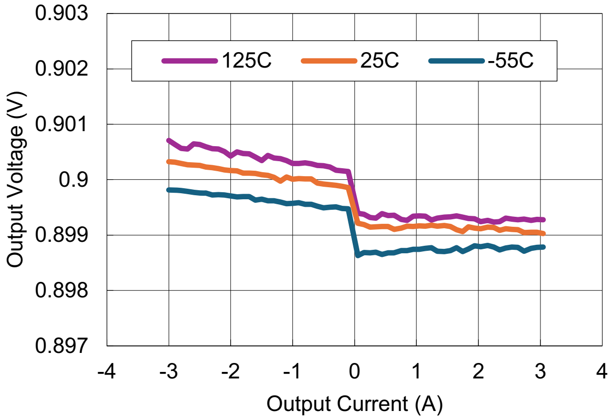


Figure 8. Output Voltage vs Output Current; DDR2 (BUF-IN = 1.8V)

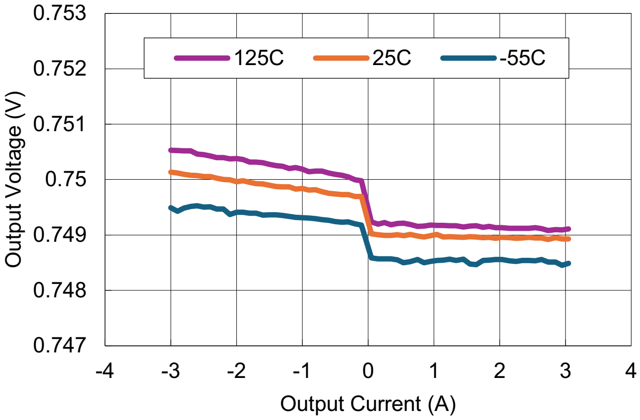


Figure 9. Output Voltage vs Output Current; DDR3 (BUF-IN = 1.5V)

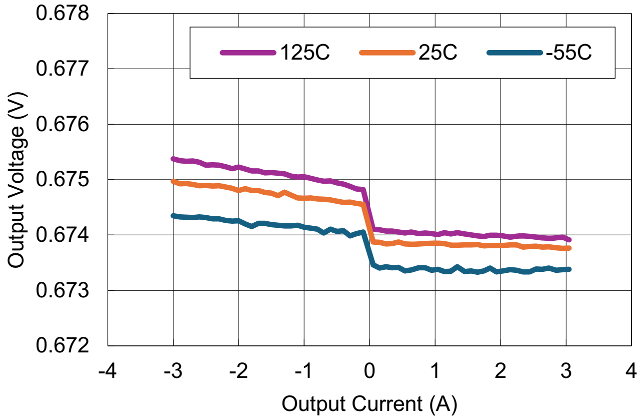


Figure 10. Output Voltage vs Output Current; DDR3L (BUF-IN = 1.35V)

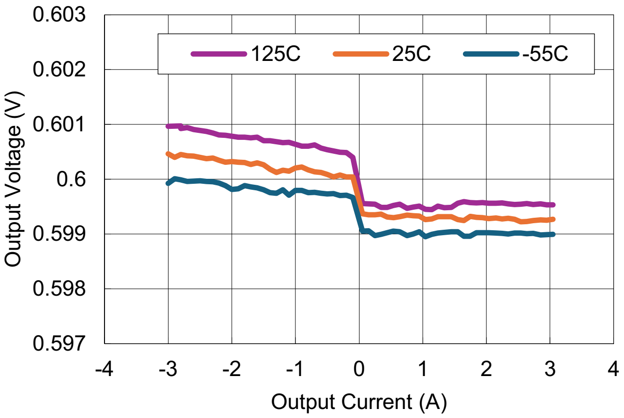


Figure 11. Output Voltage vs Output Current; DDR4 (BUF-IN = 1.2V)

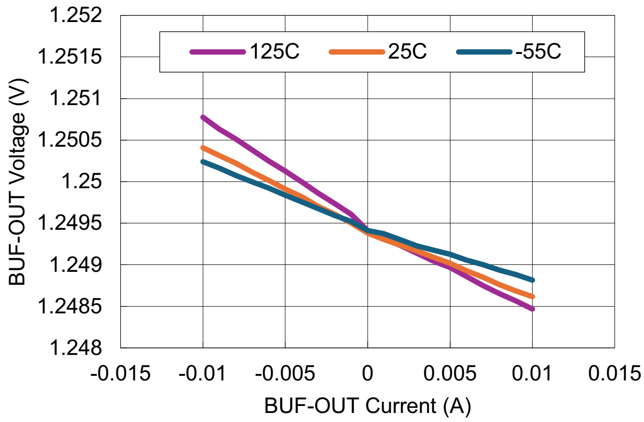


Figure 12. BUF-OUT Voltage vs BUF-OUT Current; DDR (BUF-IN = 2.5V)

V_{CC} = 3.3V, V_{IN} = 3.3V, C_{OUT} = 2x150µF Tantalum, 0.1µF ceramic, C_{SS} = 10nF, C_{BUF-IN} = 1µF, R_{BUF-IN} = 1kΩ, T_A = +25°C, unless otherwise stated. (Cont.)

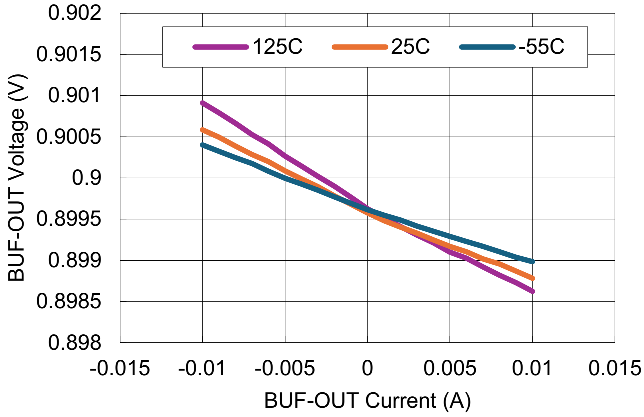


Figure 13. BUF-OUT Voltage vs BUF-OUT Current; DDR2 (BUF-IN = 1.8V)

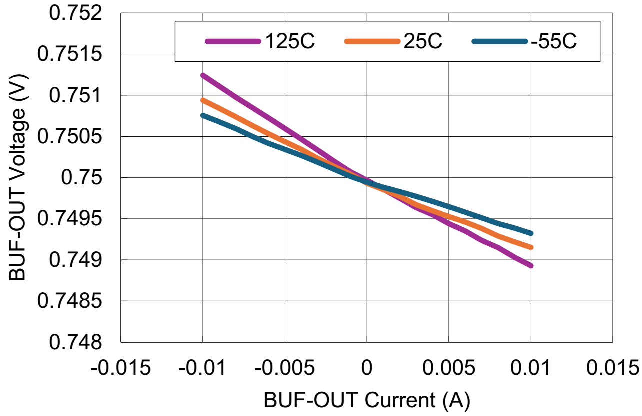


Figure 14. BUF-OUT Voltage vs BUF-OUT Current; DDR3 (BUF-IN = 1.5V)

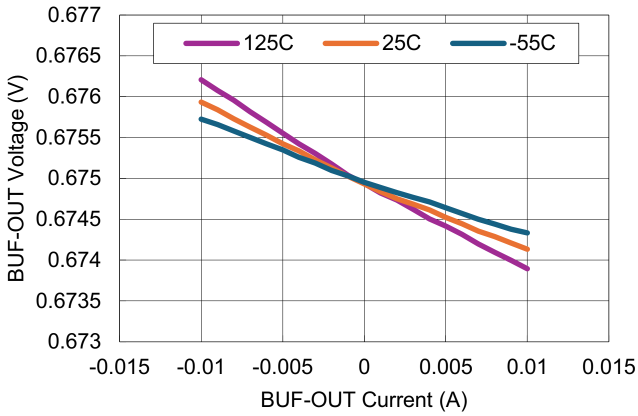


Figure 15. BUF-OUT Voltage vs BUF-OUT Current; DDR3L (BUF-IN = 1.35V)

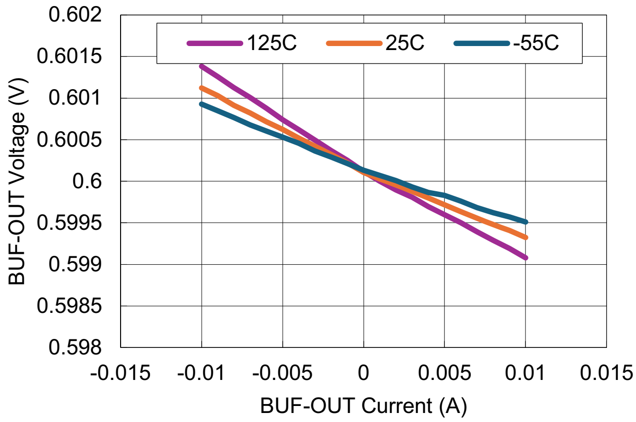


Figure 16. BUF-OUT Voltage vs BUF-OUT Current; DDR4 (BUF-IN = 1.2V)

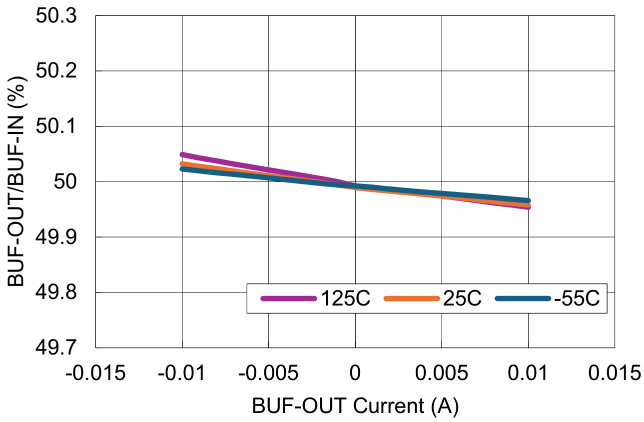


Figure 17. BUF-OUT/BUF-IN Percentage vs BUF-OUT Current; DDR (BUF-IN = 2.5V)

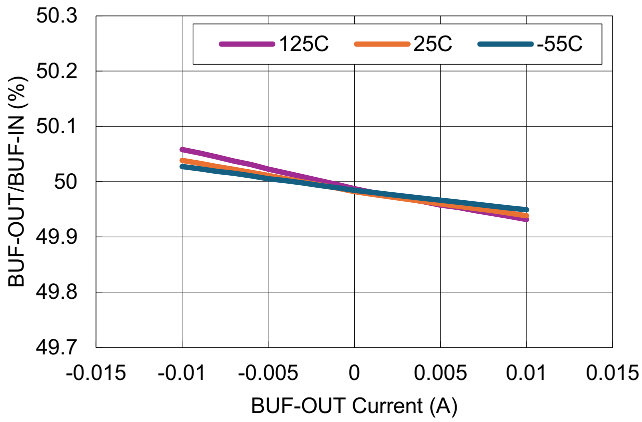


Figure 18. BUF-OUT/BUF-IN Percentage vs BUF-OUT Current; DDR2 (BUF-IN = 1.8V)

V_{CC} = 3.3V, V_{IN} = 3.3V, C_{OUT} = 2x150µF Tantalum, 0.1µF ceramic, C_{SS} = 10nF, $C_{BUF\text{-}IN}$ = 1µF, $R_{BUF\text{-}IN}$ = 1kΩ, T_A = +25°C, unless otherwise stated. (Cont.)

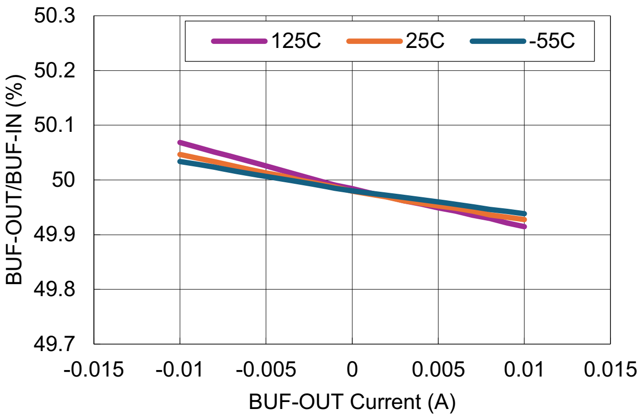


Figure 19. BUF-OUT/BUF-IN Percentage vs BUF-OUT Current; DDR3 (BUF-IN = 1.5V)

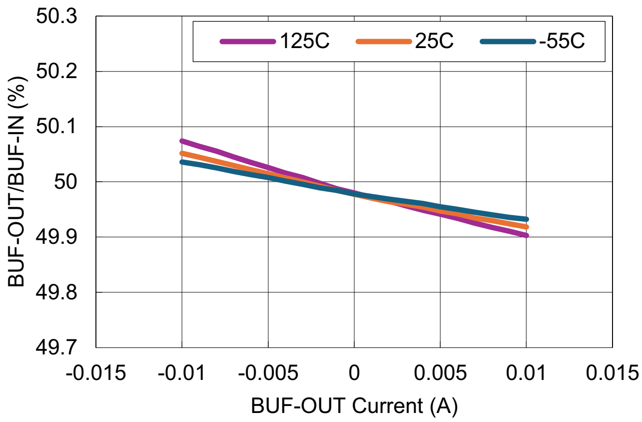


Figure 20. BUF-OUT/BUF-IN Percentage vs BUF-OUT Current; DDR3L (BUF-IN = 1.35V)

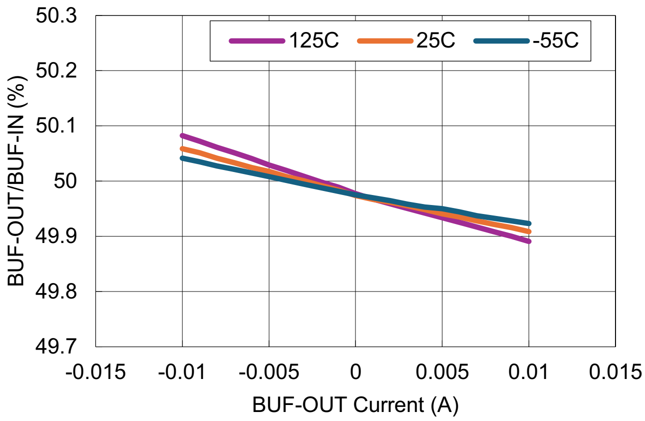


Figure 21. BUF-OUT/BUF-IN Percentage vs BUF-OUT Current; DDR4 (BUF-IN = 1.2V)

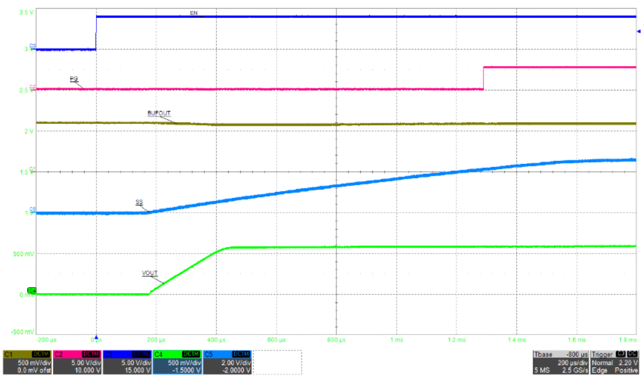


Figure 22. Startup with Soft-Start; DDR Mode (V_{IN} = BUF-IN = 1.2V, V_{CC} = 2.7V, EA+ = BUF-OUT, V_{OUT} = 0.6V, I_{OUT} = 0A)

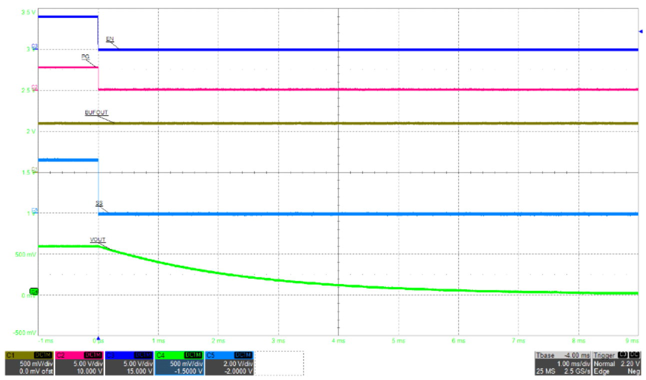


Figure 23. Shutdown; DDR Mode, Config High (V_{IN} = BUF-IN = 1.2V, V_{CC} = 2.7V, EA+ = BUF-OUT, V_{OUT} = 0.6V, I_{OUT} = 0A)

V_{CC} = 3.3V, V_{IN} = 3.3V, C_{OUT} = 2x150µF Tantalum, 0.1µF ceramic, C_{SS} = 10nF, $C_{BUF\text{-}IN}$ = 1µF, $R_{BUF\text{-}IN}$ = 1kΩ, T_A = +25°C, unless otherwise stated. (Cont.)

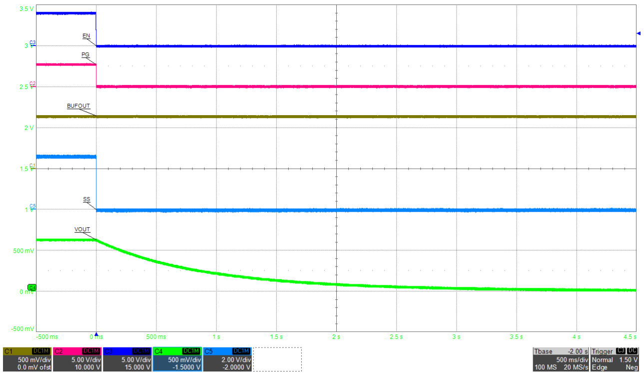


Figure 24. Shutdown; DDR Mode, Config Low (V_{IN} = BUF-IN = 1.2V, V_{CC} = 2.7V, EA+ = BUF-OUT, V_{OUT} = 0.6V, I_{OUT} = 0A)

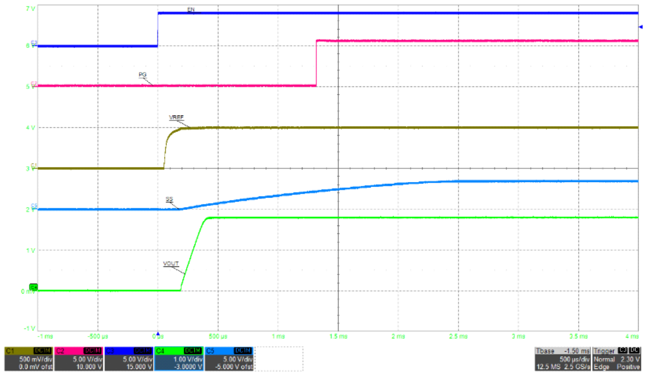


Figure 25. Startup with Soft-Start; LDO Mode (V_{IN} = 3.6V, V_{CC} = 5.5V, EA+ = VREF_INT, V_{OUT} = 1.8V, I_{OUT} = 0A)

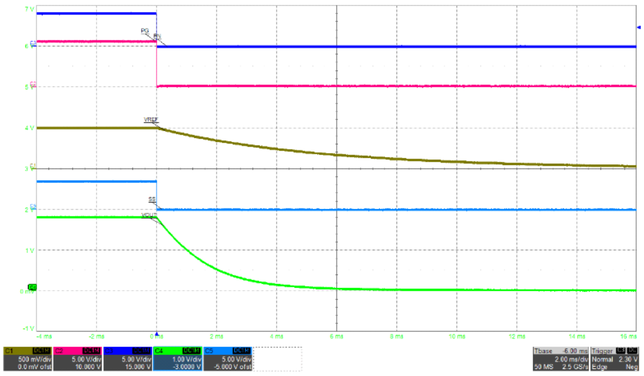


Figure 26. Shutdown; LDO Mode, Config High (V_{IN} = 3.6V, V_{CC} = 5.5V, EA+ = VREF_INT, V_{OUT} = 1.8V, I_{OUT} = 0A)

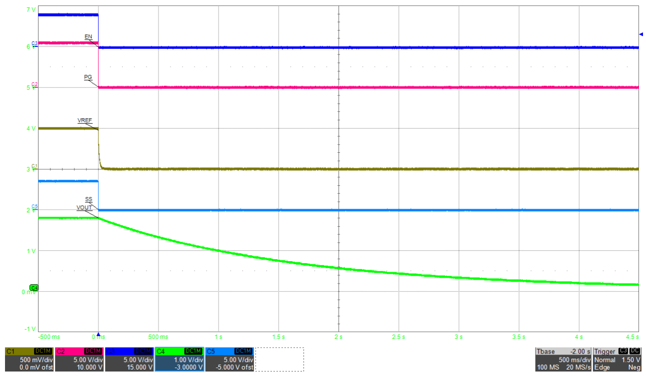


Figure 27. Shutdown; LDO Mode, Config Low (V_{IN} = 3.6V, V_{CC} = 5.5V, EA+ = VREF_INT, V_{OUT} = 1.8V, I_{OUT} = 0A)

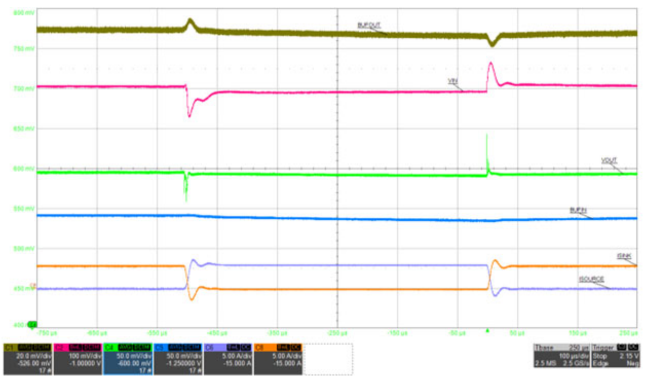


Figure 28. Load Transient Response; DDR4 (V_{IN} = BUF-IN = 1.2V, V_{CC} = 2.7V, Load step = -3A to +3A)

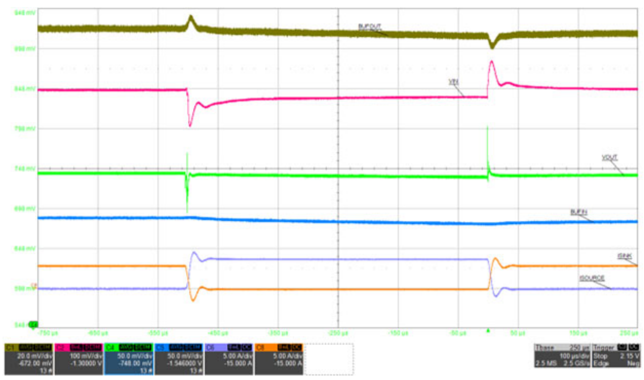


Figure 29. Load Transient Response; DDR3 (V_{IN} = BUF-IN = 1.5V, VCC = 2.7V, EA+ = BUF-OUT. Load Step = -3A to +3A)

V_{CC} = 3.3V, V_{IN} = 3.3V, C_{OUT} = 2x150µF Tantalum, 0.1µF ceramic, C_{SS} = 10nF, $C_{BUF\text{-}IN}$ = 1µF, $R_{BUF\text{-}IN}$ = 1kΩ, T_A = +25°C, unless otherwise stated. (Cont.)

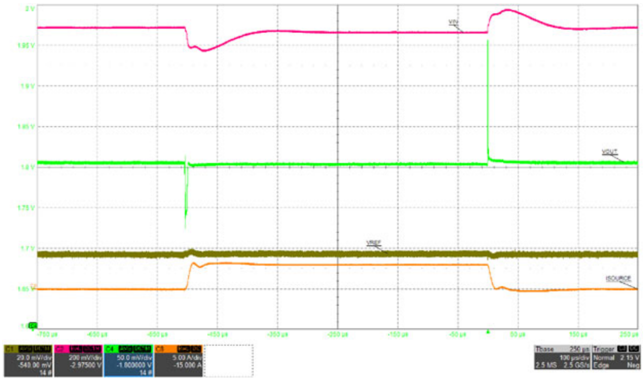


Figure 30. Load Transient Response; 1.8V LDO (V_{IN} = 3.6V, V_{CC} = 5.5V, EA+ = VREF_INT, Load Step = 0 to +3A)

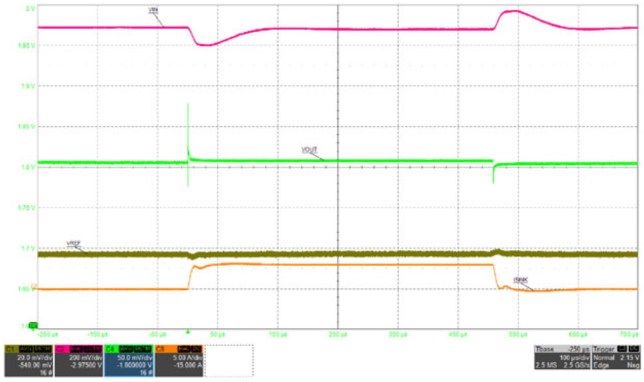


Figure 31. Load Transient Response; 1.8V LDO (V_{IN} = 3.6V, V_{CC} = 5.5V, EA+ = VREF_INT, Load Step = 0A to -3A)

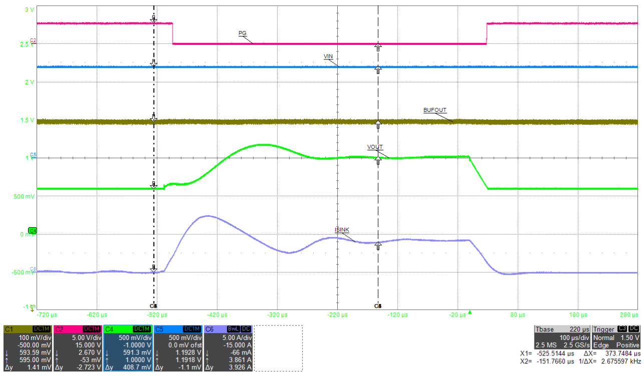


Figure 32. Overcurrent Limit Response; DDR4 - Sinking (V_{IN} = BUF-IN = 1.2V, V_{CC} = 2.7V)

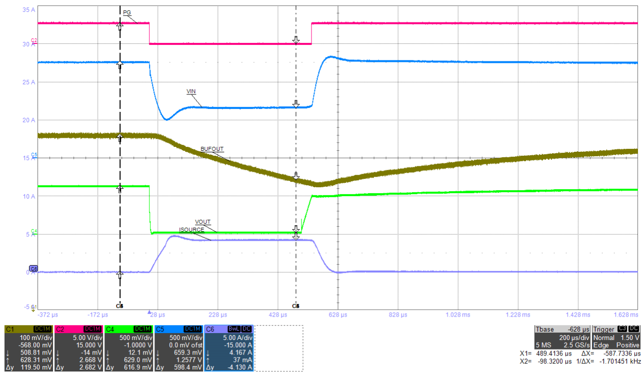


Figure 33. Overcurrent Limit Response; DDR4 - Sourcing (V_{IN} = BUF-IN = 1.2V, V_{CC} = 2.7V)

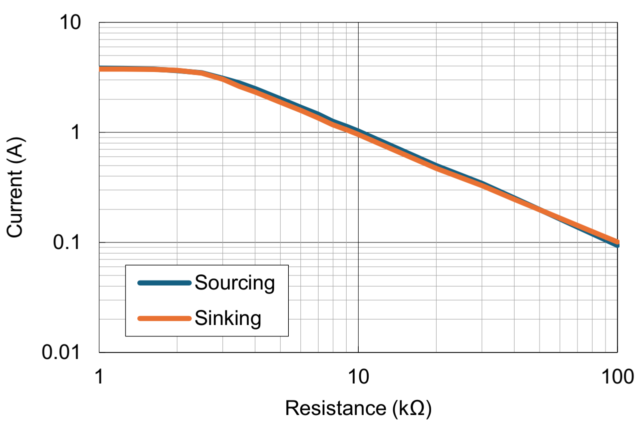


Figure 34. Overcurrent Protection Limit vs OCP Resistor

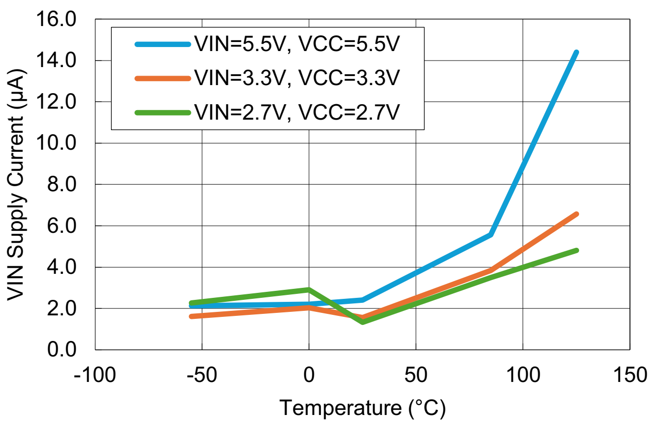


Figure 35. VIN Supply Current (EN = V_{CC}, EA+ = VREF_INT, V_{OUT} = 0.5V, I_{OUT} = 0A)

V_{CC} = 3.3V, V_{IN} = 3.3V, C_{OUT} = 2x150µF Tantalum, 0.1µF ceramic, C_{SS} = 10nF, C_{BUF-IN} = 1µF, R_{BUF-IN} = 1kΩ, T_A = +25°C, unless otherwise stated. (Cont.)

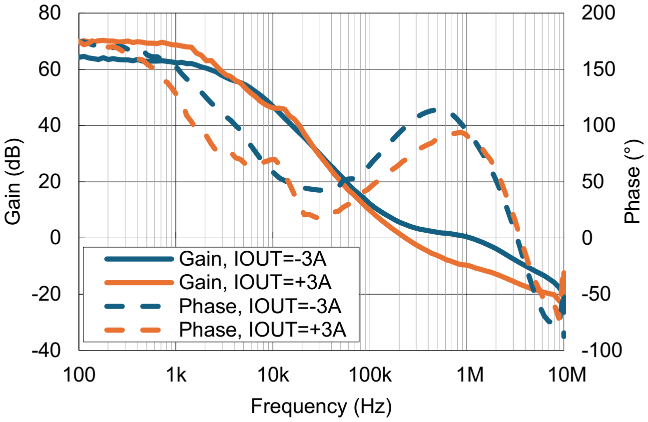


Figure 36. Bode Plot; DDR4 (V_{IN} = BUF = IN = 1.2V, V_{CC} = 3.3V, EA+ = BUF-OUT)

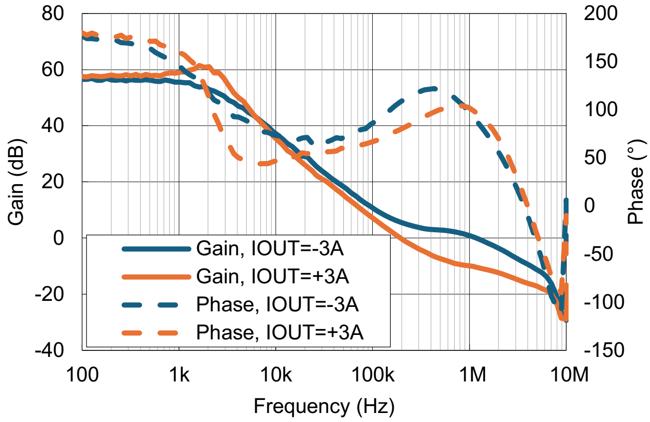


Figure 37. Bode Plot; 1.2V LDO (V_{IN} = 3.3V, V_{CC} = 3.3V, EA+ = VREF_INT, C_{OUT} = 1×330µF)

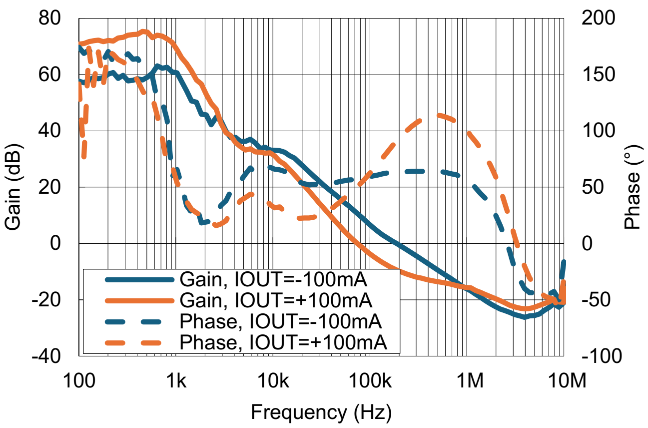


Figure 38. Bode Plot; DDR4 Light Load (V_{IN} = BUF = IN = 1.2V, V_{CC} = 3.3V, EA+ = BUF-OUT)

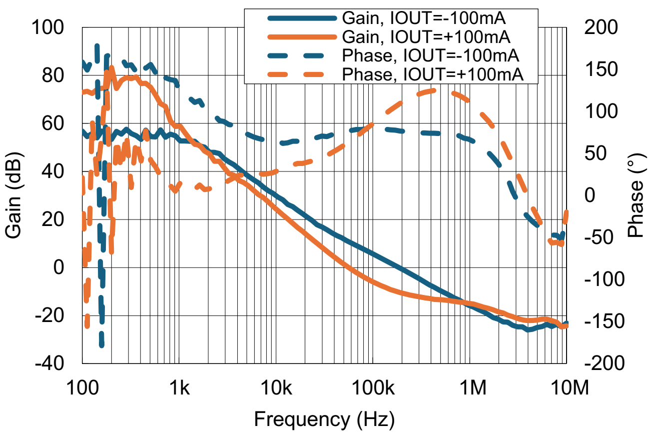


Figure 39. Bode Plot; 1.2V LDO Light Load (V_{IN} = 3.3V, V_{CC} = 3.3V, EA+ = VREF_INT, C_{OUT} = 1×330µF)

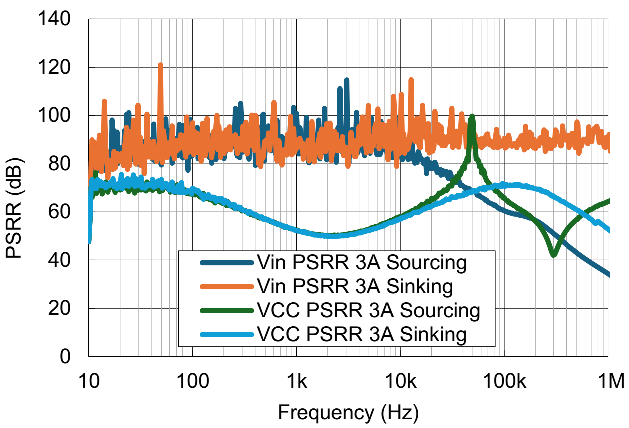


Figure 40. PSRR; 0.5V LDO (V_{IN} = 1.5V, V_{CC} = 3.3V, V_{OUT} = 0.5V)

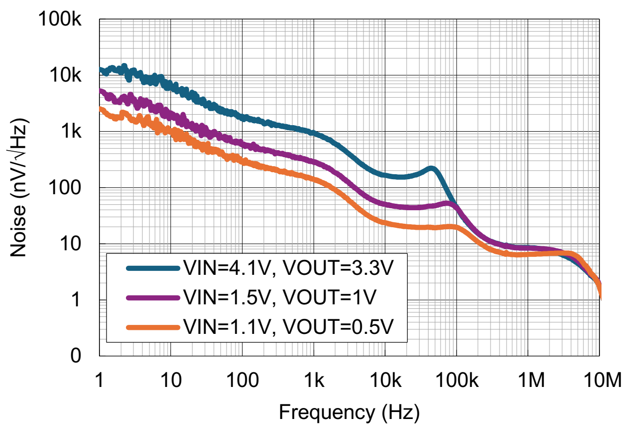


Figure 41. Noise; LDO Mode (V_{CC} = 2.7V, or 5V for V_{OUT} = 3.3V, I_{OUT} = 1A Sourcing)

5. Functional Description

The ISL75055M is a radiation tolerant 0.75V to 5.5V input, 3A sourcing and sinking low dropout linear regulator designed for powering the VTT termination rail of DDR memory modules or as a high performance general purpose point-of-load regulator. A buffered reference amplifier provides an accurate VREF reference supply for the DDR. Individual adjustable overcurrent protection (OCP) for sourcing and sinking allows the current limit of the LDO to be configured down to 300mA.

The ISL75055M features external error amplifier inputs to set VDDQ/2 as the reference voltage in DDR applications. It also features an internal 0.5V reference for standard LDO applications. Separate VCC bias and LDO VIN pins, combined with a very low dropout allows minimal internal losses while maintaining highly accurate output regulation.

5.1 LDO Architecture

The ISL75055M LDO provides both sourcing and sinking capabilities through the implementation of an NMOS power stage. The device is capable of 3A sourcing and 3A sinking for VTT termination rails in DDR memory. Highly accurate output voltage regulation is made possible through a low offset voltage error amplifier with a dead band of only 600µV. This makes the ISL75055M ideal for VTT rails in DDR4 applications with stringent output voltage specs.

The error amplifier achieves very low dead band crossover and achieves very fast transition times when moving between sourcing and sinking regulation, which results in a faster transient response and reduces the output capacitance required. For configurations where the error amplifier is operating with unity gain, such as DDR mode, the dead band is 600µV typical. For standard LDO applications, the dead band is amplified with V_{OUT}/0.5V ratio due to feedback gain.

The LDO also features an internal buffer that is accessible using the BUF-IN and BUF-OUT pins. This buffer provides a fixed output of BUF-IN/2 to generate the VTT reference voltage of VDDQ/2 in DDR applications.

An internal 500mV voltage reference is also implemented to allow for the flexibility required in programming the output voltage for standard LDO applications.

Separate from the main LDO input VIN, a VCC bias rail powers the gate drive and internal circuitry enabling the LDO to achieve very low dropout. The VIN to VOUT and VCC to VOUT headroom determine the regulator dropout voltage.

5.2 Error Amplifier Inputs

The ISL75055M provides pins for both the inverting (EA-) and non-inverting (EA+) inputs to the error amplifier. The dedicated EA+ pin configures the part for either DDR or standard LDO configurations. In the DDR configuration, BUF-OUT is used as the input to EA+, providing BUF-IN/2 as the reference voltage. In the standard LDO configuration, VREF_INT is used as the input to EA+, providing a fixed 500mV reference voltage.

The EA- pin is used for the output voltage feedback that is compared to the reference voltage on EA+. For the DDR configuration, EA- should be connected directly to VOUT at the required output voltage regulation sense point. For standard LDO configurations where V_{OUT} = 0.5V, EA- is similarly connected directly to VOUT. For all other LDO mode output voltages greater than 0.5V, the output voltage is set by a feedback resistor divider between VOUT, EA-, and AGND. Feedback resistor selection is described in more detail in LDO Output Voltage.

5.3 LDO Fault Protection

The ISL75055M features protection for undervoltage, overvoltage, over-temperature, and overcurrent.

Both the VCC and VIN inputs are protected by undervoltage lockout (UVLO). If both inputs are not above their respective UVLO thresholds of 2.62V typical for VCC rising and 472mV typical for VIN rising, the LDO is disabled.

Output undervoltage and overvoltage protection is implemented by monitoring the EA- voltage as a percentage of EA+. When the EA- voltage rises above PG overvoltage threshold or falls below the PG undervoltage threshold, PG is pulled low.

Overcurrent protection is implemented through current sensing in both the sourcing and sinking paths. When the source or sink current reaches the current limit threshold, the output is forced into constant current regulation. Sourcing and sinking OCP are independently resistor adjustable from 300mA to 3A typical, or tie OCP pins to GND for 4A typical sourcing limit and 4.1A typical sinking limit.

The die junction temperature is monitored internally. When the internal temperature reaches 165°C (typical), the LDO output is disabled. After the internal temperature falls below 155°C (typical), the device resumes normal operation. To determine the expected temperature rise of the device from ambient to junction or case to junction, calculate power dissipation using Equation 1 and Equation 2. While sourcing the voltage drop across the pass device is the difference in V_{IN} and V_{OUT}. While sinking, the voltage drop across the pass device is the difference in V_{OUT} and PGND voltage, which is typically 0V.

Sourcing LDO power dissipation:

(EQ. 1) $$P_{SRC} = (V_{IN} - V_{OUT}) \times I_{OUT}$$

Sinking LDO power dissipation:

(EQ. 2) $$P_{SNK} = V_{OUT} \times I_{OUT}$$

Using the greater of the sinking/sourcing power dissipations (P_{max}), the maximum expected ambient temperature (T_{Amax}), and the maximum junction temperature (T_{Jmax}) use Equation 3 to calculate the required thermal impedance to meet the worst-case operating conditions.

(EQ. 3) $$\theta_{JAmax} = \frac{T_{Jmax} - T_{Amax}}{P_{max}}$$

To avoid thermal shutdown, ensure the specified θ_{JA} is less than the calculated θ_{JAmax}. The θ_{JA} value used must take into account copper area, airflow, and use of heatsinks in a given system.

5.4 CONFIG Pin

The CONFIG pin enables and disables the active discharge feature of VOUT and BUF-OUT. When CONFIG is above the rising threshold, typically 1.1V, active discharge is enabled. CONFIG can be tied to VCC to set it high. When CONFIG is below the typical value of 1V, the active discharge is disabled. CONFIG can be tied to GND to set it low.

Both the VOUT and BUF-OUT discharge circuits are comprised of an NMOS FET that is turned on when discharge conditions are met. For VOUT, discharge occurs when EN falls low and disables the LDO. For BUF-OUT, discharge occurs when BUF-IN falls below its UVLO threshold.

5.5 Enable

The EN pin enables and disables the LDO output. When EN is above the Enable Threshold; Rising (1.1V typical), the LDO is enabled. When EN falls below the Enable Threshold; Falling (0.98V typical), the LDO is disabled.

EN also controls the biasing of the internal voltage reference, VREF_INT. When the EN rising/falling thresholds are met, there is a delay to VREF_INT turning on/off. This is shown as Enable Propagation Delay; Rising and Enable Propagation Delay; Falling in DC Electrical Specifications.

Tie EN to VCC if an external enable control is not required.

The EN signal falling below the enable threshold also results in VOUT discharge when the discharge function is enabled using the CONFIG pin.

Note: The buffer output (BUF-OUT) is independent of EN and is active when BUF-IN and VCC are above their respective UVLO thresholds.

5.6 Soft Start

Soft start is implemented by placing a capacitor on the SS pin. This functionality reduces inrush current and provides a smooth V_{OUT} ramp during startup. V_{OUT} starts to ramp when the SS voltage is greater than a typical value of 20mV to overcome the offset of the error amplifier. SS charges to the soft-start done threshold, typically 2.08V, at which point PG is released. V_{OUT} tracks the SS voltage until SS is greater than the EA+ voltage. SS is clamped to a typical voltage of 3V.

During the fault conditions (undervoltage, overvoltage, or over-temperature), SS discharges so that soft start can re-initiate as part of fault recovery. SS also discharges when EN is low.

The error amplifier uses the lower of SS and EA+ voltage as the non-inverting reference for regulation.

6. Application Information

6.1 Power Supply Biasing

The VIN pins function as the power supply input. A minimum input voltage of 0.75V or V_{OUT} + V_{IN_DO} is required on VIN for regulation. The maximum recommended operating voltage on VIN is 5.5V. The input capacitor should be selected to avoid VIN drooping below dropout voltage during load transients. VIN transient performance is also dependent on system factors such as the input supply bulk capacitance, distance from the LDO, and transient performance. Renesas recommends using a 150µF tantalum capacitor and two 10µF ceramic capacitors on VIN. Additional ceramic capacitors can be placed on VIN for high frequency noise filtering.

A bias supply is required on VCC to provide biasing to internal circuitry. The minimum VCC supply voltage is 2.7V or 1.5V greater than the target output voltage to provide headroom for the VCC dropout voltage of 1.4V. The maximum recommended operating voltage on VCC is 5.5V. A 1µF capacitor is required on VCC and should be placed near the device pin.

6.2 Soft-Start Capacitor

Based on the typical soft-start current of 20µA, a soft-start capacitance can be chosen for a given EA+ rise time using Equation 4. This equation is used because V_{OUT} tracks the SS ramp until it exceeds the EA+ voltage.

(EQ. 4) $$C_{SS} = \frac{I_{SS} \times t_{SS}}{EA+}$$

where:

- C_{SS} is the soft-start capacitor value.
- I_{SS} is the soft-start current.
- t_{SS} is the soft-start time.
- EA+ is the voltage on the non-inverting input of the error amplifier.

V_{OUT} is equal to EA+ in DDR configuration. In standard LDO configuration where a resistor divider is used to set the output voltage, V_{OUT} is scaled to EA+ based on the resistor divider.

C_{OUT} is charged up to V_{OUT} in t_{ss}, resulting in an inrush current that can be calculated using Equation 5:

Although the supply is in regulation, PG is not active until SS reaches the soft-start done threshold of 2.08V typical.

(EQ. 5) $$I_{INRUSH} = C_{OUT} \times \frac{V_{OUT}}{t_{SS}}$$

6.3 Buffer Input and Output for DDR Applications

In DDR applications, the VDDQ rail is typically used as the LDO input supply, VIN. Because DDR memory power supplies specify VTT as VDDQ/2, the internal buffer on the ISL75055M generates the VTT reference voltage. For applications where VDDQ is tied to both VIN and BUF-IN, Renesas recommends placing an RC low pass filter of 1kΩ and 1µF between the VIN and BUF-IN pins. This filter mitigates SETs and transients on the input supply so that the BUF-IN voltage is stable.

A minimum 1µF capacitor is recommended on BUF-OUT for SEE mitigation. The buffer output is independent of the EN pin. BUF-OUT is active if BUF-IN and VCC UVLO thresholds are met.

6.3.1 Buffer Input Range for EA+

To guarantee soft-start functionality, the recommended maximum input to BUF-IN is 3.3V when BUF-OUT is connected to EA+. The resulting BUF-OUT voltage of 1.65V, is equal to the minimum Soft-Start Done Threshold specified in DC Electrical Specifications. While BUF-IN is rated for voltages up to the VCC voltage, there are reasons to avoid voltages greater than 3.3V, when BUF-OUT is used as the reference voltage to EA+. When BUF-OUT is greater than Soft-Start Done Threshold, PG timing is affected since PG functionality becomes active before the supply reaches its regulation point, removing any delays. Additionally, the minimum soft-start clamp voltage is 2.5V. This means that for BUF-IN voltage greater than 5V (or EA+ greater than 2.5V), full regulation is not reached since the lowest of SS and EA+ is used for the error amplifier reference and the SS voltage is used as the regulation point.

6.3.2 VREF_INT for Standard LDO Applications

VREF_INT is the output of the internal 500mV voltage reference. VREF_INT becomes active when both VCC UVLO and EN rising thresholds are met. A minimum bypass capacitance of 0.1µF should be placed on this pin. For standard LDO applications, VREF_INT is used as the input to the error amplifier non-inverting input (EA+), where it acts as a voltage reference allowing for the LDO output to be programmed down to 0.5V.

6.4 LDO Output Voltage

In DDR applications, where BUF-OUT is used as the input to EA+, connect EA- directly to VOUT at the point of load (PoL) for VTT rail regulation. Under this configuration, output voltage is regulated to BUF-IN/2.

In a standard LDO application where VREF_INT is used as the input to EA+, a resistor divider placed from VOUT to EA- sets the output voltage. Use Equation 6 to determine the required resistors for a target output voltage. For supplies that require an output voltage of 0.5V, a resistor divider is not required and EA- can connect directly to VOUT at the point of load.

(EQ. 6)
$$V_{OUT} = VREF\_INT \times \left(1 + \frac{R_{FBT}}{R_{FBB}}\right)$$

where:

- R_{FBT} is the top feedback divider resistor.
- R_{FBB} is the bottom feedback resistor divider.

For applications where V_{OUT} is set through a resistor divider between VOUT and EA-, the dead band proportionally scales to the gain from EA+ to VOUT. The increase in dead band voltage from feedback loop gain increases the delta of the regulation set point as the linear regulator transitions from sourcing to sinking current.

6.5 Output Capacitance

Recommended output capacitance depends on whether the device is operating in a DDR or standard LDO configuration. In DDR mode, where the control loop is operating with unity gain, Renesas recommends using two 150µF/15mΩ Tantalum Polymer capacitors in parallel to achieve loop stability. Additionally, place a 4.99kΩ resistor between the output and EA- pin. This resistor creates a pole at the target frequency of 1.5MHz with the internal capacitance on the EA- node.

In LDO mode, where additional loop gain is introduced by the feedback resistor divider, Renesas recommends using a single 330µF/25mΩ Tantalum Polymer capacitor to achieve loop stability.

Place Tantalum Polymer capacitors near the device VOUT and PGND pins to minimize effects of ESR and ESL. Additional ceramic capacitors are not necessary for stability. If used for high frequency decoupling, place a 0.1µF capacitor near the PoL.

Bench evaluations were performed with the T530X157M016ATE015, 150µF/15mΩ ESR capacitor for DDR mode and the T541X337M016AH6520, 330µF/25mΩ capacitor for LDO mode. Stability should be validated using a bode plot and load transient analysis in the end application.

6.6 Power Good (PG)

The PG pin is an open-drain output and requires a pull-up resistor to VCC. Renesas recommends placing a 10kΩ resistor between PG and VCC.

PG pulls low during output overvoltage, undervoltage, and over-temperature conditions. PG is also low when SS is below the soft-start done threshold.

6.7 Adjustable Source and Sink Current Limit

The current limit can be programmed individually for both sourcing and sinking paths. A resistor to AGND from the OCP-SRC pin (sourcing) and OCP-SNK pin (sinking) sets the current limit. When the OCP pins are connected directly to AGND, the maximum limit of sourcing (4A typical) and sinking (4.1A typical) are set internally.

Renesas recommends using a maximum OCP resistor value of 30kΩ, which equates to a minimum sourcing/sinking current limit of 300mA. Use Equation 7 to calculate the OCP resistance based on target current limit. Figure 34 shows a typical curve for current limit vs OCP resistance in both the sinking and scouring direction. OCP resistor values above 30kΩ further reduce the current limit, but accuracy of the threshold becomes degraded and is not recommended.

(EQ. 7) $$R_{OCP} = \frac{9000[mA \times k\Omega]}{I_{OCP}}$$

where:

- R_{OCP} is the sinking or sourcing OCP resistance in kΩ.
- I_{OCP} is the target sinking or sourcing current limit in mA.

6.8 Recommended PCB Layout

PCB layout is critical for optimizing LDO performance. See Figure 42 for a recommended layout.

- Place bulk output capacitors as close as possible to the VOUT pins. Ensure the VOUT plane is wide enough to handle 3A of current.
- Connect EA- to VOUT at the point of load to avoid inaccuracies in output voltage sensing. When a resistor divider is used for setting the output voltage, place the resistors near the EA- pin to prevent noise coupling to the high impedance EA- trace.
- Place bypass capacitors on VREF_INT, VCC, BUF-IN, and BUF-OUT near the respective pins.
- The plastic TQFP package EPAD should be tied to the system GND plane through multiple vias and multiple PCB layers for optimal thermal performance.

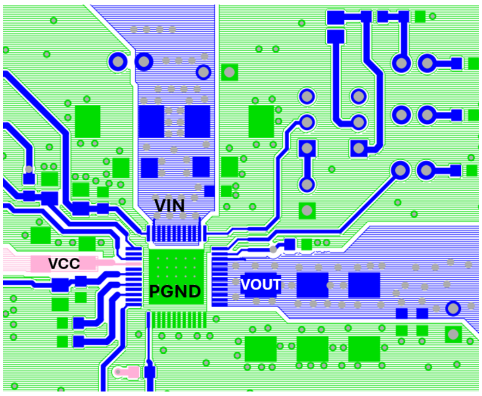


Figure 42. Layout Example

7. Radiation Tolerance

The ISL75055M is a radiation tolerant device for commercial space applications, Low Earth Orbits (LEO) applications, high altitude avionics, launch vehicles, and other harsh environments. This device's response to Total Ionizing Dose (TID) radiation effects and Single Event Effects (SEE) has been measured, characterized, and reported in the following sections. The ISL75055M30NEZ is Radiation Lot Acceptance Tested (RLAT) to 30krad(Si), and the ISL75055M50NEZ is RLAT to 50krad(Si).

7.1 Total Ionizing Dose (TID) Testing

7.1.1 Introduction

Total dose testing of the ISL75055M proceeded in accordance with the guidelines of MIL-STD-883 Test Method 1019. The experimental matrix consisted of 20 samples irradiated under bias and 19 samples irradiated with all pins grounded (unbiased). Three control units were used. Figure 43 shows the bias configuration. The devices were drawn from wafer lot F6XR21.1. All samples were packaged in the production 48Ld Plastic eTQFP.

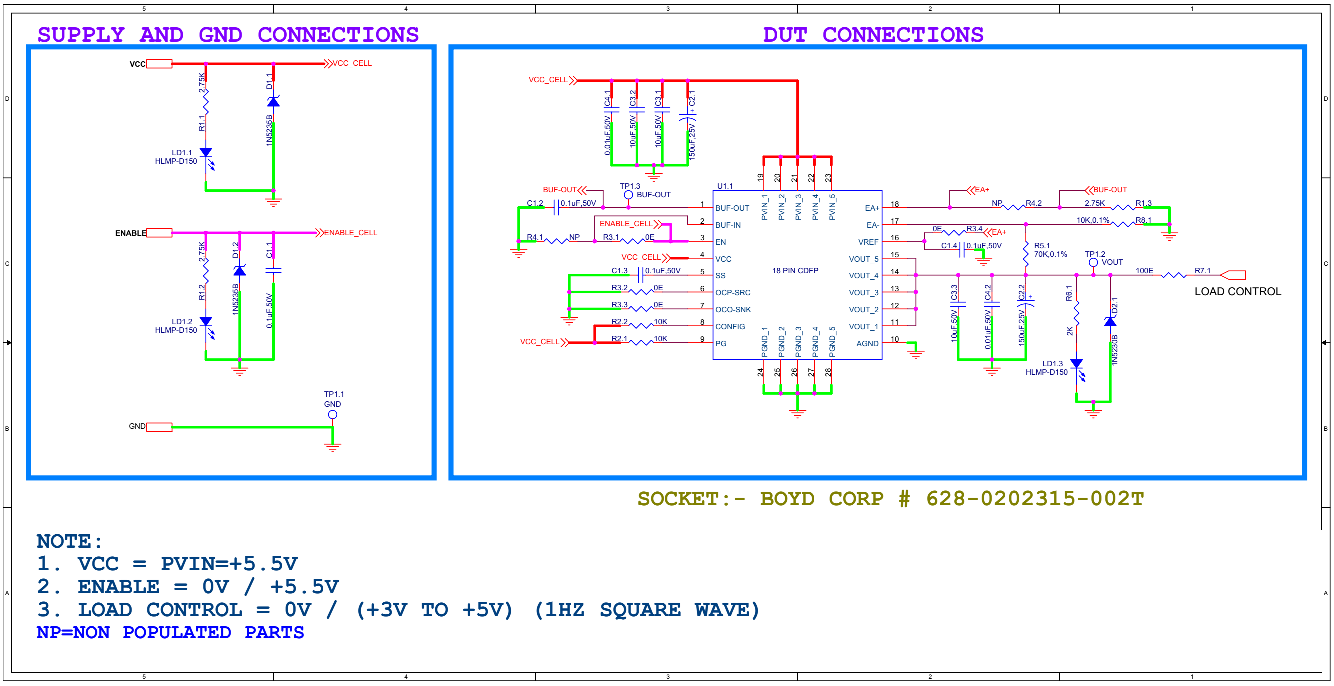


Figure 43. TID Testing Bias Configuration

7.1.2 Results

Table 1 summarizes the attributes data.

Table 1. Attributes Data

Dose Rate (rad(Si)/s)	Condition	Sample Size	Downpoint	Pass[1]	Fail
0.01	Biased (Figure 43)	20	Pre-irradiation	20	0
			10krad(Si)	20	0
			30krad(Si)	20	0
			50krad(Si)	20	0
0.01	Grounded	19	Pre-irradiation	19	0
			10krad(Si)	19	0
			30krad(Si)	19	0
			50krad(Si)	19	0

1. A 'Pass' indicates a device that passes all the datasheet specification limits.

The plots in Figure 44 through Figure 56 show data for key parameters at all downpoints. The plots show the sample size average as a function of the total dose for each irradiation condition. All parts showed excellent stability over irradiation.

7.1.3 Typical Radiation Performance

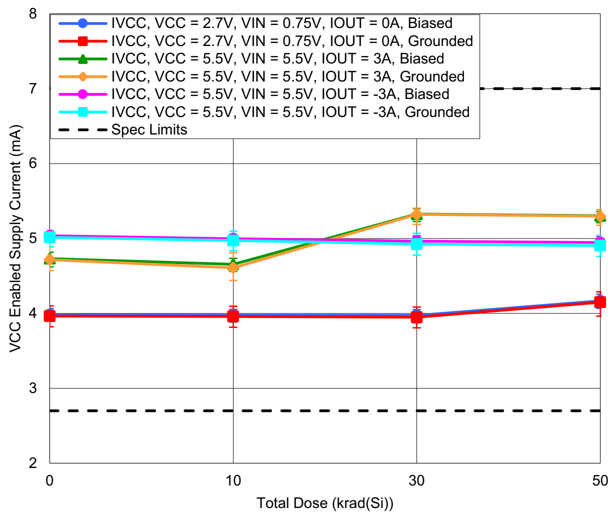


Figure 44. VCC Enabled Supply Current vs TID

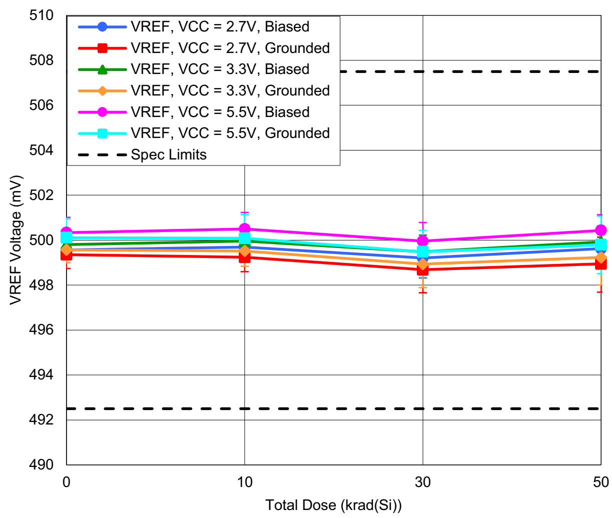


Figure 45. VREF_INT Voltage vs TID

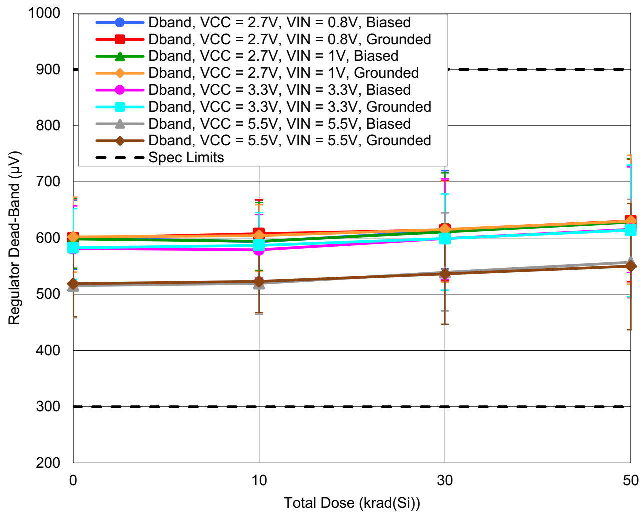


Figure 46. Regulator Dead-Band vs TID

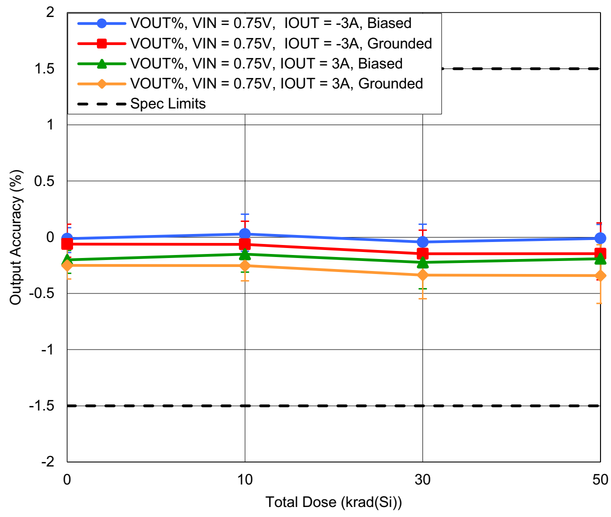


Figure 47. Output Accuracy with V_{CC} = 2.7V and V_{OUT} = 0.5V vs TID

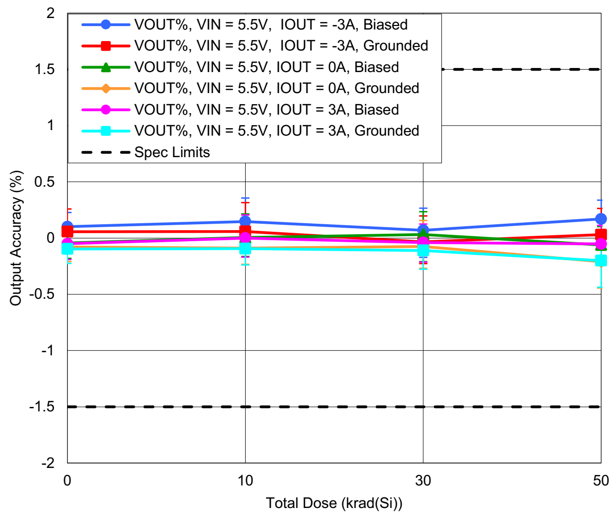


Figure 48. Output Accuracy with V_{CC} = 5.5V and V_{OUT} = 3.3V vs TID

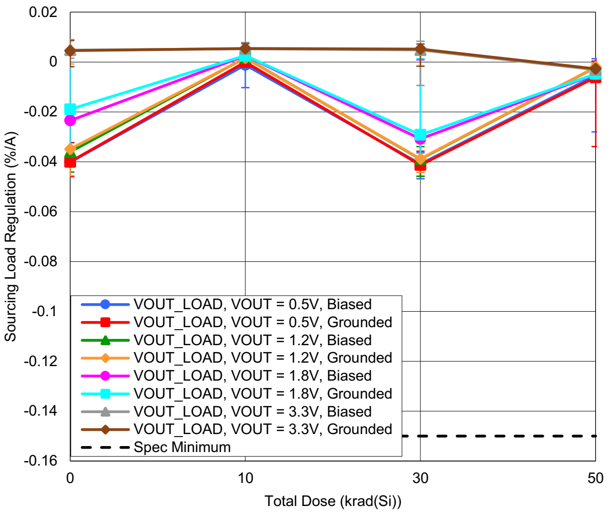


Figure 49. Sourcing Load Regulation with V_{CC} = the greater of 2.7V or VOUT+1.5V vs TID

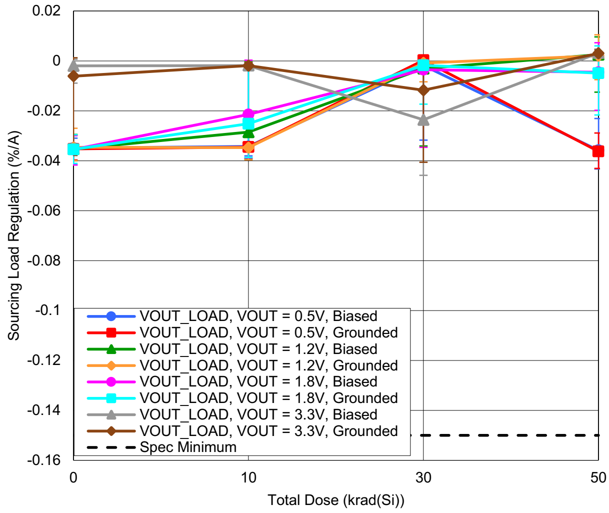


Figure 50. Sourcing Load Regulation with V_{CC} = 5.5V vs TID

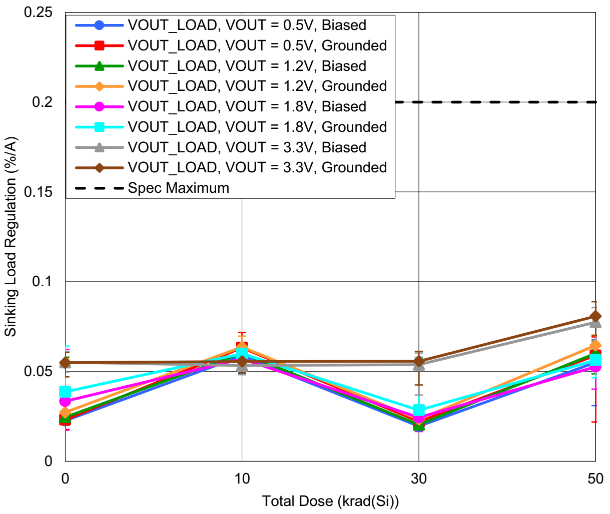


Figure 51. Sinking Load Regulation with V_{CC} = the greater of 2.7V or VOUT+1.5V vs TID

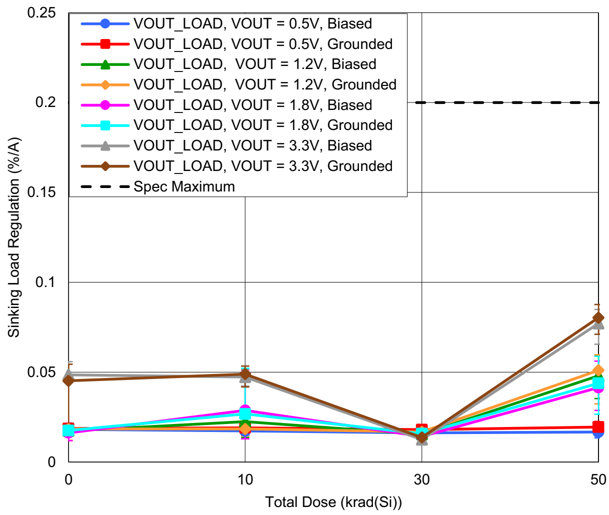


Figure 52. Sinking Load Regulation with V_{CC} = 5.5V vs TID

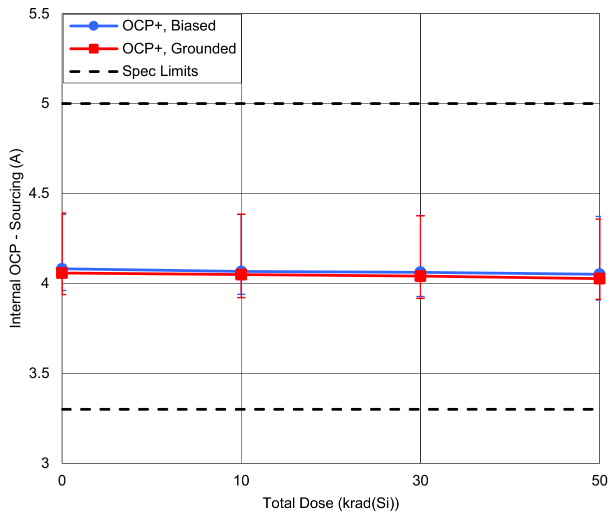


Figure 53. Internal OCP - Sourcing vs TID

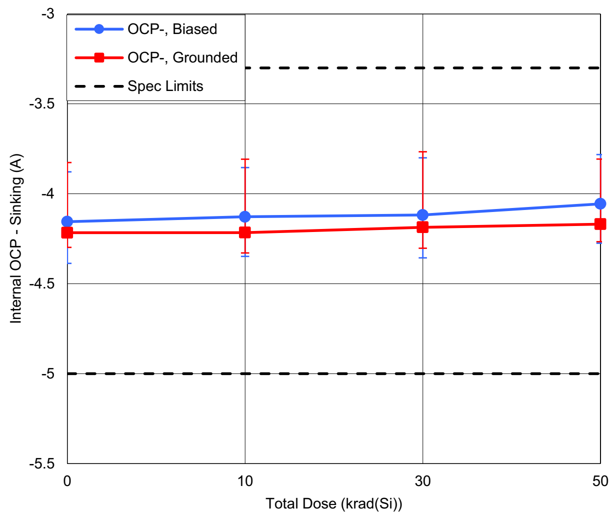


Figure 54. Internal OCP - Sinking vs TID

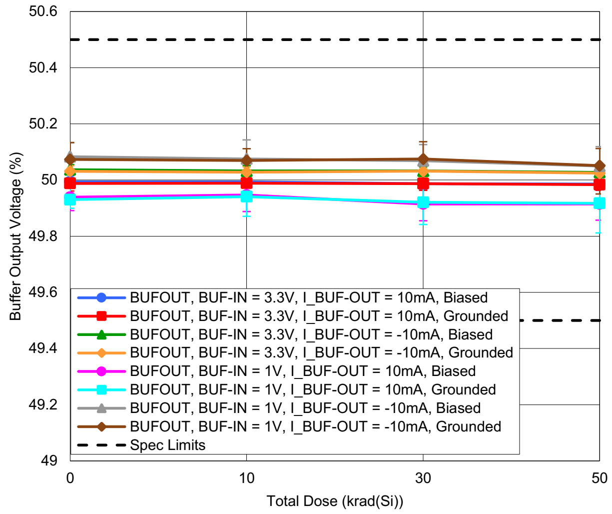


Figure 55. Buffer Output Voltage vs TID

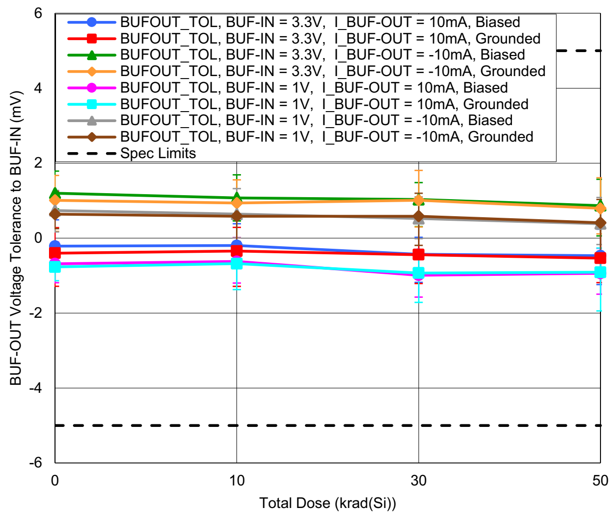


Figure 56. BUF-OUT Voltage Tolerance to BUF-IN vs TID

7.2 Single-Event Effects Testing

7.2.1 Introduction

The intense proton and heavy ion environment encountered in space applications can cause a variety of Single Event Effects (SEE) in electronic circuitry, including Single Event Upset (SEU), Single Event Transient (SET), Single Event Functional Interrupt (SEFI), Single Event Gate Rupture (SEGR), and Single Event Burnout (SEB), SEE can lead to system-level performance issues, including disruption, degradation, and destruction. Individual electronic components should be characterized for predictable and reliable space system operation to determine their SEE response. This section discusses the results of SEE testing on the ISL75055M.

7.2.2 Test Facility

SEE testing was performed at the Texas A&M University (TAMU) Radiation Effects Facility of the Cyclotron Institute heavy ion facility. The facility is coupled to a K500 super-conducting cyclotron that can generate a wide range of particle beams with the various energy, flux, and fluence levels required for advanced radiation testing. The Devices Under Test (DUTs) were in air with a 40mm air gap between them and the Aramica window for the ion beam. SEE testing was performed in April 2025 with normal incidence silver ions for an LET of

45.8MeV•cm^2/mg at the surface of the device. The LET of the ions in the active silicon layer ranged from 47.9MeV•cm^2/mg to 49.8MeV•cm^2/mg. Signals were communicated to and from the DUT test fixture through 20ft cables connecting to the control room.

7.2.3 Destructive Single Event Effects (DSEE) Results

DSEE testing was performed to determine the maximum LDO input voltage (V_{IN}) and analog bias voltage (V_{CC}) free from DSEEs at a die temperature of 125°C. The test board was laid out such that two parts could be irradiated simultaneously. During each run, the devices were exposed to heavy ions to a fluence of 1E7ions/cm^2.

To stress the entire device during DSEE testing, the BUF-IN voltage was set by a resistor divider between an external BUF-IN supply and VREF_INT, with BUF-OUT feeding into EA+. In this configuration, both the LDO and DDR terminator circuitry are exercised.

For VCC DSEE testing, V_{IN} was set to 2V, and V_{OUT} was set to 1V. I_{OUT} was switched between sourcing 3.3A and sinking 3.3A at 100Hz and 50% duty cycle. The voltage on BUF-IN was set to 1.25V and the voltage on BUF-OUT was set to 0.625V. There was no load on the buffer. EN was tied to VCC, and PG was pulled up to VCC using a 10kΩ resistor. V_{CC} was initially set to 5.5V and V_{CC} was increased in steps of 5% derating following each run. Testing concluded when V_{CC} reached 6.9V or the device exhibited a DSEE. A device was considered to have exhibited a DSEE if the output voltage at no load deviated by ±1% or the current on VCC at no load deviated by ±10%.

VIN DSEE testing was conducted in two sections, one with EN grounded and one with EN high.

VIN DSEE testing was performed with EN grounded to apply the maximum stress to the pass transistor as blocking mode is the worst-case condition for testing MOSFETs. For this testing, VOUT was tied to ground and there was no load. VCC was tied to ground. V_{IN} was initially set to 5.5V and was increased in steps of 5% derating. Testing concluded when V_{IN} reached 6.9V or the device exhibited a DSEE. A device was considered to have exhibited a DSEE if the current on VIN deviated by ±50%.

For VIN DSEE testing with EN high, the device under test sourced 3.3A. V_{CC} was set to 6.2V. V_{IN} was initially set to 5.5V and V_{OUT} was initially set to 4V. V_{IN} was increased in steps of 5% derating. V_{OUT} was simultaneously increased to maintain a 1.5V differential between V_{IN} and V_{OUT}. To increase V_{OUT} without making a board modification between runs, V_{OUT} was set using an external power supply connected to EA-. BUF-IN was increased following each run from a starting voltage of 1.33V to a maximum voltage of 1.8V. Testing concluded when V_{IN} reached the maximum voltage attained during VIN DSEE testing with EN = 0V or the device exhibited a DSEE. A device was considered to have exhibited a DSEE if the output voltage at no load deviated by ±2%, the current on VCC deviated by ±5%, or the current on VIN deviated by ±15%.

DSEE testing indicates that the ISL75055M should be operated with a maximum of V_{IN} = 6.2V and V_{CC} = 6.9V regardless of whether EN is high or low at 125°C and 45.8MeV•cm^2/mg. BUF-IN was exercised to 1.57V and passed testing.

7.2.4 SET Results

The ISL75055M was tested for SETs in both an LDO and DDR terminator configuration at 25°C and an LET of 45.8MeV•cm^2/mg. Each run was to a fluence of 1E7ions/cm^2.

For SET testing in a DDR configuration, the board was set up to irradiate one part at a time. BUF-IN was supplied directly by VIN, and a 1kΩ and 0.680µF filter was applied at the input of BUF-IN. A 0.680µF bypass capacitor was applied to BUF-OUT, and BUF-OUT fed into EA+. The devices were tested under six different test conditions as shown in Table 2. For each test condition, the load on the buffer was switched between -10mA and 10mA at 100Hz and a 50% duty cycle. EN was tied to VCC. PG was pulled up to VCC though a 10kΩ resistor.

Table 2. DDR SET Test Conditions

Test Condition	Number of Devices Tested	Total Fluence (ions/cm^2)	V_{CC} (V)	V_{IN} (V)	BUF-IN (V)	V_{OUT} (V)	BUF-OUT (V)	I_{OUT} (A)
#1	4	4E7	2.7	1.2	1.2	0.6	0.6	3
#2	4	4E7	5.5	1.2	1.2	0.6	0.6	3
#3	4	4E7	2.7	1.2	1.2	0.6	0.6	-3
#4	4	4E7	5.5	1.2	1.2	0.6	0.6	-3
#5	4	4E7	5.5	5.5	5.5	2.75	2.75	0.3
#6	4	4E7	5.5	5.5	5.5	2.75	2.75	-0.3

During irradiation, devices were monitored for VOUT SETs, BUF-OUT SETs, Differential SETs, PG SETs, and SEFIs. A VOUT SET was defined as an event when V_{OUT} deviated beyond ±2% of its operating value. A BUF-OUT SET was defined as an event when BUF-OUT deviated beyond ±2% of its operating value. A Differential SET was defined as an event when the differential between V_{OUT} and BUF-OUT deviated beyond ±40mV, a condition forbidden by the JEDEC DDR specification. A PG SET was defined as an event when PG pulled low but the device did not enter soft-start, and there was no loss of VOUT regulation. A SEFI was defined as an event when PG pulled low and there was a loss of V_{OUT} regulation. VOUT and BUF-OUT SETs were captured with a trigger set to capture events in which V_{OUT} or BUF-OUT, respectively, deviated beyond ±2% of their operating values. Differential SETs were captured with a trigger set to capture events in which the differential between V_{OUT} and BUF-OUT deviated beyond 40mV. The differential between V_{OUT} and BUF-OUT was monitored using a differential amplifier. PG SETs and SEFIs were captured with a trigger set to capture events when PG fell below 1.36V.

Table 3. DDR SET Test Summary at 45.8MeV·cm^2/mg

Test Condition	# of DUTs	Total Fluence (ions/cm^2)	# of VOUT SETs	# of BUF-OUT SETs	# of Differential SETs	# of PG SETs	# of SEFIs
#1	4	4E7	0	0	0	0	0
#2	4	4E7	0	0	0	0	0
#3	4	4E7	0	0	0	0	0
#4	4	4E7	0	0	0	0	0
#5	4	4E7	0	0	0	0	0
#6	4	4E7	0	0	0	0	0

No VOUT SETs, BUF-OUT SETs, Differential SETs, PG SETs, or SEFIs were observed during testing.

For SET testing in an LDO configuration, the board was set up to irradiate two parts at a time. A 0.068µF bypass capacitor was applied to VREF_INT, and VREF_INT fed into EA+. The devices were tested under eight different test conditions as shown in Table 4. For each test condition, EN was tied to VCC. PG was pulled up to VCC though a 10kΩ resistor.

Table 4. LDO SET Test Conditions

Test Condition	Number of Devices Tested	Total Fluence (ions/cm^2)	V_{CC}(V)	V_{IN} (V)	V_{OUT} (V)	I_{OUT} (A)
#1	4	4E7	2.7	1.5	1	3
#2	4	4E7	5.5	1.5	1	3

Table 4. LDO SET Test Conditions (Cont.)

Test Condition	Number of Devices Tested	Total Fluence (ions/cm^2)	V_{CC}(V)	V_{IN} (V)	V_{OUT} (V)	I_{OUT} (A)
#3	4	4E7	2.7	1.5	1	-3
#4	4	4E7	5.5	1.5	1	-3
#5	4	4E7	2.7	5.5	1	0.3
#6	4	4E7	5.5	5.5	1	0.3
#7	4	4E7	2.7	5.5	1	-0.3
#8	4	4E7	5.5	5.5	1	-0.3

During irradiation, devices were monitored for VOUT SETs, PG SETs, and SEFIs. A VOUT SET was defined as an event when V_{OUT} deviated beyond ±2% of its operating value. A PG SET was defined as an event when PG pulled low but the device did not enter soft-start, and there was no loss of VOUT regulation. A SEFI was defined as an event when PG pulled low and there was a loss of VOUT regulation. VOUT SETs were captured with a trigger set to capture events when V_{OUT} deviated beyond ±2% of its operating value. PG SETs and SEFIs were captured with a trigger set to capture events when PG fell below 1.5V.

Table 5. LDO SET Test Summary at 45.8MeV·cm^2/mg

Test Condition	# of DUTs	Total Fluence (ions/cm^2)	# of VOUT SETs	# of PG SETs	# of SEFIs
#1	4	4E7	0	0	0
#2	4	4E7	0	0	0
#3	4	4E7	0	0	0
#4	4	4E7	0	0	0
#5	4	4E7	0	0	0
#6	4	4E7	0	0	0
#7	4	4E7	0	0	0
#8	4	4E7	0	0	0

No VOUT SETs, PG SETs, or SEFIs were observed during testing.

7.2.5 Conclusion

The ISL75055M was found to be free of DSEE when operated with a maximum of V_{IN} = 6.2V and V_{CC} = 6.9V at 125°C regardless of whether EN is high or low at 45.8MeV•cm^2/mg.

The ISL75055M did not exhibit any VOUT SETs, BUF-OUT SETs, Differential SETs, PG SETs, or SEFIs when tested at 45.8MeV•cm^2/mg in either an LDO or DDR terminator configuration. Therefore, the ISL75055M has excellent radiation performance for radiation tolerant applications.

8. Package Outline Drawing

The package outline drawing is located at the end of this document and is accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

9. Ordering Information

Part Number[1]	Part Marking	Radiation Lot Acceptance Testing	Package Description[2] (RoHS Compliant)	Pkg. Dwg #	MSL Rating[3]	Carrier Type	Temp. Range
ISL75055M30NEZ	ISL75055 MNEZ	LDR to 30krad(Si)	48Ld Plastic eTQFP	Q48.7x7C	3	Tray	-55 to +125°C
ISL75055M30NEZ-T						Reel, 1k	
ISL75055M50NEZ	ISL75055 MNEZ	LDR to 50krad(Si)	48Ld Plastic eTQFP	Q48.7x7C	3	Tray	-55 to +125°C
ISL75055M50NEZ-T						Reel, 1k	
ISL75055MEV1Z	Evaluation Board for DDR VTT Termination and Standard LDO Applications with TQFP package						

1. These Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. For the Pb-Free Reflow Profile, see TB493.
3. For more information about Moisture Sensitivity Level (MSL), see TB363.

10. Revision History

Revision	Date	Description
1.02	Oct 24, 2025	Updated Symbol Pin Information (ECAD) section.
1.01	Oct 21, 2025	Updated the test condition for VREF_INT Voltage. Updated Regulator Dead-Band +25C (Post Rad) Max Limit.
1.00	Aug 28, 2025	Initial release

A. ECAD Design Information

This information supports the development of the PCB ECAD model for this device. It is intended to be used by PCB designers.

A.1 Part Number Indexing

Orderable Part Number	Number of Pins	Package Type	Package Code/POD Number
ISL75055M30NEZ	48	TQFP-EP	Q48.7x7C
ISL75055M30NEZ-T	48	TQFP-EP	Q48.7x7C
ISL75055M50NEZ	48	TQFP-EP	Q48.7x7C
ISL75055M50NEZ-T	48	TQFP-EP	Q48.7x7C

A.2 Symbol Pin Information

A.2.1 48-TQFP-EP

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
1	BUF-IN	Input	-
2	NC	Passive	-
3	EN	Input	-
4	VCC	Power	-
5	NC	Passive	-
6	SS	Output	-
7	NC	Passive	-
8	OCP-SRC	Input	-
9	NC	Passive	-
10	OCP-SNK	Input	-
11	NC	Passive	-
12	CONFIG	Input	-
13	PGND	Power	-
14	PGND	Power	-
15	PGND	Power	-
16	PGND	Power	-
17	PGND	Power	-
18	PGND	Power	-
19	PGND	Power	-
20	PGND	Power	-
21	PGND	Power	-
22	PGND	Power	-
23	PGND	Power	-
24	AGND	Power	-
25	VOUT	Power	-
26	VOUT	Power	-
27	VOUT	Power	-
28	VOUT	Power	-
29	VOUT	Power	-
30	VOUT	Power	-
31	VOUT	Power	-
32	VOUT	Power	-
33	VOUT	Power	-
34	VOUT	Power	-
35	VREF_INT	Power	-
36	EA-	Input	-
37	EA+	Input	-
38	VIN	Power	-
39	VIN	Power	-
40	VIN	Power	-

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
41	VIN	Power	-
42	VIN	Power	-
43	VIN	Power	-
44	VIN	Power	-
45	VIN	Power	-
46	VIN	Power	-
47	VIN	Power	-
48	BUF-OUT	Output	-
EPAD49	PGND	Power	-

A.3 Symbol Parameters

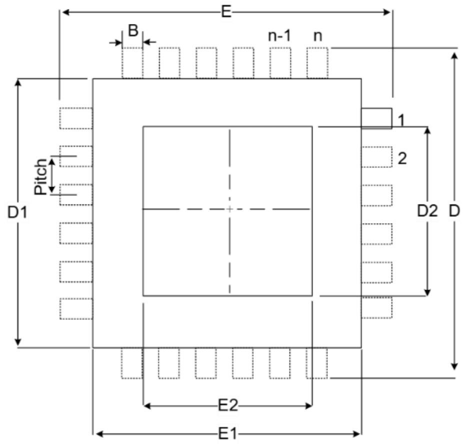
Orderable Part Number	Qualification	Radiation Qualification	LDR	Mounting Type	RoHS	Min Operating Temperature	Max Operating Temperature	Min Input Voltage	Max Input Voltage	Output Current
ISL75055M30NEZ	Space	Radiation Tolerant	30 krad(Si)	SMD	Compliant	-55 °C	125 °C	0.75 V	5.5 V	3 A
ISL75055M30NEZ-T	Space	Radiation Tolerant	30 krad(Si)	SMD	Compliant	-55 °C	125 °C	0.75 V	5.5 V	3 A
ISL75055M50NEZ	Space	Radiation Tolerant	50 krad(Si)	SMD	Compliant	-55 °C	125 °C	0.75 V	5.5 V	3 A
ISL75055M50NEZ-T	Space	Radiation Tolerant	50 krad(Si)	SMD	Compliant	-55 °C	125 °C	0.75 V	5.5 V	3 A

A.4 Footprint Design Information

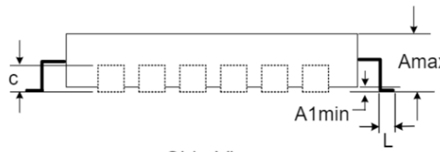
A.4.1 48-TQFP-EP

IPC Footprint Type	Package Code/ POD Number	Number of Pins
QFP	Q48.7x7C	48

Description	Dimension	Value (mm)	Diagram
Minimum lead span (vertical side)	Dmin	8.90	
Maximum lead span (vertical side)	Dmax	9.10	
Minimum lead span (horizontal side)	Emin	8.90	
Maximum lead span (horizontal side)	Emax	9.10	
Minimum body span (vertical side)	D1min	6.90	
Maximum body span (vertical side)	D1max	7.10	
Minimum body span (horizontal side)	E1min	6.90	
Maximum body span (horizontal side)	E1max	7.10	
Minimum Lead Width	Bmin	0.17	
Maximum Lead Width	Bmax	0.27	
Number of pins (vertical side)	PinCountD	12	
Number of pins (horizontal side)	PinCountE	12	
Distance between the center of any two adjacent pins	Pitch	0.50	
Location of pin 1; S2 = corner of D side, C1 = center of E side	Pin1	S2	
Minimum thermal pad size (vertical side)	D2min	5.20	
Maximum thermal pad size (vertical side)	D2max	5.40	
Minimum thermal pad size (horizontal side)	E2min	5.20	
Maximum thermal pad size (horizontal side)	E2max	5.40	
Minimum Lead Length	Lmin	0.45	
Maximum Lead Length	Lmax	0.75	
Maximum Height	Amax	1.2	
Minimum Standoff Height	A1min	0.05	
Minimum Lead Thickness	cmin	0.09	
Maximum Lead Thickness	cmax	0.20	

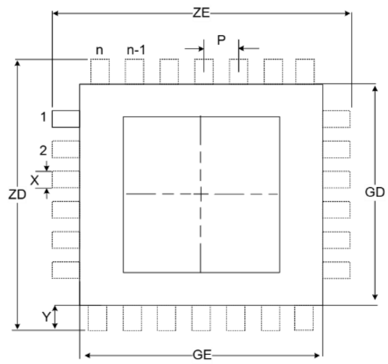


Bottom View



Side View

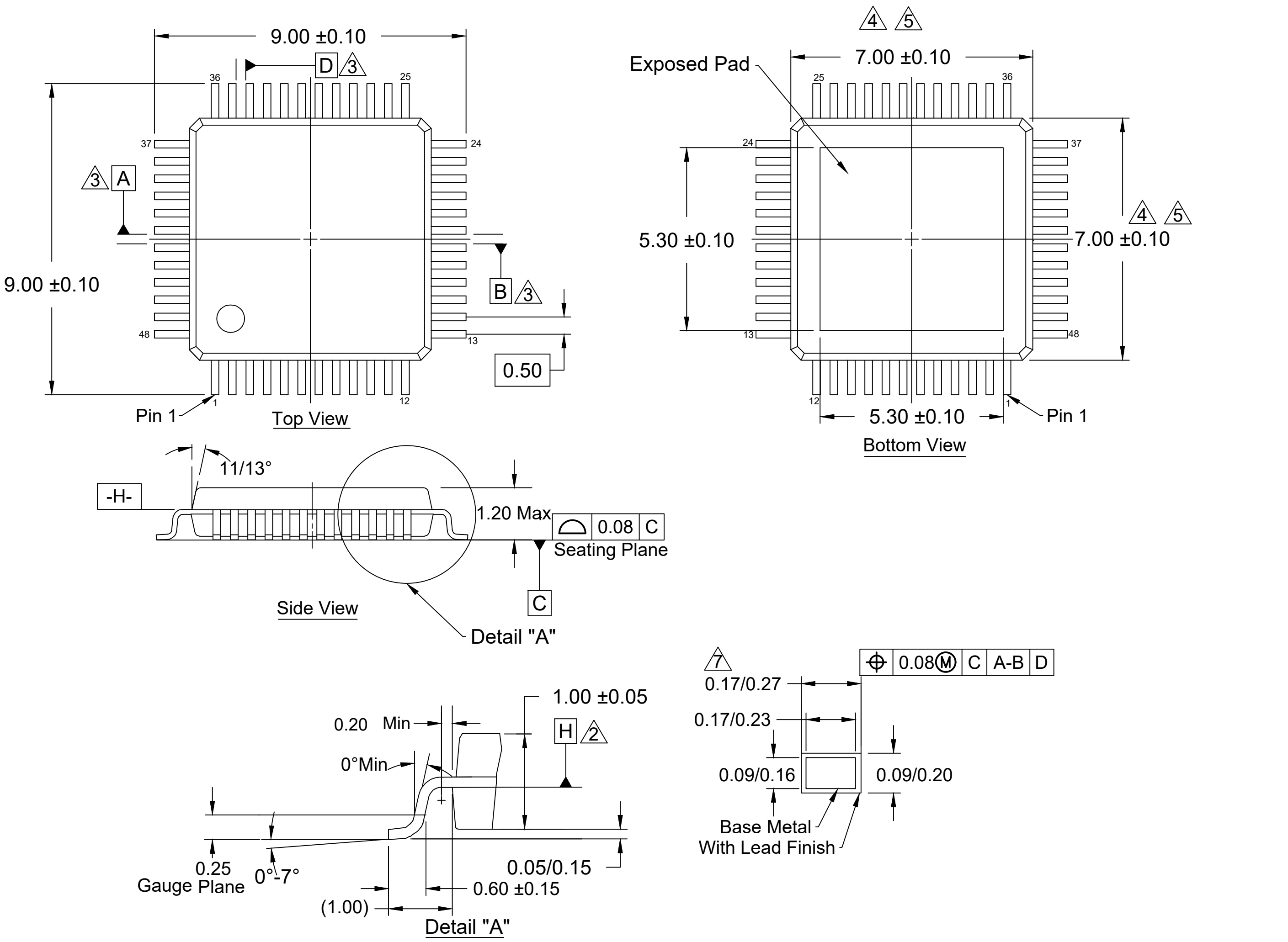
Recommended Land Pattern			
Description	**Dimension**	**Value (mm)**	**Diagram**
Distance between left pad toe to right pad toe (horizontal side)	ZE	9.60	
Distance between top pad toe to bottom pad toe (vertical side)	ZD	9.60	
Distance between left pad heel to right pad heel (horizontal side)	GE	7.20	
Distance between top pad heel to bottom pad heel (vertical side)	GD	7.20	
Pad Width	X	0.30	
Pad Length	Y	1.20	

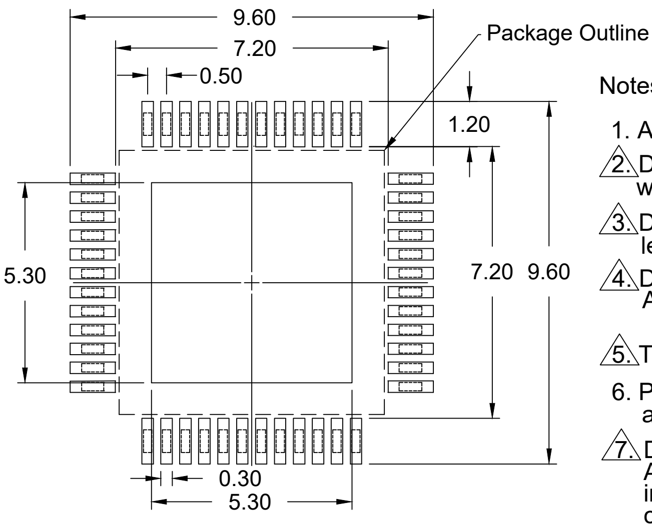


PCB Top View

Package Outline Drawing

48 Thin Plastic Quad Flatpack Exposed Pad Packages (TQFP-EP)
POD Number: Q48.7x7C, Revision: 01, Date Created:May 6, 2025





Recommended Land Pattern

Notes:

1. All dimensioning and tolerancing conform to ANSI Y14.5-1982.
2. Datum plane H located at mold parting line and coincident with lead, where lead exits plastic body at bottom of parting line.
3. Datums A-B and D to be determined at centerline between leads where leads exit plastic body at datum plane H.
4. Dimensions do not include mold protrusion. Allowable mold protrusion is 0.254 mm .
5. These dimensions to be determined at datum plane H.
6. Package top dimensions are smaller than bottom dimensions and top of package does not overhang bottom of package.
7. Dimension does not include dambar protrusion. Allowable dambar protrusion is 0.08mm total in excess of the dimension at maximum material condition. Dambar cannot be located on the lower radius or the foot.
8. Controlling dimension: millimeter.
9. This outline conforms to jedec publication 95 registration MS-026, variation ABC-HD
10. DImensions in ( ) are for reference only.

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