ISL76534

Ultra-Low Power 14-Channel Programmable Gamma Buffer with Integrated EEPROM

FN8866
Rev 0.00
July 27, 2016

The ISL76534 is a programmable gamma buffer for TFT-LCDs featuring ultra-low power operation. The ISL76534 contains an I^2C programmable, 10-bit, 14-channel gamma reference voltage generator with buffered outputs, a 10-bit programmable V_{COM} calibrator, a high output current V_{COM} amplifier, and internal EEPROM to store all reference voltage data. The EEPROM features an endurance of 10,000 write cycles and a data retention of 20 years at 105°C.

Combining gamma and V_{COM} reference voltage generators with low power operation and EEPROM, the ISL76534 provides a complete reference voltage solution ideal for TFT-LCD displays.

The ISL76534 is available in a super thin (height = 0.4mm maximum) 28 Ld 4mmx5mm X2QFN thermally enhanced package. The device is specified for operation across the ambient temperature -40°C to +105°C.

Applications

- Automotive infotainment display
- Automotive Center Information Display (CID)
- Automotive smart mirrors
- Automotive instrument cluster display
- Automotive TFT-LCD display

Features

- 14-channel gamma references, 10-bit resolution with buffered outputs
- 1-channel V_{COM} calibrator with 10-bit resolution
- High output current V_{COM} amplifier
- Ultra-low power operation, ideal for automotive displays: Typical quiescent power, 12mW at 8V AV_{DD}
- EEPROM data retention: 20 years at 105°C
- EEPROM endurance: 10,000 write cycles
  - Read/write capable over 2.25V to 3.6V D_{VDD} range
- 6.3V to 19V analog supply operating range
- 2.25V to 3.6V digital supply operating range
- Power Supply Rejection Ratio (PSRR): 75dB typical
- 28 Ld 4mmx5mm super thin X2QFN package
- Pb-free (RoHS compliant)
- AEC-Q100 qualified

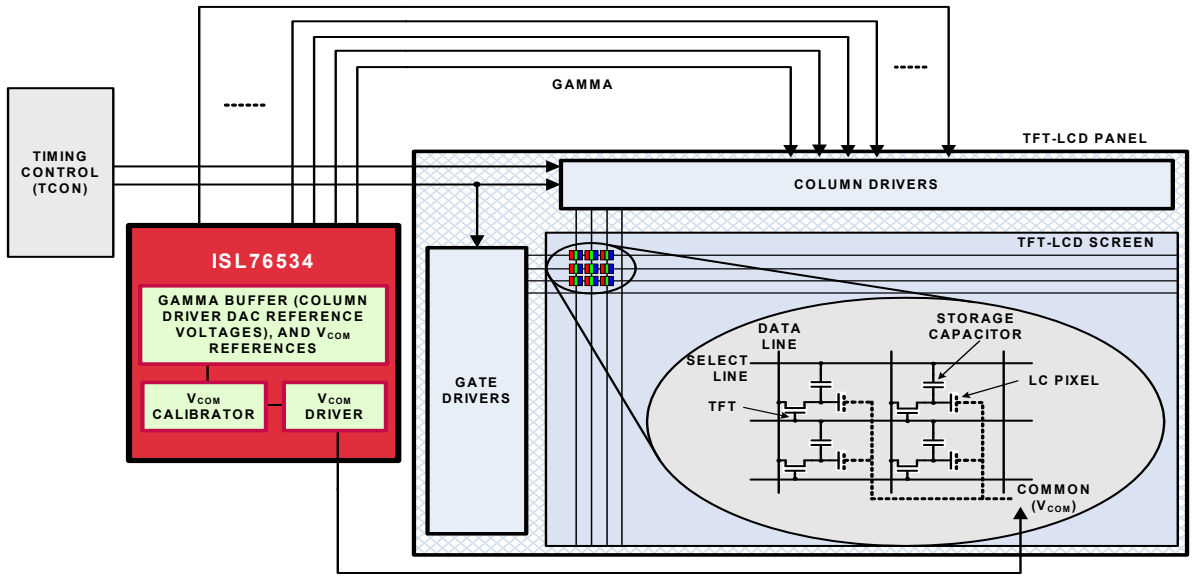


FIGURE 1. TYPICAL APPLICATION: TFT-LCD GAMMA REFERENCE VOLTAGE GENERATOR

Table of Contents

Block Diagram

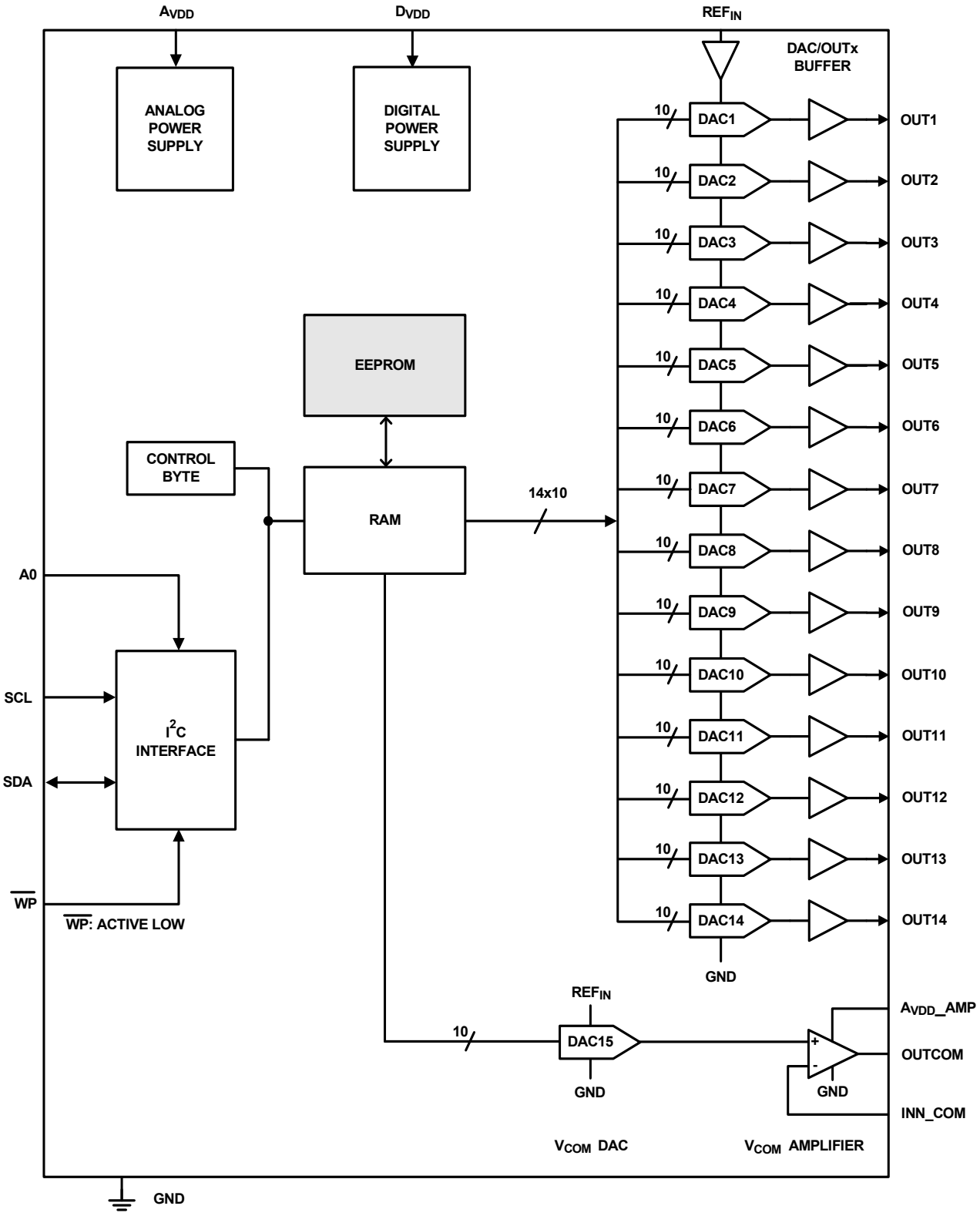


FIGURE 2. BLOCK DIAGRAM

Ordering Information

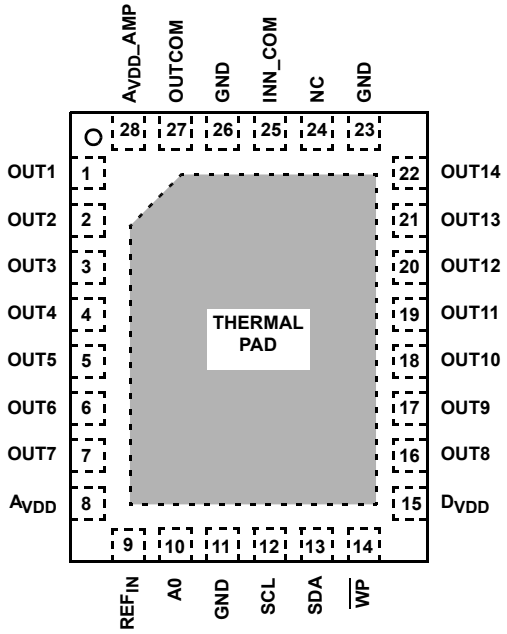
PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (RoHS COMPLIANT)	PKG. DWG. #
ISL76534ARXZ	76534 ARXZ	-40 to +105	28 Ld X2QFN	L28.4x5D
ISL76534EVAL1Z	Evaluation Board			

NOTES:

1. Add “-T13” suffix for 6k unit or “-T7A” suffix for 250 unit Tape and Reel options. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu-Ag plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL76534. For more information on MSL please see tech brief TB363.

Pin Configuration

ISL76534
(28 LD 4mmx5mm X2QFN)
TOP VIEW



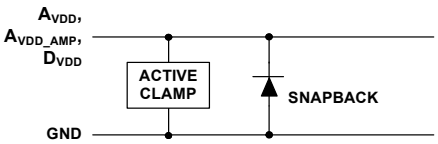
Note: Thermal pad is electrically connected to GND

Pin Descriptions

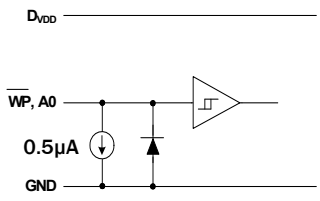
PIN #	PIN NAME	PIN TYPE	PIN FUNCTION	EQUIVALENT CIRCUIT
1, 2, 3, 4, 5, 6, 7, 16, 17, 18, 19, 20, 21, 22	OUTx	Analog Output	10-bit Programmable DAC outputs	5
8	A_{VDD}	Analog Power	Analog power supply. Include a bulk 4.7µF capacitor, and a local 0.1µF ceramic bypass capacitor to the system ground. Place the 0.1µF as close to the pin as possible; the bulk capacitor may be placed farther away from the IC.	1
9	REF_{IN}	Analog Input	High-impedance, buffered reference voltage input for 10-bit DACs. Include a local 0.1µF ceramic bypass capacitor to the system ground; place as close to the pin as possible.	4
10	A0	Digital Input	Determines the device’s 7-bit I^2C device address: 0: Device Address = 0x74 (this is the default setting if pin is left floating) 1: Device Address = 0x75 (pull-up pin externally) Note: pin has an internal pull-down to GND of 10MΩ (typical)	2

Pin Descriptions (Continued)

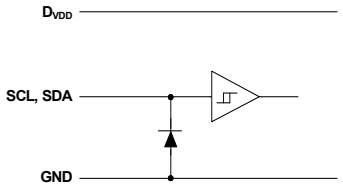
PIN #	PIN NAME	PIN TYPE	PIN FUNCTION	EQUIVALENT CIRCUIT
11, 23, 26	GND	Power	Ground	
12	SCL	Digital Input	I^2C clock (high impedance input)	3
13	SDA	Digital I/O	I^2C data (high impedance input/open-drain output)	3
14	WP	Digital Input	I^2C Write Protection, active low: 0: Prevent I^2C data writes to internal DAC registers and EEPROM (this is the default setting if pin is left floating) 1: Allow I^2C data writes to internal DAC registers and EEPROM (pull-up pin externally) Note: pin has an internal pull-down to GND of 10MΩ (typical)	2
15	D_{VDD}	Digital Power	Digital power supply. Include a local 0.1µF ceramic bypass capacitor to the system ground; place as close to the pin as possible.	1
24	NC		Not Connected Internally. Acceptable to leave pin floating.	
25	INN_COM	Analog Input	V_{COM} amplifier inverting input	6
27	OUTCOM	Analog Output	V_{COM} amplifier output	7
28	A_{VDD}_AMP	Analog Power	Analog power supply for V_{COM} amplifier. It is acceptable that A_{VDD}_AMP is tied to A_{VDD}, or set to a lower voltage: A_{VDD}_AMP ≤ A_{VDD}. Include a bulk 4.7µF capacitor (or share with the A_{VDD} bulk), and a local 0.1µF ceramic bypass capacitor to the system ground. Place the 0.1µF as close to the pin as possible; the bulk capacitor may be placed farther away from the IC.	1
-	THERMAL PAD	GND	Thermal pad. Electrically connected to GND (pins 11, 23, 26). Connect to ground plane on PCB to maximize thermal performance.	



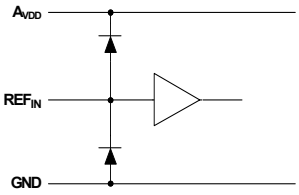
CIRCUIT 1



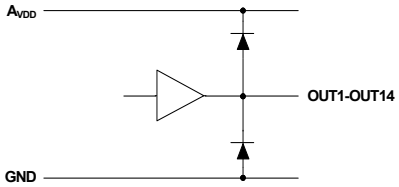
CIRCUIT 2



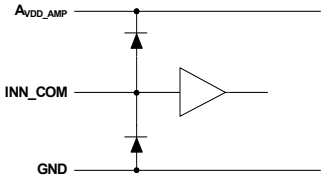
CIRCUIT 3



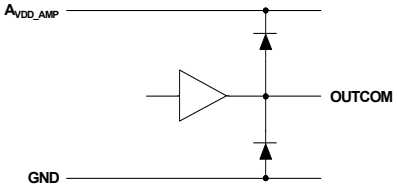
CIRCUIT 4



CIRCUIT 5



CIRCUIT 6



CIRCUIT 7

Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage
- Between A_{VDD} and GND ..... +21V
- A_{VDD}_AMP to GND ..... A_{VDD} +0.3V
- Between D_{VDD} and GND ..... +4.5V

Maximum Output Voltage
- [OUT1-OUT14] ..... A_{VDD}
- OUTCOM ..... A_{VDD_AMP}
- SDA ..... +4.5V

Maximum Input Voltage
- REF_{IN} ..... A_{VDD}
- INN_COM ..... A_{VDD_AMP}
- SCL, SDA, A0, $\overline{WP}$ ..... +4.5V

Maximum Continuous Output Current per Channel
- OUT1-OUT14 ..... ±60mA
- OUTCOM ..... ±100mA

Maximum Total Output Current
- OUT1-OUT14 ..... ±250mA

ESD Ratings
- Human Body Model (Tested per AEC-Q100-002) 3kV
- Machine Model (Tested per AEC-Q100-003) 250V
- Charged Device Model (Tested per AEC-Q100-011) 2kV

Latch-up (Tested per AEC-Q100-004) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
28 Ld X2QFN (Notes 4, 5)	37	1.5

Power Dissipation ..... See page 21
Maximum Die Temperature ..... +150°C
Storage Temperature ..... -65°C to +150°C
Pb-free Reflow Profile ..... see TB493

Recommended Operating Conditions

Operating Range
- A_{VDD} ..... 6.3V to 19V
- A_{VDD_AMP} ..... 4.5V to A_{VDD}
- D_{VDD} ..... 2.25V to 3.6V

Reference Voltage Range
- REF_{IN} to GND ..... 5V to A_{VDD}

Ambient Operating Temperature ..... -40°C to +105°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

A_{VDD} = A_{VDD_AMP} = 15V, D_{VDD} = 3.3V, REF_{IN} = 14.75V, T_A = +25°C, unless otherwise specified. **Boldface limits apply across the operating temperature range, -40°C to +105°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
SUPPLY						
Analog Supply Voltage	A_{VDD}		**6.3**		**19**	V
Analog Supply Voltage for V_{COM} Amp	A_{VDD_AMP}		**4.5**		**A_{VDD}**	V
Digital Supply Voltage	D_{VDD}		**2.25**		**3.6**	V
Analog Supply Current	I_{AVDD}	A_{VDD} = 8V, no load		1.00	**1.8**	mA
		A_{VDD_AMP} = 8V, no load		0.40	**0.75**	mA
		A_{VDD} = 15V, no load		1.30	**2.5**	mA
		A_{VDD_AMP} = 15V, no load		0.60	**1.2**	mA
Digital Supply Current	I_{DVDD}			190	**330**	µA
DAC High Reference Voltage	V_{REFIN}				**A_{VDD}**	V
Undervoltage Lockout for A_{VDD}	UVLO	A_{VDD} rising - OUTCOM, OUTx enabled	**3.9**	4.3	**4.5**	V
		A_{VDD} falling - OUTCOM, OUTx disabled	**3.7**	4.0	**4.3**	V
		Hysteresis	**200**	330	**500**	mV
ANALOG						
Highest Output Voltage for OUT1-OUT14	V_{OH}	REF_{IN} = A_{VDD}, DAC = 1023, I_{LOAD} = +5mA	**REF_{IN} - 0.150**	REF_{IN} - 0.100		V
Highest Output Voltage for OUTCOM		REF_{IN} = A_{VDD}, DAC = 1023, A_V = +1, I_{LOAD} = +5mA	**REF_{IN} - 0.100**	REF_{IN} - 0.050		V
Lowest Output Voltage for OUT1-OUT14	V_{OL}	DAC = 0, I_{LOAD} = -5mA		GND + 0.085	**GND + 0.150**	V
Lowest Output Voltage for OUTCOM		DAC = 0, A_V = +1, I_{LOAD} = -5mA		GND + 0.050	**GND + 0.100**	V

Electrical Specifications A_{VDD} = A_{VDD}_AMP = 15V, D_{VDD} = 3.3V, REF_{IN} = 14.75V, T_A = +25°C, unless otherwise specified. **Boldface limits apply across the operating temperature range, -40°C to +105°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
Power Supply Rejection Ratio	PSRR	OUT1-OUT14: OUTx = 0.5*A_{VDD} A_{VDD} varied from 14V to 16V	**55**	75		dB
		OUTCOM: OUTCOM = 0.5*A_{VDD} A_{VDD}_AMP varied from 14V to 16V	**50**	70		dB
DAC Integral Non-Linearity	INL	DAC1 through DAC14	**-2**	0	**2**	LSB
		DAC15 (OUTCOM)	**-2**	0	**2**	LSB
Input Leakage Current of REF_{IN}	I_{L_REF}	REF_{IN} = 0.5*A_{VDD}	**-1**	0	**1**	µA
Input Leakage Current of V_{COM} Amplifier	I_{L_INN}	V_{COM} Amplifier: INN = 0.5*A_{VDD}	**-1**	0	**1**	µA
Short-Circuit Current	I_{SC}	OUT1-OUT14: OUTx = V_{OH}, OUTx short to GND (source) through 10Ω	**170**	230	**400**	mA
		OUT1-OUT14: OUTx = V_{OL}, OUTx short to A_{VDD} (sink) through 10Ω	**150**	200	**400**	mA
		V_{COM} Amplifier (OUTCOM): OUTx = 0.5*A_{VDD}_AMP, short to GND (source) through 10Ω	**400**	530	**700**	mA
		V_{COM} Amplifier (OUTCOM): OUTx = 0.5*A_{VDD}_AMP, short to A_{VDD}_AMP (sink) through 10Ω	**450**	570	**750**	mA
Load Regulation	REG	OUT1-OUT14: I_{LOAD} = ±5mA step	**0**	1.5	**5**	mV/mA
		OUTCOM: I_{LOAD} = ±5mA step	**0**	1.5	**5**	mV/mA
Slew Rate	SR	OUT1-OUT14: Full-scale DAC code change	**2**	5	**40**	V/µs
		V_{COM} amplifier: A_V = -1, 0.5V ≤ OUTx ≤ 5.5V, C_L = 10pF to GND	**4**	10	**40**	V/µs
V_{COM} Amplifier Bandwidth	BW	A_V = -1, OUTx = 4V, R_L = 10kΩ || C_L = 10pF to GND		5		MHz
Time to Load EEPROM Data to DAC Registers at Power-ON	$t_{Data\_loading}$	Start of EEPROM loading to when OUTx is enabled, (Note 7)		6		ms
DIGITAL						
Logic '1' Input Voltage	V_{IH}	SCL, SDA, A0, $\overline{WP}$	**0.8*D_{VDD}**			V
Logic '0' Input Voltage	V_{IL}	SCL, SDA, A0, $\overline{WP}$			**0.2 * D_{VDD}**	V
I^2C SCL Clock Frequency	f_{CLK}	(Note 8)			**400**	kHz
Input Leakage Current	I_L	SCL, SDA, A0, $\overline{WP}$: at GND	**-1**	0	**1**	µA
		SCL, SDA: at D_{VDD}	**-1**	0	**1**	µA
		A0, $\overline{WP}$: at D_{VDD}	**0.10**	0.55	**1**	µA

NOTES:

6. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
7. The "$t_{Data\_loading}$" parameter is determined by IC design, and simulation.
8. For more detailed information regarding I^2C timing characteristics, refer to Table 1 on page 13.

Typical Performance Curves T_A = +25°C, unless otherwise specified.

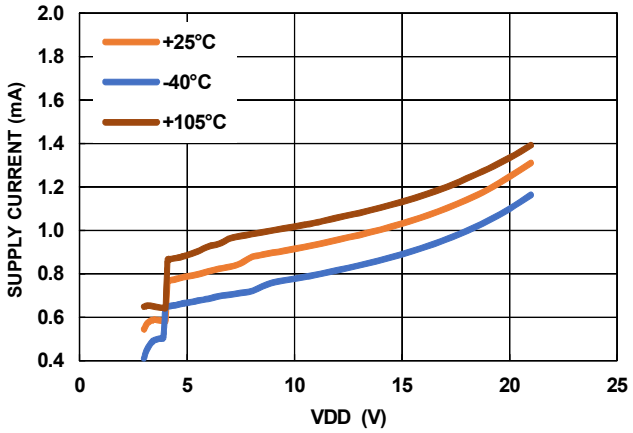


FIGURE 3. A_{VDD} SUPPLY CURRENT vs VOLTAGE

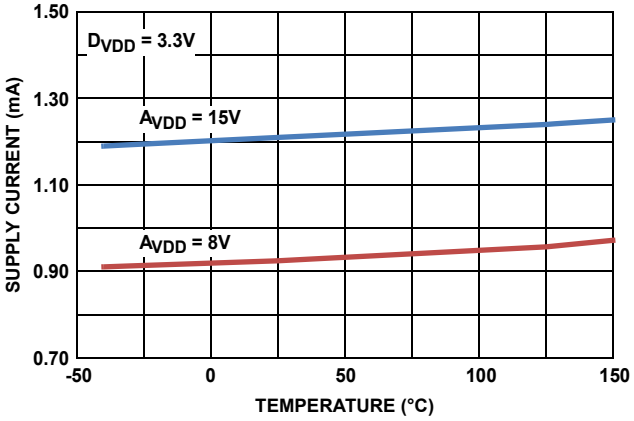


FIGURE 4. A_{VDD} SUPPLY CURRENT vs TEMPERATURE

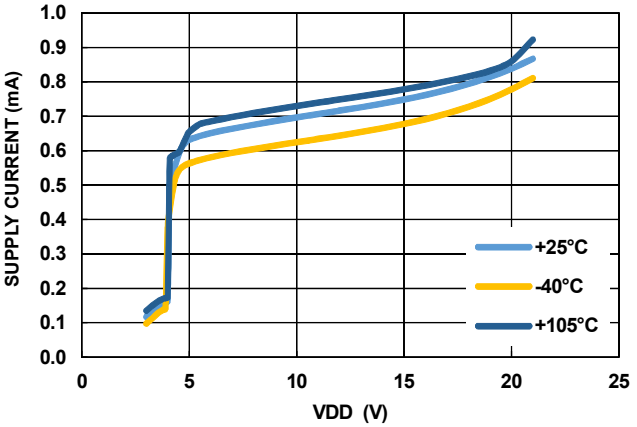


FIGURE 5. A_{VDD}_AMP SUPPLY CURRENT vs VOLTAGE

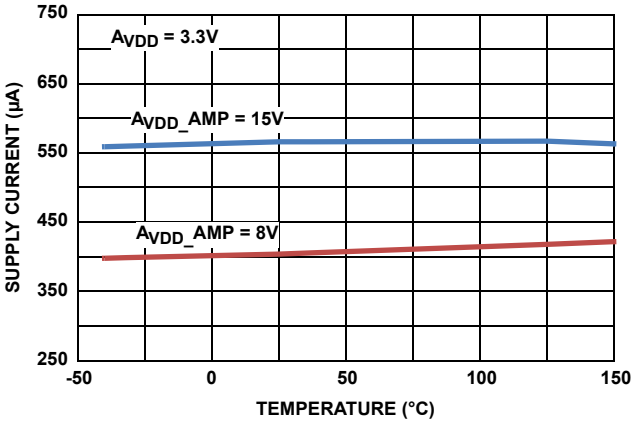


FIGURE 6. A_{VDD}_AMP SUPPLY CURRENT vs TEMPERATURE

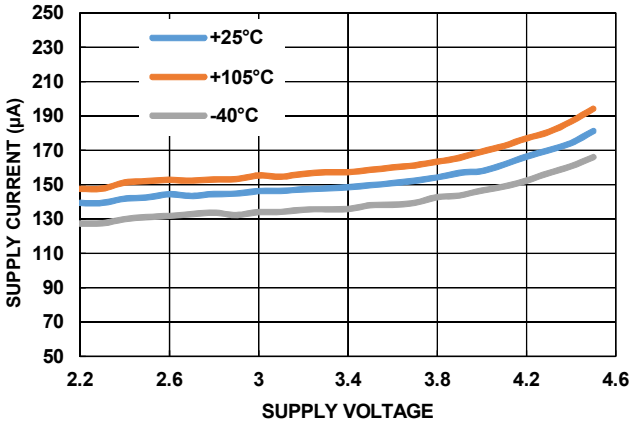


FIGURE 7. D_{VDD} SUPPLY CURRENT vs VOLTAGE

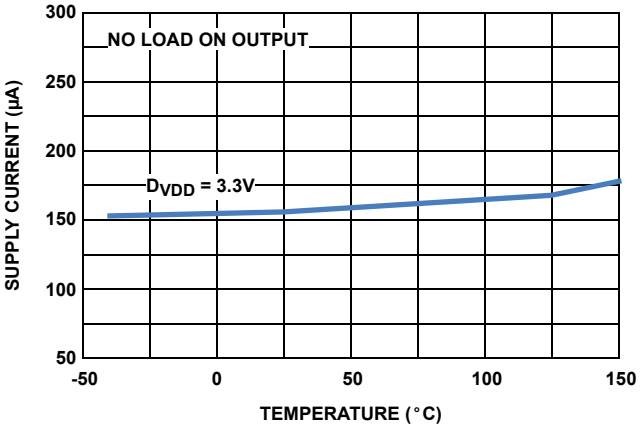


FIGURE 8. D_{VDD} SUPPLY CURRENT vs TEMPERATURE

Typical Performance Curves T_A = +25°C, unless otherwise specified. (Continued)

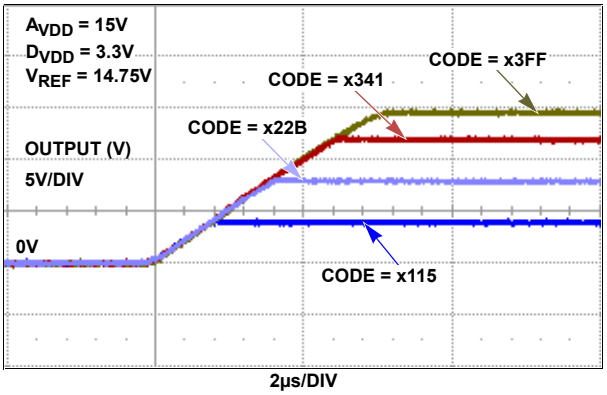


FIGURE 9. OUT1-OUT14 POSITIVE SLEW RATE (DAC CODE CHANGE)

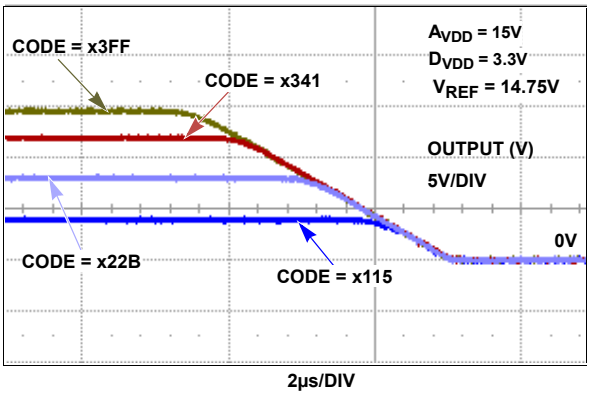


FIGURE 10. OUT1-OUT14 NEGATIVE SLEW RATE (DAC CODE CHANGE)

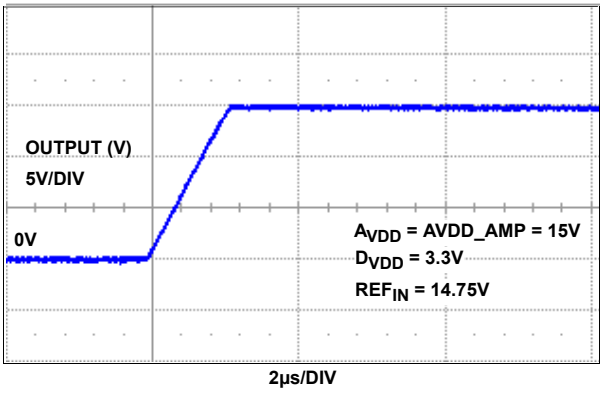


FIGURE 11. V_{COM} AMPLIFIER POSITIVE SLEW RATE

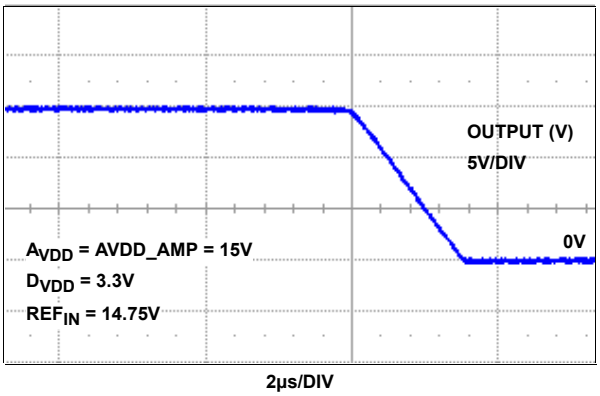


FIGURE 12. V_{COM} AMPLIFIER NEGATIVE SLEW RATE

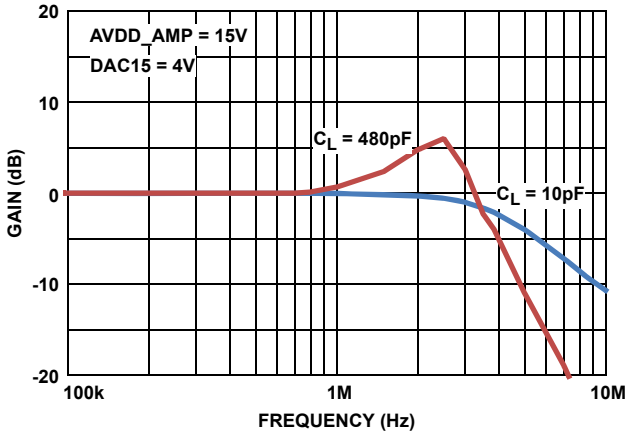


FIGURE 13. V_{COM} AMPLIFIER BANDWIDTH vs CAPACITIVE LOADING

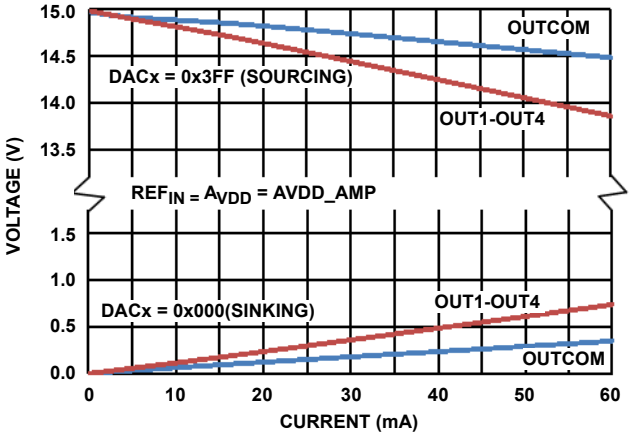


FIGURE 14. OUT1-OUT14 AND OUTCOM OUTPUT VOLTAGE vs OUTPUT CURRENT (V_{OH} AND V_{OL})

Typical Performance Curves T_A = +25°C, unless otherwise specified. (Continued)

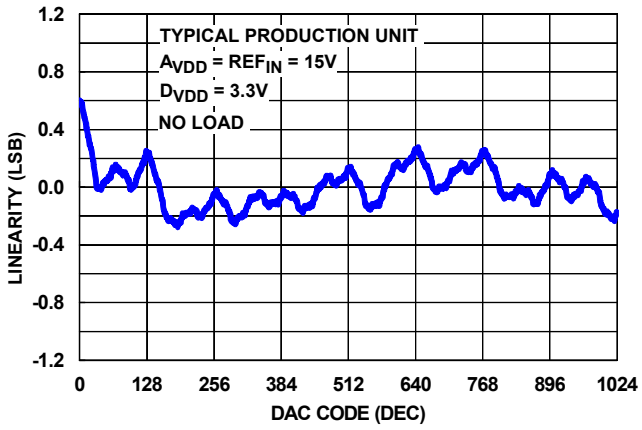


FIGURE 15. DAC1-DAC15 INL (REF_{IN} = A_{VDD} = 15V) AT +25°C

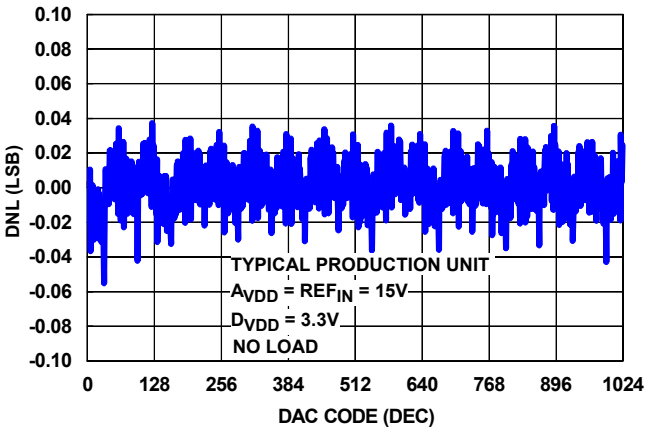


FIGURE 16. DAC1-DAC15 DNL (REF_{IN} = A_{VDD} = 15V) AT +25°C

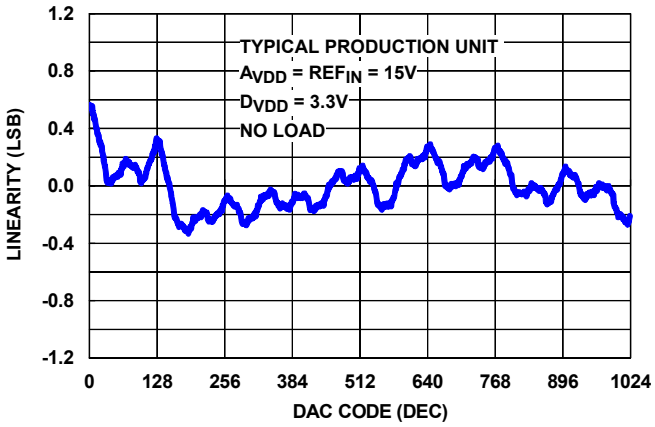


FIGURE 17. DAC1-DAC15 TYPICAL INL (REF_{IN} = A_{VDD} = 15V) AT -40°C

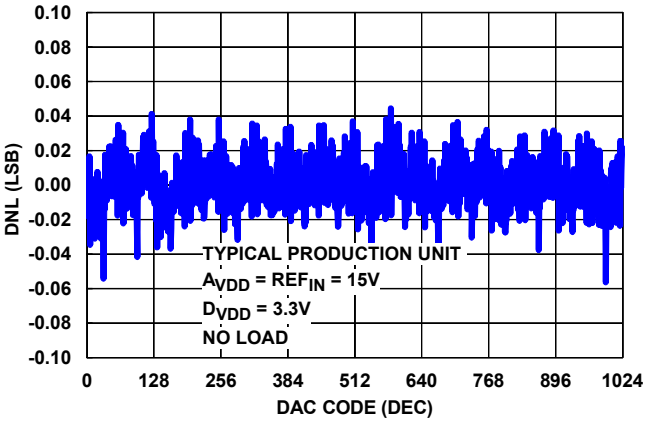


FIGURE 18. DAC1-DAC15 TYPICAL DNL (REF_{IN} = A_{VDD} = 15V) AT -40°C

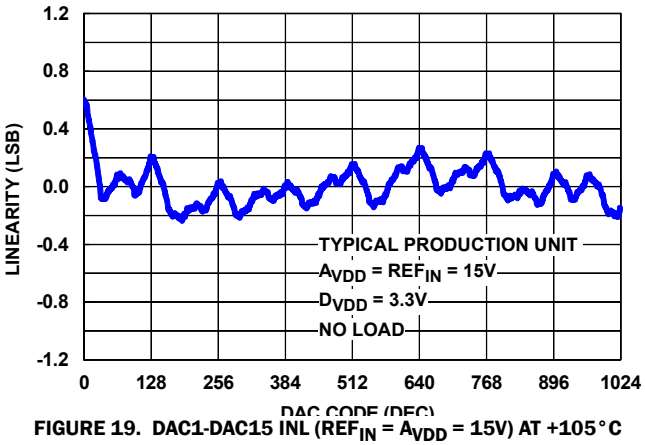


FIGURE 19. DAC1-DAC15 INL (REF_{IN} = A_{VDD} = 15V) AT +105°C

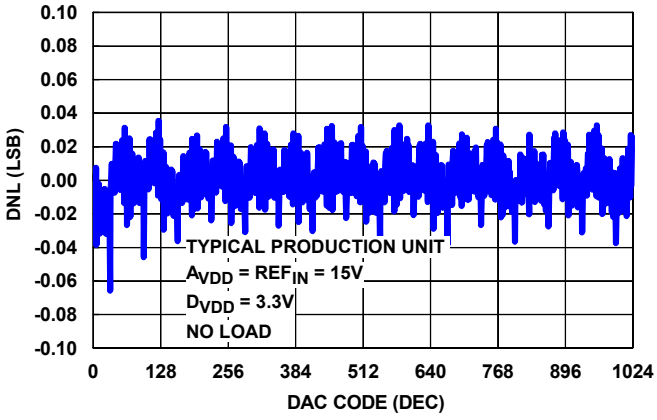


FIGURE 20. DAC1-DAC15 DNL (REF_{IN} = A_{VDD} = 15V) AT +105°C

Typical Performance Curves T_A = +25°C, unless otherwise specified. (Continued)

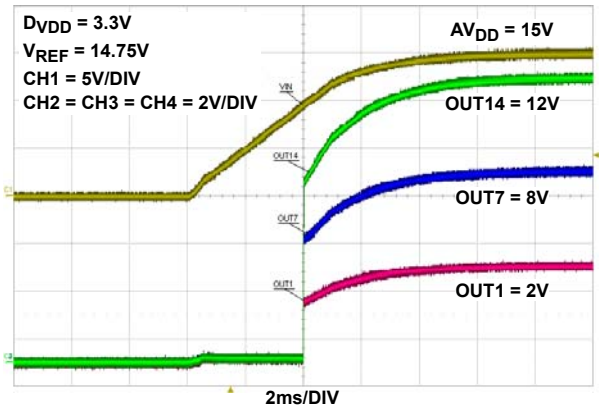


FIGURE 21. OUT1-OUT7-OUT14 AT POWER-ON

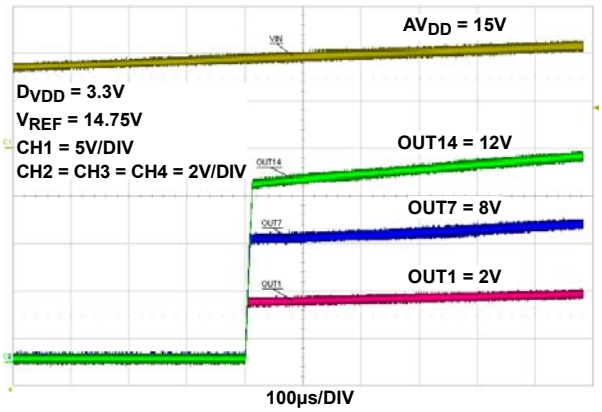


FIGURE 22. OUT1-OUT7-OUT14 AT POWER-ON (ZOOMED IN)

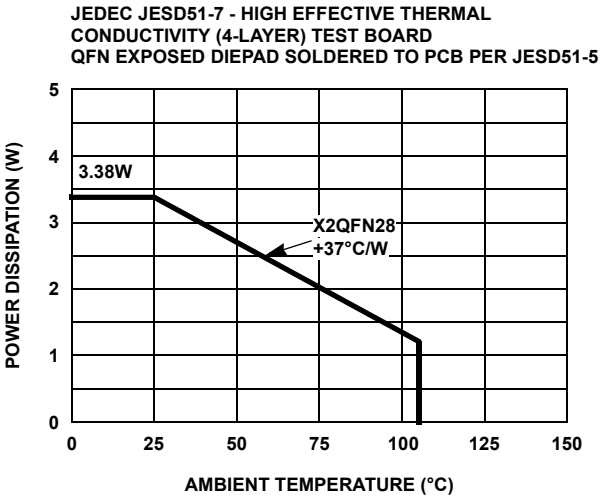


FIGURE 23. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE (4-LAYER BOARD)

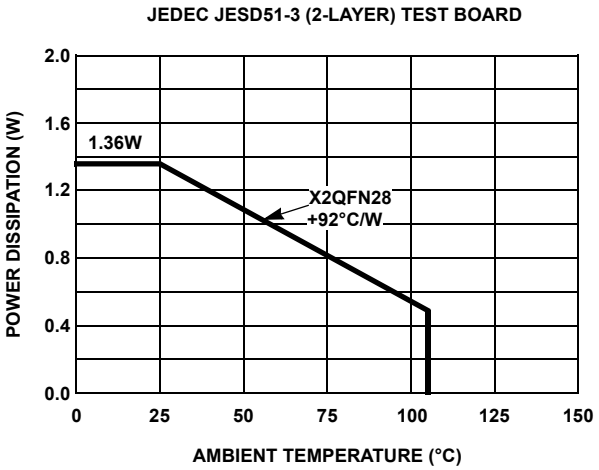


FIGURE 24. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE (2-LAYER BOARD)

General Description

The Voltage/Transmission (V/T) transfer curve or gamma curve of LCD panels require adjustment to achieve the desired optimal visual response (often called gamma correction).

The ISL76534 has a total of 15 channels (14xgamma channels + 1x$V_{COM\ channel}$) independent, programmable reference voltage outputs whose output voltage can be set with 10-bit resolution. The ISL76534 has integrated EEPROM to store all gamma and V_{COM} data.

In addition to the 14-channel gamma DACs, the ISL76534 provides a V_{COM} calibrator DAC with 10-bit resolution and a high output current operational amplifier to drive the V_{COM} voltage also required by the LCD panel.

I^2C Digital Interface

The ISL76534 uses a standard I^2C interface bus for communication. The two-wire interface links a master(s) and uniquely addressable slave devices. The master generates clock signals and is responsible for initiating data transfers. The serial clock is on the SCL line and the serial data (bidirectional) is on the SDA line. The ISL76534 supports clock rates up to 400kHz (fast-mode), and is backwards compatible with standard 100kHz clock rates (standard-mode).

The SDA and SCL lines must be HIGH when the bus if free - not in use. An external pull-up resistor (typically 2.2kΩ to 4.7kΩ) or current source is required for SDA and SCL.

The ISL76534 meets standard I^2C timing specifications; see Figure 25 and Table 1, which show the standard timing definitions and specifications for I^2C communication.

Data Validity

The data on the SDA line must be stable (clearly defined as HIGH or LOW) during the HIGH period of the clock signal. The state of the SDA line can only change when the SCL line is low (except to create a START or STOP condition). See timing specifications on Table 1 on page 13.

The voltage levels used to indicate a logical '0' (LOW) and logical '1' (HIGH) are determined by the V_{IL} and V_{IH} thresholds, respectively; see the "Electrical Specifications" table on page 6.

START and STOP Condition

All I^2C communication begins with a START condition, indicating the beginning of a transaction, and ends with a STOP condition, signaling the end of the transaction.

A START condition is signified by a HIGH to LOW transition on the Serial Data line (SDA) while the Serial Clock Line (SCL) is HIGH. A STOP condition is signified by a LOW to HIGH transition on the SDA line while SCL is HIGH. See timing specifications in Table 1.

The master always initiates START and STOP conditions. After a START condition, the bus is considered "busy." After a STOP condition, the bus is considered "free." The ISL76534 also supports repeated STARTs, where the bus will remain busy for continued transaction(s).

Byte Format

Every byte on the SDA must be 8 bits in length. After every byte of data sent by the transmitter, there must be an acknowledge bit (from the receiver) to signify that the previous 8 bits were transferred successfully. Data is always transferred on the SDA with the Most Significant Bit (MSB) first. If the data is larger than 8 bits then it can be separated into multiple 8-bit bytes. See "Data Word (WRITE/READ)" on page 19.

Acknowledge (ACK)

Each 8-bit data transfer is followed by an Acknowledge (ACK) bit from the receiver. The Acknowledge bit signifies that the previous 8 bits of data was transferred successfully (master-slave or slave-master).

When the master sends data to the slave (e.g. during a WRITE transaction), after the 8th bit of a data byte is transmitted, the master tri-states the SDA line during the 9th clock. The slave device acknowledges that it received all 8 bits by pulling down the SDA line, generating an ACK bit.

When the master receives data from the slave (e.g. during a data READ transaction), after the 8th bit is transmitted, the slave tri-states the SDA line during the 9th clock. The master acknowledges that it received all 8 bits by pulling down the SDA line, generating an ACK bit.

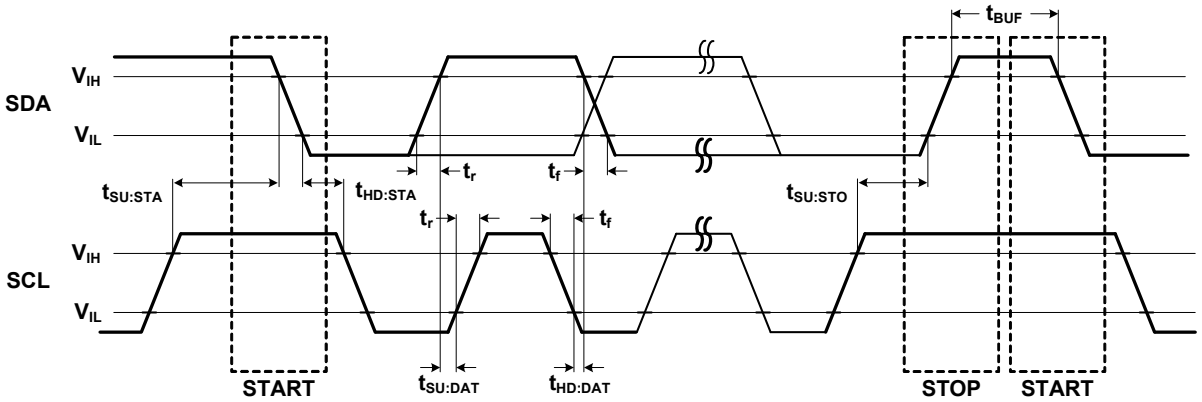


FIGURE 25. I^2C TIMING DEFINITIONS

TABLE 1. I^2C TIMING CHARACTERISTICS

PARAMETER	SYMBOL	FAST-MODE		STANDARD-MODE		UNIT
		MIN	MAX	MIN	MAX	
SCL Clock Frequency	f_{SCL}	0	400	0	100	kHz
Set-Up Time for a START Condition	$t_{SU:STA}$	0.6		4.7		µs
Hold Time for a START Condition	$t_{HD:STA}$	0.6		4.0		µs
Set-Up Time for a STOP Condition	$t_{SU:STO}$	0.6		4.0		µs
Bus Free Time between a STOP and START Condition	t_{BUF}	1.3		4.7		µs
Data Set-Up Time	$t_{SU:DAT}$	100		250		ns
Data Hold Time	$t_{HD:DAT}$	0		0		µs
Rise Time of SDA and SCL (Note 9)	t_r	$20 + 0.1C_b$	300		1000	ns
Fall Time of SDA and SCL (Note 9)	t_f	$20 + 0.1C_b$	300		300	ns

NOTE:

9. C_b = total capacitance of one bus line in pF

Not Acknowledge (NACK)

A Not Acknowledge (NACK) is generated when the receiver does not pull down the SDA line during the acknowledge clock (i.e., SDA line remains HIGH during the 9th clock). This indicates to the master that it can generate a STOP condition to end the transaction and free the bus.

A NACK can be generated for various reasons, for example:

- After an I^2C device address is transmitted, there is NO receiver with that address on the bus to respond.
- The receiver is busy performing an internal operation (e.g. reset, recall, etc.), and cannot respond.
- The master (acting as a receiver) needs to indicate the end of a transfer with the slave (acting as a transmitter).

Device Address and R/$\overline{W}$ Bit

Data transfers follow the format shown in Figures 26 through 27. After a valid START condition, the first byte sent in a transaction contains the 7-bit device (slave) Address plus a direction (R/$\overline{W}$) bit. The Device Address identifies which device (of up to 127 devices on the I^2C bus) the master wishes to communicate with.

After a START condition, the ISL76534 monitors the first 8 bits (Device Address byte) and checks for it is 7-bit Device Address in the MSBs. If it recognizes the correct Device Address it will ACK, and becomes ready for further communication. If it does not see it is Device Address, it will sit idle until another START condition is issued on the bus.

To access the ISL76534 DACs, the Device Addresses allowed are 0x74 hex (1110100x), or 0x75 hex (1110101x). The first 6 bits (b_7 to b_2, MSBs) of the 7-bit device address have been factory programmed and are always 111010. Only the least significant bit of the Device Address (bit b_1, LSB) is allowed to change. The value of the LSB (bit b_1) is set by the hardware “A0” pin. When A0 = HIGH, the device will only respond to a Device Address of 0x75. When A0 = LOW, the device will only respond to a Device Address of 0x74. This allows for two ISL76534 devices to be used on the same I^2C bus, each with a different Device Address.

Note: The eighth bit of the Device Address byte (bit b_0) indicates the direction of transfer, READ or WRITE (R/$\overline{W}$). A “0” indicates a WRITE operation- the master will transmit data to the ISL76534 (receiver). A “1” indicates a Read operation- the master will receive data from the ISL76534 (transmitter).

Application Information

ISL76534 Communication Protocol

The ISL76534 allows the user to sequentially read or write all the registers with a single multi-byte I^2C READ or WRITE operation (“Burst Mode”).

The ISL76534 also allows the user to READ or WRITE to a specific register only (or a specific range of registers), using Register Pointer addressing (“Register Mode”). With Register Mode, a specific V_{COM} value, Gamma DAC value or range of values may be read or written without having to read or write the other registers.

Register Description and Pointer

Table 2 contains a detailed register description. All registers contain 10 bits, which span over two data bytes (16 bits) and the data is latched-in after the 16th bit (LSB) is received. The only exception is the Control Register, where the data is latched in after the first 8 bits are received.

Reading/writing always begins at location specified by the Register Pointer. The Register Pointer automatically increments by 0x01 with every two bytes transferred. For example, when using Register Pointer 0x01 to address DAC1 (MSB and LSB), the device automatically increments the pointer to 0x02, 0x03... after every two data bytes are received. This enables Burst Mode operation where only the first Register Pointer for a given sequence of registers is needed.

To address separate or non-sequential register locations, a full I^2C START, Device Address, Register Pointer, Data..., STOP sequence must be used to address each register location; see “WRITE TRANSACTION” on page 15.

The Control Register is located at Register Pointer 0x00, while the 10-bit DAC data is at Register Pointers 0x01 though 0x0F.

TABLE 2. REGISTER DESCRIPTION

REGISTER POINTER	REGISTER	BIT(S)	FUNCTION NAME	DESCRIPTION
0x00	Control Byte (data latched in after each byte, b[15:8] and b[7:0], is received by I^2C)	15:14	Reserved	Set to 0
		13:12	Reserved	Set to 0
		11	Output Enable (active low)	0: Outputs Enabled, default at power-ON 1: Outputs Disabled
		10:9	Recall EEPROM	00: Normal Operation 11: When Register Pointer 0x00 = 0x06; “Software Reset.” Recalls stored EEPROM data to DAC registers. Device will NACK during the 9th SCL pulse when a Reset command is issued.
		8:0	Reserved	Set to 0
0x01 ~ 0x0F	Gamma Data	15	Reserved	Set to 0
		14	Write EEPROM	0: Write data to DAC only 1: Write data to DAC and EEPROM
		13:10	Reserved	Set to 0
		9:0	DAC data	10-bit data for DACs 1 through 15
0x10 ~ 0xFF	Reserved	15:0	Reserved	Do not write data to these registers

NOTES:

10. Any Register Pointers not indicated in Table 2 are Reserved Registers, and should not be used.
11. A write to an EEPROM register can take up to 35ms to complete. To avoid errors and ensure correct EEPROM data, any writes to EEPROM registers should be spaced at least 35ms apart. For more information, refer to “Writing to the EEPROM” on page 20.

Write Operation

Table 3 describes a write operation and Figures 26 and 27 shows the write timing diagram.

TABLE 3. WRITE TRANSACTION

I^2C DATA FROM MASTER	I^2C DATA FROM ISL76534	NOTES
START		I^2C START Signal
0xE8 or 0xEA	ACK	Send Device Address + R/$\overline{W}$ bit (depends on the state of A0 pin) 1110100 + 0, if A0 = LOW 1110101 + 0, if A0 = HIGH
Register Pointer	ACK	Register Pointer indicating starting register location to write to. Register Pointer = 0x00 for Control Byte Register Pointer = 0x01 for DAC 1 MSB/LSB data Register Pointer = 0x02 for DAC 2 MSB/LSB data ... Register Pointer = 0x0E for DAC 14 MSB/LSB data Register Pointer = 0x0F for DAC 15 MSB/LSB data For more information on the Register Pointer see Table 2 on page 14.
Byte 1	ACK	If Register Pointer = 0x00, Byte 1 is the Control Byte. When Register Pointer = 0x00 and Byte 1 = 0x06, data is recalled from EEPROM and written into the DAC registers (RAM). If Register Pointer = 0x01 or more, Byte 1 is the MSB byte of the DAC word
Byte 2	ACK	If Register Pointer = 0x00, Byte 2 is a null byte and will be ignored If Register Pointer = 0x01 or more, Byte 2 is the LSB of the DAC word
Byte 3	ACK	MSB of DAC (1 + Register Pointer). Ex) Register Pointer = 0x00, MSB of DAC1
Byte 4	ACK	LSB of DAC (1 + Register Pointer). Ex) Register Pointer = 0x00, LSB of DAC1
Byte 5	ACK	MSB of DAC (2 + Register Pointer)
Byte 6	ACK	LSB of DAC (2 + Register Pointer)
...	...	The WRITE operation can be stopped at any time after a register has been written. The DAC channel output is updated after ALL 10-bit channel data is received.
STOP		I^2C STOP Signal

Write Timing Diagrams

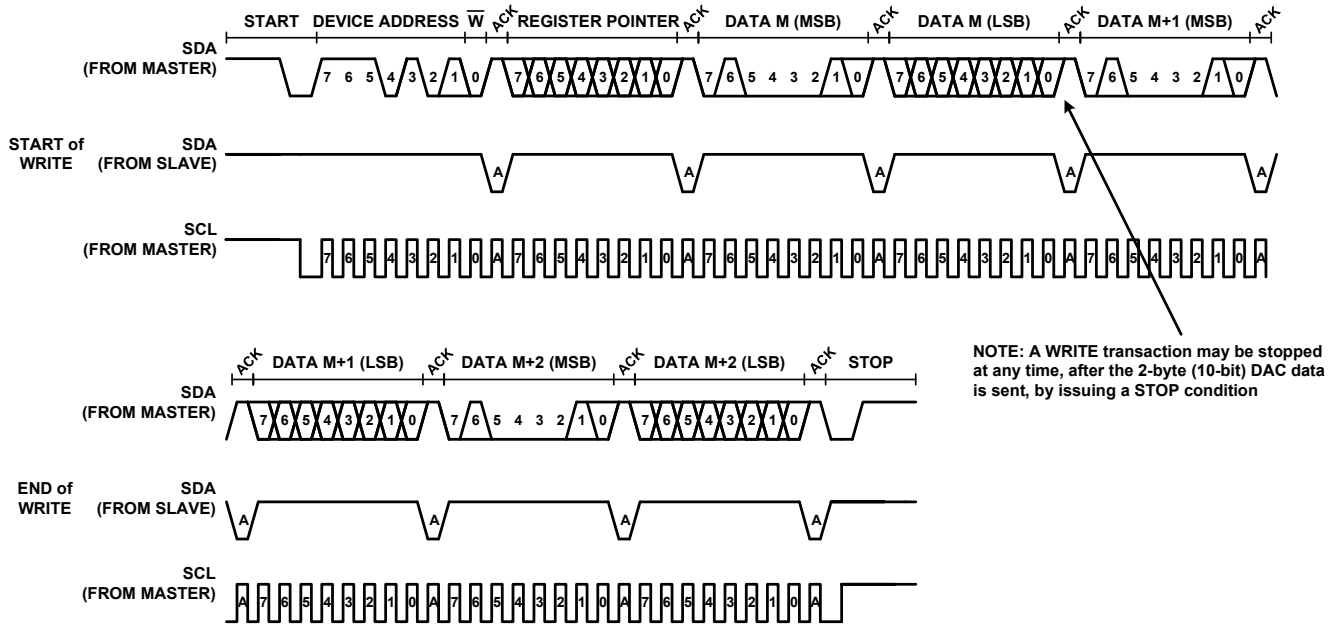


FIGURE 26. WRITE DATA BYTES

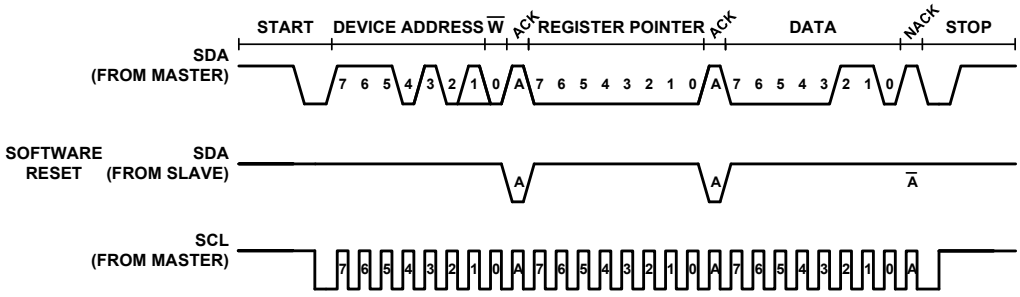


FIGURE 27. RECALL DATA FROM EEPROM (SOFTWARE RESET)

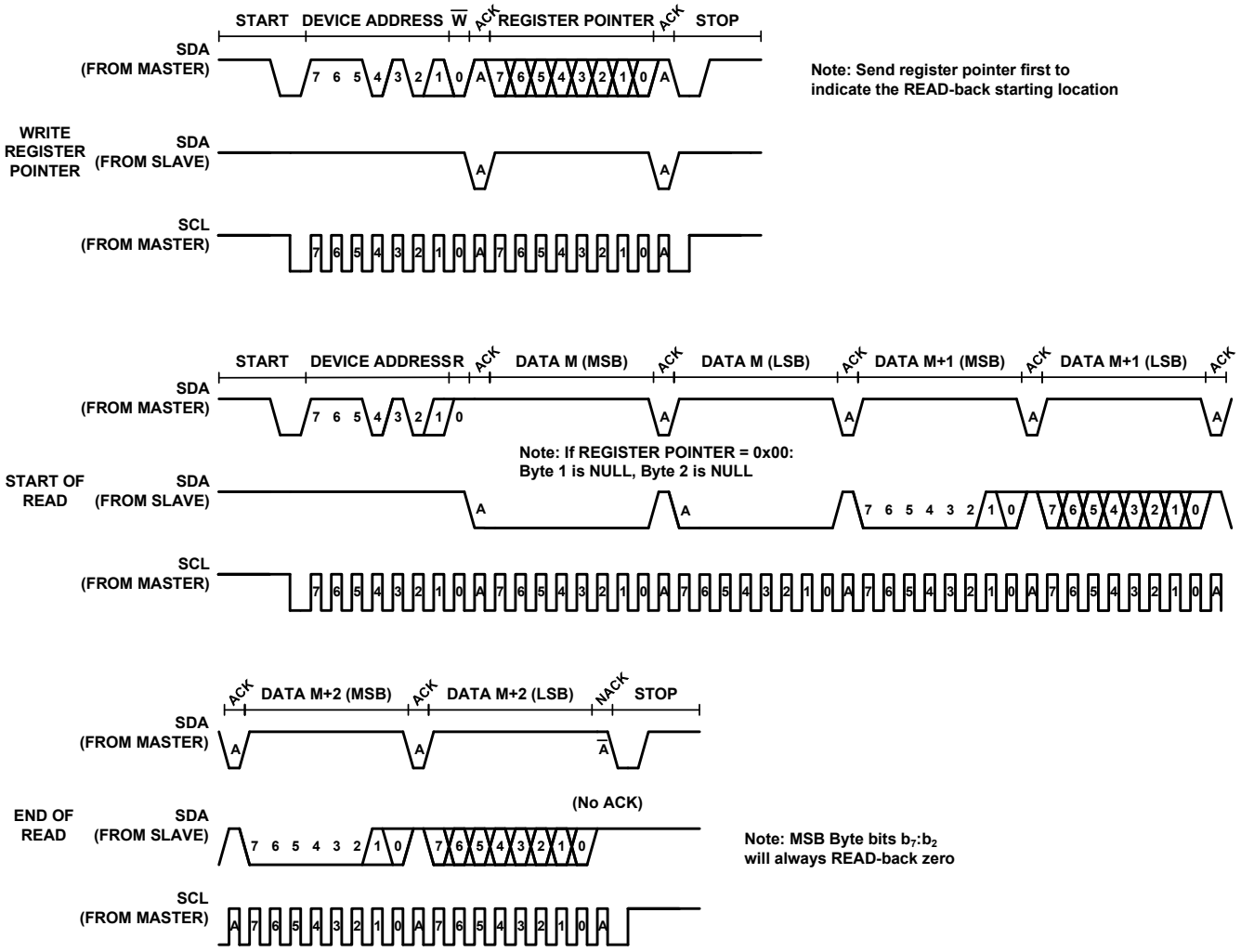
Read Operation

Table 4 describes a Read operation and Figure 28 shows the read timing diagram.

TABLE 4. READ TRANSACTION

I^2C DATA FROM MASTER	I^2C DATA FROM ISL76534	NOTES
START		I^2C START Signal
0xE8 or 0xEA	ACK	Send Device Address + R/$\overline{W}$ Bit (depends on the state of A0 pin) 1110100 + 0, if A0 = LOW 1110101 + 0, if A0 = HIGH
Register Pointer	ACK	Register Pointer indicating starting register location to write to. Register Pointer = 0x00 for Control Byte Register Pointer = 0x01 for DAC 1 MSB/LSB data Register Pointer = 0x02 for DAC 2 MSB/LSB data ... Register Pointer = 0x0E for DAC 14 MSB/LSB data Register Pointer = 0x0F for DAC 15 MSB/LSB data For more information on the Register Pointer see Table 2 on page 14.
STOP		I^2C STOP signal
START		I^2C START signal
0xE9	ACK	Send Device Address + R/$\overline{W}$ Bit 1110100 + 1
0xE9 or 0xEB	ACK	Send Device Address + R/$\overline{W}$ Bit (depends on the state of A0 pin) 1110100 + 1, if A0 = LOW 1110101 + 1, if A0 = HIGH
ACK	Byte 1	If Register Pointer = 0x00, Byte 1 is a Null Byte If Register Pointer = 0x01 or more, Byte 1 is the MSB byte of the DAC word ...
ACK	Byte 2	If Register Pointer = 0x00, Byte 2 is a Null Byte If Register Pointer = 0x01 or more, Byte 2 is the LSB byte of the DAC word ...
ACK	Byte 3	MSB of DAC (1 + Register Pointer). Ex) Register Pointer = 0x00, MSB of DAC1
ACK	Byte 4	LSB of DAC (1 + Register Pointer). Ex) Register Pointer = 0x00, LSB of DAC1
ACK	Byte 5	MSB of DAC (2 + Register Pointer)
ACK	Byte 6	LSB of DAC (2 + Register Pointer)
...	...	The READ operation can be stopped at any time after a register has been read
NAK	DAC 15 LSB	8 LSBs of DAC 15's 10-bit value: dddd dddd
STOP		I^2C STOP Signal

Read Timing Diagram



NOTE: The READ operation can be stopped at any time after the DAC register data has been read by sending a STOP condition.

FIGURE 28. READ TIMING DIAGRAM

TABLE 5. DAC CALCULATION

b_{15}	b_{14}	b_{13}	b_{12}	b_{11}	b_{10}	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
						1	0	1	1	1	0	1	0	1	0

$$2^9 \times (1) + 2^8 \times (0) + 2^7 \times (1) + 2^6 \times (1) + 2^5 \times (1) + 2^4 \times (0) + 2^3 \times (1) + 2^2 \times (0) + 2^1 \times (1) + 2^0 \times (0)$$

Data Word (WRITE/READ)

Data Words contain the data written or read from the 10-bit DACs. Each 10-bit DAC data is transmitted in one word (e.g. two bytes, 16-bits), as shown in Table 5. Bits [b_9:b_0] represent the 10-bit data. Bits [b_{15}:b_{10}] are "do not cares" and will default to zero when reading data, however, when writing data bit b_{14} indicates the type of write. If b_{14} = '0': WRITE data to the DAC register; if b_{14} = '1': WRITE data to the DAC and EEPROM (program).

For any DAC, the first data byte of the word is called the Upper Byte (or MSB), and the two LSBs of this byte represent the MSBs of the 10-bit data, [b_9:b_8]. The second data byte of the word, or Lower Byte (LSB), contains the remaining 8-bits (LSBs) of the 10-bit DAC data, [b_7:b_0]. These data words provide the DAC values that ultimately determine the output voltages of the ISL76534.

Refer to Table 2 for more information about the byte structure, and refer to the following sections for information about the expected DAC output voltage.

DAC Transfer Function of OUT1-OUT14

Equation 1 shows the transfer function for each 10-bit DAC channel (expected output voltage). The transfer function relates the REF_{IN} voltage and a DAC_CODE to a DAC output voltage, "V_{OUT}." The DAC_CODE is the decimal value of the 10-bit data written to a given DAC channel.

$$V_{OUT} = REF_{IN} \times \frac{DAC\_CODE}{1024} \quad \text{(EQ. 1)}$$

DAC_CODE: 0 ~ 1023

Example calculation to find the expected V_{OUT}:

A_{VDD} = 15V REF_{IN} = 14.75V

$$1LSB = \frac{14.75V}{1024} = 14.40mV$$

$$V_{OUT} = 14.40mV \times DAC\_CODE$$

$$V_{OUT}(DAC\_CODE = 512) = 14.40mV \times 512 = 7.375V$$

DAC Output Accuracy

The relationship between the actual/measured DAC output voltage and the expected voltage is the "Output Accuracy" (OUT_{AC}). Equation 2 shows how to determine output accuracy:

$$OUT_{AC} = V_{OUT(expected)} - V_{OUT(measured)} \quad \text{(EQ. 2)}$$

The ISL76534 features are very good and have consistent output accuracy across all DAC codes and REF_{IN} voltages, ±15mV (typical). Some competitor devices have diverging accuracy performance near the high rail and have significantly larger output accuracy variances compared to ISL76534.

The output accuracy performance of the ISL76534 provides highly accurate reference voltages ideal for TFT-LCD applications. This is important in TFT-LCD applications that require the DACs/EEPROM to be programmed with the same digital codes (e.g. gamma references determined from gamma calibration) on a production line, and especially when using reflected code gamma calibration methods. Ensuring accurate gamma references is also important for optimizing pixel/panel reliability.

DAC Reference Voltage

The REF_{IN} pin is the reference voltage input for the 10-bit DACs. It is a high impedance input. The voltage can be set using an external resistor divider, regulated voltage, or tied directly to the A_{VDD} power rail. The REF_{IN} pin should always be well bypassed to minimize noise, and provide the best DAC performance. Use a 0.1µF ceramic capacitor (to GND), placed as close to the pin as possible.

See example of the typical application circuits in Figures 30 and 31.

DAC Channel Outputs

The DAC output buffers are optimized to drive rail-to-rail for optimal flexibility. Generally, in a TFT-LCD half of the required gamma reference voltages will lie between V_{COM} and A_{VDD} (or REF_{IN}), and the other half will lie between V_{COM} and GND. For maximum flexibility, all ISL76534 outputs (OUT1-OUT14) can drive to within 100mV of REF_{IN} (A_{VDD} = REF_{IN}) and to within 85mV of GND (with ±5mA load). See "Electrical Specifications" table on page 6 for more details about output channel capabilities.

Each DAC is updated as soon as the entire 10-bit value for that DAC is received via I^2C. DAC data is latched, and the respective DAC responds, on the falling edge of the 8th SCL clock (which corresponds to the DAC LSB data bit, bit b_0).

V_{COM} Amplifier

The ISL76534 V_{COM} amplifier is capable of rail-to-rail output swings and the ability to drive highly capacitive loads. It can source/sink up to 100mA of continuous current and over 500mA of peak current. The output capability of the V_{COM} amplifier is described in detail in "Electrical Specifications" table on page 6.

The V_{COM} amplifier is powered from a separate power supply than the rest of the IC, called A_{VDD}_AMP. This allows A_{VDD}_AMP to be set at a voltage lower than AVDD, to save system power. Though it is acceptable to set A_{VDD}_AMP = A_{VDD}.

A_{VDD}_AMP is not required for the rest of the IC to operate, so if an application is not utilizing the V_{COM} Amplifier in the ISL76534 (OUTCOM), then A_{VDD}_AMP can be tied to GND to disable the function and save IC and system power. If A_{VDD}_AMP is powered but not connected in the application, then the V_{COM} amplifier should be set in a buffer (A_V = +1) configuration (INN_COM tied to OUTCOM). See example typical application circuits in Figures 30 and 31.

The device offers access to the inverting pin of the amplifier, INN_COM, which enables various types of circuit configurations depending on the requirements of the TFT-LCD panel architecture. Most common applications either buffer the amplifier for direct driving and response (INN_COM tied to OUTCOM), or they may utilize feedback from the TFT-LCD panel as an input to the INN_COM pin.

Output Stability

The ISL76534 outputs are designed to drive capacitive loads, such as in TFT-LCD panel. However, purely capacitive loads should not exceed 1nF without appropriate external load isolation and/or amplifier compensation.

As load capacitance increases, the -3dB bandwidth will decrease and peaking can occur. Depending on the application, it may be necessary to reduce peaking and improve device stability. To do this, a snubber circuit (compensation) or a series resistor (isolation) may be added to the output of the ISL76534.

A snubber is a shunt load consisting of a resistor in series with a capacitor. An optimized snubber can improve the phase margin and the stability of the ISL76534 by adding a zero in the loop response. The advantage of a snubber circuit is that it does not draw any DC load current or reduce the gain.

Another method to reduce peaking is to add a series output resistor (typically between 1Ω to 10Ω). Depending on the capacitive loading, a small value resistor may be the most appropriate choice to minimize any reduction in gain.

Write Protection ($\overline{WP}$)

The ISL76534 has an I^2C write protection ($\overline{WP}$) pin. $\overline{WP}$ is a logic level input pin and is active low.

- $\overline{WP}$ = 0 (LOW): Protected, device ignores I^2C data writes to the internal DAC registers and EEPROM
- $\overline{WP}$ = 1 (HIGH): Not Protected, device allows I^2C data writes to the internal DAC registers and EEPROM

Whether $\overline{WP}$ is set HIGH or LOW, the device will ACK to proper I^2C commands, however, when $\overline{WP}$ = LOW the device internally ignores the data bytes.

The logic state of $\overline{WP}$ can be changed during device operation. However, $\overline{WP}$ should not be changed during the EEPROM write procedure time.

Writing to the EEPROM

During an I^2C transaction, setting bit b_{14} of a Data Word HIGH indicates to the device that the data in that same Data Word should be written to both the DAC and EEPROM. The EEPROM programming cycle for the appropriate channel(s) is started as soon as a subsequent STOP command is issued on the I^2C bus.

After the STOP condition is issued, it takes up to 35ms (maximum) for a single EEPROM Register Write, and 420ms (maximum) to write all registers to EEPROM. To ensure EEPROM data validity, wait at least 35ms between single EEPROM Register Writes, and before sending any other I^2C commands. When writing all registers to EEPROM, wait at least 420ms before sending any other I^2C commands. During the EEPROM programming cycle time, the device's I^2C bus is internally busy and will NACK I^2C commands.

Note, the normal DAC writes (bit b_{14} = '0') can be written to as quickly as the I^2C bus can support.

OUT1-OUT14 AND OUTCOM BEHAVIOR

During the EEPROM writing/programming cycle the ISL76534 gamma outputs (OUT1-OUT14) and V_{COM} amplifier output (OUTCOM) remain enabled.

Recalling The EEPROM

There are two ways to initiate a recall of the stored EEPROM data:

- Automatic recall - Power cycle (or power-ON) the device
- Manual recall - Perform a "software reset" using I^2C

The recall operation will overwrite all current DAC register values with the values stored in EEPROM.

AUTOMATIC RECALL

When the device is powered-ON, the ISL76534 automatically recalls the EEPROM data and loads it into the DAC registers (RAM) after D_{VDD} reaches ~2.2V. The time for the EEPROM recall to complete is the "$t_{Data\_loading}$" time and is 6ms (typical) by design. This operation restores all DAC registers to the values stored in EEPROM.

MANUAL RECALL

A recall can be initiated by performing a software reset using I^2C. A software reset is done by writing data 0x06 to Register Pointer 0x00 (Control Byte), and then on the falling edge of 8^{th} SCL clock (of the Control Byte), the recall operation will be started. The device will then issue a NACK on the 9^{th} SCL clock.

Recalling the ISL76534 EEPROM data to the output DACs takes 6ms typical) to complete. During the EEPROM recall time (power-ON or during a software reset), OUT1-OUT14 and OUTCOM will be set to high impedance and the device will NACK to any I^2C commands. Once the EEPROM recall is complete OUT1-OUT14 and OUTCOM will enable simultaneously and the outputs will slew to the correct level. If some or all of the outputs (OUT1-OUT14, OUTCOM) need to be defined (not high impedance) during this delay time, an external resistor divider may be used to set a "coarse" voltage until the DAC outputs are enabled.

Note, the ISL76534 EEPROM values are pre-programmed to the default values explained in the "DEFAULT EEPROM VALUES" section.

EEPROM Default Values

The ISL76534 has factory programmed (default) EEPROM values for the output channels, which will be recalled from EEPROM and loaded to the DAC registers at initial power-ON. The default EEPROM values are shown in Table 6.

TABLE 6. DEFAULT EEPROM VALUES

DAC #	CHANNEL	CODE (hex)	EXPECTED OUTPUT VOLTAGE (V)
DAC1-14	OUT1-14	0x000	GND
DAC15	OUTCOM	0x200	$REF_{IN}/2$

UVLO and Output Enable

The ISL76534 includes an Undervoltage Lock-Out (UVLO) for A_{VDD}. At power-ON the output drivers, OUTx and OUTCOM, are initially in a high impedance (disabled) state, A_{VDD} < UVLO.

The OUT1-OUT14 outputs are ENABLED when the internal EEPROM recall has been completed (see "Recalling The EEPROM" on page 20), and A_{VDD} rises above 4.5V (maximum). Although OUTCOM is powered from A_{VDD}_AMP, it is internally linked to the A_{VDD} UVLO function. The OUTCOM will be enabled when A_{VDD} and A_{VDD}_AMP rise above 4.5V (maximum).

The OUT1-OUT14 and OUTCOM outputs are DISABLED if A_{VDD} falls below 3.5V (minimum).

Power Sequencing

The ISL76534 has no restrictions on power supply sequencing of A_{VDD} and D_{VDD}. A_{VDD}_AMP should not exceed A_{VDD}. A_{VDD}_AMP can also be set to GND to disable the function.

The DAC reference, REF_{IN}, voltage should not exceed A_{VDD}. This ensures the ESD protection diodes from REF_{IN} to A_{VDD} do not become forward biased. If REF_{IN} does exceed A_{VDD}, then the current flow through the ESD diode should not exceed 10mA.

Thermal Shutdown

The ISL76534 features thermal shutdown, which protects the device from damage due to overheating. When the junction (die) temperature rises to 160°C (typical) all outputs, OUTx and OUTCOM, are disabled (high-impedance). When the die temperature cools by 20°C (typical) all outputs are re-enabled.

Power Dissipation

With high short-circuit and continuous output current capability for each channel, it is possible to exceed the +150°C absolute maximum junction (die) temperature. Therefore, it is important to calculate the maximum junction temperature for the application to determine if load or circuit conditions need to be modified to keep the device in a safe operating region.

The maximum power dissipation allowed in a package is determined according to Equation 3:

$$P_{DMAX} = \frac{T_{JMAX} - T_{AMAX}}{\Theta_{JA}} \quad \text{(EQ. 3)}$$

Where:

- T_{JMAX} = Maximum junction temperature
- T_{AMAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package
- P_{DMAX} = Maximum power dissipation in the package

For more details on the allowable package power dissipation, refer to Figures 23 and 24.

Power Supply Bypassing and Printed Circuit Board Layout

Good Printed Circuit Board (PCB) layout is necessary for optimum performance. The following are recommendations to achieve optimum high frequency performance from your PCB.

- To optimize thermal performance, solder the ISL76534's exposed thermal pad to GND. PCB vias should be placed below the device's exposed thermal pad and connected to GND to transfer heat away from the device (see "General PowerPAD Design Considerations"). If the thermal pad is not connected to GND then it should be electrically isolated.
- Maximize use of AC decoupled PCB layers. All signal I/O lines should be routed over continuous ground planes (i.e., no split planes or PCB gaps under these lines). Avoid vias in the signal I/O lines.
- When testing, use good quality connectors and cables, match cable types and keep cable lengths to a minimum.
- A minimum of two power supply decoupling capacitors are recommended (typically 4.7µF and 0.1µF) per supply and placed as close to the IC as possible. Avoid placing vias between the capacitor and the device because vias add unwanted inductance. Larger value capacitors can be placed farther away.

General PowerPAD Design Considerations

Figure 29 is an example of how to use vias to distribute heat away from an IC.

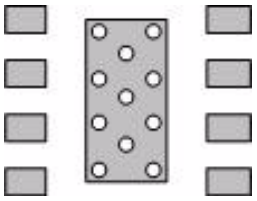


FIGURE 29. PCB VIA PATTERN

For optimal thermal performance, use vias to distribute heat away from the IC and to a system power plane. Fill the thermal pad area with vias that are spaced 3x their radius (typically), center-to-center, from each other. The via diameters should be kept small, but they should be large enough to allow solder wicking during reflow. To optimize heat transfer efficiency, do not connect vias using "thermal relief" patterns. Vias should be directly connected to the plane with plated through-holes.

Connect all vias to the correct voltage potential (power plane) indicated in the datasheet. For the ISL76534, the thermal pad potential is ground (GND).

Typical Applications

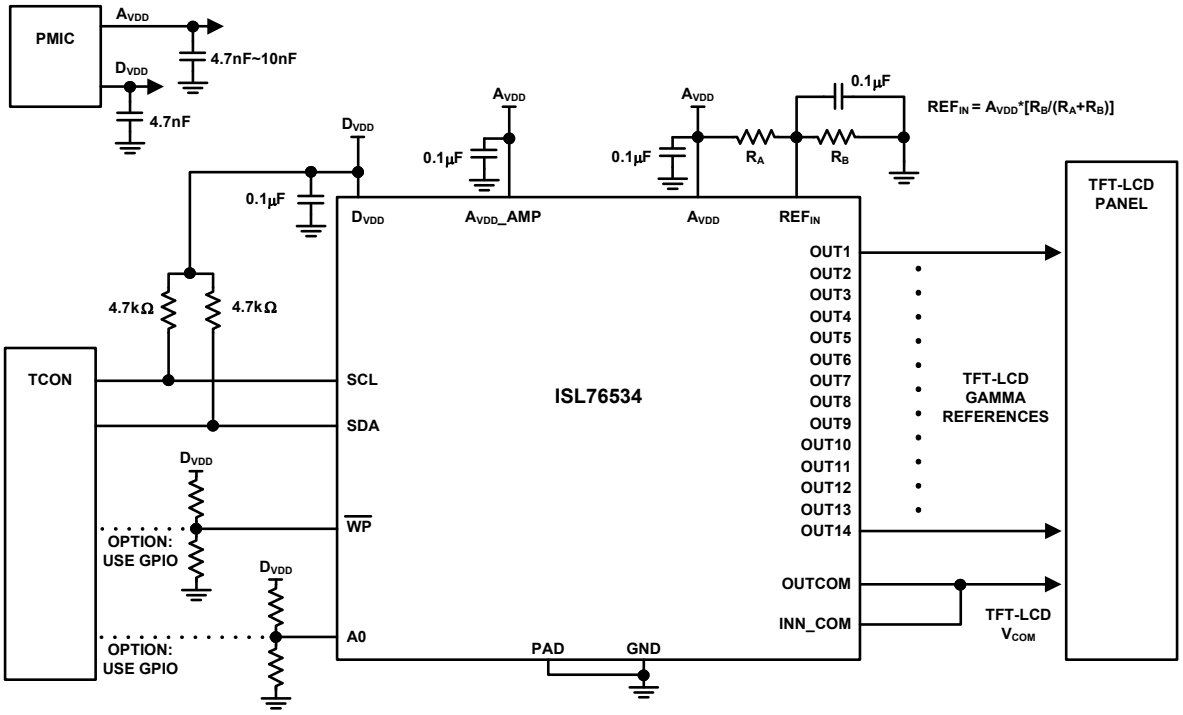


FIGURE 30. TFT-LCD GAMMA and V_{COM} REFERENCE GENERATOR

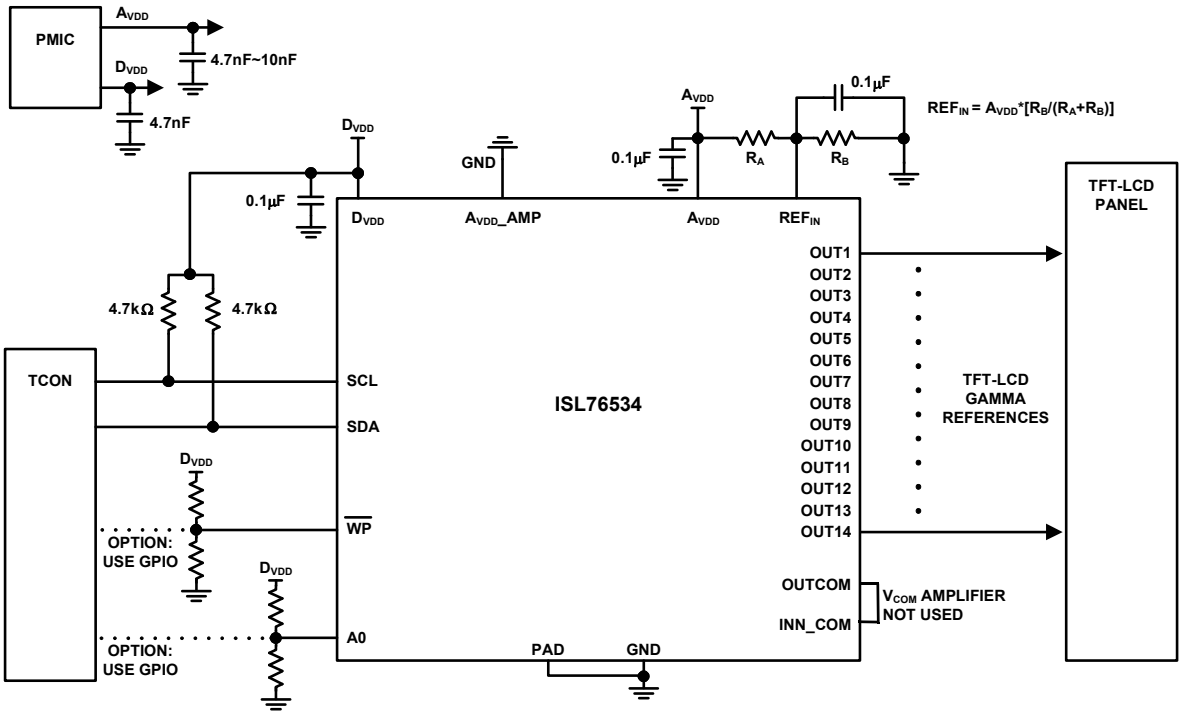


FIGURE 31. TFT-LCD GAMMA REFERENCE GENERATOR: V_{COM} AMPLIFIER DISABLED

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
July 27, 2016	FN8866.0	Initial release

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

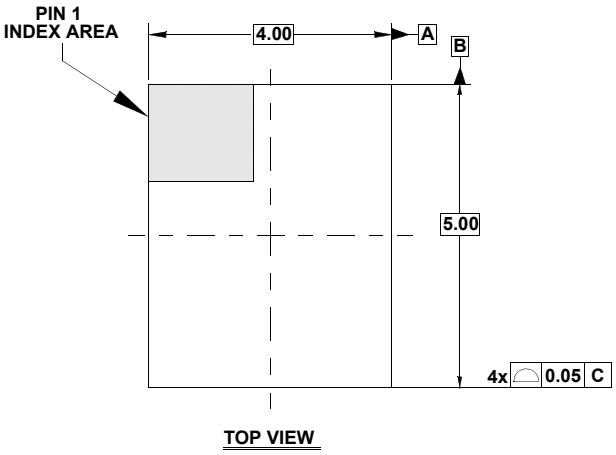
Reliability reports are also available from our website at www.intersil.com/support.

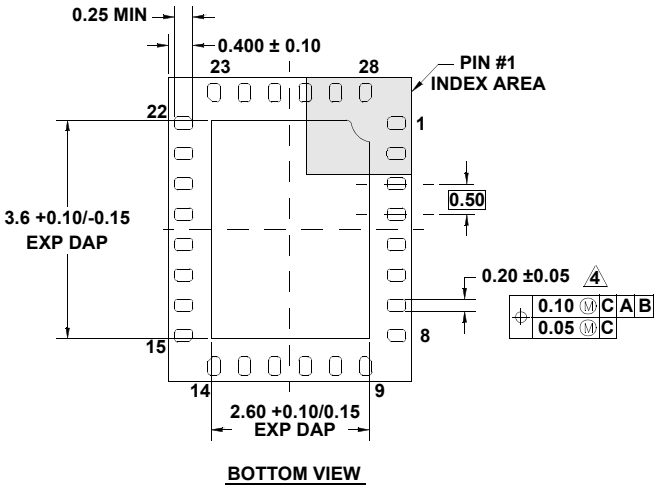
Package Outline Drawing

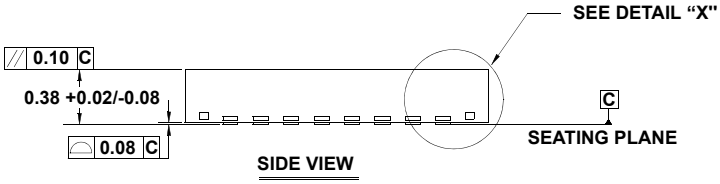
L28.4x5D

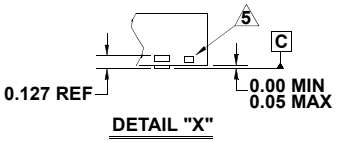
28 LEAD SUPER THIN QUAD FLAT NO LEAD PLASTIC PACKAGE

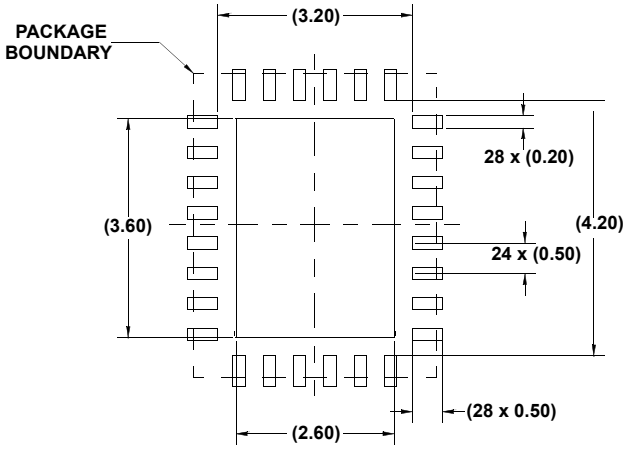
Rev 0, 3/11











NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal. If terminal has a radius on its end, dimension should not be measured in that radius area.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.
7. Reference Document: JEDEC MO-228.