ISL78224

4-Phase 12V/48V Bidirectional Synchronous PWM Controller

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The ISL78224 is a 4-phase, bidirectional, synchronous PWM controller designed to perform power conversion between 12V and 48V buses up to 3kW at >95% conversion efficiency. One ISL78224 supports both Buck and Boost power conversion, enabling a compact and robust design with minimum components.

The ISL78224 regulates both voltage and current to control power transfer from bus to bus. The multiphase architecture uses interleaved timing to support up to four parallel power stages per ISL78224. By interleaving the power stages, the ripple frequency is multiplied, reducing input and output ripple voltage and current. Lower ripple results in fewer input/output capacitors and therefore lower component cost and smaller circuit implementation.

The IC is designed to be interleaved in a master/slave architecture to be scalable for higher power. Integrated within the device is a dual-output Flyback controller that generates both a 12V supply for the power stage FET drivers and a 6V supply for the ISL78224 from either of the two buses. A 200mA auxiliary linear regulator supplies a local microcontroller or interface devices.

A PMBus interface provides system control and diagnostics to support functional safety requirements. This digital interface offers the system controller the ability to program operating modes, voltage and current limit warning and protection thresholds, individual fault response, and rapid fault condition detection.

Applications

- Automotive bidirectional DC/DC converter
- Bidirectional DC/DC for smart grid
- Backup battery DC/DC converter

Features

- 4-phase bidirectional synchronous 12V to 48V controller
- Master/slave architecture supports up to 4 ICs in parallel
- Voltage and current regulation
- Phase dropping facilitated with companion FET driver
- 2% current monitor gain accuracy from 0 to full load
- Supply and clock redundancy for functional safety
- Cycle-by-cycle peak current limiting
- Cycle-by-cycle negative current limiting
- Digitally programmable average current limit
- Analog and/or digital control of output voltage
- PMBus for status monitoring and fault response control
- Selectable phase dropping and diode emulation for light-load efficiency improvement
- Comprehensive protection with selectable hiccup or latch-off fault responses
- Digitally programmable warning and fault thresholds
- Dual-output Flyback controller
- 200mA adjustable output linear regulator
- 10mmx10mm 64 Ld TQFP with exposed pad thermal interface
- AEC-Q100 Grade 1

Related Literature

For a full list of related documents, visit our website

- ISL78224 product page

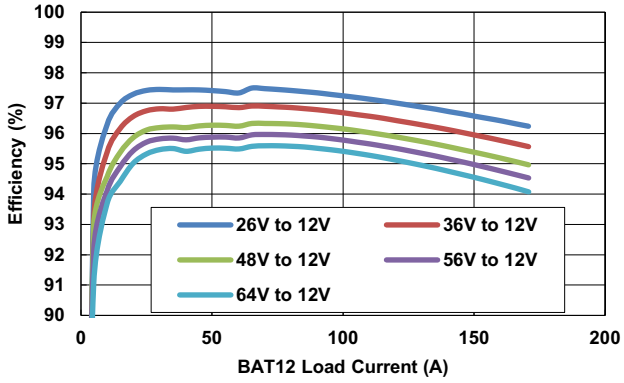


Figure 1. Buck Mode, DE Mode, Phase-Drop Enabled

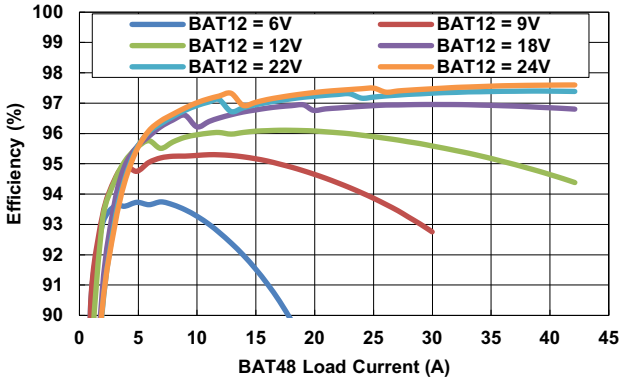


Figure 2. Boost Mode, DE Mode, Phase-Drop Enabled

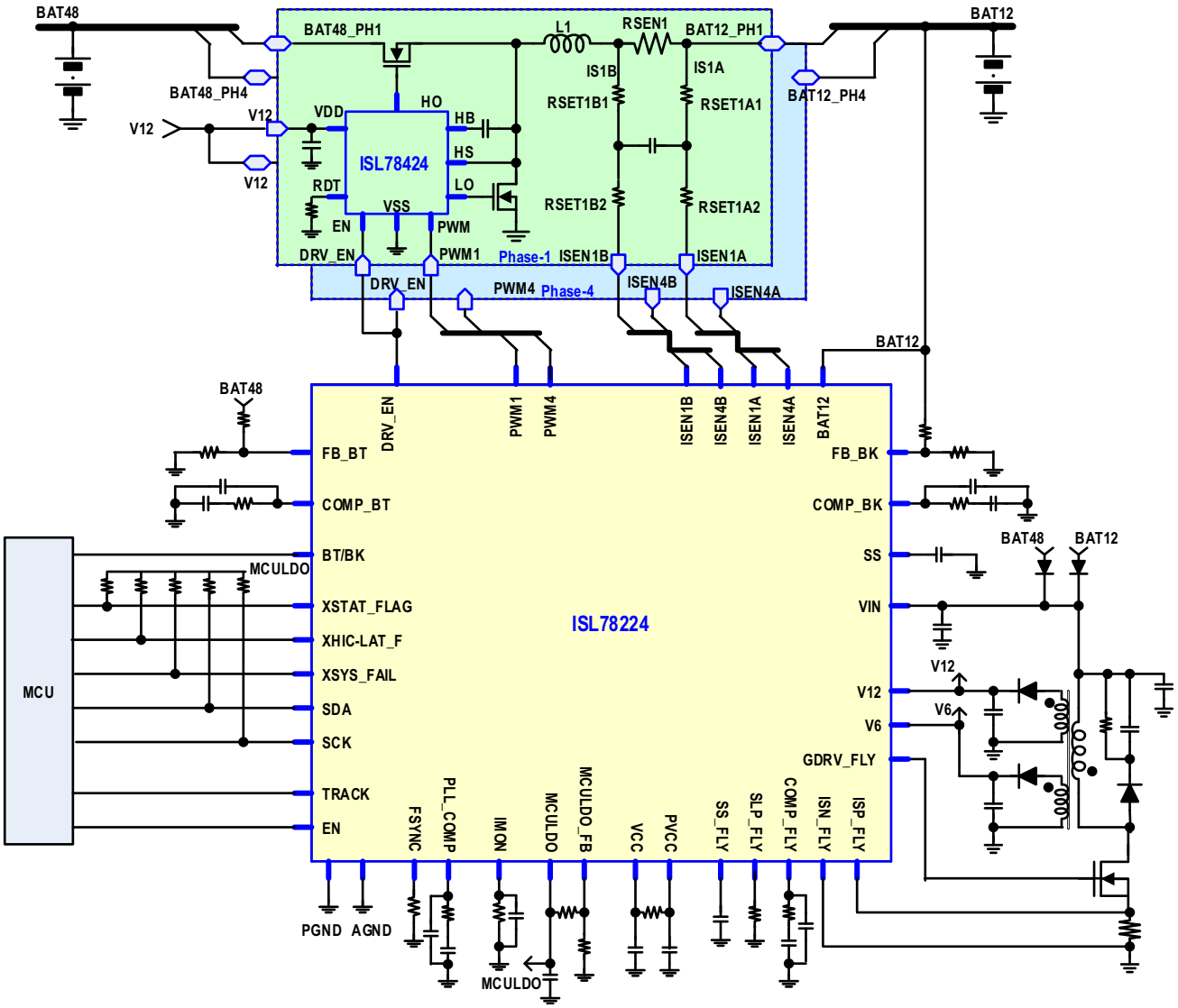


Figure 3. Simplified Typical Application Schematic

Contents

1. Overview

1.1 Typical Application Schematics

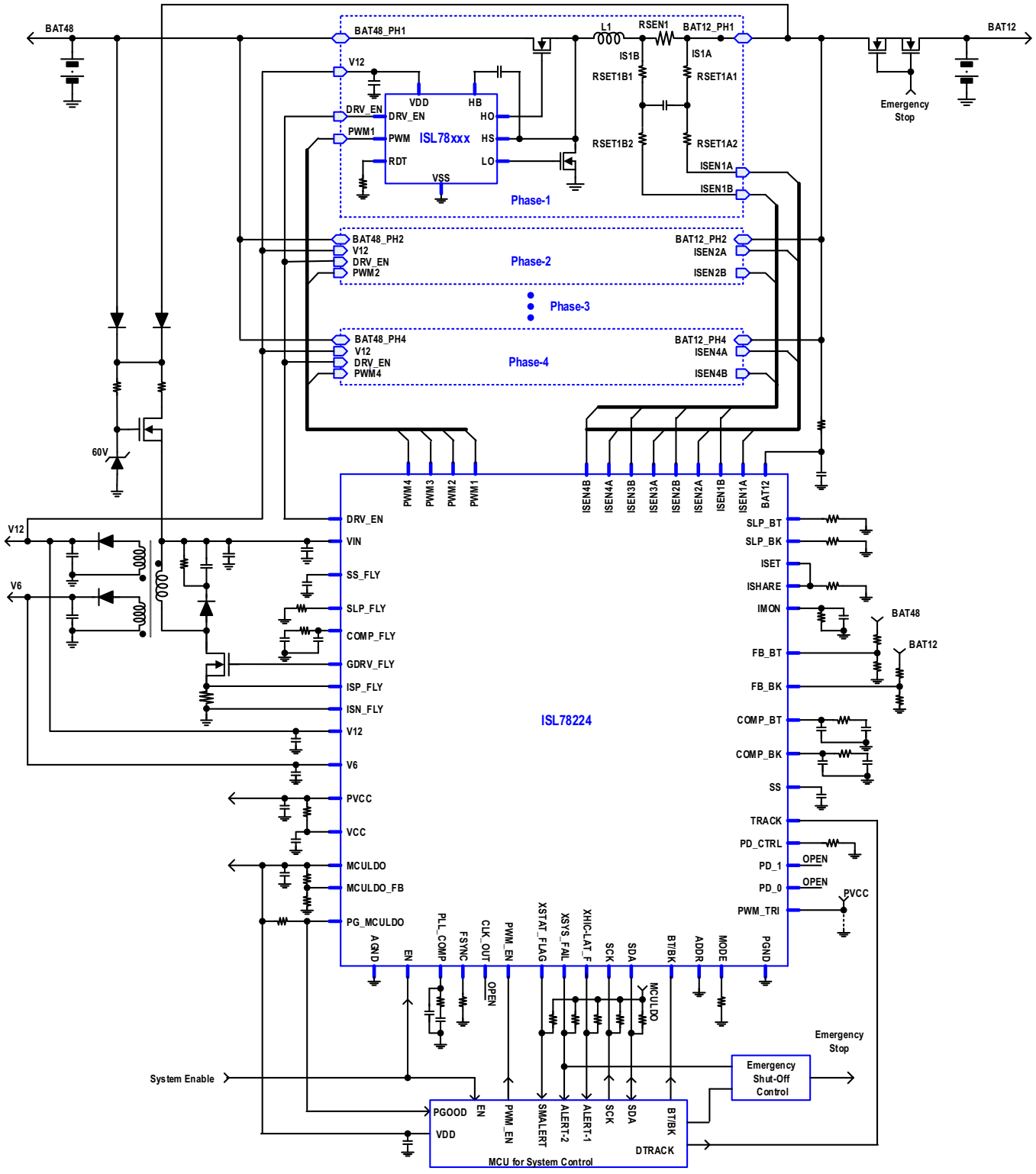


Figure 4. 4-Phase Synchronous Bidirectional Converter with Single Device Configuration

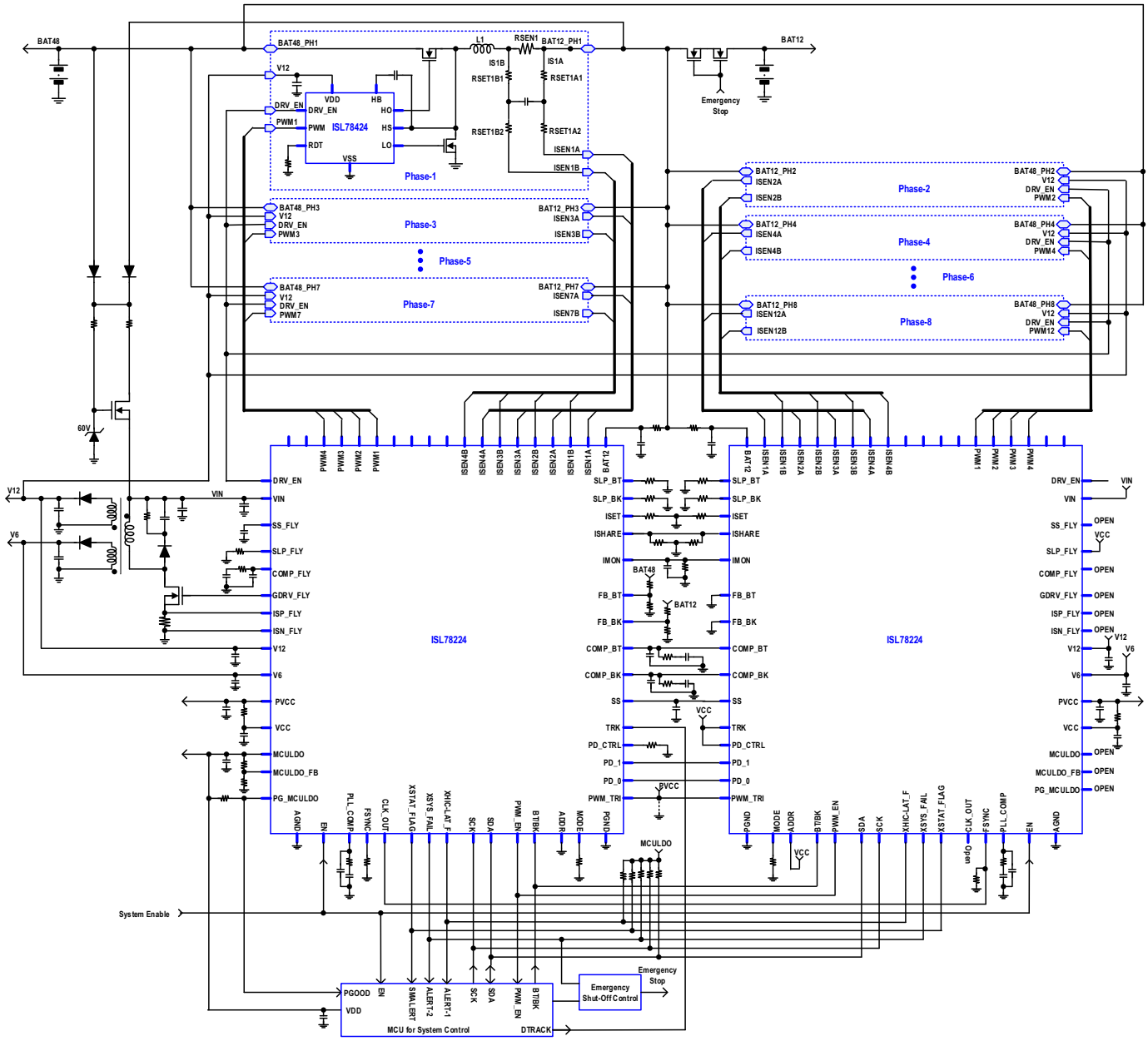


Figure 5. 8-Phase Synchronous Bidirectional Converter with Two-Device Parallel Configuration

1.2 Block Diagram

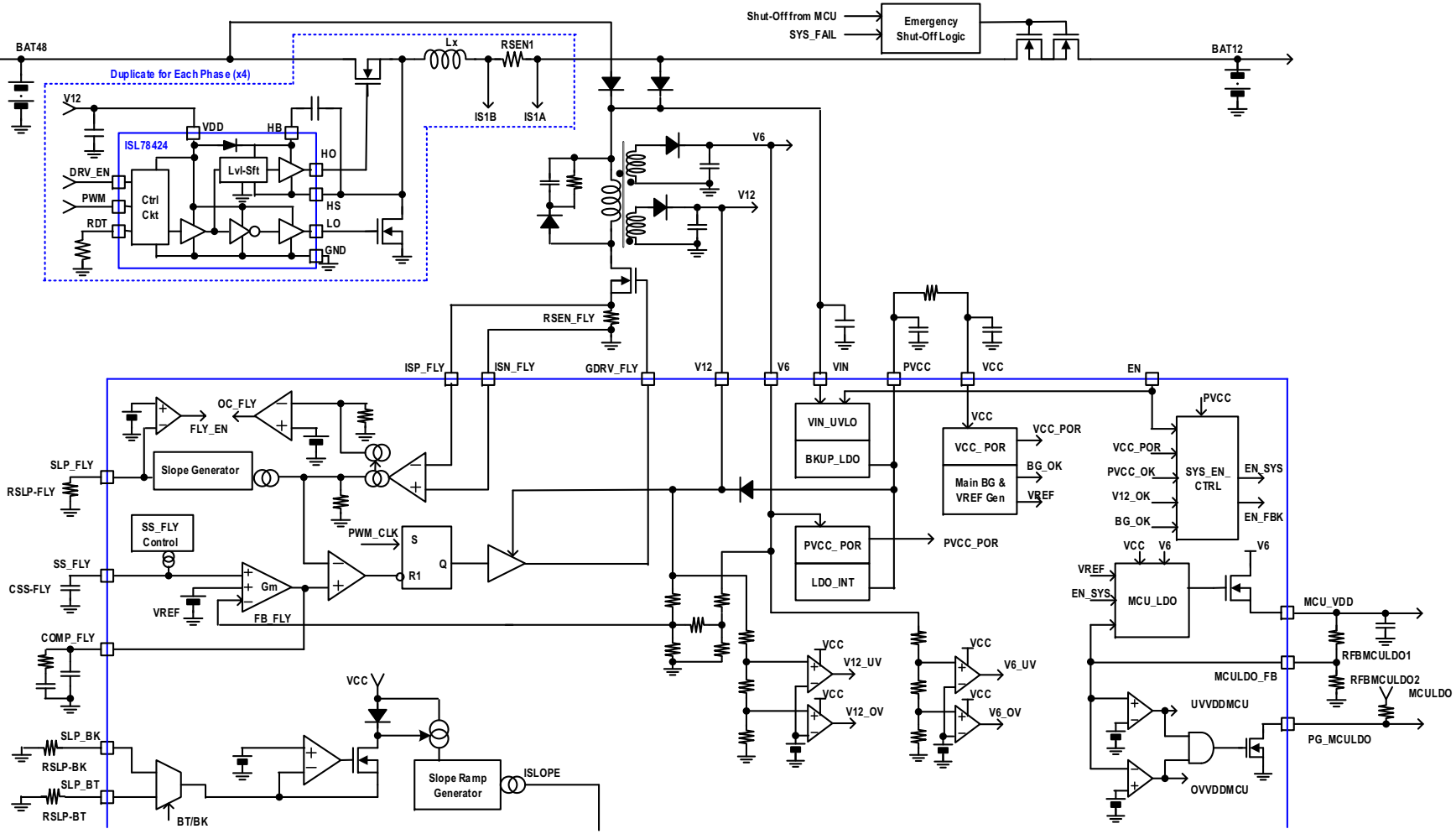


Figure 6. Block Diagram - Top

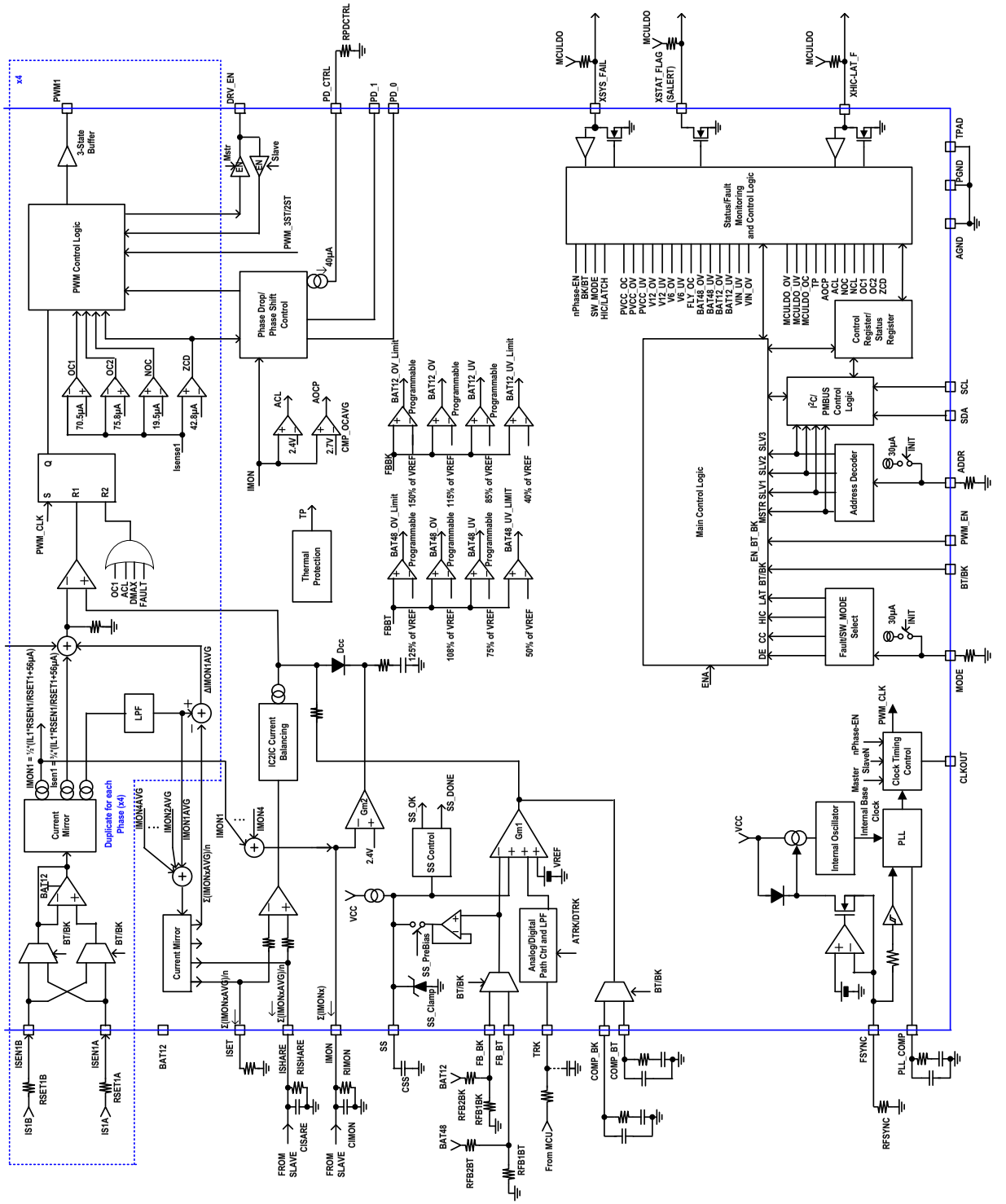


Figure 7. Block Diagram - Bottom

1.3 Ordering Information

Part Number (Notes 2, 3)	Part Marking	Temp Range (°C)	Tape and Reel (Units) (Note 1)	Package (RoHS Compliant)	Pkg. Dwg. #
ISL78224ANZ	ISL78224ANZ	-40 to +125		64 Ld 10x10 EP-TQFP	Q64.10x10H
ISL78224ANZ-T	ISL78224ANZ	-40 to +125	1k	64 Ld 10x10 EP-TQFP	Q64.10x10H
ISL78224EVKIT1Z	ISL78224 evaluation kit				

Notes:

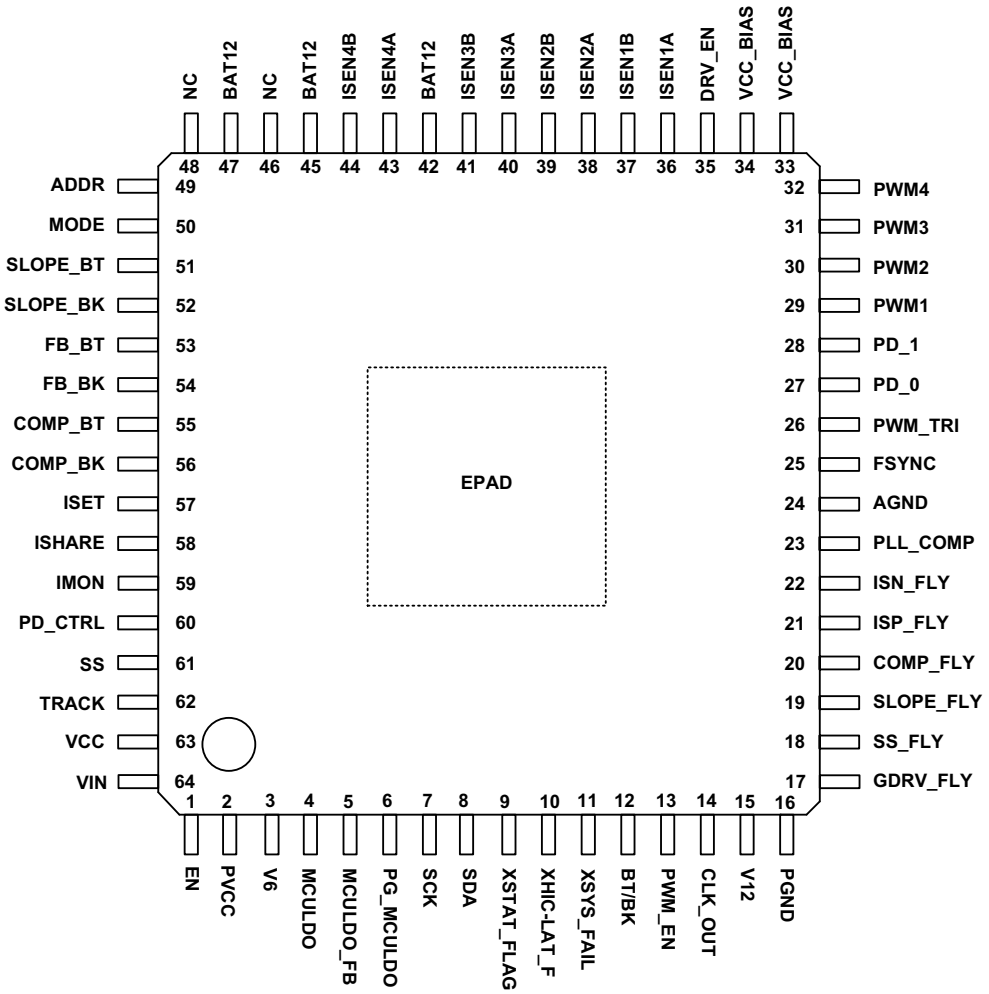
1. Refer to TB347 for details about reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), see the ISL78224 device information page. For more information about MSL, see TB363.

Table 1. Key Differences Between Family of Parts

Part Number	Phase Output
ISL78224	4-Phase Output
ISL78226	6-Phase Output

1.4 Pin Configurations

64 Ld 10x10 TQFP
Top View



1.5 Pin Descriptions

Pin Name	I/O	Pin Number	Description
EN	I	1	Device Enable/shut-off control pin. When the EN pin is driven above 1.4V, the ISL78224 is active. The operating mode depends on the configurations of the mode setting pins, control registers, and fault register status. The fault status is kept while the EN pin is high unless internal Power-On Reset (POR) becomes low. When the EN pin is driven below 0.7, the device clears all fault statuses and goes into shutdown mode. While in shutdown mode, the device's current consumption is less than 1µA.
PVCC	PS (O)	2	Internal linear regulator output that provides bias for the internal analog and logic circuits. The PVCC operating range is 4V to 5.4V. A ceramic capacitor of 4.7µF minimum is recommended between PVCC and PGND for noise decoupling. Connect this capacitor as close as possible to PVCC and PGND.
V6	I	3	V6 is biased by an external ~6V source and is one of the control loop feedback inputs for the Flyback converter.

Pin Name	I/O	Pin Number	Description
MCULDO	O	4	The output of MCULDO supply an external MCU or an external general purpose circuit. The output voltage of MCULDO can be adjusted with an external feedback resistor network which is connected between this output, MCULDO_FB, and AGND.
MCULDO_FB	I	5	Feedback for the MCULDO output. The midpoint of a resistor voltage divider between MCULDO and AGND is connected to this pin and is compared with an internal reference voltage (1.2V) to regulate the MCULDO output voltage.
PG_MCULDO	O	6	An open-drain output for MCULDO voltage power-good indication. Pull this pin up with a resistor to the supply voltage of an external MCU interface. When the output voltage is within the regulation limit and soft-start is complete, the internal pull down of this pin is released and this pin is pulled high by the external resistor. This pin is pulled low when the MCULDO output OV or UV condition is detected.
SCK	I	7	I^2C/SMBus communication clock input. Requires external pull-up.
SDA	I/O	8	I^2C/SMBus communication data input/output. Requires external pull-up.
XSTAT_FLAG	O	9	An open-drain output that indicates any status changes at the internal status register. Pull this pin up with a resistor to VCC or to the supply voltage of an external MCU interface. This includes both fault condition detection and warning condition detection. To recognize the status, an external MCU should read the status registers from the I^2C/PMBus.
XHIC-LAT_F	I/O	10	Open-drain output that indicates a Hiccup or Latch-Off fault and communicates the hiccup or latch-off fault status between the multiple ISL78224 devices when used in parallel. This node must be pulled up to VCC with an external resistor. If one of the devices detects the Hiccup or Latch-Off fault, the pin of the fault detected device is driven low and pulls down the pins of all the other devices connected in parallel. All devices connected in parallel devices stop all PWM outputs and DRV_EN pins are driven low. When Hiccup mode is selected, the device tries to restart from soft-start at 500ms intervals until the fault condition is removed. When Latch-Off mode is selected, the EN or PWM_EN pins must be toggled for restart.
XSYS_FAIL	O	11	An open-drain output that indicates a potential serious system failure condition. Pull this pin up with a resistor to VCC or to the external MCU interface supply voltage. Detects cases in which the high-side transistor is shorted, low-side transistor is shorted, the BAT48 is shorted to GND, or an abnormally large current is sensed at the current-sense resistor. When this abnormal condition (continuous Overcurrent-2 (OC2) or Negative Overcurrent (NOC) in both on and off cycles) continues for three switching cycles, the device detects this serious failure condition and pulls the XSYS_FAIL pin low. Renesas recommends designing the system with an emergency protection circuit to disconnect the battery from the system using a fuse or an external path switch when this signal is pulled low. This flag indicates a potential serious system failure such as a high-side or low-side transistor short. This flag does not detect all of the serious failure conditions, such as when the high-side or low-side transistor is shorted with some resistance. The combination of fault detection information and an additional external failure detection system is recommended to build robust failure detection.
BT/BK	I	12	Converter direction selector pin. When this pin is high, the device operates in Boost mode. When this pin is low, the device operates in Buck mode.
PWM_EN	I	13	Bidirectional PWM controller enable/disable control signal. While this pin is Low, the bidirectional PWM controller is turned off. When this pin becomes High, the bidirectional PWM controller starts up from the initialized condition. If latch-off occurs, toggling this pin restarts the bidirectional PWM output. This pin does not affect the Flyback converter.
CLK_OUT	O	14	Provides a clock signal to synchronize with another ISL78224. The rising edge signal on the CLKOUT pin is the same timing of the rising edge of the PWM1 output.
V12	I	15	Monitors the bridge driver power supply voltage, which is generated by the Flyback regulator. The Flyback regulator output voltage for the bridge driver is set to 12V internally. This pin is also used as the power supply for the gate drive of the flyback MOSFET.
PGND	GND	16	Power and digital ground pin. This pin is the reference for internal digital blocks and is connected to the PWMx output buffer and Flyback gate driver that generates noisy peak currents. Sensitive analog signal traces should not share common traces with this driving return path. Connect this pin directly to the copper ground plane and put several vias as close as possible to this pin. The PGND and AGND should be connected at a common solid ground plane near the IC.

Pin Name	I/O	Pin Number	Description
GDRV_FLY	O	17	PWM output to drive the gate of primary side switching NMOS of Flyback regulator. At system startup, this driver is powered by an internal backup LDO output (5V typical) and is switched over to V12 when the V12 voltage exceeds the internal backup LDO output voltage.
SS_FLY	I	18	Use this pin to set the soft-start time of Flyback regulator output. A capacitor placed from SS_FLY to GND sets up the soft-start ramp rate and in turn, determines the soft-start time. Refer to the "Flyback Controller" on page 72 for more information.
SLOPE_FLY	I	19	Programs the slope compensation for the Flyback controller. Connect a resistor from the SLOPE_FLY pin to GND. Refer to the "Flyback Controller" on page 72 for more information.
COMP_FLY	I/O	20	The output of the transconductance amplifier of the Flyback controller. Place the compensation network between the COMP_FLY pin and GND for compensation loop design of the Flyback regulator. Refer to the "Flyback Controller" on page 72 for more information.
ISP_FLY	I	21	Connect this pin to the positive node of the current-sense resistor, which is connected to the source of the primary side switching NMOS of the Flyback regulator. Refer to the "Flyback Controller" on page 72 for more information.
ISN_FLY	I	22	Connect this pin to the GND side of the current-sense resistor, which is connected to the source of the primary side switching NMOS of the Flyback regulator. Refer to the "Flyback Controller" on page 72 for more information.
PLL_COMP	I/O	23	PLL_COMP is used as the compensation node for the PLL. A second order passive-loop filter connected between the PLL_COMP pin and GND compensates the PLL feedback loop.
AGND	GND	24	Analog ground pin and internal analog circuit reference. Connect this pin to a large, quiet copper ground plane. In PCB layout planning, avoid having switching current flowing into the AGND area. The PGND and AGND should be connected at a common solid ground plane.
FSYNC	I	25	Adjusts the internal oscillator frequency or to synchronize with an external clock input. The internal oscillator switching frequency is adjusted with a resistor from this pin to GND. If an external synchronous clock is applied to this pin, the internal oscillator locks to the rising edge. There is a 25ns (typical) delay from the FSYNC pin's input clock rising edge to the PWM1 rising edge.
PWM_TRI	I	26	Enables the Tri-Level of the PWM output signal. Pull the PWM_TRI to VCC to enable the Tri-Level PWM output signals so the PWM output can be at the 2.5V tri-level condition. To use the Tri-Level output, the external driver needs to be applicable to this function. The ISL78420 is an example. Pulling this pin to GND forces the PWM output to be two-level logic.
PD_0	I/O	27	If the ISL78224 is used stand-alone, PD_0 and PD_1 should not be connected. PD_0 and PD_1 control the phase dropping between multiple ISL78224s in parallel. If the controller is configured as the Master Controller, PD_0 and PD_1 are configured as outputs to indicate the number of the operation phases of the system to slave devices. The Slave Controller receives the phase dropping indicator signal from PD_0 and PD_1. The relation between the phase dropping and PD_0 and PD_1 levels are described in Table 2 on page 65. Phases are dropped or added three switching cycles after the changes of PD_0 and PD_1 signals for both master and slave controllers. The PD_0 and PD_1 signals also indicate the Boot-Refresh timing to the slave devices from the master device. When the master detects the Boot-Refreshing timing while operating in Buck mode, the PD_0 and/or PD_1 pins are toggled to low level for one PLL-Clock period (1/12 of PWM clock cycle), which initializes the boot refresh timing of the slave devices.
PD_1	I/O	28	
PWM1	O	29	Pulse-Width Modulation (PWM) output for Phase 1. Connect this output to the PWM input of an external driver IC of Phase 1.
PWM2	O	30	PWM output for Phase 2. Connect this output to the PWM input of an external driver IC of Phase 2.
PWM3	O	31	PWM output for Phase 3. Connect this output to the PWM input of an external driver IC of Phase 3. If this pin is connected to VCC, the device operates in 2-phase mode and PWM3 and PWM4 outputs are disabled.
PWM4	O	32	PWM output for Phase 4. Connect this output to the PWM input of an external driver IC of Phase 4. If this pin is connected to VCC, the device operates in 3-phase mode and PWM4 output is disabled.
VCC_BIAS	I	33, 34	VCC_BIAS. Connect this pin to VCC.

Pin Name	I/O	Pin Number	Description
DRV_EN	O	35	Driver Enable signal output pin. This pin is connected to the Enable pins of the drivers. When the ISL78224 is ready to output the PWM signal, the DRV_EN signal goes high. If the ISL78224 is disabled, or the hiccup/latch-off fault condition occurs, or the MCU overrides the DRV_EN register to be low (disabled), this output is pulled low and disables the drivers.
ISEN1A	I	36	Current-Sense Amplifier (CSA) 1 input. With a combination of ISEN1B and gain setting resistors R_{SET1A} and R_{SET1B}, the current flowing at Current-Sense Resistor-1 is converted to the sensed current signal and forwarded into the device. Connect ISEN1A at the negative side of Current-Sense Resistor-1 in Buck mode configuration. This pin ultimately senses the BAT12 voltage side of the current-sensing shunt through the filter (refer to Figures 6 and 7). The resistive shunt must be Kelvin connected; do not allow this connection to take place anywhere else on the BAT12 plane. The sensed current information is used for peak current mode control, average current control, and overcurrent protections.
ISEN1B	I	37	The other side of Current-Sense Amplifier (CSA) 1 input. With a combination of ISEN1A and gain setting resistors, R_{SET1A} and R_{SET1B}, the current flowing at Current-Sense Resistor-1 is converted to the sensed current signal and forwarded into the device. Connect ISEN1B at the positive side of Current-Sense Resistor-1 in Buck mode configuration. This pin ultimately senses the inductor side of the current-sensing shunt through the filter (refer to Figures 6 and 7). The resistive shunt must be Kelvin connected. The sensed current information is used for peak current mode control, average current control, and overcurrent protections.
ISEN2A	I	38	Current-Sense Amplifier (CSA) 2 input. With a combination of ISEN2B and gain setting resistors, R_{SET2A} and R_{SET2B}, the current flowing at Current Sense Resistor-2 is converted to the sensed current signal and forwarded into the device. Connect ISEN2A at the negative side of Current-Sense Resistor-2 in Buck mode configuration. This pin ultimately senses the BAT12 voltage side of the current-sensing shunt through the filter (refer to Figures 6 and 7). The resistive shunt must be Kelvin connected; do not allow this connection to take place anywhere else on the BAT12 plane. The sensed current information is used for peak current mode control, average current control, and overcurrent protections.
ISEN2B	I	39	The other side of Current-Sense Amplifier (CSA) 2 input. With a combination of ISEN2A and gain setting resistors, R_{SET2A} and R_{SET2B}, the current flowing at Current-Sense Resistor-2 is converted to the sensed current signal and forwarded into the device. Connect ISEN2B at the positive side of Current-Sense Resistor-2 in Buck mode configuration. Ultimately senses the inductor side of the current-sensing shunt through the filter, refer to Figures 6 and 7. The resistive shunt MUST be Kelvin connected. The sensed current information is used for peak current mode control, average current control, and overcurrent protections.
ISEN3A	I	40	Current-Sense Amplifier (CSA) 3 input. With a combination of ISEN3B and gain setting resistors, R_{SET3A} and R_{SET3B}, the current flowing at Current-Sense Resistor-3 is converted to the sensed current signal and forwarded into the device. Connect ISEN3A at the negative side of Current-Sense Resistor-3 in Buck mode configuration. This pin ultimately senses the BAT12 voltage side of the current-sensing shunt through the filter (refer to Figures 6 and 7). The resistive shunt must be Kelvin connected; do not allow this connection to take place anywhere else on the BAT12 plane. The sensed current information is used for peak current mode control, average current control, and overcurrent protections. If this phase is not used, connect the ISEN3A to BAT12.
ISEN3B	I	41	The other side of Current-Sense Amplifier (CSA) 3 input. With a combination of ISEN3A and gain setting resistors, R_{SET3A} and R_{SET3B}, the current flowing at Current-Sense Resistor-3 is converted to the sensed current signal and forwarded into the device. Connect ISEN3B at the positive side of Current-Sense Resistor-3 in Buck mode configuration. This pin ultimately senses the inductor side of the current-sensing shunt through the filter (refer to Figures 6 and 7). The resistive shunt must be Kelvin connected. The sensed current information is used for peak current mode control, average current control, and overcurrent protections. If this phase is not used, float or do not connect the ISEN3B pin.
BAT12	I	42	Power supply for internal current-sense amplifier. Connect to the 12V side of current sense resistor with an RC filter (10Ω resistor and 0.1µF ceramic capacitor).

Pin Name	I/O	Pin Number	Description
ISEN4A	I	43	Current-Sense Amplifier (CSA) 4 input. With a combination of ISEN4B and gain setting resistors, R_{SET4A} and R_{SET4B}, the current flowing at Current-Sense Resistor-4 is converted to the sensed current signal and forwarded into the device. Connect ISEN4A at the negative side of Current-Sense Resistor-4 in Buck mode configuration. This pin utimately senses the BAT12 voltage side of the current-sensing shunt through the filter (refer to Figures 6 and 7). The resistive shunt must be Kelvin connected; do not allow this connection to take place anywhere else on the BAT12 plane. The sensed current information is used for peak current mode control, average current control, and overcurrent protections. If this phase is not used, connect the ISEN4A to BAT12.
ISEN4B	I	44	The other side of Current-Sense Amplifier (CSA) 4 input. With a combination of ISEN4A and gain setting resistors, R_{SET4A} and R_{SET4B}, the current flowing at Current-Sense Resistor-4 is converted to the sensed current signal and forwarded into the device. Connect ISEN4B at the positive side of Current-Sense Resistor-4 in Buck mode configuration. This pin ultimately senses the inductor side of the current-sensing shunt through the filter (refer to Figures 6 and 7). The resistive shunt must be Kelvin connected. The sensed current information is used for peak current mode control, average current control, and overcurrent protections. If this phase is not used, float or do not connect the ISEN4B pin.
BAT12	I	45, 47	Connect this pin to BAT12.
NC	I	46, 48	Do not connect this pin.
ADDR	I	49	Controller address configuration pin. At the initialization phase, the device forces 30µA constant current at this pin and determines the order of the device (Master, Slave-1, Slave-2, Save-3) based on this pin's setting. If this pin is connected to GND directly, the device operates as the Master. If this pin is connected to VCC directly, the device operates as Slave-1. If a 33.2kΩ or 68.1kΩ resistor is connected between this pin and GND, the device operates as Slave-2 and Slave-3, respectively.
MODE	I	50	The MODE pin determines the operation switching mode (Diode Emulation (DE) mode or Forced PWM mode) and fault response (hiccup or latch-off) at the initialization period of device startup. To select the proper operation mode, connect a resistor between this pin to GND or directly connect to VCC or GND. This pin sources 30µA current while in the initialization period. If the pin is connected to GND directly, the device operates in DE mode and has the Hiccup fault response. If a 33.2kΩ resistor is connected between this pin and GND, the device operates in PWM mode and has the Hiccup fault response. If a 68.1kΩ resistor is connected between this pin and GND, the device operates in DE mode and has the Latch-Off fault response. If this pin is directly connected to VCC, the device operates in Forced PWM mode and has the Latch-Off fault response. DE and Forced PWM mode cannot be changed by internal register options when selected at EN.
SLOPE_BT	I	51	Programs the slope of the internal slope compensation for Boost mode operation. Connect a resistor from the SLOPE_BT pin to GND. This pin is activated when BT/BK pin is high. Slope resistor value setting and selection guidance is provided in the "Loop Compensation Design - Boost" section on page 136.
SLOPE_BK	I	52	Programs the slope of the internal slope compensation for Buck mode operation. Connect a resistor from the SLOPE_BK pin to GND. This pin is activated when BT/BK pin is high. Slope resistor value setting and selection guidance is provided in the "Loop Compensation Design: Buck" section on page 139.

Pin Name	I/O	Pin Number	Description
FB_BT	I	53	The inverting input of the transconductance amplifier for Boost mode operation and the input for BAT48 rail monitoring. Place a resistor voltage divider between the FB_BT pin, the BAT48 rail, and GND to set the Boost mode output voltage and to monitor the BAT48 rail voltage. This function is activated when configured as the Master and the BT/BK pin is high. When configured as a slave device, the combination of FB_BT and FB_BK determines the total slave device count for the proper phase shifting. If the system is configured as a 1-master/1-slave operation, connect FB_BT and FB_BK pins of the slave device to GND. If the system is configured as a 1-master/2-slave operation, connect the FB_BT and FB_BK pins of the slave devices to VCC. If the system is configured as a 1-master/3-slave operation, connect the FB_BT and FB_BK pins of the slave devices to GND and VCC, respectively.
FB_BK	I	54	The inverting input of the transconductance amplifier for Buck mode operation and the input for BAT12 rail monitoring. Place a resistor voltage divider between the FB_BK pin, the BAT12 rail, and GND to set the Buck mode output voltage and to monitor the BAT12 rail voltage. This pin is activated when configured as the Master and the BT/BK pin is low. When configured as a slave device, the combination of the FB_BT and FB_BK determines the total slave device count for the proper phase shifting. If the system is configured as a 1-master/1-slave operation, connect the FB_BT and FB_BK pins of the slave device to GND. If the system is configured as a 1-master/2-slave operation, connect the FB_BT and FB_BK pins of the slave devices to VCC. If the system is configured as a 1-master/3-slave operation, connect the FB_BT and FB_BK pins of the slave devices to GND and VCC, respectively.
COMP_BT	I/O	55	The output of the transconductance amplifier for Boost mode operation. Place the compensation network between the COMP_BT pin and GND for compensation loop design. This function is activated when the BT/BK pin is high. For information about setting the compensation network, refer to "Loop Compensation Design - Boost" on page 136.
COMP_BK	I/O	56	The output of the transconductance amplifier for Buck mode operation. Place the compensation network between the COMP_BK pin and GND for compensation loop design. This function is activated when the BT/BK pin is high. For information about setting the compensation network, refer to the "Loop Compensation Design: Buck" on page 139.
ISET	I/O	57	An average output current monitor pin of the phases controlled by this device. The output current from this pin is proportional to the sum of averaged sense current of each phases at ISENx plus an offset current. A resistor (R_{ISET}) is required at this pin to make a reference voltage for current balancing between the devices.
ISHARE	I/O	58	Indicates the average current sensed at all of the current-sense resistors in the system when two or more controller devices are connected in parallel. With a filter comprised of a resistor and a capacitor connected in parallel from the ISHARE pin to GND, the voltage at the ISHARE pin describes the average output current and is used for current balancing between the controller devices. The "common to all" ISHARE voltage is compared with the individual ISET voltage in each device and generates an error signal that adjusts the current balance between the devices. For this purpose, the resistor value on this pin should be R_{ISET}/n, where n represents the number of master and slave devices connected in parallel. If the controller is used as a stand-alone in the system, connect ISHARE to ISET.

Pin Name	I/O	Pin Number	Description
IMON	I/O	59	Used for the Average Current Limiting and Average Current Protection. In Boost mode operation, a current that is proportional to the average inductor current plus an offset current while the low-side transistor is in off state comes out from this pin. In Buck mode operation, the average inductor current, which is equivalent to the average output current, comes out from this pin. An external RC filter circuit is required to filter out the pulse current. The IMON pin is used for the Average Current Limiting and Protection as well as Phase Dropping. - Constant Current Limiting: An average constant output current limiting loop is implemented by comparing the average current-sense signal and a 2.4V reference to have the output average current limited at a constant level. - Average Current Protection: If IMON pin voltage is higher than 2.7V, the device moves into the Hiccup mode or Latch-off mode depending on the HIC/LATCH pin configuration. When a phase dropping operation is selected (PD_CTRL is connected to GND with an external resistor), the voltage at this pin is used to determine phase drop timing. For example, if a 4-phase operation is selected, a 2-phase to 3-phase add occurs when the IMON pin voltage is 86% of the PD_CTRL pin voltage. Likewise, a 3-phase to 4-phase add occurs when the IMON pin voltage is 89% of the PD_CTRL pin voltage.
PD_CTRL	I	60	Selects whether the phase drop function is enabled or not. If the Phase Drop function is enabled, this pin provides the reference level of phase dropping/adding threshold. If the PD_CRTL is connected to VCC, the Phase Drop function is disabled. The device operates in the maximum phase count defined by the connection of PWM3 and PWM4 at the initialization stage. To enable the Phase Drop feature, connect a resistor from PD_CTRL to GND. A 40µA constant current flows from this pin and generates the reference voltage for the phase dropping/adding threshold. The phase dropping/adding threshold is determined by comparing the PD_CTRL pin voltage and IMON pin. Phase drop thresholds can be overwritten by internal register settings.
SS	I	61	Use this pin to set the soft-start time. This pin is commonly used for both Buck mode and Boost mode. A capacitor placed from SS to GND sets up the soft-start ramp rate and, in turn, determines the soft-start time. For Master/Slave operation, the soft-start current is increased by the number of controllers used in parallel. As an example, 5µA is multiplied by the number of controllers used. If maintaining a soft-start time previously achieved by a single controller is desired, use a capacitor that is N times larger.
TRACK	I	62	Tracking reference input for both Buck mode and Boost mode operation to provide an external reference for the device feedback loop to follow. By default, the device is defined as Digital Tracking. When the analog input is selected by register setting from I^2C/PMBus, the feedback reference tracks the analog voltage applied to this pin. Digital tracking is accomplished by injecting a pulse width modulated rectangular waveform into the TRACK pin with respect to GND. The output voltage is a function of the duty ratio of this PWM signal. Connect this pin to VCC if the tracking function is not used. The lowest voltage of SS, TRACK, or internal reference (1.6V) is used as the reference of the Buck or Boost mode voltage error amplifier.
VCC	PS (I)	63	Provides bias power for the IC analog circuit. Connect an RC filter (10Ω resistor and 1µF capacitor) between this pin and PVCC. Use a minimum 1µF ceramic capacitor between VCC and GND for noise decoupling purposes.
VIN	PS	64	Power Supply input for device wakeup. At the beginning of the startup of the system, the internal backup LDO, reference, and enable control circuit are powered from this pin. The Flyback controller is powered by the backup LDO while starting up. After the flyback starts up, V6 is active and the bias current is supplied by V6.
EPAD	-	EPAD	Bottom thermal pad. It is not connected to any electrical potential of the IC. In layout, it must be connected to a PCB large ground copper plane that does not contain noisy power flows. Put multiple vias (as many as possible) in this pad, connecting to the ground copper plane to help reduce the IC's θ_{JA}.

2. Specifications

2.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
Supply Voltage: VIN (Note 5)	- 0.3	+65	
Voltage at V12, GDRV_FLY	-0.3	+18	V
Voltage at V6	-0.3	+14	V
Voltage at PVCC, VCC	-0.3	+6.5	V
Voltage Differences at V_{ISENxA} - V_{ISENxB}	-300	+300	mV
Voltage at ISENxA, ISENxB		BAT12 ± 0.3	V
Voltage at BAT12	-0.3	+45	V
Voltage at All Other Pins	-0.3	V_{CC} + 0.3	V
ESD Rating	**Value**		**Unit**
Human Body Model (Tested per AEC-Q100-002)	2		kV
Charged Device Model (Tested per AEC-Q100-011)	750		V
Latch-Up (Tested per AEC-Q100-004)	100		mA

Notes:

4. Unless otherwise noted, all voltages provided in this specification refer to GND.
5. Maximum Operation Voltage includes DC operation voltage level and transient peak noise level.

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

2.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
64 Ld 10x10 EP-TQFP Package (Notes 6, 7)	25	1.2

Notes:

6. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with “direct attach” features. See TB379.
7. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature (Plastic Package)		+150	°C
Maximum Storage Temperature Range	-65	+150	°C
Pb-Free Reflow Profile	Refer to TB493		

2.3 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Supply Voltage at VIN	6	64	V
Voltage at V12	9	15	V
Voltage at V6	5.2	11	V
Voltage at GDRV_FLY	0	15	V
Voltage at BAT12	6	40	V
Output Voltage at MCULDO	2.5	5	V

Output Current at MCULDO	0	200	mA
Output Current at PVCC	0	50	mA
Voltage at ISENxA, ISENxB		BAT12 ±0.2	V
ISN_FLY, ISP_FLY Common-Mode Voltage	0	0.5	V
ISN_FLY to ISP_FLY Differential Voltage	0	0.15	V
Operational Ambient Temperature Range (Automotive)	-40	+125	°C

2.4 Electrical Specifications

Refer to the Block Diagram (Figures 6 and 7) and Typical Application Schematics (Figure 3 on page 2). Operating conditions unless otherwise noted: V_{VIN} = 48V, V_{V6} = 6V, V_{V12} = 12V, V_{BAT12} = 12V, V_{PVCC} = 5.2V, V_{VCC} = 5.2V, V_{EN} = 5.0V, and T_A = -40°C to +125°C. Typicals are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +125°C.**

Parameter	Symbol	Test Conditions	Min (Note 8)	Typ	Max (Note 8)	Unit
Supply Input						
Input Voltage Range for V_{IN}	V_{VIN}		**6**	48	**64**	V
V_{IN} UVLO Threshold (VIN_POR Lower Threshold)	V_{UVLO_VIN}	EN = 5V, V_{IN} rising	**4.5**	5	**5.5**	V
V_{IN} UVLO Hysteresis	$V_{HYS\_VIN-UVLO}$	Falling from V_{UVLO_VIN}		0.5		V
V_{IN} Supply Current (Shutdown Mode)	$I_{Q\_SD\_VIN}$	EN = GND		0.1	**1**	µA
V_{IN} Supply Current after V6 Startup (Normal Mode)	I_{Q_VIN}			200	**300**	µA
Input Voltage Range for BAT12	V_{BAT12}		**6**		**40**	V
BAT12 UVLO Threshold	V_{UVLO_BAT12}	EN = 5V, V_{BAT12} rising	**3.00**	3.50	**4.05**	V
BAT12 UVLO Hysteresis	$V_{HYS\_BAT12-UVLO}$	Falling from V_{UVLO_BAT12}		260		mV
Input Leakage Current at ISENxA, ISENxB Pins (Shutdown Mode)	$I_{Q\_ISENxA/B}$	EN = GND, ISENxA = ISENxB =12V	**-1**	0	**1**	µA
Backup Linear Regulator (Backup LDO)						
Backup LDO Output Voltage (PVCC Pin)	$V_{BKUPLDO}$	V_{VIN} = 6V to 64V, V6 = Floating, EN = 5V, C_{PVCC} = 4.7µF from PVCC to PGND, I_{PVCC} = 10mA	**4.75**	5.00	**5.25**	V
Backup LDO Dropout Voltage (PVCC Pin)	$V_{DO\_BKUPLDO}$	V_{VIN} = 5.3V (after startup), V6 = Floating, C_{PVCC} = 4.7µF from PVCC to PGND, I_{VCC} = 10mA		0.25		V
Backup LDO Load Regulation (PVCC Pin)	$dV_{BKUPLDO}/dI_{O\_BKUPLDO}$	V_{V6} = Floating, EN = 5V, C_{PVCC} = 4.7µF from PVCC to AGND, IO_{PVCC} = 1mA to 100mA		0.1	**0.5**	%
Backup LDO Line Regulation (PVCC Pin)	$dV_{BKUPLDO}/dV_{V6}$	V_{VIN} = 5.5V to 64V, EN = 5V, V_{V6} = Floating, C_{PVCC} = 4.7µF from PVCC to AGND		0.2	**0.3**	%
Backup LDO Current Limit (PVCC Pin)	$I_{OC\_BKUPLDO}$	V_{VIN} = 6V, V_{V6} = Floating, C_{PVCC} = 4.7µF from PVCC to AGND, V_{PVCC} = 4.5V	**105**	180	**220**	mA
Backup LDO Output Short Current (PVCC Pin)	I_{OS_PVCC}	V_{VIN} = 6V, V_{V6} = Floating, C_{PVCC} = 4.7µF from PVCC to AGND, V_{PVCC} = 0V		90		mA

Refer to the Block Diagram (Figures 6 and 7) and Typical Application Schematics (Figure 3 on page 2). Operating conditions unless otherwise noted: V_{VIN} = 48V, V_{V6} = 6V, V_{V12} = 12V, V_{BAT12} = 12V, V_{PVCC} = 5.2V, V_{VCC} = 5.2V, V_{EN} = 5.0V, and T_A = -40°C to +125°C. Typicals are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +125°C. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 8)	Typ	Max (Note 8)	Unit
Internal Linear Regulator (Internal LDO)						
Internal LDO Output Voltage at PVCC Pin	V_{PVCC}	EN = 5V, C_{PVCC} = 4.7µF from AVCC to PGND, I_{PVCC} = 100mA	**4.94**	5.2	**5.46**	V
Internal LDO Dropout Voltage at PVCC Pin	V_{DO_PVCC}	V_{V6} = 5.5V, C_{PVCC} = 4.7µF from PVCC to AGND, I_{PVCC} = 100mA		0.4		V
Internal LDO Load Regulation at PVCC Pin	dV_{PVCC}/dI_{O_PVCC}	EN = 5V, C_{PVCC} = 4.7µF from PVCC to AGND, IO_{PVCC} = 1mA to 100mA		0.1	**0.5**	%
Internal LDO Line Regulation at PVCC Pin	dV_{PVCC}/dV_{V6}	V_{V6} = 5.7V to 12V, EN = 5V, C_{PVCC} = 4.7µF from PVCC to AGND, 100mA load		0.4	**1.0**	%
Internal LDO Current Limit at PVCC Pin	I_{OC_PVCC}	C_{PVCC} = 4.7µF from PVCC to AGND V_{PVCC} = 4.2V		200		mA
MCU Linear Regulator (MCULDO)						
MCULDO_FB Pin Voltage (MCULDO Output Voltage Accuracy)	V_{MCULDO_FB}	EN = 5V, C_{MCULDO} = 10µF from MCULDO to GND, I_{MCULDO} = 200mA	**1.14**	1.20	**1.26**	V
MCULDO Output Dropout Voltage	V_{DO_MCULDO}	V_{V6} = 5.2V, EN = 5V, setup of V_{MCULDO} = 5V, C_{MCULDO} = 10µF from MCULDO to AGND, no load		185		mV
MCULDO Output Load Regulation	$LDREG_{MCULDO}$	EN = 5V, Setup of V_{MCULDO} = 5V, C_{MCULDO} = 10µF from MCULDO to AGND, IO_{MCULDO} = 1mA to 200mA		0.1	**0.5**	%
MCULDO Output Line Regulation	$LINE\_REG_{MCULDO}$	V_{V6} = 5.5V to 12V, EN = 5V, setup of V_{MCULDO} = 5V, C_{MCULDO} = 10µF from MCULDO to AGND		0.1	**0.5**	%
MCULDO Output Current Limit	I_{OCL_MCULDO}	EN = 5V, C_{MCULDO} = 10µF, V_{MCULDO} = target - 1.0V		250		mA
MCULDO Power-Good Upper Limit at MCULDO_FB Pin	V_{PGH_MCULDO}	C_{MCULDO} = 10µF from MCULDO to AGND, V_{PVCC} = 0V	**1.26**	1.3	**1.34**	V
MCULDO Power-Good Hysteresis at MCULDO_FB Pin	V_{PGL_MCULDO}	C_{MCULDO} = 10µF from MCULDO to AGND, V_{PVCC} = 0V		40		mV
MCULDO Power-Good Lower Limit at MCULDO_FB Pin	V_{PGL_MCULDO}	C_{MCULDO} = 10µF from MCULDO to AGND, V_{PVCC} = 0V	**1.075**	1.100	**1.125**	V
PG_MCULDO Leakage Current	$I_{LK\_PGMCULDO}$	Forced output voltage at pins (XSTAT_FLAG, XHIC-LAT_F, XSYS_FAIL) = 5V			**1**	µA
PG_MCULDO Low Level Output Voltage	V_{OL_FAULTS}	Output sink current at PG_MCULDO = 3mA		0.1	**0.5**	V
V_{CC} Power-On Reset (VCC_POR)						
V_{CC} Power-On Reset Threshold (Rising)	V_{POR_VCC-R}		**4.35**	4.5	**4.75**	V
V_{CC} Power-On Reset Threshold (Falling)	V_{POR_VCC-F}		**4.05**	4.15	**4.25**	V
V_{CC} POR Hysteresis	$V_{POR\_VCC-HYS}$			0.4		V

Refer to the Block Diagram (Figures 6 and 7) and Typical Application Schematics (Figure 3 on page 2). Operating conditions unless otherwise noted: V_{VIN} = 48V, V_{V6} = 6V, V_{V12} = 12V, V_{BAT12} = 12V, V_{PVCC} = 5.2V, V_{VCC} = 5.2V, V_{EN} = 5.0V, and T_A = -40°C to +125°C. Typicals are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +125°C. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 8)	Typ	Max (Note 8)	Unit
EN						
Enable Threshold	V_{TH_EN-R}	Rising	**1.1**	1.2	**1.4**	V
	V_{TH_EN-F}	Falling	**0.85**	0.95	**1.10**	V
	V_{TH_EN-HYS}	Hysteresis		250		mV
Clock Generator (FSYNC, PLL_COMP, CLKOUT Pin)						
FSYNC Voltage	V_{FSYNC}	R_{FSYNC} = 46.4kΩ (0.1%) from FSYNC to AGND		500		mV
PWM Switching Frequency	f_{CLK}	R_{FSYNC} = 46.4kΩ (0.1%) from FSYNC to AGND	**93**	100	**107**	kHz
Minimum Adjustable Switching Frequency	$f_{CLK-Range}$	T_A = +25°C		40		kHz
Maximum Adjustable Switching Frequency	$f_{CLK-Range}$	T_A = +25°C		750		kHz
Minimum Synchronization Frequency with External Clock at FSYNC	$f_{SYNC-IN}$	T_A = +25°C		40		kHz
Maximum Synchronization Frequency with External Clock at FSYNC	$f_{SYNC-IN}$	T_A = +25°C		750		kHz
Phase Lock Loop Locking Time	t_{PLL_DLY}	From POR to initiation of soft-start. R_{PLLCMP} = 3.24k, $C_{PLLCMP1}$ = 6.8nF, $C_{PLLCMP2}$ = 6.8nF, R_{FSYNC} = 14.9k, f_{SW} = 300kHz		800		µs
High Level CLKOUT Output Voltage	$CLKOUT_H$	I_{CLKOUT} = -500µA	**V_{CC} - 0.5**	V_{CC} - 0.1		V
Low Level CLKOUT Output Voltage	$CLKOUT_L$	I_{CLKOUT} = 500µA		0.1	**0.5**	V
Output Pulse Width				$1/(12*f_{CLK})$		s
Phase Shift from PWM-1 Rising Edge to CLKOUT Pulse Rising Edge		PWM - 1 = Open		0		°
Synchronization (FSYNC Pin)						
Input High-Level Threshold	V_{IH_FSYNC}		**3.5**			V
Input Low-Level Threshold	V_{IL_FSYNC}				**1.5**	V
Input Minimum Pulse Width (Low Level)	t_{wL_FSYNC}		**20**			ns
Input Minimum Pulse Width (High Level)	t_{wH_FSYNC}		**20**			ns
Delay from Input Pulse Rising to PWM-1 Output Rising Edge	$t_{dCK-PWM0}$	PWM -1 = Open, Master mode		25		ns
Input Impedance	Z_{IN_FSYNC}			2		kΩ
Reference Voltage						
Reference Accuracy	V_{REF_FB}	Measured at FB_BK pin in Buck mode or FB_BT pin in Boost mode	**1.576**	1.6	**1.620**	V
FB Pin Input Bias Current	I_{IN_FB}	V_{FB} = 1.6V, V_{TRACK} = Open	**-0.05**		**0.05**	µA

Refer to the Block Diagram (Figures 6 and 7) and Typical Application Schematics (Figure 3 on page 2). Operating conditions unless otherwise noted: V_{VIN} = 48V, V_{V6} = 6V, V_{V12} = 12V, V_{BAT12} = 12V, V_{PVCC} = 5.2V, V_{VCC} = 5.2V, V_{EN} = 5.0V, and T_A = -40°C to +125°C. Typicals are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +125°C. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 8)	Typ	Max (Note 8)	Unit
Flyback Controller						
Flyback Error Amplifier Transconductance Gain	Gm_{EA_FLY}			2		mS
COMP_FLY Output Impedance	$Z_{O\_EA\_FLY}$			7.5		MΩ
Flyback Error Amplifier Unity Gain Bandwidth	f_{BW_FLY}	C_{CMP_FLY} = 100pF from COMP_FLY pin to GND		3.3		MHz
Flyback Error Amplifier Slew Rate	SL_{EA_FLY}	C_{CMP}_FLY = 100pF from COMP_FLY pin to GND		±3		V/µs
COMP_FLY Output Current Capability	$I_{O\_EA\_FLY}$			±300		µA
Maximum COMP_FLY Output Voltage	$V_{CLMP\_EA\_FLY}$		**3.7**	3.9	**4.1**	V
Minimum COMP_FLY Output Voltage	$V_{OMIN\_EA\_FLY}$				**0.3**	V
Flyback Controller Soft-Start Current	I_{SS_FLY}	V_{SS_FLY} = 0V	**4.7**	5.2	**5.7**	µA
Flyback Controller Soft-Start Prebias Voltage Accuracy	$V_{SS\_FLY\_PRE-ACC}$	$V_{SS\_FLY\_PRE}$ = 0.5V, measured at SS_FLY pin	**-5**		**5**	%
Flyback Controller Soft-Start Clamp Voltage	$V_{SS\_CLMP\_FLY}$			3.4		V
SLOPE_FLY Pin Bias Voltage	V_{SLOP_FLY}	R_{SLOP_FLY} = 20kΩ from SLOPE_FLY to AGND	**480**	500	**520**	mV
Flyback Controller Slope Accuracy		R_{SLOP_FLY} = 20kΩ (0.1%)	**-25**		**25**	%
Flyback Controller Primary Side Overcurrent Limit Threshold	$V_{OC\_IS\_FLY}$	Voltage differences between ISN_FLY to ISP_FLY	**50**	75	**90**	mV
Low Level GDRV_FLY Output Voltage	$V_{OL\_GDRVFLY}$	$I_{O\_GDRVFLY}$ = 10mA		0.1	**0.5**	V
High Level GDRV_FLY Output Voltage	$V_{OH\_GDRVFLY}$	$I_{O\_GDRVFLY}$ = -10mA	**V12 - 0.5**	V12 - 0.1		V
Minimum On-Time of Flyback Gate Driver	$t_{ONMIN\_GDRV\_FLY}$	GDRV_FLY = Open		100		ns
Maximum On Duty of Flyback Gate Driver	$t_{OFFMIN\_GDRV\_FLY}$	GDRV_FLY = Open, percentage of the PWM clock cycle time. Control Register 0xBF[2:0] = 000		91.7		%
V6 and V12 Pins						
Input Voltage Range of V6	V_{V6}		**5.5**	6	**11**	V
Input Supply Current at V6 (Shutdown Mode)	$I_{Q\_SD\_V6}$	V_{V6} = 6V, EN = GND		0.1	**5**	µA
Input Supply Current at V6 (Normal Mode)	I_{Q_V6}	MCULDO = Open, flyback switching frequency = 500kHz, C_{GDRV_FLY} = 5nF, MCULDO load = 0A, f_{SW} = 500kHz, PWMx = Open		20	**40**	mA

Refer to the Block Diagram (Figures 6 and 7) and Typical Application Schematics (Figure 3 on page 2). Operating conditions unless otherwise noted: V_{VIN} = 48V, V_{V6} = 6V, V_{V12} = 12V, V_{BAT12} = 12V, V_{PVCC} = 5.2V, V_{VCC} = 5.2V, V_{EN} = 5.0V, and T_A = -40°C to +125°C. Typicals are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +125°C. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 8)	Typ	Max (Note 8)	Unit
V6 Undervoltage Fault Threshold (Rising)	V_{TH_V6UV-R}		**4.66**	4.90	**5.14**	V
V6 Undervoltage Fault Threshold (Falling)	V_{TH_V6UV-F}		**4.50**	4.80	**5.04**	V
V6 Undervoltage Fault Threshold Hysteresis	$V_{TH\_V6UV-HYS}$			150		mV
V6 Overvoltage Fault Threshold (Rising)	V_{TH_V6OV-R}		**11.4**	12	**12.6**	V
V6 Overvoltage Fault Threshold (Falling)	V_{TH_V6OV-F}		**11.3**	11.9	**12.5**	V
V6 Overvoltage Fault Threshold Hysteresis	$V_{TH\_V6OVHYS}$			150		mV
Input Voltage Range of V12	V_{V12}		**9**	12	**15**	V
Input Supply Current at V12 (Shutdown Mode)	$I_{Q\_SD\_V12}$	EN = GND		0.3	**5**	µA
Input Supply Current at V12 (Normal Mode)	I_{Q_V12}	Flyback switching frequency = 500kHz, C_{GDRV_FLY} = 5nF		35	**50**	mA
V12 Undervoltage Fault Threshold (Rising)	$V_{TH\_V12UV-R}$		**8.65**	9.10	**9.55**	V
V12 Undervoltage Fault Threshold (Falling)	$V_{TH\_V12UV-F}$		**8.55**	9	**9.45**	V
V12 Undervoltage Fault Threshold Hysteresis	$V_{TH\_V12UV-HYS}$			100		mV
V12 Overvoltage Fault Threshold (Rising)	$V_{TH\_V12OV-R}$		**14.82**	15.60	**16.38**	V
V12 Overvoltage Fault Threshold (Falling)	$V_{TH\_V12OV-F}$		**14.72**	15.50	**16.28**	V
V12 Overvoltage Fault Threshold Hysteresis	$V_{TH\_V12OVHYS}$			100		mV
Track Pin - Analog Input (When Analog Track Input is Selected by Control Register Setting: 0X00[4] = 1)						
TRACK Pin Analog Input Voltage Range	V_{TRK-A}	In prebias output condition; $V_{SS\_PRE} = V_{FB}$	**0**		**1.6**	V
TRACK Pin Input Bias Current	I_{IN_TRK-A}	V_{TRK} = 1.5V	**-1**	-0.5	**-0.3**	µA
TRACK Input Reference Voltage Accuracy	V_{TRK_ACC-A}	V_{TRK} = 1.5V, measured at FB_BK pin (Buck mode) or FB_BT pin (Boost mode)	**-1.5**		**0.5**	%
		V_{TRK} = 0.85V, measured at FB_BK pin (Buck mode) or FB_BT pin (Boost mode)	**-0.5**		**1.5**	%
Track Pin - Digital Input						
TRACK Pin Low Level Logic Input Voltage	V_{IL_TRK-D}				**0.8**	V
TRACK Pin High Level Logic Input Voltage	V_{IH_TRK-D}		**2**			V

Refer to the Block Diagram (Figures 6 and 7) and Typical Application Schematics (Figure 3 on page 2). Operating conditions unless otherwise noted: V_{VIN} = 48V, V_{V6} = 6V, V_{V12} = 12V, V_{BAT12} = 12V, V_{PVCC} = 5.2V, V_{VCC} = 5.2V, V_{EN} = 5.0V, and T_A = -40°C to +125°C. Typicals are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +125°C. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 8)	Typ	Max (Note 8)	Unit
TRACK Pin Input Leakage Current	I_{IN-off_TRK-D}	EN = 0V, V_{IN_TRK} = 5V	**-1**	0	**1**	µA
TRACK Pin Input Pull-Up Current	I_{IN_TRK-D}	EN = V_{CC}, V_{IN_TRK} = 0V	**0.80**	1.25	**1.70**	µA
TRACK Pin Input Pull-Up Compliance	I_{IN_TRK-D}	EN = V_{CC}, Track pin = Open		2.5		V
Duty Cycle Conversion (FB Accuracy)	V_{TRK_ACC-D}	35% Duty cycle input. Track input frequency = 200kHz, measured at FB_BK pin (Buck mode) or FB_BT pin (Boost mode)	**0.869**	0.887	**0.904**	V
		50% Duty cycle input. Track input frequency = 200kHz, measured at FB_BK pin (Buck mode) or FB_BT pin (Boost mode)	**1.237**	1.263	**1.288**	V
		60% Duty cycle input, Track input frequency = 200kHz, measured at FB_BK pin (Buck mode) or FB_BT pin (Boost mode)	**1.45**	1.495	**1.53**	V
Soft-Start						
Soft-Start Current	I_{SS}	V_{SS} = 0V	**4.5**	5	**5.5**	µA
Soft-Start Prebias Voltage Accuracy	$V_{SS\_PRE-ACC}$	V_{SS_PRE} = 0.5V, measured at FB_BK pin (Buck mode) or FB_BT pin (Boost mode)	**-5**		**5**	%
Soft-Start Clamp Voltage	V_{SS_CLAMP}		**3**	3.4	**3.8**	V
Error Amplifier						
Transconductance Gain	Gm_{EA}			0.3		mS
COMP Output Impedance	Z_{O_EA}			7.5		MΩ
Unity Gain Bandwidth	f_{BW}	C_{CMP} = 100pF from COMP pin to GND		3.3		MHz
Slew Rate	SL_{EA}	C_{CMP} = 100pF from COMP pin to GND		±3		V/µs
COMP Output Current Capability	I_{O_EA}			±300		µA
COMP Output Voltage High	V_{CLMP_EA}		**3.5**	3.7		V
COMP Output Voltage Low	V_{OMIN_EA}				**0.3**	V
Slope Compensation						
SLOPE Pin Bias Voltage	V_{SLOPE}	R_{SLP_BK} or R_{SLP_BT} = 20kΩ (0.1%)	**480**	500	**520**	mV
SLOPE Accuracy		R_{SLP_BK} or R_{SLP_BT} = 40.2kΩ (0.1%)	**-25**		**25**	%
Current-Sense Amplifier/Current Monitoring						
ISENxA, ISENxB Offset Current	I_{OFST_ISENx}	Sinking into pin, EN = 5V, R_{SETxA} = R_{SETxB} = 998Ω (0.1%), V_{ISENxA} = V_{ISENxB} = 3.15V to V_{BAT12}		56		µA

Refer to the Block Diagram (Figures 6 and 7) and Typical Application Schematics (Figure 3 on page 2). Operating conditions unless otherwise noted: V_{VIN} = 48V, V_{V6} = 6V, V_{V12} = 12V, V_{BAT12} = 12V, V_{PVCC} = 5.2V, V_{VCC} = 5.2V, V_{EN} = 5.0V, and T_A = -40°C to +125°C. Typicals are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +125°C. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 8)	Typ	Max (Note 8)	Unit
ISET Output Current	I_{ISET}	4-phase, R_{SETxA} = R_{SETxB} = 998Ω (0.1%), V_{ISENxB} - V_{ISENxA} = 20mV, V_{ISENxA} = V_{BAT12}		152		µA
		4-phase, R_{SETxA} = R_{SETxB} = 998Ω (0.1%), V_{ISENxB} - V_{ISENxA} = 30mV, V_{ISENxA} = V_{BAT12}		172		µA
		4-phase, R_{SETxA} = R_{SETxB} = 998Ω (0.1%), V_{ISENxB} - V_{ISENxA} = 0mV, V_{ISENxA} = V_{BAT12}		112		µA
		4-phase, R_{SETxA} = R_{SETxB} = 998Ω (0.1%), V_{ISENxB} - V_{ISENxA} = -30mV, V_{ISENxA} = V_{BAT12}		52		µA
ISHARE Output Current	I_{ISHARE}	4-phase, R_{SETxA} = R_{SETxB} = 998Ω (0.1%), V_{ISENxB} - V_{ISENxA} = 20mV, V_{ISENxA} = V_{BAT12}		152		µA
		4-phase, R_{SETxA} = R_{SETxB} = 998Ω (0.1%), V_{ISENxB} - V_{ISENxA} = 30mV, V_{ISENxA} = V_{BAT12}		172		µA
		4-phase, R_{SETxA} = R_{SETxB} = 998Ω (0.1%), V_{ISENxB} - V_{ISENxA} = 0mV, V_{ISENxA} = V_{BAT12}		112		µA
		4-phase, R_{SETxA} = R_{SETxB} = 998Ω (0.1%), V_{ISENxB} - V_{ISENxA} = -30mV, V_{ISENxA} = V_{BAT12}		52		µA
Current Matching between ISET and ISHARE (within Same Chip)		4-phase, R_{SETxA} = R_{SETxB} = 998Ω (0.1%), V_{ISENxB} - V_{ISENxA} = -30mV ~ +30mV, V_{ISENxA} = V_{BAT12}	**-3**		**3**	µA
IMON Output Current (Buck Mode)	I_{IMON_BK}	4-phase, R_{SETxA} = R_{SETxB} = 998Ω (0.1%), V_{ISENxB} - V_{ISENxA} = 30mV, V_{ISENxA} = V_{BAT12}, R_{IMON} = 10.56kΩ	**251**	258	**269**	µA
		4-phase, R_{SETxA} = R_{SETxB} = 998Ω (0.1%), V_{ISENxB} - V_{ISENxA} = 20mV, V_{ISENxA} = V_{BAT12}, R_{IMON} = 10.56kΩ, V_{IN} = 48V, BAT48 = 48V, BAT12 = 12V, T_A = +25°C	224.5	228.5	232.2	µA
		4-phase, R_{SETxA} = R_{SETxB} = 998Ω (0.1%), V_{ISENxB} - V_{ISENxA} = 20mV, V_{ISENxA} = V_{BAT12}, R_{IMON} = 10.56kΩ	**221**	228.5	**238**	µA
		4-phase, R_{SETxA} = R_{SETxB} = 998Ω (0.1%), V_{ISENxB} - V_{ISENxA} = 0mV, V_{ISENxA} = V_{BAT12}, R_{IMON} = 10.56kΩ	**160**	168	**178**	µA
		4-phase, R_{SETxA} = R_{SETxB} = 998Ω (0.1%), V_{ISENxB} - V_{ISENxA} = -30mV, V_{ISENxA} = V_{BAT12}	**70**	78	**88**	µA
IMON Gain 20mV	IMON_Gain_ 20mV_BK	(IMON_BK (20mV) - IMON_BK (0mV))/20mV 4-phase, R_{SETxA} = R_{SETxB} = 998Ω (0.1%)	**2.975**	3.03	**3.09**	µA/mV

Refer to the Block Diagram (Figures 6 and 7) and Typical Application Schematics (Figure 3 on page 2). Operating conditions unless otherwise noted: V_{VIN} = 48V, V_{V6} = 6V, V_{V12} = 12V, V_{BAT12} = 12V, V_{PVCC} = 5.2V, V_{VCC} = 5.2V, V_{EN} = 5.0V, and T_A = -40°C to +125°C. Typicals are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +125°C. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 8)	Typ	Max (Note 8)	Unit
IMON Gain 30mV	IMON_Gain_30mV_BK	(IMON_BK (30mV) - IMON_BK (0mV))/30mV 4-phase, R_{SETxA} = R_{SETxB} = 998Ω (0.1%)	**2.975**	3.03	**3.09**	µA/mV
IMON Output Current (Boost Mode)	I_{IMON_BT}	4-phase, R_{SETxA} = R_{SETxB} = 998Ω (0.1%), V_{ISENxA} - V_{ISENxB} = 30mV, V_{ISENxA} = V_{BAT12}, R_{IMON} = 10.56kΩ	**243.5**	258	**263.5**	µA
		4-phase, R_{SETxA} = R_{SETxB} = 998Ω (0.1%), V_{ISENxA} - V_{ISENxB} = 20mV, V_{ISENxA} = V_{BAT12}, R_{IMON} = 10.56kΩ, V_{IN} = 48V, BAT48 = 48V, BAT12 = 12V, T_A = +25°C	222.5	228.5	232	µA
		4-phase, R_{SETxA} = R_{SETxB} = 998Ω (0.1%), V_{ISENxA} - V_{ISENxB} = 20mV, V_{ISENxA} = V_{BAT12}, R_{IMON} = 10.56kΩ, V_{IN} = 48V, BAT48 = 48V, BAT12 = 12V	**213.5**	228.5	**234**	µA
		4-phase, R_{SETxA} = R_{SETxB} = 998Ω (0.1%), V_{ISENxA} - V_{ISENxB} = 0mV, V_{ISENxA} = V_{BAT12}, R_{IMON} = 10.56kΩ	**153.5**	168	**173**	µA
		4-phase, R_{SETxA} = R_{SETxB} = 998Ω (0.1%), V_{ISENxA} - V_{ISENxB} = -30mV, V_{ISENxA} = V_{BAT12}	**62.5**	78	**83.1**	µA
IMON Gain 20mV	IMON_Gain_20mV_BT	(IMON_BT (20mV) - IMON_BT (0mV))/20mV 4-phase, R_{SETxA} = R_{SETxB} = 998Ω (0.1%)	2.92	3	3.09	µA/mV
IMON Gain 30mV	IMON_Gain_30mV_BT	(IMON_BT (30mV) - IMON_BT (0mV))/30mV 4-phase, R_{SETxA} = R_{SETxB} = 998Ω (0.1%)	2.92	3	3.09	µA/mV
Zero Crossing Detection						
Sense Current Zero Crossing Detection (ZCD) Threshold	V_{TH_ZCD}	Voltage differences at current-sense resistor (V_{ISENxB} - V_{ISENxA}), V_{ISENxA} = V_{BAT12} R_{SETxA} = R_{SETxB} = 998Ω (0.1%)		1		mV
Overcurrent Protection						
Cycle-by-Cycle Peak Current Limit (OC1) Threshold for individual Phases (Buck mode)	V_{OC1}	Defined by voltage differences at current-sense resistor (V_{ISENxB} - V_{ISENxA}), Buck mode, V_{ISENxA} = V_{BAT12}, R_{SETxA} = R_{SETxB} = 998Ω (0.1%)	**26**	38	**48.5**	mV
Cycle-by-Cycle Peak Current Limit (OC1) Threshold for Individual Phases (Boost mode)	V_{OC1}	Defined by voltage differences at current-sense resistor (V_{ISENxA} - V_{ISENxB}), Boost mode, V_{ISENxA} = V_{BAT12}, R_{SETxA} = R_{SETxB} = 998Ω (0.1%)	**27**	38	**49**	mV
Cycle-by-Cycle Peak Current Limit (OC1) Delay	t_{d_OC1}	PWMx = Open, Buck mode, from V_{OC1-BK} detection at PWMx to PWMx falling		50		ns

Refer to the Block Diagram (Figures 6 and 7) and Typical Application Schematics (Figure 3 on page 2). Operating conditions unless otherwise noted: V_{VIN} = 48V, V_{V6} = 6V, V_{V12} = 12V, V_{BAT12} = 12V, V_{PVCC} = 5.2V, V_{VCC} = 5.2V, V_{EN} = 5.0V, and T_A = -40°C to +125°C. Typicals are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +125°C. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 8)	Typ	Max (Note 8)	Unit
Cycle-by-Cycle Peak Current Limit (OC1) to XSTAT_FLAG Fault Flag Delay	$t_{d\_OC1-FAULT}$	PWMx = Open, Buck or Boost mode, from V_{OC1-BK} or V_{OC1-BT} detection at PWMx to XSTAT_VFLAG Falling		50		ns
Peak Current Hiccup/Latch-Off Protection (OC2) Threshold for Individual Phases (Buck mode)	V_{OC2}	Defined by voltage differences at current-sense resistor (V_{ISENxB} - V_{ISENxA}), Buck mode, V_{ISENxA} = V_{BAT12}, R_{SETxA} = R_{SETxB} = 998Ω (0.1%)	**30**	45	**55**	mV
Peak Current Hiccup/Latch-Off Protection (OC2) Threshold for Individual Phases (Boost mode)	V_{OC2}	Defined by voltage differences at current-sense resistor (V_{ISENxA} - V_{ISENxB}), Boost mode, V_{ISENxA} = V_{BAT12}, R_{SETxA} = R_{SETxB} = 998Ω (0.1%)	**33**	45	**57**	mV
OC2 Hiccup/Latch-Off Blanking Time	t_{d_OC2}	Consecutive OC2 detection switching cycles		3		Switching cycles
OC2 Hiccup Retry Delay	$t_{d\_OC2-Retry}$	In Hiccup mode, OC2 detection to next soft-start starting		500		ms
OC2 Hiccup/Latch-Off Fault Detection to XHICLAT_F and XSTAT_FLAG Fault Flag Delay	$t_{d\_OC2-FAULT}$	PWMx = Open, Buck, or Boost mode from V_{OC2-BK} or V_{OC2-BT} detection at PWMx to PWMx stopping, XHICLAT_F and XSTAT_FLAG falling		50		ns
High-Side Transistor Short Detection in Buck Mode, or Low-Side Transistor Short Detection in Boost Mode for XSYS_FAIL Falling	$t_{d\_OC2\_Short}$	Continuous OC2 condition duration after the OC2 hiccup/latch-off triggered		3		Switching cycles
Cycle-by-Cycle Negative Peak Current Limit (NOC) Threshold for Individual Phases (Buck Mode)	V_{NOC}	Defined by voltage differences at current-sense resistor (V_{ISENxB} - V_{ISENxA}), Buck mode, V_{ISENxA} = V_{BAT12}, R_{SETxA} = R_{SETxB} = 998Ω (0.1%)	**-38**	-30	**-24**	mV
Cycle-by-Cycle Negative Peak Current Limit (NOC) Threshold for Individual Phases (Boost mode)	V_{NOC}	Defined by Voltage differences at current-sense resistor (V_{ISENxA} - V_{ISENxB}), Boost mode, V_{ISENxA} = V_{BAT12}, R_{SETxA} = R_{SETxB} = 998Ω (0.1%)	**-39**	-30	**-25**	mV
Cycle-by-Cycle Negative Peak Current Limit (NOC) Delay	t_{d_NOC}	PWMx = Open, Buck mode, from V_{NOC-BK} detection at PWMx to PWMx rising and XSTAT_FLAG falling		50		ns
Cycle-by-Cycle Negative Peak Current Limit (NOC) Fault Flag Delay	$t_{d\_NOC-FAULT}$	PWMx = Open, Buck mode, from V_{NOC-BK} or V_{NOC-BT} detection at PWMx to XSTAT_FLAG falling		50		ns
Low-Side Transistor Short Detection in Buck Mode or High-Side Transistor Short Detection in Boost Mode for XSYS_FAIL Falling	t_{d_ONC}	Continuous negative overcurrent limit exceeding duration		3		Switching cycles

Refer to the Block Diagram (Figures 6 and 7) and Typical Application Schematics (Figure 3 on page 2). Operating conditions unless otherwise noted: V_{VIN} = 48V, V_{V6} = 6V, V_{V12} = 12V, V_{BAT12} = 12V, V_{PVCC} = 5.2V, V_{VCC} = 5.2V, V_{EN} = 5.0V, and T_A = -40°C to +125°C. Typicals are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +125°C. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 8)	Typ	Max (Note 8)	Unit
Average Overcurrent Protection and Constant Current Limiting Loop						
Average Constant Current Limit (ACL) Reference Voltage	V_{ACL_REF}	IMON pin voltage while average constant current limiting is working 0xED[2,0] = 0,0,0	**2.33**	2.4	**2.47**	V
		0xED[2,0] = 0,0,1		2.3		V
		0xED[2,0] = 0,1,0		2.2		V
		0xED[2,0] = 0,1,1		2.1		V
		0xED[2,0] = 1,0,0		2.0		V
		0xED[2,0] = 1,0,1		1.9		V
		0xED[2,0] = 1,1,0		1.8		V
		0xED[2,0] = 1,1,1		1.7		V
Average Overcurrent Protection (AOCP) Hiccup/Latch-Off Fault Threshold at IMON pin (Buck Mode)	V_{TH_AOCP}	Selected latch-off/hiccup response. 0xED[5,3] = 0,0,0	**2.57**	2.7	**2.83**	V
		0xED[5,3] = 0,0,1		2.6		V
		0xED[5,3] = 0,1,0		2.5		V
		0xED[5,3] = 0,1,1		2.4		V
		0xED[5,3] = 1,0,0		2.3		V
		0xED[5,3] = 1,0,1		2.2		V
		0xED[5,3] = 1,1,0		2.1		V
		0xED[5,3] = 1,1,1		2.0		V
Hiccup Retry Delay when Average Overcurrent Protection Detected	td_AOCP-Retry	In Hiccup mode, AOCP detection to next soft-start starting		500		ms
Master/Slave Setting						
ADDR Output Current (Initialization Period Only)	I_{O_ADDR}	Initialization period only, ADDR pin voltage = 0V	**26**	30	**34**	µA
Recommended Resistor Value for Master Mode at ADDR Pin to GND	R_{ADDR_MSTR}			0		Ω
Recommended Resistor Value for Slave-1 Setting at ADDR Pin to VCC	R_{ADDR_SLV1}			0		Ω
Recommended Resistor Value for Slave-2 Mode at ADDR Pin to GND	R_{ADDR_SLV2}			33.2		kΩ
Recommended Resistor Value for Slave-3 Mode at ADDR Pin to GND	R_{ADDR_SLV3}			68.1		kΩ
DRV_EN						
Low-Level DRV_EN Output Voltage (Master Device Only)	V_{OL_DRVEN}	I_{O_DRVEN} = 1mA, ADDR = 0V		0.1	**0.5**	V
High-Level DRV_EN Output Voltage (Master Device Only)	V_{OH_DRVEN}	I_{O_DRVEN} = -1mA, ADDR = 0V	**V_{CC} - 0.5**	V_{CC} - 0.1		V

Refer to the Block Diagram (Figures 6 and 7) and Typical Application Schematics (Figure 3 on page 2). Operating conditions unless otherwise noted: V_{VIN} = 48V, V_{V6} = 6V, V_{V12} = 12V, V_{BAT12} = 12V, V_{PVCC} = 5.2V, V_{VCC} = 5.2V, V_{EN} = 5.0V, and T_A = -40°C to +125°C. Typicals are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +125°C. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 8)	Typ	Max (Note 8)	Unit
Low-Level DRV_EN Input Voltage (Slave Device Only)	V_{IL_DRVEN}	ADDR = VCC	**0**		**0.8**	V
High-Level DRV_EN Input Voltage (Slave Device Only)	V_{IH_DRVEN}	ADDR = VCC	**V_{CC} - 0.8**		**V_{CC}**	V
PWMx Control/PWMx Output						
Low-Level PWMx Output Voltage	V_{OL_PWMx}	I_{O_PWMx} = 1mA		0.2	**0.5**	V
High-Level PWMx Output Voltage	V_{OH_PWMx}	I_{O_PWMx} = -1mA	**V_{CC} - 0.5**	V_{CC} - 0.2		V
Tri-State Level PWMx Output Voltage	V_{OTRI_PWMx}	I_{O_PWMx} = ±100µA	**2.3**	2.5	**2.7**	V
PWMx Pull-Down Current (Effective in Initialization Period Only)	I_{O_PWMx}	During Phase count detection period while in initialization, V_{PWMx} = 1.0V		50		µA
Minimum Low-Level PWMx Output Pulse Width (Boost Mode Default Minimum ON Time)	t_{WL-MIN}	PWMx = open		340		ns
Minimum High Level PWMx Output Pulse Width (Buck Mode Default Minimum ON Time)	t_{WH-MIN}	PWMx = open		340		ns
Maximum Low-Level PWMx Output Pulse Width (Boost Mode Default Maximum ON Duty)	$t_{ON-MAX-BT}$	PWMx = open		91.7		%
Maximum High-Level PWMx Output Pulse Width (Buck Mode Default Maximum ON Duty)	$t_{ON-MAX-BK}$	PWMx = open		91.7		%
PWM_TRI Low-Level Input Voltage	V_{IL_PWMTRI}		**0**		**0.8**	V
PWM_TRI High-Level Input Voltage	V_{IH_PWMTRI}		**2.1**		**V_{CC}**	V
Phase Dropping/Adding						
PD_CTRL Pin Pull-Up Current (Master Device Only)	I_{O_PDCTRL}	V_{PDCTRL} = 2V, ADDR = 0V (Master mode only)	**37.85**	40	**41.25**	µA
PD_CTRL Pin Voltage to Disable Phase Drop (Master Device Only)	$V_{TH\_PD-DISA}$	ADDR = 0V (Master mode)	**V_{CC} - 0.5**	V_{CC}		V
IMON Pin Voltage for Phase Adding from 4-Phase to 4-Phase in 4-Phase configuration (Master Device Only)	V_{TH_PD6-64}	V_{PDCTRL} = 2.35V, ADDR = 0V (Master mode)	**2.075**	2.10	**2.12**	V

Refer to the Block Diagram (Figures 6 and 7) and Typical Application Schematics (Figure 3 on page 2). Operating conditions unless otherwise noted: V_{VIN} = 48V, V_{V6} = 6V, V_{V12} = 12V, V_{BAT12} = 12V, V_{PVCC} = 5.2V, V_{VCC} = 5.2V, V_{EN} = 5.0V, and T_A = -40°C to +125°C. Typicals are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +125°C. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 8)	Typ	Max (Note 8)	Unit
IMON Pin Voltage for Phase Adding from 3-Phase to 4Phase in4Phase configuration (Master Device Only)	V_{TH_PD6-43}	V_{PDCTRL} = 2.35V, ADDR = 0V (Master mode)	**1.975**	2.00	**2.03**	V
IMON Pin Voltage for Phase Adding from 2-Phase to 3-Phase in 4-phase configuration (Master Device Only)	V_{TH_PD6-32}	V_{PDCTRL} = 2.35V, ADDR = 0V (Master mode)	**1.885**	1.91	**1.94**	V
IMON Pin Voltage for Phase Adding from 3-Phase to 4-Phase in 4-Phase configuration (Master Device Only)	V_{TH_PD4-43}	V_{PDCTRL} = 2.35V, ADDR = 0V (Master mode)	**2.075**	2.10	**2.13**	V
IMON Pin Voltage for Phase Adding from 2-Phase to 3-Phase in 4-Phase configuration (Master Device Only)	V_{TH_PD4-32}	V_{PDCTRL} = 2.35V, ADDR = 0V (Master mode)	**1.975**	2.01	**2.03**	V
IMON Pin Voltage for Phase Adding from 2-Phase to 3-Phase in 3-Phase configuration (Master Device Only)	V_{TH_PD3-32}	V_{PDCTRL} = 2.35V, ADDR = 0V (Master mode)	**2.055**	2.08	**2.11**	V
Phase Dropping Masking Time	t_{MASK_PD}	After IMON Voltage reached to phase-drop threshold		15		Cycle
IMON Pin Voltage Hysteresis from the Phase Adding Threshold to the Phase Dropping Threshold (Master Device Only)	V_{TH_PAD}	R_{PDCTRL} = 60kΩ from PD_CTRL pin to AGND, ADDR = 0V (Master mode), 4-phase, 4-phase and 3-phase configuration		40		mV
Phase Adding Delay Time	t_{d_PA}	After IMON Voltage reached to phase-add threshold		1		Switch Cycle
Instant All Phase Adding Threshold against the OC1 Current Level	I_{SEN_PAA}	Sensed peak current at any individual phases, V_{ISENxA} = V_{BAT12}, R_{SETxA} = R_{SETxB} = 998Ω (0.1%)		80		%
Instance All Phase Adding Delay Time	t_{d_PAA}	After PWMx sensed current reached at all phase adding threshold		1		Switch Cycle
High-Level PD_0 Output Voltage (Master Device Only)	$V_{OH\_PD\_0}$	$I_{OH\_PD\_0}$ = -100µA, ADDR = 0V (Master mode)	**4.5**	5.1		V
Middle-Level PD_0 Output Voltage (Master Device Only)	$V_{OM\_PD\_0}$	$I_{OM\_PD\_0}$ = ±100µA, ADDR = 0V (Master mode)	**2.25**	2.5	**2.75**	V
Low-Level PD_0 Output Voltage (Master Device Only)	$V_{OL\_PD\_0}$	$I_{OL\_PD\_0}$ = 100µA, ADDR = 0V (Master mode)		0.1	**0.5**	V
High-Level PD_1 Output Voltage (Master Device Only)	$V_{OH\_PD\_1}$	$I_{OH\_PD\_1}$ = -100µA, ADDR = 0V (Master mode)	**4.5**	5.1		V

Refer to the Block Diagram (Figures 6 and 7) and Typical Application Schematics (Figure 3 on page 2). Operating conditions unless otherwise noted: V_{VIN} = 48V, V_{V6} = 6V, V_{V12} = 12V, V_{BAT12} = 12V, V_{PVCC} = 5.2V, V_{VCC} = 5.2V, V_{EN} = 5.0V, and T_A = -40°C to +125°C. Typicals are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +125°C. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 8)	Typ	Max (Note 8)	Unit
Low-Level PD_1 Output Voltage (Master Device Only)	$V_{OL\_PD\_1}$	$I_{OL\_PD\_1}$ = 100µA, ADDR = 0V (Master mode)		0.1	**0.5**	V
High-Level PD_0 Input Voltage (Slave Device Only)	$V_{IH\_PD\_0}$	ADDR = V_{CC} (Slave mode)	**4.0**		**V_{CC}**	V
Middle-Level PD_0 Input Voltage (Slave Device Only)	$V_{IM\_PD\_0}$	ADDR = V_{CC} (Slave mode)	**2.15**		**2.85**	V
Low-Level PD_0 Input Voltage (Slave Device Only)	$V_{IL\_PD\_0}$	ADDR = V_{CC} (Slave mode)	**0**		**1**	V
High-Level PD_1 Input Voltage (Slave Device Only)	$V_{IH\_PD\_1}$	ADDR = V_{CC} (Slave mode)	**4.0**		**V_{CC}**	V
Low-Level PD_1 Input Voltage (Slave Device Only)	$V_{IL\_PD\_1}$	ADDR = V_{CC} (Slave mode)	**0**		**1**	V
BAT12 and BAT48 Overvoltage Detection and Protection						
BAT12 Overvoltage Fault Detection Threshold at FB_BK Pin. (Rising) (Percentage to the Internal Reference Voltage (1.6V))	V_{BAT12_OV}	Default setting: Individual Fault Response Control Register Bit (0xB0[7]) = 0, Internal Fault Flag setting and XSTAT_VLAG falling	**112**	115	**118**	%
		Register Setting: Individual Fault Response Control Register Bit (0xB0[7]) = 1, BAT12_Overvoltage Detection Control Register (0xB9[2:0]) = 000	**112**	115	**118**	%
		0xB0[7] = 1, 0xB9[2:0] = 001		110		%
		0xB0[7] = 1, 0xB9[2:0] = 010		120		%
		0xB0[7] = 1, 0xB9[2:0] = 011		125		%
		0xB0[7] = 1, 0xB9[2:0] = 100		130		%
		0xB0[7] = 1, 0xB9[2:0] = 101		135		%
		0xB0[7] = 1, 0xB9[2:0] = 110		140		%
		0xB0[7] = 1, 0xB9[2:0] = 111		145		%

Refer to the Block Diagram (Figures 6 and 7) and Typical Application Schematics (Figure 3 on page 2). Operating conditions unless otherwise noted: V_{VIN} = 48V, V_{V6} = 6V, V_{V12} = 12V, V_{BAT12} = 12V, V_{PVCC} = 5.2V, V_{VCC} = 5.2V, V_{EN} = 5.0V, and T_A = -40°C to +125°C. Typicals are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +125°C. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 8)	Typ	Max (Note 8)	Unit
BAT12 Overvoltage Protection Threshold at FB_BK Pin. (Rising) (Percentage to the Internal Reference Voltage (1.6V))	V_{BAT12_OVP}	Default setting: Individual Fault Response Control Register Bit (0xB0[7]) = 0, Internal fault bit setting, XSTAT_FLAG and XHIC_LAT_F falling, hiccup or latch-off response	**146**	150	**153**	%
		Register setting: Individual Fault Response Control Register Bit (0xB0[7]) = 1, BAT12_Overvoltage Limit Control Register (0xB9[5:3]) = 000	**146**	150	**153**	%
		0xB0[7] = 1, 0xB9[5:3] = 001		140		%
		0xB0[7] = 1, 0xB9[5:3] = 010		130		%
		0xB0[7] = 1, 0xB9[5:3] = 011		160		%
		0xB0[7] = 1, 0xB9[5:3] = 100		170		%
		0xB0[7] = 1, 0xB9[5:3] = 101		180		%
		0xB0[7] = 1, 0xB9[5:3] = 110		190		%
		0xB0[7] = 1, 0xB9[5:3] = 111		200		%
BAT48 Overvoltage Fault Detection Threshold at FB_BT Pin. (Rising) (Percentage to the Internal Reference Voltage (1.6V))	V_{BAT48_OV}	Default setting: Individual Fault Response Control Register Bit (0xB0[7]) = 0, Internal fault flag setting and XSTAT_VLAG falling	**105**	108	**111**	%
		Register Setting: Individual Fault Response Control Register Bit (0xB0[7]) = 1, BAT48_Overvoltage Detection Control Register (0xBB[2:0]) = 000	**105**	108	**111**	%
		0xB0[7] = 1, 0xBB[2:0] = 001		110		%
		0xB0[7] = 1, 0xBB[2:0] = 010		113		%
		0xB0[7] = 1, 0xBB[2:0] = 011		117		%
		0xB0[7] = 1, 0xBB[2:0] = 100		121		%
		0xB0[7] = 1, 0xBB[2:0] = 101		125		%
		0xB0[7] = 1, 0xBB[2:0] = 110		106		%
		0xB0[7] = 1, 0xBB[2:0] = 111		104		%

Refer to the Block Diagram (Figures 6 and 7) and Typical Application Schematics (Figure 3 on page 2). Operating conditions unless otherwise noted: V_{VIN} = 48V, V_{V6} = 6V, V_{V12} = 12V, V_{BAT12} = 12V, V_{PVCC} = 5.2V, V_{VCC} = 5.2V, V_{EN} = 5.0V, and T_A = -40°C to +125°C. Typicals are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +125°C. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 8)	Typ	Max (Note 8)	Unit
BAT48 Overvoltage Protection Threshold at FB_BT Pin. (Rising) (Percentage to the Internal Reference Voltage (1.6V))	V_{BAT48_OVP}	Default setting: Individual Fault Response Control Register Bit (0xB0[7]) = 0, Internal Fault bit setting, XSTAT_VLAG and XHIC_LAT_F falling, hiccup or latch-off response	**122**	125	**128**	%
		Register Setting: Individual Fault Response Control Register Bit (0xB0[7]) = 1, BAT48_Overvoltage Limit Control Register (0xBB[5:3]) = 000	**122**	125	**128**	%
		0xB0[7] = 1, 0xBB[5:3] = 001		129		%
		0xB0[7] = 1, 0xBB[5:3] = 010		133		%
		0xB0[7] = 1, 0xBB[5:3] = 011		138		%
		0xB0[7] = 1, 0xBB[5:3] = 100		142		%
		0xB0[7] = 1, 0xBB[5:3] = 101		146		%
		0xB0[7] = 1, 0xBB[5:3] = 110		150		%
		0xB0[7] = 1, 0xBB[5:3] = 111		121		%
BAT12/BAT48 Overvoltage Detection and Protection Threshold Hysteresis	V_{FBOV_HYS}			4		%
BAT12/BAT48 Overvoltage Detection and Protection Delay	t_{MASK_FBOV}	Overvoltage detection filter		1		µs
BAT12 and BAT48 Undervoltage Detection and Protection						
BAT12 Undervoltage Fault Detection Threshold at FB_BK Pin. (Falling) (Percentage to the Internal Reference Voltage (1.6V))	V_{BAT12_UV}	Default setting: Individual Fault Response Control Register Bit (0xB0[7]) = 0, Internal fault flag setting and XSTAT_VLAG falling	**82**	85	**88**	%
		Register setting: Individual Fault Response Control Register Bit (0xB0[7]) = 1, BAT12_Undervoltage Detection Control Register (0xBA[2:0]) = 000	**82**	85	**88**	%
		0xB0[7] = 1, 0xBA[2:0] = 001		82.5		%
		0xB0[7] = 1, 0xBA[2:0] = 010		80		%
		0xB0[7] = 1, 0xBA[2:0] = 011		77.5		%
		0xB0[7] = 1, 0xBA[2:0] = 100		75		%
		0xB0[7] = 1, 0xBA[2:0] = 101		72.5		%
		0xB0[7] = 1, 0xBA[2:0] = 110		87.5		%
		0xB0[7] = 1, 0xBA[2:0] = 111		90		%
BAT12 Undervoltage Protection Threshold at FB_BK Pin. (Rising) (Percentage to the Internal Reference Voltage (1.6V))	V_{BAT12_UVP}	Internal fault bit setting, XSTAT_VLAG and XHIC_LAT_F falling, hiccup or latch-off response	**37**	40	**43**	%

Refer to the Block Diagram (Figures 6 and 7) and Typical Application Schematics (Figure 3 on page 2). Operating conditions unless otherwise noted: V_{VIN} = 48V, V_{V6} = 6V, V_{V12} = 12V, V_{BAT12} = 12V, V_{PVCC} = 5.2V, V_{VCC} = 5.2V, V_{EN} = 5.0V, and T_A = -40°C to +125°C. Typicals are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +125°C. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 8)	Typ	Max (Note 8)	Unit
BAT48 Undervoltage Fault Detection Threshold at FB_BK Pin. (Falling) (Percentage to the Internal Reference Voltage (1.6V))	V_{BAT48_UV}	Default setting: Individual Fault Response Control Register Bit (0x00[7]) = 0, Internal Fault Flag setting and XSTAT_VLAG falling	**72**	75	**78**	%
		Register Setting: Individual Fault Response Control Register Bit (0xB0[7]) = 1, BAT48_Undervoltage Detection Control Register (0xBA[5:3]) = 000	**72**	75	**78**	%
		0xB0[7] = 1, 0xBA[5:3] = 001		71		%
		0xB0[7] = 1, 0xBA[5:3] = 010		67		%
		0xB0[7] = 1, 0xBA[5:3] = 011		63		%
		0xB0[7] = 1, 0xBA[5:3] = 100		58		%
		0xB0[7] = 1, 0xBA[5:3] = 101		54		%
		0xB0[7] = 1, 0xBA[5:3] = 110		79		%
		0xB0[7] = 1, 0xBA[5:3] = 111		83		%
BAT48 Undervoltage Protection Threshold at FB_BK Pin. (Falling) (Percentage to the Internal Reference Voltage (1.6V))	V_{BAT48_UVP}	Internal Fault bit setting, XSTAT_VLAG and XHIC_LAT_F falling, hiccup or latch-off response	**47**	50	**53**	%
BAT12/BAT48 Undervoltage Detection and Protection Threshold Hysteresis	V_{FBUV_HYS}			4		%
BAT12/BAT48 Undervoltage Detection and Protection Delay	t_{MASK_FBUV}	Undervoltage detection filter		1		µs
Switching Mode (DE Mode/Forced PWM Mode)/Fault Response (Hiccup/Latch-Off) Select						
MODE Pin Output Current (Initialization Period Only)	I_{O_MODE}	Initialization period only	**26**	30	**34**	µA
Recommended MODE Pin Setting Resistor Value from MODE pin to VCC Switching Mode = Forced PWM/Fault Response = Latch-Off	R_{MODE-0}	Mode pin to VCC		0		Ω
Recommended MODE Pin Setting Resistor Value from MODE pin to GND Switching Mode = DE/Fault Response = Latch-Off	R_{MODE-1}			68.1		kΩ
Recommended MODE Pin Setting Resistor Value from MODE pin to GND Switching Mode = Forced PWM/Fault Response = Hiccup	R_{MODE-2}			33.2		kΩ

Refer to the Block Diagram (Figures 6 and 7) and Typical Application Schematics (Figure 3 on page 2). Operating conditions unless otherwise noted: V_{VIN} = 48V, V_{V6} = 6V, V_{V12} = 12V, V_{BAT12} = 12V, V_{PVCC} = 5.2V, V_{VCC} = 5.2V, V_{EN} = 5.0V, and T_A = -40°C to +125°C. Typicals are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +125°C. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 8)	Typ	Max (Note 8)	Unit
Recommended MODE Pin Setting Resistor Value from MODE Pin to GND Switching Mode = DE/Fault Response = Hiccup	R_{MODE-3}	Mode pin to GND		0		Ω
BT/BK PIN, PWM_EN PIN, PWM_TRI Pin						
Input Leakage Current	I_{ILK}	Forced input voltage at pins (BT/BK, PWM_EN, PWM_TRI) = 0V to 5V	**-1**		**1**	µA
Low-Level Input Voltage	V_{IL}				**0.8**	V
High-Level Input Voltage	V_{IH}		**2.0**			V
FAULT/ALERT Output (XSTAT_FLAG, XHIC-LAT_F, XSYS_FAIL)						
Leakage Current	I_{LK_FAULTS}	Forced output voltage at pin XSTAT_FLAG = 5V			**1**	µA
Pull-Down Current	I_{PD_FAULTS}	Forced output voltage at pins (XHIC-LAT_F, XSYS_FAIL) = 5V	**0.5**	1.1	**2.0**	µA
Low-Level Output Voltage	V_{OL_FAULTS}	Output sink current at pins (XSTAT_FLAG, XHIC-LAT_F, XSYS_FAIL) = 3mA		0.1	**0.5**	V
Low-Level Input Voltage	V_{IL_FAULTS}	Input mode at XHIC-LAT_F			**0.8**	V
High-Level Input Voltage	V_{IH_FAULTS}	Input mode at XHIC-LAT_F	**2.0**			V
I^2C/PMBus Interface						
Logic Low-Level Input Voltage	V_{IL}	SDA (Input mode), SCK pin	**0**		**0.8**	V
Logic High-Level Input Voltage	V_{IH}	SDA (Input mode), SCK pin	**2.1**		**V_{CC}**	V
Hysteresis	V_{HYS}	SDA (Input mode), SCK pin		0.5		V
SDA Low-Level Output Voltage	V_{OL}	I_{OUT_SDA} = 3mA, SDA pin (Output mode)			**0.5**	V
Input Current	I_I	SDA (Input mode), SCK pin	**-1**		**1**	µA
SCK Clock Frequency	f_{SCK}				**400**	kHz
Input Capacitance	C_{IN}	SDA (Input mode), SCK pin		5		pF
SCK Falling Edge to SDA Valid Time	t_H				**1**	µs
Over-Temperature Protection						
Over-Temperature Threshold				+160		°C
Over-Temperature Recovery Threshold				+145		°C

Notes:

8. Compliance to datasheet limits is assured by one or more methods; production test, characterization, and/or design.
9. The IC is tested in conditions with minimum power dissipation in the IC, meaning $T_A = T_J$.

3. Typical Performance Curves

All the performance curves are taken from the Evaluation Board (ISL78224EVAL1Z) unless otherwise noted. All references to temperature are for the ISL78224 only. All other components are fan cooled with respect to room temperature. PD = Phase Drop.

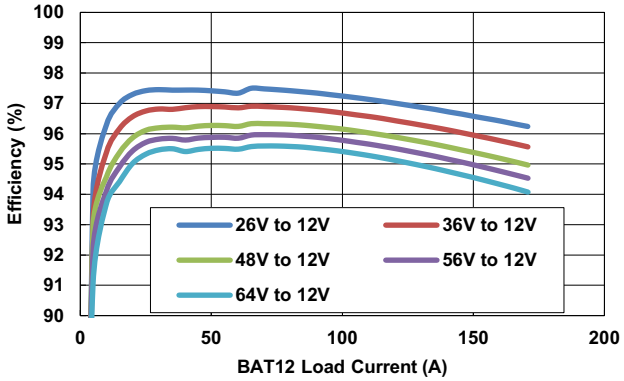


Figure 8. Buck Efficiency (4-Phase, Buck Mode, DE Mode, Phase Drop Enabled, f_{CLK} = 100kHz)

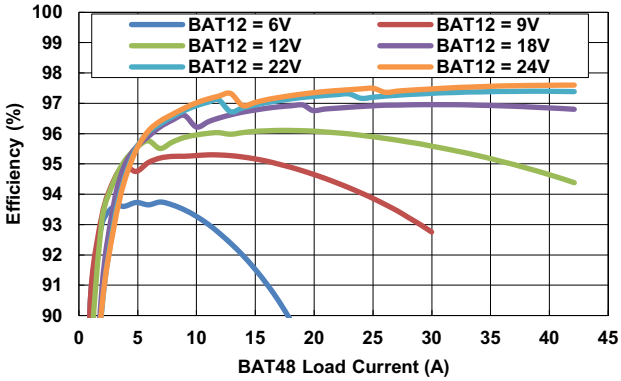


Figure 9. Boost Efficiency (4-Phase, Boost Mode, DE Mode, Phase Drop Enabled, f_{CLK} = 100kHz). 10V to 48V Curve Goes Into Current Limit at ~48A.

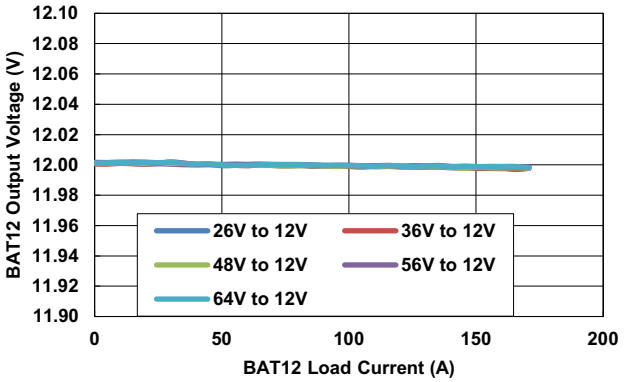


Figure 10. BAT12 Output Voltage (+25°C, 4-Phase, Buck Mode, DE Mode, Phase Drop Enabled, f_{CLK} = 100kHz)

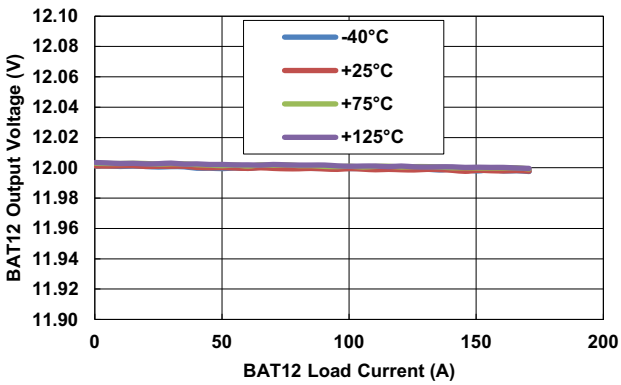


Figure 11. BAT12 Output Voltage ($48V_{IN}$, 4-Phase, Buck Mode, DE Mode, Phase Drop Enabled, f_{CLK} = 100kHz)

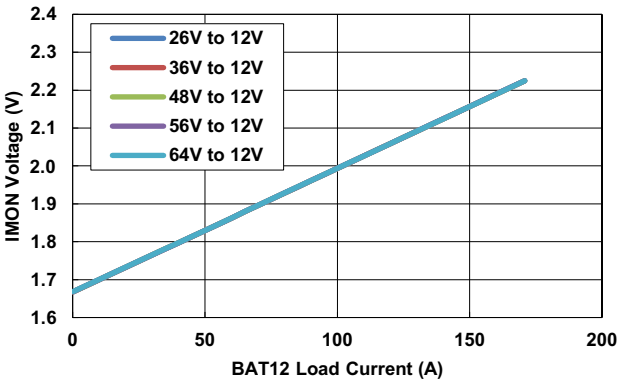


Figure 12. Buck IMON Voltage (+25°C, 4-Phase, Buck Mode, DE Mode, Phase Drop Enabled, f_{CLK} = 100kHz)

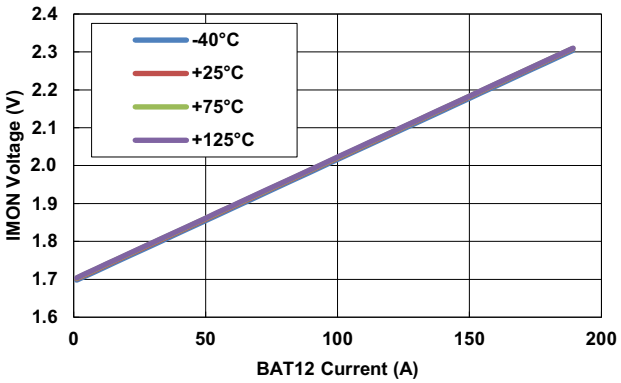


Figure 13. Boost IMON Voltage, BAT12 = 12V (4-Phase, Boost Mode, DE Mode, Phase Drop Enabled, f_{CLK} = 100kHz)

All the performance curves are taken from the Evaluation Board (ISL78224EVAL1Z) unless otherwise noted. All references to temperature are for the ISL78224 only. All other components are fan cooled with respect to room temperature. PD = Phase Drop. **(Continued)**

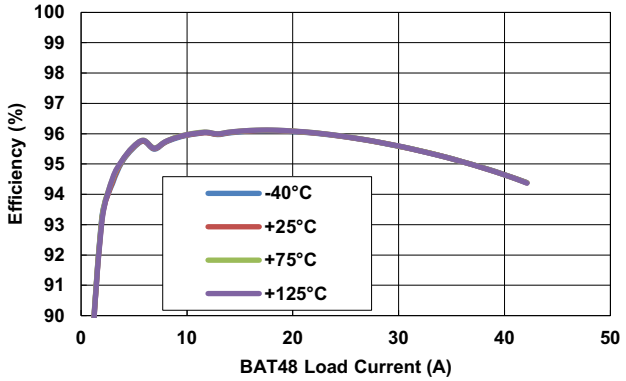


Figure 14. BAT12 = 12V, Boost to 48V (4-Phase, Boost Mode, DE Mode, Phase Drop Enabled, f_{CLK} = 100kHz)

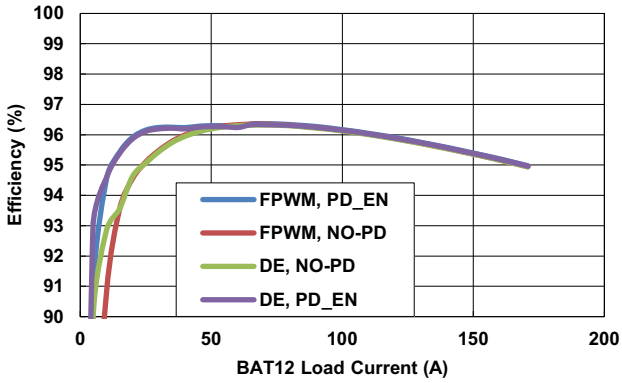


Figure 15. 48V to 12V (4-Phase, Buck Mode, f_{CLK} = 100kHz)

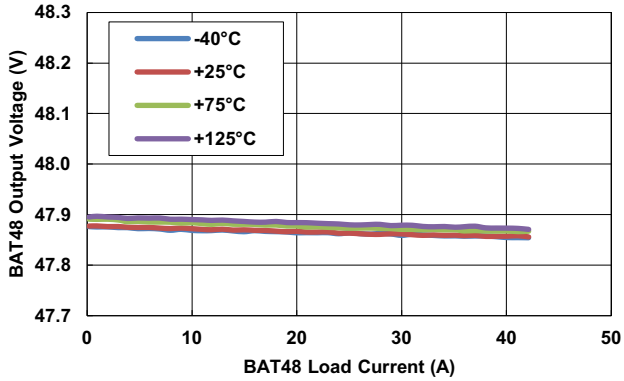


Figure 16. BAT48 Output Voltage, BAT12 = 12V (4-Phase, Boost Mode, DE Mode, Phase Drop Enabled, f_{CLK} = 100kHz)

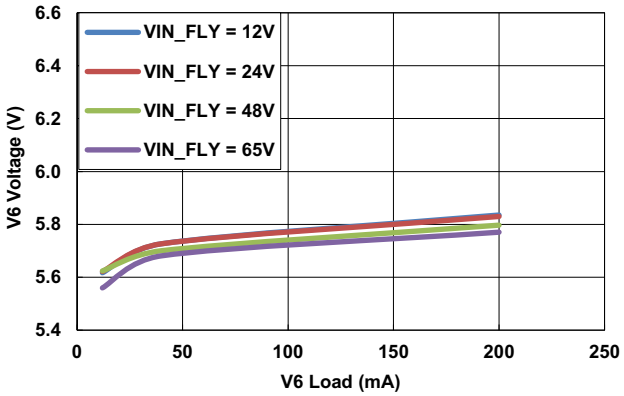


Figure 17. V6 Flyback Output Voltage (f_{CLK} = 100kHz, +25°C)

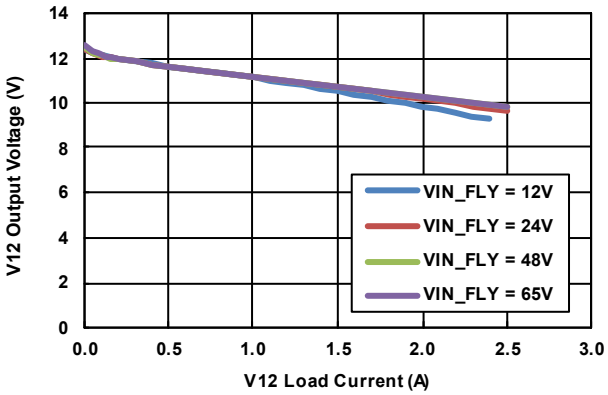


Figure 18. V12 Flyback Output Voltage (f_{CLK} = 100kHz, +25°C)

All the performance curves are taken from the Evaluation Board (ISL78224EVAL1Z) unless otherwise noted. All references to temperature are for the ISL78224 only. All other components are fan cooled with respect to room temperature. PD = Phase Drop. **(Continued)**

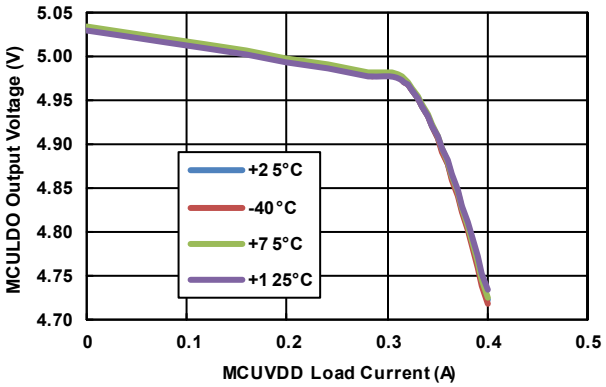


Figure 19. MCULDO Output Voltage (V6 = 6V)

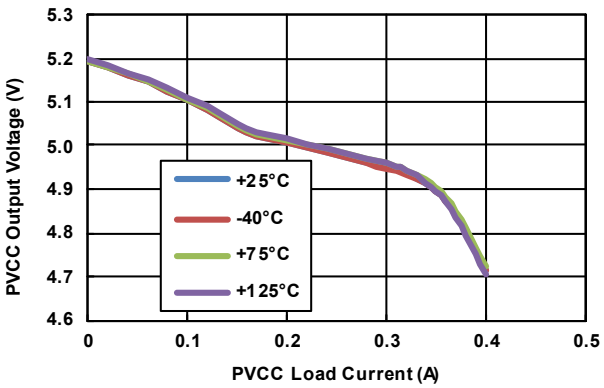


Figure 20. PVCC Output Voltage (V6 = 6V)

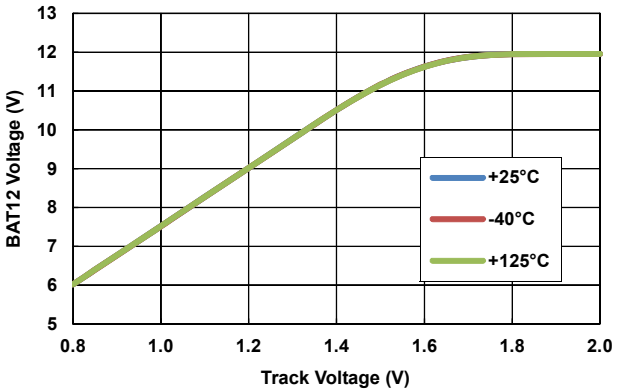


Figure 21. Analog Buck Tracking vs Track Voltage (Analog Tracking Mode, Buck Mode, DE Mode, Phase Drop Disabled, f_{CLK} = 100kHz)

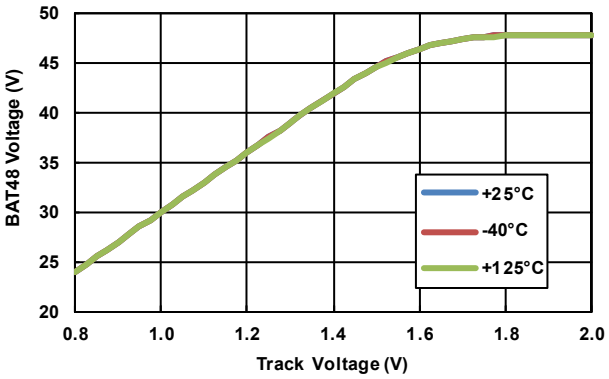


Figure 22. Analog Boost Tracking vs Track Voltage (Analog Tracking Mode, Boost Mode, DE Mode, Phase Drop Disabled, f_{CLK} = 100kHz)

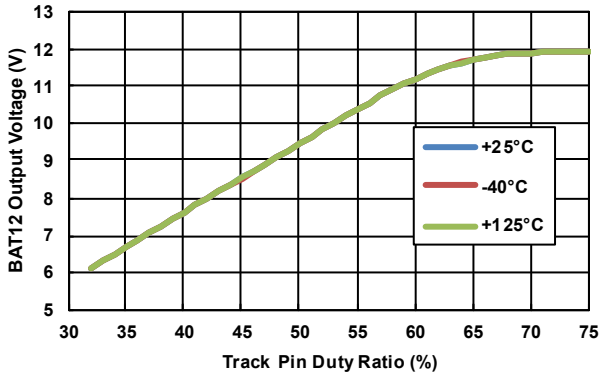


Figure 23. BAT12 Output Voltage (Digital Tracking Mode, FTRK = 500kHz, Buck Mode, DE Mode, Phase Drop Disabled, f_{CLK} = 100kHz)

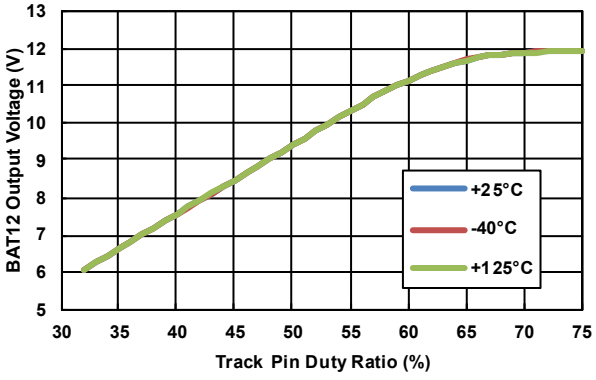


Figure 24. BAT12 Output Voltage (Digital Tracking Mode, FTRK = 200kHz, Buck Mode, DE Mode, Phase Drop Disabled, f_{CLK} = 100kHz)

All the performance curves are taken from the Evaluation Board (ISL78224EVAL1Z) unless otherwise noted. All references to temperature are for the ISL78224 only. All other components are fan cooled with respect to room temperature. PD = Phase Drop. **(Continued)**

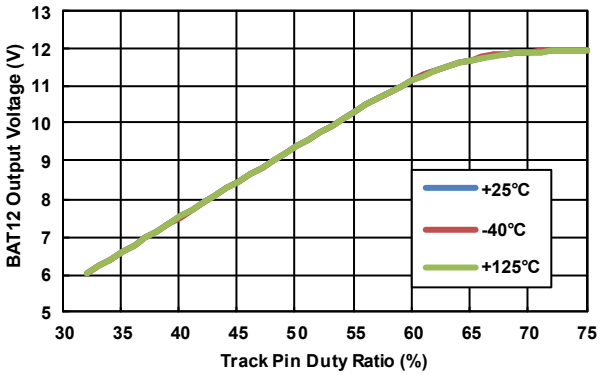


Figure 25. BAT12 Output Voltage (Digital Tracking Mode, FTRK = 150kHz, Buck Mode, DE Mode, Phase Drop Disabled, f_{CLK} = 100kHz)

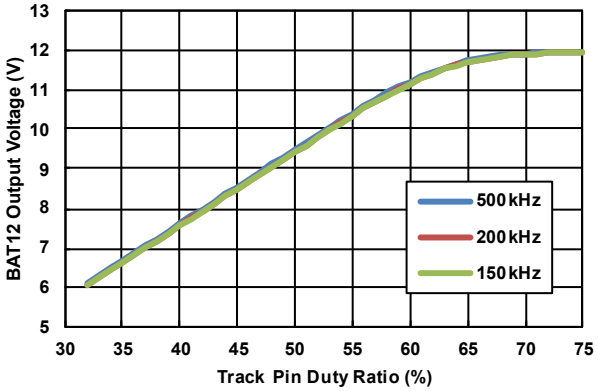


Figure 26. BAT12 Output Voltage at Three Track Pin Frequencies (Digital Tracking Mode, Buck Mode, DE Mode, Phase Drop Disabled, f_{CLK} = 100kHz)

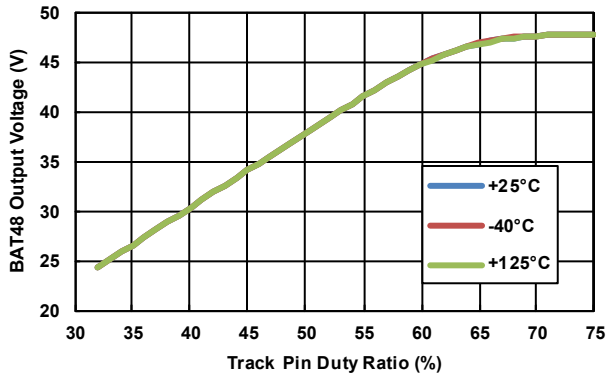


Figure 27. BAT48 Output Voltage (Digital Tracking Mode, FTRK = 500kHz, Boost Mode, DE Mode, Phase Drop Disabled, f_{CLK} = 100kHz)

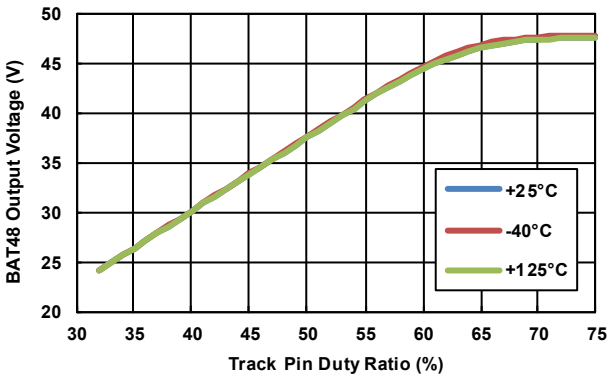


Figure 28. BAT48 Output Voltage (Digital Tracking Mode, FTRK = 200kHz, Boost Mode, DE Mode, Phase Drop Disabled, f_{CLK} = 100kHz)

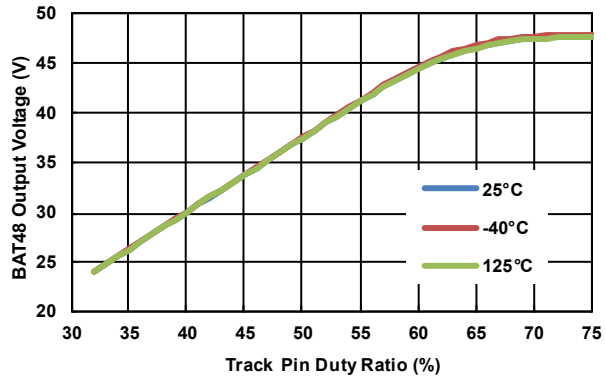


Figure 29. BAT48 Output Voltage (Digital Tracking Mode, FTRK = 150kHz, Boost Mode, DE Mode, Phase Drop Disabled, f_{CLK} = 100kHz)

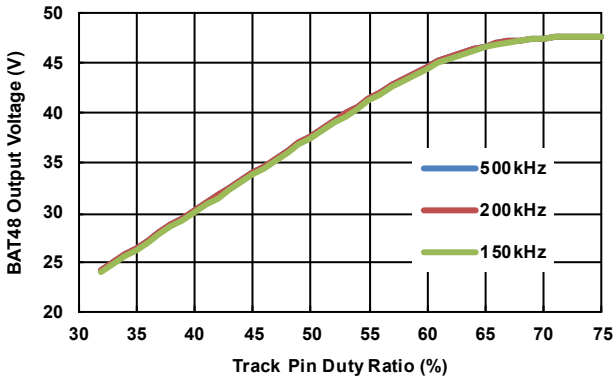


Figure 30. BAT48 Output Voltage at Three Track Pin Frequencies (Digital Tracking Mode, Boost Mode, DE Mode, Phase Drop Disabled, f_{CLK} = 100kHz)

All the performance curves are taken from the Evaluation Board (ISL78224EVAL1Z) unless otherwise noted. All references to temperature are for the ISL78224 only. All other components are fan cooled with respect to room temperature. PD = Phase Drop. **(Continued)**

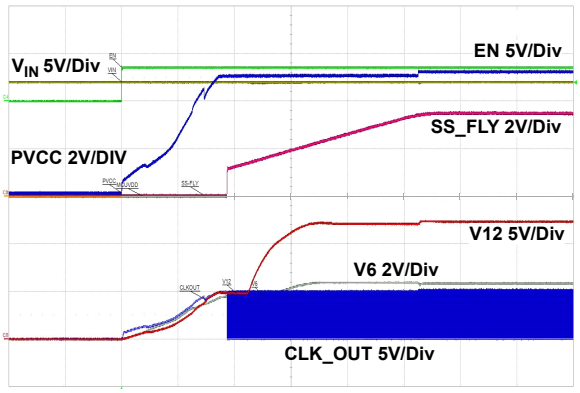


Figure 31. Startup of LDO with Flyback, Flyback-Startup, V_{IN} = 12V, I_L = 1mA, EN On

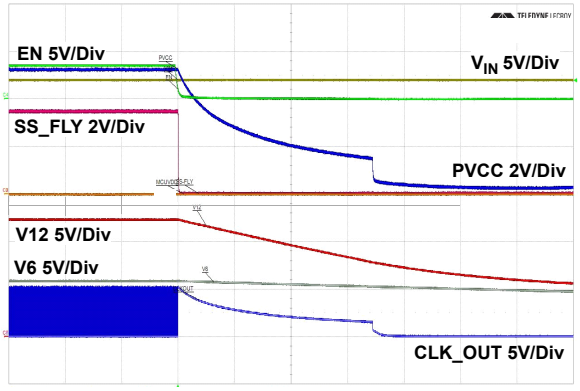


Figure 32. Shutdown of LDO with Flyback, Flyback-Shutdown, V_{IN} = 12V, I_L = 1mA, EN Off

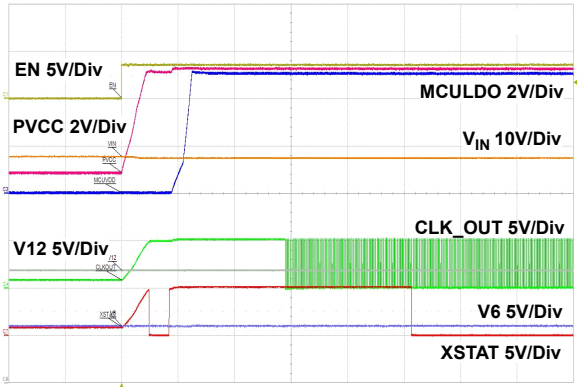


Figure 33. Startup of LDO Without Flyback, LDO-Startup, V_{IN} → V12 and V6 → EN (without BAT12-PREBIAS): EN On

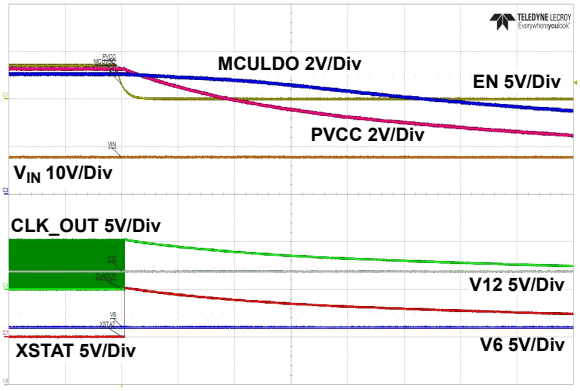


Figure 34. Shutdown of LDO Without Flyback, LDO-Startup, V_{IN} → V12 AND V6 → EN (without BAT12-Prebias): EN Off

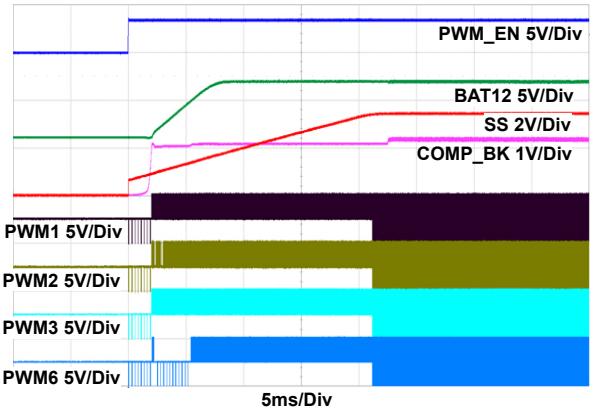


Figure 35. Soft-Start in Buck/DE/NO-PD, 48V to 12V, 6Ω Load on BAT12

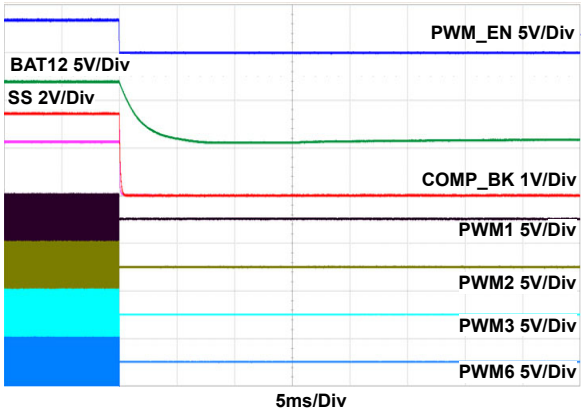


Figure 36. Shutdown in Buck/DE/NO-PD, 48V to 12V, 6Ω Load on BAT12

All the performance curves are taken from the Evaluation Board (ISL78224EVAL1Z) unless otherwise noted. All references to temperature are for the ISL78224 only. All other components are fan cooled with respect to room temperature. PD = Phase Drop. **(Continued)**

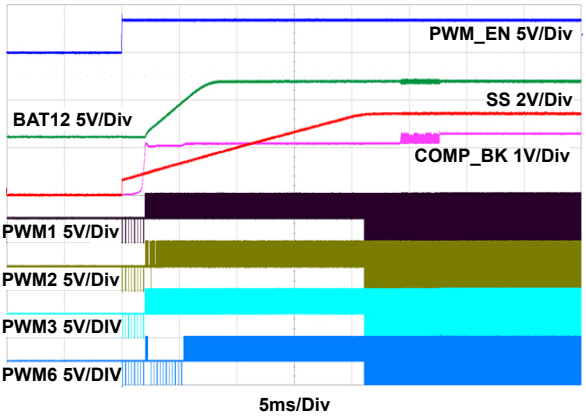


Figure 37. Soft-start in Buck/FPWM/NO-PD, 48V to 12V, 6Ω Load on BAT12

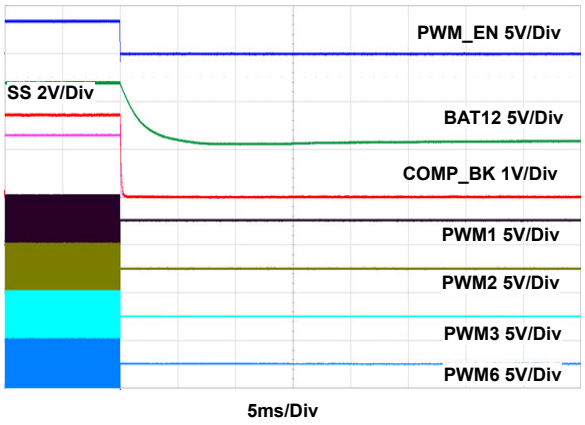


Figure 38. Shutdown in Buck/FPWM/NO-PD, 48V to 12V, 6Ω Load on BAT12

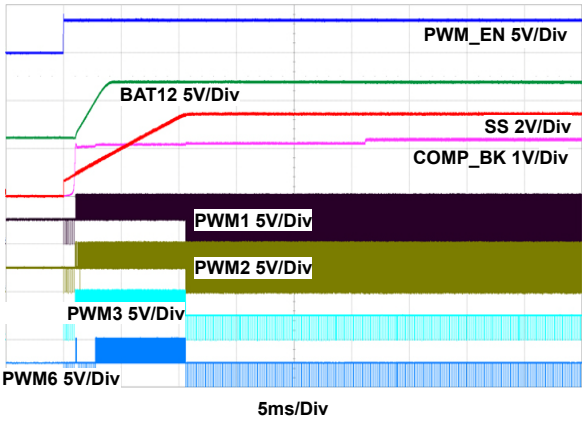


Figure 39. Soft-Start in Buck/DE/PD-Enabled, 48V to 12V, 6Ω Load on BAT12

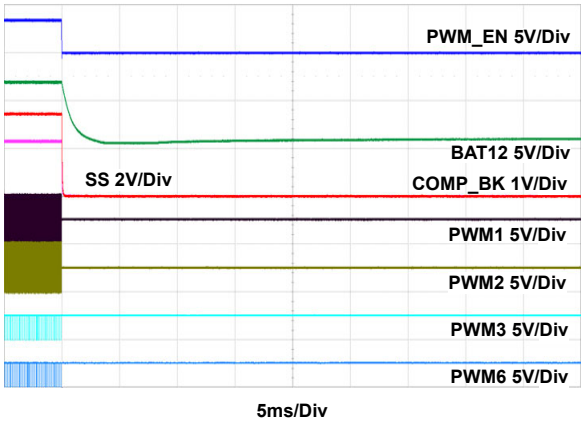


Figure 40. Shutdown in Buck/DE/PD-Enabled, 48V to 12V, 6Ω Load on BAT12

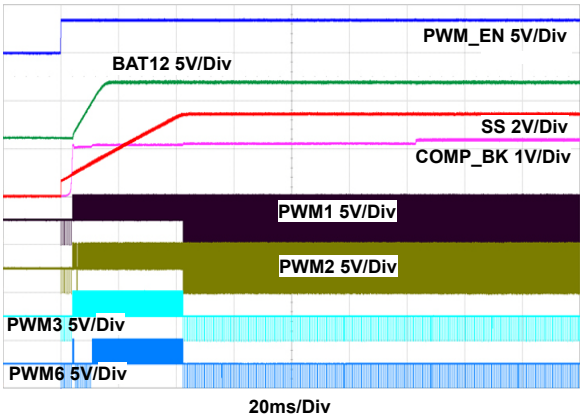


Figure 41. Soft-Start in Buck/FPWM/PD-Enabled, 48V to 12V, 6Ω Load on BAT12

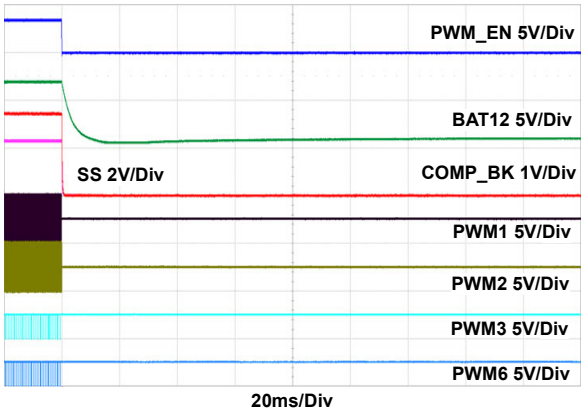


Figure 42. Shutdown in Buck/FPWM/PD-Enabled, 48V to 12V, 6Ω Load on BAT12

All the performance curves are taken from the Evaluation Board (ISL78224EVAL1Z) unless otherwise noted. All references to temperature are for the ISL78224 only. All other components are fan cooled with respect to room temperature. PD = Phase Drop. **(Continued)**

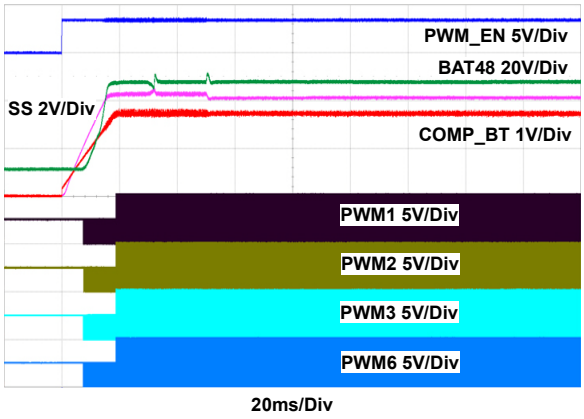


Figure 43. Soft-Start in Boost/DE/NO-PD, 12V to 48V, 6Ω Load on BAT48

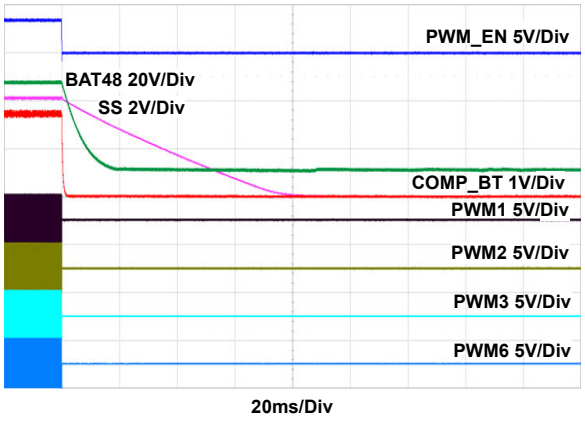


Figure 44. Shutdown in Boost/DE/NO-PD, 12V to 48V, 6Ω Load on BAT48

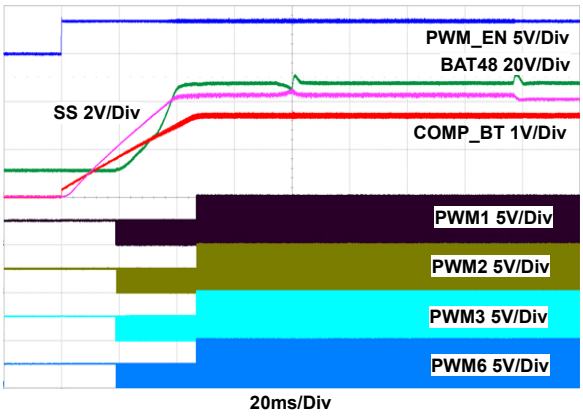


Figure 45. Soft-Start in Boost/FPWM/NO-PD, 12V to 48V, 6Ω Load On BAT48

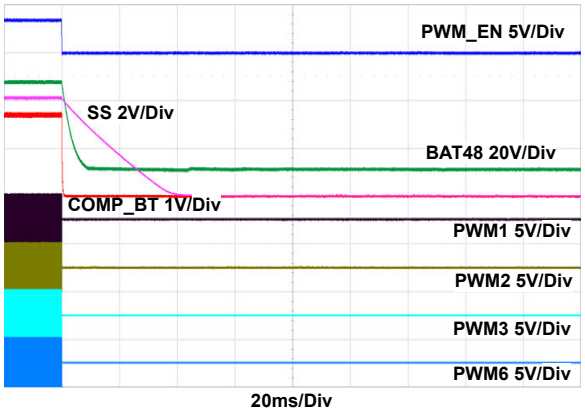


Figure 46. Shutdown in Boost/FPWM/NO-PD, 12V to 48V, 6Ω Load on BAT48

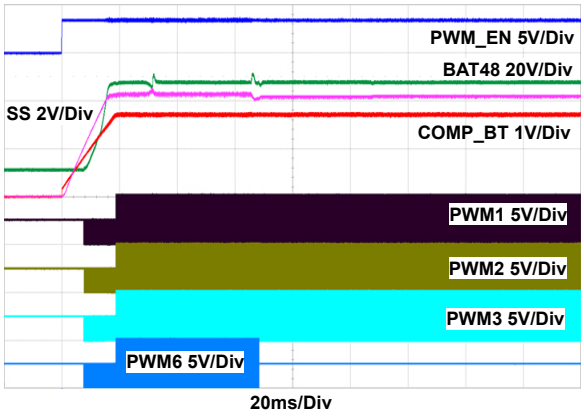


Figure 47. Soft-start in Boost/DE/PD-Enabled, 12V to 48V, 6Ω Load on BAT48

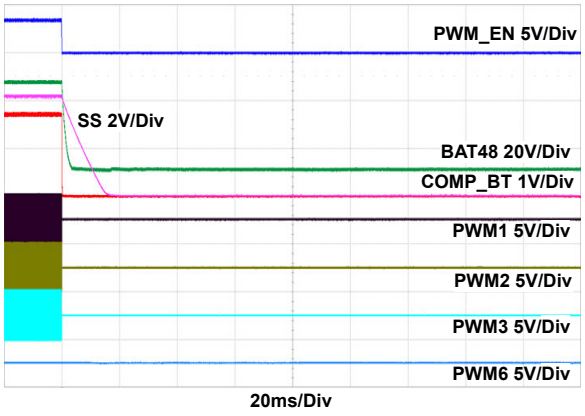


Figure 48. Shutdown In Boost/DE/PD-Enabled, 12V to 48V, 6Ω Load on BAT48

All the performance curves are taken from the Evaluation Board (ISL78224EVAL1Z) unless otherwise noted. All references to temperature are for the ISL78224 only. All other components are fan cooled with respect to room temperature. PD = Phase Drop. **(Continued)**

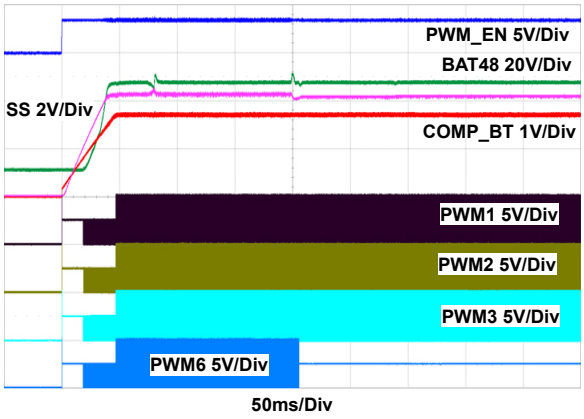


Figure 49. Soft-Start in Boost/FPWM/PD-Enabled, 12V to 48V, 6Ω Load on BAT48

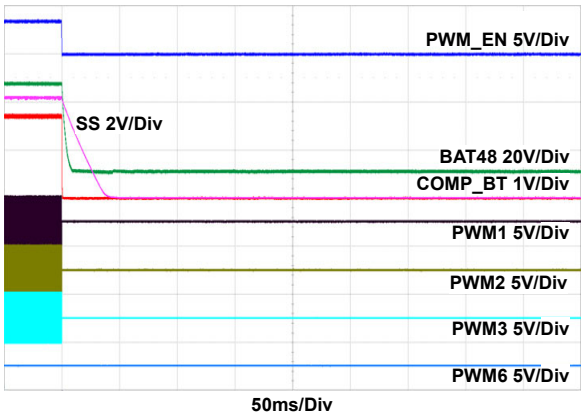


Figure 50. Shutdown in Boost/FPWM/PD-Enabled, 12V to 48V, 6Ω Load on BAT48

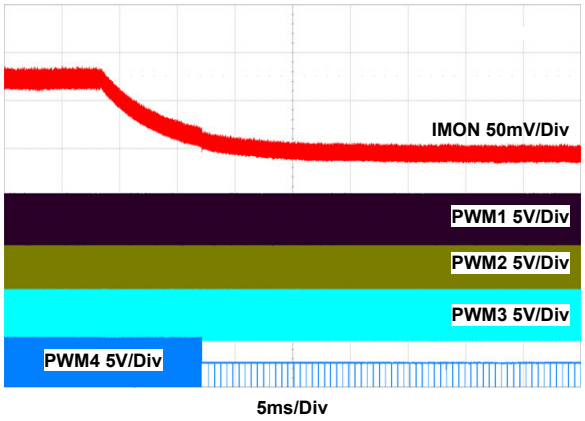


Figure 51. Phase Drop Transition in Buck/DE (4PH → 3PH), I_O = 100A → 64A

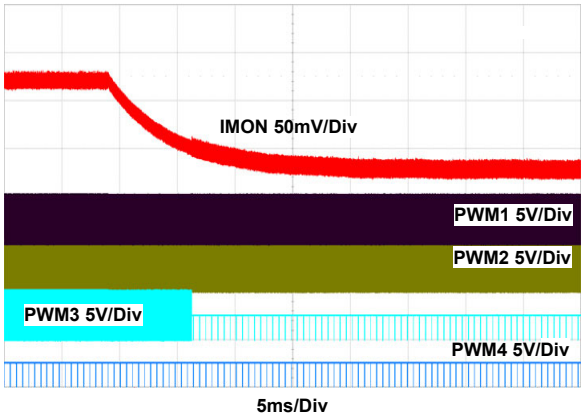


Figure 52. Phase Drop Transition in Buck/DE (3PH → 2PH), I_O = 75A → 35A

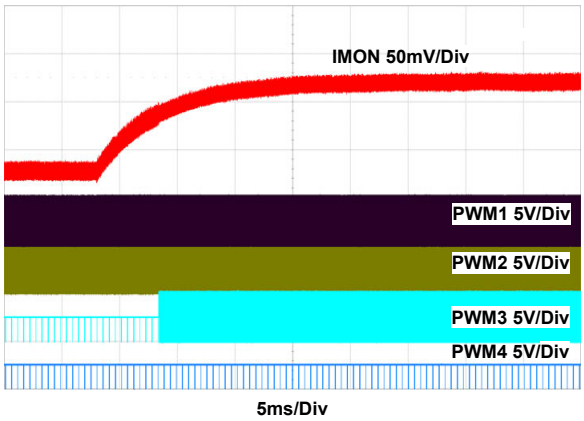


Figure 53. Phase Add Transition in Buck/DE (2PH → 3PH), I_O = 1A → 50A

All the performance curves are taken from the Evaluation Board (ISL78224EVAL1Z) unless otherwise noted. All references to temperature are for the ISL78224 only. All other components are fan cooled with respect to room temperature. PD = Phase Drop. **(Continued)**

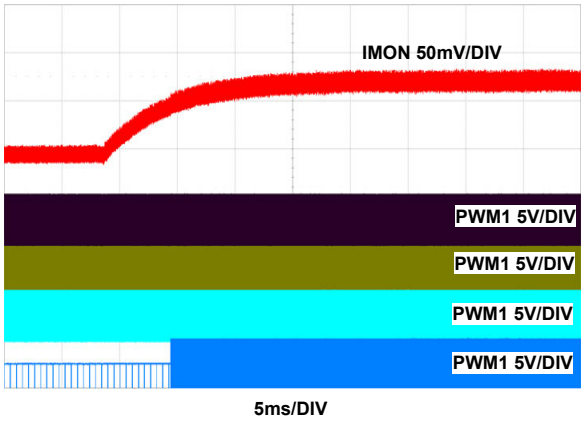


Figure 54. Phase Add Transition in Buck/DE (3PH → 4PH), I_O = 36A → 80A

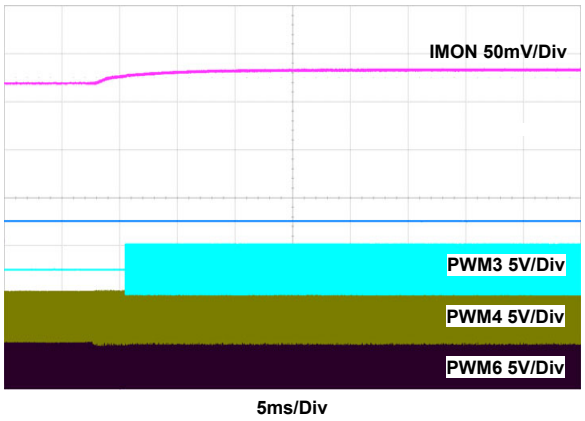


Figure 55. Phase Add Transition in Boost/ DE (3PH → 4PH), I_O = 4A → 13A

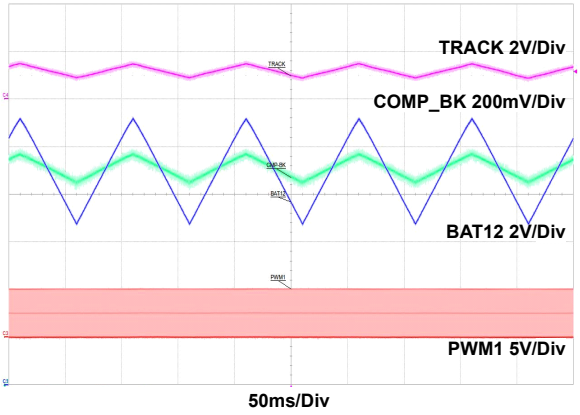


Figure 56. Analog Tracking Transient Waveforms in Buck/DE/NO-PD, A-Track Sweep: 0.9V to 1.5V, I_{OUT} = 100A

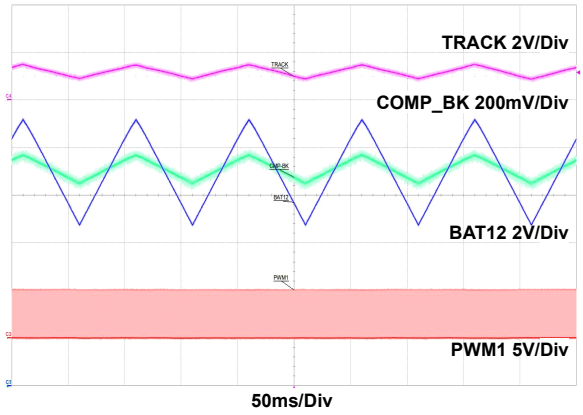


Figure 57. Analog Tracking Transient Waveforms in Buck/FPWM/NO-PD, A-Track Sweep: 0.9V to 1.5V, I_{OUT} = 100A

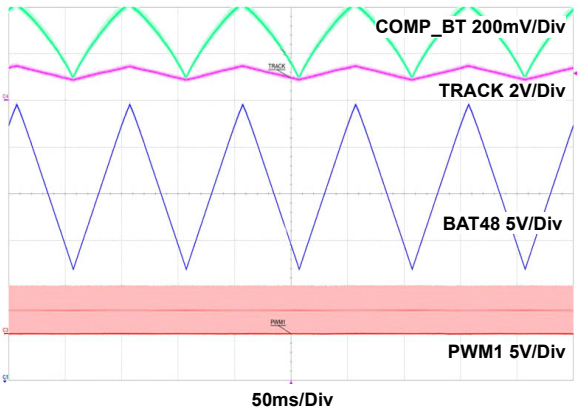


Figure 58. Analog Tracking Transient Waveforms in Boost/DE/NO-PD, A-Track Sweep: 0.9V to 1.5V, I_{OUT} = 20A

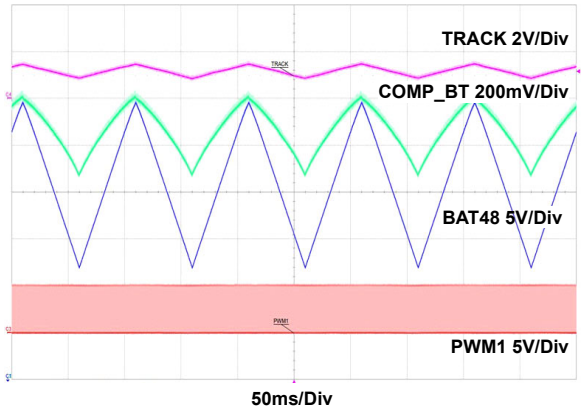


Figure 59. Analog Tracking Transient Waveforms in Boost/FPWM/NO-PD, A-Track Sweep: 0.9V to 1.5V, I_{OUT} = 20A

All the performance curves are taken from the Evaluation Board (ISL78224EVAL1Z) unless otherwise noted. All references to temperature are for the ISL78224 only. All other components are fan cooled with respect to room temperature. PD = Phase Drop. **(Continued)**

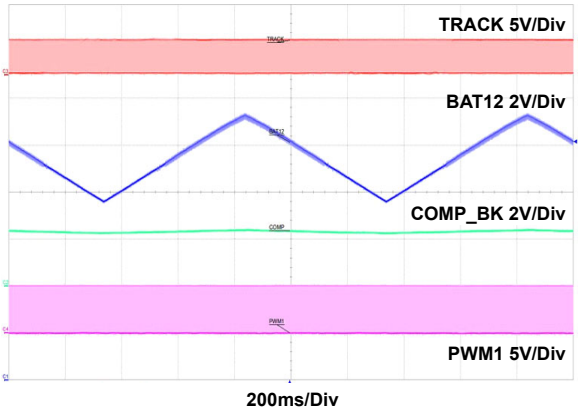


Figure 60. Digital Tracking Transient Waveforms in Buck/DE/NO-PD, D-Track Duty Sweep: 40% to 60%, Frequency-Digital Tracking = 400kHz, I_{OUT} = 100A

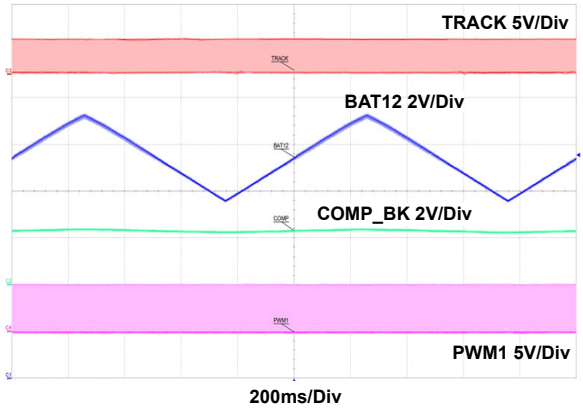


Figure 61. Digital Tracking Transient Waveforms in Buck/FPWM/NO-PD, D-Track Duty Sweep: 40% to 60%, Frequency-Digital Tracking = 400kHz, I_{OUT} = 100A

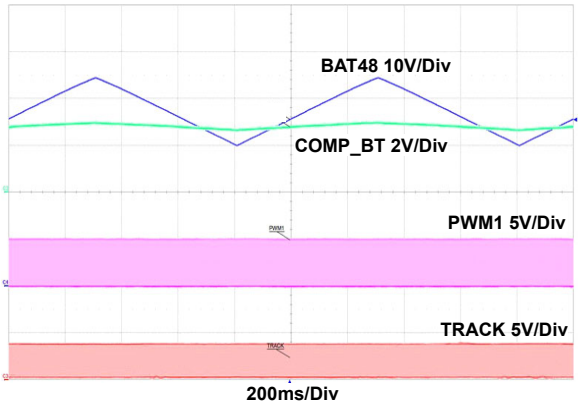


Figure 62. Digital Tracking Transient Waveforms in Boost/DE/NO-PD, D-Track Duty Sweep: 40% to 60%, F-Digital Tracking = 400kHz, I_{OUT} = 20A

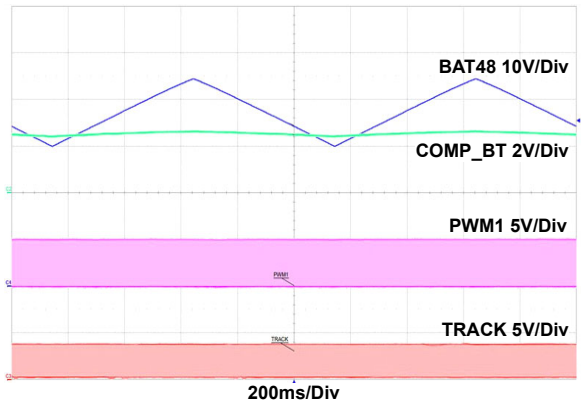


Figure 63. Digital Tracking Transient Waveforms in Boost/FPWM/NO-PD, Digital Tracking Duty Sweep: 40% to 60%, Frequency-Digital Tracking = 400kHz, I_{OUT} = 20A

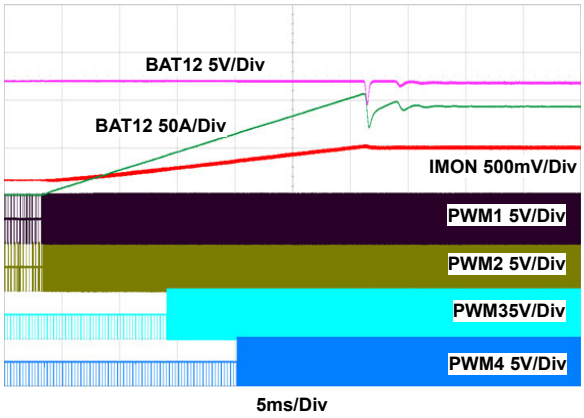


Figure 64. RL1 = 0.15Ω → 0.1Ω

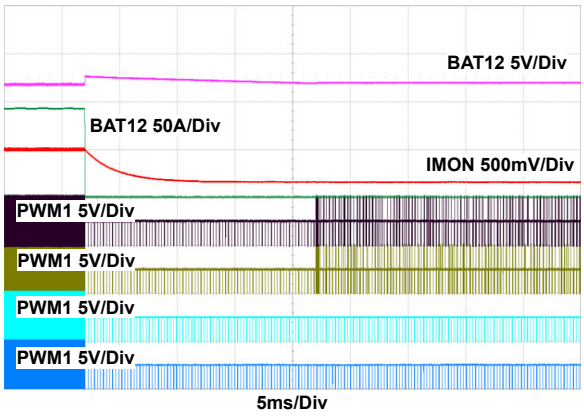


Figure 65. RL = 0.10Ω → 0.15Ω

All the performance curves are taken from the Evaluation Board (ISL78224EVAL1Z) unless otherwise noted. All references to temperature are for the ISL78224 only. All other components are fan cooled with respect to room temperature. PD = Phase Drop. **(Continued)**

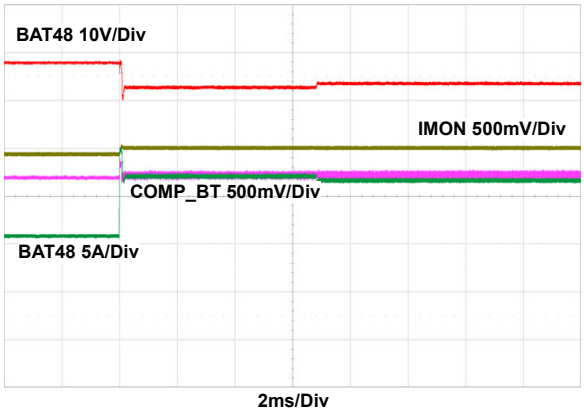


Figure 66. Average Constant Current Control Loop, CCL Transition in Boost/DE/NO-PD, RL1 = 2.5Ω → 2Ω

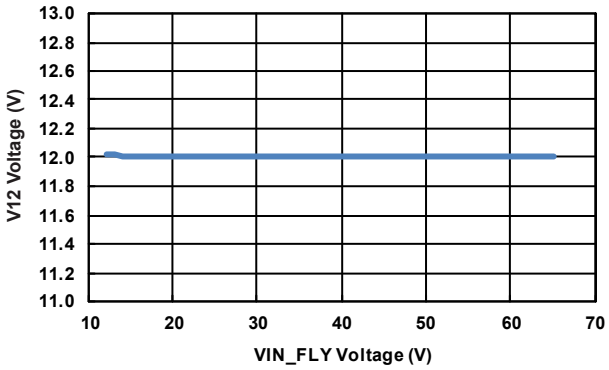


Figure 67. V12 Line Regulation, Temp = +25°C, f_{SW} = 100kHz, V6 Load = 200Ω, V12 Load = 200mA

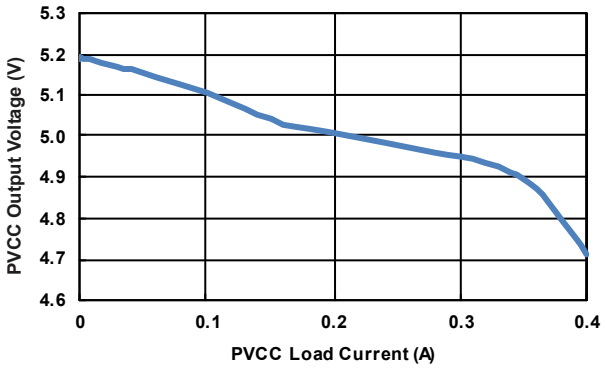


Figure 68. PVCC LDO Load Regulation, V6 = 6V

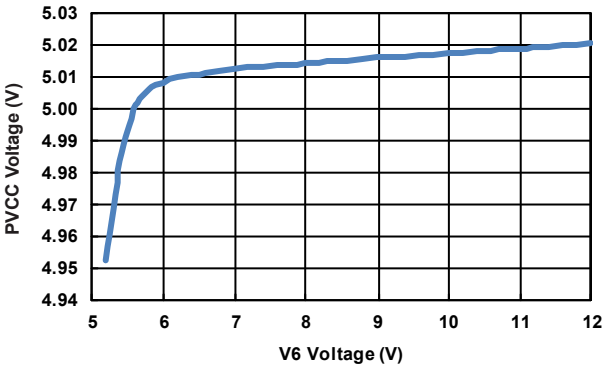


Figure 69. PVCC LDO Line Regulation, 0.2A Load

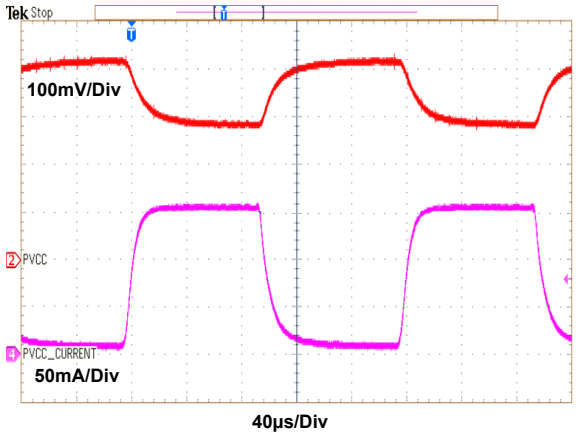


Figure 70. Internal LDO Load Transient, PVCC Offset 4.79V, Transient Load 0mA to 150mA, +25°C

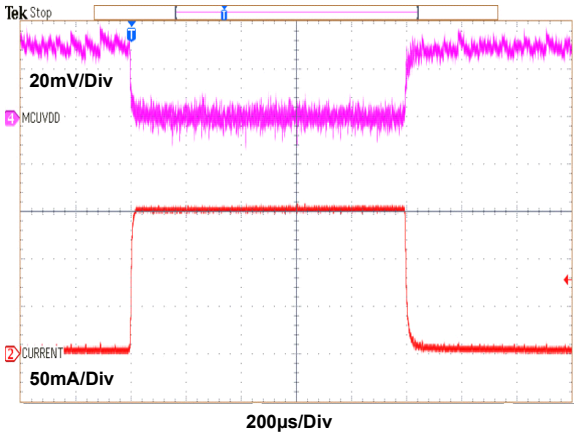


Figure 71. MCULDO Load Transient, I_{LOAD} = 0 to 150mA, MCULDO Offset = 5.0V

All the performance curves are taken from the Evaluation Board (ISL78224EVAL1Z) unless otherwise noted. All references to temperature are for the ISL78224 only. All other components are fan cooled with respect to room temperature. PD = Phase Drop. **(Continued)**

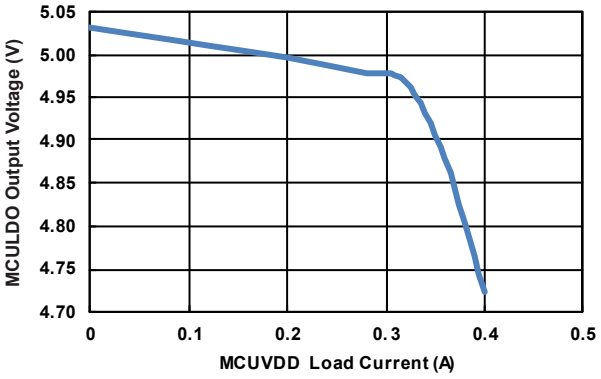


Figure 72. MCULDO Load Regulation, V6 = 6V

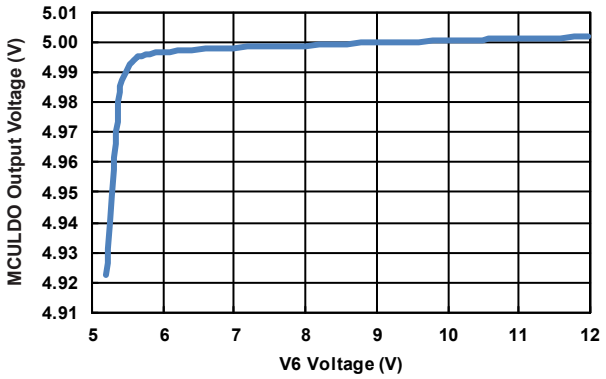


Figure 73. MCULDO Line Regulation, 0.2A Load on MCULDO

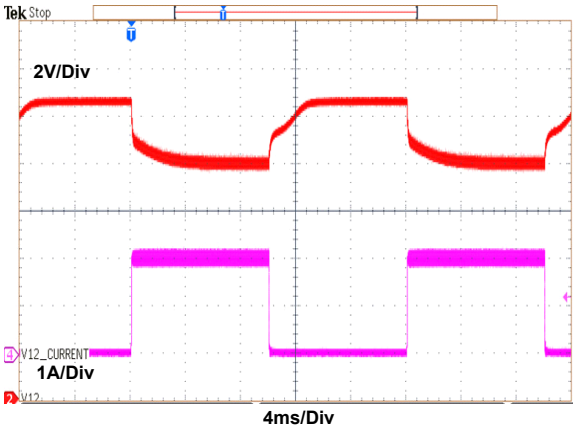


Figure 74. V12 Load Transient, VIN_FLY = 12V, V6 Load = 200Ω, V12 Current = 0 to 2A

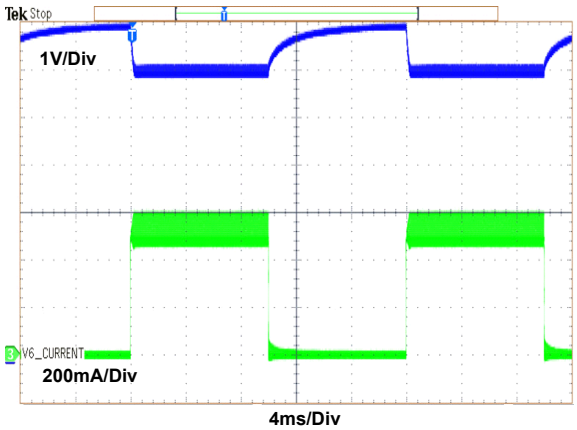


Figure 75. V6 Load Transient, V12 = 9Ω, V6 Current = 0mA to 500mA

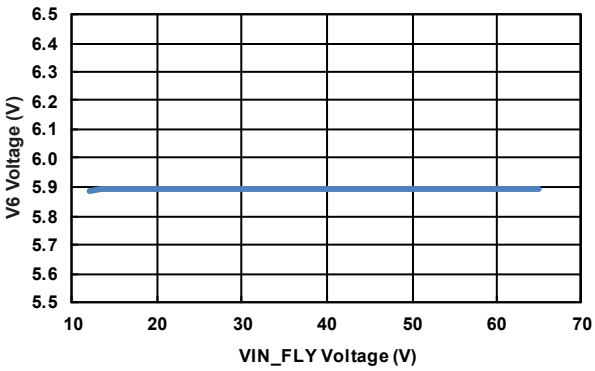


Figure 76. V6 Line Regulation, Temperature = +25°, f_{SW} = 100kHz, V12 Load = 200mA

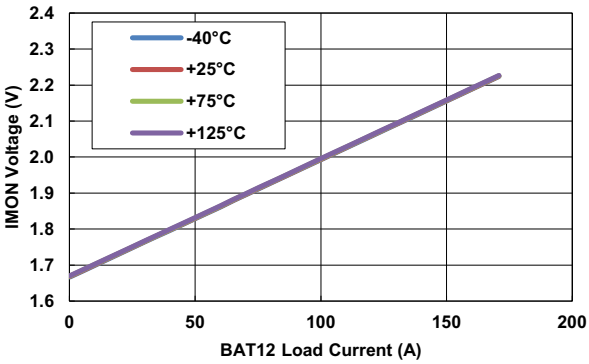


Figure 77. IMON vs Load Current in Buck/DE/PD with Temperature Variable

All the performance curves are taken from the Evaluation Board (ISL78224EVAL1Z) unless otherwise noted. All references to temperature are for the ISL78224 only. All other components are fan cooled with respect to room temperature. PD = Phase Drop. **(Continued)**

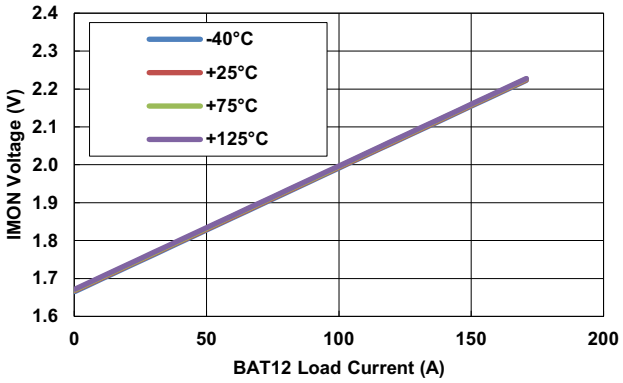


Figure 78. IMON vs Load Current in Buck/DE/NO-PD with Temperature Variable

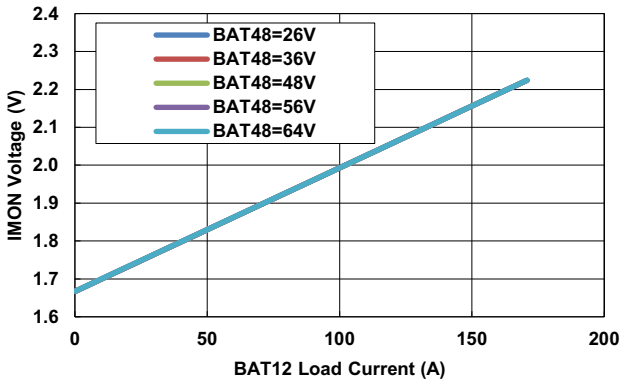


Figure 79. IMON vs Load Current in Buck/DE/NO-PD with BAT48 Variable

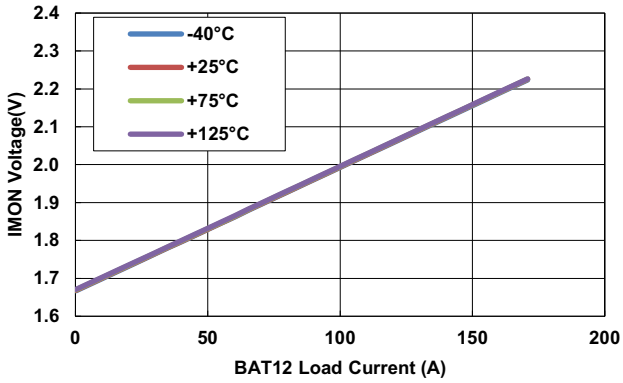


Figure 80. IMON vs Load Current in Buck/FPWM/PD with Temperature Variable

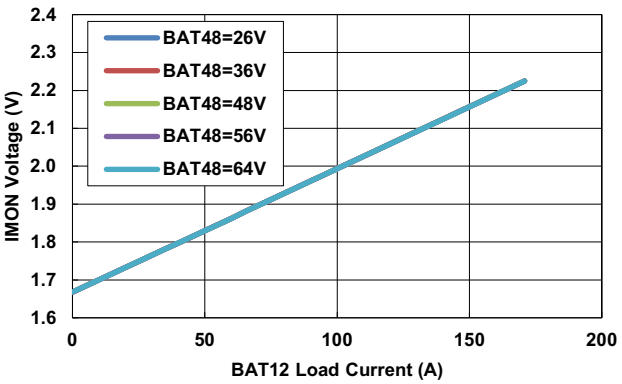


Figure 81. IMON vs Load Current in Buck/FPWM/PD with BAT48 Variable

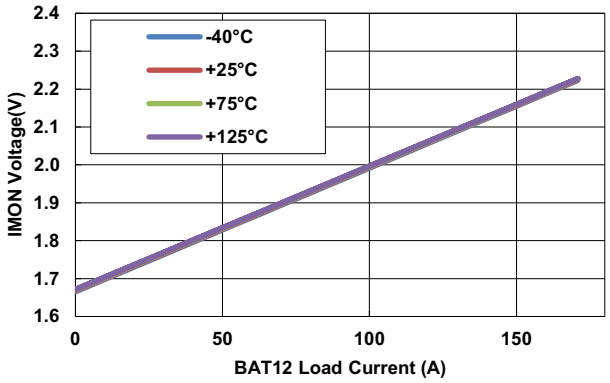


Figure 82. IMON vs BAT12 Load Current in Buck/FPWM/NO-PD with Temperature Variable

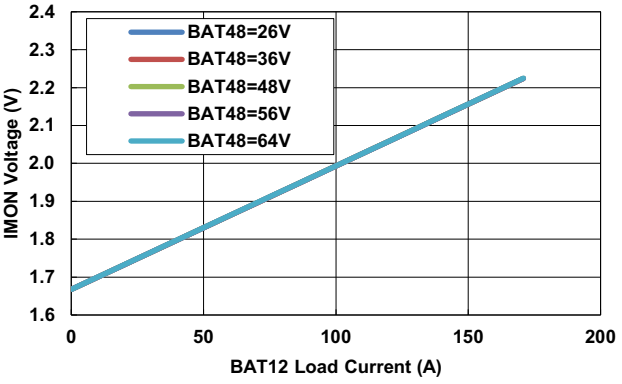


Figure 83. IMON vs Load Current in Buck/FPWM/NO-PD with BAT48 Variable

All the performance curves are taken from the Evaluation Board (ISL78224EVAL1Z) unless otherwise noted. All references to temperature are for the ISL78224 only. All other components are fan cooled with respect to room temperature. PD = Phase Drop. **(Continued)**

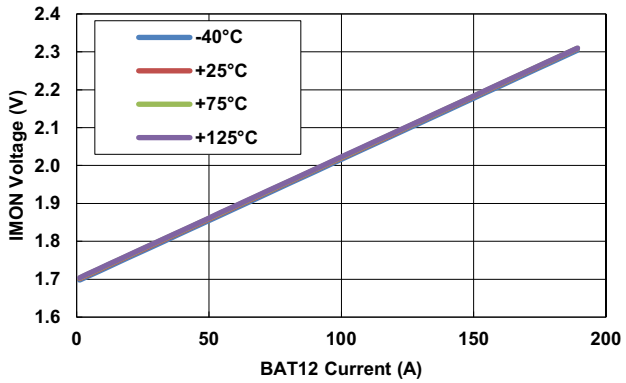


Figure 84. IMON vs BAT12 Current in Boost/DE/PD with Temperature Variable

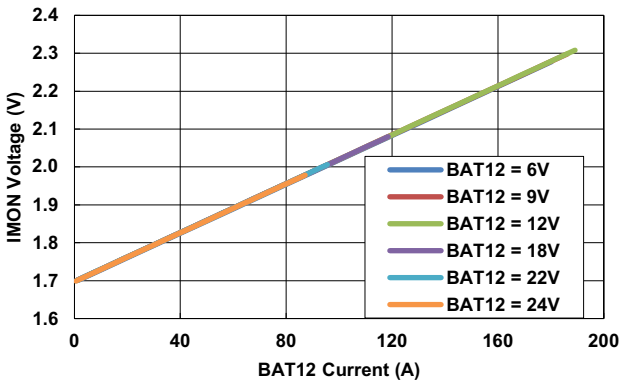


Figure 85. IMON vs BAT12 Current in Boost/DE/PD with BAT12 Variable

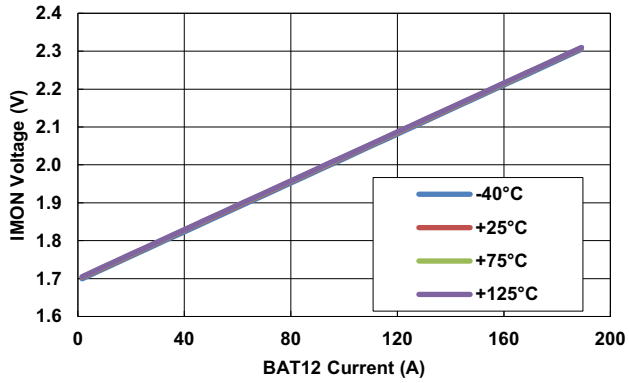


Figure 86. IMON vs BAT12 Current in Boost/DE/NO-PD with Temperature Variable

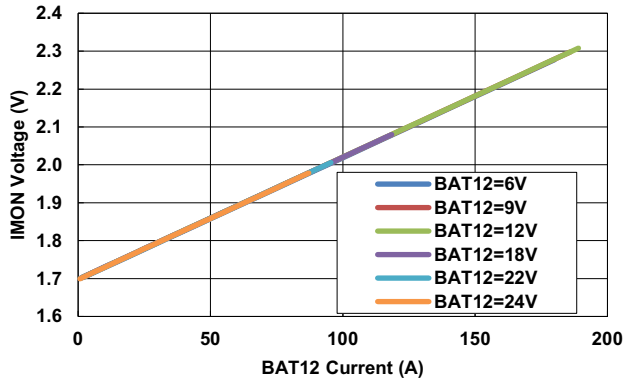


Figure 87. IMON vs BAT12 Current in Boost/DE/NO-PD with BAT12 Variable, f_{CLK} = 100kHz

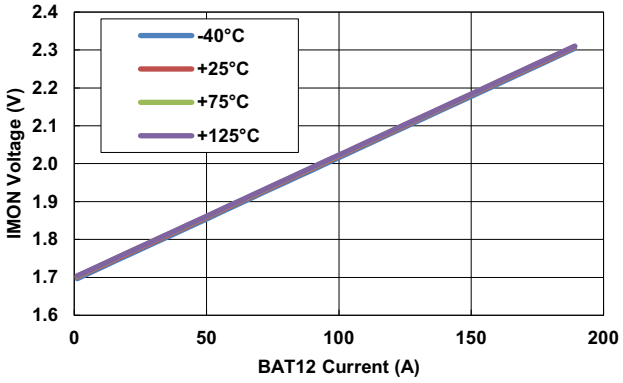


Figure 88. IMON vs BAT12 Current in Boost/FPWM/PD with Temperature Variable, f_{CLK} = 100kHz

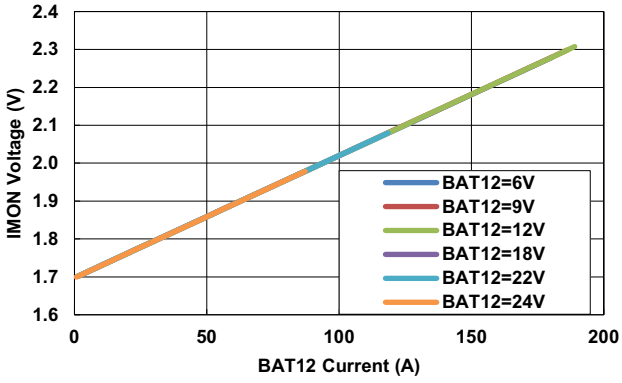


Figure 89. IMON vs BAT12 Current in Boost/FPWM/PD with BAT12 Variable

All the performance curves are taken from the Evaluation Board (ISL78224EVAL1Z) unless otherwise noted. All references to temperature are for the ISL78224 only. All other components are fan cooled with respect to room temperature. PD = Phase Drop. **(Continued)**

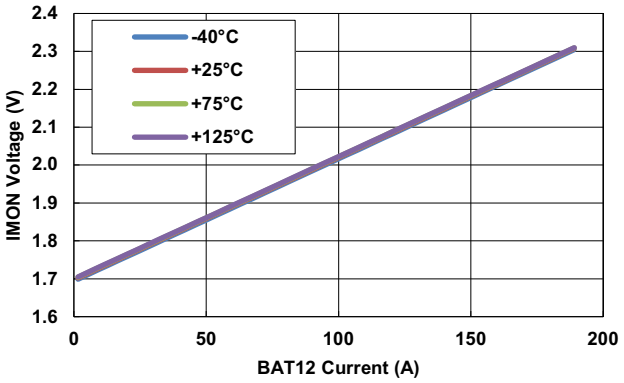


Figure 90. IMON vs BAT12 Current in Boost/FPWM/NO-PD with Temperature Variable

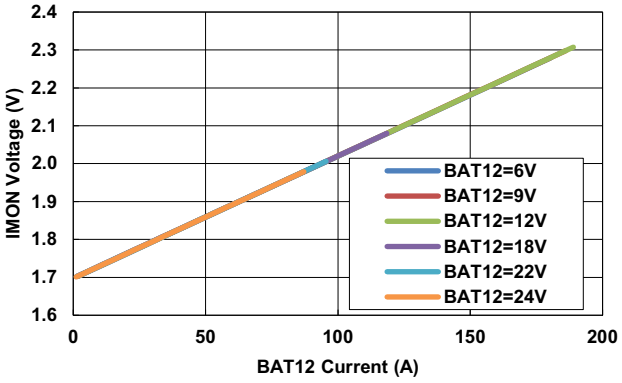


Figure 91. IMON vs BAT12 Current in Boost/FPWM/NO-PD with BAT12 Variable

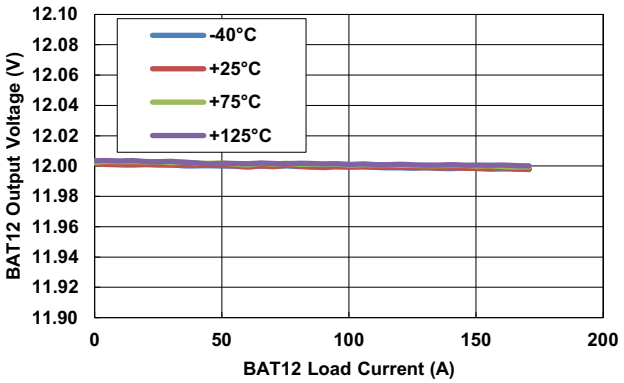


Figure 92. BAT12 Output Voltage In Buck/FPWM/PD with Temperature Variable

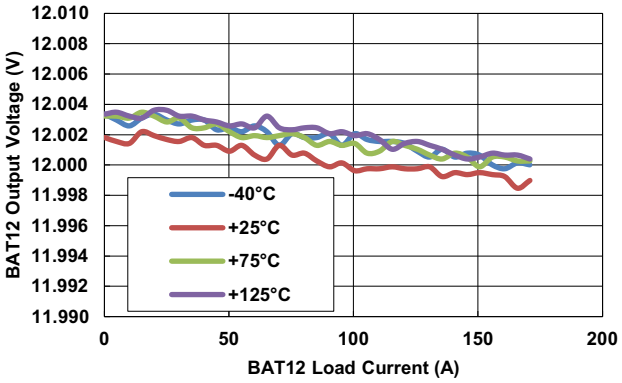


Figure 93. BAT12 Output Voltage in Buck/DE/NO-PD with Temperature Variable

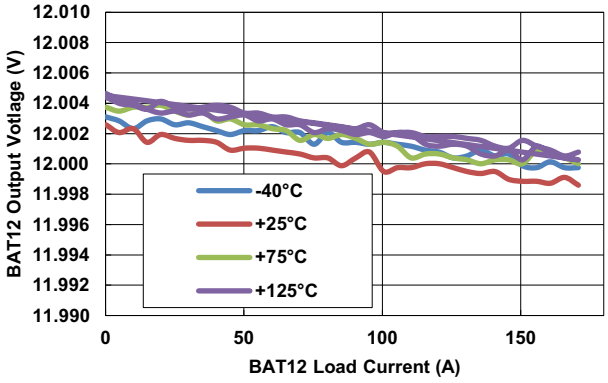


Figure 94. BAT12 Output Voltage in Buck/FPWM/NO-PD with Temperature Variable

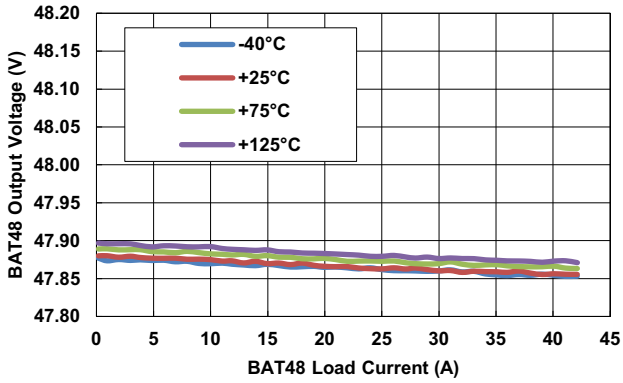


Figure 95. BAT48 Voltage In Boost/DE/NO-PD with Temperature Variable, f_{CLK} = 100kHz

All the performance curves are taken from the Evaluation Board (ISL78224EVAL1Z) unless otherwise noted. All references to temperature are for the ISL78224 only. All other components are fan cooled with respect to room temperature. PD = Phase Drop. **(Continued)**

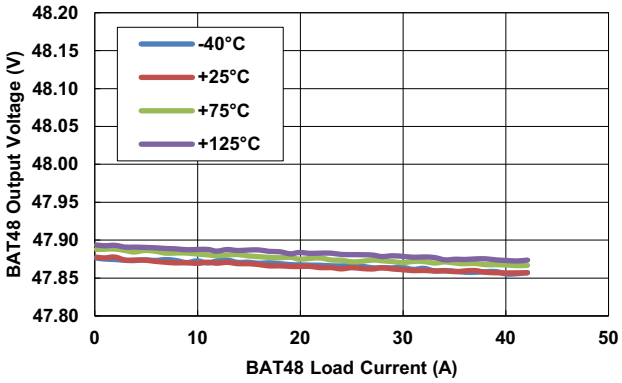


Figure 96. BAT48 Voltage in Boost/FPWM/PD with Temperature Variable, f_{CLK} = 100kHz

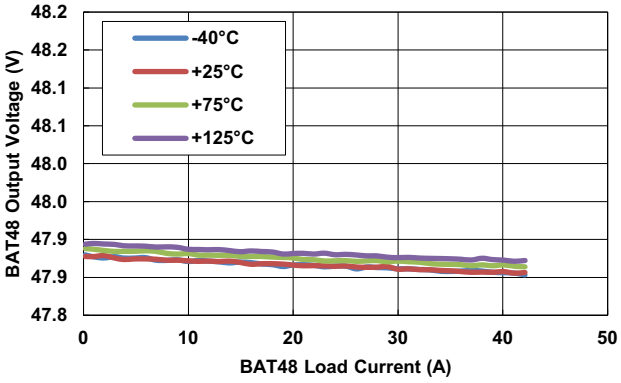


Figure 97. BAT48 Voltage in Boost/FPWM/NO-PD with Temperature Variable, f_{CLK} = 100kHz

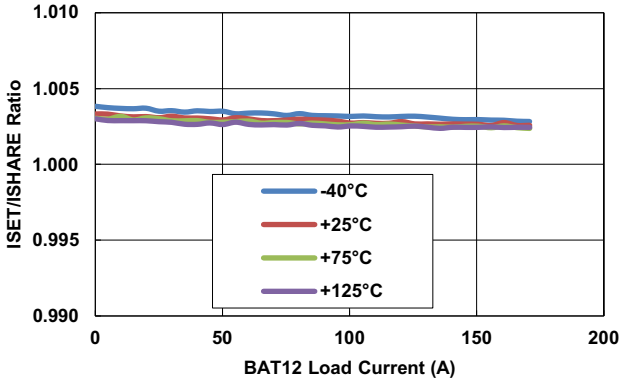


Figure 98. ISET/ISHARE Ratio vs Load Current in Buck/DE/NO-PD

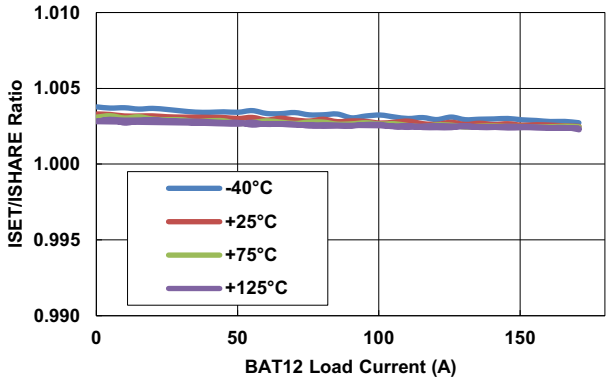


Figure 99. ISET/ISHARE Ratio vs Load Current in Buck/FPWM/NO-PD

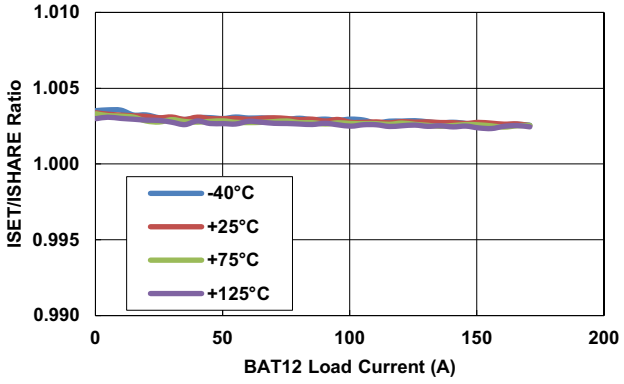


Figure 100. ISET/ISHARE Ratio vs Load Current in Buck/DE, +25°C, BAT48 = 48, PD-Enabled

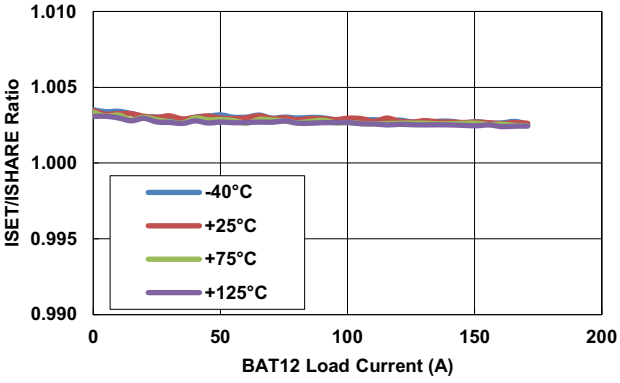


Figure 101. ISET/ISHARE Ratio vs Load Current in Buck/FPWM, +25°C, BAT48 = 48V, PD-Enabled

All the performance curves are taken from the Evaluation Board (ISL78224EVAL1Z) unless otherwise noted. All references to temperature are for the ISL78224 only. All other components are fan cooled with respect to room temperature. PD = Phase Drop. **(Continued)**

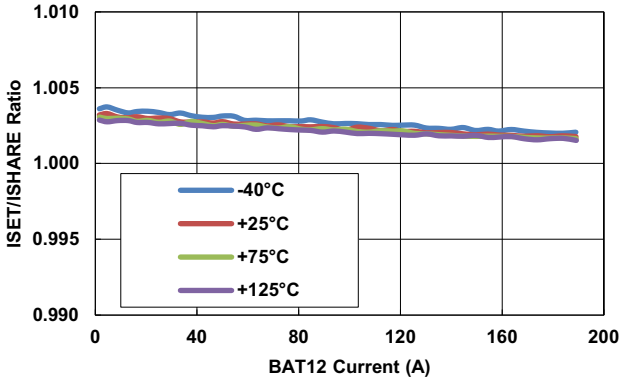


Figure 102. ISET/ISHARE Ratio vs BAT12 Current in Boost/DE/NO-PD

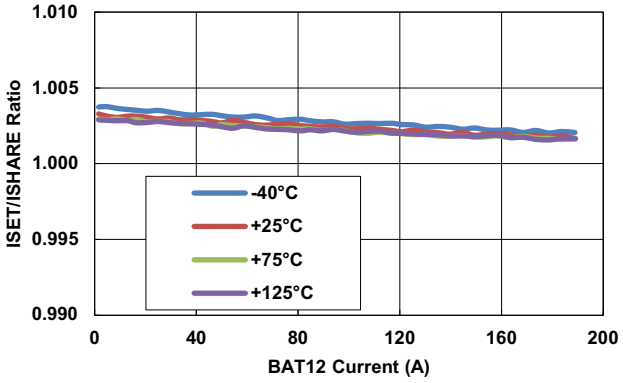


Figure 103. ISET/ISHARE Ratio vs BAT12 Current in Boost/FPWM/NO-PD

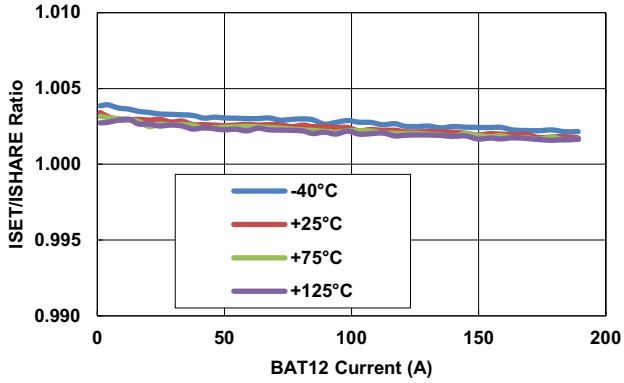


Figure 104. ISET/ISHARE Ratio vs BAT12 Current in Boost/DE/PD

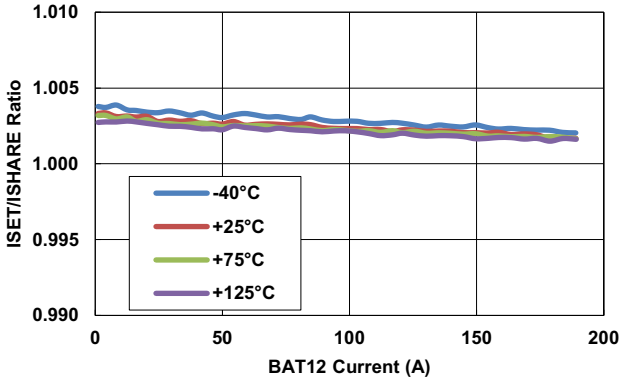


Figure 105. ISET/ISHARE Ratio vs BAT12 Current in Boost/FPWM/PD

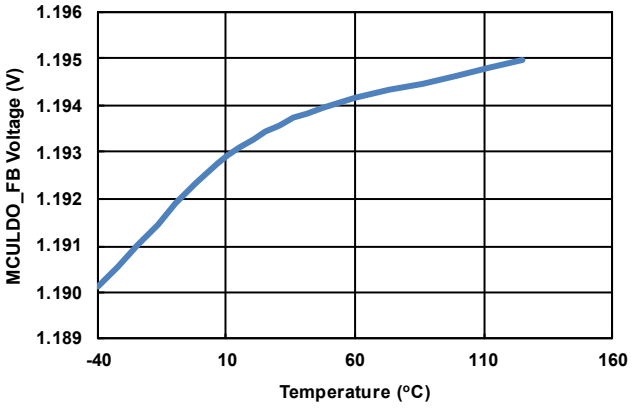


Figure 106. V_{MCULDO_FB}

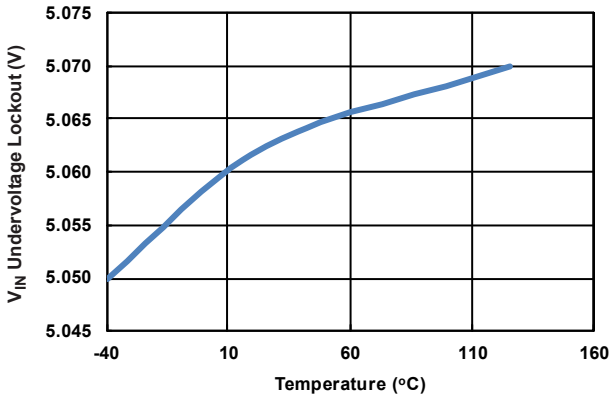


Figure 107. V_{IN} Undervoltage Lockout vs Temperature, Default Register Setting

All the performance curves are taken from the Evaluation Board (ISL78224EVAL1Z) unless otherwise noted. All references to temperature are for the ISL78224 only. All other components are fan cooled with respect to room temperature. PD = Phase Drop. **(Continued)**

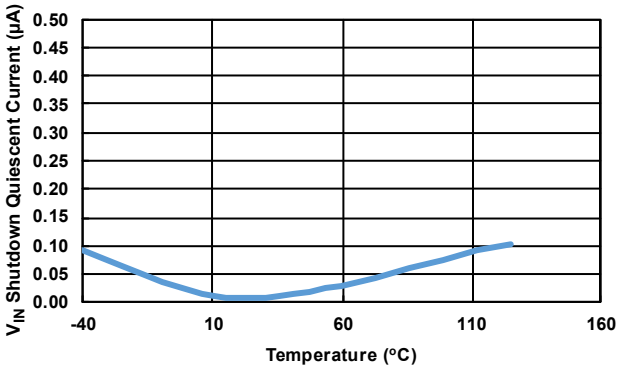


Figure 108. V_{IN} Shutdown Quiescent Current vs Temperature, Default Register Setting

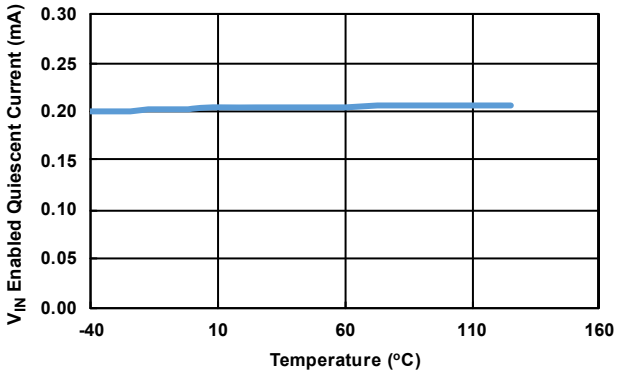


Figure 109. V_{IN} Enabled Quiescent Current vs Temperature, Default Register Setting

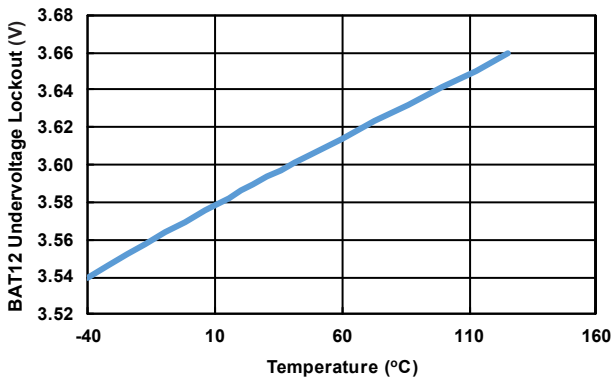


Figure 110. BAT12 Undervoltage Lockout vs Temperature, Default Register Setting

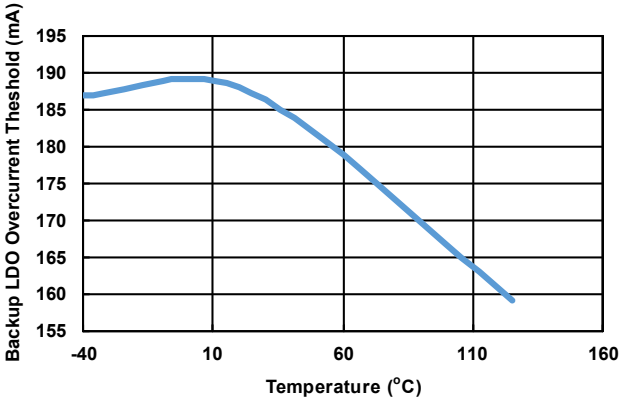


Figure 111. Backup LDO Overcurrent Threshold vs Temperature, Default Register Setting

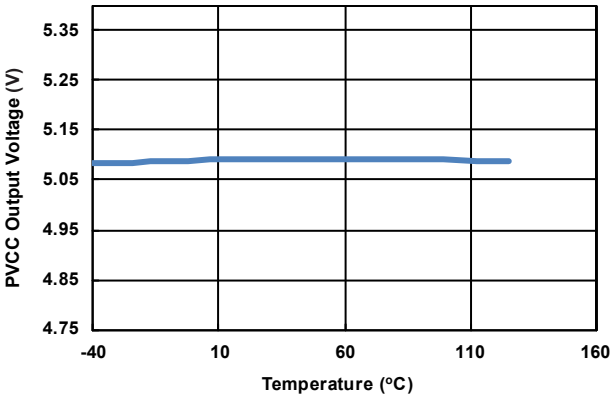


Figure 112. PVCC Output Voltage vs Temperature

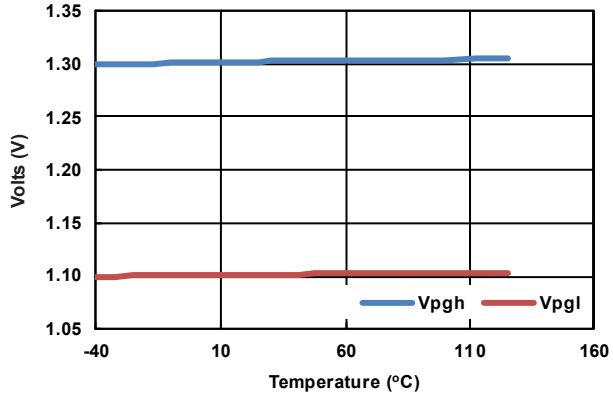


Figure 113. MCULDO_FB Power-Good Voltage Limits, High and Low (V)

All the performance curves are taken from the Evaluation Board (ISL78224EVAL1Z) unless otherwise noted. All references to temperature are for the ISL78224 only. All other components are fan cooled with respect to room temperature. PD = Phase Drop. **(Continued)**

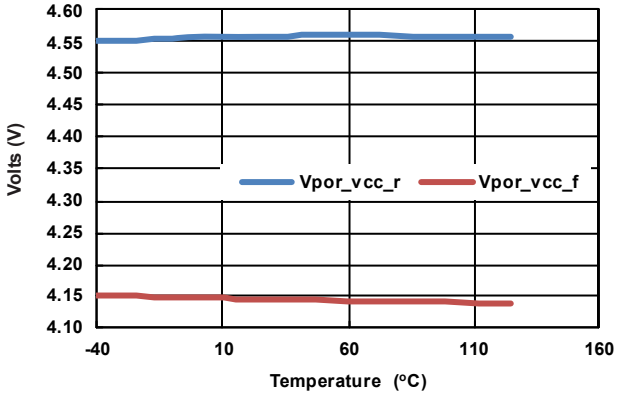


Figure 114. V_{CC} Power-On Reset Voltage, Rising and Falling

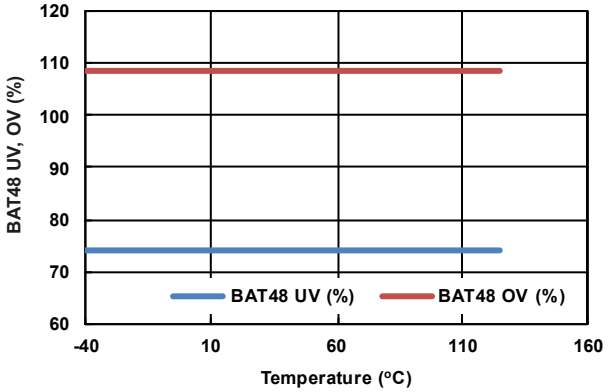


Figure 115. BAT48 UV and OV Warning Detection Threshold, Default Register Setting

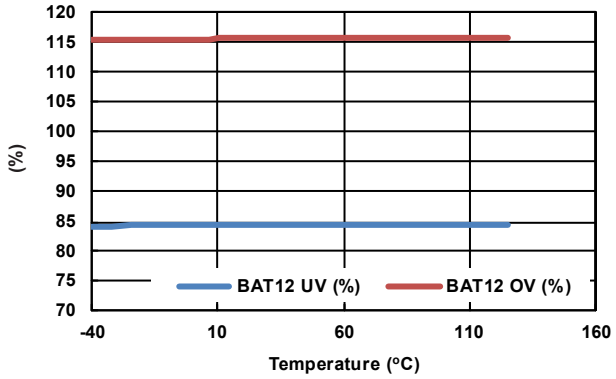


Figure 116. BAT12 UV and OV Warning Detection Threshold, Default Register Setting

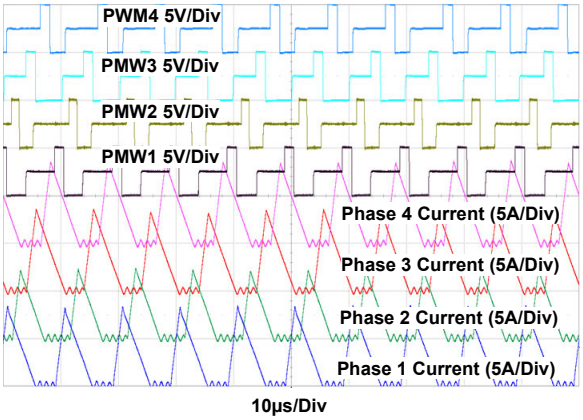


Figure 117. Steady-State Operation (Current) Waveform in Buck/DE/NO-PD/Light Load (5A)

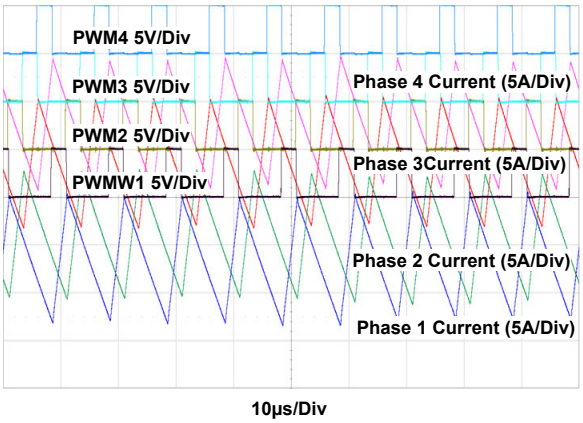


Figure 118. Steady-State Operation (Current) Waveform in BUCK/DE/NO-PD/Heavy Load (100A)

All the performance curves are taken from the Evaluation Board (ISL78224EVAL1Z) unless otherwise noted. All references to temperature are for the ISL78224 only. All other components are fan cooled with respect to room temperature. PD = Phase Drop. **(Continued)**

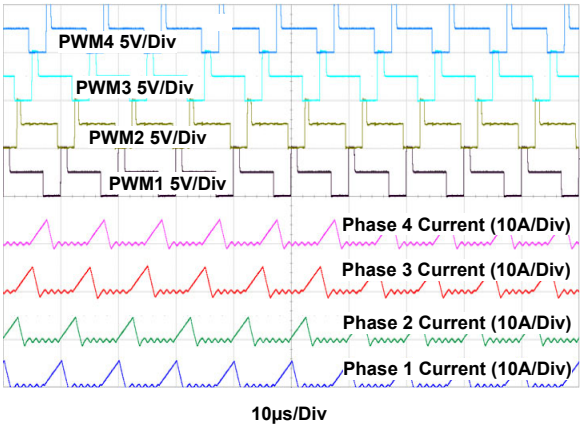


Figure 119. Steady-State Operation (Current) Waveform in Boost/DE/NO-PD/Light Load (1A)

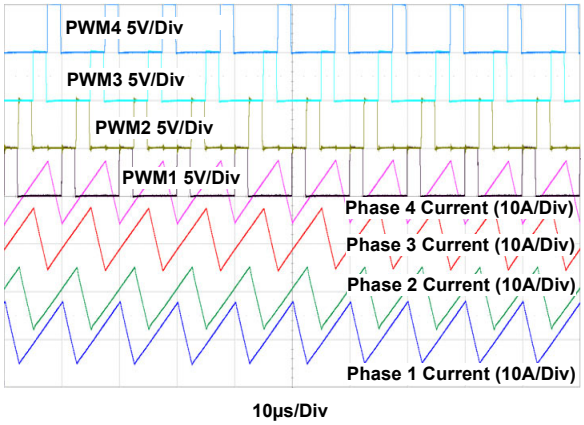


Figure 120. Steady-State Operation (Current) Waveform in Boost/DE/NO-PD/Heavy Load (20A)

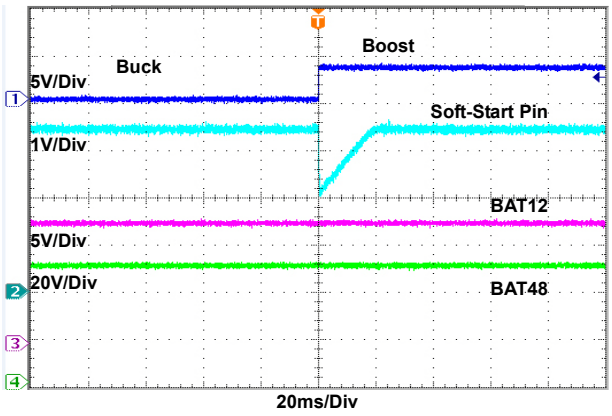


Figure 121. Buck to Boost

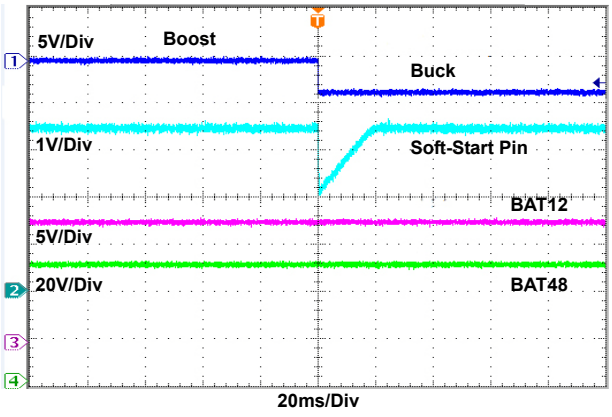


Figure 122. Boost to Buck

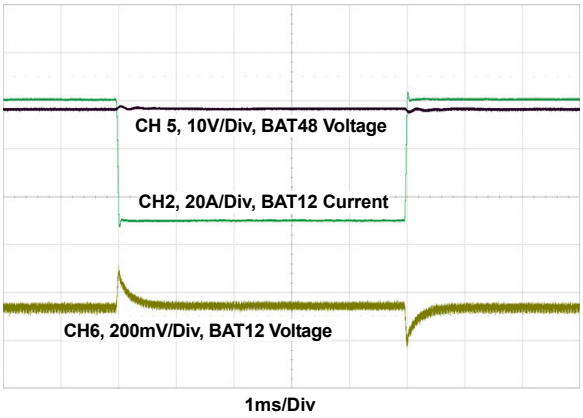


Figure 123. Buck Transient Response 100A to 200A, BAT48 Input ~48V

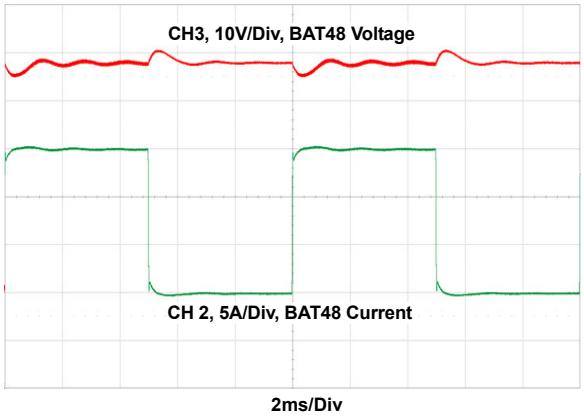


Figure 124. Boost Transient Response, 45A to 55A, BAT12 Input ~12V

All the performance curves are taken from the Evaluation Board (ISL78224EVAL1Z) unless otherwise noted. All references to temperature are for the ISL78224 only. All other components are fan cooled with respect to room temperature. PD = Phase Drop. **(Continued)**

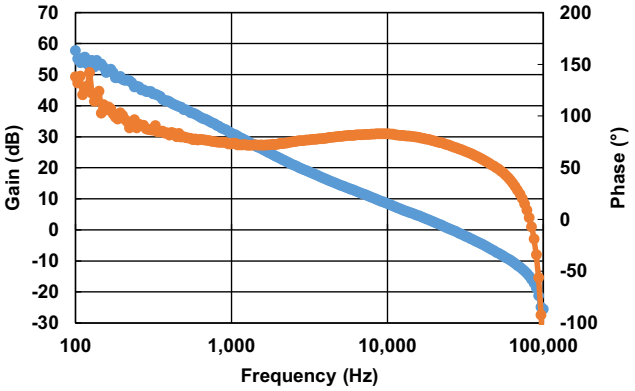


Figure 125. Buck Bode Plot, BAT48 Input = 48V, BAT12 Load at 100A

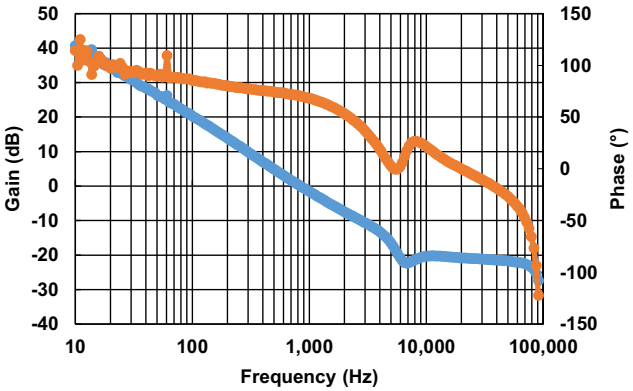


Figure 126. Boost Bode Plot, BAT12 Input = 12V, BAT48 Load at 42A

4. Operation Description

The ISL78224 is an automotive grade (AEC Q100 Grade-1) 4-phase synchronous bidirectional controller. This controller enables the configuration of a multiphase bidirectional power converter system between a 12V battery and a 48V battery with external FET drivers, N-channel power MOSFETs, and a few additional passive components. Typically, a converter system with a power rating of up to 3kW can be realized with the combination of driver ICs and adequately rated power MOSFETs. The device also supports parallel connection of up to four ISL78224 devices to realize up to 8-phase operation.

The ISL78224 also offers selectable phase dropping and a Diode Emulation mode for enhanced light-load efficiency.

The ISL78224 employs a constant frequency Peak Current Mode Control (PCMC) scheme, which offers the benefits of input voltage feed-forward regulation, a simpler loop compensator compared to voltage mode control, and inherent current sharing capability.

In addition to cycle-by-cycle current limiting, the ISL78224 has a dedicated average Constant Current (CC) control loop which enables accurate control of the average output current for Buck mode operation and average input current for Boost mode operation without shutdown. It enables the user to fully utilize the system's power device capability by accurately controlling constant input power.

The ISL78224 provides several system diagnostics and fault detection features including input/output overvoltage warning and protection, input/output undervoltage warning and protection, overcurrent warning and protection, and device status monitoring. The status of the device operation and faults are communicated to a host microcontroller in the system using a PMBus-compliant digital interface. This digital interface also provides access to useful system control parameters through internal registers.

The ISL78224 implements an internal LDO for stable device operation, an MCULDO for external MCU or other system power supply, and a Flyback controller to generate driver power supply and pre-regulated supply voltage for the device. These features support the minimization of effort and components in designing the required power supplies in the system.

Function details are described in the following sections.

4.1 Bidirectional Power Conversion

Due to the increase of electrical power demand in a vehicle and strong motivation for environmental and energy-saving requirements, a 48V battery system is considered a solution for next-generation vehicles in addition to the conventional 12V battery system. In this system, a multiphase bidirectional power converter between the batteries (a Buck converter from 48V to 12V, or a Boost converter from 12V to 48V) is required to supplement the power of each battery system. The ISL78224 enables the multiphase bidirectional power converter with one controller.

4.2 Multiphase Interleaving Control

For an n-phase, interleaved, multiphase converter, the PWM switching of each phase is distributed evenly with a 360/n phase shift. The total combined current ripples at the input and output are reduced where smaller input and output capacitors can be used. In addition, it is beneficial to have a smaller equivalent inductor for a faster loop response. In some applications, especially in high-current cases, multiphase operation allows smaller inductors for each phase rather than one large inductor (single-phase), which is sometimes more costly or unavailable on the market at the high-current rating. Smaller size inductors also help to achieve a low profile design.

The ISL78224 is a controller for a multiphase, interleaved converter which enables selection of 4-, 3-, and 2-phase operations. In 4-, 3-, and 2-phase operations, each phase operates with 90°, 120°, and 180° phase shift, respectively. This means that each PWM pulse is triggered 1/4, 1/3, and 1/2, respectively, of a cycle after the start of the PWM pulse of the previous phase. Figure 127 on page 57 illustrates the interleaving effect on input ripple current in 4-phase operation in Buck mode. The AC component of the 4-phase currents (I_{L1}, I_{L2}, I_{L3}, and I_{L4}) interleave each other and the combined AC current ripple (I_{Ltotal}) at input is reduced. Equivalently, the frequency of the AC inductor ripple at the input is four times that of the switching frequency per phase. Figure 128 on page 57 is an oscillogram of individual inductor currents and total inductor current when the ISL78224 is being run with four phases. The top trace is total inductor current.

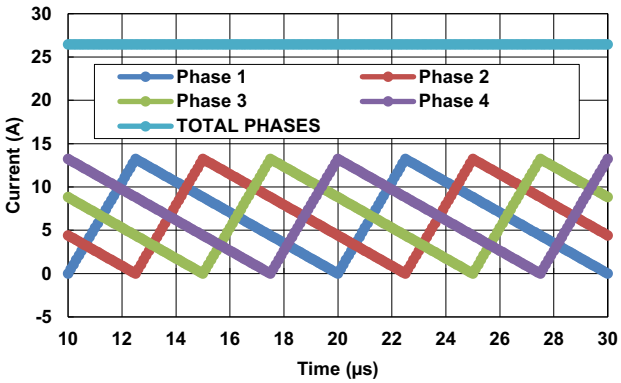


Figure 127. Total and per Phase Inductor Ripple Current

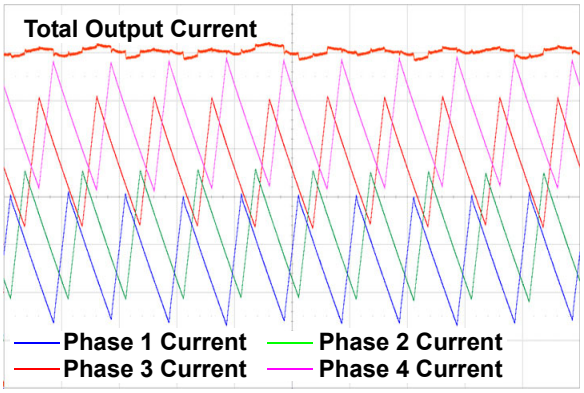


Figure 128. Measured per Phase Inductor Current and Total Output Current for a 4-Phase Converter, BAT12 = 50A

4.3 Oscillator and Clock Synchronization

The switching frequency is determined by the selection of the frequency-setting resistor, R_{FSYNC}, connected from the FSYNC pin to GND. Equation 1 provides assistance in selecting the correct resistor value.

(EQ. 1) $$R_{FSYNC} = 4.6x10^{9}x\left(\frac{1}{f_{SW}} - 9.2X10^{-8}\right)$$

where f_{SW} is the switching frequency of each phase in Hz.

Figure 129 shows the relationship between R_{FSYNC} and switching frequency.

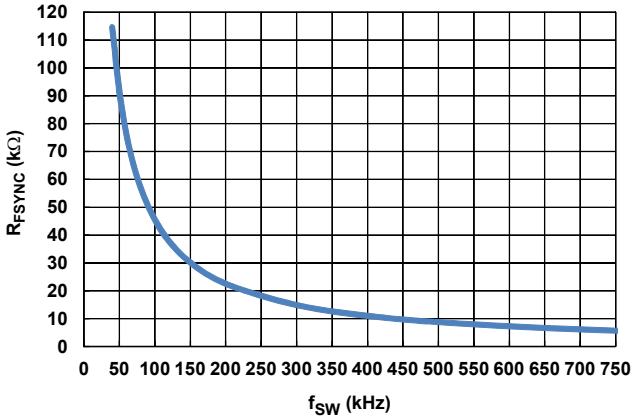


Figure 129. R_{FSYNC} vs Switching Frequency

The maximum frequency at each PWM output is 750kHz. If the FSYNC pin is accidentally shorted to GND or connected to a low impedance node, the internal circuits detect this fault condition and the ISL78224 stops switching and reports to the corresponding status register.

The ISL78224 contains a Phase-Lock Loop (PLL) circuit and has frequency synchronization capability by simply connecting the FSYNC pin to an external square pulse waveform (typically 20% to 80% duty cycle). In normal operation, the external synchronizing frequency needs to be at least 20% faster than the internal oscillator frequency setting. The ISL78224 synchronizes its switching frequency to the fundamental frequency of the input waveform. The frequency synchronization feature synchronizes the rising edge of the PWM1 clock signal with the rising edge of the external clock signal at the FSYNC pin.

The PLL is compensated with a series resistor-capacitor (R_c and C_c) from the PLL_COMP pin to GND and a capacitor (C_p) from PLL_COMP to GND. Typical values are R_c = 3.24kΩ, C_c = 6.8nF, and C_p = 1nF. The typical lock time is around 0.5ms.

The CLK_OUT pin provides a rectangular pulse waveform at the switching frequency. The amplitude is 5V with approximately 40% positive duty cycle, and the rising edge is synchronized with the leading edge of PWM1.

4.4 Output Voltage Regulation Loop

The resistor divider R_{FB2BK} and R_{FB1BK} from BAT12 to FB_BK, and the resistor divider R_{FB2BT} and R_{FB1BT} from BAT48 to FB_BT can be selected to set the desired output voltage for Buck converting and Boost converting, respectively. The BAT12 output voltage V_{BAT12} in Buck mode and BAT48 output voltage V_{BAT48} in Boost mode can be calculated by Equations 2 and 3, respectively.

(EQ. 2) $$V_{BAT12} = V_{REF} \cdot \left(1 + \frac{R_{FB2BK}}{R_{FB1BK}}\right)$$

(EQ. 3) $$V_{BAT48} = V_{REF} \cdot \left(1 + \frac{R_{FB2BT}}{R_{FB1BT}}\right)$$

The V_{REF} can be either the voltage of the soft-start ramp (V_{SS}), the converted digital tracking reference or an analog tracking reference voltage (V_{REF_TRK}), or the internal system reference voltage (V_{REF_BG}). The error amplifier (Gm) uses the lowest value among V_{SS}, V_{REF_TRK}, and V_{REF_BG}. The V_{SS}, V_{REF_TRK}, and V_{REF_BG} are valid for Gm during and after soft-start. In general operation, V_{REF_TRK} and V_{REF_BG} are normally HIGH before soft-start and V_{SS} normally ramps up from a voltage lower than V_{REF_TRK} and V_{REF_BG}, so V_{SS} controls the output voltage ramp-up during soft-start. After soft-start is complete, the output voltage is controlled by V_{REF_BG} or V_{REF_TRK} which sets the desired voltage.

4.5 Peak Current Mode Control

Figure 127 on page 57 shows the timing diagram of each phase operation for a 4-phase operation. Each phase's PWM operation is initiated by the fixed clock for each phase from the oscillator. The initiation clock for each phase is separated by 90°. In Buck mode, the ISL78224 provides a high-side MOSFET turn-on timing signal to the driver based on the initiation clock timing. At the beginning of the PWM cycle, the driver turns on the high-side MOSFET and, the inductor current ramps up after a preset dead time delay. The ISL78224's Current-Sense Amplifiers (CSA) sense each phase inductor current and generates the current-sense signal I_{SENx}. The I_{SENx} is added with the compensating slope and generates V_{RAMPx}. When V_{RAMPx} reaches the error amplifier (Gm) output voltage, the PWM comparator generates the high-side MOSFET turn-off timing and the low-side turn on signal for the driver. Following the high-side turn-off/low-side turn-on timing signal, the driver turns off the high-side MOSFET immediately and turns on the low-side synchronous MOSFET after the preset dead time. The high-side MOSFET stays off until the next clock signal comes for the next PWM cycle. The turn-off timing of the low-side MOSFET is determined by either the PWM turn-on time at the next PWM cycle or when the inductor current becomes zero in Diode Emulation mode.

4.6 3-State PWM Control Output

Diode Emulation (DE) mode can be used to turn off the synchronous Buck or Boost MOSFETs when the inductor current goes to zero. Efficiency is enhanced by not allowing negative current to flow "backwards" in the inductor during the off time. The ISL78224 can employ a 3-state PWM control output. The high level PWM output commands the high-side power MOSFET to turn on, the low level PWM output commands the low-side power MOSFET to turn on, and the middle level (2.5V typical) commands both high-side and low-side power MOSFETs to turn off. The ISL78420 with a 3-state PWM input is a recommended driver to realize this efficient converter system.

4.7 2-State PWM Control Output

Forced PWM is realized if 2-state PWM output is commanded, that is, high and low level outputs only. Forced PWM is optimal for asynchronous operation or cases requiring continuous switching. Select the 2-state PWM

output by setting the PWM_TRI pin low. In this case, the PWM outputs indicate the on/off timing of the main switching MOSFETs.

When using two-level PWM outputs (PWM_TRI = 0), ensure the system starts up smoothly in the presence of pre-biased outputs. Typically, in this case, only the main FET should be switched, preventing negative current out of the pre-biased output during the synchronous phase. However, with two-level PWM outputs, it is not possible to run in non-synchronous fashion. Therefore, Renesas recommends disabling the synchronous FETs during the soft-start period when using two-level PWM outputs. Alternatively, the entire converter can operate asynchronously at all times.

4.8 Boot Refreshing

At system start-up or when restarting the dropped phase, the boot capacitor of the external driver can be discharged. In Buck mode with DE mode selected, this condition can cause a high-side MOSFET turn-on issue due to insufficient gate drive voltage. To charge the Boot capacitor, the low-side MOSFET needs to turn on. However, because the high-side MOSFET is not turned on, the low-side MOSFET cannot turn on and, therefore, the Boot capacitor cannot be charged. To prevent this issue, the ISL78224 has a boot refreshing feature for operating in Buck mode with DE mode selected.

At device start-up, the ISL78224 provides boot refresh pulses that force low-side MOSFET turn-on for a limited duration with limited pulse count. By default, the ISL78224 provides eight low-side MOSFET turn-on pulses with the duration of 1/12 switching cycle. The low-side MOSFET on duration can be changed to 1/6 cycle and the pulse count can be changed to 16 pulses by an external microcontroller from the I^2C/PMBus. While the boot refreshing pulses are provided, the phase shift between the phases is kept as normal switching. Refer to Register 0xEC, Boot Refresh Control Register, in the "Boot Refresh Control Register (0xEC)" on page 105 for more information.

If a phase is dropped due to a light-load condition, the ISL78224 provides boot refreshing pulses periodically for the dropped phase (or phases). After the first phase drop is detected, the device starts an internal counter. When the counter reaches the defined time duration, the device provides boot refreshing pulses to the dropped phase, maintaining the proper phase shift timing. The default boot refresh pulse count is four pulses and the default low-side MOSFET on duration is 1/12 cycle. The boot refresh pulse count during the phase drop condition can be changed to eight pulses and the low-side MOSFET on duration can be changed to 1/6 cycle. Refer to Register 0xEC, Boot Refresh Control Register, in the "Boot Refresh Control Register (0xEC)" on page 105 for more information.

At a very light-load condition, the device may move into pulse skipping operation. In this case, as with phase dropping, the ISL78224 provides the boot refreshing pulses to all the phases. The interval of boot refreshing, pulse count, and pulse width are the same as that of phase dropping.

4.9 Current Sharing between Phases

The peak current mode control inherently has current sharing capability. As shown in Figure 131 on page 63, the current-sense ramp, V_{RAMPx}, of each phase is compared to the same error amplifier's output at the COMP pin by the PWM comparators to turn off the high-side MOSFET when V_{RAMPx} reaches the COMP voltage. Thus, the V_{RAMPx} peaks are controlled to be the same for each phase. V_{RAMPx} is the sum of the instantaneous inductor current-sense ramp and the compensating slope. Because the compensating slopes are the same for all of the active phases, the inductor peak current of each phase is controlled to be the same.

The same mechanism applies to the case when multiple ISL78224s are configured in parallel for multiphase bidirectional converter. The COMP pin of master ISL78224 is tied to each phase's current-sense ramp peak to be compared with the same COMP voltage, meaning the inductor peak current of all the phases are controlled to be the same.

The peak current control scheme works well for sharing current in most cases. However, if the inductance variation is large, the power converting of each phase may not be well-controlled. To provide better current balancing, the ISL78224 has the option to control the average current of each phase. The device averages the current of each phase and adds the error information between the overall averaged current and average current of each phase to the ramp signal.

4.10 Tracking

The ISL78224 has a TRACK input feature, which enables the user to provide the reference voltage to change the output voltage.

The default input for the TRACK is a digital signal (Digital Tracking), which enables control of the output voltage based on the duty ratio of an input digital pulse. This can be overridden with analog signal input (Analog Tracking) by changing the ATRAK/DTRAK control register bit (0xb0: [4]) to 1, refer to "Control Register 1 (0xB0)" on page 79).

Figures 6 and 7 show the TRACK function block diagram. VREF_TRK is fed into Gm1 as one of the reference voltages. The Gm1 takes the lowest voltage of SS, VREF_TRK, and VREF as the actual reference. When VREF_TRK is the lowest voltage, it is used as the actual reference voltage for Gm1 and the output voltage is adjusted with the TRACK signal changes. Under the default configuration, the VREF_TRK voltage can take 0.8V or higher voltage. The lower voltage limit is constrained by the minimum input or output undervoltage limit which is set inside the device at 50% of the input or output target voltage. If the input or output undervoltage limit function is ignored by overriding the corresponding individual fault control registers, the user can set the VREF_TRK to lower than 0.8V. However, in this case, the input or output undervoltage limit fault response is flagging only and no hiccup or latch-off function is performed, even if the output or input voltage becomes lower than 50% of their target.

Because the Gm1 takes the lowest voltage of SS, VREF, and VREF_TRK, the maximum effective range for VREF_TRK is determined by the SS or VREF voltage, whichever is lower. For example, after soft-start, when the SS = 3.4V (typical) and VREF = 1.6V (default), the maximum effective voltage for VREF_TRK is 1.6V (refer to Figure 21 on page 37).

By default, the TRACK pin is configured as a digital input (digital tracking). The average duty of a digital PWM signal applied to the TRACK pin is converted to the VREF_TRK. Equation 4 describes the relation between VREF_TRK voltage and duty of the input digital PWM pulse. A 2-stage RC filter is prepared inside the device to filter the digital pulses to the analog VREF_TRK voltage.

(EQ. 4) $$V_{REFTRK} = 2.5 \cdot D$$

The PWM signals' amplitude at the TRACK pin does not affect the VREF_TRK accuracy. Only the duty cycle value changes the VREF_TRK value. The built-in low-pass filter converts the PWM signal's duty cycle value to a low noise reference. The low pass filter has a cutoff frequency of 1.75kHz and a gain of -80dB at 200kHz. This does not affect the output voltage because of the limited bandwidth of the system. A 400kHz frequency is recommended for the PWM signal at the TRACK pin. A minimum 200kHz frequency at the TRACK input is possible, but VREF_TRK has a higher AC ripple. A bench test evaluation is needed to make sure the output voltage is not affected by this VREF_TRK AC ripple. Refer to Figures 24 and 25 on page 38.

Digital tracking is the default setting of the device; however, the user can select the analog tracking function. When setting the ATRK_DTRK control register (0xB0:[4] = 1) through the PMBus, the internal MUX connects the TRACK pin voltage to the input of the 2-stage RC filter R1/C1/R2/C2 (see "Control Register 1 (0xB0)" on page 79). In this way, the TRACK pin accepts analog signal inputs, with the Gm's VREF_TRK input equal to the voltage on the TRACK pin. It has the same low-pass filter with a cutoff frequency of 1.75kHz.

If the TRACK pin is not used, leave it floating or tied to VCC with the internal VREF working as the reference.

The TRACK function is enabled before the SS pin soft-start. Therefore, the VREF_TRK can be controlled by TRACK inputs at start-up.

The converter's control loop bandwidth limits the maximum reference's (VREF_TRK) transition speed, sympathetically limiting the output voltage tracking rate. Generally, the tracking reference signal's frequency should be 10 times lower than the Boost loop crossover frequency. Otherwise, the Boost output voltage cannot track the tracking reference signal and the output voltage is distorted.

4.11 Current Sense

The ISL78224 peak current control architecture senses the inductor current of each phase continuously for fast response. A sense resistor (shunt) is placed in-series with the power inductor for each phase. The ISL78224 Current-Sense Amplifiers (CSA) continuously sense the respective inductor current (as shown in Figure 130) by sensing the voltage signal across the sense resistor R_{SENx} (where "x" indicates the specific phase number and same note applied throughout this document). The sensed current for each active phase is used for peak current mode control loop, phase current balance, individual phase cycle-by-cycle peak current limiting (OC1), individual phase overcurrent fault protection (OC2), averaged Constant Current Limit (CCL) control, Average Overcurrent Protection (AOCP), Diode Emulation (DE), and Phase Drop/Add control. The internal circuitry shown in Figure 130 represents a single phase and is repeated for each phase.

Place the current-sense resistor (R_{SENx}) at the non-switching side (BAT12 side) of the inductor, that is, the output side of the inductor in Buck mode and the input side of the inductor in Boost mode. Connect the ISENxA pin to the BAT12 side (output side in Buck mode and input side in Boost mode) and the ISENxB pin should be connected to the inductor side of the current-sense resistor.

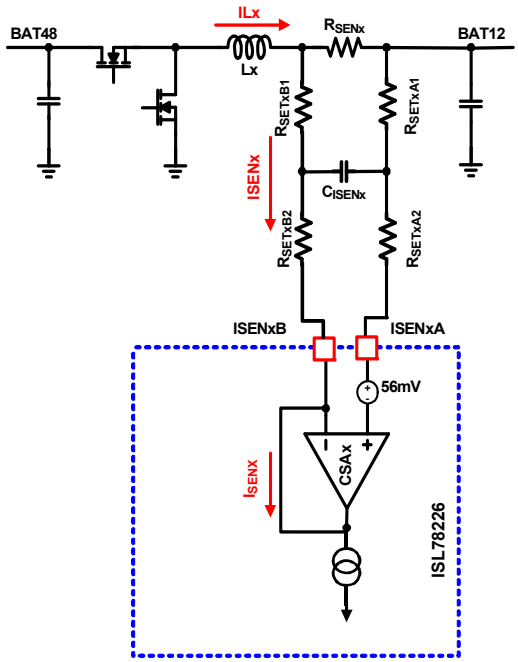


Figure 130. Current-Sensing Block Diagram for Individual Phase I_{SENX}

The recommended configuration of the RC network between the R_{SENx} and ISENxA/ISENxB pins is shown in Figure 130. The current gain setting resistor, R_{SETxB}, is R_{SETxB1} plus R_{SETxB2} in Figure 130. That sum should be fixed at 1kΩ for equal boost and buck current indications at IMON.

(EQ. 5) $$R_{SETx} = R_{SETxA} = R_{SETxB} = R_{SETxB1} + R_{SETxB2}$$

Renesas recommends that $R_{SETxA} = R_{SETxB}$ and that all four resistors are as equal in value as standard values allow. Insert a capacitor, C_{ISENX}, between them as shown in Figure 130. This forms a symmetric noise filter for the small current-sense signals. The differential filtering time constant equals $(R_{SETxA1}+R_{BIASxB1})*C_{ISENx}$. This time constant is typically selected in the range of tens of ns depending on the actual noise levels.

To detect the bidirectional current signal, CSA has -56mV internal series offset voltage to its non-inverting input, which enables changing the polarity of the input signal between Buck mode and Boost mode. Therefore, to balance the zero current point properly, the total resistor value of R_{SETx} needs to be set to 1kΩ in the application circuit. With this setting, the CSA output current, I_{SENx}, is proportional to each phase inductor current, I_{Lx}, after

consideration of a 56µA offset and enables detection of both positive and negative direction current at the inductor. I_{SENx} per phase can be derived in Equation 6, where I_{Lx} is the per-phase current flowing through R_{SENx}.

(EQ. 6)
$$I_{CSAxOUT} = (56mV + I_{Lx} \bullet R_{SENx})/R_{SETx}, \text{ for Buck mode}$$
$$I_{CSAxOUT} = 112\mu A - (56mV - I_{Lx} \cdot R_{SENx})/R_{SETx}, \text{ for Boost mode}$$

Recommendations for using R_{SETx} values other than 1.00kΩ are described in "Current Monitoring — IMON" on page 62. This allows for the use of R_{SEN} resistor values that are more commonly available as shunts.

R_{SEN} and R_{SET} resistor values must be selected by considering the desired cycle-by-cycle peak current limiting level OC1.

4.12 Current Monitoring — IMON

The ISL78224 continuously monitors the inductor current of each phase, I_{Lx}, at the current sense resistor R_{SEN}, of each phase. An R_{SEN} shunt is connected in series with the inductor of each of the individual phases. A current, which is a function of the inductor current of each phase, is added to the total output current of the IMON pin. By connecting an RC filter network at the IMON pin, the voltage at the IMON pin reflects a filtered replica of the total inductor currents. This is the output current for Buck mode and the input current for Boost mode. Equation 7 shows the relationship between the I_{IMON} pin output current and the buck regulator BAT12 output current during Buck mode operation.

(EQ. 7)
$$I_{IMON} = \frac{4 \cdot 56mV + I_{BUCKOUTPUT} \cdot R_{SEN}}{2 \cdot R_{SET}}$$

I_{IMON} = Output Current from the IMON pin

$I_{BUCKOUTOUT}$ = Total output current of buck regulator

R_{SEN} = Sense resistor value

R_{SET} = Gain setting resistor value

Equation 8 shows the relationship between the I_{IMON} pin output current and the boost regulator output current during boost mode operation.

(EQ. 8)
$$I_{IMON} = \frac{4 \cdot \left(112\mu A - \frac{56mV}{R_{SET}}\right) + I_{BOOSTINPUT} \cdot \frac{R_{SEN}}{R_{SET}}}{2}$$

$I_{BOOSTINPUT}$ = Total input current of boost regulator

Use a 1.00kΩ R_{SET} resistor if buck and boost modes are required to have equal I_{IMON} current for equal inductor current. In general, this is not required if buck and boost IMON currents are not required to track each other.

The IMON voltage V_{IMON} is the function expressed by Equation 9 for the output current in Buck mode or for the input current in Boost mode.

(EQ. 9)
$$V_{IMON} = R_{IMON} \cdot I_{IMON}$$

R_{IMON} is the value of the resistor connected from the IMON pin to GND. Because the IMON voltage V_{IMON} is used for the Constant Current Control Loop (CCL), Average Current Limit (ACL) control, and Phase Drop/Add control, it is recommended to use a 0.1µF to 1µF ceramic filter capacitor from IMON to GND to filter out the ripple at the IMON pin.

Refer to "Average Constant Current Control Loop (CCL)" on page 66, "Average Overcurrent Protection (AOCP)" on page 75, and "Automatic Phase Dropping/Adding" on page 64 for more information about these functions.

4.13 Adjustable Slope Compensation

For a converter with peak current mode control, slope compensation is needed when the duty cycle is larger than 50%. Renesas recommends adding slope compensation when the duty cycle is approximately 30% to 40%, becuase a transient load step can push the duty cycle higher than the steady state level. When slope compensation is too low,

the converter suffers from subharmonic oscillation, which may result in noise emissions at half the switching frequency. On the other hand, overcompensation of the slope may reduce the phase margin. Therefore, proper design of the slope compensation is needed.

The ISL78224 features adjustable slope compensation by setting the resistor value R_{SLP_BT} and R_{SLP_BK} from the SLOPE_BT and SLOPE_BK pins to ground, for Boost and Buck mode, respectively.

Figure 131 on page 63 shows the block diagram related to slope compensation. For current mode control, the compensation slope slew rate, m_{SL}, theoretically needs to be larger than 50% of the inductor current down ramp slope slew rate m_b.

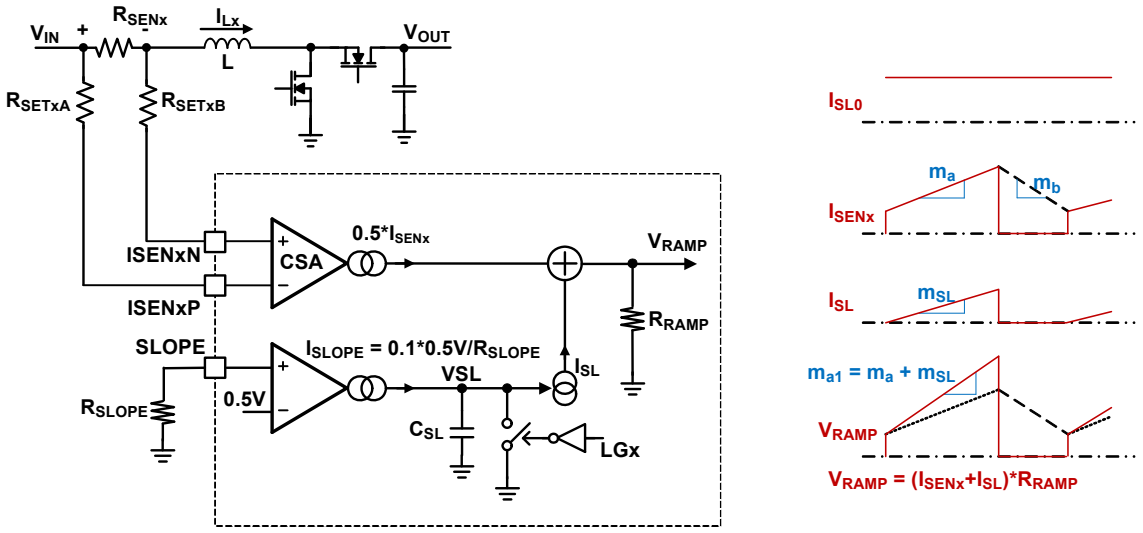


Figure 131. Slope Compensation Block Diagram

Equations 10 and 11 show the resistor value, R_{SLPBT} and R_{SLPBK}, at the SLOPE pin to create a compensation ramp for Boost and Buck modes.

$$R_{SLPBT} = \frac{2.14 \cdot 10^5 \cdot L_x \cdot R_{SETx}}{K_{SLOPE} \cdot (VOUT\_MAX - VIN\_MIN) \cdot R_{SENx}} (\Omega) \quad \text{(EQ. 10)}$$

$$R_{SLPBK} = \frac{2.14 \cdot 10^5 \cdot L_x \cdot R_{SETx}}{K_{SLOPE} \cdot VOUT\_MAX \cdot R_{SENx}} (\Omega) \quad \text{(EQ. 11)}$$

where K_{SLOPE} is the selected gain of compensation slope over inductor down slope. For example, $K_{SLOPE} = 1$ gives the R_{SLOPE} value generating a compensation slope equal to inductor current down ramp slope. Theoretically, the K_{SLOPE} needs to be larger than 0.5, but practically more than 1.0 is used as shown in Equation 10 for Boost mode with a maximum of V_{OUT} and a minimum of V_{IN}, and in Equation 11 for Buck mode with a maximum of V_{OUT}.

4.14 Light-Load Efficiency Enhancement

For switch mode power supplies, the total loss is related to conduction loss and switching loss. At heavy load, the conduction loss dominates, while the switching loss dominates at light-load. Therefore, if a multiphase converter is running at a fixed phase number for the entire load range, the efficiency starts to drop significantly below a certain load current. The ISL78224 has selectable automatic phase dropping. The cycle-by-cycle diode emulation and the pulse skipping features serve to enhance the light-load efficiency. By observing the total output current in Buck mode and input current in Boost mode on-the-fly, and dropping under utilized active phases, the system can achieve optimized efficiency over the entire load range.

4.14.1 Diode Emulation at Light-Load Condition

Use the MODE pin to select Diode Emulation (DE) mode or Forced PWM (FPWM or CCM) mode. When the MODE pin is connected to GND directly or a 68kΩ (typical) resistor is connected from the MODE pin to GND, DE mode is activated. If the MODE pin is connected to VCC directly, or a 33kΩ (typical) resistor is connected from the MODE pin to GND, Forced PWM mode is activated.

The MODE pin consolidates the selection of switching mode (DE mode or FPWM mode) and fault response (hiccup or latch-off).

Refer to the "Switching Mode and Fault Response Selection" on page 76 for details about MODE pin settings.

When DE mode is enabled, the ISL78224 has cycle-by-cycle diode emulation operation at light load and achieves Discontinuous Conduction Mode (DCM) operation. With DE mode operation, negative inductor current is prevented and the conduction loss is reduced, therefore, high efficiency can be achieved at light-load conditions.

4.14.2 Pulse Skipping at Deep Light-Load Condition

If the converter enters DE mode and the load is still reducing, eventually pulse skipping occurs to increase the deep light-load efficiency. Either one enabled phase or a combination of phases pulse skips at these deep light-load conditions.

4.14.3 Automatic Phase Dropping/Adding

To enhance the light-load efficiency, the ISL78224 has an Adjustable Automatic Phase Dropping/Adding option. Only the master device controls phase adding/dropping. The slave devices follow the phase dropping/adding decision made by the master device.

Phase dropping is available only when the tri-state driver is used. If PWM_TRI is low, phase dropping related signals are ignored and all phases are active.

The PD_CTRL pin controls enabling or disabling the phase dropping feature, and phase dropping/adding threshold. The phase dropping function can be enabled by connecting the appropriate resistor from PD_CTRL to GND. By connecting PD_CTRL pin to VCC or leaving it floating, the phase dropping function is disabled.

When the phase drop function is enabled, the ISL78224 automatically drops or adds phases by comparing the voltage at the IMON pin (VIMON) to the phase dropping/adding thresholds. These thresholds are determined by the resistor value connected from PD_CTRL pin to GND, where V_{IMON} is proportional to the average output current in Buck mode or average input current in Boost mode.

4.14.3.1 Phase Dropping/Adding at Master Device

If the PD_CTRL pin of the master device is connected to VCC, the Adjustable Automatic Phase Dropping/Adding function is disabled and the device operates with its maximum phase count.

If a resistor (R_{PDCTRL}) is connected between PD_CTRL of the master device and GND, and the voltage at the PD_CTRL pin (V_{PDCTRL}) is lower than its disable threshold of 4V, the Adjustable Automatic Phase Dropping/Adding function is enabled. When the ISL78224 controller works in this mode, it automatically adjusts the active phase number by comparing the voltage at IMON pin (V_{IMON}), which is proportional to the total output current, to the threshold voltage defined by the PD_CTRL voltage. The PD_CTRL pin sources a constant 40µA current to the resistor (R_{PDCTRL}), which is connected to this pin and generates the reference voltage (V_{PDCTRL}) to determine the threshold(s) of phase dropping and adding. The threshold to determine how many phases are in operation is dependent on two factors:

(1) The maximum configured phase number.

(2) The voltage on the IMON pin (V_{IMON}) and the voltage at the PD_CRTL pin (V_{PDCTRL}).

The phase adding threshold is defined as follows:

• $V_{PDCTRL} = 40\mu A * R_{PDCTRL}$

If the maximum phase count is configured as 4-phase:

• 3- to 4-phase add when V_{IMON} increases to = 89% of V_{PDCTRL} (typical)

• 2- to 3-phase add when V_{IMON} increases to = 86% of V_{PDCTRL} (typical)

If the maximum phase count is configured as 3-phase:

• 2 to 3-phase add when V_{IMON} increases to = 89% of V_{PDCTRL} (typical)

If PWM_TRI is tied to VCC, the PWM output of the dropped phases is 2.5V. The external driver has to identify this tri-state signal and turn off both the low-side and high-side switches accordingly. For better transient response during phase dropping, the ISL78224 gradually reduces the duty cycle of the dropping phase from steady state to zero, typically within 15 switching cycles. This gradual dropping scheme helps with a smooth change of the PWM signal and, in turn, helps stabilize the system when phase dropping happens.

The ISL78224 also has an automatic phase adding feature similar to phase dropping. When adding a phase, the required adding phases are added instantly to take care of the increased load condition. The phase adding scheme is controlled by three factors.

(1) The maximum configured phase number

(2) The voltage at the IMON pin (V_{IMON}) and the PD_CRTL pin (VPDCTRL) voltage

(3) Individual phase peak current

Factors 1 and 2 are similar to the phase dropping scheme. If the V_{IMON} is higher than the phase dropping threshold plus the hysteresis voltage, the dropped phase are added back one by one instantly.

The above mentioned phase-adding method is sufficient in cases in which the load current increases slowly. However, if the load is increasing quickly, the IC uses a different phase adding scheme. The ISL78224 monitors the individual channel current for all active phases. If any of the phase's sensed currents hit 80% of OC1 level, all the phases are added back instantly.

After a fixed 1.5ms delay, the phase dropping circuit is reactivated and the system reacts by dropping the phase number to the correct value.

During phase adding, when either phase hits 80% of OC1, 200µs blanking time occurs so that per-channel Overcurrent Protection (OC2) is not triggered during this blanking time.

4.14.3.2 Phase Dropping/Adding at Slave Device

If multiple ISL78224 parts are connected in parallel, the master device makes the phase dropping/adding decision and the slave devices synchronize to the action of the master device.

The PD_0 and PD_1 pins control the phase dropping of slave devices. On the master device, PD_0 and PD_1 are configured as outputs and are connected to the slave devices' pins, respectively. On the slave device, PD_0 and PD_1 are configured as inputs and follow the phase dropping/adding determined by the master device.

Table 2 on page 65 shows the relation between PD_0, PD_1, and dropping phases.

Table 2. Master/Slave Phase Drop Communicationm

PD_0	PD_1	Active Phase Count
M (1/2 VCC)	H	4 phases
L	H	3 phases (Drop Phase 4)
H	L	2 phases (Drop Phase 4 and 3)
L	L	(Phase drop is disabled)

4.15 Average Current Control

4.15.1 Average Constant Current Control Loop (CCL)

To control the output voltage constant in normal PWM operation, the PWM pulse is terminated when the ramp voltage that is proportional to the sensed peak current reaches the error amplifier control voltage. However, in some applications, such as charging a battery, a constant output current control may be desired instead of output voltage control. To support such requirements, a dedicated, average constant Current Control Loop (CCL) is implemented on the ISL78224 to control the average output current in Buck mode and average input current in Boost mode to be constant.

As described in "Current Monitoring — IMON" on page 62, the V_{IMON} represents the average input or output current in boost or buck operation, respectively. This V_{IMON} is sent to the error amplifier Gm2 input to be compared with the internal CC reference V_{REF_CC}, which is 2.4V as default and can be programmed to different values by setting the CCL Threshold Control Register (0xED[2:0]) with I^2C/PMBus. This is shown in Figures 6 and 7. The Gm2 output drives the COMP voltage through diode D_{CC}. Thus, the COMP voltage can be controlled by either the Gm1 output or Gm2 output through D_{CC}.

When V_{IMON} is lower than the V_{REF_CC}, the Gm2 output is kept high, close to VCC level, and D_{CC} is blocked and not forward-conducting. In this condition, the COMP voltage is controlled by the voltage loop error amplifier Gm1's output to have output voltage regulated.

If V_{IMON} reaches V_{REF_CC}, the Gm2 output falls, D_{CC} is forward-conducting, and the Gm2 output overrides the Gm1 output to drive COMP. In this way, the CC loop overrides the voltage loop, meaning V_{IMON} is controlled to be constant, achieving average constant current operation.

Connect an RC network between the IMON pin and GND so that the ripple current signal can be filtered out and converted to a voltage signal to represent the averaged output current. The time constant of the RC network should be on the order of 10 to 100 times slower than the voltage loop bandwidth so that the CCL circuit does not interfere with the control loop stability.

4.15.2 Average Overcurrent Protection (AOCP)

The ISL78224 monitors the IMON pin voltage (which represents the averaged total output or input current in Buck mode or Boost mode, respectively) to detect if an Average Overcurrent (OC_AOCP) fault occurs. As shown in Figures 6 and 7, the comparator CMP_OCAVG compares V_{IMON} to internal average overcurrent threshold voltage (2.7V as default) threshold. When V_{IMON} is higher than the threshold, the OC_AVG fault is triggered. The corresponding status register bit (0xD5;[5]) is set to 1 and the XSTAT_FLAG pin is pulled low. Refer to "Fault Status Register-4 (0xD5)" on page 115.

4.16 Power Supply to the Device

To start up the device, VIN needs to be supplied to the device. VIN is used as the temporary power supply until the Flyback controller starts up and V6 and V12 are supplied to the device. If Flyback is not used, V6 and V12 need to be provided to the device externally at the same time or after VIN is provided.

PVCC and VCC are started from VIN initially and are supplied by V6 after V6 becomes higher than the PVCC voltage.

4.17 Enabling the Device (EN Pin)

To enable the device, the external enable signal or resistor divider between VIN and GND need to drive the EN pin higher than 1.2V (typical). The EN pin has an internal 5MΩ (typical) pull-down resistor. This pin also has an internal 5.2V (typical) clamp circuit with a 5kΩ (typical) resistor in-series to prevent excess voltage from being applied to the internal circuits. When applying the EN signal using resistor divider from VIN, internal pull-down resistance needs to be considered. The resistor divider ratio needs to be adjusted as its EN pin input voltage may not exceed 5.2V.

To disable or reset all fault status, the EN pin needs to be driven lower than 0.95V (typical). When the EN pin is driven low, the ISL78224 turns off all of the blocks to minimize the off-state quiescent current.

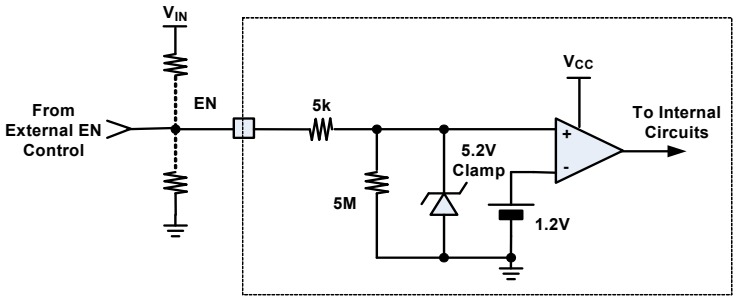


Figure 132. Enable Block

4.18 Initialization and Startup Sequence

4.18.1 Initialization and Internal Bias Circuit Startup

Startup Timing Diagram 1 in Figure 133 on page 68 shows the typical initialization and startup sequences of internal blocks before the main PWM controller startup with the ISL78224. Before the converter starts initialization, the BAT48, BAT12, and V_{IN} voltages need to be applied to the device (t_0 to t_1). The EN pin voltage then needs to be set higher than its rising threshold (1.2V typical) (t_1) to start up the internal regulators. Following the EN pin rise, the internal Backup LDO starts up and the PVCC/VCC voltages become higher than the rising POR threshold (t_2). At this point, the controller begins initialization.

Detailed descriptions on startup procedures for the initialization period and internal power supplies are described in the following sections:

t_0 - t_1: The enable comparator holds the ISL78224 in shutdown until the V_{EN} rises above 1.2V (typical) at the time of t_1.

t_1 - t_2: After EN is set to higher than its rising threshold, $V_{PVCC/VCC}$ gradually increase and reach the internal Power-On Reset (POR) rising threshold 4.5V (typical) at t_2.

t_2 - t_3: During t_2 - t_3, the ISL78224 goes through an initialization process to detect certain pin configurations (ADDR, MODE, PWMx) to latch in the selected operation modes. The time duration for t_2 - t_3 is typically 195µs.

After t3, the I^2C/PMBus communication can be established to check the device and system status and to configure the device operation mode.

t_3 - t_4: During this period, the ISL78224 waits until the internal PLL circuits are locked to the preset oscillator frequency. When PLL locking is achieved at t_4, the oscillator generates an output at the CLKOUT pin. The time duration for t_3 - t_4 depends on the PLLCOMP pin configuration. The PLL is compensated with a series resistor-capacitor (R_{PLL} and C_{PLL1}) from the PLLCOMP pin to GND and a capacitor (C_{PLL2}) from PLLCOMP to GND. At the 100kHz switching frequency, typical values are R_{PLL} = 3.24kΩ, C_{PLL1} = 6.8nF, and C_{PLL2} = 1nF. With this PLLCOMP compensation, the time duration for t_3 - t_4 is around 0.7ms.

t_4 - t_6: The PLL locks the frequency at t_4 and the system is ready to start the Flyback controller, internal LDO, and MCULDO. If Flyback block is used, the Flyback circuit starts its soft-start at t_4. The Flyback circuitry prebiases the SS_FLY pin voltage to be equal to V_{FB_FLY} just after the t_4, which takes around 50µs. The Flyback controller starts switching at this time and the V6/V12 voltages rise following the SS_FLY pin. After V6 and V12 reach their target voltage ranges and the Flyback soft-start period is completed, the SS_FLY pin voltage reaches higher than 3.4V (typical) at t_5 and the internal LDO starts up. The internal LDO switches the main power supply path to the PVCC/VCC from the VIN to V6 to reduce the power loss at the power path transistor of the LDO output stage. With this power source transition, the PVCC voltage from the Internal LDO becomes 5.2V. At timing t_5, the MCULDO also starts up. The output voltage of the MCULDO can be defined by the resistor network connected between MCULDO output, MCULDO_FB, and GND.

If the Flyback block is not used, disable it by connecting SLOPE_FLY to GND through a 51.1kΩ resistor. Connect COMP_FLY directly to GND. This disables the Flyback controller portion of the IC. Connect ISP_FLY and ISN_FLY to GND through 2kΩ resistors. GDRV_FLY and SS_FLY can be left unconnected. V6 may be driven by PVCC or MCUVDD if desired. V12 must be driven with a voltage within its valid range.

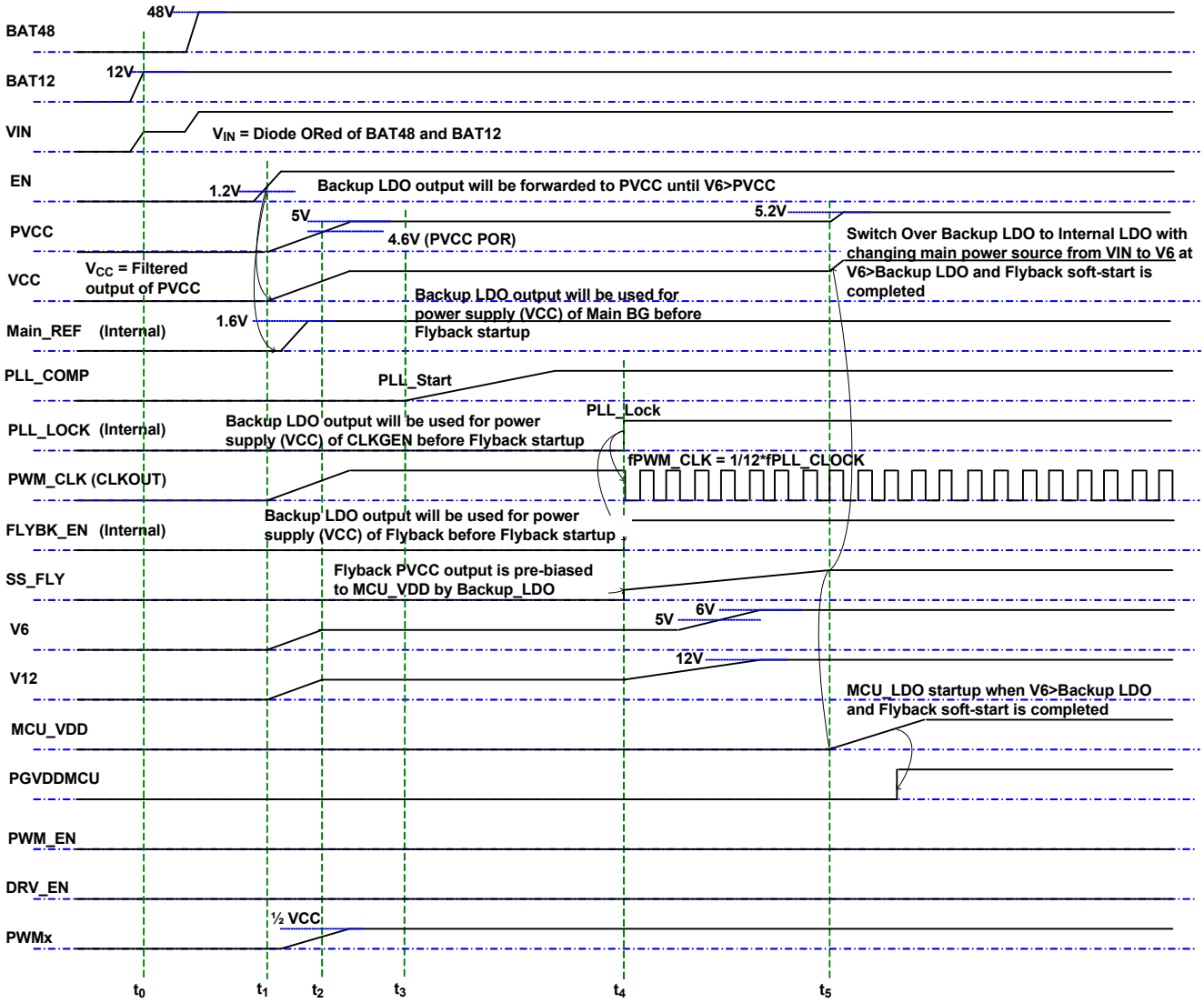


Figure 133. Circuit Initialization and Soft-Start

4.18.1.1 Startup of Main Controller

After t_5, the system is ready to start the main PWM controller. Renesas recommends reconfiguring the device operation mode and individual fault handling between t_5 and t_6, if necessary.

Figure 134 on page 69 shows the timing diagram of the main controller startup with Buck mode, Forced PWM mode, and Phase Drop-Enabled case examples.

t_6 - t_9: While PWM_EN is kept lower than its falling threshold (1.0V typical), the ISL78224 keeps the main controller turned off by keeping DRV_EN signal low. The PWMx outputs that control high-side and low-side MOSFET switching are kept to 1/2 V_{CC} to turn off both high-side and low-side MOSFETs. When PWM_EN becomes higher than its rising threshold (1.2V typical) at t_6, the controller moves into the soft-start period. As the beginning of the soft-start period (t_6), the device prebiases the SS pin voltage to the FB_BK voltage in order to minimize the time lag to start soft-start when the output voltage is prebiased. After the completion of SS

prebiasing, the SS pin ramps up by charging the soft-start capacitor, which is connected between the SS pin and GND, with the constant soft-start current (I_{SS}). Just after the completion of prebiasing of SS pin, the DRV_EN output is pulled high to enable the drivers to control the MOSFETs based on the PWMx signals. The ISL78224 then generates Boot Refresh pulses that pull the PWMx outputs low to turn on the low-side FETs with minimum on-time for eight clock cycles to charge the bootstrap capacitor.

After the boot refresh period, the COMP_BK voltage starts to ramp up from this timing as well. Drivers are enabled during this period but are not allowed to switch until COMP_BK becomes higher than the current-sense ramp offset. When the COMP_BK pin voltage becomes higher than the current-sense ramp offset (at t_7), the PWMx outputs begin switching the drivers. The output voltage ramps up while the FB_BK voltage is following the SS ramp during this soft-start period. At t_8, the output voltage reaches the regulation level and the FB voltage reaches 1.6V. After the SS voltage reaches 1.6V at t_8, SS continues ramping up until it reaches the SS clamp voltage (VSSPCLAMP) 3.47V at t_9, indicating that the SS pin ramp-up is completed. At t_9, the ISL78224 generates an internal soft-start complete signal. While in the soft-start period, the device operates in non-synchronous mode.

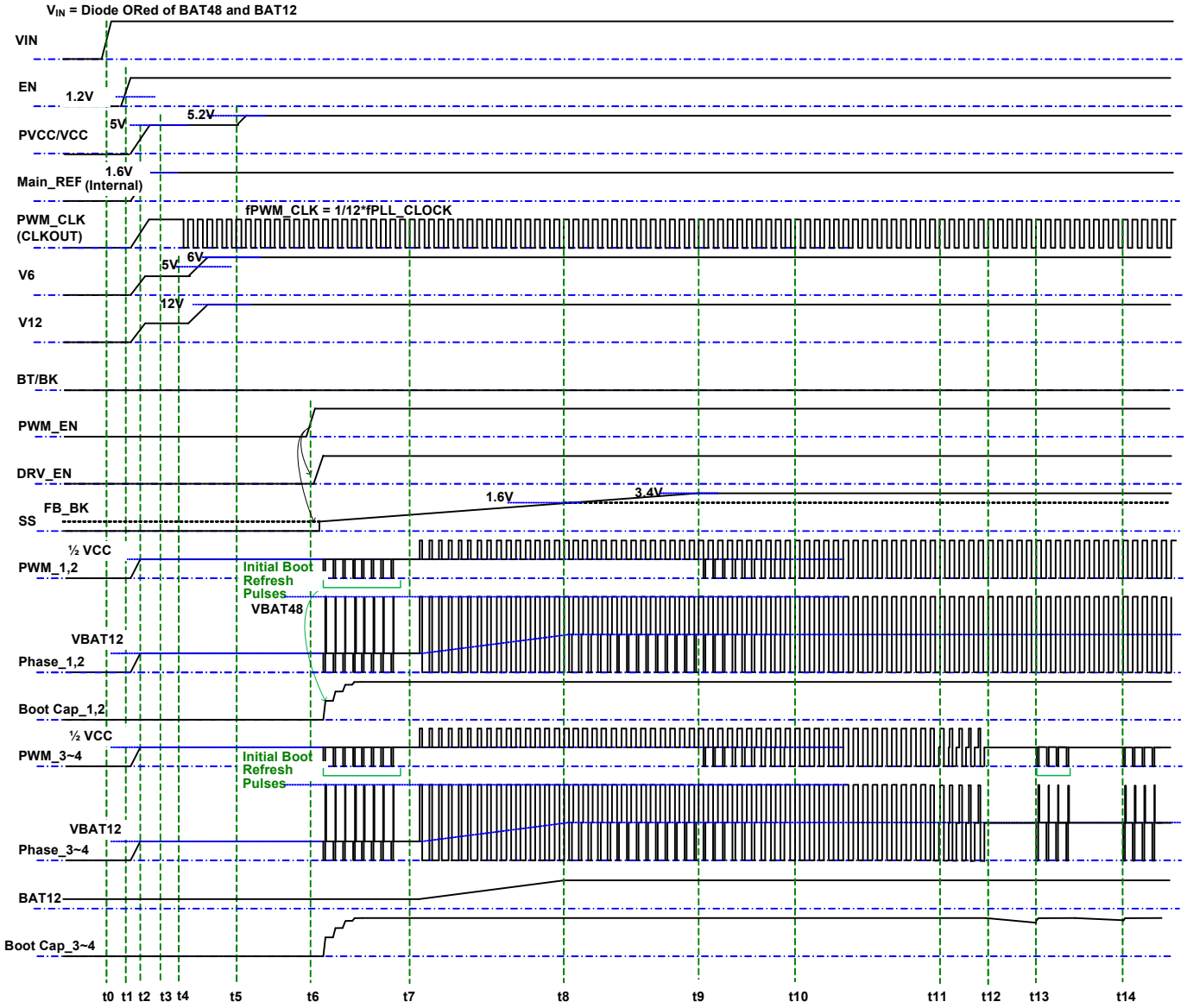


Figure 134. Startup Sequence for Main PWM Controller – Buck Mode/Forced PWM Mode with Phase-Drop

t_9 - t_{10}: During the period of t_9 to t_{10}, the ISL78224 changes its switching from Non-Synchronous mode to Synchronous mode gradually. To avoid the large negative current caused by the sudden full-on of synchronous FET, the ISL78224 controls the synchronous FETs on-time to gradually increase. This period is called the soft-on period and has the duration of up to 100ms (typical).

t_{10} - t_{11}: After the completion of the soft-on period at t_{10}, the converter starts to drop phases during the period of t_{11} and t_{12}. In this duration, the high-side MOSFET of the phases to be dropped is gradually reduced cycle-by-cycle and is finally turned off at t_{12}.

t_{11} - t_{12}: If the phase dropping function is selected, and the load current is low enough to reduce the switching phase count, the controller starts to drop the phases to be dropped during the period of t_{11} and t_{12}. In this duration, the On-duty of high-side MOSFET of the phases to be dropped is gradually reduced cycle-by-cycle and is finally turned off at t_{12}.

t_{12} and after: After t_{12}, as long as the load current is not changing, the controller keeps the same phase count at the timing of t_{12}. And to keep the bootstrap capacitor for high-side MOSFETs drive charged, the controller provides boot refresh pulses every 500µs. While in Boot Refreshing period, PWMx of the dropped phases are pulled low for four clock cycles with minimum on-time to turn on the low-side MOSFET.

The circuit may not start if V_{IN} is directly set to 64V before EN is toggled high. It starts if V_{IN} is initially set to a lower voltage such as 62V, then EN is toggled high. After startup V_{IN} can be increased to 64V.

4.19 LDOs

The ISL78224 has three LDOs. The first is the backup LDO and is implemented for the initial startup of the system. The second is the 5.2V internal LDO and is prepared for the main regulated power rail for the device. The third is the MCULDO and is an output voltage programmable LDO for general purpose use in the system.

4.19.1 Backup LDO

In a 12V/48V battery system, the converter system needs to start up with the power rail at either 12V or 48V. To generate the appropriate voltage for internal analog and logic circuits, typically around 5V, a backup LDO which generates 5.0V output to PVCC from either the 12V or 48V input is implemented on the ISL78224. However, if the power is always supplied from a high voltage rail, the LDO power dissipation is too large to support continuous operation current of the device and the device temperature becomes unnecessarily high. Therefore, the backup LDO is switched over to the internal 5.2V LDO, which is supplied by the V6 rail and is generated by the device-implemented Flyback converter or external power supply system after V6 voltage becomes higher than 5V (typical).

The input voltage of the backup LDO can tolerate up to 64V (65V absolute maximum) and has a current limit of 180mA (typical). The backup LDO can be used continuously with high-load current conditions, although this is not recommended. With this method, the power losses at the LDO need to be considered. At high V_{IN}, the LDO has significant power dissipation that can raise the junction temperature where the implemented thermal shutdown occurs. Figure 135 shows the relationship between maximum allowed backup LDO output current and input voltage. The curves are based on the +25°C/W thermal resistance θ_{JA} of the package.

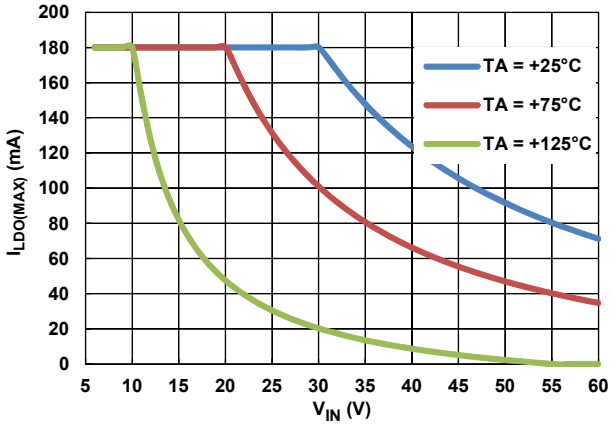


Figure 135. Power Derating Curve

4.19.2 Internal 5.2V LDO

After the backup LDO starts up and the V6 voltage, which is generated by Flyback or external power supply system, becomes higher than 5.2V (typical), the internal 5.2V LDO switches over from the backup LDO and supplies 5.2V (typical) output voltage to PVCC. The internal 5.2V LDO has a fixed 5.2V output and up to 200mA (typical) current limit capability. A 10µF, 10V, or higher X7R typical ceramic capacitor is recommended between PVCC and GND. At low V_{IN} operation, when the internal LDO is saturated or the load current becomes too large to force output voltage to be lower than 5V, the backup LDO turns on again to supply the additional current. If the system falls into this condition, account for power loss as described in "Backup LDO" on page 70.

The output of this LDO, PVCC, is mainly used for the internal logic and PWM driver output. With VCC connected to PVCC as in the typical application, PVCC also supplies other internal analog circuitry. To provide a quiet power rail to the internal analog circuitry, Renesas recommends placing an RC filter between PVCC and VCC. Use a minimum of 1µF ceramic capacitor from VCC to ground for noise decoupling purposes. Because PVCC is providing noisy logic current, a small resistor (10Ω or smaller) between the PVCC and VCC helps to prevent the noise interfering from PVCC to VCC.

4.19.3 MCULDO

The ISL78224 implements a general purpose LDO, called MCULDO, to supply the regulated power rail for external MCU and/or other logic/analog functions. V6 is used as the power supply for the MCULDO. The output voltage of MCULDO can be configured with a resistor network between MCULDO, MCULDO_FB, and GND. Because the reference voltage at MCULDO_FB is set at 1.2V (typical), the output voltage of MCULDO at MCULDO pin is defined by Equation 12.

$$V_{MCUVDD} = 1.2 \cdot \left(1 + \frac{R_{MCUVDDFB1}}{R_{MCUVDDFB2}}\right) \quad \text{(EQ. 12)}$$

$R_{MCULDOFB2}$ is the GND referenced resistor.

To stabilize the output of the MCULDO, Renesas recommends placing a 10µF, 10V, or higher rated X7R ceramic capacitor between MCULDO and GND. The MCULDO has its own power-good threshold to indicate that the MCULDO output is within the target range. An open-drain logic output of PG_MCULDO is pulled low if the MCULDO output is lower or higher than the target range. The rising threshold of undervoltage and overvoltage of MCULDO power-good is 91.7% and 108.3%, respectively, and with 2% of hysteresis. The MCULDO's current limit is 250mA (typical).

4.20 Flyback Controller

The ISL78224 implements a controller for a Flyback converter consisting of an external FET, a current-sensing shunt, and a Flyback transformer. The controller can generate a 6V and 12V bus that can power the V6 and V12 pins on the IC. V6 biases circuits internal to the ISL78224 and V12 biases the external FET drivers.

The design follows typical Flyback converter guidelines. A Flyback transformer, which is really a three-winding, coupled inductor, is selected that is able to absorb energy due to current buildup in its primary winding during the FET on-time. The Flyback transformer then delivers that energy during the FET off-time from its two secondary windings. Enough energy must be absorbed during the FET on-time to support the power required during a switching cycle. The energy absorbed by the end of the FET on-time is stated in Equation 13:

(EQ. 13) $$E = \frac{1}{2} \cdot L_{PRI} \cdot I_{PRI}^2$$

The primary current slope during the FET on-time is proportional to the primary input voltage and inversely proportional to the Flyback transformer primary inductance. Multiplying the current slope by the on-time yields the peak current as shown in Equation 14.

(EQ. 14) $$I_{PK} = \frac{T_{on} \cdot V_{FLYIN}}{L_{PRIMARY}}$$

The peak primary current is detected by a shunt resistor connected between the FET source and ground. The voltage across this shunt resistor must be detected by a Kelvin connection and fed back to the ISL78224 through ISP_FLY and ISN_FLY. Use caution; because one lead of the shunt resistor goes to ground, a layout tool may allow this connection to be non-Kelvin. If the voltage fed back from this shunt resistor is too high, the FET is turned off prematurely and current limiting occurs.

The secondary turns ratio should be 2:1 because the output voltage ratio is V12:V6. The output voltage feedback loop regulation target is satisfied when V6 ~ 6V and V12 ~ 12V.

4.21 Fault Handling

The ISL78224 continuously monitors the input and output voltage of the 12V and 48V battery rails, inductor current of the individual phases, the average output current in Buck mode, the average input current in Boost mode, the Flyback output voltages (6V/12V), the Flyback primary side switching current, and the PVCC/VCC voltages to detect any abnormal voltage or current conditions if present. If a fault condition is detected, depending upon the level of the fault condition, the ISL78224 provides the warning flags, auto/start, hiccup or latch-off functions, as the response to faults. The hiccup or latch-off response can be selected by configuring the MODE pin, or can be overridden by setting corresponding control register bits. The fault status can be read out by an external microcontroller from the I^2C/PMBus interface.

4.21.1 12V/48V (BAT12/BAT48) Rail Input/Output Overvoltage and Undervoltage Fault

The ISL78224 has two levels of overvoltage/undervoltage detection for each input case and output case at the 12V and 48V rails. When the 12V and/or 48V battery voltage becomes higher than the overvoltage warning threshold or lower than the undervoltage warning threshold, the ISL78224 sets the corresponding status register bit (0xD2: BAT12/BAT48 Over/Undervoltage Status Register) to indicate the fault condition and pull down the XSTAT_FLAG (an alert flag). The XSTAT_FLAG alerts the external microcontroller to the fault detection. The external microcontroller can read out the status register bits (0xD2: BAT12/BAT48 Over/Undervoltage Status Register) from the I^2C/PMBus to recognize the fault condition.

In the default setting, the BAT12 Input or Output Overvoltage Warning Threshold is set at 115% of the target voltage, the BAT12 Undervoltage Warning Threshold is set at 85% of the target voltage, the BAT48 Overvoltage Warning Threshold is set at 108% of the target voltage, and BAT48 Undervoltage Warning is set at 75% of the target voltage. These thresholds can be overridden by setting the corresponding Fault Threshold Control Registers (0xB9[2,0]: BAT12 Overvoltage Warning Threshold Control Register, 0xBA[2,0]: BAT12

Undervoltage Warning Threshold Control Register, 0xBB[2,0] BAT48 Overvoltage Warning Threshold Control Register, and 0xBA[5,3]: BAT48 Undervoltage Warning Threshold Control Register).

The over/undervoltage warning fault response can be overridden by setting the corresponding control bit in control registers 0xB1 and 0xB2. The Individual Fault Response Control Register bit 0xB0[7] must be set to 1 to make changes effective.

If the overvoltage or undervoltage conditions reach the second threshold, which is the maximum or minimum operation voltage limit, the device sets the corresponding fault status register (0xD7: BAT12/BAT48 Over/Undervoltage Limit Status Register), pulls down the XSTAT_FLAG, and moves into the Hiccup or Latch-Off mode that is defined by the MODE pin. The fault response defined by MODE pin can be overridden by setting the corresponding control bit in control registers 0xB7 and 0xB8. The Individual Fault Response Control Register bit 0xB0[7] must be set to 1 in order to make changes effective.

If the device moves into Hiccup mode by the BAT12 or BAT48 Over/Undervoltage Limit, the device stops the main controller switching but keeps the Flyback controller, Internal LDOs, and MCULDO active. After the 500ms interval, the device restarts automatically from soft-start. If the device moves into Latch-Off mode by the BAT12 or BAT48 Over/Undervoltage Limit, the device stops the main controller but keeps the Flyback controller, Internal LDOs, and MCULDO active, and waits for the toggling of the EN_PWM or EN pin. If the EN_PWM is toggled, the main controller restarts from soft-start. If the EN pin is toggled, the device stops the Flyback controller, internal LDOs, and MCULDO once, and restarts from the device initialization.

In the default setting, the BAT12 Input or Output Overvoltage Limit Threshold is set at 150% of the target voltage, the BAT12 Undervoltage Limit Threshold is set at 40% of the target voltage, the BAT48 Overvoltage Limit Threshold is set at 125% of the target voltage, and BAT48 Undervoltage Limit Threshold is set at 50% of the target voltage. These thresholds can be overridden by setting the corresponding Fault Threshold Control Registers (0xB9[5,3]: BAT12 Overvoltage Limit Threshold Control Register and 0xBB[5,3] BAT48 Overvoltage Limit Threshold Control Register).

4.21.2 V_{IN} Overvoltage Protection

In a typical application, the ISL78224 is powered by the BAT12 and/or BAT48 rail at the VIN pin for the initial start up. To prevent a V_{IN} overvoltage condition, it is recommended to put a 64V or lower clamp circuit at the VIN pin. The ISL78224 has overvoltage protection at the VIN pin to prevent device operation when V_{IN} is higher than 64V.

4.21.3 Flyback Output (V12/V6) Over/Undervoltage Detection and Protection

The ISL78224 has a Flyback controller to generate the power supply voltages for external drivers (V12 = 12V) and ISL78224 itself (V6 = 6V) from the 12V and/or 48V battery. The flyback input voltage may vary widely around 6V to 64V. The ISL78224 has overvoltage/undervoltage detection/protection for the Flyback outputs (V6 and V12).

If the V12 voltage exceeds 130% of the target voltage (15.6V typical), or V6 becomes higher than 12V, the device sets the corresponding fault status register (0xD3[2]: V12 Overvoltage Limit Status Register, 0xD3[0]: V6 Overvoltage Limit Status Register), pulls down the XSTAT_FLAG, and moves into the Hiccup or Latch-Off mode that is defined by the MODE pin. The fault response defined by the MODE pin can be overridden by setting the corresponding control bit in Control Register 0xB3. The Individual Fault Response Control Register bit 0xB0[7] must be set to 1 in order to make changes effective.

If the V12 voltage becomes lower than 75% of the target voltage (9.1V typical), or V6 becomes lower than 4.9V typical, the device sets the corresponding fault status register (0xD3[3]: V12 Undervoltage Limit Status Register, 0xD3[1]: V6 Undervoltage Limit Status Register), pulls down the XSTAT_FLAG, and moves into the Hiccup or Latch-Off mode that is defined by the MODE pin. The fault response defined by the MODE pin can be overridden by setting the corresponding control bit in control registers 0xB3. The Individual Fault Response Control Register bit 0xB0[7] must be set to 1 in order to make changes effective.

If the device moves into Hiccup mode by V12 or V6 overvoltage limit, the device stops switching the main controller, Flyback controller, internal LDOs, and MCULDO. After the 500ms interval, the device restarts automatically from the device initialization. If the device moves into Latch-Off mode by V12 or V6 overvoltage limit, the device stops the main controller, Flyback controller, internal LDOs, and MCULDO, and waits for the toggling of EN pin. When the EN pin is toggled, the device restarts from the device Initialization.

4.21.4 Flyback Overcurrent Protection

The ISL78224 also monitors the switching current of the Flyback converter at the primary side.

If the voltage across the Flyback switching current-sensing resistor, which is connected between source side of Flyback switching MOSFET and GND, exceeds 75mV, the device sets the corresponding fault status register (0xD3[4]: Flyback Overcurrent Status Register), pulls down the XSTAT_FLAG, and moves into the Hiccup or Latch-Off mode that is defined by the MODE pin. The fault response defined by the MODE pin can be overridden by setting the corresponding control register bit in control registers 0xB4[1,0]. The Individual Fault Response Control Register bit 0xB0[7] must be set to 1 in order to make changes effective.

If the device moves into Hiccup mode by Flyback Overcurrent Protection, the device stops switching the main controller, Flyback controller, internal LDOs, and MCULDO. After the 500ms interval, the device restarts automatically from the device initialization. If the device moves into Latch-Off mode by Flyback Overcurrent Protection, the device stops the main controller, Flyback controller, internal LDOs, and MCULDO, and waits for the toggling of the EN pin. When the EN pin is toggled, the device restarts from the device initialization.

4.21.5 Overcurrent Protection

The ISL78224 has multiple levels of overcurrent protection. Each phase is protected from an overcurrent condition by limiting its peak current, and the combined total current is protected on an average basis. Each phase has cycle-by-cycle negative current protection.

4.21.6 Cycle-by-Cycle Overcurrent Limiting (OC1)

The current flowing through the inductor is monitored by a current-sense resistor (R_{SENx}) and is protected from the overcurrent condition (OC1) by limiting its peak current, cycle-by-cycle basis. When the sensed inductor current reaches the OC1 threshold (I_{SENx} = 94µA = 38µA of Sensed Current + 56µA offset), the main switching transistor (high-side transistor for Buck mode, and low-side transistor for Boost mode) is turned off to limit the peak current. When the OC1 condition is detected, the device sets the corresponding status register bit (0xD5[0]: OC1 Status Register, 0xD9[5,0]: Fault Phase Indicator Register) to indicate the fault condition and pull down the XSTAT_FLAG (an Alert flag). The XSTAT_FLAG alerts the microcontroller to the fault condition. The external microcontroller can read out the status register bits (0xD5[0]: OC1 Status Register, 0xD9[5,0]: Fault Phase Indicator Register) using I^2C/PMBus to recognize the fault condition.

4.21.7 Inductor Peak Current Overcurrent Protection (OC2)

If the output current increases even though OC1 is triggered, the device has a second level of overcurrent threshold (OC2) to protect against further current increase. When the sensed inductor current reaches the OC2 threshold (I_{SENx} = 101µA = 45µA of Sensed Current + 56µA offset), the device sets the corresponding fault status register (0xD5[1]: OC2 Fault Status Register, 0xDA[5,0]: Fault Phase Indicator Register), pulls down the XSTAT_FLAG, and moves into the Hiccup or Latch-Off mode that is defined by the MODE pin. The fault response defined by the MODE pin can be overridden by setting the corresponding control bit in control registers 0xB6. The Individual Fault Response Control Register bit 0xB0[7] must be set to 1 in order to make changes effective.

If the device moves into Hiccup mode by the OC2 fault, the device stops switching the main controller but keeps the Flyback controller, internal LDOs, and MCULDO active. After the 500ms interval, the device restarts automatically from soft-start. If the device moves into Latch-Off mode by the OC2 fault, the device stops the main controller but keeps the Flyback controller, internal LDOs, and MCULDO active, and waits for the toggling of EN_PWM or EN pin. If the EN_PWM is toggled, the main controller restarts from the soft-start. If

the EN pin is toggled, the device stops the Flyback controller, internal LDOs, MCULDO once, and restarts from the device initialization.

4.21.8 Average Overcurrent Protection (AOCP)

The device continuously monitors the total average output current at the IMON pin. If the IMON pin voltage reaches 2.7V, the Average Overcurrent Protection (AOCP) is triggered. At AOCP, the device sets the corresponding fault status register (0xD5[5]: AOCP Fault Status Register), pulls down the XSTAT_FLAG, and moves into the Hiccup or Latch-Off mode that is defined by the MODE pin. The fault response defined by the MODE pin can be overridden by setting the corresponding control bit in control registers 0xB4[5,4]. The Individual Fault Response Control Register bit 0xB0[7] must be set to 1 in order to make changes effective.

If the device moves into Hiccup mode by the AOCP fault, the device stops switching the main controller but keeps the Flyback controller, internal LDOs, and MCULDO active. After the 500ms interval, the device restarts automatically from soft-start. If the device moves into Latch-Off mode by the AOCP fault, the device stops the main controller but keeps Flyback controller, internal LDOs, and MCULDO active, and waits for the toggling of EN_PWM or EN pin. If the EN_PWM is toggled, the main controller restarts from the soft-start. If the EN pin is toggled, the device stops the Flyback controller, internal LDOs, and MCULDO once, and restarts from the device initialization.

4.21.9 Negative Overcurrent Protection (NOC)

The ISL78224 also monitors the negative inductor current. If the negative side of inductor current reaches the Negative Overcurrent Protection (NOC) threshold, the device turns off the synchronous switching transistor (low-side transistor in Buck mode, and high-side transistor in Boost mode) in each cycle to limit the negative current. When cycle-by-cycle NOC is triggered, the device sets the corresponding fault status register (0xD5[2]: NOC Fault Status Register, 0xD9[5,0]: Fault Phase Indicator Register) and pulls down the XSTAT_FLAG.

4.21.10 Fault Phase Removal (Phase-Disable)

The Fault Phase Removal feature enables the device to operate without the specific phases that might be damaged when OC2, NOC, and/or external FET shorts are detected. When these faults are detected, the ISL78224 moves into Hiccup/Latch-Off mode, which is defined by the pin or register configuration, and reports the status. The external MCU determines the necessity of disabling specific phases based on status information and sets the corresponding register bit of 0xBC[5:0]. The ISL78224 starts up by disabling the specified phases. In this case, phase shifting is not provided. If more than half of the maximum operation phase count phases are removed, the device moves into the Hiccup or Latch-Off mode and waits for the toggling of the PWM_EN or EN pin if register 0xB6 [5] is enabled. Hiccup or Latch-off fault response is controlled by register 0xB6 [6,7].

4.21.11 Overriding Individual Fault Responses

The default fault responses (hiccup or latch-off) for all fault conditions are set by the MODE pin configuration. In addition to the default hardware setting of fault responses, the ISL78224 enables the user to override the individual fault responses by setting corresponding registers with the I^2C/PMBus interface. When the individual fault response setting is selected by setting an Individual Fault Response Enable/Disable Control bit (0xB0; [7]) to “1”, all fault responses follow the settings of individual fault response control registers. For details about the control register assignment, refer to “Control and Status Registers” on page 79.

4.22 Operation Mode Setting

The ISL78224 provides several operation modes with the combination of the BT/BK, MODE, PWM_TRI, and ADDR pins.

4.22.1 Converter Direction Selection

The BT/BK pin switches the direction of the converter between Boost mode and Buck mode. When the BT/BK is logic high (VCC > BT/BK > VCC-0.7V), the ISL78224 operates in Boost mode. When the BT/BK is logic low

(0V < BT/BK < 0.7V), the device operates in Buck mode. The BT/BK pin can be controlled by the external microcontroller to change the converter direction. When the BT/BK direction is changed on the fly, the device detects the zero cross of the inductor current, stops the PWMx outputs, and sets DRV_EN low. The device then moves into the soft-start states to restart in the opposite direction from the normal soft-start.

4.22.2 PWM Output Mode Selection

The PWM_TRI pin selects the 3-state or 2-state output of PWMx output pins. If PWM_TRI is connected to VCC, the PWMx outputs are set as 3-state outputs. In this case, the external drivers need to recognize middle level (2.5V) to turn off both high-side and low-side MOSFETs. PWMx output high means the high-side MOSFETs are on and PWMx output low means the low-side MOSFETs are on. If the PWM_TRI is connected to GND, the PWMx outputs take a two-state output (that is, high and low). In this case, the PWMx outputs indicates the on/off timing of the main switching transistor.

4.22.3 Switching Mode and Fault Response Selection

The MODE pin is used to select switching mode (DE mode or Forced PWM mode) and Fault Response (Hiccup or Latch-Off). This pin has four internal threshold levels to determine the combination of switching mode and fault response. At the startup/initialization period of the device, a 30µA current is sourced from the MODE pin. By connecting this pin to GND, VCC, or an external resistor, the desired voltage level for the mode setting is generated and latched into the device. The relation between the MODE pin connection (resistor value) and operation mode are shown in Table 3.

Table 3. Mode Selection Configuration

Mode Pin Voltage	Recommended Connection or Resistor at Mode Pin	DE Mode or Forced PWM	Hiccup or Latch
GND	GND	DE	Hiccup
1.0V	33.2kΩ	Forced PWM	Hiccup
2.05V	68.1kΩ	DE	Latch-Off
VCC	VCC	Forced PWM	Latch-Off

The DE mode is valid only when the PWM_TRI is connected to VCC, meaning the 3-state driver is used. If PWM_TRI is connected to GND, the PWMx output indicates the main switching transistor is on/off only.

4.22.4 Master Controller and Slave Controller Setting

The connection of the ADDR pin determines the main controller (master) and sub-controller (slave) when multiple ISL78224s are used in parallel.

As with the MODE pin, at the startup/initialization of the device, a 30µA current is sourced from the ADDR pin. By connecting this pin to GND, VCC, or an external resistor from this pin to GND, the desired voltage level for the device address setting is generated and latched into the device. The relation between the ADDR pin connection (resistor value) and master or slave selection are shown in Table 4. Up to four devices (and up to eight phases) can operate in parallel.

Table 4. Address Configuration, Master/Slave

ADDR Pin Voltage	Recommended Connection or Resistor at ADDR Pin	Device Order (Master/slave)
GND	GND	Master
1.0V	33.2kΩ	Slave-2
2.05V	68.1kΩ	Slave-3
VCC	VCC	Slave-1

If selected as a slave device, the Flyback controller, MCULDO, BAT12/BAT48 over and undervoltage detection/protection, and feedback loop (GM amp, compensation loop, soft-start, and tracking) of the controller

is disabled. Also, to communicate phase dropping information and synchronize with the master device, the DRV_EN, PD_1, and PD2 pins are set to input.

The slave device also needs to recognize how many slaves are connected in parallel to perform the proper phase shifting. For this purpose, the FB_BT and FB_BK pins are used for the slave device count indicator.

- If the system is configured as a 1-master/1-slave operation, connect FB_BT and FB_BK pins of slave device to GND.
- If the system is configured as a 1-master/2-slave operation, connect FB_BT and FB_BK pins of slave devices to VCC.
- If the system is configured as a 1-master/3-slave operation, connect FB_BT and FB_BK pins of slave devices to GND and VCC, respectively.

When the system is configured by one master device only, connect the ADDR pin to GND.

4.23 Operating Phase Count Setting and Phase Shifting

The ISL78224 can work in 2-, 3-, or 4-phase configuration.

Connecting the PWM4 to VCC selects 3-phase operation and each of the PWM output pulses are shifted in 1/3 cycle (120°) increments. Connecting the PWM3 to VCC selects 2-phase operation and each of the PWM output pulses are shifted in 1/2 cycle (180°) increments.

Unused current-sense amplifier inputs ISENxA should be connected to BAT12. Unused current-sense amplifier inputs ISENxB should be left unconnected.

4.24 I^2C/PMBus Communication

The ISL78224 is implemented with an I^2C/PMBus compatible digital interface for the user to monitor and change a few operating parameters allowing smart control of the regulator.

The Power Management Bus (PMBus) is an open-standard digital power management protocol. It uses SMBus as its physical communication layer and includes support for the SMBus Alert (SALERT). In much the same way as SMBus defines the general means to manage portable power, PMBus defines the means to manage power subsystems.

PMBus and SMBus are I^2C derived bus standards that are generally electrically compatible with I^2C. They are more robust (Timeouts Force Bus Reset) and offer more features than I^2C, such as an SMBALERT(SALERT) line for interrupts, Packet Error Checking (PEC), and Host Notify Protocol.

4.24.1 Monitor Faults and Configure Fault Responses

When any of the fault conditions are detected, the corresponding bit of the FAULT_STATUS register is set to 1 and the XSTAT_FLAG pin is pulled low. The I^2C/PMBus host controller is interrupted by monitoring the XSTAT_FLAG pin and responds as follows:

- ISL78224 device pulls XSTAT_FLAG low.
- The host detects that XSTAT_FLAG is low, then performs transmission with Alert Response Address to find which device is pulling XSTAT_FLAG low.
- The host talks to the device that is pulling XSTAT_FLAG low. The actions that the host performs next are up to the system designer.

Each individual bit of the FAULT_STATUS register can only be cleared to 0 by writing to that register from the I^2C/PMBus, or by CLEAR_FAULTS command, or POR recycle. When all the bits of FAULT_STATUS register are reset to 0, the XSTAT_FLAG pin is released to be pulled HIGH. To reset or clear each individual bit of the FAULT_STATUS register, write the same value to the individual bit of interest.

4.24.2 Set Operation/Fault Thresholds via I²C/PMBus

A system controller can change the ISL78224 operating parameters through the I²C/PMBus interface. These commands include, but are not limited to, the following:

- Set input/output overvoltage/undervoltage threshold
- Set the fault responses of each individual fault
- Enable or disable the PWM operation of specific phase
- Set constant current control thresholds

4.24.3 Accessible Timing for I²C/PMBus Registers Status

All the I²C/PMBus command registers are set to default values during the t_2 - t_3 initialization period, as shown in Figure 133 on page 68. The I²C/PMBus is accessible after this part initialization period.

After part start-up, as long as EN and PVCC/VCC are kept HIGH, all the PMBus registers values are accessible from the PMBus.

When the part is in Latch-Off status or Hiccup mode triggered by any fault, the internal LDO is still enabled and keeps PVCC/VCC HIGH. All the PMBus register values are accessible from PMBus. The FAULT_STATUS register values are accessible for the host to diagnose the type of fault.

Either EN low or PVCC/VCC falling below POR disables the ISL78224. All the registers are reset and are not accessible from the PMBus.

5. Control and Status Registers

To access the ISL78224 Control Registers or Status Registers from the I^{2}C/PMBus interface, an appropriate device address needs to be provided. The address IDs for Master device, Slave-1 device, Slave-2 device, and Slave-3 device are 0x4C, Ox4D, 0x4E, and 0x4F, respectively. A complete map of the ISL78224 status and control registers is available on the Renesas website.

5.1 Control Registers

Control registers enable the selection of functions such as analog tracking, inverting of PWM output polarity, individual fault responses for each fault mode, fault and control threshold setting, maximum/minimum on-duty, and boot-refreshing timing control, etc.

Control Register 1 (0xB0)

Definition: Enables/disables the analog tracking, inverting PWM output polarity, clear faults command, and individual fault settings.

Data Length in Bytes: 1

Data Format: Bit Field

Typical: R/W

Protectable: Yes

Default Value: 00h

Units: N/A

Register Name	Control Register 1 (0xB0)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Individual Fault Response Control Bit	Clear Faults	PWM_INV	ATRAK/DT RACK	Reserved			
Default Value	0	0	0	0	0	0	0	0

Individual Fault Response Enable/Disable Control Bit (0xB0: Bit 7)

Enables/disables the individual fault response control with control registers.

0xB0 Bit 7	Description
0 (Default)	Disables individual fault response control. Use default fault responses defined by the MODE pin setting.
1	Enables individual fault response control by dedicated control registers. For details, refer to descriptions of each control register.

Clear Faults (0xB0: Bit 6)

Clears all fault bits. After a soft-start is complete, clear all faults and then keep the faults by setting Bit 6 to 1 and then to 0. Faults indicated after this are true faults and not the result of changing registers during startup.

0xB0 Bit 6	Description
0 (Default)	Keeps the faults
1	Clears all faults. After the external MCU reads the fault status, set this bit to “1” to clear the faults, then return to “0” to get next fault. If the error status remains in the system, the error bits are altered at corresponding registers immediately after this bit returns to “0”.

PWM_INV (0xB0: Bit 5)
Inverts the PWM output polarity.

0xB0 Bit 5	Description
0 (Default)	Normal polarity. When an ISL78224 PWMx output is “High”, its associated FET driver is commanded at its input to turn on the high-side FET and to turn off the low-side FET. When an ISL78224 PWMx output is “Low”, its associated FET driver is commanded at its input to turn off the high-side FET and to turn on the low-side FET. When a PWMx output is “middle” (when the 3-state PWM output is used), turn off both high-side and low-side FETs.
1	Inverted polarity. When an ISL78224 PWMx output is “High”, its associated FET driver is commanded at its input to turn off the high-side FET and to turn on the low-side FET. When an ISL78224 PWMx output is “Low”, its associated FET driver is commanded at its input to turn on the high-side FET and to turn off the low-side FET. When a PWMx output is “middle” (when the 3-state PWM output is used), turn off both high-side and low-side FETs.

ATRK/DTRK Control Bit (0xB0: Bit 4)
Selects the track pin input mode as either analog or digital.

0xB0 Bit 4	Description
0 (Default)	Digital tracking input
1	Analog tracking input

Individual Fault Response Control Register 1 (0xB1)

Definition: BAT12 input and output overvoltage and undervoltage fault response setting.

Data Length in Bytes: 1

Data Format: Bit Field

Typical: R/W

Protectable: Yes

Default Value: 00h

Units: N/A.

Register Name	Individual Fault Response Control Register 1 (0xB1)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	BAT12 Input Undervoltage Fault Control Bits		BAT12 Input Overvoltage Fault Control Bits		BAT12 Output Undervoltage Fault Control Bits		BAT12 Output Overvoltage Fault Control Bits	
Default Value	0	0	0	0	0	0	0	0

BAT12 Output Overvoltage Fault (Warning) Control Bit (0xB1: Bit 1:0)

When the individual fault response enable/disable control bit (0xB0[7]) is “1”, the device selects the fault response when BAT12 exceeds the first level of overvoltage threshold. When the individual fault response enable/disable control Bit (0xB0[7]) is “0”, the “MODE” pin setting is used for the fault control and this register setting is ignored.

0xB1 Bit 1	0xB1 Bit 0	Description
0	0	Flagging only (Default) When the BAT12 output voltage exceeds the first overvoltage threshold, the corresponding fault status register (0xD2[0]) is set to “1”, and the XSTAT_FLAG is pulled low. The system continues to operate. No hiccup or latch-off responses.
0	1	Hiccup (Auto Restart) When the BAT12 output voltage exceeds the first overvoltage threshold, the corresponding fault status register (0xD2[0]) is set to “1”, and the XSTAT_FLAG is pulled low. At the same time, the system stops PWM switching. The PWM switching recovers automatically 500ms (typical) after the overvoltage condition is removed.
1	0	Latch-Off When the BAT12 output voltage exceeds the first overvoltage threshold, the corresponding fault status register (0xD2[0]) is set to “1”, and the XSTAT_FLAG is pulled low. At the same time, the system stops PWM switching. The PWM switching does not recover automatically when the overvoltage condition is removed. To recover the switching, toggle PWM_EN or EN.
1	1	Flagging only (same as “0,0”)

BAT12 Output Undervoltage Fault (Warning) Control Bit (0xB1: Bit 3:2)

When the individual fault response enable/disable control bit (0xB0[7]) is “1”, the device selects the fault response when the BAT12 output voltage becomes lower than the first level of undervoltage threshold. When the individual fault response enable/disable control bit (0xB0[7]) is “0”, the “MODE” pin setting is used for the fault control and this register setting is ignored.

0xB1 Bit 3	0xB1 Bit 2	Description
0	0	Flagging only (Default) When the BAT12 output voltage becomes lower than the first undervoltage threshold, the corresponding fault status register (0xD2[1]) is set to “1”, and the XSTAT_FLAG is pulled low. The system continues to operate. No hiccup or latch-off responses.
0	1	Hiccup (Auto Restart) When the BAT12 output voltage becomes lower than the first undervoltage threshold, the corresponding fault status register (0xD2[1]) is set to “1”, and the XSTAT_FLAG is pulled low. At the same time, the system stops PWM switching. The PWM switching recovers automatically 500ms (typical) after the undervoltage condition is removed.
1	0	Latch-Off When the BAT12 output voltage becomes lower than the first undervoltage threshold, the corresponding fault status register (0xD2[1]) is set to “1”, and the XSTAT_FLAG is pulled low. At the same time, the system stops PWM switching. The PWM switching does not recover automatically when the undervoltage condition is removed. To recover the switching, toggle PWM_EN or EN.
1	1	Flagging only (same as “0,0”)

BAT12 Input Overvoltage Fault (Warning) Control Bit (0xB1: Bit 5:4)

When the individual fault response enable/disable control bit (0xB0[7]) is “1”, the device selects the fault response when BAT12 input voltage exceeds the first level of overvoltage threshold. When the individual fault response enable/disable control bit (0xB0[7]) is “0”, the “MODE” pin setting is used for the fault control and this register setting is ignored.

0xB1 Bit 5	0xB1 Bit 4	Description
0	0	Flagging only (Default) When the BAT12 input voltage exceeds the first overvoltage threshold, the corresponding fault status register (0xD2[2]) is set to “1”, and the XSTAT_FLAG is pulled low. The system continues to operate. No hiccup or latch-off responses.
0	1	Hiccup (Auto Restart) When the BAT12 input voltage exceeds the first overvoltage threshold, the corresponding fault status register (0xD2[2]) is set to “1”, and the XSTAT_FLAG is pulled low. At the same time, the system stops PWM switching. The PWM switching recovers automatically 500ms (typical) after the overvoltage condition is removed.
1	0	Latch-Off When the BAT12 input voltage exceeds the first overvoltage threshold, the corresponding fault status register (0xD2[2]) is set to “1”, and the XSTAT_FLAG is pulled low. At the same time, the system stops PWM switching. The PWM switching does not recover automatically when the overvoltage condition is removed. To recover the switching, toggle PWM_EN or EN.
1	1	Flagging only (same as “0,0”)

BAT12 Input Undervoltage Fault (Warning) Control Bit (0xB1: Bit 7:6)

When the individual fault response enable/disable control bit (0xB0[7]) is “1”, the device selects the fault response when BAT12 becomes lower than the first level of undervoltage threshold. When the individual fault response enable/disable control bit (0xB0[7]) is “0”, the “MODE” pin setting is used for the fault control and this register setting is ignored.

0xB1 Bit 7	0xB1 Bit 6	Description
0	0	Flagging only (Default) When the BAT12 input voltage becomes lower than the first undervoltage threshold, the corresponding fault status register (0xD2[3]) is set to “1”, and the XSTAT_FLAG is pulled low. The system continues to operate. No hiccup or latch-off responses.
0	1	Hiccup (Auto Restart) When the BAT12 input voltage becomes lower than the first undervoltage threshold, the corresponding fault status register (0xD2[3]) is set to “1”, and the XSTAT_FLAG is pulled low. At the same time, the system stops PWM switching. The PWM switching recovers automatically 500ms (typical) after the undervoltage condition is removed.
1	0	Latch-Off When the BAT12 input voltage becomes lower than the first undervoltage threshold, the corresponding fault status register (0xD2[3]) is set to “1”, and the XSTAT_FLAG is pulled low. At the same time, the system stops PWM switching. The PWM switching does not recover automatically when the undervoltage condition is removed. To recover the switching, toggle PWM_EN or EN.
1	1	Flagging only (same as “0,0”)

Individual Fault Response Control Register 2 (0xB2)

Definition: BAT48 input and output overvoltage and undervoltage fault response setting.

Data Length in Bytes: 1

Data Format: Bit Field

Typical: R/W

Protectable: Yes

Default Value: 00h

Units: N/A

Register Name	Individual Fault Response Control Register 2 (0xB2)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	BAT48 Input Undervoltage Fault Control Bits		BAT48 Input Overvoltage Fault Control Bits		BAT48 Output Undervoltage Fault Control Bits		BAT48 Output Overvoltage Fault Control Bits	
Default Value	0	0	0	0	0	0	0	0

BAT48 Output Overvoltage Fault (Warning) Control Bit (0xB2: Bit 1:0)

When the individual fault response enable/disable control bit (0xB0[7]) is “1”, the device selects the fault response when BAT48 exceeds the first level of overvoltage threshold. When the individual fault response enable/disable control bit (0xB0[7]) is “0”, the “MODE” pin setting is used for the fault control and this register setting is ignored.

0xB2 Bit 1	0xB2 Bit 0	Description
0	0	Flagging only (Default) When the BAT48 output voltage exceeds the first overvoltage threshold, the corresponding fault status register (0xD2[4]) is set to “1”, and the XSTAT_FLAG is pulled low. The system continues to operate. No hiccup or latch-off responses.
0	1	Hiccup (Auto Restart) When the BAT48 output voltage exceeds the first overvoltage threshold, the corresponding fault status register (0xD2[4]) is set to “1”, and the XSTAT_FLAG is pulled low. At the same time, the system stops PWM switching. The PWM switching recovers automatically 500ms (typical) after the overvoltage condition is removed.
1	0	Latch-Off When the BAT48 output voltage exceeds the first overvoltage threshold, the corresponding fault status register (0xD2[4]) is set to “1”, and the XSTAT_FLAG is pulled low. At the same time, the system stops PWM switching. The PWM switching does not recover automatically when the overvoltage condition is removed. To recover the switching, toggle PWM_EN or EN.
1	1	Flagging only (same as “0,0”)

BAT48 Output Undervoltage Fault (Warning) Control Bit (0xB2: Bit 3:2)

When the individual fault response enable/disable control bit (0xB0[7]) is “1”, the device selects the fault response when BAT48 output voltage becomes lower than the first level of undervoltage threshold. When the individual fault response enable/disable control bit (0xB0[7]) is “0”, the “MODE” pin setting is used for the fault control and this register setting is ignored.

0xB2 Bit 3	0xB2 Bit 2	Description
0	0	Flagging only (Default) When the BAT48 output voltage becomes lower than the first overvoltage threshold, the corresponding fault status register (0xD2[5]) is set to “1”, and the XSTAT_FLAG is pulled low. The system continues to operate. No hiccup or latch-off responses.
0	1	Hiccup (Auto Restart) When the BAT48 output voltage becomes lower than the first overvoltage threshold, the corresponding fault status register (0xD2[5]) is set to “1”, and the XSTAT_FLAG is pulled low. At the same time, the system stops PWM switching. The PWM switching recovers automatically 500ms (typical) after the undervoltage condition is removed.
1	0	Latch-Off When the BAT48 output voltage becomes lower than the first Under voltage threshold, the corresponding fault status register (0xD2[5]) is set to “1”, and the XSTAT_FLAG is pulled low. At the same time, the system stops PWM switching. The PWM switching does not recover automatically when the undervoltage condition is removed. To recover the switching, toggle PWM_EN or EN.
1	1	Flagging only (same as “0.0”)

BAT48 Input Overvoltage Fault (Warning) Control Bit (0xB2: Bit 5:4)

When the individual fault response enable/disable control bit (0xB0[7]) is “1”, the device selects the fault response when the BAT48 input voltage exceeds the first level of overvoltage threshold. When the individual fault response enable/disable control bit (0xB0[7]) is “0”, the “MODE” pin setting is used for the fault control and this register setting is ignored.

0xB2 Bit 5	0xB2 Bit 4	Description
0	0	Flagging only (Default) When the BAT48 input voltage exceeds the first overvoltage threshold, the corresponding fault status register (0xD2[6]) is set to “1”, and the XSTAT_FLAG is pulled low. The system continues to operate. No hiccup or latch-off responses.
0	1	Hiccup (Auto Restart) When the BAT48 input voltage exceeds the first overvoltage threshold, the corresponding fault status register (0xD2[6]) is set to “1”, and the XSTAT_FLAG is pulled low. At the same time, the system stops PWM switching. The PWM switching recovers automatically 500ms (typical) after the overvoltage condition is removed.
1	0	Latch-Off When the BAT48 input voltage exceeds the first overvoltage threshold, the corresponding fault status register (0xD2[6]) is set to “1”, and the XSTAT_FLAG is pulled low. At the same time, the system stops PWM switching. The PWM switching does not recover automatically when the overvoltage condition is removed. To recover the switching, toggle PWM_EN or EN.
1	1	Flagging only (same as “0.0”)

BAT48 Input Undervoltage Fault (Warning) Control Bit (0xB2: Bit 7:6)

When the individual fault response enable/disable control bit (0xB0[7]) is “1”, the device selects the fault response when BAT48 becomes lower than the first level of undervoltage threshold. When the individual fault response enable/disable control bit (0xB0[7]) is “0”, the “MODE” pin setting is used for the fault control and this register setting is ignored.

0xB2 Bit 7	0xB2 Bit 6	Description
0	0	Flagging only (Default) When the BAT48 input voltage becomes lower than the first undervoltage threshold, the corresponding fault status register (0xD2[7]) is set to “1”, and the XSTAT_FLAG is pulled low. The system continues to operate. No hiccup or latch-off responses.
0	1	Hiccup (Auto Restart) When the BAT48 input voltage becomes lower than the first undervoltage threshold, the corresponding fault status register (0xD2[7]) is set to “1”, and the XSTAT_FLAG is pulled low. At the same time, the system stops PWM switching. The PWM switching recovers automatically 500ms (typical) after the undervoltage condition is removed.
1	0	Latch-Off When the BAT48 input voltage becomes lower than the first undervoltage threshold, the corresponding fault status register (0xD2[7]) is set to “1”, and the XSTAT_FLAG is pulled low. At the same time, the system stops PWM switching. The PWM switching does not recover automatically when the undervoltage condition is removed. To recover the switching, toggle PWM_EN or EN.
1	1	Flagging only (same as “0,0”)

Individual Fault Response Control Register 3 (0xB3)

Definition: V12 and V6 (Flyback output, or external input when Flyback is not used) overvoltage and undervoltage fault response setting.

Data Length in Bytes: 1

Data Format: Bit Field

Typical: R/W

Protectable: Yes

Default Value: 00h

Units: N/A

Register Name	Individual Fault Response Control Register 3 (0xB3)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	V6 Undervoltage Fault Control Bits		V6 Overvoltage Fault Control Bits		V12 under Voltage Fault Control Bits		V12 Overvoltage Fault Control Bits	
Default Value	0	0	0	0	0	0	0	0

V12 Overvoltage Fault Control Bit (0xB3: Bit 1:0)

When the individual fault response enable/disable control bit (0xB0[7]) is “1”, the device selects the fault response when V12 exceeds the overvoltage threshold. When the individual fault response enable/disable control bit (0xB0[7]) is “0”, the “MODE” pin setting is used for the fault control and this register setting is ignored.

0xB3 Bit 1	0xB3 Bit 0	Description
0	0	Flagging only (Default) When the V12 voltage exceeds the overvoltage threshold, the corresponding fault status register (0xD3[2]) is set to “1”, and the XSTAT_FLAG is pulled low. The system continues to operate. No hiccup or latch-off responses.
0	1	Hiccup (Auto Restart) When the V12 voltage exceeds the overvoltage threshold, the corresponding fault status register (0xD3[2]) is set to “1”, and the XSTAT_FLAG is pulled low. At the same time, the system stops PWM switching. The PWM switching recovers automatically 500ms (typical) after the overvoltage condition is removed.
1	0	Latch-Off When the V12 voltage exceeds the overvoltage threshold, the corresponding fault status register (0xD3[2]) is set to “1”, and the XSTAT_FLAG is pulled low. At the same time, the system stops PWM switching. The PWM switching does not recover automatically when the overvoltage condition is removed. To recover the switching, toggle PWM_EN or EN.
1	1	Flagging only (same as “0,0”)

V12 Undervoltage Fault Control Bit (0xB3: Bit 3:2)

When the individual fault response enable/disable control bit (0xB0[7]) is “1”, the device selects the fault response when the V12 voltage becomes lower than the undervoltage threshold. When the individual fault response enable/disable control bit (0xB0[7]) is “0”, the “MODE” pin setting is used for the fault control and this register setting is ignored.

0xB3 Bit 3	0xB3 Bit 2	Description
0	0	Flagging only (Default) When the V12 output voltage becomes lower than the undervoltage threshold, the corresponding fault status register (0xD3[3]) is set to “1”, and the XSTAT_FLAG is pulled low. The system continues to operate. No hiccup or latch-off responses.
0	1	Hiccup (Auto Restart) When the V12 voltage becomes lower than the undervoltage threshold, the corresponding fault status register (0xD3[3]) is set to “1”, and the XSTAT_FLAG is pulled low. At the same time, the system stops PWM switching. The PWM switching recovers automatically 500ms (typical) after the undervoltage condition is removed.
1	0	Latch-Off When the V12 voltage becomes lower than the undervoltage threshold, the corresponding fault status register (0xD3[3]) is set to “1”, and the XSTAT_FLAG is pulled low. At the same time, the system stops PWM switching. The PWM switching does not recover automatically when the undervoltage condition is removed. To recover the switching, toggle PWM_EN or EN.
1	1	Flagging only (same as “0,0”)

V6 Overvoltage Fault Control Bit (0xB3: Bit 5:4)

When the individual fault response enable/disable control bit (0xB0[7]) is “1”, the device selects the fault response when the V6 voltage exceeds the overvoltage threshold. When the individual fault response enable/disable control bit (0xB0[7]) is “0”, the “MODE” pin setting is used for the fault control and this register setting is ignored.

0xB3 Bit 5	0xB3 Bit 4	Description
0	0	Flagging only (Default) When the V6 voltage exceeds the overvoltage threshold, the corresponding fault status register (0xD3[0]) is set to “1”, and the XSTAT_FLAG is pulled low. The system continues to operate. No hiccup or latch-off responses.
0	1	Hiccup (Auto Restart) When the V6 voltage exceeds the overvoltage threshold, the corresponding fault status register (0xD3[0]) is set to “1”, and the XSTAT_FLAG is pulled low. At the same time, the system stops PWM switching. The PWM switching recovers automatically 500ms (typical) after the overvoltage condition is removed.
1	0	Latch-Off When the V6 voltage exceeds the overvoltage threshold, the corresponding fault status register (0xD3[0]) is set to “1”, and the XSTAT_FLAG is pulled low. At the same time, the system stops PWM switching. The PWM switching does not recover automatically when the overvoltage condition is removed. To recover the switching, toggle PWM_EN or EN.
1	1	Flagging only (same as “0,0”)

V6 Undervoltage Fault Control Bit (0xB3: Bit 7:6)

If the individual fault response enable/disable control bit (0xB0[7]) is “1”, the device selects the fault response when V6 becomes lower than the undervoltage threshold. If the individual fault response enable/disable control bit (0xB0[7]) is “0”, the “MODE” pin setting is used for the fault control and this register setting is ignored.

0xB3 Bit 7	0xB3 Bit 6	Description
0	0	Flagging only (Default) When the V6 voltage becomes lower than the undervoltage threshold, the corresponding fault status register (0xD3[1]) is set to “1”, and the XSTAT_FLAG is pulled low. The system continues to operate. No hiccup or latch-off responses.
0	1	Hiccup (Auto Restart) When the V6 voltage becomes lower than the undervoltage threshold, the corresponding fault status register (0xD3[1]) is set to “1”, and the XSTAT_FLAG is pulled low. At the same time, the system stops PWM switching. The PWM switching recovers automatically 500ms (typical) after the undervoltage condition is removed.
1	0	Latch-Off When the V6 voltage becomes lower than the undervoltage threshold, the corresponding fault status register (0xD3[1]) is set to “1”, and the XSTAT_FLAG is pulled low. At the same time, the system stops PWM switching. The PWM switching does not recover automatically when the undervoltage condition is removed. To recover the switching, toggle PWM_EN or EN.
1	1	Flagging only (same as “0,0”)

Individual Fault Response Control Register 4 (0xB4)

Definition: Flyback overcurrent and Average Overcurrent Protection (AOCP) fault response setting.

Data Length in Bytes: 1

Data Format: Bit Field

Typical: R/W

Protectable: Yes

Default Value: 00h

Units: N/A

Register Name	Individual Fault Response Control Register 4 (0xB4)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Flyback Switching FET Short Protection Control	Reserved	Average Overcurrent Protection Control Bits		Reserved		Flyback Switching FET Overcurrent Protection Control Bits	
Default Value	0	0	0	0	0	0	0	0

Flyback Primary Side Switching FET Overcurrent Protection Control Bits (0xB4: Bit 1:0)
If the individual fault response enable/disable control bit (0xB0[7]) is “1”, the device selects the fault response when detecting overcurrent situations at the primary side switching FET of Flyback. If the individual fault response enable/disable control bit (0xB0[7]) is “0”, the “MODE” pin setting is used for the fault control and this register setting is ignored.

0xB4 Bit 1	0xB4 Bit 0	Description
0	0	Flagging only (Default) When the overcurrent condition at the primary side of the Flyback switching FET is detected, the corresponding fault status register (0xD3[4]) is set to “1”, and the XSTAT_FLAG is pulled low. The system continues to operate. No hiccup or latch-off responses.
0	1	Hiccup (Auto Restart) When the overcurrent condition at the primary side of the Flyback switching FET is detected, the corresponding fault status register (0xD3[4]) is set to “1”, and the XSTAT_FLAG is pulled low. At the same time, the system stops switching the Flyback and PWMx outputs. The Flyback switching recovers automatically 500ms (typical) after the overcurrent condition is removed. The PWM switchings recover using the normal soft-start period after the Flyback recovery.
1	0	Latch-Off When the overcurrent condition at the primary side of the Flyback switching FET is detected, the corresponding fault status register (0xD3[4]) is set to “1”, and the XSTAT_FLAG is pulled low. At the same time, the system stops switching the Flyback and PWMx outputs. The Flyback switching does not recover automatically even if the overcurrent condition is removed. To recover switching, toggle EN. To restart PWMx switching, set PWM_EN to “high” after the Flyback restart and V6/V12 becomes a proper level.
1	1	Flagging only (same as “0,0”)

Average Overcurrent Fault Control Bit (0xB4: Bit 5:4)
When the individual fault response enable/disable control bit (0xB0[7]) is “1”, the device selects the fault response when average overcurrent protection (average output overcurrent in Buck mode and average input overcurrent in Boost mode) condition is detected. When the individual fault response enable/disable control bit (0xB0[7]) is “0”, the “MODE” pin setting is used for the fault control and this register setting is ignored.

0xB4 Bit 5	0xB4 Bit 4	Description
0	0	Flagging only (Default) When an Average Overcurrent Protection (AOCP) (average output overcurrent in Buck mode and average input overcurrent in Boost mode) condition is detected, the corresponding fault status register (0xD5[5]) is set to “1”, and the XSTAT_FLAG is pulled low. The system continues to operate. No hiccup or latch-off responses.
0	1	Hiccup (Auto Restart) When an Average Overcurrent Protection (AOCP) (average output overcurrent in Buck mode or average input overcurrent in Boost mode) condition is detected, the corresponding fault status register (0xD5[5]) is set to “1”, and the XSTAT_FLAG is pulled low. At the same time, the system stops PWM switching. The PWM switching recovers automatically 500ms (typical) after the AOCP condition is removed.
1	0	Latch-Off When an Average Overcurrent Protection (AOCP) (average output overcurrent in Buck mode or average input overcurrent in Boost mode) condition is detected, the corresponding fault status register (0xD5[5]) is set to “1”, and the XSTAT_FLAG is pulled low. At the same time, the system stops PWM switching. The PWM switching does not recover automatically when the AOCP condition is removed. To recover the switching, toggle PWM_EN or EN.
1	1	Flagging only (same as “0.0”)

Flyback Primary Side Switching FET Short Fault Control Bit (0xB4: Bit 7)

If the individual fault response enable/disable control bit (0xB0[7]) is “1”, the device selects the fault response when detecting the short condition at the primary side switching FET of Flyback. If the individual fault response enable/disable control bit (0xB0[7]) is “0”, the “MODE” pin setting is used for the fault control and this register setting is ignored.

0xB4 Bit 7	Description
0 (Default)	When detecting the short condition at the primary side of the Flyback switching FET, the corresponding fault status register (0xD8[4]) is set to “1”, the XSTAT_FLAG is pulled low, and the XSYS_FAIL is pulled low to stop the system. Flyback and PWMx switching is stopped. To recover, toggle EN.
1	Flagging only When detecting the short condition at primary side switching FET of Flyback, the corresponding fault status register (0xD8[4]) is set to “1” and the XSTAT_FLAG is pulled low. The XSYS_FAIL pin is not pulled low.

Individual Fault Response Control Register 6 (0xB6)

Definition: Cycle-by-cycle Overcurrent 2 (OC2) fault response setting.

Data Length in Bytes: 1

Data Format: Bit Field

Typical: R/W

Protectable: Yes

Default Value: 00h

Units: N/A

Register Name	Individual Fault Response Control Register 5 (0xB6)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	OC2 and phase disable fault response control bits		Phase disable response	Reserved				
Default Value	0	0	0	0	0	0	0	0

OC2 and >50% Phase Disable Fault Response Control Bits (0xB6: Bit 7:6)

If the individual fault response enable/disable control bit (0xB0[7]) is “1”, the device selects the fault response when detecting Overcurrent 2 condition at any of the PWM switching channels. If the individual fault response enable/disable control bit (0xB0[7]) is “0”, the “MODE” pin setting is used for the fault control and this register setting is ignored.

0xB6 Bit 7	0xB6 Bit 6	Description
0	0	Flagging only (Default) When the overcurrent 2 (OC2) condition is detected at any of the PWM switching channels, the corresponding fault status register (0xD5[1]) is set to “1”, and the XSTAT_FLAG is pulled low. Also, the fault-detected channel information can be obtained by reading a status register 0xDA[3:0]). The system continues to operate. No hiccup or latch-off responses.
0	1	Hiccup (Auto Restart) When the overcurrent 2 (OC2) condition is detected at any of the PWM switching channels, the corresponding fault status register (0xD5[1]) is set to “1”, and the XSTAT_FLAG is pulled low. Also, the fault-detected channel information can be obtained by reading a status register 0xDA[3:0]). At the same time, the system stops PWM switching. The PWM switching recovers automatically 500ms (typical) after the OC2 condition is removed.
1	0	Latch-Off When the overcurrent 2 (OC2) condition is detected at any of the PWM switching channels, the corresponding fault status register (0xD5[1]) is set to “1”, and the XSTAT_FLAG is pulled low. Also, the fault detected channel information can be obtained by reading a status register 0xDA[3:0]). At the same time, the system stops PWM switching. The PWM switching is not recovered automatically. To recover the PWM switching, toggle PWM_EN or EN.
1	1	Flagging only (same as “0,0”)

Fault Phase Removal Control Bit (0XB6:Bit 5)

0xB6 Bit 5	Description
0 (Default)	No fault is triggered from phase disabling.
1	If more than half of the set number of phases are disabled writing into register 0xBC[3:0], hiccup or latch-off as set by register 0xB6 [6,7] is triggered.

Individual Fault Response Control Register 6 (0xB7)

Definition: BAT12 input and output overvoltage and undervoltage limit (protection) response setting.

Data Length in Bytes: 1

Data Format: Bit Field

Typical: R/W

Protectable: Yes

Default Value: 00h

Units: N/A

Register Name	Individual Fault Response Control Register 6 (0XB7)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	BAT12 Input Undervoltage Limit Fault Control Bits		BAT12 Input Overvoltage Limit Fault Control Bits		BAT12 Output Undervoltage Limit Fault Control Bits		BAT12 Output Overvoltage Limit Fault Control Bits	
Default Value	0	0	0	0	0	0	0	0

BAT12 Output Overvoltage Limit Fault Control Bit (0xB7: Bit 1:0)

If the individual fault response enable/disable control bit (0xB0[7]) is “1”, the device selects the fault response when BAT12 exceeds the second level of overvoltage threshold. If the individual fault response enable/disable control bit (0xB0[7]) is “0”, the “MODE” pin setting is used for the fault control and this register setting is ignored.

0xB7 Bit 1	0xB7 Bit 0	Description
0	0	Flagging only (Default) When the BAT12 output voltage exceeds the second overvoltage threshold, the corresponding fault status register (0xD7[0]) is set to “1”, and the XSTAT_FLAG is pulled low. The system continues to operate. No hiccup or latch-off responses.
0	1	Hiccup (Auto Restart) When the BAT12 output voltage exceeds the second overvoltage threshold, the corresponding fault status register (0xD7[0]) is set to “1”, and the XSTAT_FLAG is pulled low. At the same time, the system stops PWM switching. The PWM switching recovers automatically 500ms (typical) after the overvoltage condition is removed.
1	0	Latch-Off When the BAT12 output voltage exceeds the second overvoltage threshold, the corresponding fault status register (0xD7[0]) is set to “1”, and the XSTAT_FLAG is pulled low. At the same time, the system stops PWM switching. The PWM switching does not recover automatically when the overvoltage condition is removed. To recover the switching, toggle PWM_EN or EN.
1	1	Flagging only (same as “0,0”)

BAT12 Output Undervoltage Limit Fault Control Bit (0xB7: Bit 3:2)

If the individual fault response enable/disable control bit (0xB0[7]) is “1”, the device selects the fault response when BAT12 output voltage becomes lower than the second level of undervoltage threshold. If the individual fault response enable/disable control bit (0xB0[7]) is “0”, the “MODE” pin setting is used for the fault control and this register setting is ignored.

0xB7 Bit 3	0xB7 Bit 2	Description
0	0	Flagging only (Default) When the BAT12 output voltage becomes lower than the second undervoltage threshold, the corresponding fault status register (0xD7[1]) is set to “1”, and the XSTAT_FLAG is pulled low. The system continues to operate. No hiccup or latch-off responses.
0	1	Hiccup (Auto Restart) When the BAT12 output voltage is lower than the second Under voltage threshold, the corresponding fault status register (0xD7[1]) is set to “1”, and the XSTAT_FLAG is pulled low. At the same time, the system stops PWM switching. PWM switching recovers automatically 500ms (typical) after the undervoltage condition is removed.
1	0	Latch-Off When the BAT12 output voltage is lower than the second Under voltage threshold, the corresponding fault status register (0xD7[1]) is set to “1”, and the XSTAT_FLAG is pulled low. At the same time, the system stops PWM switching. PWM switching does not recover automatically when the undervoltage condition is removed. To recover the switching, toggle PWM_EN or EN.
1	1	Flagging only (same as “0,0”)

BAT12 Input Overvoltage Limit Fault Control Bit (0xB7: Bit 5:4)

If the individual fault response enable/disable control bit (0xB0[7]) is “1”, the device selects the fault response when the BAT12 input voltage exceeds the second level of overvoltage threshold. When the individual fault response enable/disable control bit (0xB0[7]) is “0”, the “MODE” pin setting is used for the fault control and this register setting is ignored.

0xB7 Bit 5	0xB7 Bit 4	Description
0	0	Flagging only (Default) When the BAT12 input voltage exceeds the second overvoltage threshold, the corresponding fault status register (0xD7[2]) is set to “1”, and the XSTAT_FLAG is pulled low. The system continues to operate. No hiccup or latch-off responses.
0	1	Hiccup (Auto Restart) When the BAT12 input voltage exceeds the second overvoltage threshold, the corresponding fault status register (0xD7[2]) is set to “1”, and the XSTAT_FLAG is pulled low. At the same time, the system stops PWM switching. PWM switching recovers automatically 500ms (typical) after the overvoltage condition is removed.
1	0	Latch-Off When the BAT12 input voltage exceeds the second overvoltage threshold, the corresponding fault status register (0xD7[2]) is set to “1”, and XSTAT_FLAG is pulled low. At the same time, the system stops PWM switching. The PWM switching does not recover automatically when the overvoltage condition is removed. To recover the switching, toggle PWM_EN or EN.
1	1	Flagging only (same as “0,0”)

BAT12 Input Undervoltage Limit Fault Control Bit (0xB7: Bit 7:6)

If the individual fault response enable/disable control bit (0xB0[7]) is “1”, the device selects the fault response when BAT12 becomes lower than the second level of undervoltage threshold. If the individual fault response enable/disable control bit (0xB0[7]) is “0”, the “MODE” pin setting is used for the fault control and this register setting is ignored.

0xB7 Bit 7	0xB7 Bit 6	Description
0	0	Flagging only (Default) When the BAT12 input voltage is lower than the second undervoltage threshold, the corresponding fault status register (0xD7[3]) is set to “1”, and XSTAT_FLAG is pulled low. The system continues to operate. No hiccup or latch-off responses.
0	1	Hiccup (Auto Restart) When the BAT12 input voltage is lower than the second undervoltage threshold, the corresponding fault status register (0xD7[3]) is set to “1”, and XSTAT_FLAG is pulled low. At the same time, the system stops PWM switching. PWM switching recovers automatically 500ms (typical) after the undervoltage condition is removed.
1	0	Latch-Off When the BAT12 input voltage becomes lower than the second undervoltage threshold, the corresponding fault status register (0xD7[3]) is set to “1”, and XSTAT_FLAG is pulled low. At the same time, the system stops PWM switching. PWM switching does not recover automatically when the undervoltage condition is removed. To recover the switching, toggle PWM_EN or EN.
1	1	Flagging only (same as “0,0”)

Individual Fault Response Control Register 7 (0xB8)

Definition: BAT48 input and output overvoltage and undervoltage limit (protection) response setting.

Data Length in Bytes: 1

Data Format: Bit Field

Typical: R/W

Protectable: Yes

Default Value: 00h

Units: N/A

Register Name	Individual Fault Response Control Register 7 (0XB8)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	BAT48 Input Undervoltage Limit Fault Control Bits		BAT48 Input Overvoltage Limit Fault Control Bits		BAT48 Output Undervoltage Limit Fault Control Bits		BAT48 Output Overvoltage Limit Fault Control Bits	
Default Value	0	0	0	0	0	0	0	0

BAT48 Output Overvoltage Limit Fault Control Bit (0xB8: Bit 1:0)

If the individual fault response enable/disable control bit (0xB0[7]) is “1”, the device selects the fault response when BAT48 exceeds the second level of overvoltage threshold. If the individual fault response enable/disable control bit (0xB0[7]) is “0”, the “MODE” pin setting is used for the fault control and this register setting is ignored.

0xB8 Bit 1	0xB8 Bit 0	Description
0	0	Flagging only (Default) When the BAT48 output voltage exceeds the second overvoltage threshold, the corresponding fault status register (0xD7[4]) is set to “1”, and XSTAT_FLAG is pulled low. The system continues to operate. No hiccup or latch-off responses.
0	1	Hiccup (Auto Restart) When the BAT48 output voltage exceeds the second overvoltage threshold, the corresponding fault status register (0xD7[4]) is set to “1”, and XSTAT_FLAG is pulled low. At the same time, the system stops PWM switching. PWM switching recovers automatically 500ms (typical) after the overvoltage condition is removed.
1	0	Latch-Off When the BAT48 output voltage exceeds the second overvoltage threshold, the corresponding fault status register (0xD7[4]) is set to “1”, and XSTAT_FLAG is pulled low. At the same time, the system stops PWM switching. PWM switching does not recover automatically when the overvoltage condition is removed. To recover the switching, toggle PWM_EN or EN.
1	1	Flagging only (same as “0,0”)

BAT48 Output Undervoltage Limit Fault Control Bit (0xB8: Bit 3:2)

If the individual fault response enable/disable control bit (0xB0[7]) is “1”, the device selects the fault response when BAT12 output voltage becomes lower than the second level of undervoltage threshold. If the individual fault response enable/disable control bit (0xB0[7]) is “0”, the “MODE” pin setting is used for the fault control and this register setting is ignored.

0xB8 Bit 3	0xB8 Bit 2	Description
0	0	Flagging only (Default) When the BAT48 output voltage is lower than the second undervoltage threshold, the corresponding fault status register (0xD7[5]) is set to “1”, and XSTAT_FLAG is pulled low. The system continues to operate. No hiccup or latch-off responses.
0	1	Hiccup (Auto Restart) When the BAT48 output voltage is lower than the second undervoltage threshold, the corresponding fault status register (0xD7[5]) is set to “1”, and XSTAT_FLAG is pulled low. At the same time, the system stops PWM switching. PWM switching recovers automatically 500ms (typical) after the undervoltage condition is removed.
1	0	Latch-Off When the BAT48 output voltage is lower than the second undervoltage threshold, the corresponding fault status register (0xD7[5]) is set to “1”, and XSTAT_FLAG is pulled low. At the same time, the system stops PWM switching. PWM switching does not recover automatically when the undervoltage condition is removed. To recover the switching, toggle PWM_EN or EN.
1	1	Flagging only (same as “0,0”)

BAT48 Input Overvoltage Limit Fault Control Bit (0xB8: Bit 5:4)

If the individual fault response enable/disable control bit (0xB0[7]) is “1”, the device selects the fault response when the BAT48 input voltage exceeds the second level of overvoltage threshold. When the individual fault response enable/disable control bit (0xB0[7]) is “0”, the “MODE” pin setting is used for the fault control and this register setting is ignored.

0xB8 Bit 5	0xB8 Bit 4	Description
0	0	Flagging only (Default) When the BAT48 input voltage exceeds the second overvoltage threshold, the corresponding fault status register (0xD7[6]) is set to “1”, and XSTAT_FLAG is pulled low. The system continues to operate. No hiccup or latch-off responses.
0	1	Hiccup (Auto Restart) When the BAT48 input voltage exceeds the second overvoltage threshold, the corresponding fault status register (0xD7[6]) is set to “1”, and XSTAT_FLAG is pulled low. At the same time, the system stops PWM switching. PWM switching recovers automatically 500ms (typical) after the overvoltage condition is removed.
1	0	Latch-Off When the BAT48 input voltage exceeds the second overvoltage threshold, the corresponding fault status register (0xD7[6]) is set to “1”, and XSTAT_FLAG is pulled low. At the same time, the system stops PWM switching. PWM switching does not recover automatically when the overvoltage condition is removed. To recover the switching, toggle PWM_EN or EN.
1	1	Flagging only (same as “0,0”)

BAT48 Input Undervoltage Limit Fault Control Bit (0xB8: Bit 7:6)

If the individual fault response enable/disable control bit (0xB0[7]) is “1”, the device selects the fault response when BAT12 is lower than the second level of undervoltage threshold. If the individual fault response enable/disable control bit (0xB0[7]) is “0”, the “MODE” pin setting is used for the fault control and this register setting is ignored.

0xB8 Bit 7	0xB8 Bit 6	Description
0	0	Flagging only (Default) When the BAT48 input voltage is lower than the second undervoltage threshold, the corresponding fault status register (0xD7[7]) is set to “1”, and XSTAT_FLAG is pulled low. The system continues to operate. No hiccup or latch-off responses.
0	1	Hiccup (Auto Restart) When the BAT48 input voltage is lower than the second undervoltage threshold, the corresponding fault status register (0xD7[7]) is set to “1”, and XSTAT_FLAG is pulled low. At the same time, the system stops PWM switching. PWM switching recovers automatically 500ms (typical) after the undervoltage condition is removed.
1	0	Latch-Off When the BAT48 input voltage is lower than the second undervoltage threshold, the corresponding fault status register (0xD7[7]) is set to “1”, and XSTAT_FLAG is pulled low. At the same time, the system stops PWM switching. PWM switching does not recover automatically when the undervoltage condition is removed. To recover the switching, toggle PWM_EN or EN.
1	1	Flagging only (same as “0,0”)

BAT12 Overvoltage Threshold Setting Register (0xB9)

Definition: BAT12 input and output overvoltage first level (warning) and second level (protection) threshold setting register.

Data Length in Bytes: 1

Data Format: Bit Field

Typical: R/W

Protectable: Yes

Default Value: 00h

Units: N/A.

Register Name	BAT12 Overvoltage Threshold Setting Register (0XB9)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Reserved		BAT12 Overvoltage (2nd Level = Protection Level) Threshold Setting Bit			BAT12 Overvoltage (1st level = Warning Level) Threshold Setting Bit		
Default Value	0	0	0	0	0	0	0	0

BAT12 Overvoltage (1st Level = Warning Level) Threshold Setting Bit (0xB9: Bit 2:0)

Sets the first level (warning level) of the BAT12 overvoltage fault threshold.

0xB9 Bit 2	0xB9 Bit 1	0xB9 Bit 0	Description
0	0	0	115% of BAT12 target voltage (default)
0	0	1	110% of BAT12 target voltage
0	1	0	120% of BAT12 target voltage
0	1	1	125% of BAT12 target voltage
1	0	0	130% of BAT12 target voltage
1	0	1	135% of BAT12 target voltage
1	1	0	140% of BAT12 target voltage
1	1	1	145% of BAT12 target voltage

BAT12 Overvoltage (2nd Level = Protection Level) Threshold Setting Bit (0xB9: Bit 5:3)

Sets the second level (protection level) of the BAT12 overvoltage fault threshold.

0xB9 Bit 5	0xB9 Bit 4	0xB9 Bit 3	Description
0	0	0	150% of BAT12 target voltage (default)
0	0	1	140% of BAT12 target voltage
0	1	0	130% of BAT12 target voltage
0	1	1	160% of BAT12 target voltage
1	0	0	170% of BAT12 target voltage
1	0	1	180% of BAT12 target voltage
1	1	0	190% of BAT12 target voltage
1	1	1	200% of BAT12 target voltage

BAT12 and BAT48 Undervoltage Threshold Setting Register (0xBA)

Definition: BAT12 and BAT48 input and output undervoltage level (first level = warning level) threshold setting register.

Data Length in Bytes: 1

Data Format: Bit Field

Typical: R/W

Protectable: Yes

Default Value: 00h

Units: N/A

Register Name	BAT12/BAT48 Undervoltage Threshold Setting Register (0XBA)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Reserved		BAT48 Undervoltage (1st Level = Warning Level) Threshold Setting Bit			BAT12 Undervoltage (1st Level = Warning Level) Threshold Setting Bit		
Default Value	0	0	0	0	0	0	0	0

BAT12 Undervoltage (1st Level = Warning Level) Threshold Setting Bit (0xBA: Bit 2:0)

Sets the first level (warning level) of the BAT12 undervoltage fault threshold.

0xBA Bit 2	0xBA Bit 1	0xBA Bit 0	Description
0	0	0	85% of BAT12 target voltage (default)
0	0	1	82.5% of BAT12 target voltage
0	1	0	80% of BAT12 target voltage
0	1	1	77.5% of BAT12 target voltage
1	0	0	75% of BAT12 target voltage
1	0	1	72.5% of BAT12 target voltage
1	1	0	87.5% of BAT12 target voltage
1	1	1	90% of BAT12 target voltage

BAT48 Undervoltage (1st Level = Warning Level) Threshold Setting Bit (0xBA: Bit 5:3)

Sets the first level (warning level) of the BAT48 undervoltage fault threshold.

0xBA Bit 5	0xBA Bit 4	0xBA Bit 3	Description
0	0	0	75% of BAT48 target voltage (default)
0	0	1	71% of BAT48 target voltage
0	1	0	67% of BAT48 target voltage
0	1	1	63% of BAT48 target voltage
1	0	0	58% of BAT48 target voltage
1	0	1	54% of BAT48 target voltage
1	1	0	79% of BAT48 target voltage
1	1	1	83% of BAT48 target voltage

BAT48 Overvoltage Threshold Setting Register (0xBB)

Definition: BAT48 input and output overvoltage (first (warning) level and second (protection) level) threshold setting register.

Data Length in Bytes: 1

Data Format: Bit Field

Typical: R/W

Protectable: Yes

Default Value: 00h

Units: N/A

Register Name	BAT48 Overvoltage Threshold Setting Register (0XBB)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Reserved		BAT48 Overvoltage (Second Level = Protection Level) Threshold Setting Bit			BAT48 Overvoltage (First Level = Warning Level) Threshold Setting Bit		
Default Value	0	0	0	0	0	0	0	0

BAT48 Overvoltage (1st Level = Warning Level) Threshold Setting Bit (0xBB: Bit 2:0)

Sets the first level warning level) of the BAT48 overvoltage fault threshold.

0xBB Bit 2	0xBB Bit 1	0xBB Bit 0	Description
0	0	0	108% of BAT48 target voltage (default)
0	0	1	110% of BAT48 target voltage
0	1	0	113% of BAT48 target voltage
0	1	1	117% of BAT48 target voltage
1	0	0	121% of BAT48 target voltage
1	0	1	125% of BAT48 target voltage
1	1	0	106% of BAT48 target voltage
1	1	1	104% of BAT48 target voltage

BAT48 Overvoltage (2nd Level = Protection Level) Threshold Setting Bit (0xBB: Bit 5:3)

Sets the second level (protection level) of the BAT48 Overvoltage fault threshold.

0xBB Bit 5	0xBB Bit 4	0xBB Bit 3	Description
0	0	0	125% of BAT48 target voltage (default)
0	0	1	129% of BAT48 target voltage
0	1	0	133% of BAT48 target voltage
0	1	1	138% of BAT48 target voltage
1	0	0	142% of BAT48 target voltage
1	0	1	146% of BAT48 target voltage
1	1	0	150% of BAT48 target voltage
1	1	1	121% of BAT48 target voltage

Individual Phase Removal Control Register (0xBC)

Definition: Individual phase removal control register.

Data Length in Bytes: 1

Data Format: Bit Field

Typical: R/W

Protectable: Yes

Default Value: 00h

Units: N/A

Register Name	Individual Phase Removal Control Register (0XBC)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	V6/V12 UV/OV Detection Enable/Disable Control Bit	Reserved	Reserved	Reserved	Disable Phase 4	Disable Phase 3	Disable Phase 2	Disable Phase 1
Default Value	0	0	0	0	0	0	0	0

Phase-1 PWM Operation Enable/Disable Control Bit (0xBC: Bit 0)

Disables (removes) Phase-1 PWM operation when desired.

0xBC Bit 0	Description
0	Enables PWM operation of Phase-1 (default)
1	Disables (removes) Phase-1

Phase-2 PWM Operation Enable/Disable Control Bit (0xBC: Bit 1)

Disable (remove) Phase-2 PWM operation when desired.

0xBC Bit 1	Description
0	Enables PWM operation of Phase-2 (default)
1	Disables (removes) Phase-2

Phase-3 PWM Operation Enable/Disable Control Bit (0xBC: Bit 2)

Disable (remove) Phase-3 PWM operation when desired.

0xBC Bit 2	Description
0	Enables PWM operation of Phase-3 (default)
1	Disables (removes) Phase-3

Phase-4 PWM Operation Enable/Disable Control Bit (0xBC: Bit 3)

Disable (remove) Phase-4 PWM operation when desired.

0xBC Bit 3	Description
0	Enables PWM operation of Phase-4 (default)
1	Disables (removes) Phase-4

V6/V12 Overvoltage/Undervoltage Detection Enable/Disable Control Bit (0xBC: Bit 7)
Enables or disables the V6/V12 overvoltage and undervoltage detection. V6 and V12 OV/UV are functional, but are not reported in the register.

0xBC Bit 7	Description
0	Enables V6/V12 OV/UV detection (default)
1	Disables V6/V12 OV/UV detection

Serious Fault Response Control Register (0xBD)

Definition: Serious fault response control register.

Data Length in Bytes: 1

Data Format: Bit Field

Typical: R/W

Protectable: Yes

Default Value: 00h

Units: N/A

Register Name	Serious Fault Response Control Register (0XBD)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Boost Mode BAT48 Short to GND Fault Response Control	Buck Mode BAT48 Short to GND Fault Response Control	Boost Mode Low-Side FET Short Fault Response Control	Buck Mode Low-Side FET Short Fault Response Control	Reserved	Buck Mode BAT12 Short to GND Fault Response Control	Boost Mode High-Side FET Short Fault Response Control	Buck Mode High-Side FET Short Fault Response Control
Default Value	0	0	0	0	0	0	0	0

Note: The ISL78224 detects potential serious fault conditions, such as external power MOSFET shorts, by monitoring the input/output voltages and continuous overcurrent situations. If a potential serious fault has been detected, the ISL78224 stops the PWMx outputs, which stops the converter, pulls down the “XSYS_FAIL” pin, and turns off the system immediately by using the external shutdown circuit. Even with this fault detection, however, there is a delay of a few switching cycles as the fault conditions are being determined. Therefore, this function is recommended for use as a supplemental fault detector rather than a primary fault detector.

Buck Mode High-Side MOSFET Short Fault Response Control Bit (0xBD: Bit 0)
Set the XSYS_FAIL function when detecting the potential short of high-side MOSFET in Buck mode operation.

0xBD Bit 0	Description
0	Pulls down XSYS_FAIL when the potential high-side MOSFET short is detected in Buck mode (default). PWM switching stops immediately and latched-off. To restart, toggle EN or PWM_EN.
1	Does not pull down XSYS_FAIL when the potential high-side MOSFET short is detected in Buck mode. PWM switching shuts off or keeps running depending on the related fault (OC2, BAT12 UV) response settings.

Boost Mode High-Side MOSFET Short Fault Response Control Bit (0xBD: Bit 1)

Sets the XSYS_FAIL function when detecting the potential short of high-side MOSFET in Boost mode operation.

0xBD Bit 1	Description
0	Pulls down XSYS_FAIL when the potential high-side MOSFET short is detected in Boost mode (default). PWM switching stops immediately and latches off. To restart, toggle EN or PWM_EN.
1	Does not pull down XSYS_FAIL when the potential high-side MOSFET short is detected in Buck mode. PWM switching shuts off or keeps running depending on the related fault (OC2, BAT48 UV, BAT12 OV) response settings.

Buck Mode BAT12 Short to GND Fault Response Control Bit (0xBD: Bit 2)

Sets the XSYS_FAIL function when detecting the potential short of high-side MOSFET in Buck mode operation.

0xBD Bit 2	Description
0	Pulls down XSYS_FAIL when the potential short of BAT12 to GND is detected in Buck mode (default). PWM switching stops immediately and latches off. To restart, toggle EN or PWM_EN.
1	Does not pull down XSYS_FAIL when the potential short of BAT12 to GND is detected in Buck mode. PWM switching shuts off or keeps running depending on the related fault (NOC, BAT12 UV) response settings.

Buck Mode Low-Side MOSFET Short Fault Response Control Bit (0xBD: Bit 4)

Sets the XSYS_FAIL function when detecting the potential short of low-side MOSFET in Buck mode operation.

0xBD Bit 4	Description
0	Pulls down XSYS_FAIL when the potential low-side MOSFET short is detected in Buck mode (default). PWM switching stops immediately and latches off. To restart, toggle EN or PWM_EN.
1	Does not pull down XSYS_FAIL when the potential low-side MOSFET short is detected in Buck mode. PWM switching shuts off or keeps running depending on the related fault (NOC, BAT12 UV) response settings.

Boost Mode Low-Side MOSFET Short Fault Response Control Bit (0xBD: Bit 5)

Sets the XSYS_FAIL function when detecting the potential short of low-side MOSFET in Boost mode operation.

0xBD Bit 5	Description
0	Pulls down XSYS_FAIL when the potential low-side MOSFET short is detected in Boost mode (default). PWM switching stops immediately and latches off. To restart, toggle EN or PWM_EN.
1	Does not pull down XSYS_FAIL when the potential low-side MOSFET short is detected in Boost mode. PWM switching shuts off or keeps running depending on the related fault (OC2, BAT12 UV) response settings.

Buck Mode BAT48 Short to GND Fault Response Control Bit (0xBD: Bit 6)

Sets the XSYS_FAIL function when detecting the potential short of BAT48 to GND in Buck mode operation.

0xBD Bit 6	Description
0	Pulls down XSYS_FAIL when the potential short of BAT48 to GND is detected in Buck mode (default). PWM switching stops immediately and latches off. To restart, toggle EN or PWM_EN.
1	Does not pull down XSYS_FAIL when the potential short of BAT48 to GND is detected in Buck mode. PWM switching shuts off or keeps running depending on the related fault (OC2, BAT12 UV) response settings.

Boost Mode BAT48 Short to GND Fault Response Control Bit (0xBD: Bit 7)

Set the XSYS_FAIL function when detecting the potential short of high-side MOSFET in Buck mode operation.

0xBD Bit 7	Description
0	Pulls down XSYS_FAIL when the potential short of BAT48 to GND is detected in Buck mode (default). PWM switching stops immediately and latches off. To restart, toggle EN or PWM_EN.
1	Does not pull down XSYS_FAIL when the potential short of BAT48 to GND is detected in Buck mode. PWM switching shuts off or keeps running depending on the related fault (OC2, BAT12 UV) response settings.

Minimum On-Time, Current Balancing Setting Register (0xBE)

Definition: Minimum on-time setting and current balance enable/disable control register.

Data Length in Bytes: 1

Data Format: Bit Field

Typical: R/W

Protectable: Yes

Default Value: 00h

Units: N/A

Register Name	Minimum On-Time, Current Balance Setting Register (0xBE)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Reserved				Current Balance Enable/Disable Control Bits		Minimum On-Time Setting Bits	
Default Value	0	0	0	0	0	0	0	0

Minimum On-Time Setting Bits (0xBE: Bit 1:0)

Sets the minimum on-time of PWM output pulses (minimum high-side FET on-time for Buck mode and minimum low-side FET on-time for Boost mode).

0xBE Bit1	0xBE Bit0	Description
0	0	340ns (default)
0	1	280ns
1	0	220ns
1	1	180ns

Current Balancing Circuit Enable/Disable Control Bits (0xBE: Bit 3:2)

Enables or disables the current balancing circuit within the device and between the devices.

0xBE Bit3	0xBE Bit2	Description
0	0	Disables the current balancing both within and between the devices (default).
0	1	Enables current balancing within the device, but disable the current balancing between the devices.
1	0	Disables the current balancing within the device and enable the current balancing between the devices.
1	1	Enables the current balancing both within and between the devices

Maximum On-Duty Setting Register (0xBF)

Definition: Maximum on-duty setting register.

Data Length in Bytes: 1

Data Format: Bit Field

Typical: R/W

Protectable: Yes

Default Value: 00h

Units: N/A

Register Name	Maximum On-Duty Setting Register (0xBF)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Reserved					Maximum On-Duty Setting Bits		
Default Value	0	0	0	0	0	0	0	0

Maximum On-Duty Setting Bits (0xBF: Bit 2:0)

Sets the maximum on-duty of the main switching FET (maximum on-duty of the high-side FET for Buck mode and the maximum on-duty of the low-side FET for Boost mode. This register also sets the maximum on-time duty ratio for the Flyback controller.

0xBF Bit2	0xBF Bit1	0xBF Bit0	Description
0	0	0	91.7% (default)
0	0	1	95.8%
0	1	0	87.5%
0	1	1	83.3%
1	0	0	79.2%
1	0	1	75.0%
1	1	0	Not assigned
1	1	1	Not assigned

Boot Refresh Control Register (0xEC)

Definition: Boot refresh control register/phase drop enable blanking time control register.

Data Length in Bytes: 1

Data Format: Bit Field

Typical: R/W

Protectable: Yes

Default Value: 00h

Units: N/A

Register Name	Boot Refresh Control Register (0xEC)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Reserved	Phase Drop Enable Blank Time After Phase-Added	Reserved	Boot Refresh Pulse Count	Boot Refresh Pulse Width Control Bit	Boot Refresh Interval Control Bits		
Default Value	0	0	0	0	0	0	0	0

Boot Refresh Interval Control Bits (0xEC: Bit 2:0)

Sets the interval of boot refresh pulses.

0xEC Bit 2	0xEC Bit 1	0xEC Bit 0	Description
0	0	0	500µs (default)
0	0	1	100µs
0	1	0	200µs
0	1	1	300µs
1	0	0	750µs
1	0	1	1ms
1	1	0	1.5ms
1	1	1	2ms

Boot Refresh Pulse Width Control Bit (0xEC: Bit 3)

Sets the boot refresh pulse width.

0xEC Bit 3	Description
0	1/12 of PWM pulse period (default)
1	1/6 of PWM pulse period

Boot Refresh Pulse Count (0xEC: Bit 4)

Sets the boot refresh pulse count.

0xEC Bit 4	Description
0	8 pulses at initial startup; 4 pulses during startup, phase drop, and pulse skipping
1	16 pulses at initial startup; 8 pulses during startup, phase drop, and pulse skipping

Phase Drop Enable Blanking Time after Phase-Add (0xEC: Bit 6)
Sets blanking time to re-enable phase drop after phase add.

0xEC Bit 6	Description
0	1.5ms (default)
1	10ms

CCL/ACL Threshold Control Register (0xED)

Definition: Constant Current Control Loop (CCL) kick-in threshold and Average Current Limit (ACL) kick-in threshold control register.

Data Length in Bytes: 1

Data Format: Bit Field

Typical: R/W

Protectable: Yes

Default Value: 00h

Units: N/A

Register Name	CCL/ACL Threshold Control Register (0xED)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Reserved		ACL Threshold Setting Bits			CCL Threshold Setting Bits		
Default Value	0	0	0	0	0	0	0	0

Constant Current Control Loop (CCL) Kick-in Threshold Setting Bits (0xED: Bit 2:0)
Sets the CCL kick-in threshold voltage.

0xED Bit2	0xED Bit1	0xED Bit0	Description
0	0	0	2.4V (default)
0	0	1	2.3V
0	1	0	2.2V
0	1	1	2.1V
1	0	0	2.0V
1	0	1	1.9V
1	1	0	1.8V
1	1	1	1.7V

Average Current Limit (ACL) Kick-in Threshold Setting Bits (0xED: Bit 5:3)
Sets the CCL kick-in threshold voltage.

0xED Bit5	0xED Bit4	0xED Bit3	Description
0	0	0	2.7V (default)
0	0	1	2.6V
0	1	0	2.5V
0	1	1	2.4V
1	0	0	2.3V
1	0	1	2.2V
1	1	0	2.1V
1	1	1	2.0V

WRITE_PROTECT (10h)

Definition: Controls writing to the ISL78224. This command provides protection against accidental changes. This command does not provide protection against deliberate changes to a device's configuration or operation. All supported commands may have their parameters read, regardless of the WRITE_PROTECT settings.

Data Length in Bytes: 1

Data Format: Bit Field

Typical: R/W Byte

Protectable: Yes

Default Value: 80h

Units: N/A

Command	WRITE_PROTECT (0x10)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Register Write Enable/Disable Control Bits	Reserved						
Default Value	1	0	0	0	0	0	0	0

Register Write Enable/Disable Control Bit (0x10: Bit 7)
Enable/disable register access.

0x10 Bit 7	Description
0	Enables writes to all registers
1	Disables all writes to the registers except to the WRITE_PROTECT command (default)

5.2 Status Registers

Status registers indicate the operation and error status of the device. An external MCU can poll the status any time to confirm the operation status of the device. Also, when any fault condition is detected, the XSTAT_FLAG pin is pulled down to notice the event of a fault to external MCU. Following the XSTAT_FLAG low signal, the MCU can find the fault location by reading the Fault Index register (0xC0) and the corresponding resistors that are indicated by the Fault Index register. The fault flag initiated at the Fault Status registers are kept until it is cleared by the "Clear All" command or by overriding the same value to the target register by the external MCU. To clear the faults, the Write Protection control bit must be set to "Write Enable" before sending the "Clear All" command or overriding the same value to the target register.

Fault Index Register (0xC0)

Definition: Indicates the register location having the fault flags.

Data Length in Bytes: 1

Data Format: Bit Field

Typical: R/W

Protectable: Yes

Default Value: 00h

Units: N/A

Register Name	Fault Index Register (0xC0)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	XSTAT_FLAG flag indicator	Fault on "Fault Status Register-7" (0xD8)	Fault on "Fault Status Register-6" (0xD7)	Fault on "Fault Status Register-5" (0xD6)	Fault on "Fault Status Register-4" (0xD5)	Fault on "Fault Status Register-3" (0xD4)	Fault on "Fault Status Register-2" (0xD3)	Fault on "Fault Status Register-1" (0xD2)
Default Value	0	0	0	0	0	0	0	0

Fault Indicator - Fault on "Fault Status Register-1 (0xD2)" (0xC0: Bit 0)

Indicates one or more faults are detected at "Fault Status Register-1 (0xD2)" if this bit is set to "1".

0xC0 Bit 0	Description
0	OK: No fault at "Fault Status Register-1 (0xD2)"
1	Faults are detected at "Fault Status Register-1 (0xD2)"

Fault Indicator - Fault on "Fault Status Register-2 (0xD3)" (0xC0: Bit 1)

Indicates one or more faults are detected at "Fault Status Register-2 (0xD3)" if this bit is set to "1".

0xC0 Bit 1	Description
0	OK: No fault at "Fault Status Register-2 (0xD3)"
1	Faults are detected at "Fault Status Register-2 (0xD3)"

Fault Indicator - Fault on "Fault Status Register-3(0xD4)" (0xC0: Bit 2)

Indicates one or more faults are detected at "Fault Status Register-3 (0xD4)" if this bit is set to "1".

0xC0 Bit 2	Description
0	OK: No fault at "Fault Status Register-3 (0xD4)"
1	Faults are detected at "Fault Status Register-3 (0xD4)"

Fault Indicator - Fault on “Fault Status Register-4 (0xD5)” (0xC0: Bit 3)
Indicates one or more faults are detected at “Fault Status Register-4 (0xD5)” if this bit is set to “1”.

0xC0 Bit 3	Description
0	OK: No fault at “Fault Status Register-4 (0xD5)”
1	Faults are detected at “Fault Status Register-4 (0xD5)”

Fault Indicator - Fault on “Fault Status Register-5 (0xD6)” (0xC0: Bit 4)
Indicates one or more faults are detected at “Fault Status Register-5 (0xD6)” if this bit is set to “1”.

0xC0 Bit 4	Description
0	OK: No fault at “Fault Status Register-5 (0xD6)”
1	Faults are detected at “Fault Status Register-5 (0xD6)”

Fault Indicator - Fault on “Fault Status Register-6 (0xD7)” (0xC0: Bit 5)
Indicates one or more faults are detected at “Fault Status Register-6 (0xD7)” if this bit is set to “1”.

0xC0 Bit 5	Description
0	OK: No fault at “Fault Status Register-6 (0xD7)”
1	Faults are detected at “Fault Status Register-6 (0xD7)”

Fault Indicator - Fault on “Fault Status Register-7 (0xD8)” (0xC0: Bit 6)
Indicates one or more faults are detected at “Fault Status Register-7 (0xD8)” if this bit is set to “1”.

0xC0 Bit 6	Description
0	OK: No fault at “Fault Status Register-7 (0xD8)”
1	Faults are detected at “Fault Status Register-7 (0xD8)”

Alert Flag Indicator (0xC0: Bit 7)
Indicates the fault is detected and the XSTAT_FLAG pin becomes “low” if this bit is set to “1”.

0xC0 Bit 7	Description
0	OK: No fault in the system
1	Faults are detected and XSTAT_FLAG pin pulled low.

Fault Status Register-1 (0xD2)

Definition: Fault Status Register-1 – BAT12/BAT48 overvoltage and undervoltage fault (warning level) status register.

Data Length in Bytes: 1

Data Format: Bit Field

Typical: R/W

Protectable: Yes

Default Value: 00h

Units: N/A

Register Name	Fault Status Register-1 (0xD2)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	BAT48 Input Undervoltage	BAT48 Input Overvoltage	BAT48 Output Undervoltage	BAT48 Output Overvoltage	BAT12 Input Undervoltage	BAT12 Input Overvoltage	BAT12 Output Undervoltage	BAT12 Output Overvoltage
Default Value	0	0	0	0	0	0	0	0

BAT12 Output Overvoltage (Warning Level) Flag (0xD2: Bit 0)

The device detected a BAT12 output overvoltage fault (warning level) in Buck mode.

0xD2 Bit 0	Description
0	OK: No BAT12 output overvoltage fault
1	BAT12 output overvoltage fault (warning level) is detected

BAT12 Output Undervoltage (Warning Level) Flag (0xD2: Bit 1)

The device detected a BAT12 output undervoltage fault (warning level) in Buck mode.

0xD2 Bit 1	Description
0	OK: No BAT12 output undervoltage fault
1	BAT12 output undervoltage fault (warning level) is detected

BAT12 Input Overvoltage (Warning Level) Flag (0xD2: Bit 2)

The device detected a BAT12 input overvoltage fault (warning level) in Boost mode.

0xD2 Bit 2	Description
0	OK: No BAT12 input overvoltage fault
1	BAT12 input overvoltage fault (warning level) is detected

BAT12 Input Undervoltage (Warning Level) Flag (0xD2: Bit 3)

The device detected a BAT12 input undervoltage fault (warning level) in Boost mode.

0xD2 Bit 3	Description
0	OK: No BAT12 input undervoltage fault
1	BAT12 input undervoltage fault (warning level) is detected

BAT48 Output Overvoltage (Warning Level) Flag (0xD2: Bit 4)
The device detected a BAT48 output overvoltage fault (warning level) in Boost mode.

0xD2 Bit 4	Description
0	OK: No BAT48 output overvoltage fault
1	BAT48 output overvoltage fault (warning level) is detected

BAT48 Output Undervoltage (Warning Level) Flag (0xD2: Bit 5)
The device detected a BAT48 output undervoltage fault (warning level) in Boost mode.

0xD2 Bit 5	Description
0	OK: No BAT48 output undervoltage fault
1	BAT48 output undervoltage fault (warning level) is detected

BAT48 Input Overvoltage (Warning Level) Flag (0xD2: Bit 6)
The device detected a BAT48 input overvoltage fault (warning level) in Buck mode.

0xD2 Bit 6	Description
0	OK: No BAT48 input overvoltage fault
1	BAT48 input overvoltage fault (warning level) is detected

BAT48 Input Undervoltage (Warning Level) Flag (0xD2: Bit 7)
The device detected a BAT48 Input Undervoltage fault (warning level) in Buck mode.

0xD2 Bit 7	Description
0	OK: No BAT48 input undervoltage fault
1	BAT48 input undervoltage fault (warning level) is detected

Fault Status Register-2 (0xD3)

Definition: Fault Status Register-2 – V_{IN} V6 V12 Flyback fault status register.

Data Length in Bytes: 1

Data Format: Bit Field

Typical: R/W

Protectable: Yes

Default Value: 00h

Units: N/A

Register Name	Fault Status Register-2 (0xD3)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	POR	BAT12 UVLO	V_{IN} Overvoltage	Flyback Switch Overcurrent	V12 Undervoltage	V12 Overvoltage	V6 Undervoltage	V6 Overvoltage
Default Value	0	0	0	0	0	0	0	0

V6 Overvoltage Flag (0xD3: Bit 0)

The device detected a V6 overvoltage fault.

0xD3 Bit 0	Description
0	OK: Not V6 overvoltage.
1	V6 overvoltage fault is detected.

V6 Undervoltage Flag (0xD3: Bit 1)

The device detected a V6 undervoltage fault.

0xD3 Bit 1	Description
0	OK: No V6 undervoltage fault.
1	V6 undervoltage fault is detected.

V12 Overvoltage Flag (0xD3: Bit 2)

The device detected a V12 overvoltage fault.

0xD3 Bit 2	Description
0	OK: Not V12 overvoltage.
1	V12 overvoltage fault is detected.

V12 Undervoltage Flag (0xD3: Bit 3)

The device detected a V12 undervoltage fault.

0xD3 Bit 3	Description
0	OK: No V12 undervoltage fault.
1	V12 undervoltage fault is detected.

Flyback Primary Side Overcurrent Flag (0xD3: Bit 4)
The device detected overcurrent at Flyback primary side.

0xD3 Bit 4	Description
0	OK: Flyback switching current is okay.
1	Overcurrent is detected at Flyback primary side.

V_{IN} Overvoltage Flag (0xD3: Bit 5)
The device detected a V_{IN} overvoltage fault.

0xD3 Bit 5	Description
0	OK: V_{IN} is lower than the overvoltage threshold.
1	V_{IN} Voltage is higher than the overvoltage threshold.

BAT12 UVLO Flag (0xD3: Bit 6)
BAT12 at current-sense amplifier input voltage is lower than the UVLO threshold.

0xD3 Bit 6	Description
0	OK: BAT12 is higher than the UVLO threshold.
1	BAT12 is lower than the UVLO threshold.

POR Flag (0xD3: Bit 7)
The device detected Power-On Reset (POR) condition.

0xD3 Bit 7	Description
0	OK: Normal operation
1	Detected a POR condition. The external MCU needs to load the control registers value if this bit is high. Clear this flag after completing data loading of the control registers.

Fault Status Register-3 (0xD4)

Definition: Fault Status Register-3 LDO output fault status register.

Data Length in Bytes: 1

Data Format: Bit Field

Typical: R/W

Protectable: Yes

Default Value: 00h

Units: N/A

Register Name	Fault Status Register-3 (0xD4)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Reserved		MCULDO Undervoltage	MCULDO Overvoltage	Reserved			PVCC Power-Good
Default Value	0	0	0	0	0	0	0	0

PVCC Power-Good Flag (0xD4: Bit 0)

Indicates whether PVCC/VCC is in normal operation range.

0xD4 Bit 0	Description
0	PVCC is okay (4.8V < PVCC < 5.6V).
1	PVCC is out of target range.

MCULDO Overvoltage Fault Flag (0xD4: Bit 4)

The device detected an MCULDO overvoltage fault.

0xD4 Bit 4	Description
0	OK: MCULDO is not overvoltage.
1	MCULDO overvoltage condition detected.

MCULDO Undervoltage Fault Flag (0xD4: Bit 5)

The device detected MCULDO undervoltage fault.

0xD4 Bit 5	Description
0	OK: MCULDO is not undervoltage
1	MCULDO undervoltage condition detected

Fault Status Register-4 (0xD5)

Definition: Fault Status Register-4 overcurrent and thermal fault status register.

Data Length in Bytes: 1

Data Format: Bit Field

Typical: R/W

Protectable: Yes

Default Value: 00h

Units: N/A.

Register Name	Fault Status Register-4 (0xD5)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Thermal Protection	Reserved	AOCP Fault	CCL Operation	Reserved	NOC at PWMx	OC2 Fault at PWMx	OC1 at PWMx
Default Value	0	0	0	0	0	0	0	0

OC1 Flag (0xD5: Bit 0)

Indicates whether the cycle-by-cycle Overcurrent 1 condition is detected.

When this flag is altered, OC1 has occurred and the phase location can be obtained by reading Fault Status Register-10 (0xD9).

0xD5 Bit 0	Description
0	OK: OC1 is not detected.
1	OC1 is detected at PWMx.

OC2 Fault Flag (0xD5: Bit 1)

Indicates whether the cycle-by-cycle Overcurrent 2 (OC2) condition is detected.

When this flag is altered, OC2 has occurred and the phase location can be obtained by reading Fault Status Register-11 (0xDA).

0xD5 Bit 1	Description
0	OK: OC2 is not detected.
1	OC2 is detected at PWMx.

NOC Fault Flag (0xD5: Bit 2)

Indicates whether a Negative Overcurrent (NOC) condition is detected.

When this flag is altered, an NOC has occurred and the phase location can be obtained by reading Fault Status Register-10 (0xD9).

0xD5 Bit 2	Description
0	OK: NOC is not detected.
1	NOC is detected at PWMx.

CCL Operation Indicator (0xD5: Bit 4)

Indicates the device is operating in Constant Current Control Loop (CCL) mode.

0xD5 Bit 4	Description
0	Not in CCL operation. (Constant Voltage Output).
1	Device is operating in CCL mode.

AOCP Fault Flag (0xD5: Bit 5)

Indicates the device detected Average Current Limit Protection (AOCP) fault.

0xD5 Bit 5	Description
0	OK: AOCP is not detected.
1	AOCP fault is detected.

Thermal Protection Fault Flag (0xD5: Bit 7)

Indicates the device has detected a thermal protection condition (T_J > +150°C).

0xD5 Bit 7	Description
0	OK: Normal temperature range. (T_J < +150°C).
1	Thermal Protection condition (T_J > +150°C) is detected.

Fault Status Register-5 (0xD6)

Definition: Serious overcurrent fault status register.

Data Length in Bytes: 1

Data Format: Bit Field

Typical: R/W

Protectable: Yes

Default Value: 00h

Units: N/A

Register Name	Fault Status Register-5 (0xD6)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Reserved			Continuous NCO	Reserved	Continuous OC2	Reserved	
Default Value	0	0	0	0	0	0	0	0

Continuous OC2 Fault Flag (0xD6: Bit 2)

Indicates an OC2 condition has continuously occurred and turned off the external FETs.

Potentially, the high-side NMOS is shorted in Buck mode, the low-side NMOS is shorted in Boost mode, or BAT12 is shorted to GND in Buck mode.

0xD6 Bit 2	Description
0	OK: No continuous OC2 condition is detected.
1	OC2 condition is continuously detected for more than three clock cycles and has turned off the external MOSFETs.

Continuous NOC Fault Flag (0xD6: Bit 4)

Indicates a NOC condition has continuously occurred and turned off the external FETs.

Potentially, the low-side NMOS is shorted in Buck mode, the high-side NMOS is shorted in Boost mode, or BAT48 is shorted to GND in Boost mode.

0xD6 Bit 4	Description
0	OK: No continuous NOC condition is detected.
1	NOC condition is continuously detected for more than three clock cycles and has turned off the external MOSFETs.

Fault Status Register-6 (0xD7)

Definition: Fault Status Register-6 – BAT12/BAT48 overvoltage and undervoltage limit fault (protection level) status register.

Data Length in Bytes: 1

Data Format: Bit Field

Typical: R/W

Protectable: Yes

Default Value: 00h

Units: N/A

Register Name	Fault Status Register-6 (0xD7)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	BAT48 Input Undervoltage Limit	BAT48 Input Overvoltage Limit	BAT48 Output Undervoltage Limit	BAT48 Output Overvoltage Limit	BAT12 Input Undervoltage Limit	BAT12 Input Overvoltage Limit	BAT12 Output Undervoltage Limit	BAT12 Output Overvoltage Limit
Default Value	0	0	0	0	0	0	0	0

BAT12 Output Overvoltage Limit (Protection Level) Fault Flag (0xd7: Bit 0)

The device detected a BAT12 output overvoltage limit fault (protection level) in Buck mode.

0xD7 Bit 0	Description
0	OK: No BAT12 output overvoltage limit fault .
1	BAT12 output overvoltage limit fault (protection level) is detected.

BAT12 Output Undervoltage Limit (Protection Level) Fault Flag (0xD7: Bit 1)

The device detected a BAT12 output undervoltage limit fault (protection level) in Buck mode.

0xD7 Bit 1	Description
0	OK: No BAT12 output undervoltage limit fault.
1	BAT12 output undervoltage limit fault (protection level) is detected.

BAT12 Input Overvoltage Limit (Protection Level) Fault Flag (0xD7: Bit 2)

The device detected a BAT12 Input Overvoltage Limit Fault (protection level) in Boost mode.

0xD7 Bit 2	Description
0	OK: No BAT12 input overvoltage limit fault.
1	BAT12 input overvoltage limit fault (protection level) is detected.

BAT12 Input Undervoltage Limit (Protection Level) Fault Flag (0xD7: Bit 3)

The device detected a BAT12 Input Undervoltage Limit Fault (protection level) in Boost mode.

0xD7 Bit 3	Description
0	OK: No BAT12 input undervoltage limit fault.
1	BAT12 input undervoltage limit fault (protection level) is detected.

BAT48 Output Overvoltage Limit (Protection Level) Fault Flag (0xD7: Bit 4)
The device detected a BAT48 output overvoltage limit fault (protection level) in Boost mode.

0xD7 Bit 4	Description
0	OK: No BAT48 output overvoltage limit fault.
1	BAT48 output overvoltage limit fault (protection level) is detected.

BAT48 Output Undervoltage Limit (Protection Level) Fault Flag (0xD7: Bit 5)
The device detected a BAT48 output undervoltage limit fault (protection level) in Boost mode.

0xD7 Bit 5	Description
0	OK: No BAT48 output undervoltage limit fault.
1	BAT48 output undervoltage limit fault (protection level) is detected.

BAT48 Input Overvoltage Limit (Protection Level) Fault Flag (0xD7: Bit 6)
The device detected a BAT48 input overvoltage limit fault (protection level) in Buck mode.

0xD7 Bit 6	Description
0	OK: No BAT48 input overvoltage limit fault.
1	BAT48 input overvoltage limit fault (protection level) is detected.

BAT48 Input Undervoltage Limit (Protection Level) Fault Flag (0xD7: Bit 7)
The device detected a BAT48 input undervoltage limit fault (protection level) in Buck mode.

0xD7 Bit 7	Description
0	OK: No BAT48 input undervoltage limit fault.
1	BAT48 input undervoltage limit fault (protection level) is detected.

Fault Status Register-7 (0xD8)

Definition: Fault Status Register-7 potential serious fault status register.

Data Length in Bytes: 1

Data Format: Bit Field

Typical: R/W

Protectable: Yes

Default Value: 00h

Units: N/A

Register Name	Fault Status Register-7 (0xD8)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Reserved			Flyback NMOS Short	BAT48 Short to GND	Low-Side NMOS Short	BAT12 Short to GND	High-Side NMOS Short
Default Value	0	0	0	0	0	0	0	0

Potential High-Side NMOS Short Flag (0xD8: Bit 0)

The device detected a potential external high-side NMOS short.

0xD8 Bit 0	Description
0	High-side NMOS not shorted
1	Potentially high-side NMOS is shorted

Potential BAT12 Short to GND Flag (0xD8: Bit 1)

The device detected the potential short of BAT12 to GND.

0xD8 Bit 1	Description
0	BAT12 is not shorted to GND.
1	Potentially BAT12 is shorted to GND.

Potential Low-Side NMOS Short Flag (0xD8: Bit 2)

The device detected the potential external low-side NMOS short.

0xD8 Bit 2	Description
0	Low-side NMOS not shorted.
1	Potentially low-side NMOS is shorted.

Potential BAT48 Short to GND Flag (0xD8: Bit 3)

The device detected the potential short of BAT48 to GND.

0xD8 Bit 3	Description
0	BAT48 is not shorted to GND.
1	Potentially BAT48 is shorted to GND.

Potential Switching NMOS Short at Flyback Flag (0xD8: Bit 4)

The device detected the potential short of switching NMOS of Flyback.

0xD8 Bit 4	Description
0	Flyback NMOS is not shorted.
1	Potentially Flyback NMOS is shorted.

Fault Status Register-8 (0xD9)

Definition: Fault Status Register-8 – OC1 or NOC fault channel indicator register

Data Length in Bytes: 1

Data Format: Bit Field

Typical: R/W

Protectable: Yes

Default Value: 00h

Units: N/A

Register Name	Fault Status Register-8 (0xD9)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Reserved		Reserved	Reserved	OC1 or NOC at Phase-4	OC1 or NOC at Phase-3	OC1 or NOC at Phase-2	OC1 or NOC at Phase-1
Default Value	0	0	0	0	0	0	0	0

OC1 or NOC at Phase-1 Indicator (0xD9: Bit 0)

The device detected the OC1 or NOC condition at Phase-1.

0xD9 Bit 0	Description
0	OK: No OC1 or NOC condition is detected at Phase-1.
1	OC1 or NOC is detected at Phase-1.

OC1 or NOC at Phase-2 Indicator (0xD9: Bit 1)

The device detected the OC1 or NOC condition at Phase-2.

0xD9 Bit 1	Description
0	OK: No OC1 or NOC condition is detected at Phase-2.
1	OC1 or NOC is detected at Phase-2.

OC1 or NOC at Phase-3 Indicator (0xD9: Bit 2)

The device detected the OC1 or NOC condition at Phase-3.

0xD9 Bit 2	Description
0	OK: No OC1 or NOC condition is detected at Phase-3.
1	OC1 or NOC is detected at Phase-3.

OC1 or NOC at Phase-4 Indicator (0xD9: Bit 3)

The device detected the OC1 or NOC condition at Phase-4.

0xD9 Bit 3	Description
0	OK: No OC1 or NOC condition is detected at Phase-4.
1	OC1 or NOC is detected at Phase-4.

Fault Status Register-9 (0xDA)

Definition: Fault Status Register-9 – OC2 fault channel indicator register.

Data Length in Bytes: 1

Data Format: Bit Field

Typical: R/W

Protectable: Yes

Default Value: 00h

Units: N/A

Register Name	Fault Status Register-9 (0xDA)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Reserved		Reserved	Reserved	OC2 at Phase-4	OC2 at Phase-3	OC2 at Phase-2	OC2 at Phase-1
Default Value	0	0	0	0	0	0	0	0

OC2 at Phase-1 Indicator (0xDA: Bit 0)

The device detected the OC2 condition at Phase-1.

0xDA Bit 0	Description
0	OK: No OC2 condition is detected at Phase-1.
1	OC2 is detected at Phase-1.

OC2 at Phase-2 Indicator (0xDA: Bit 1)

The device detected the OC2 condition at Phase-2.

0xDA Bit 1	Description
0	OK: No OC2 condition is detected at Phase-2.
1	OC2 is detected at Phase-2.

OC2 at Phase-3 Indicator (0xDA: Bit 2)

The device detected the OC2 condition at Phase-3.

0xDA Bit 2	Description
0	OK: No OC2 condition is detected at Phase-3.
1	OC2 is detected at Phase-3.

OC2 at Phase-4 Indicator (0xDA: Bit 3)

The device detected the OC2 condition at Phase-4.

0xDA Bit 3	Description
0	OK: No OC2 condition is detected at Phase-4.
1	OC2 is detected at Phase-4.

System Status Register-1 (0xDC)

Definition: System Status register 1.

Data Length in Bytes: 1

Data Format: Bit Field

Typical: R/W

Protectable: Yes

Default Value: 00h

Units: N/A

Register Name	System Status Register-1 (0xDC)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	PWM Output Ready	Reserved	PWM Output Mode	Protection Mode	Switching Mode	Device Position		Converter Direction
Default Value	-	0	-	-	-	-	-	0

Converter Direction (0xDC: Bit 0)

Indicates the current converter direction, Buck or Boost. Reflects the BT/BK pin status.

0xDC Bit 0	Description
0	Buck mode
1	Boost mode

Device Position (0xDC: Bit 2:1)

Indicates the device position in the system: Master, Slave-1, Slave-2, or Slave-3. Reflects the ADDR pin configuration, which is latched at the initialization period of device startup.

0xDC Bit 2	0XDC Bit 1	Description
0	0	Master
0	1	Slave-1
1	0	Slave-2
1	1	Slave-3

Switching Mode (0xDC: Bit 3)

Indicates the current switching mode (DE mode or Forced PWM mode) of the device. The register reflects the MODE pin configuration, which is latched at the initialization period of device startup.

0xDC Bit 3	Description
0	DE mode
1	Forced PWM mode

Protection Mode (0xDC: Bit 4)

Indicates the current pin configuration of Protection mode. Reflects the MODE pin configuration, which is latched at the initialization period of device startup. If the individual fault response setting is used, ignore this status bit and use individual fault response setting register values.

0xDC Bit 4	Description
0	Latch-Off mode
1	Hiccup mode

PWM Output Mode (0xDC: Bit 5)

Indicates the PWM output mode: 3-state or 2-state. Reflects the PWM_TRI pin configuration, which is latched at the initialization period of the device startup.

0xDC Bit 5	Description
0	2-state output
1	3-state output

PWM Output Ready (0xDC: Bit 7)

Indicates whether the PWM output is ready or not.

0xDC Bit 7	Description
0	PWM output is not ready. (For slave devices, this bit is always “0” because it is not controlling the DRV_EN).
1	PWM output is ready.

System Status Register-2 (0xDD)

Definition: System Status register 2.

Data Length in Bytes: 1

Data Format: Bit Field

Typical: R/W

Protectable: Yes

Default Value: 00h

Units: N/A

Register Name	System Status Register-2 (0xDD)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	Reserved	Configured Maximum Phase Count			Operating Phase Count			Phase Drop Enabled/Disabled
Default Value	0	-	-	-	-	-	-	-

Phase Drop Enabled or Disabled Indicator (0xDD: Bit 0)

Indicates whether the Phase Drop/Add function is enabled or disabled. Reflects the PD_CTRL pin configuration.

0xDD Bit 0	Description
0	Phase Drop/Add function is Enabled.
1	Phase Drop/Add function is Disabled. (For slave devices, this bit is always “1” because phase drop is controlled by the master device)

Operating Phase Count (0xDD: Bit 3:1)

These bits indicate the current operating phase count.

0xDC Bit 3	0xDC Bit 2	0xDC Bit 1	Description
1	1	1	4-phase operation
1	0	1	4-phase operation
0	1	1	3-phase operation
1	1	0	2-phase operation
1	0	0	Not assigned
0	1	0	Not assigned
0	0	1	Not assigned
0	0	0	Not assigned

Configured Maximum Operating Phase Count (0xDD: Bit 6:4)

These bits indicate the maximum operating phase count, which is configured by the hardware connection of PWMx pins and latched at the initialization period of device startup.

0xDC Bit 6	0xDC Bit 5	0xDC Bit 4	Description
0	0	0	4-phase operation
0	0	1	4-phase operation
0	1	0	3-phase operation (PWM4 is connected to VCC for 3-phase configuration)
0	1	1	2-phase operation (PWM 3 is connected to VCC for 2-phase configuration)
1	0	0	Not assigned
1	0	1	Not assigned
1	1	0	Not assigned
1	1	1	Setting Error (PWM1 or PWM2 is connected to VCC at startup of the device)

System Status Register-3 (0xDF)

Definition: System Status register 3.

Data Length in Bytes: 1

Data Format: Bit Field

Typical: R/W

Protectable: Yes

Default Value: 00h

Units: N/A

Register Name	System Status Register-3 (0xDF)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	FSYNC Status		PLL_COMP Short	Clock Source Changed	Soft ON Completed	SS Complete	PLL Locked	Clock Source
Default Value	0	0	-	-	-	-	-	-

Clock Source Indicator (0xDF: Bit 0)

Indicates which external clock or internal clock is used as the PWM clock source.

0xDD Bit 0	Description
0	Internal Clock (clock frequency is determined by the resistor connected between FSYNC and GND).
1	External Clock

PLL Locked Indicator (0xDF: Bit 1)

Indicates whether the PLL is properly locked. If the PLL is not locked, the system clock is not provided from CLKOUT and the PWM operation does not start.

0xDF Bit 1	Description
0	PLL is not locked.
1	PLL is locked and CLKOUT is ready to use.

Soft-Start Complete Indicator (0xDF: Bit 2)
Indicates whether the soft-start period of the main converter is finished.

0xDF Bit 2	Description
0	Soft-start period is not completed.
1	Soft-start period is completed.

Soft-On Period Complete Indicator (0xDF: Bit 3)
Indicates whether the soft-on period (Transition period from non-synchronous to synchronous (Forced PWM or DE) at the end of soft-start) is complete.

0xDF Bit 3	Description
0	Soft-on period.
1	Completed soft-on period (Normal operation).

Clock Source Change Indicator (0xDF: Bit 4)
Indicates when the clock source is changed from internal to external or external to internal.

0xDF Bit 4	Description
0	Clock source is stable (not changed).
1	Clock source change is detected.

PLL_COMP Short (0xDF: Bit 5)
Indicates that PLL_COMP is shorted.

0xDF Bit 5	Description
0	PLL_COMP is normal.
1	PLL_COMP is shorted to GND. PLL cannot lock and system may not startup.

FSYNC Current Status (0xDF: Bit 7:6)
FSYNC pin connection status indicator. (Error indicator)

0xDF Bit 7	0xDF Bit 6	Description
0	0	OK: FSYNC is connected to the frequency setting resistor properly or driven by the external clock.
0	1	FSYNC may be shorted to GND.
1	0	FSYNC is open or shorted to VCC.
1	1	Not used

Device ID (0xAD)

Definition: Device ID (device name) .

Data Format: Bit Field

Data Length: 2-byte

Typical: R

Default Value: Fixed to 0x8224

Units: N/A

Register Name	Device ID (0xAD)															
Format	Bit Field															
Bit Position	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
Access	Read Only															
Value (Fixed)	1	0	0	0	0	0	1	0	0	0	1	0	0	1	0	0

Chip Revision (0xAE)

Definition: Chip revision (internal chip revision control code)

Data Format: Bit Field

Data Length: 2-byte

Typical: R

Default Value: Fixed to 0x0C01

Units: N/A

Register Name	Device ID (0xAE)															
Format	Bit Field															
Bit Position	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
Access	Read Only															
Value (Fixed)	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	1

6. Application Information

There are several ways to define the external components and parameters of a bidirectional converter system. This section shows one example of how to select the parameters of the external components based on the typical application schematics as shown in Figure 3 on page 2. In the actual application, the parameters may need to be adjusted and additional components may be needed for the specific application regarding noise, physical sizes, thermal, testing, and/or other requirements.

6.1 Operation Mode Setting

The ISL78224 provides selection of operation mode configurations such as converter direction, switching mode (DE mode or Forced PWM mode), and master or slave configuration by the combination of the BT/BK, MODE, and ADDR pins.

6.1.1 Converter Boost or Buck Mode Selection

The BT/BK pin switches the direction of the converter between Boost mode and Buck mode. When the BT/BK is logic high, the ISL78224 operates in Boost mode. When the BT/BK is logic low, the device operates in Buck mode. The BT/BK pin can be controlled by an external microcontroller to change the converter direction. In a typical application, the direction is supposed to be changed after disabling the switching by setting PWM_EN to low. However, the ISL78224 also allows changing the direction with switching enabled. If the BT/BK direction is changed on the fly, the device stops the PWMx outputs, then detects the zero cross of the inductor current, and moves into the soft-start state to restart in the opposite direction. This scheme helps prevent large inrush current when the voltage at the new output side is lower than the target voltage.

Table 5. Boost or Buck Mode Selection

BT/BK Pin Level	Converter Direction
High	Boost
Low	Buck

6.1.2 PWM Output Mode Selection

The PWM_TRI pin must be connected to VCC to select 3-state output of the PWMx output pins. In the 3-state output mode, the external drivers need to recognize a middle level (2.5V) to turn off both the high-side and low-side MOSFETs. In 3-state output mode, the PWMx output high means the high-side MOSFETs are on and PWMx output low means that the low-side MOSFETs are on. Both upper and lower FETs are off while PWMx is at mid level.

6.1.3 Switching Mode and Fault Response Selection

The MODE pin is used to select the switching mode (Diode Emulation (DE) mode or Forced PWM (CCM) mode) and fault response (Hiccup or Latch-off). This pin has three internal threshold levels corresponding to four voltage states to determine the combination of switching mode and fault response. At the startup/initialization period of the device, a 30µA current is sourced from the MODE pin. By connecting the MODE pin to GND, VCC, or an external resistor from this pin to GND, the desired voltage level for the mode setting is generated and latched into the device. The relation between the MODE pin connection (resistor value) and operation mode is shown in Table 6.

Table 6. Switch Mode and Fault Response Selection

Mode Pin Voltage	Recommended Connection or Resistor at Mode Pin	DE Mode or Forced PWM	Hiccup or Latch
GND	GND	DE	Hiccup
1.0V	33.2kΩ	Forced PWM	Hiccup
2.05V	68.1kΩ	DE	Latch-Off
VCC	VCC	Forced PWM	Latch-Off

6.1.3.1 POR Faults that Involve BAT12 Going Through UVLO

If the ISL78224 detects a BAT12 UVLO condition, it enters a reset (POR) state and waits until this UVLO condition is removed. When the BAT12 voltage becomes greater than the UVLO threshold, the IC goes through the main state machine to soft-start and achieve normal switching if PWM_EN is high.

6.1.4 Master Controller and Slave Controller Setting

The connection of the ADDR pin determines whether the ISL78224 is used as the main controller (master) or a sub-controller (slave) when multiple ISL78224 devices are used in parallel.

As with the MODE pin, at the startup/initialization of the device, a 30µA current is sourced from the ADDR pin. By connecting this pin to GND, VCC, or an external resistor from this pin to GND, the desired voltage level for the device address setting is generated and latched into the device. The relation between the ADDR pin connection (resistor value) and master or slave selection is shown in Table 7.

The maximum number of phases is 8. The maximum number of devices is four, one master and three slaves. One example is four devices operating with three phases each. Another example is two devices operating with four phases.

Table 7. Master and Slave Selection

ADDR Pin Voltage	Recommended Connection or Resistor at ADDR Pin	Device Order (Master/Slave)
GND	GND	Master
1.0V	33.2kΩ	Slave-2
2.05V	68.1kΩ	Slave-3
VCC	VCC	Slave-1

If defined as a slave device, the Flyback controller, MCULDO, overvoltage and undervoltage detection/protection of BAT12 and BAT48, and the main feedback loops (GM amp, compensation loop, and tracking) are disabled. To communicate phase-dropping information and synchronize with the master device, the DRV_EN, PD_0, and PD_1 pins in the slave device are set to receive input signals from the master.

The slave devices also need to recognize how many slaves are connected in parallel to perform the proper phase shifting. For this purpose, the FB_BT and FB_BK pins are used as the slave device count indicator.

- If the system is configured as a 1-master/1-slave operation, connect the FB_BT and FB_BK pins of the slave device to GND
- If the system is configured as a 1-master/2-slave operation, connect the FB_BT and FB_BK pins of the slave devices to VCC
- If the system is configured as a 1-master/3-slave operation, connect the FB_BT and FB_BK pins of the slave devices to GND and VCC respectively

Table 8.

FB_BT Connection at Slave Device	FB_BK Connection at Slave Device	Number of Slave Devices
GND	GND	1
VCC	VCC	2
GND	VCC	3

If the system is configured with one device only, connect the ADDR pin of the device to GND.

6.2 Soft-Start Capacitor Selection

A soft-start capacitor connected from the SS pin to GND controls the startup dynamics of the main controller as indicated in Figures 6 and 7.Voltage error amplifier, Gm1, controls the output voltage. The lowest of the non-inverting inputs is used as the reference, while the feedback voltage is applied to the inverting input through the

BT/BK switch. A nominal soft-start current of 5µA is sourced from the SS pin to charge the SS capacitor voltage at a rate of 5µA/C, where C is the value of the soft-start capacitor. See the example in the "Buck to Boost and Boost to Buck Operation" on page 141. This soft-start voltage is clamped at 3.4V by the SS_Clamp circuit, higher than the reference voltage of 1.6V where steady-state operation begins to occur. An SS_PreBias circuit shortens the soft-start time if a voltage is already present at the selected output.

6.3 Output Voltage Setting

The target output voltage of BAT12 in Buck mode (V_{BAT12}) and BAT48 in Boost mode (V_{BAT48}) can be defined by Equations 2 and 3 on page 58. For details, refer to "Output Voltage Regulation Loop" on page 58.

6.4 Switching Frequency

Switching frequency is determined by requirements of transient response time, solution size, EMC/EMI, power dissipation and efficiency, ripple noise level, and input and output voltage range. Higher frequency can improve the transient response and help to reduce the solution size. However, this can increase the switching losses and EMC/EMI concerns. Thus, a balance of these parameters is needed when deciding the switching frequency.

When the switching frequency, f_{SW}, is decided, the frequency setting resistor, R_{FSYNC}, can be determined by Equation 1 on page 57.

6.5 Inductor Selection

While the converter is operating in steady-state Continuous Conduction Mode (CCM), the duty ratio of the main FET (high-side FET in Buck mode and low-side FET in Boost mode) is shown in Equations 15 and 16.

(EQ. 15) $$D_{Boost} = 1 - \frac{V_{BAT12}}{V_{BAT48}}$$

(EQ. 16) $$D_{Buck} = \frac{V_{BAT12}}{V_{BAT48}}$$

where D_{Boost} is the duty ratio of the low-side FET in boost configuration, and D_{Buck} is the duty ratio of the high-side FET in buck configuration.

Under this CCM condition, the inductor peak-to-peak ripple current of each phase in Boost and Buck mode can be calculated as shown in Equations 17 and 18, respectively:

(EQ. 17) $$I_{LBT(P-P)} = D_{Boost} \cdot T \cdot \frac{V_{BAT12}}{L}$$

(EQ. 18) $$I_{LBK(P-P)} = D_{Buck} \cdot T \cdot \frac{V_{BAT48} - V_{BAT12}}{L}$$

where T is the switching period ($1/f_{SW}$) of each phase and L is the inductance of each phase.

Because a design uses the same inductor for both Boost and Buck configuration, and assuming that the inductor ripple current in Boost and Buck mode are the same, from the previous equations, the inductor value is determined by Equation 19:

(EQ. 19) $$L = \left(1 - \frac{V_{BAT12}}{V_{BAT48}}\right) \cdot \frac{V_{BAT12}}{I_{L(P-P)} \cdot f_{SW}}$$

where $I_{L(P-P)}$ is the peak-to-peak inductor current in either Buck or Boost mode.

Use Equation 19 to calculate L, where values of V_{BAT12}, V_{BAT48}, and $I_{L(P-P)}$ are based on the considerations described in the following:

- One method is to select the minimum input voltage and the maximum output voltage under long term operation as the conditions to select the inductor. In this case, the inductor DC current is the largest
- The general rule is to select an inductor that has a ripple current $I_{L(P-P)}$ around 30% to 50% of the maximum inductor DC current. The individual maximum DC inductor current for the n-phase boost and buck converter can be estimated by Equations 20 and 21 on page 132, respectively. $P_{OUTBTmax}$ is the maximum DC output power in Boost mode and η_{BT} is the estimated efficiency in Boost mode

(EQ. 20) $$I_{LBTmax} = \frac{P_{OUTBTmax}}{V_{BAT12min} \cdot \eta_{BT} \cdot n}$$

(EQ. 21) $$I_{LBKmax} = \frac{P_{OUTBKmax}}{V_{BAT12min} \cdot \eta_{BK} \cdot n}$$

(EQ. 22) $$L_{min} = \left(1 - \frac{V_{BAT12min}}{V_{BAT48max}}\right) \cdot \frac{V_{BAt12min}^2 \cdot \eta \cdot n}{P_{OUTmax} \cdot K \cdot f_{SW}}$$

Using Equation 22 with the two conditions listed previously, a reasonable starting point for the minimum inductor value can be estimated from Equations 20 and 21. The value of K in Equation 22 is typically selected as 30%.

Increasing the value of the inductor reduces the ripple current and therefore the ripple voltage. However, the large inductance value can reduce the converter's response time to a load transient. This also reduces the ramp signal and can cause a noise sensitivity issue.

The peak current at maximum load condition must be lower than the saturation current rating of the inductor with enough margin. In the actual design, the largest peak current may be observed at some transient conditions like the start-up or heavy load transient. Therefore, the inductor's size needs to be determined with the consideration of these conditions.

To avoid exceeding the inductor's saturation rating, OC1 peak current limiting (refer to "Cycle-by-Cycle Overcurrent Limiting (OC1)" on page 74) should be selected below the inductor's saturation current rating.

6.6 Current Monitor Setting

The ISL78224 monitors inductor current continuously to provide the features of cycle-by-cycle peak overcurrent protections (OC1 and OC2), averaged inductor current monitoring (output current for Buck mode and input current for Boost mode), average Constant Current Loop (CCL), Average Overcurrent Protection (AOCP), and phase dropping. For more information about the current-sensing scheme, refer to "Current Sense" on page 61.

6.7 IMON Resistor and Average Constant Current Loop (CCL) Threshold Setting

As described in "Current Monitoring — IMON" on page 62, the IMON current is proportional to the total inductor current (output current in Buck mode and input current in Boost mode).

Equation 7 on page 62 describes the buck IMON current and Equation 8 on page 62 describes the boost IMON pin current when R_{IMON} is connected from the IMON pin to GND.

Because the IMON voltage is used for average Constant Current Loop (CCL) control, the IMON resistor (R_{IMON}) value needs to be selected considering the CCL threshold voltage, which is clamped at the CCL current level in normal operation. In the default setting, the CCL threshold voltage is set at 2.4V (typical). The CCL threshold voltage can be changed from 1.7V to 2.4V in 0.1V steps by register settings using the I^2C/PMBus. Use the "CCL/ACL Threshold Control Register (0xED)" on page 106 to accomplish this. For more information about CCL function, refer to "Average Constant Current Control Loop (CCL)" on page 66. To set the CCL current level at I_{CCL} using the CCL threshold level of V_{CCL}, the R_{IMON} value is calculated with Equation 23:

(EQ. 23) $$R_{IMON} = V_{IMON} \cdot I_{IMON}$$

To realize higher accuracy output/input current monitoring, a 0.1% tolerance resistor for R_{IMON} is recommended.

To filter out the ripple voltage at the IMON pin, connect an X5R or X7R ceramic capacitor from the IMON pin to GND. This capacitor can range from 0.1µF to 1µF.

When multiple ISL78224 devices are used in parallel, Equation 23 can be used for the R_{IMON} calculation by adding up all of the currents from the various IMON pins. It is required to place the R_{IMON} resistor and filter capacitor close to each of the IMON pins of each device.

6.8 Phase Drop/Add Control

During low power operation, switching losses dominate the efficiency curve and losses are reduced by switching a fewer number of FETs (phases). During high current operation, conduction losses dominate the efficiency curve and losses are reduced by operating more FETs essentially in parallel by increasing the number of operational phases. For a given constant phase count, the efficiency curve arcs to a peak and decreases as higher currents are applied as shown in Figure 136. The goal of phase adding/dropping is to turn on more phases when the current is higher, and it is advantageous from an efficiency perspective to do so. Conversely, it is advantageous to turn off phases at lower currents when a lower operating phase count would result in a higher efficiency. The optimum phase add/drop load current can be established by plotting efficiency as a function of inductor current for the two highest phase counts being considered and noting the inductor current at the efficiency intersection. The ISL78224 exhibits ~40mV of hysteresis on the IMON pin between adding and dropping.

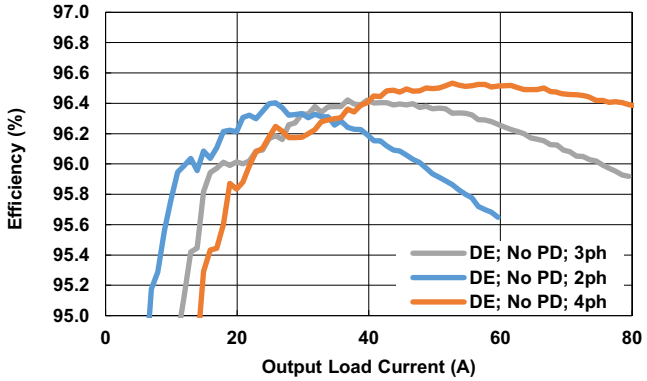


Figure 136. Determination of Optimum Phase Add Threshold

As described in "Automatic Phase Dropping/Adding" on page 64, the ISL78224 provides the phase dropping/adding function to improve the light-load efficiency. This is accomplished by comparing the IMON pin voltage with the PD_CTRL pin voltage to add or drop phases.

The PD_CTRL pin sources 40µA of constant current to generate a reference voltage (V_{PDCTRL}), which corresponds to the maximum (100%) level of the phase dropping/adding control voltage. Typically, the maximum phase dropping/adding control voltage should be set equal to, or slightly lower than, the IMON voltage level at the CCL threshold. The resistor value at the PD_CTRL pin can be calculated using Equation 24.

(EQ. 24) $$R_{PDCTRL} = \frac{V_{PDCTRL}}{40\mu A}$$

Based on this setting, the typical phase dropping/adding threshold is shown in Table 9.

Table 9. Phase Add/Drop Thresholds

Configured Maximum Phase Count	Phase Count Transition	Phase Drop Threshold (% V_{IMON}/ V_{PDCTRL})	Phase Add Threshold (% V_{IMON}/ V_{PDCTRL})
4	4 - 3	87.7	89.4
	3 - 2	83.8	85.5
3	3 - 2	86.8	88.5

For the stable operation of phase dropping/adding, it is recommended to place a 1000pF or larger ceramic capacitor (X5R or X7R) between the PD_CTRL pin and GND.

If the Phase Dropping/Adding feature is not required, connect the PD_CTRL pin to VCC.

6.9 V_{IN} Input Capacitor

Depending upon the system input power rail conditions, aluminum electrolytic type capacitors are normally used to provide a stable input voltage. Ceramic capacitors must be placed near the VIN and PGND pin of the IC. Multiple ceramic capacitors including 1µF and 0.1µF are recommended. Place these capacitors as close as possible to the IC.

6.10 PVCC and VCC Filter Capacitor

To provide a quiet power rail to the internal analog circuitry, an RC filter between PVCC and VCC is required. A 10Ω resistor between PVCC and VCC and at least 1µF ceramic capacitor from VCC to GND are recommended.

6.11 MCULDO Setting

The MCULDO is an LDO output that can be used to bias external components such as a microcontroller. Its output voltage can be adjusted with an external resistive voltage divider connected from MCULDO to GND. The resistor center tap should be connected to MCULDO_FB. The MCULDO_FB pin is the inverting input of an error amplifier with a reference of 1.2V. The MCULDO output voltage is expressed by Equation 25 where R_{UPPER} and R_{LOWER} are the upper and lower voltage divider resistors, respectively.

(EQ. 25) $$V_{MCUVDD} = \frac{1.2V \cdot (R_{LOWER} + R_{UPPER})}{R_{LOWER}}$$

Bypass the MCULDO output with a 10µF ceramic capacitor in parallel with a 0.1µF ceramic capacitor.

6.12 External Flyback Converter Setup

The ISL78224 supports the control functions of a Flyback converter that can be used to generate a 6V and 12V rail to bias the V6 and V12 pins, respectively. Refer to Figures 6 and 7. The voltages into V6 and V12 are fed back and combined in ratio to form the inverting input of a voltage (gm) error amplifier, an internal signal designated FB_FLY. The internal flyback reference is combined at a gm amplifier that is compensated at the COMP_FLY pin. The soft-start pin, SS_FLY, controls the turn-on time during the soft-start period, which is determined by the value of the capacitor connected to the SS_FLY pin. The Flyback controller soft-start current is nominally 5.2µA supplied by an internal source. The flyback soft-start voltage is given by Equation 26 when starting from a discharged soft-start capacitor.

(EQ. 26) $$V(t)_{SSFLY} = \frac{t \cdot 5.2 \cdot 10^{-6}}{C_{SS}}$$

The flyback soft-start voltage is clamped at 3.4V, but control is turned over to the reference at the reference crossing. GDRV_FLY is the output that drives the gate of an external N_CH FET, which ultimately controls the output voltages of the Flyback regulator.

The external flyback power processing components are a flyback transformer (actually a coupled inductor with three windings), an N_CH FET, two diodes, input and output capacitors, and a shunt resistor sensing primary current.

The flyback transformer is selected or specified first by having a primary inductance low enough so that sufficient energy is absorbed during the on-time to support the on- and off-time power requirements at minimum input voltage. The turns ratio of the two secondaries should be 2:1 because of the 2:1 nature of the V12 to V6 voltage.

The N_CH FET should be chosen to support the off-time voltage. The off-time voltage is the sum of the flyback input voltage and the voltage reflected back through the $V_{PRIMARY}$/V12 turns ratio, plus spikes due to layout and transformer leakage inductances. A snubber (voltage clamp) can limit the voltage on the FET during the off-time,

also shown in Figures 6 and 7. The FET should also have a sufficiently low $r_{DS(ON)}$ to support the high-peak primary current during the on time.

Two diodes are required that allow current flow to their respective outputs during the FET off time. The voltage on the diodes during their off time is the output voltage (V6 or V12) minus a negative voltage reflected from primary to secondary winding, in addition to spikes. The FET needs to accommodate the primary voltage and the voltage reflected from the secondary.

Energy is delivered to the output only during the FET off time. Capacitors at the V6 and V12 outputs clamp voltage as they absorb current, causing a voltage increase (ripple) at each output. The amplitude of this voltage ripple is inversely proportional to the value of the respective output capacitor. During the FET on-time, charge is drained off of these capacitors by their respective loads and their voltage ramps down.

Connect a shunt resistor from the FET source to GND. The voltage on this shunt is connected through a filter to ISP_FLY and ISN_FLY. The peak value of this voltage controls the duty ratio. The pulse terminates prematurely if this peak voltage reaches 75mV, on a cycle-by-cycle basis resulting in power limiting to V6 and V12. Again, it is required to connect this shunt Kelvin style and not allow the PCB layout tool to merely connect the GND side of the shunt to the GND plane.

6.13 Capacitor Selection for BAT48 and BAT12

To filter the inductor ripple current into an acceptably smooth voltage and to have sufficiently bounded voltage transient response to a change in current, “input” and “output” capacitors are required. In the case of the bidirectional converter BAT48 and BAT12, capacitors are both “input” and “output” in the same design and must support both functions. A combination of ceramic and electrolytic capacitors is normally used.

The ceramic capacitors filter the high frequency components (spikes) of the main switching devices. In layout, these ceramic capacitors must be placed as close as possible to the main switching devices to maintain the smallest inductance and resistance in the switching loop. To maintain capacitance over the biased voltage and temperature range, good quality ceramic capacitors such as X7R or X5R are recommended.

Electrolytic capacitors normally handle load transients and switching ripple. A physical electrolytic capacitor can be modeled by an ideal capacitor in series with a relatively small value resistor designated the Equivalent Series Resistance (ESR). The capacitor voltage is the product of this series impedance times the capacitor current. Multiple capacitors in parallel are recommended to handle the RMS currents.

The ripple currents can be determined by running a time domain simulation over a periodic switching interval. Renesas provides a Simplis model of this device on the Renesas web site.

6.14 FET Driver IC Selection

The ISL78224 is capable of controlling 3-state FET drivers from its PWMx signals. The PWMx signals out of the ISL78224 are set to 3-state by connecting the PWM_TRI pin to VCC.

The ISL78420 is an example of a high quality 3-state driver and works well with the ISL78224.

6.15 Power MOSFET Selection

Carefully select the external MOSFETs driven by the driver IC to optimize the design of the bidirectional regulator.

The MOSFETs’ BV_{DSS} rating needs to have enough voltage margin against the maximum boost output voltage plus the phase node voltage transient during switching.

The MOSFET V_{GS} rating needs to be considered while selecting the FETs. The V_{GS} rating needs to comply with the driver’s output voltage. A 20V gate-to-source rating is suggested.

The MOSFET should have low total gate charge (Q_g), low ON-resistance ($r_{DS(ON)}$), and small gate resistance (R_g <1.5Ω is recommended). The minimum V_{GS} threshold also needs to be considered in order to prevent false turn-on by noise spikes due to high dV/dt during phase node switching.

6.16 Driver Bootstrap Capacitor Selection

In general, the power required for the high-side MOSFET drive is provided by the boot capacitor connected between the BOOT and PHASE pins of the driver. The bootstrap capacitor can be chosen using Equation 27:

(EQ. 27) $$C_{BOOT} > \frac{Q_{gate}}{\Delta V_{BOOT}}$$

where Q_{gate} is the total gate charge of the high-side MOSFET(s) and ΔV_{BOOT} is the maximum droop voltage across the bootstrap capacitor while turning on the high-side MOSFET.

Though the maximum charging voltage across the bootstrap capacitor is the driver supply voltage minus the bootstrap diode drop (~0.4V), large excursions below GND by the PHASE node should be considered when selecting the bootstrap capacitor voltage rating. A 50V ceramic capacitor is recommended in a typical application with the ISL78420 driver. To keep enough capacitance over the biased voltage and temperature range, a good quality capacitor such as an X7R or X5R is recommended. Refer to the guidance contained in the driver datasheet.

6.17 Loop Compensation Design - Boost

The ISL78224 uses constant frequency peak current mode control architecture with a transconductance amplifier for the error amp. Figures 137 and 138 show the conceptual schematic and control block diagram.

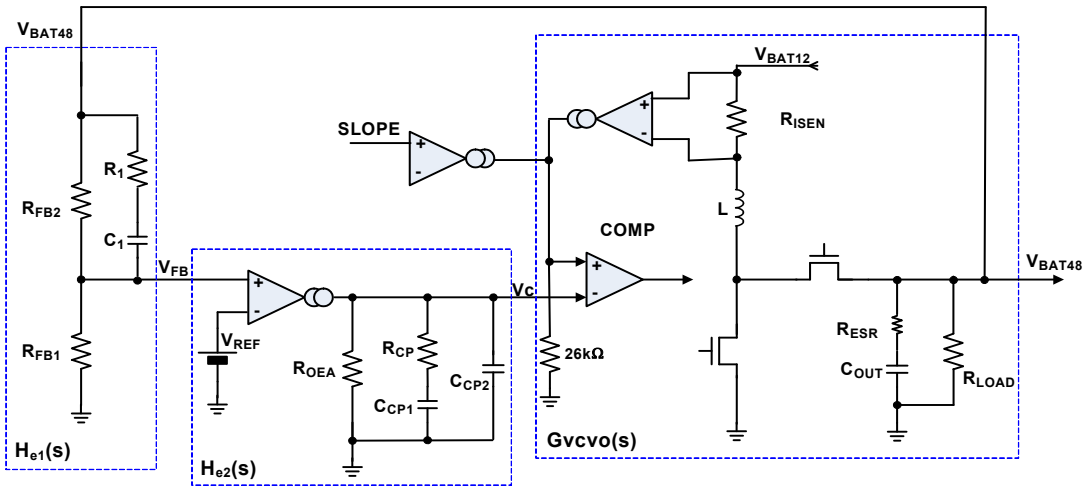


Figure 137. Conceptual Block Diagram of Peak Current Mode Controlled Boost Regulator

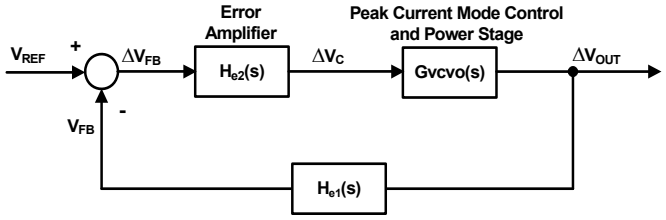


Figure 138. Conceptual Control Block Diagram

6.17.1 Boost Powerstage Transfer Function

The transfer function from the error amplifier control output, V_C, to the output voltage, V_{OUT}, is given by Equation 28 where "s" is the Laplace complex number frequency parameter "$\sigma + j\omega$", ω is the radian frequency $2\pi f$ and f_{SW} is the switching frequency of each phase.

(EQ. 28) $$G_{vcvo}(s) = K_{DC} \cdot \frac{\left(1 + \frac{s}{\omega_{ESR}}\right) \cdot \left(1 - \frac{s}{\omega_{RHZ}}\right)}{\left(1 + \frac{s}{\omega_{PS}}\right) \cdot \left(1 + \frac{s}{Q_p \cdot \pi \cdot f_{SW}} + \left(\frac{s}{\pi \cdot f_{SW}}\right)^2\right)}$$

The K_{DC} variable describes the low frequency gain, or gain at DC. This gain in a Current Mode Boost regulator is determined by regulator load (R_{LOAD}), the Duty Cycle (D) and the gain from the current sense resistor voltage to the PWM Comparator (K_{ISEN}).

(EQ. 29) $$K_{DC} = \frac{R_{LOAD} \cdot (1 - D)}{2 \cdot K_{ISEN}}$$

K_{ISEN} is the current sense gain shown in Equation 30, where R_{SENx} and R_{SETx} are the per-phase current sense resistors and setting resistors described in "Current Sense" on page 61. The ratio of R_{SENx} and R_{SETx} establishes the transimpedance of the current sense amplifier, the output current is attenuated 25%, and then it is applied to a 26kΩ resistor accounting for the 19,500 factor. N is the number of phases.

(EQ. 30) $$K_{ISEN} = \frac{R_{SENx} \cdot 19500}{R_{SETx} \cdot N}$$

The AC response of the power stage is determined by the zeros contributed by Right Half-Plane Zero (RHPZ) of boost modulation and the ESR zero from the C_{OUT} resistance, and Poles contributed by the load resistance in parallel with the output capacitance (C_{OUT}), and the slope compensation double-pole.

A power stage RHPZ occurs in all switching topologies where a switch interrupts the current flowing from the inductor to the output capacitance. When the PWM modulator is commanded to increase power output in response to a load change, the increase in D causes a decrease in the time that the inductor is connected to the output capacitor and load. This action causes the output voltage to temporarily droop, which is the opposite of the command. This effect in the frequency domain appears as a zero in amplitude but acts as a pole in phase (90° of phase loss). The loop design must avoid the RHPZ to maintain good phase margin so the RHPZ limits loop bandwidth to typically 20% or less of the full-load RHPZ frequency. The RHPZ parameters are R_{LOAD}, the total equivalent load resistance ($R_{LOAD} = V_{OUT}/I_{OUT\_total}$), D is the boost converter duty cycle ($D = 1 - V_{IN}/V_{OUT}$ or $D = (V_{OUT} - V_{IN})/V_{OUT}$) and L_{eq} is the equivalent inductance for the multiphase boost which is the inductance of the single phase inductor and divided by the number of power stage phases. Because L_{eq} is in the denominator, reducing L_{eq} increases the available loop bandwidth, while at the same time increases ripple current thereby increasing AC loses. If there is any significant net inductance in the Power Distribution Network (PDN) it must also be included in this calculation. This also applies to the buck loop design as PDN's effective inductance is seen in the buck bode plots as an RHPZ. Adequate decoupling capacitance is used to negate this effect.

(EQ. 31) $$\omega_{RHZ} = \frac{R_{LOAD} \cdot (1 - D)^2}{L_{eq}}$$

The ESR Zero parameters are simply C_{OUT}, the total output capacitance of the multiphase boost converter, and R_{ESR}, the output capacitor's Equivalent Series Resistance (ESR) of the total output capacitor bank.

(EQ. 32) $$\omega_{ESR} = \frac{1}{C_{OUT} \cdot R_{ESR}}$$

The Powerstage Pole radian frequency is:

(EQ. 33) $$\omega_{PS} = \frac{2}{C_{OUT} \cdot R_{LOAD}}$$

In the denominator of $G_{VCVO}(s)$, the power stage pole is multiplied by a quadratic polynomial containing the term Q_P, the variable that indicates the "quality" of damping provided by slope compensation for the double-pole at half the switching frequency caused by current mode sampling. Q_P is dependent upon D, the duty cycle, and the expression S_e/S_n, which means the rate of the slope compensation signal compared to the

rate of a single-phase inductor current signal at the PWM comparator during the on-time. It can be calculated by Equation 34, where K_{SLOPE} is the selected ratio of the rate of the slope compensation signal compared to the rate of a single-phase inductor current signal at the PWM comparator during the off-time, and using the worst case condition (highest di/dt), which is V_{BAT48_MAX} and V_{BAT12_MIN} (refer to "Adjustable Slope Compensation" on page 62).

$$\frac{S_e}{S_n} = \frac{K_{SLOPE} \cdot (VBAT48\_MAX - VBAT12\_MIN)}{VBAT12\_MIN} \quad \text{(EQ. 34)}$$

$$Q_p = \frac{1}{\pi \cdot \left[(1-D) \cdot \frac{S_e}{S_n} + 0.5 - D\right]} \quad \text{(EQ. 35)}$$

6.17.2 Compensation Design: Boost

Generally, simple Type-2 compensation stabilizes the loop response. In the actual application however, extra phase margin can be provided by Type-3 compensation. Figure 139 shows the circuit diagram of a Type-3 compensation network.

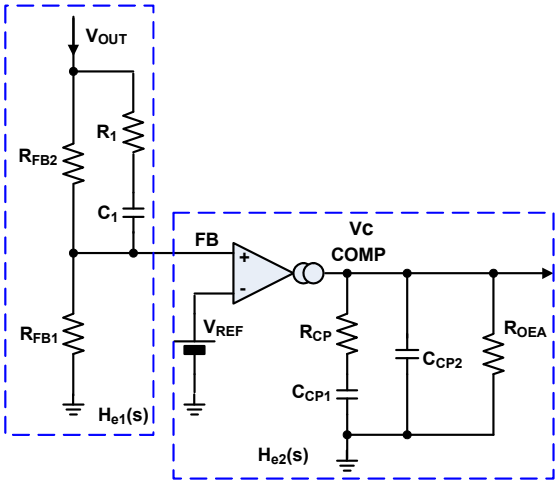


Figure 139. Type-3 Compensation

The transfer function of the compensation network is shown in Equation 36.

$$H_{e2}(s) = \frac{V_C}{V_{FB}} = g_m \cdot Z_{COMP} = g_m \frac{(1+sR_{CP}C_{CP1})R_{OEA}}{1+s[R_{CP}C_{CP1}+R_{OEA}(C_{CP1}+C_{CP2})]+C_{CP2}C_{CP1}R_{CP}R_{OEA}s^2} \quad \text{(EQ. 36)}$$

R_{OEA} (approximately 100MΩ) is the gm error amplifier's output impedance and is much greater than the impedances of R_{CP}, C_{CP1}, and C_{CP2}. Assuming that R_{OEA} = infinite, the equation can be simplified as Equation 37:

$$H_{e2}(s) = g_m \cdot \frac{1+s \cdot R_{CP} \cdot C_{CP1}}{s \cdot C_{CP1} \cdot (1+s \cdot R_{CP} \cdot C_{CP2})} = \frac{\omega_1}{s} \cdot \frac{1+\frac{s}{\omega_{z2}}}{1+\frac{s}{\omega_{p2}}} \quad \text{(EQ. 37)}$$

where:

$$\omega_{p2} = \frac{g_m}{C_{CP1}} \quad \text{(EQ. 38)}$$

$$\omega_{z2} = \frac{1}{R_{CP} \cdot C_{CP1}} \quad \text{(EQ. 39)}$$

(EQ. 40) $$\omega_{p3} = \frac{1}{R_{CP} \cdot C_{CP2}}$$

g_m is the transconductance of the error amplifier, $g_m = 340\mu s$ for this device.

If Type-3 compensation is desired, the transfer function from the output voltage to the error amp input is shown in Equation 41:

(EQ. 41) $$H_{e1}(S) = \frac{R_{FB1}}{R_{FB1} + R_{FB2}} \cdot \frac{1 + \frac{s}{\omega_{z1}}}{1 + \frac{s}{\omega_{p1}}}$$

where:

(EQ. 42) $$\omega_{z1} = \frac{1}{C_1 \cdot (R_{FB2} + R_1)}$$

(EQ. 43) $$\omega_{p1} = \frac{1}{C_1 \cdot \frac{R_{FB2} \cdot R_{FB1} + R_{FB2} \cdot R_1 + R_{FB1} \cdot R_1}{R_{FB2} + R_{FB1}}}$$

The total transfer function with compensation network and gain stage are expressed:

(EQ. 44) $$G_{open}(s) = G_{vcvo}(s) \cdot H_{e1}(s) \cdot H_{e2}(s)$$

Use $f = \omega/2\pi$ to convert the pole and zero expressions to frequency domain, and from Equation 28, 36, 41, and 44, select the compensation's pole and zero locations. The poles (ω_{Px}) are used to reduce the loop gain, thereby limiting the loop bandwidth to prevent oscillation, but also to reduce the loop phase. The zeros (ω_{Zx}) increase loop gain (or flatten out the effect of the poles) to increase loop bandwidth and increase phase. It is desirable to have as much gain and bandwidth as possible, but the power stage components limit this.

In general, as described earlier, Type-2 compensation is adequate. Typically, the crossover frequency is set 20% or less of the ω_{RHZ} frequency. For the compensation as a general rule, set $\omega_{p2}/2\pi$ at a very low frequency; set $\omega_{z2}/2\pi$ at 1/5 of the crossover frequency; set $\omega_{p3}/2\pi$ at the ESR zero or the RHPZ frequency $\omega_{RHZ}/2\pi$, whichever is lower.

6.18 Loop Compensation Design: Buck

Figures 140 and 138 on page 136 show the conceptual schematic and control block diagram for the Buck operation.

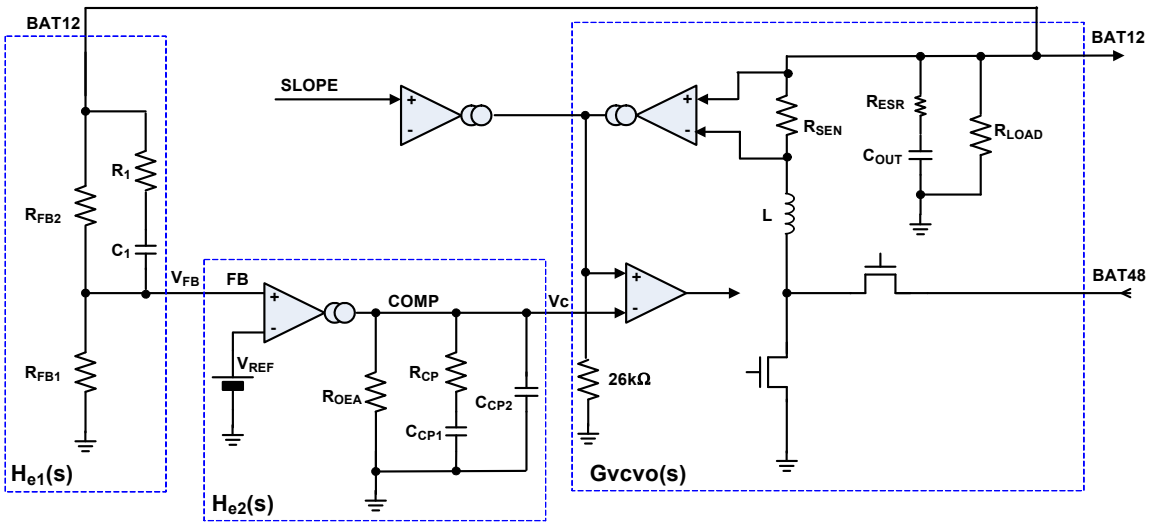


Figure 140. Conceptual Block Diagram of Peak Current Mode Controlled Buck Regulator

6.18.1 Buck Powerstage Transfer Function

The transfer function from the error amplifier output V_C to the output voltage V_{OUT} is shown in Equation 45.

$$G_{vcvo}(s) = K_{DC} \cdot \frac{\left(1 + \frac{s}{\omega_{ESR}}\right)}{\left(1 + \frac{s}{\omega_{PS}}\right) \cdot \left(1 + \frac{s}{Q_p \cdot \pi \cdot f_{SW}} + \left(\frac{s}{\pi \cdot f_{SW}}\right)^2\right)} \quad \text{(EQ. 45)}$$

where:

$$K_{DC} = \frac{R_{LOAD}}{K_{ISEN}} \cdot \frac{1}{1 + \frac{R_{LOAD} \cdot \left[(1-D) \cdot \frac{S_e}{S_n} + 0.5 - D\right]}{f_{SW} \cdot L_{eq}}} \quad \text{(EQ. 46)}$$

$$\omega_{esr} = \frac{1}{C_{OUT} \cdot R_{ESR}} \quad \text{(EQ. 47)}$$

$$\omega_{PS} = \frac{1}{C_{OUT} \cdot R_{LOAD}} + \frac{1}{L_{eq} \cdot f_{SW} \cdot C_{OUT}}\left[(1-D) \cdot \frac{S_e}{S_n} + 0.5 - D\right] \quad \text{(EQ. 48)}$$

$$Q_p = \frac{1}{\pi\left[(1-D) \cdot \frac{S_e}{S_n} + 0.5 - D\right]} \quad \text{(EQ. 49)}$$

where the parameters are interpreted below:

- R_{LOAD} is the total equivalent load resistance, $R_{LOAD} = V_{OUT}/I_{OUT\_total}$.
- D is buck converter duty cycle. $D = V_{OUT}/V_{IN}$
- K_{ISEN} is the current sense gain as shown in Equation 50, where R_{SENx} and R_{SETx} are per phase current sense resistors and setting resistor is described in "Current Sense" on page 61. N is the number of phases.

$$K_{ISEN} = \frac{R_{SENx} \cdot 19500}{R_{SENx} \cdot N} \quad \text{(EQ. 50)}$$

- L_{eq} is the equivalent inductance for the multiphase buck that can be expressed as Equation 51, in which L is the inductance of the per phase inductor and N is the number of phases:

$$L_{eq} = \frac{L}{N} \quad \text{(EQ. 51)}$$

- f_{SW} is the switching frequency of each phase.
- R_{ESR} is the output capacitor's Equivalent Series Resistance (ESR) of the total output capacitors.
- C_{OUT} is the total output capacitance of the multiphase buck converter.
- Se/Sn is gain of the SELECTED compensating slope over the sensed inductor current up-ramp. It can be calculated by Equation 52, where K_{SLOPE} is the selected gain of the compensating slope over the sensed I_L worst case down ramp slope assuming the worst case being VOUT_MAX (refer to "Adjustable Slope Compensation" on page 62)

$$\frac{S_e}{S_n} = \frac{K_{SLOPE} \cdot V_{OUTmax}}{V_{IN} - V_{OUT}} \quad \text{(EQ. 52)}$$

6.18.2 Compensation Design: Buck

The buck compensation network uses the same Type-2 or Type-3 configuration network described in "Compensation Design: Boost" on page 138 (refer to Figure 139). The transfer functions for Type-2 and Type-3 compensation are given in Equations 36 and 41 on page 139.

Similar to the boost application, usually Type-2 compensation can be used to stabilize the control loop. In the actual application, if extra phase margin is desired, Type-3 compensation can be used.

As a general rule in compensation design, the crossover frequency is typically set at 1/5 to 1/10 of the switching frequency f_{SW}; $\omega_{p2}/2\pi$ is set at a very low frequency; $\omega_{z2}/2\pi$ is set at 1/5 of the crossover frequency; set $\omega_{p3}/2\pi$ at the ESR zero frequency, or 0.35 to 0.5 times the switching frequency, whichever is lower. If Type-3 compensation is needed, set $\omega_{z1}/2\pi$ at 1/5 of the crossover frequency to get extra phase margin; set $\omega_{p1}/2\pi$ at frequency somewhere higher than $\omega_{z1}/2\pi$ (by 5 to 10 times as an example).

6.19 Loop Compensation Design – Boost and Buck

Type 2 compensation is recommended unless power processor parasitics are well understood.

The inductance of the input cables connected to the capacitance at the input terminals comprises an input filter. The dynamic input resistance of a switcher run with a constant load is negative because input current goes down as the input voltage goes up. The equivalent filter must have an output impedance smaller in magnitude than the magnitude of the input impedance of the switcher in order to achieve stability. This is achieved by designing the source with low inductance cabling, selecting input capacitors of adequate value, and designing for the maximum required load.

6.20 Buck to Boost and Boost to Buck Operation

Figures 121 and 122 on page 54 show the operation of the transition between Buck to Boost and Boost to Buck of the ISL78224, respectively. The test was performed using 12V and 48V batteries to simulate real-world conditions. The outputs were not loaded during the test. The top trace is the BT/BK pin. When the BT/BK pin is logic-level high (>2V), the ISL78224 is operating in Boost mode. When the BT/BK pin is logic-level low (<0.8), the operation is Buck mode. The second trace from the top is the soft-start pin (SS). The soft-start timing is adjusted by the value of a capacitor connected between the SS pin and ground. The value of the capacitor on the SS pin for this test was 0.068µF. There is a 5µA bias current charging the SS cap that creates the SS voltage ramp (dt = C*dv/5µA). The conditions of the test resulted in a delta v and t of about 1.5V. Then, dt = (1.5V*0.068µF)/5µA = close to 20ms as seen in both curves. The last two curves show the supply rails (no loads) of the batteries used during the test.

7. Layout Considerations

For DC/DC converter designs, the PCB layout is very important to ensure the desired performance.

(1) Place input ceramic capacitors as close as possible to the VIN and AGND/PGND pins of the IC.

(2) Place high quality ceramic bypass capacitors as close as possible to the power MOSFET stack from BAT48 to GND, see Figure 143. Keep this loop (ceramic bypass capacitors and MOSFET stack) as small as possible for each phase to reduce voltage spikes induced by the trace parasitic inductances when the MOSFETs are switching ON and OFF.

(3) Place aluminum electrolytic capacitors across BAT48 close to the power MOSFET stack as well.

(4) Keep the phase node copper area small in order to minimize capacitive coupling, but large enough to handle the load current and heat sinking requirements.

(5) Place aluminum electrolytic and some ceramic capacitors close to the BAT12 side of the inductors and lower power MOSFET sources.

(6) Place multiple vias under the thermal pad of the IC. Connect the thermal pad to the ground copper plane with as large an area as possible in multiple layers to effectively reduce the thermal impedance. Figure 141 shows the layout example for vias on the IC bottom pad.

(7) Place a 10µF ceramic decoupling capacitor from the PVCC pin to GND as close as possible to the IC. Place multiple vias close to the ground pad of this capacitor.

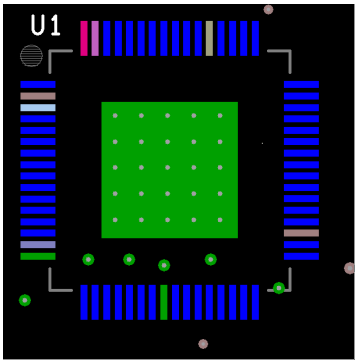


Figure 141. Recommended Layout Pattern for Vias on the IC Bottom Pad

(8) Place a high quality 1µF decoupling ceramic capacitor from the VCC pin to GND, and as close as possible to the IC. Place multiple vias close to the ground pad of this capacitor.

(9) Regarding the driver ICs, keep the bootstrap capacitor as close as possible to the driver IC. Minimize both the resistance and inductance of this connection.

(10) Keep the gate and source driver traces to the FETs as short as possible and with relatively large width (25 mil to 40 mil is recommended), and avoid using vias or a minimal number of vias in the driver path to achieve the lowest impedance, in other words avoid series vias.

(11) Place the current-sense setting resistors and the filter capacitor (shown as R_{SETxB}, R_{BIASxB}, and C_{ISENx} in Figure 130 on page 61) as close as possible to the IC. Keep each pair of the traces close to each other to avoid undesired switching noise injection.

(12) The current-sensing traces must be laid out very carefully since they carry tiny signals with only tens of mV. For the current-sensing traces close to the power sense resistor (R_{SENx}), the layout pattern shown in Figure 142 on page 143 is recommended. Assuming the R_{SENx} is placed on the top layer (red), route one current-sense connection from the middle of one R_{SENx} pad in the top layer under the resistor (red trace). For the other current-sensing trace (green trace), from the middle of the other pad on R_{SENx} top layer, after a short distance, via down to the second layer, and route this trace right under the top layer current-sense trace.

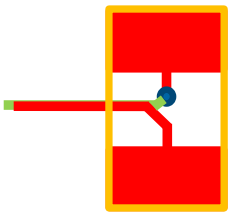


Figure 142. Recommended Layout Pattern for Current-Sense Traces Regulator

(13) Keep the current-sensing traces far from noisy traces such as gate driving traces (LGx, UGx, and PHx), phase nodes in the power stages, BOOTx signals, output switching pulse currents, driving bias traces, input inductor ripple current signals, etc. It is recommended that these two traces per phase are shielded between two quiet ground planes.

7.1 Layout Philosophy

The objective of a good printed circuit board layout is to isolate noisy aggressor traces (voltage nodes) from quiet signal victim traces. An aggressor trace is one that is capable of impressing an artifact of itself onto another signal trace, called the victim. This can be accomplished by two mechanisms. Rapidly changing currents cause rapidly changing magnetic fields. These fields impress this artifact onto a potential victim trace via mutual inductance, or Faraday's law. As the victim trace is separated in distance from the source of the magnetic field the disturbance is decreased. The second method is that an aggressor trace that has a rapidly changing voltage can capacitively couple an artifact of its voltage signal to the victim via changing the electric field. Again as before, the mitigation is to separate the victim from the aggressor.

- Place ceramic capacitor(s) as close as possible to the IC's constant voltage pins such as PVCC, V6, MCULDO, V12, BAT12, and VCC to prevent them from becoming victims. The ground side of these "bypass" capacitors should connect with low impedance (resistance plus inductance) to the IC thermal pad and ground pins of the IC. Short and wide traces with no vias is optimum.
- The most major example of an aggressor trace is the phase node(s). They carry both high switching current and voltage, and with fast transition rates. The major components of the phase node are two FETs and an inductor. Trapezoidal current flows alternately from each of the FETs to the inductor. The inductor current is a triangular combination of the two trapezoids. Consider two current loops, one when the high-side FET is on and the other when the low-side FET is on, see Figure 143. When the high-side FET is on, provide for a local source of current from a bypass capacitor. Connect this local input voltage source capacitor, the input side to the drain of the high-side FET, and the ground side to the source of the low-side FET. Minimize the impedance of this node to the ground side of the output capacitors by using a ground plane. The area of the phase node must be kept small to minimize capacitive coupling to other nodes, but large enough to dissipate heat from the power processing components. Do not route potential victim traces near any phase node.

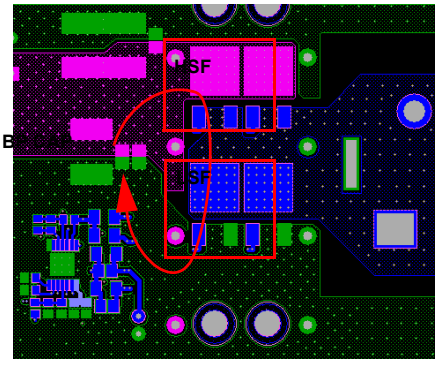


Figure 143. Recommended Layout Pattern for Phase Node

- A “boot” voltage needs to be generated at each FET driver IC because N-channel FETs require a gate-to-source voltage higher than any voltage otherwise available in an application to turn them on. This is achieved by charging a boot capacitor during the on-time of the low-side FET. This capacitor acts as the power source for the high-side FET driver. Although average currents are very low, peak currents for short time intervals are very high. The boot capacitor should be connected to the driver IC via very low impedance routing, wide, and short.
- The four external FET drivers, both low-side and high-side, require low impedance connections to their respective gates and sources. Use short and wide routing traces, ideally with no vias. If vias are used, place multiple vias side by side to minimize routing resistance.
- Place multiple vias under the thermal pad of the IC and connect them to all of the available ground planes. Each parallel via represents a thermal conductor and an electrical admittance. Use them liberally, see Figure 141 on page 142.
- The ISL78224 controller IC issues four PWMx signals that command the driver ICs to control the FETs. The PWMx signals are tri-state and noise may cause incorrect selection of the proper FET state. These traces should not be routed near aggressors such as phase nodes nor should they be routed near potential victims such as current-sense shunt feedback traces.
- Current-sensing resistors, sometimes called “shunts”, require special considerations during their layout. These devices must be connected Kelvin style as shown in Figure 142 on page 143. The sensed voltage must be sensed exactly at the shunt terminals. A common problem encountered routing shunts, is that if one side of the shunt is connected to a common terminal, such as GND or BAT12, a layout tool does not flag an error if this connection is not geometrically correct! Verify that the shunts are Kelvin connected. Specific to the ISL78224, each of the four phase resistors measure current into or out of BAT12, and the flyback shunt measures current into ground. Voltages measured on shunts are always necessarily small. They are also the most common victim seriously enough affected by a layout error to render the layout inoperable. Do not route shunt traces near aggressors such as phase nodes. Shunt routing and the controller IC itself should be placed favoring the lower noise BAT12 side of the board. Current-sense trace pairs should be placed side by side or one on top of the other as shown in Figure 142.

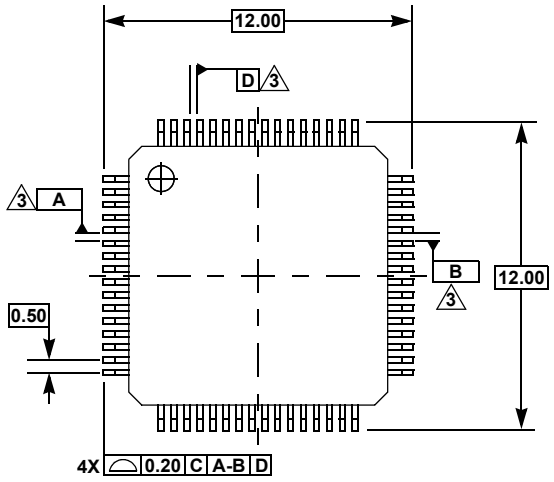
8. Revision History

Rev.	Date	Description
0.00	Oct 10, 2018	Initial release.

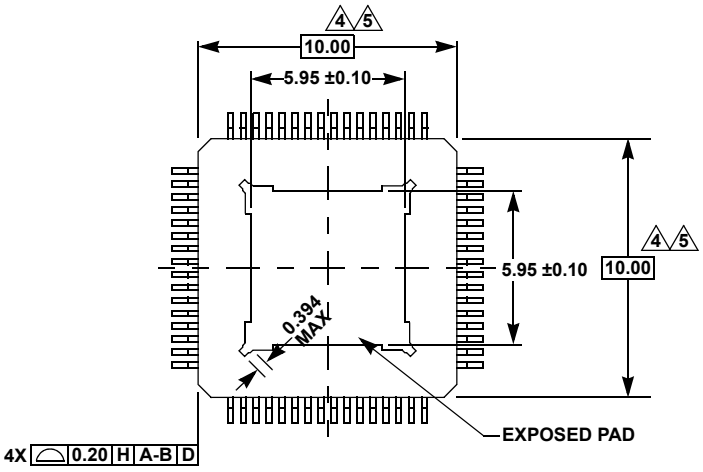
9. Package Outline Drawing

For the most recent package outline drawing, see Q64.10x10H.

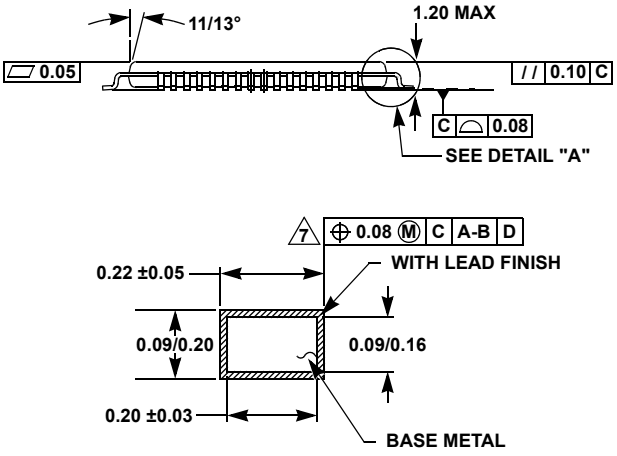
Q64.10x10H
64 LEAD THIN PLASTIC QUAD FLATPACK PACKAGE WITH EXPOSED PAD (EP-TQFP)
Rev 0, 4/15



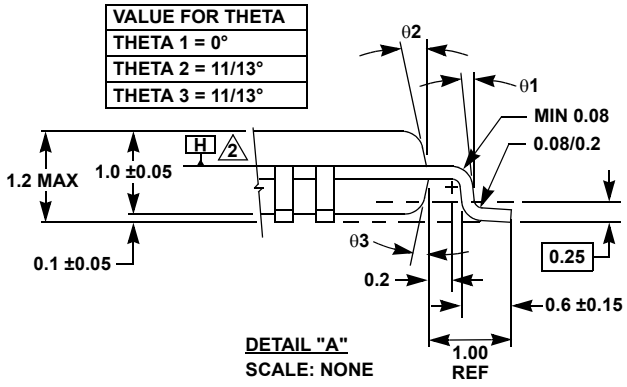
TOP VIEW



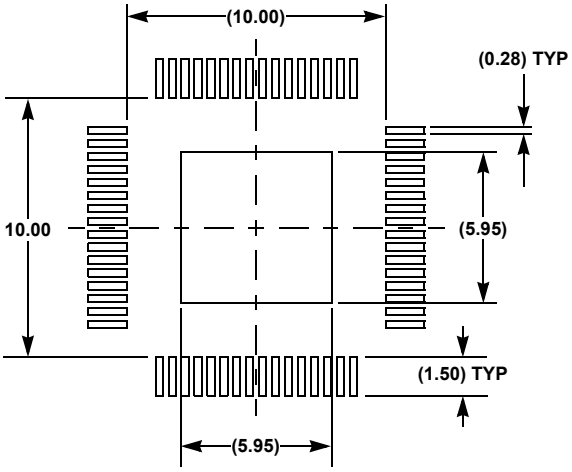
BOTTOM VIEW



VALUE FOR THETA
THETA 1 = 0°
THETA 2 = 11/13°
THETA 3 = 11/13°



DETAIL "A"
SCALE: NONE



RECOMMENDED LAND PATTERN

NOTES:

1. All dimensioning and tolerancing conform to ANSI Y14.5-1982.
2. Datum plane H located at mold parting line and coincident with lead, where lead exits plastic body at bottom of parting line.
3. Datums A-B and D to be determined at centerline between leads where leads exit plastic body at datum plane H.
4. Dimensions do not include mold protrusion. Allowable mold protrusion is 0.25mm. per side.
5. These dimensions to be determined at datum plane H.
6. Package top dimensions are smaller than bottom dimensions and top of package will not overhang bottom of package.
7. Dimension b does not include dam bar protrusion. Allowable dam bar protrusion shall not cause the lead width to exceed the b dimension by more than 0.08mm. Dam bar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07mm.
   △ Exact shape of each corner is optional.
8. Controlling dimension: millimeter.
9. This outline conforms to JEDEC publication 95 registration MS-026, variation ACD.
10. Dimensions in ( ) are for reference only.

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