ISL8118

3.3V to 20V, Single-Phase PWM Controller with Integrated 2A/4A MOSFET Drivers

FN6325
Rev 3.00
August 12, 2014

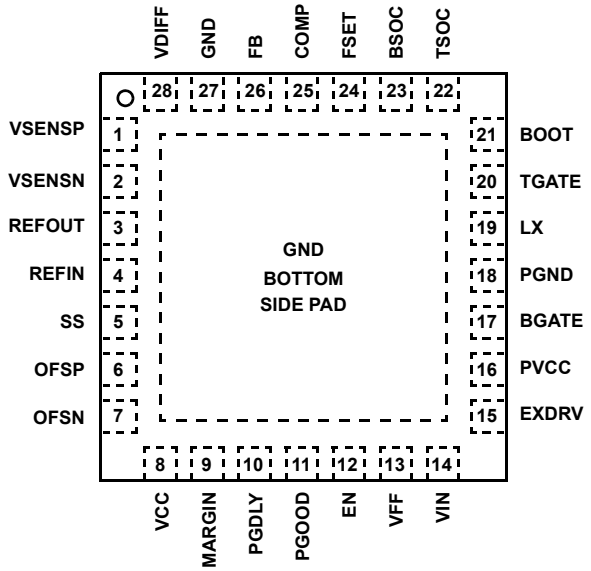
The ISL8118 is a single-phase PWM controller featuring an input voltage range of +3.3V to +20V and integrated MOSFET drivers. Utilizing voltage-mode operation with input voltage feed-forward compensation, the ISL8118 maintains a constant loop gain, providing optimal transient response for applications with a wide input operating voltage range.

The output voltage can be precisely regulated down to 0.591V with a system tolerance of ±1.0% over the industrial temperature range and line and load variations. A external reference input is provided to bypass the internal reference for voltage tracking or DDR memory applications. The compact 28 Ld 5x5 QFN package, integrated linear regulator as well as the external linear regulator drive option, integrated differential remote sense amplifier and integrated voltage margining with adjustable upper and lower settings decrease external component count and reduce board space requirements.

Programmable soft-start with pre-biased load capability, adjustable operating frequency from 250kHz to 2MHz, sourcing and sinking overcurrent protection, overvoltage and undervoltage protection, and power-good indication with programmable delay combine to make the ISL8118 a superior choice for many power supply systems.

Pinout

ISL8118
(28 LD 5x5 QFN)
TOP VIEW



Features

- Wide Input Voltage Range: +3.3V to +20V
- High-Speed 2A/4A MOSFET Gate Drivers that Operate from 2.9V to 5.6V
- Operating Junction Temperature Range –40°C to +125°C
- External Reference Input
- Input Voltage Feed-forward Compensation
- Internal Linear Regulator
- External Linear Regulator Drive Available
- High System Accuracy:
  - ±0.68% Over the Range of 0°C to +70°C
  - ±1.00% Over the Range of -40°C to +85°C
- Programmable Operating Frequency from 250kHz to 2MHz
- Programmable Soft-Start with Pre-biased Load Capability
- Integrated Unity-Gain Differential Remote Sense Amplifier
- Enable Input with Voltage Monitoring Capability
- Integrated Voltage Margining with Independent Upper and Lower Settings
- Overvoltage and Undervoltage Protection
- Low-Side and High-Side MOSFET Current Sensing
- Overcurrent Protection for Sourcing and Sinking Currents
- Power-Good Indicator with Programmable Delay
- Compact 28 Ld 5x5 QFN Package
- Pb-Free (RoHS Compliant)

Applications

- Telecom and Datacom Servers
- Point of Load Modules
- Routers and Switchers
- High Current Distributed Power Supplies

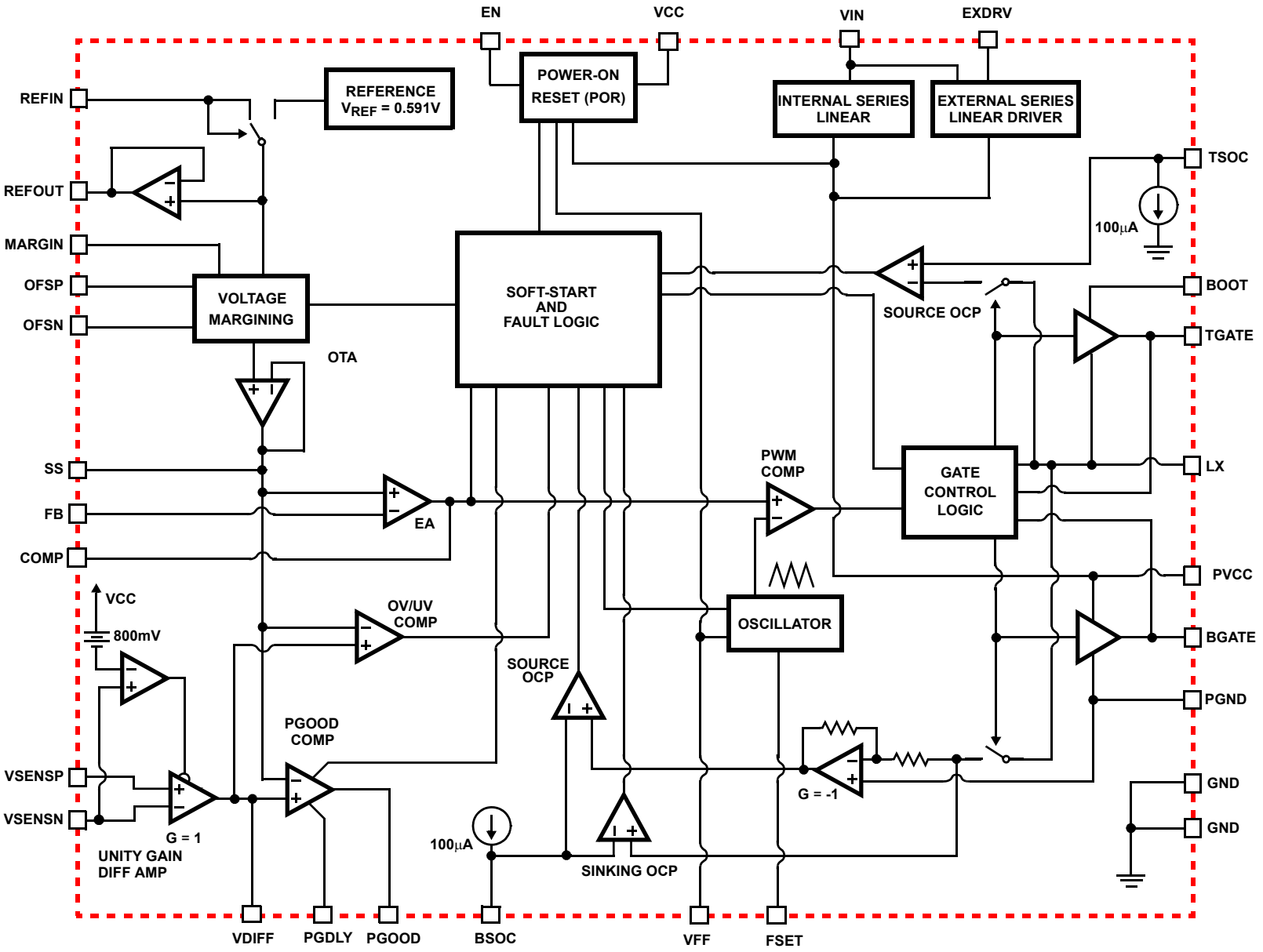
Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL8118CRZ	ISL8118CRZ	0 to +70	28 Ld 5x5 QFN	L28.5x5
ISL8118IRZ	ISL8118IRZ	-40 to +85	28 Ld 5x5 QFN	L28.5x5

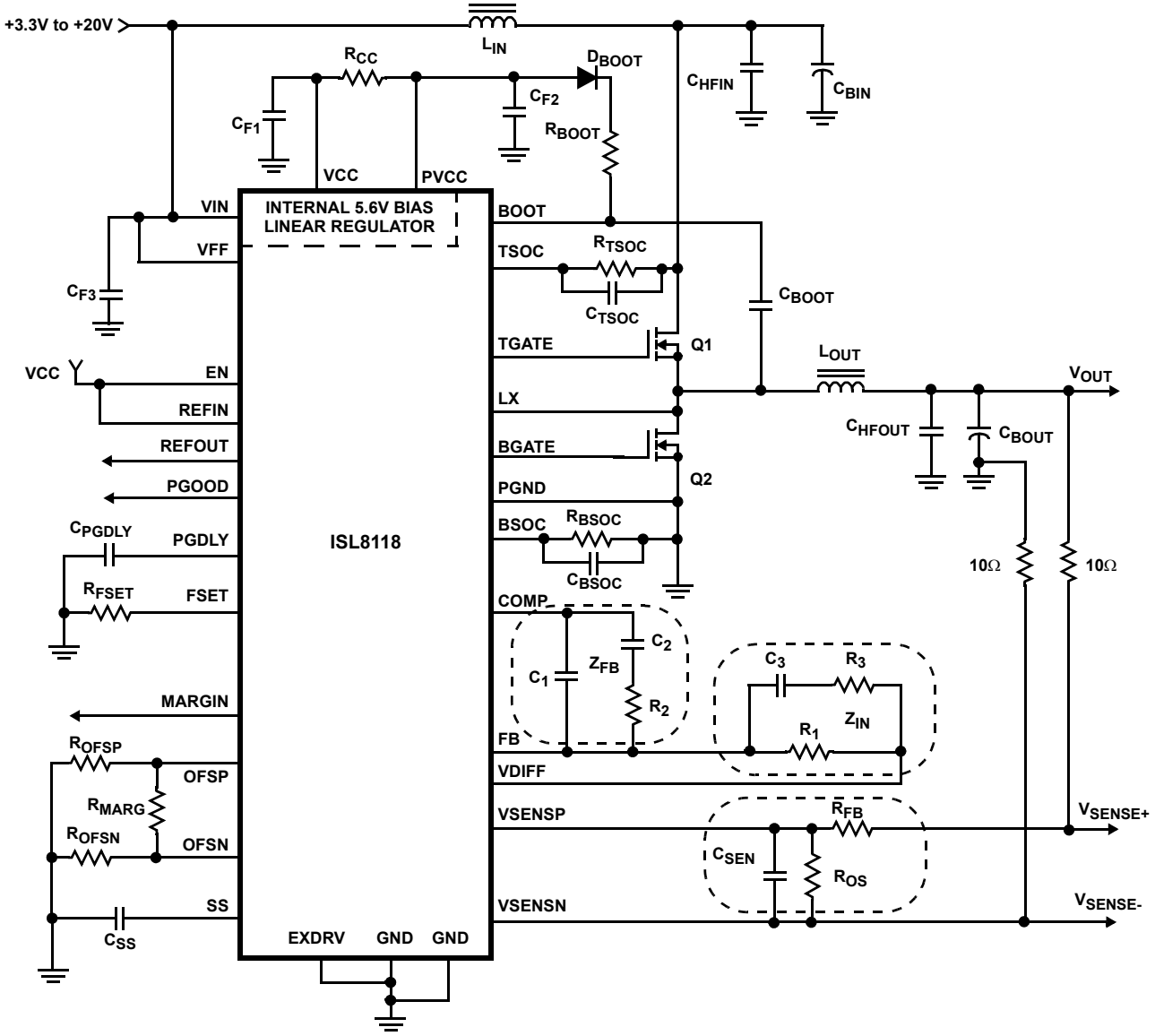
Add “-T*” suffix for tape and reel. Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

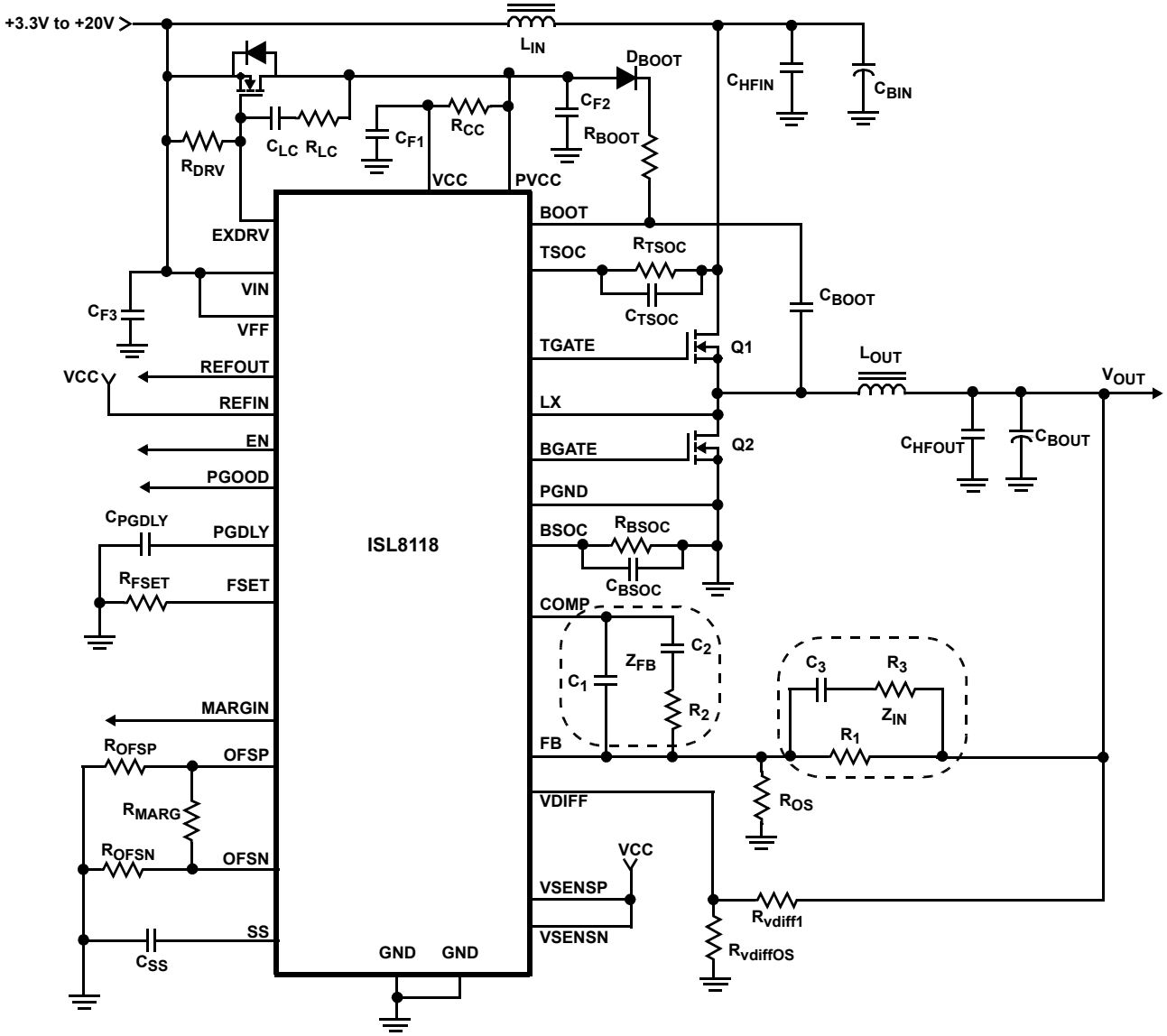
Block Diagram



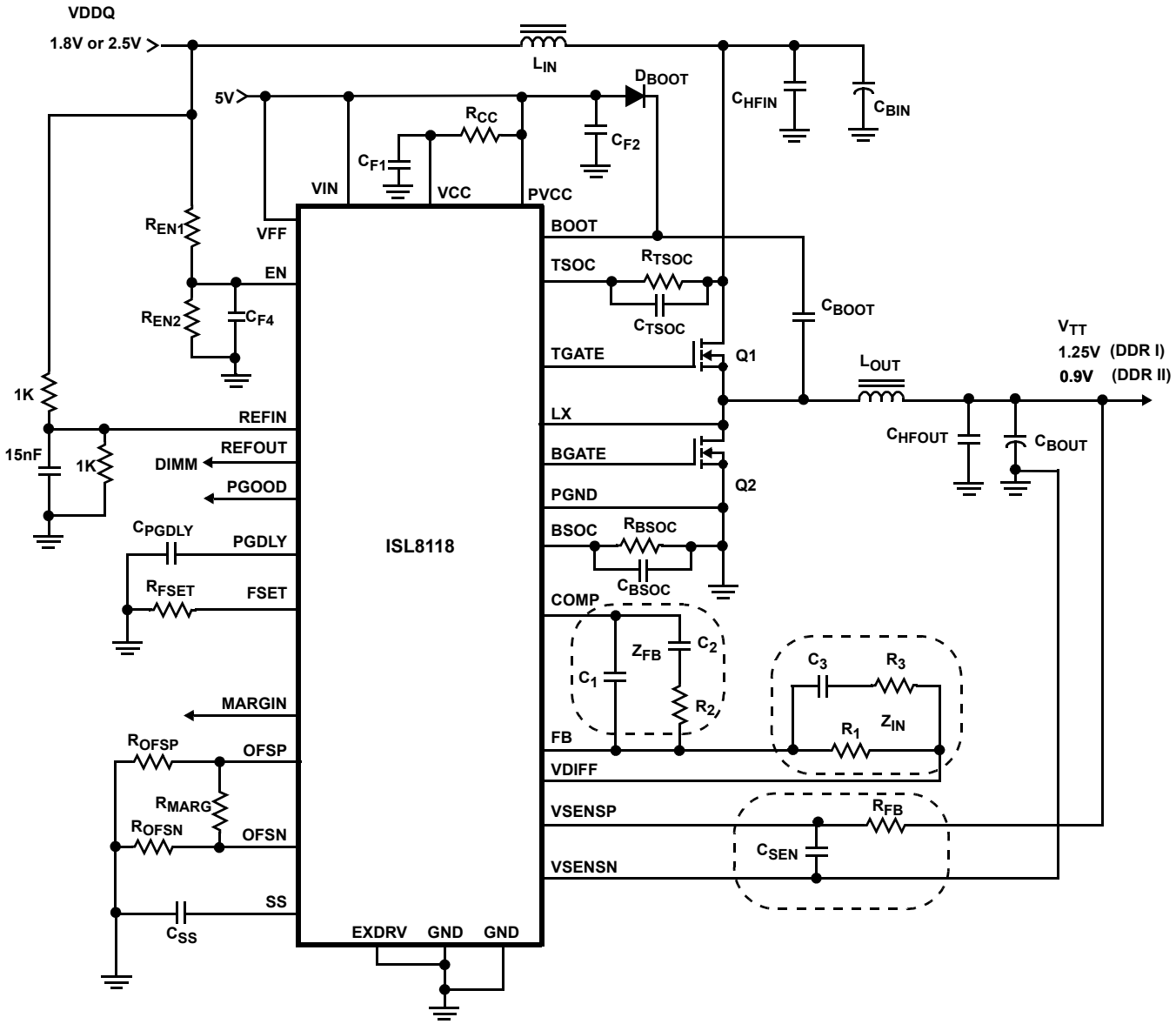
Typical Application I (Internal Linear Regulator with Remote Sense)



Typical Application II (External Linear Regulator without Remote Sense)



Typical Application III (Dual Data Rate I or II)



Absolute Maximum Ratings

Input Voltage, VIN, VFF . . . . . -0.3V to +22.0V
Signal Bias Voltage, VCC . . . . . -0.3V to +6.0V
Driver Bias Voltage, PVCC . . . . . -0.3V to +6.0V
Boot Voltage, V_{BOOT} . . . . . -0.3V to +36V
LX Voltage, V_{LX} . . . . . V_{BOOT} - 6V to V_{BOOT} + 0.3V
Boot to LX Voltage, V_{BOOT} - V_{LX} 6V
Other Input or Output Voltages . . . . . -0.3V to VCC +0.3V
ESD Classification . . . . . Class 2

Recommended Operating Conditions

Input Voltage, VIN, VFF . . . . . 3.3V to 20V ±10%
Signal Bias Voltage, VCC . . . . . 2.9V to 5.6V
Driver Bias Voltage, PVCC . . . . . 2.9V to 5.6V
Boot to LX Voltage (Overcharged), V_{BOOT} - V_{LX} . . . . . <6V
Ambient Temperature Range . . . . . -40°C to +85°C
Junction Temperature Range . . . . . -40°C to +125°C

Thermal Information

Thermal Resistance (Notes 1, 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
QFN Package	32	5

Maximum Junction Temperature . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profilesee link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features.
2. θ_{JC}, "case temperature" location is at the center of the package underside exposed pad. See Tech Brief TB379 for details.

Electrical Specifications

Recommended Operating Conditions, Unless Otherwise Noted. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY CURRENTS						
Nominal VIN Supply Current	I_{VIN}	VIN = VCC = PVCC = 5V, Fs = 600kHz, TGATE and BGATE Open	-	0.5	1	mA
Nominal VCC Supply Current	I_{VCC}	VIN = VCC = PVCC = 5V, Fs = 600kHz, TGATE and BGATE Open	-	8	13	mA
Nominal PVCC Supply Current	I_{PVCC}	VIN = VCC = PVCC = 5V; Fs = 600kHz, TGATE and BGATE Open	-	3	4	mA
Shutdown VIN Supply Current	I_{VIN_S}	EN = 0V, VCC = PVCC = VIN = 5V	-	0.5	1	mA
Shutdown VCC Supply Current	I_{PVCC_S}	EN = 0V, VCC = PVCC = VIN = 5V	-	1	2	mA
Shutdown PVCC Supply Current	I_{VCC_S}	EN = 0V, VCC = PVCC = VIN = 5V	-	3	4	mA
ENABLE						
Input Reference Voltage	V_{EN_REF}		0.485	0.500	0.515	V
Hysteresis Source Current	I_{EN_HYS}		7.5	10	11.5	µA
Maximum Input Voltage	V_{EN}		-	VCC+0.3	-	V
OSCILLATOR						
Nominal Maximum Frequency	OSC_{FMAX}	(Note 3)	-	2000	-	kHz
Nominal Minimum Frequency	OSC_{FMIN}	(Note 3)	-	250	-	kHz
Total Variation	ΔOSC	FSET = 250kHz to 2MHz, VFF = 3.3V to 20V	-17	-	+17	%
Ramp Amplitude	ΔV_{OSC}		-	0.16*VFF	-	V_{P-P}
Ramp Bottom	V_{OSC_MIN}		-	1.0	-	V
Minimum Usable VFF Voltage	VFF	VCC = 5V	-	3.3	-	V
POWER-ON RESET						
Rising VCC Threshold	POR_{VCC_R}		2.79	-	2.89	V
Falling VCC Threshold	POR_{VCC_F}		2.59	-	2.69	V

Electrical Specifications Recommended Operating Conditions, Unless Otherwise Noted. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VCC Hysteresis	POR_{VCC_H}		187	215	250	mV
Rising PVCC Threshold	POR_{PVCC_R}		2.79	-	2.91	V
Falling PVCC Threshold	POR_{PVCC_F}		2.59	-	2.70	V
PVCC Hysteresis	POR_{PVCC_H}		193	215	250	mV
Rising VFF Threshold	POR_{VFF_R}		1.48	-	1.54	V
Falling VFF Threshold	POR_{VFF_F}		1.35	-	1.41	V
VFF Hysteresis	POR_{VFF_H}		127	137	146	mV
REFERENCE						
Reference Voltage	V_{REF_COM}	T_A = 0°C to +70°C	0.587	0.591	0.595	V
	V_{REF_IND}	T_A = -40°C to +85°C	0.585	0.591	0.597	V
System Accuracy	V_{SYS_COM}	T_A = 0°C to +70°C	-0.68	-	0.68	%
	V_{SYS_IND}	T_A = -40°C to +85°C	-1.0	-	1.0	%
REFERENCE TRACKING						
Input Voltage Range	V_{REFIN}	VCC = 5V	0.068	-	VCC-1.8V	V
External Reference Offset	V_{REFIN_OS}	REFIN = 0.6V	-1.8	0	2.2	mV
Maximum Drive Current	I_{REFOUT}	C_L = 1µF, VCC = 5V, REFOUT = 1.25V	-	19	-	mA
Output Voltage Range	V_{REFOUT}	C_L = 1µF	0.01	-	VCC-1.8V	V
Maximum Output Voltage Offset	V_{REFOUT_OS}	C_L = 1µF REFOUT = 1.25V	-6	-	11	mV
Minimum Load Capacitance	C_{REFOUT_MIN}	REFOUT = 1.25V	-	1.0	-	µF
Input Disable Voltage	V_{REFIN_DIS}	VCC = 5V	VCC-0.6	-	VCC-0.58	V
ERROR AMPLIFIER						
DC Gain		R_L = 10k, C_L = 100p, at COMP Pin	-	88	-	dB
Unity Gain-Bandwidth	UGBW	R_L = 10k, C_L = 100p, at COMP Pin	-	15	-	MHz
Slew Rate	SR	R_L = 10k, C_L = 100p, at COMP Pin	-	6	-	V/µs
DIFFERENTIAL AMPLIFIER						
DC Gain	UG	Standard Instrumentation Amplifier	-	0	-	dB
Unity Gain Bandwidth	UGBW		-	20	-	MHz
Slew Rate	SR	COMP = 10pF	-	10	-	V/µs
Offset			-1.9	0	1.9	mV
Negative Input Source Current	I_{VSENSN}		-	6		µA
Input Common Mode Range Max			-	VCC-1.8	-	V
Input Common Mode Range Min			-	-0.2	-	V
VSENSN Disable Voltage	V_{VSEN_DIS}		-	VCC	-	V
OPERATIONAL TRANSCONDUCTANCE AMPLIFIER (OTA)						
DC Gain		C_{SS} = 0.1µF, at SS Pin	-	88	-	dB
Drive Capability		C_{SS} = 0.1µF, at SS Pin	30	37	44	µA
PWM						
Maximum Duty Cycle	D_{MAX}	Leading and Trailing-edge Modulation	-	100	-	%
Minimum Duty Cycle	D_{MIN}	Leading and Trailing-edge Modulation	-	0	-	%
GATE DRIVERS						
TGATE Source Resistance	R_{TGATE}	500mA Source Current, PVCC = 5.0V	-	1.0	-	Ω

Electrical Specifications Recommended Operating Conditions, Unless Otherwise Noted. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
TGATE Source Saturation Current	I_{TGATE}	$V_{TGATE-LX}$ = 2.5V, PVCC = 5.0V	-	2.0	-	A
TGATE Sink Resistance	R_{TGATE}	500mA Sink Current, PVCC = 5.0V	-	1.0	-	Ω
TGATE Sink Saturation Current	I_{TGATE}	$V_{TGATE-LX}$ = 2.5V, PVCC = 5.0V	-	2.0	-	A
Bgate Source Resistance	R_{BGATE}	500mA Source Current, PVCC = 5.0V	-	1.0	-	Ω
Bgate Source Saturation Current	I_{BGATE}	V_{BGATE} = 2.5V, PVCC = 5.0V	-	2.0	-	A
Bgate Sink Resistance	R_{BGATE}	500mA Sink Current, PVCC = 5.0V	-	0.4	-	Ω
Bgate Sink Saturation Current	I_{BGATE}	V_{BGATE} = 2.5V, PVCC = 5.0V	-	4.0	-	A
INTERNAL LINEAR REGULATOR						
Maximum Current	I_{VIN}		-	200	-	mA
Saturated Equivalent Impedance	R_{LIN}	VIN = 3.3V	-	2	3.9	Ω
Linear Regulator Voltage	PVCC	VIN = 20V, Load = 0 to 100mA	5.3	5.5	5.71	V
Maximum VIN DV/DT	VIN_{DV/DT_Max}	V_{IN} = 0V to V_{IN} step, PVCC < 2.0V at V_{IN} application; V_{IN} > 6.5V	-	1	-	V/µs
		V_{IN} = 2.0V to V_{IN} step, 2.0V < PVCC at V_{IN} application; V_{IN} > 6.5V	-	0.05	-	V/µs
EXTERNAL LINEAR REGULATOR						
Maximum Sinking Drive Current	LIN_DRV	LIN_DRV = VIN = 20V	1.30	4.17	5.30	mA
		LIN_DRV = VIN = 3.3V	1.67	3.88	4.67	mA
OVERCURRENT PROTECTION (OCP)						
Bottom Side OCP (BSOC) Current Source	I_{BSOC}	BSOC = 0V to VCC - 1.0V, T_A = 0°C to +70°C	86	100	107	µA
		BSOC = 0V to VCC - 1.0V, T_A = -40°C to +85°C	84	100	109	µA
BSOC Maximum Offset Error	I_{BSOC_OFSET}	Vcc = 2.9V and 5.6V t_{SAMPLE} < 10µs	-	±2	-	mV
Top Side OCP (TSOC) Current Source	I_{TSOC}	TSOC = 0.8V to 22V T_A = 0°C to +70°C	91	100	106	µA
		TSOC = 0.8V to 22V T_A = -40°C to +85°C	89	100	107	µA
	I_{TSOC_LOW}	TSOC = 0.3V to 0.8V	84	-	107	µA
TSOC Maximum Offset Error	I_{TSOC_OFSET}	VCC = 2.9V and 5.5V t_{SAMPLE} < 10µs	-	±2	-	mV
POWER GOOD MONITOR						
Undervoltage Rising Trip Point	V_{UVR}		-7%	-9%	-11%	V_{SS}
Undervoltage Falling Trip Point	V_{UVF}		-13%	-15%	-17%	V_{SS}
Overvoltage Rising Trip Point	V_{OVR}		13%	15%	17%	V_{SS}
Overvoltage Falling Trip Point	V_{OVF}		7%	9%	11%	V_{SS}
PGOOD Delay	t_{PGDLY}	C_{PGDLY} = 0.1µF	-	7.1	-	ms
PGOOD Delay Source Current	I_{PGDLY}		17	21	24	µA
PGOOD Delay Threshold Voltage	V_{PGDLY}		1.45	1.49	1.52	V
PGOOD Low Output Voltage	I_{PG_LOW}	I_{PGOOD} = 5mA	-	-	0.150	V
Maximum Sinking Current	I_{PG_MAX}	V_{PGOOD} = 0.8V	23	-	-	mA
Maximum Open Drain Voltage	V_{PG_MAX}	VCC = 3.3V	-	6	-	V
MARGINING CONTROL						
Minimum Margining Voltage of Internal Reference	V_{MARG}	R_{MARG} = 10kΩ, R_{OFSN} = 6.01kΩ, MAR_CRTL = 0V	-187	-197	-209	mV
Maximum Margining Voltage of Internal Reference	V_{MARG}	R_{MARG} = 10kΩ, R_{OFSP} = 6.01kΩ, MAR_CRTL = VCC	185	197	208	mV

Electrical Specifications Recommended Operating Conditions, Unless Otherwise Noted. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Margining Transfer Ratio	N_{MARG}	$N_{MARG} = (V_{OFSN}-V_{OFSP})/V_{MARG}$	4.84	5	5.22	SDR
Positive Margining Threshold	MARGIN		1.51	1.8	2.02	V
Negative Margining Threshold	MARGIN		0.75	0.9	1.05	V
Tri-state Input Level	MARGIN	Disable Mode	1.21	1.325	1.40	V

NOTE:

3. Limits should be considered typical and are not production tested.

Functional Pin Descriptions

VSENSP (Pin 1)

This pin provides differential remote sense for the ISL8118. It is the positive input of a standard instrumentation amplifier topology with unity gain, and should connect to the positive rail of the load/processor. The voltage at this pin should be set equal to the internal system reference voltage (0.591V typical).

VSENSN (Pin 2)

This pin provides differential remote sense for the regulator. It is the negative input of the instrumentation amplifier, and should connect to the negative rail of the load/processor. Typically 6µA is sourced from this pin. The output of the remote sense buffer is disabled (High Impedance) by pulling VSENSN to VCC.

REFOUT (Pin 3)

This pin connects to the unmargined system reference through an internal buffer. It has a 19mA drive capability with an output common mode range of GND to VCC. The REFOUT buffer requires at least 1µF of capacitive loading to be stable. This pin should not be left floating.

REFIN (Pin 4)

When the external reference pin (REFIN) is NOT within ~800mV of VCC, the REFIN pin is used as the system reference instead of the internal 0.591V reference. The recommended REFIN input voltage range is ~60mV to VCC - 1.8V.

SS (Pin 5)

This pin provides soft-start functionality for the ISL8118. A capacitor connected to ground along with the internal 38µA Operational Transconductance Amplifier (OTA), sets the soft-start interval of the converter. This pin is directly connected to the non-inverting input of the Error Amplifier. To prevent noise injection into the error amplifier, the SS capacitor should be located within 150 mils of the SS and GND pins.

OFSP (Pin 6)

This pin sets the positive margining offset voltage. Resistors should be connected to GND (R_{OFSP}) and OFSN (R_{MARG}) from this pin. With MARGIN logic low, the internal 0.591V reference is developed at the OFSP pin across resistor R_{OFSP}. The voltage on OFSP is driven from OFSN through R_{MARG}. The resulting voltage differential between OFSP and OFSN is divided by 5 and imposed on the system reference. The maximum designed offset of 1V between OFSP and OFSN pins translates to a 200mV offset.

OFSN (Pin 7)

This pin sets the negative margining offset voltage. Resistors should be connected to GND (R_{OFSN}) and OFSP (R_{MARG}) from this pin. With MARGIN logic low, the internal 0.591V reference is developed at the OFSN pin across resistor R_{OFSN}. The voltage on OFSN is driven from OFSP through R_{MARG}. The resulting voltage differential between OFSP and OFSN is divided by 5 and imposed on the system reference. The maximum designed offset of -1V between OFSP and OFSN pins translates to a -200mV offset of the system reference.

VCC (Pin 8, Analog Circuit Bias)

This pin provides power for the ISL8118 analog circuitry. The pin should be connected to a 2.9V to 5.6V bias through an RC filter from PVCC to prevent noise injection into the analog circuitry. This pin can be powered off the internal or external linear regulator options.

MARGIN (Pin 9)

The MARGIN pin controls margining function, a logic high enables positive margining, a logic low sets negative margining, a high impedance disables margining.

PGDLY (Pin 10)

Provides the ability to delay the output of the PGOOD assertion by connecting a capacitor from this pin to GND. A 0.1µF capacitor produces approximately a 5ms delay.

PGOOD (Pin 11)

Provides an open drain Power Good signal when the output is within 9% of nominal output regulation point with 6% hysteresis (15%/9%), and after soft-start is complete. PGOOD monitors the VDIFF pin.

EN (Pin 12)

This pin is compared with an internal 0.50V reference and enables the soft-start cycle. This pin also can be used for voltage monitoring. A 10µA current source to GND is active while the part is disabled, and is inactive when the part is

enabled. This provides functionality for programmable hysteresis when the EN pin is used for voltage monitoring.

VFF (Pin 13)

The voltage at this pin is used for input voltage feed forward compensation and sets the internal oscillator ramp peak to peak amplitude at 0.16*VFF. An external RC filter may be required at this pin in noisy input environments. The minimum recommended VFF voltage is 2.97V.

VIN (Pin 14, Internal Linear Regulator Input)

This pin should be tied directly to the input rail when using the internal or external linear regulator options. It provides power to the External/Internal Linear drive circuitry. When used with an external 3.3V to 5V supply, this pin should be tied directly to PVCC.

EXDRV (Pin 15, External Linear Regulator Drive)

This pin allows the use of an external pass element to power the IC for input voltages above 5.0V. It should be connected to GND when using an external 5V supply or the internal linear regulator. When using the external linear regulator option, this pin should be connected to the gate of a PMOS pass element, a pull-up resistor must be connected between the PMOS device's gate and source for proper operation.

PVCC (Pin 16, Driver Bias Voltage)

This pin is the output of the internal series linear regulator. It also provides the bias for both bottom side and top side MOSFET drivers. The maximum voltage differential between PVCC and PGND is 6V. Its recommended operational voltage range is 2.9V to 5.6V. At minimum, a 10µF capacitor is required for decoupling PVCC to PGND. For proper operation the PVCC capacitor must be within 150 mils of the PVCC and the PGND pins and must be connected to these pins with dedicated traces.

BGATE (Pin 17)

This pin provides the drive for the bottom side MOSFET and should be connected to its gate.

PGND (Pin 18, Power Ground)

This pin connects to the bottom side MOSFET's source and provides the ground return path for the lower MOSFET driver and internal power circuitries. In addition, PGND is the return path for the bottom side MOSFET's rDS(ON) current sensing circuit.

LX (Pin 19)

This pin connects to the source of the top side MOSFET and the drain of the bottom side MOSFET. This pin represents the return path for the top side gate driver. During normal switching, this pin is used for top side and bottom side current sensing.

TGATE (Pin 20)

This pin provides the drive for the top side MOSFET and should be connected to its gate.

BOOT (Pin 21)

This pin provides the bootstrap bias for the top side driver. The absolute maximum voltage differential between BOOT and LX is 6.0V (including the voltage added due to the overcharging of the bootstrap capacitor); its operational voltage range is 2.5V to 5.6V with respect to LX. It is recommended that a 2.2Ω resistor be placed in series with the bootstrap diode to prevent over charging of the BOOT capacitor during normal operation.

TSOC (Pin 22)

The top side sourcing current limit is set by connecting this pin with a resistor and capacitor to the drain of the top side MOSEFT. A 100µA current source develops a voltage across the resistor which is then compared with the voltage developed across the top side MOSFET. An initial ~120ns blanking period is used to eliminate sampling error due to the switching noise before the current is measured.

BSOC (Pin 23)

The bottom side source and sinking current limit is set by placing a resistor (RBSOC) and capacitor between this pin and PGND. A 100µA current source develops a voltage across RBSOC which is then compared with the voltage developed across the bottom side MOSFET when on. The sinking current limit is set at 1x of the nominal sourcing limit in ISL8118. An initial ~120ns blanking period is used to eliminate the sampling error due to switching noise before the current is measured.

FSET (Pin 24)

This pin provides oscillator switching frequency adjustment by placing a resistor (RFSET) from this pin to GND.

COMP (Pin 25)

This pin is the error amplifier output. It should be connected to the FB pin through the desired compensation network.

FB (Pin 26)

This pin is the inverting input of the error amplifier and has a maximum usable voltage of VCC-1.8V. When using the internal differential remote sense functionality, this pin should be connected to VDIFF by a standard feedback network. In the event the remote sense buffer is disabled, the VDIFF pin should be connected to VOUT by a resistor divider along with FB's compensation network.

GND (Pin 27, Analog Ground)

Signal ground for the IC. All voltage levels are measured with respect to this pin. This pin should not be left floating.

VDIFF (Pin 28)

This pin is the output of the differential remote sense instrumentation amplifier. It is connected internally to the OV/UV/PGOOD comparators. The VDIFF pin should be connected to the FB pin by a standard feedback network. In the event that the remote sense buffer is disabled, the VDIFF

pin should be connected to VOUT by a resistor divider along with FB's compensation network. An RC filter should be used if VDIFF is to be connected directly to FB instead of to VOUT through a separate resistor divider network.

GND (Bottom Side Pad, Analog Ground)

Signal ground for the IC. All voltage levels are measured with respect to this pin. This pin should not be left floating.

Functional Description

Initialization

The ISL8118 automatically initializes upon receipt of power without requiring any special sequencing of the input supplies. The Power-On Reset (POR) function continually monitors the input supply voltages (PVCC,VFF, VCC) and the voltage at the EN pin. Assuming the EN pin is pulled to above ~0.50V, the POR function initiates soft-start operation after all input supplies exceed their POR thresholds.

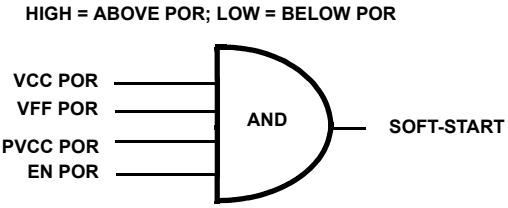
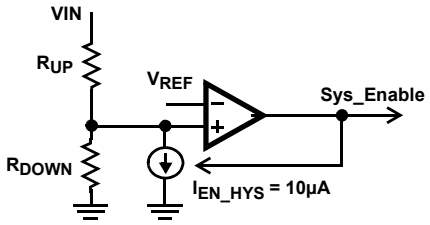


FIGURE 1. SOFT-START INITIALIZATION LOGIC

With all input supplies above their POR thresholds, driving the EN pin above 0.50V initiates a soft-start cycle. In addition to normal TTL logic, the enable pin can be used as a voltage monitor with programmable hysteresis through the use of the internal 10mA sink current and an external resistor divider. This feature is especially designed for applications that have input rails greater than a 3.3V and require specific input rail POR and Hysteresis levels for better undervoltage protection. Consider for a 12V application choosing RUP = 100kΩ and RDOWN = 5.76kΩ there by setting the rising threshold (VEN_RTH) to 10V and the falling threshold (VEN_FTH) to 9V, for 1V of hysteresis (VEN_HYS). Care should be taken to prevent the voltage at the EN pin from exceeding VCC when using the programmable UVLO functionality.



$$R_{UP} = \frac{V_{EN\_HYS}}{I_{EN\_HYS}}$$

$$R_{DOWN} = \frac{R_{UP} \bullet V_{EN\_REF}}{V_{EN\_FTH} - V_{EN\_REF}}$$

$$V_{EN\_FTH} = V_{EN\_RTH} - V_{EN\_HYS}$$

FIGURE 2. ENABLE POR CIRCUIT

Soft-start

The POR function activates the internal 38µA OTA which begins charging the external capacitor (C_{SS}) on the SS pin to a target voltage of VCC. The ISL8118's soft-start logic continues to charge the SS pin until the voltage on COMP exceeds the bottom of the oscillator ramp, at which point, the driver outputs are enabled, with the bottom side MOSFET first being held low for 200ns to provide for charging of the bootstrap capacitor. Once the driver outputs are enabled, the OTA's target voltage is then changed to the margined (if margining is being used) reference voltage (V_{REF_MARG}), and the SS pin is ramped up or down accordingly. This method reduces start-up surge currents due to a pre-charged output by inhibiting regulator switching until the control loop enters its linear region. By ramping the positive input of the error amplifier to VCC and then to V_{REF_MARG}, it is even possible to mitigate surge currents from outputs that are pre-charged above the set output voltage. As the SS pin connects directly to the non-inverting input of the Error Amplifier, noise on this pin should be kept to a minimum through careful routing and part placement. To prevent noise injection into the error amplifier, the SS capacitor should be located within 150 mils of the SS and GND pins. Soft-start is declared done when the drivers have been enabled and the SS pin is within ±3mV of V_{REF_MARG}.

Power Good

The power good comparator references the voltage on the soft-start pin to prevent accidental tripping during margining. The trip points are shown on Figure 3. Additionally, power good will not be asserted until after the completion of the soft-start cycle. A 0.1µF capacitor at the PGDLY pin will add an additional ~7.1ms delay to the assertion of power good. PGDLY does not delay the deassertion of power good.

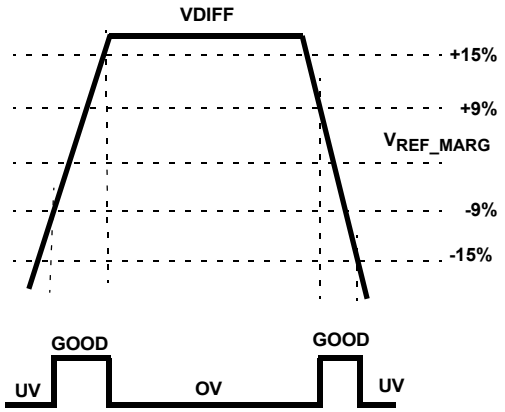


FIGURE 3. UNDERVOLTAGE-OVERVOLTAGE WINDOW

$$T_{PGDLY} = C_{PGDLY} \cdot \frac{1.5V}{30\mu A}$$

Undervoltage and Overvoltage Protection

The Undervoltage (UV) and Overvoltage (OV) protection circuitry compares the voltage on the VDIFF pin with the reference that tracks with the margining circuitry to prevent accidental tripping. UV and OV functionality is not enabled until the end of soft-start.

An OV event is detected asynchronously and causes the top side MOSFET to turn off, the bottom side MOSFET to turn on (effectively a 0% duty cycle), and PGOOD to pull low. The regulator stays in this state and overrides sourcing and sinking OCP protections until the OV event is cleared.

A UV event is detected asynchronously and results in the PGOOD pulling low.

Overcurrent Protection

The ISL8118 monitors both the top side MOSFET and bottom side MOSFET for overcurrent events. Dual sensing allows the ISL8118 to detect overcurrent faults at the very low and very high duty cycles that can result from the ISL8118's wide input range. The OCP function is enabled with the drivers at start-up and detects the peak current during each sensing period. A resistor and a capacitor between the BSOC pin and GND set the bottom side source and sinking current limits. A 100µA current source develops a voltage across the resistor which is then compared with the voltage developed across the bottom side MOSFET at conduction mode. The measurement comparator uses offset correcting circuitry to provide precise current measurements with roughly ±2mV of offset error. An ~120ns blanking period, implemented on the upper and lower MOSFET current sensing circuitries, is used to reduce the current sampling error due to the leading-edge switching noise. An additional 120ns low pass filter is used to further reduce measurement error due to noise. In sourcing current applications, the BSOC voltage is inverted and compared with the voltage across the MOSFET while on. When this voltage exceeds the BSOC set voltage, a sourcing OCP fault is triggered. A 1000pF or greater filter capacitor should be used in parallel with R_{BSOC} to prevent on chip parasitics from impacting the accuracy of the OCP measurement.

Simple Bottom Side OCP Equation

$$R_{BSOC} = \frac{I_{OC\_SOURCE} \bullet r_{DS(ON)Botside}}{100\mu A}$$

Detailed Bottom Side OCP Equations

$$R_{BSOC} = \frac{\left(I_{OC\_SOURCE} + \frac{\Delta I}{2}\right) \bullet r_{DS(ON)B}}{I_{BSOC} \bullet N_B}$$

$$\Delta I = \frac{V_{IN} - V_{OUT}}{F_S L} \bullet \frac{V_{OUT}}{V_{IN}}$$

$$I_{OC\_SINK} = \frac{I_{BSOC} \bullet N_B \bullet R_{BSOC}}{r_{DS(ON)B}} - \frac{\Delta I}{2}$$

N_B = Number of Bottom side MOSFETs

The ISL8118's sinking current limit is set to the same voltage as its sourcing limit. In sinking applications, when the voltage across the MOSFET is greater than the voltage developed across the resistor (RBSOC) a sinking OCP event is triggered. To avoid non-synchronous operation at light load, the peak-to-peak output inductor ripple current should not be greater than twice of the sinking current limit.

The top side sourcing current limit is set by connecting the TSOC pin with a resistor (R_{TSOC}) and a capacitor to the drain of the top side MOSEFT. A 100µA current source develops a voltage across the resistor which is then compared with the voltage developed across the top side MOSFET while on. When the voltage drop across the MOSFET exceeds the voltage drop across the resistor, a sourcing OCP event occurs. A 1000pF or greater filter capacitor should be used in parallel with R_{TSOC} to prevent on chip parasitics from impacting the accuracy of the OCP measurement and to smooth the voltage across R_{TSOC} in the presence of switching noise on the input bus.

Sourcing OCP faults cause the regulator to disable (TGATE and BGATE drives pulled low, PGOOD pulled low, soft-start capacitor discharged) itself for a fixed period of time after which a normal soft-start sequence is initiated. The period of time the regulator waits before attempting a soft-start sequence is set by three charge and discharge cycles of the soft-start capacitor.

Simple Top Side OCP Equation

$$R_{TSOC} = \frac{I_{OC\_SOURCE} \bullet r_{DS(ON)T}}{100\mu A}$$

Detailed Top Side OCP Equation

$$R_{TSOC} = \frac{\left(I_{OC\_SOURCE} + \frac{\Delta I}{2}\right) \bullet r_{DS(ON)T}}{I_{TSOC} \bullet N_T}$$

N_T = Number of top side MOSFETs

Sinking OCP faults cause the bottom side MOSFET drive to be disabled, effectively operating the ISL8118 in a non-synchronous manner. The fault is maintained for three clock cycles at which point it is cleared and normal operation is restored. OVP fault implementation overrides sourcing and sinking OCP events, immediately turning on the bottom side MOSFET and turning off the top side MOSFET. The OC trip point varies mainly due to the MOSFETs rDS(ON) variations and system noise. To avoid overcurrent tripping in the normal operating load range, find the RTSOC and/or RBSOC resistor from the previous detailed equations with:

1. Maximum rDS(ON) at the highest junction temperature;
2. Minimum IBSOC and/or ITSOC from specification table;
3. Determine the overcurrent trip point greater than the maximum output continuous current at maximum inductor ripple current.

Frequency Programming

By tying a resistor to GND from FSET pin, the switching frequency can be set between 250kHz and 2MHz.

Oscillator/VFF

The Oscillator is a triangle waveform, providing for leading and falling edge modulation. The bottom of the oscillator waveform is set at 1.0V. The ramp's peak-to-peak amplitude is determined from the voltage on the VFF (Voltage Feed Forward) pin by Equation 1:

$$D_{VOSC} = 0.16 \bullet VFF \qquad \text{(EQ. 1)}$$

An internal RC filter of 233kΩ and 2pF (341kHz) provides filtering of the VFF voltage. An external RC filter may be required to augment this filter in the event that it is insufficient to prevent noise injection or control loop interactions. Voltages below 2.9V on the VFF pin may result in undesirable operation due to extremely small peak-to-peak oscillator waveforms. The oscillator waveform should not exceed VCC -1.0V. For high VFF voltages the internal/external 5.6V linear regulator should be used. 5.6V on VCC provides sufficient headroom for 100% duty cycle operation when using the maximum VFF voltage of 22V. In the event of sustained 100% duty cycle operation, defined as 32 clock cycles where no BG pulse is detected, BG will be pulsed on to refresh the design's Bootstrap capacitor.

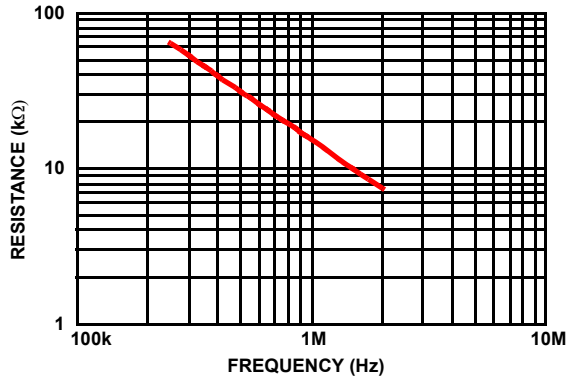


FIGURE 4. R_{FS} RESISTANCE vs FREQUENCY

$$Fs[Hz] \approx 1.178 \times 10^{10} \bullet R_T[\Omega]^{-0.973} \quad (R_T \text{ TO GND}) \qquad \text{(EQ. 2)}$$

Internal Series Linear Regulator

The VIN pin is connected to PVCC with a 2Ω internal series linear regulator, which is internally compensated. The external Series Linear regulator option should be used for applications requiring pass elements of less than 2Ω. When using the internal regulator, the EXDRV pin should be connected directly to GND. The PVCC and VIN pins should have a bypass capacitor (at least 10µF on PVCC is required) connected to PGND. For proper operation, the PVCC capacitor must be within 150 mils of the PVCC and the PGND pins, and be connected to these pins with dedicated traces. The internal series linear regulator's input (VIN) can range between 3.3V to 20V ±10%. The internal linear regulator is to provide power for both the internal MOSFET drivers through the PVCC pin and the analog circuitry through the VCC pin. The VCC pin should be connected to the PVCC pin with an RC filter to prevent high frequency driver switching noise from entering the analog circuitry. When VIN drops below 5.6V, the pass element will saturate; PVCC will track VIN, minus the dropout of the linear regulator: PVCC = VIN-2xIVIN. When used with an external 5V supply, the VIN pin should be tied directly to PVCC.

External Series Linear Regulator

The EXDRV pin provides sinking drive capability for an external pass element linear regulator controller. The external linear options are especially useful when the internal linear dropout is too large for a given application. When using the external linear regulator option, the EXDRV pin should be connected to the gate of a PMOS device, and a resistor should be connected between its gate and source. A resistor and a capacitor should be connected from gate to source to compensate the control loop. A PNP device can be used instead of a PMOS device, in which case the EXDRV pin should be connected to the base of the PNP pass element. The maximum sinking capability of the EXDRV pin is 0.5mA, and should not be exceeded if using an external resistor for a PMOS device. The designer should take care in designing a stable system when using external pass elements. The VCC pin should be connected to the PVCC pin with an RC filter to prevent high frequency driver switching noise from entering the analog circuitry.

High Speed MOSFET Gate Driver

The integrated driver has similar drive capability and features to Intersil's ISL6605 stand alone gate driver. The PWM tri-state feature helps prevent a negative transient on the output voltage when the output is being shut down. This eliminates the Schottky diode that is used in some systems for protecting the microprocessor from reversed-output-voltage damage. See the ISL6605 datasheet for specification parameters that are not defined in the current ISL8118 Electrical Specifications table.

A 1Ω to 2Ω resistor is recommended to be in series with the bootstrap diode when using VCCs above 5.0V to prevent the bootstrap capacitor from overcharging due to the negative swing of the trailing edge of the LX node.

Margining Control

When MARGIN is pulled high or low, the positive or negative margining functionality is respectively enabled. When MARGIN is left floating, the function is disabled. Upon positive margining, an internal buffer drives the OFSN pin from VCC to maintain OFSP at 0.591V. The resistor divider, RMARG and ROFSP, causes the voltage at OFSN to be increased. Similarly, upon Negative margining, an internal buffer drives the OFSP pin from VCC to maintain OFSN at 0.591V. The resistor divider, RMARG and ROFSN, causes the voltage at OFSP to be increased. In both modes, the voltage difference between OFSP and OFSN is then sensed with an instrumentation amplifier and is converted to the desired margining voltage by a 5:1 ratio. The maximum designed margining range of the ISL8118 is ±200mV; this sets the MINIMUM value of ROFSP or ROFSN at approximately 5.9k for an RMARG of 10k for a MAXIMUM of 1V across RMARG.

The OFS pins are completely independent and can be set to different margining levels. The maximum usable reference voltage for the ISL8118 is VCC - 1.8V, and should not be exceeded when using the margining functionality, i.e, VREF_MARG < VCC - 1.8V.

$$V_{MARG\_POS} = \frac{V_{REF}}{5} \bullet \frac{R_{MARG}}{R_{OFSP}} \quad \text{(EQ. 3)}$$

$$V_{MARG\_NEG} = \frac{V_{REF}}{5} \bullet \frac{R_{MARG}}{R_{OFSN}} \quad \text{(EQ. 4)}$$

An alternative calculation provides for a desired percentage change in the output voltage when using the internal 0.591V reference:

$$V_{PCT\_POS} = 20 \bullet \frac{R_{MARG}}{R_{OFSP}} \quad \text{(EQ. 5)}$$

$$V_{PCT\_NEG} = 20 \bullet \frac{R_{MARG}}{R_{OFSN}} \quad \text{(EQ. 6)}$$

When not used in a design OFSP, OFSN, and MARGIN should be left floating. To prevent damage to the part, OFSP and OFSN should not be tied to VCC or PVCC.

Reference Output Buffer

The internal buffer's output tracks the unmargined system reference. It has a 19mA drive capability, with maximum and minimum output voltage capabilities of VCC and GND respectively. Its capacitive loading can range from 1µF to above 17.6µF, which is designed for 1 to 8 DIMM systems in DDR (Dual Data Rate) applications. 1µF of capacitance should always be present on REFOUT. It is not designed to drive a resistive load and any such load added to the system should be kept above 300kΩ total impedance.

Reference Input

The REFIN pin allows the user to bypass the internal 0.591V reference with an external reference. Asynchronously, if REFIN is NOT within ~800mV of VCC, the external reference pin is used as the control reference instead of the internal 0.591V reference. The minimum usable REFIN voltage is ~60mV while the maximum is VCC - 1.8V - V_{MARG} (if present). The limitation is set by the error amplifier's maximum common mode input range of VCC - 1.8V for the industrial temperature ranges.

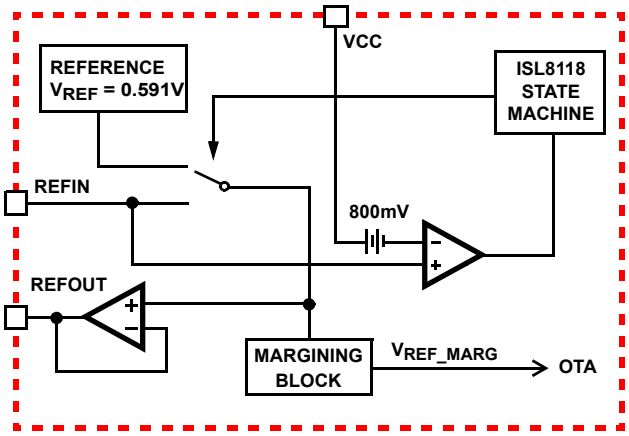


FIGURE 5. SIMPLIFIED REFERENCE BUFFER

Internal Reference and System Accuracy

The internal reference is trimmed to 0.591V. The total DC system accuracy of the system is within 0.85% over commercial temperature range, and 1.25% over industrial temperature range. System accuracy includes error amplifier offset, OTA error, and bandgap error. Differential remote sense offset error is not included. As a result, if the differential remote sense is used, then an extra 3mV of offset error enters the system. The use of REFIN may add up to 1.8mV of additional offset error.

Differential Remote Sense Buffer

The differential remote sense buffer is essentially an instrumentation amplifier with unity gain. The offset is trimmed to 3mV for high system accuracy. As with any instrumentation amplifier, typically 6µA are sourced from the VSENSN pin. The output of the remote sense buffer is connected directly to the internal OV/UV comparator. As a result, a resistor divider should be placed on the input of the buffer for proper regulation, as shown in Figure 6. The VDIFF pin should be connected to the FB pin by a standard feed-back network. A small capacitor, C_{SEN} in Figure 6, can be added to filter out noise, typically C_{SEN} is chosen so the corresponding time constant does not reduce the overall phase margin of the design, typically this is 2x to 10x switching frequency of the regulator.

As some applications will not use the differential remote sense, the output of the remote sense buffer can be disabled (high impedance) by pulling VSENSN within 800mV of VCC.

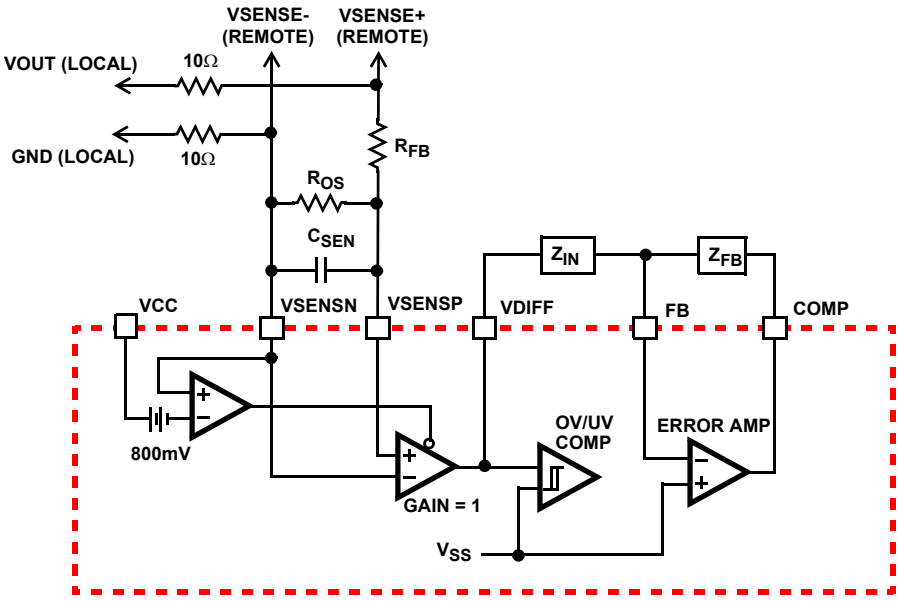


FIGURE 6. SIMPLIFIED UNITY GAIN DIFFERENITAL SENSING IMPLEMENTATION

As the VDIFF pin is connected internally to the OV/UV/PGOOD comparator, an external resistor divider must then be connected to VDIFF to provide correct voltage information for the OV/UV comparator. An RC filter should be used if VDIFF is to be connected directly to FB instead of to VOUT through a separate resistor divider network. This filter prevents noise injection from disturbing the OV/UV/PGOOD comparators on VDIFF. VDIFF may also be connected to the SS pin, which completely bypasses the OV/UV/PGOOD functionality.

Application Guidelines

Layout Considerations

As in any high frequency switching converter, layout is very important. Switching current from one power device to another can generate voltage transients across the impedances of the interconnecting bond wires and circuit traces. These interconnecting impedances should be minimized by using wide, short printed circuit traces. The critical components should be located as close together as possible using ground plane construction or single point grounding.

Figure 7 shows the critical power components of the converter. To minimize the voltage overshoot/undershoot the interconnecting wires indicated by heavy lines should be part of ground or power plane in a printed circuit board. The components shown in Figure 8 should be located as close together as possible. Please note that the capacitors CIN and CO each represent numerous physical capacitors. Locate the ISL8118 within 3 inches of the MOSFETs, Q1 and Q2. The circuit traces for the MOSFETs' gate and source connections from the ISL8118 must be sized to handle up to 4A peak current.

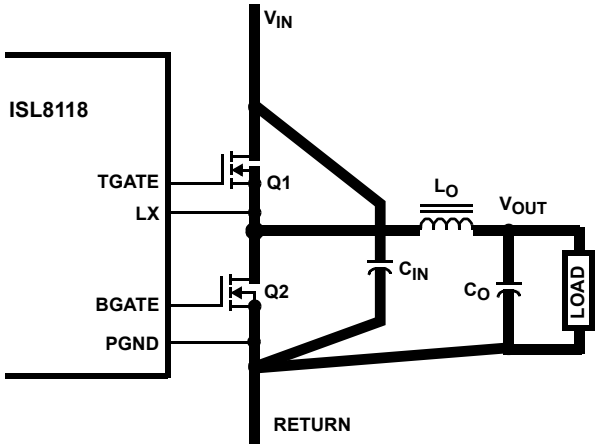


FIGURE 7. PRINTED CIRCUIT BOARD POWER AND GROUND PLANES OR ISLANDS

Proper grounding of the IC is important for correct operation in noisy environments. The PGND pin should be connected to board ground at the source of the bottom side MOSFET with a wide short trace. The GND pin should be connected to a large copper fill under the IC which is subsequently connected to board ground at a quite location on the board, typically found at an input or output bulk (electrolytic) capacitor.

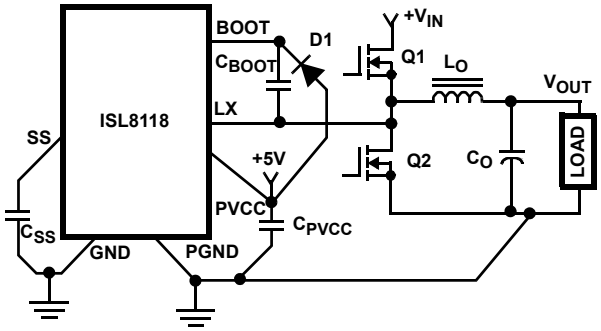


FIGURE 8. PRINTED CIRCUIT BOARD SMALL SIGNAL LAYOUT GUIDELINES

Figure 8 shows the circuit traces that require additional layout consideration. Use single point and ground plane construction for the circuits shown. Minimize any leakage current paths on the SS pin and locate the capacitor, CSS close to the SS pin (as described earlier) as the internal current source is only 38µA. Provide local decoupling between PVCC and PGND pins as described earlier. Locate the capacitor, CBOOT as close as practical to the BOOT and LX pins.

Compensating the Converter

The ISL8118 single-phase converter is a voltage-mode controller. This section highlights the design considerations for a voltage-mode controller requiring external compensation. To address a broad range of applications, a type-3 feedback network is recommended (see Figure 9).

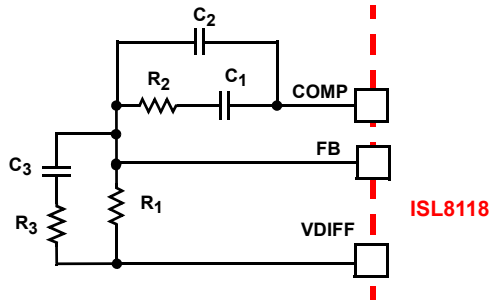


FIGURE 9. COMPENSATION CONFIGURATION FOR ISL8118 WHEN USING DIFFERENTIAL REMOTE SENSE

Figure 10 highlights the voltage-mode control loop for a synchronous-rectified buck converter, when using an internal differential remote sense amplifier. The output voltage (V_{OUT}) is regulated to the reference voltage, VREF, level. The error amplifier output (COMP pin voltage) is compared with the oscillator (OSC) triangle wave to provide a pulse-width modulated wave with an amplitude of V_{IN} at the LX node. The PWM wave is smoothed by the output filter (L and C). The output filter capacitor bank's equivalent series resistance is represented by the series resistor ESR.

The modulator transfer function is the small-signal transfer function of V_{OUT}/V_{COMP}. This function is dominated by a DC gain, given by $d_{MAX}V_{IN}/V_{OSC}$, and shaped by the output filter, with a double pole break frequency at F_{LC} and a zero at F_{CE}. For the purpose of this analysis C and ESR represent the total output capacitance and its equivalent series resistance.

$$F_{LC} = \frac{1}{2\pi \cdot \sqrt{L \cdot C}} \quad \text{(EQ. 7)}$$

$$F_{CE} = \frac{1}{2\pi \cdot C \cdot ESR} \quad \text{(EQ. 8)}$$

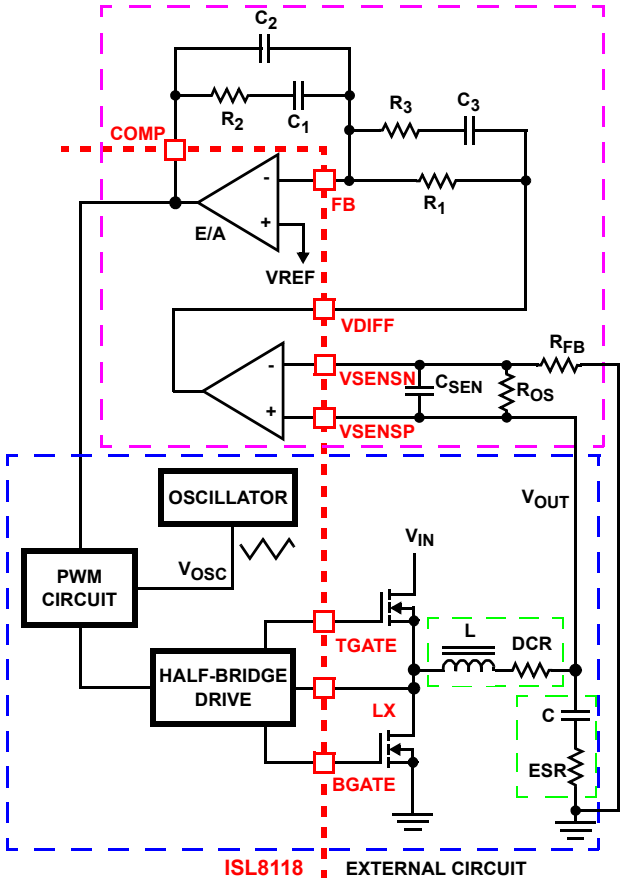


FIGURE 10. VOLTAGE-MODE BUCK CONVERTER COMPENSATION DESIGN

The compensation network consists of the error amplifier (internal to the ISL8118) and the external R_1-R_3, C_1-C_3 components. The goal of the compensation network is to provide a closed loop transfer function with high 0dB crossing frequency (F_0; typically 0.1 to 0.3 of F_{SW}) and adequate phase margin (better than 45°). Phase margin is the difference between the closed loop phase at F_{0dB} and 180°. The equations that follow relate the compensation network's poles, zeros and gain to the components (R_1, R_2, R_3, C_1, C_2, and C_3) in Figures 9 and 10. Use the following guidelines for locating the poles and zeros of the compensation network:

1. Select a value for R_1 (1kΩ to 10kΩ, typically). Calculate value for R_2 for desired converter bandwidth (F_0). If setting the output voltage to be equal to the reference set voltage as shown in Figure 9, the design procedure can be followed as presented. However, when setting the output voltage via a resistor divider placed at the input of the differential amplifier (as shown in Figure 10), in order to compensate for the attenuation introduced by the resistor divider, the below obtained R_2 value needs be multiplied by a factor of $(R_{OS} + R_{FB})/R_{OS}$. The remainder of the calculations remain unchanged, as long as the compensated R_2 value is used.

$$R_2 = \frac{V_{OSC} \cdot R_1 \cdot F_0}{d_{MAX} \cdot V_{IN} \cdot F_{LC}} \quad \text{(EQ. 9)}$$

A small capacitor, C_{SEN} in Figure 10, can be added to filter out noise, typically C_{SEN} is chosen so the corresponding time constant does not reduce the overall phase margin of the design, typically this is 2x to 10x switching frequency of the regulator. As the ISL8118 supports 100% duty cycle, d_{MAX} equals 1. The ISL8118 also uses feed-forward compensation, as such V_{OSC} is equal to 0.16 multiplied by the voltage at the VFF pin. When tying VFF to V_{IN}, Equation 9 simplifies to:

$$R_2 = \frac{0.16 \cdot R_1 \cdot F_0}{F_{LC}} \quad \text{(EQ. 10)}$$

2. Calculate C_1 such that F_{Z1} is placed at a fraction of the F_{LC}, at 0.1 to 0.75 of F_{LC} (to adjust, change the 0.5 factor to desired number). The higher the quality factor of the output filter and/or the higher the ratio F_{CE}/F_{LC}, the lower the F_{Z1} frequency (to maximize phase boost at F_{LC}).

$$C_1 = \frac{1}{2\pi \cdot R_2 \cdot 0.5 \cdot F_{LC}} \quad \text{(EQ. 11)}$$

3. Calculate C_2 such that F_{P1} is placed at F_{CE}.

$$C_2 = \frac{C_1}{2\pi \cdot R_2 \cdot C_1 \cdot F_{CE} - 1} \quad \text{(EQ. 12)}$$

4. Calculate R_3 such that F_{Z2} is placed at F_{LC}. Calculate C_3 such that F_{P2} is placed below F_{SW} (typically, 0.5 to 1.0 times F_{SW}). F_{SW} represents the regulator's switching frequency. Change the numerical factor to reflect desired placement of this pole. Placement of F_{P2} lower in frequency helps reduce the gain of the compensation network at high frequency, in turn reducing the HF ripple component at the COMP pin and minimizing resultant duty cycle jitter.

$$R_3 = \frac{R_1}{\frac{F_{SW}}{F_{LC}} - 1} \quad \text{(EQ. 13)}$$

$$C_3 = \frac{1}{2\pi \cdot R_3 \cdot 0.7 \cdot F_{SW}} \quad \text{(EQ. 14)}$$

It is recommended that a mathematical model is used to plot the loop response. Check the loop gain against the error amplifier's open-loop gain. Verify phase margin results and adjust as necessary. The following equations describe the frequency response of the modulator (G_{MOD}), feedback compensation (G_{FB}) and closed-loop response (G_{CL}):

$$G_{MOD}(f) = \frac{d_{MAX} \cdot V_{IN}}{V_{OSC}} \cdot \frac{1 + s(f) \cdot ESR \cdot C}{1 + s(f) \cdot (ESR + DCR) \cdot C + s^2(f) \cdot L \cdot C} \quad \text{(EQ. 15)}$$

$$G_{FB}(f) = \frac{1 + s(f) \cdot R_2 \cdot C_1}{s(f) \cdot R_1 \cdot (C_1 + C_2)} \cdot \frac{1 + s(f) \cdot (R_1 + R_3) \cdot C_3}{(1 + s(f) \cdot R_3 \cdot C_3) \cdot \left(1 + s(f) \cdot R_2 \cdot \left(\frac{C_1 \cdot C_2}{C_1 + C_2}\right)\right)} \quad \text{(EQ. 16)}$$

$$G_{CL}(f) = G_{MOD}(f) \cdot G_{FB}(f) \quad \text{where, } s(f) = 2\pi \cdot f \cdot j \quad \text{(EQ. 17)}$$

As before, when tying VFF to VIN, terms in the previous equations can be simplified as follows:

$$\frac{d_{MAX} \cdot V_{IN}}{V_{OSC}} = \frac{1 \cdot V_{IN}}{0.16 \cdot V_{IN}} = 6.25 \quad \text{(EQ. 18)}$$

COMPENSATION BREAK FREQUENCY EQUATIONS

$$F_{Z1} = \frac{1}{2\pi \cdot R_2 \cdot C_1} \quad \text{(EQ. 19)}$$

$$F_{Z2} = \frac{1}{2\pi \cdot (R_1 + R_3) \cdot C_3} \quad \text{(EQ. 20)}$$

$$F_{P2} = \frac{1}{2\pi \cdot R_3 \cdot C_3} \quad \text{(EQ. 22)}$$

$$F_{P1} = \frac{1}{2\pi \cdot R_2 \cdot \frac{C_1 \cdot C_2}{C_1 + C_2}} \quad \text{(EQ. 21)}$$

Figure 11 shows an asymptotic plot of the DC/DC converter's gain vs. frequency. The actual modulator gain has a high gain peak dependent on the quality factor (Q) of the output filter, which is not shown. Using the above guidelines should yield a compensation gain similar to the curve plotted. The open loop error amplifier gain bounds the compensation gain. Check the compensation gain at F_{P2} against the capabilities of the error amplifier. The closed loop gain, G_{CL}, is constructed on the log-log graph of Figure 11 by adding the modulator gain, G_{MOD} (in dB), to the feedback compensation gain, G_{FB} (in dB). This is equivalent to multiplying the modulator transfer function and the compensation transfer function and then plotting the resulting gain.

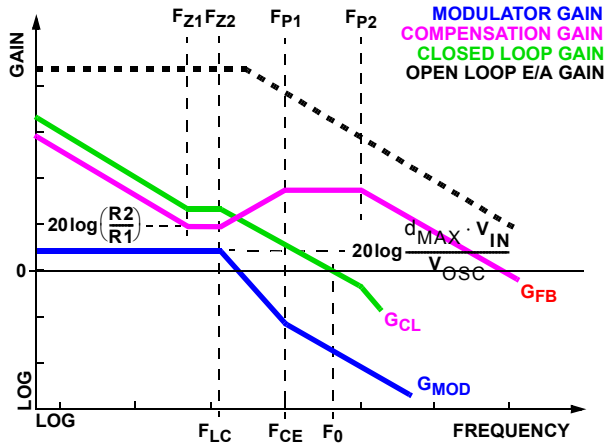


FIGURE 11. ASYMPTOTIC BODE PLOT OF CONVERTER GAIN

A stable control loop has a gain crossing with close to a -20dB/decade slope and a phase margin greater than 45°. Include worst case component variations when determining phase margin. The mathematical model presented makes a number of approximations and is generally not accurate at frequencies approaching or exceeding half the switching frequency. When designing compensation networks, select target crossover frequencies in the range of 10% to 30% of the switching frequency, F_{SW}.

Component Selection Guidelines

Output Capacitor Selection

An output capacitor is required to filter the output and supply the load transient current. The filtering requirements are a function of the switching frequency and the ripple current. The load transient requirements are a function of the slew rate (di/dt) and the magnitude of the transient load current. These requirements are generally met with a mix of capacitors and careful layout.

Modern microprocessors produce transient load rates above 1A/ns. High frequency capacitors initially supply the transient and slow the current load rate seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the ESR (effective series resistance) and voltage rating requirements rather than actual capacitance requirements.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. Consult with the manufacturer of the load on specific decoupling requirements. For example, Intel recommends that the high frequency decoupling for the Pentium Pro be composed of at least forty (40) 1.0µF ceramic capacitors in the 1206 surface-mount package. Follow on specifications have only increased the number and quality of required ceramic decoupling capacitors.

Use only specialized low-ESR capacitors intended for switching-regulator applications for the bulk capacitors. The bulk capacitor's ESR will determine the output ripple voltage and the initial voltage drop after a high slew-rate transient. An aluminum electrolytic capacitor's ESR value is related to the case size with lower ESR available in larger case sizes. However, the equivalent series inductance (ESL) of these capacitors increases with case size and can reduce the usefulness of the capacitor to high slew-rate transient loading. Unfortunately, ESL is not a specified parameter. Work with your capacitor supplier and measure the capacitor's impedance with frequency to select a suitable component. In most cases, multiple electrolytic capacitors of small case size perform better than a single large case capacitor.

Output Inductor Selection

The output inductor is selected to meet the output voltage ripple requirements and minimize the converter's response time to the load transient. The inductor value determines the converter's ripple current and the ripple voltage is a function of the ripple current. The ripple voltage and current are approximated by the following equations:

$$\Delta I = \frac{V_{IN} - V_{OUT}}{F_S \times L} \bullet \frac{V_{OUT}}{V_{IN}} \quad \text{(EQ. 23)}$$

$$\Delta V_{OUT} = \Delta I \times ESR \quad \text{(EQ. 24)}$$

Increasing the value of inductance reduces the ripple current and voltage. However, the large inductance values reduce the converter's response time to a load transient.

One of the parameters limiting the converter's response to a load transient is the time required to change the inductor current. Given a sufficiently fast control loop design, the ISL8118 will provide either 0% or 100% duty cycle in response to a load transient. The response time is the time required to slew the inductor current from an initial current value to the transient current level. During this interval the difference between the inductor current and the transient current level must be supplied by the output capacitor. Minimizing the response time can minimize the output capacitance required.

The response time to a transient is different for the application of load and the removal of load. The following equations give the approximate response time interval for application and removal of a transient load:

$$t_{RISE} = \frac{L_O \times I_{TRAN}}{V_{IN} - V_{OUT}} \quad \text{(EQ. 25)}$$

$$t_{FALL} = \frac{L_O \times I_{TRAN}}{V_{OUT}} \quad \text{(EQ. 26)}$$

where: ITRAN is the transient load current step, tRISE is the response time to the application of load, and tFALL is the response time to the removal of load. With a lower input source such as 1.8V or 3.3V, the worst case response time can be either at the application or removal of load and dependent upon the output voltage setting. Be sure to check both of these equations at the minimum and maximum output levels for the worst case response time.

Input Capacitor Selection

Use a mix of input bypass capacitors to control the voltage overshoot across the MOSFETs. Use small ceramic capacitors for high frequency decoupling and bulk capacitors to supply the current needed each time Q1 turns on. Place the small ceramic capacitors physically close to the MOSFETs and between the drain of Q1 and the source of Q2.

The important parameters for the bulk input capacitor are the voltage rating and the RMS current rating. For reliable operation, select the bulk capacitor with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and a voltage rating of 1.5 times is a conservative guideline. The RMS current rating requirement

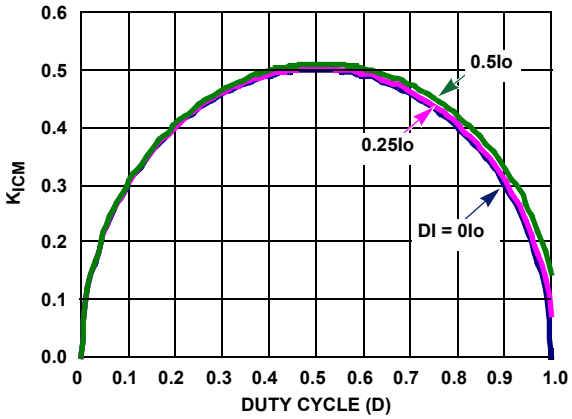


FIGURE 12. INPUT-CAPACITOR CURRENT MULTIPLIER FOR SINGLE-PHASE BUCK CONVERTER

for the input capacitor of a buck regulator is approximated in the following.

$$I_{IN,RMS} = \sqrt{I_O^2(D - D^2) + \frac{\Delta I^2}{12}D} \qquad D = \frac{V_O}{VIN} \qquad \text{(EQ. 27)}$$

OR

$$I_{IN,RMS} = K_{ICM} \bullet I_O$$

For a through hole design, several electrolytic capacitors (Panasonic HFQ series or Nichicon PL series or Sanyo MV-GX or equivalent) may be needed. For surface mount designs, solid tantalum capacitors can be used, but caution must be exercised with regard to the capacitor surge current rating. These capacitors must be capable of handling the surge-current at power-up. The TPS series available from AVX, and the 593D series from Sprague are both surge current tested.

MOSFET Selection/Considerations

The ISL8118 requires 2 N-Channel power MOSFETs. These should be selected based upon rDS(ON), gate supply requirements, and thermal management requirements.

In high-current applications, the MOSFET power dissipation, package selection and heatsink are the dominant design factors. The power dissipation includes two loss components; conduction loss and switching loss. The conduction losses are the largest component of power dissipation for both the top and the bottom MOSFETs. These losses are distributed between the two MOSFETs according to duty factor (see the following equations). The upper MOSFET exhibits turn-on and turn-off switching losses as well as the reverse recover loss, while the synchronous rectifier exhibits body-diode conduction losses during the leading and trailing edge dead times.

$$P_{BOTTOM} = \left(I_O^2 + \frac{\Delta I^2}{12}\right) \bullet \frac{r_{DS(ON)B}}{N_B} \bullet (1 - D) + P_{DEAD} \qquad \text{(EQ. 28)}$$

$$P_{DEAD} = \left[\left(I_O + \frac{\Delta I}{12}\right) \bullet V_{DT} \bullet t_{DT} + \left(I_O - \frac{\Delta I}{12}\right) \bullet V_{DB} \bullet t_{DB}\right] \bullet F_S \qquad \text{(EQ. 29)}$$

$$P_{TOP} = \left(I_O^2 + \frac{\Delta I^2}{12}\right) \bullet \frac{r_{DS(ON),T}}{N_T} \bullet D + P_{SW} + P_{Qrr} \qquad \text{(EQ. 30)}$$

$$P_{SW} = \left[\left(I_O + \frac{\Delta I}{12}\right) \bullet t_{OFF} + \left(I_O - \frac{\Delta I}{12}\right) \bullet t_{ON}\right] \bullet VIN \bullet F_S \qquad \text{(EQ. 31)}$$

$$P_{Qrr} = Q_{rr} \bullet VIN \bullet F_S \qquad \text{(EQ. 32)}$$

where D is the duty cycle = V_O / VIN; Q_{rr} is the reverse recover charge; t_{DL} and t_{DT} are leading and trailing edge dead time, and t_{ON} & t_{OFF} are the switching intervals.

These equations do not include the gate-charge losses that are proportional to the total gate charge and the switching frequency and partially dissipated by the internal gate resistance of the MOSFETs. Ensure that both MOSFETs are within their maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal-resistance specifications. A separate heatsink may be necessary depending upon MOSFET power, package type, ambient temperature and air flow.

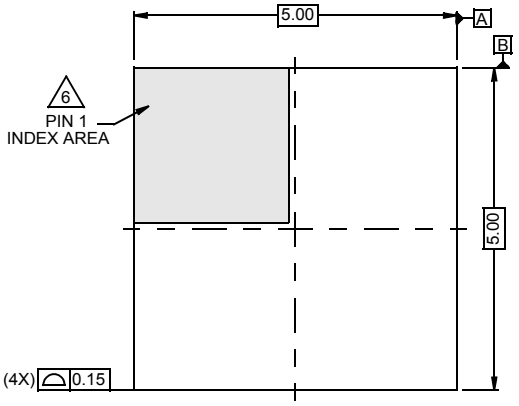
ISL8118 DC/DC Converter Application Circuit

Detailed information on the application circuit, including a complete Bill of Materials and circuit board description, can be found in application note AN1204. See Intersil's home page on the web: http://www.intersil.com.

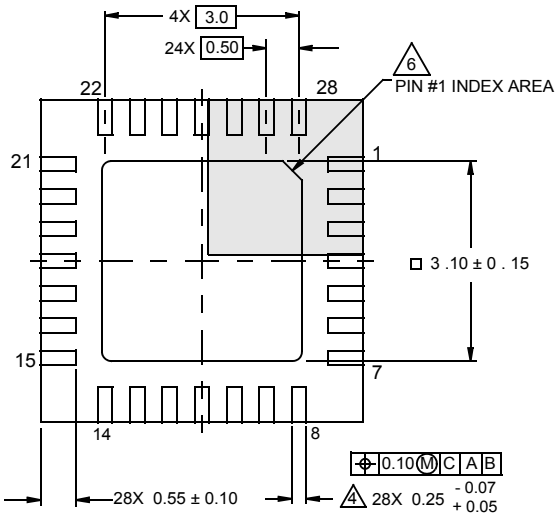
Package Outline Drawing

L28.5x5

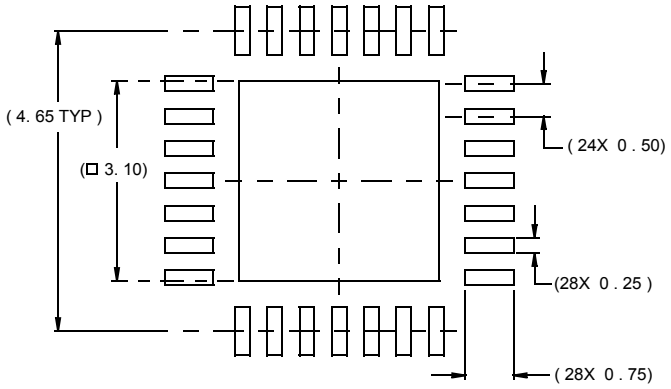
28 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 2, 10/07



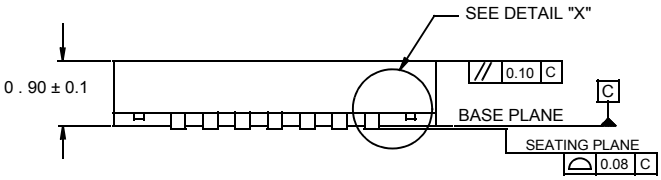
TOP VIEW



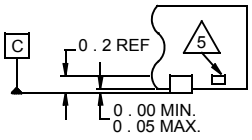
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.