ISL81801

80V Bidirectional 4-Switch Synchronous Buck-Boost Controller

The ISL81801 is a true bidirectional 4-switch synchronous buck-boost controller with peak and average current sensing and monitoring at both ends. With wide input and output voltage ranges, the controller is suitable for industrial, telecommunication, and after-market automotive applications.

The ISL81801 uses a proprietary buck-boost control algorithm with valley current modulation for Boost mode and peak current modulation for Buck mode control.

The ISL81801 has four independent control loops for input and output voltages and currents. Inherent peak current sensing at both ends and cycle-by-cycle current limit of this family of products ensures high operational reliability by providing instant current limit in fast transient conditions at either end and in both directions. It also has two current monitoring pins at both input and output to facilitate Constant Current (CC) limit and other system management functions. CC operation down to low voltages avoids any runaway condition at over load or short-circuit conditions. In addition to multilayer overcurrent protection, it also provides full protection features such as OVP, UVP, OTP, average and peak current limit on both input and output to ensure high reliability in both unidirectional and bidirectional operation.

The IC is packaged in a space-conscious 32 LD 5mm x5mm TQFN package or easy to assemble 4.4mm x9.7mm 38 LD HTSSOP package. Both packages use an EPAD to improve thermal performance and noise immunity. Low pin count, fewer external components, and default internal values make the ISL81801 an ideal solution for time to market simple power supply designs. The unique DE/Burst mode at light-load dramatically lowers standby power consumption with consistent output ripple over different load levels.

Features

- Single inductor 4-switch buck-boost controller
- On-the-fly bidirectional operation with independent control of voltage and current on both ends
- Proprietary algorithm for smoothest mode transition
- MOSFET drivers with adaptive shoot-through protection
- Wide input voltage range: 4.5V to 80V
- Wide output voltage range: 0.8V to 80V
- Supports startup into pre-biased rails
- Programmable frequency: 100kHz to 600kHz
- Supports parallel operation current sharing with cascade phase interleaving
- External sync with clock out or frequency dithering
- External bias for higher efficiency for 8V to 36V input
- Output and input current monitor
- Selectable PWM mode operation between PWM/DE/Burst modes
- Accurate EN/UVLO and PGOOD indicator
- Low shutdown current: 2.7µA
- Complete protection: OCP, SCP, OVP, OTP, and UVP
  - Dual-level OCP with average current and pulse-by-pulse peak current limit, also provides Short Circuit Protection (SCP)
  - Selectable OCP response with either hiccup or constant current mode
  - Negative pulse-by-pulse peak current limit

Applications

- Battery backup
- UPS/storage systems
- Battery powered industrial applications
- Renewable energy
- Aftermarket automotive
- Redundant power supplies
- Robots and drones
- Medical equipment
- Building and industrial automation
- Security surveillance

© 2020-2024 Renesas Electronics

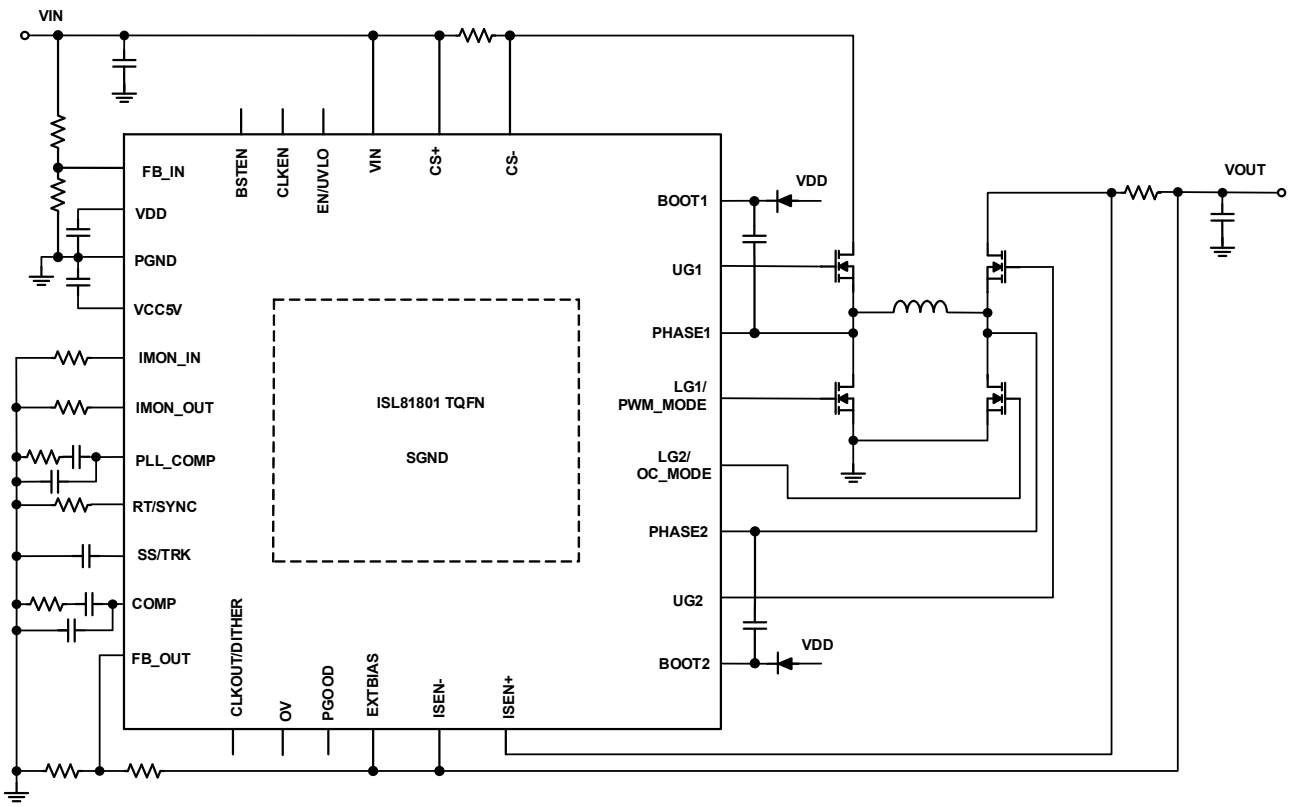


Figure 1. Typical Application Diagram

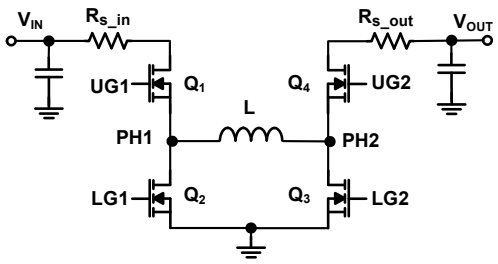


Figure 2. Buck-Boost Power Train Topology

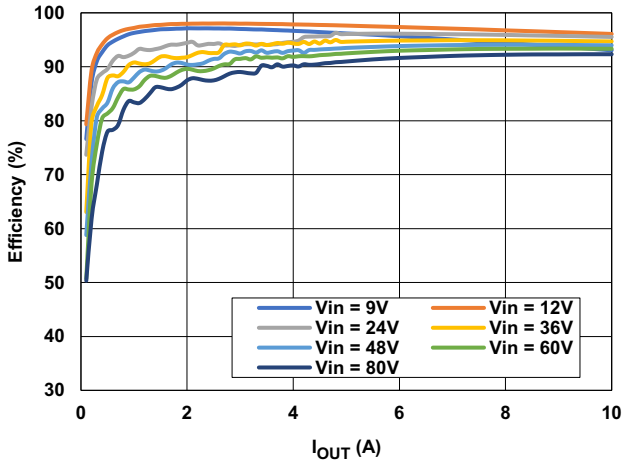


Figure 3. Efficiency (V_{OUT} = 12V, DE Mode)

Contents

1. Overview . . . 5

1.1 Typical Application Schematics . . . 5
1.2 Block Diagram . . . 7
1.3 Ordering Information . . . 8

2. Pin Information. . . . 9

2.1 Pin Assignments . . . 9
2.2 Pin Descriptions . . . 9

3. Specifications. . . . 12

3.1 Absolute Maximum Ratings . . . 12
3.2 Thermal Information. . . . 12
3.3 Recommended Operating Conditions . . . 12
3.4 Electrical Specifications . . . 13

4. Typical Performance Graphs . . . 19

5. Functional Description . . . 25

5.1 General Description . . . 25
5.2 Internal 8V Linear Regulator (VDD), External Bias Supply (EXTBIAS), and 5V Linear Regulator (VCC5V) . . . 25
5.3 Enable (EN/UVLO) and Soft-Start Operation . . . 25
5.4 Tracking Operation . . . 26
5.5 Control Loops . . . 27
5.6 Buck-Boost Conversion Topology and Control Algorithm . . . 30
5.7 Light-Load Efficiency Enhancement . . . 33
5.8 Prebiased Power-Up . . . 34
5.9 Frequency Selection . . . 34
5.10 Phase Lock Loop (PLL) . . . 35
5.11 Frequency Synchronization and Dithering . . . 35
5.12 Parallel Operation Current Sharing . . . 37
5.13 Gate Drivers. . . . 38
5.14 Power-Good Indicator . . . 39

6. Protection Circuits. . . . 40

6.1 Input Undervoltage Lockout (UVLO) . . . 40
6.2 VCC5V Power-On Reset (POR) . . . 40
6.3 Overcurrent Protection (OCP) . . . 40
6.4 Overvoltage Protection (OVP) . . . 41
6.5 Over-Temperature Protection (OTP) . . . 41

7. Layout Guidelines . . . 42

7.1 Layout Considerations . . . 42
7.2 General EPAD Design Considerations . . . 43

8. Component Selection Guideline. . . . 44

8.1 MOSFET Considerations . . . 44
8.2 Inductor Selection . . . 45
8.3 Output Capacitor Selection . . . 45
8.4 Input Capacitor Selection. . . . 46

9. Revision History **47**

10. Package Outline Drawings **48**

1. Overview

1.1 Typical Application Schematics

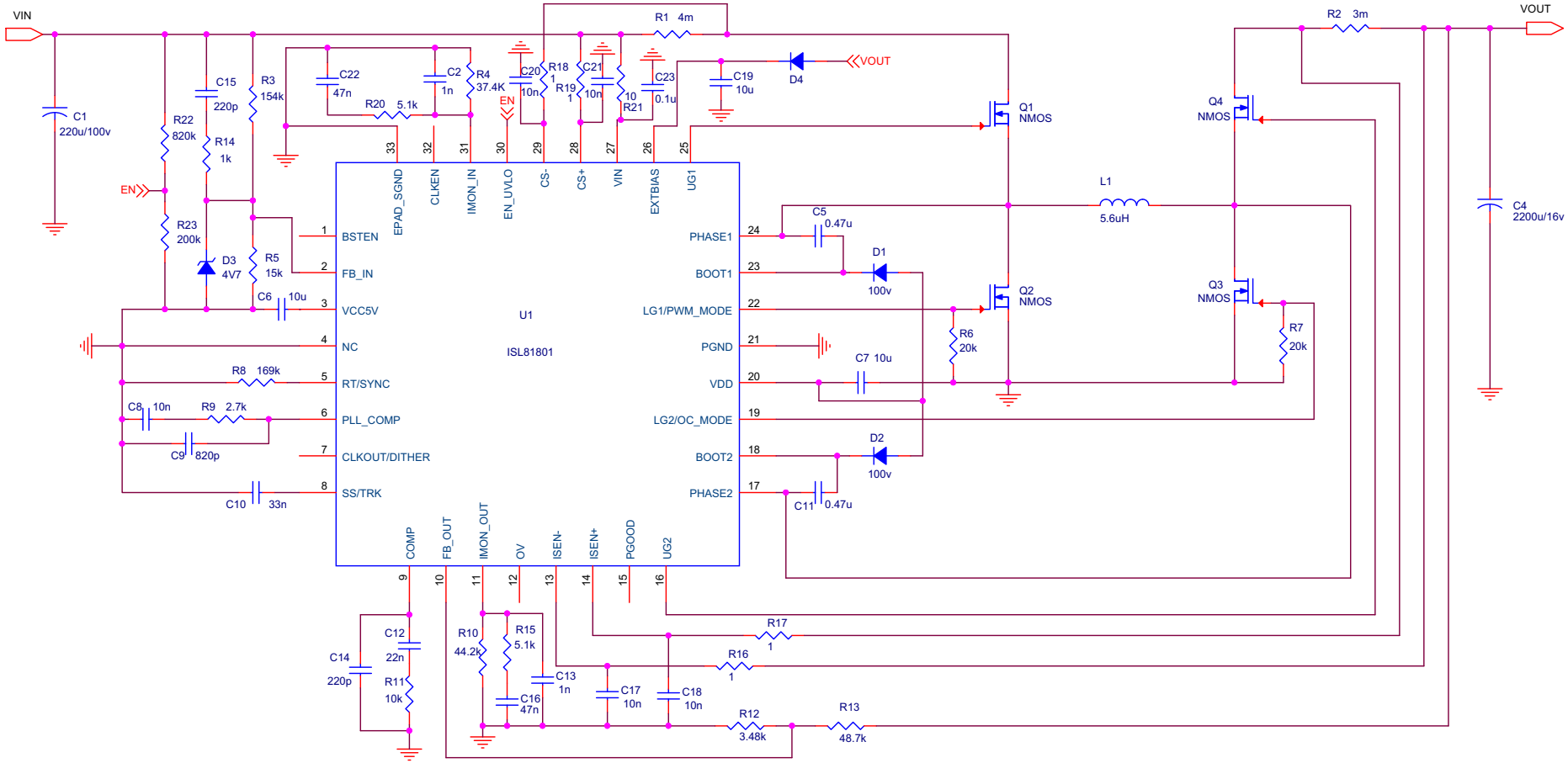


Figure 4. ISL81801EVAL1Z (V_{IN} = 9V to 80V, V_{OUT} = 12V, I_{OUT} = 10A) Evaluation Board Schematic

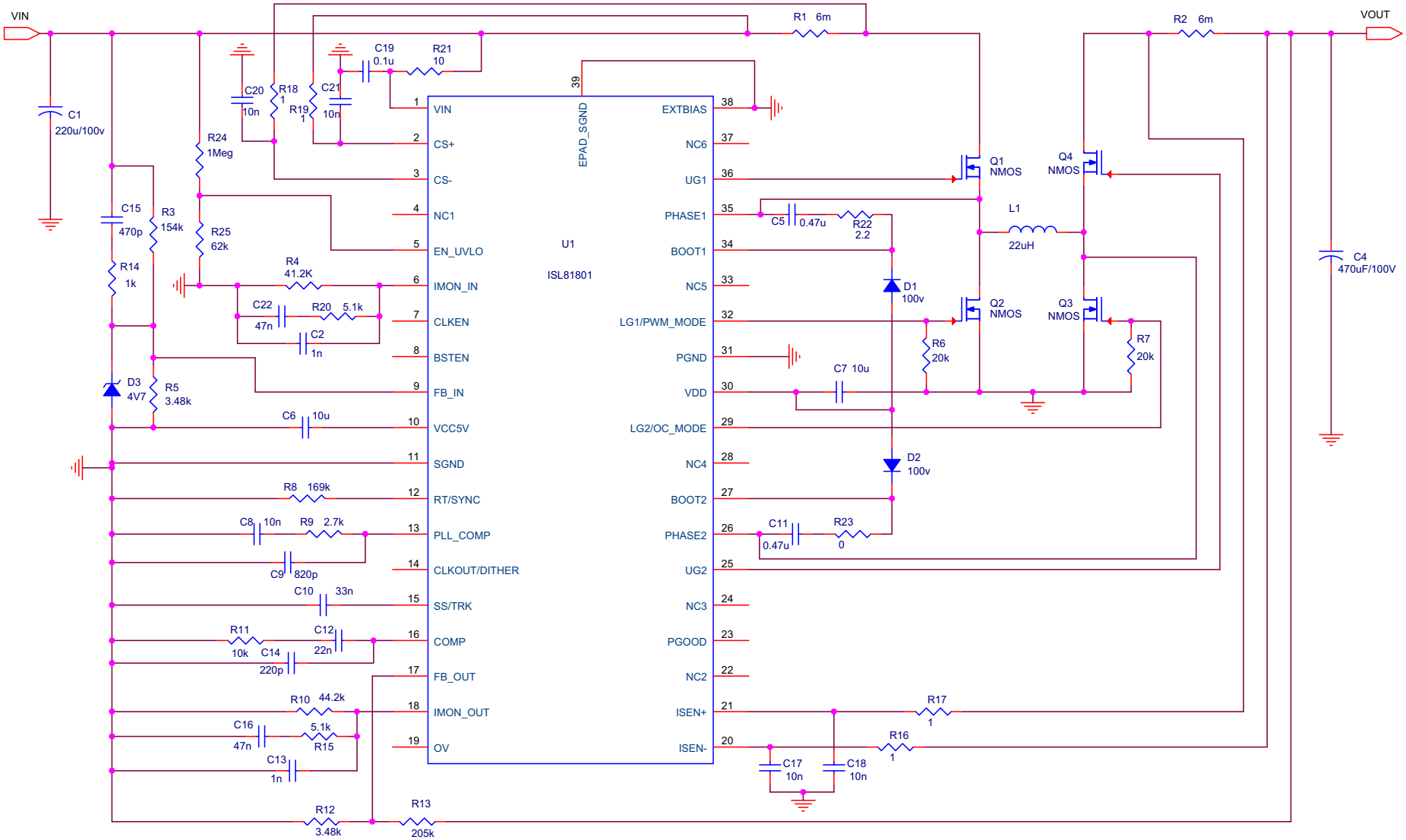


Figure 5. ISL81801EVAL2Z (V_{IN} = 32V to 80V, V_{OUT} = 48V, I_{OUT} = 5A) Evaluation Board Schematic

1.2 Block Diagram

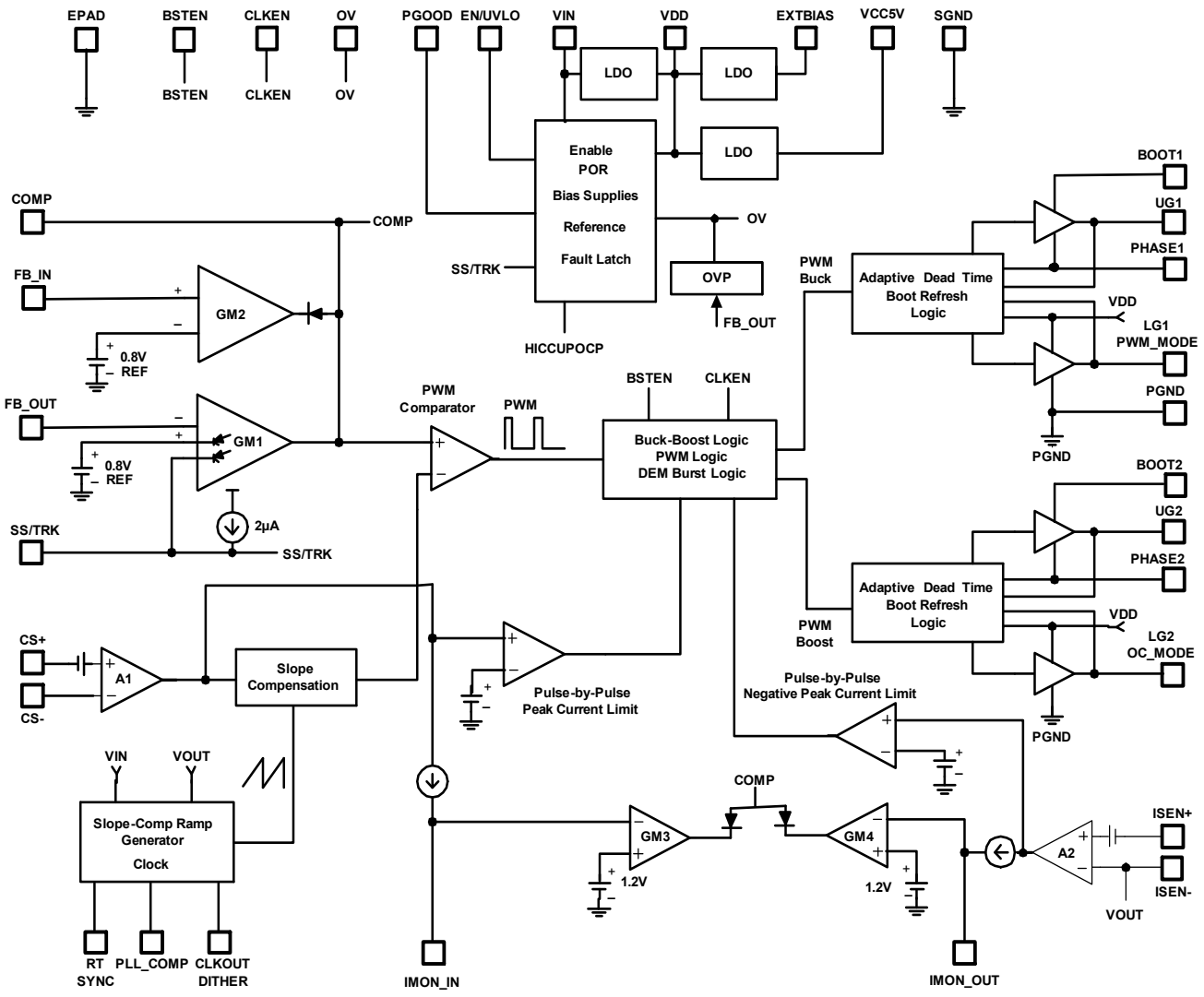


Figure 6. Block Diagram

1.3 Ordering Information

Part Number (Notes 2, 3)	Part Marking	Package Description (RoHS Compliant)	Pkg. Dwg. #	Carrier Type (Note 1)	Temp. Range
ISL81801FRTZ-T	81801 FRTZ	32 Ld 5x5 TQFN	L32.5x5A	Reel, 6k	-40 to +125°C
ISL81801FRTZ-T7A				Reel, 250	
ISL81801FVEZ-T	ISL81801 FVEZ	38 Ld HTSSOP	M38.173C	Reel, 2.5k	
ISL81801FVEZ-T7A				Reel, 250	
ISL81801EVAL1Z	Evaluation Board for TQFN				
ISL81801EVAL2Z	Evaluation Board for HTSSOP				

Notes:

1. See TB347 for details about reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
3. For Moisture Sensitivity Level (MSL), see the ISL81801 device page. For more information about MSL, see TB363.

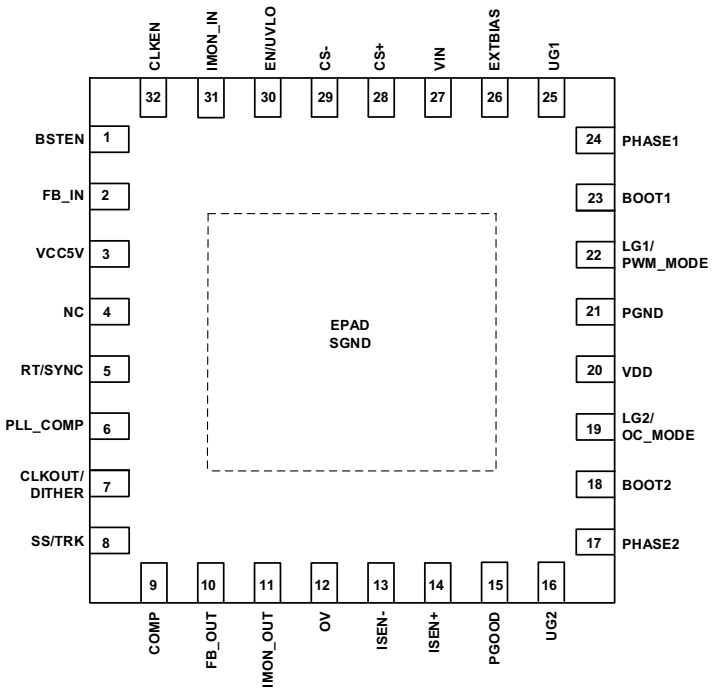
Table 1. Key Differences Between Family of Parts

Part Number	V_{IN} Op/ Max (V)	V_{DD} (V)	Current Control	Parallelable	Dithering	Removed Pins	Pin 12
ISL81801	80/80	8	Bidirectional	Yes	Yes	None	OV
ISL81601	60/70	8	Bidirectional	Yes	Yes	None	OV
ISL81401	40/45	5.3	Bidirectional	Yes	Yes	BSTEN, CLKEN	MODE
ISL81401A	40/45	5.3	Unidirectional	No	No	BSTEN, CLKEN, FIB_IN, CLKOUT	MODE

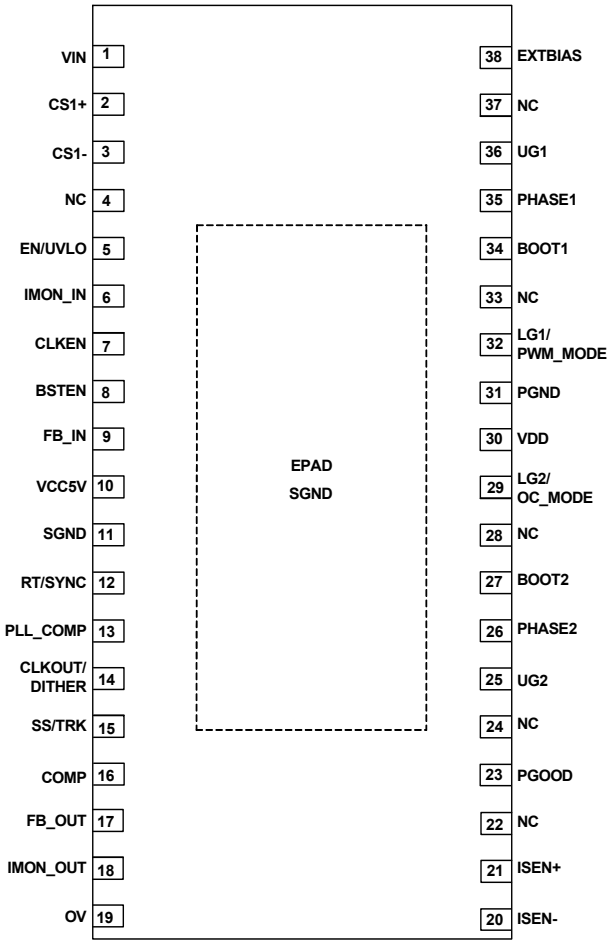
2. Pin Information

2.1 Pin Assignments

32 Ld 5x5 TQFN
Top View



38 Ld HTSSOP
Top View



2.2 Pin Descriptions

Pin # (TQFN)	Pin # (HTSSOP)	Pin Name	Function
1	8	BSTEN	DE Burst mode enable signal. The pin is pulled up to 5V by an internal 250k resistor in PWM and DE mode. It is pulled low in Burst mode. The pull-down MOSFET $r_{DS(ON)}$ resistance is about 4.5k. Connect this pin together in the multi-chip parallel operation application to sync all the chips together for Burst mode operation.
2	9	FB_IN	Input voltage feedback pin for reverse direction operation. Use a resistor divider to feed the input voltage back to this pin. When the input voltage drops and pulls the pin voltage below 0.8V, the internal control loop reduces the duty cycle to sink in current from output to input to keep the pin voltage regulated at 0.8V. Keep the pin voltage below 0.3V to disable the reverse direction operation. When the reverse operation function is not used, tie this pin to VCC5V or SGND to set up the phase shift for the interleaving parallel operation.
3	10	VCC5V	Output of the internal 5V linear regulator. This output supplies bias for the IC. The VCC5V pin must always be decoupled to SGND with a minimum of 4.7µF ceramic capacitor placed close to the pin.
4	4, 22, 24, 28, 33, 37	NC	No connection pin.

Pin # (TQFN)	Pin # (HTSSOP)	Pin Name	Function
5	12	RT/SYNC	A resistor from this pin to ground adjusts the default switching frequency from 100kHz to 600kHz. The default switching frequency of the PWM controller is determined by the resistor R_T as shown in Equation 1. (EQ. 1) $R_T = \left(\frac{34.7}{f_{SW}} - 4.78\right) \cdot k\Omega$ where f_{SW} is the switching frequency in MHz. When this pin is open or tied to VCC5V, f_{SW} is set to 120kHz. When this pin is tied to GND, f_{SW} is set to 575kHz. When an external clock signal is applied to this pin, the internal frequency is synchronized to the external clock frequency.
6	13	PLL_COMP	Compensation pin for the internal PLL circuit. A compensation network shown in the Figure 52 is required. R_{PLL}(2.7kΩ), C_{PLL1} (10nF), and C_{PLL2} (820pF) are recommended.
7	14	CLKOUT/ DITHER	Dual function pin. When there is no capacitor connected to this pin, it provides a clock signal to synchronize the other ISL81801(s). The phase shift of the clock signal is set by the FB_IN and IMON_IN pin voltages. When a capacitor is connected to this pin, the clock out function is disabled and the frequency dither function is enabled before the soft-start. The capacitor is charged and discharged by internal current sources. As the voltage on the pin ramps up and down, the oscillator frequency is modulated between -15% and +15% of the nominal frequency set by the R_T resistor. The frequency dither function is disabled in the external Sync mode or if the RT pin is open or shorted.
8	15	SS/TRK	Dual function pin. When used for soft-start control, a soft-start capacitor is connected from this pin to ground. A regulated 2µA current source charges up the soft-start capacitor. The value of the soft-start capacitor sets the output voltage ramp. When used for tracking control, an external supply rail is configured as the master, and the output voltage of the master supply is applied to this pin using a resistor divider. The output voltage tracks the master supply voltage.
9	16	COMP	Voltage error GM amplifier output. It sets the reference of the inner current loop. The feedback compensation network is connected between the COMP and SGND pins. When the COMP pin is pulled below 1V, the PWM duty cycle reduces to 0%.
10	17	FB_OUT	Output voltage feedback input. Connect FB_OUT to a resistive voltage divider between the output and SGND to adjust the output voltage. The FB_OUT pin voltage is regulated to the internal 0.8V reference.
11	18	IMON_OUT	Output current monitor. The current from this pin is proportional to the differential voltage between the ISEN+ and ISEN- pins. Connect a resistor and capacitor network between this pin and SGND to make the pin voltage proportional to the average output current. When the pin voltage reaches 1.2V, the internal average current limit loop reduces the output voltage to keep the output current constant when constant current OCP mode is set or the converter shuts down when hiccup OCP mode is set. In DE Burst mode, when this pin voltage is less than 850mV, the controller runs in Burst mode. When this pin voltage is higher than 880mV, the controller exits Burst mode. When a higher resistance on this pin sets its voltage higher than 880mV at no load condition, the controller runs in DE mode with no burst operation.
12	19	OV	OVP comparator output signal. The pin is pulled low to GND by an internal 250k resistor in normal operation. It is pulled high when output OVP trips. The pull-up MOSFET $r_{DS(ON)}$ resistance is about 4.5k. Connect this pin with other OV pins in multi-chip parallel operation applications to sync all of the OV indicators of the chips together for the OVP reaction.
13	20	ISEN-	Output current sense signal negative input pin.
14	21	ISEN+	Output current sense signal positive input pin.
15	23	PGOOD	Power Good open-drain logic output that indicates the status of output voltage. This pin is pulled low when the output is not within ±10% of the nominal voltage or the EN pin is pulled LOW.
16	25	UG2	High-side MOSFET gate driver output controlled by the boost PWM signal.
17	26	PHASE2	Phase node connection of the boost converter. This pin is connected to the junction of the upper MOSFET source, filter inductor, and lower MOSFET drain of the boost converter.
18	27	BOOT2	Bootstrap pin to provide bias for the boost high-side driver. The positive terminal of the bootstrap capacitor connects to this pin. Connect a bootstrap diode between this pin and VDD to create the bias for the high-side driver. The BOOT2 to PHASE2 voltage is monitored internally. When the voltage drops to 5.95V at no switching condition, a minimum off-time pulse is issued to turn off UG2 and turn on LG2 to refresh the bootstrap capacitor and maintain the high-side driver bias voltage.

Pin # (TQFN)	Pin # (HTSSOP)	Pin Name	Function
19	29	LG2/ OC_MODE	Low-side MOSFET gate driver output controlled by the boost PWM signal and OCP mode set pin. The OCP mode is set by a resistor connected between the pin and ground during the initialization period before soft-start. During the initialization period, the pin sources 10µA of current to set the voltage on the pin. If the pin voltage is less than 0.3V, OCP is set to constant current mode. If the pin voltage is greater than 0.3V, OCP is set to Hiccup mode.
20	30	VDD	Output of the internal 8V linear regulator supplied by either VIN or EXTBIAS. This output supplies bias for the IC low-side drivers and the boot circuitries for the high-side drivers. The VDD pin must always be decoupled to PGND pin with a minimum of 4.7µF ceramic capacitor placed close to the pin.
21	31	PGND	Power ground connection. Connect the pin to the sources of the lower MOSFETs and the (-) terminals of the VDD decoupling capacitors.
22	32	LG1/ PWM_MODE	Low-side MOSFET gate driver output controlled by the buck PWM signal and PWM mode set pin. The PWM mode is set by a resistor connected between the pin and ground during the initialization period before soft-start. During the initialization period, the pin sources 10µA of current to set the voltage on the pin. If the pin voltage is less than 0.3V, the converter is set to forced PWM mode. If the pin voltage is greater than 0.3V, the converter is set to Diode Emulation (DE) mode.
23	34	BOOT1	Bootstrap pin to provide bias for the buck high-side driver. The positive terminal of the bootstrap capacitor connects to this pin. Connect a bootstrap diode between this pin and VDD to create the bias for the high-side driver. The BOOT1 to PHASE1 voltage is monitored internally. When the voltage drops to 5.95V at no switching condition, a minimum off-time pulse is issued to turn off UG1 and turn on LG1 to refresh the bootstrap capacitor and maintain the high-side driver bias voltage.
24	35	PHASE1	Phase node connection of the buck converter. This pin is connected to the junction of the upper MOSFET source, filter inductor, and the lower MOSFET drain of the buck converter.
25	36	UG1	High-side MOSFET gate driver output controlled by the buck PWM signal.
26	38	EXTBIAS	External bias input for the optional VDD LDO. There is an internal switch to disconnect the VIN LDO when EXTBIAS voltage is higher than 7.5V. Decouple this pin to ground with a 10µF ceramic capacitor when it is in use, otherwise tie this pin to ground. DO NOT float this pin.
27	1	VIN	Tie this pin to the input rail using a 5-10Ω resistor. It provides power to the internal LDO for VDD. Decouple this pin with a small ceramic capacitor (10nF to 1µF) to ground.
28	2	CS+	Input current sense signal positive input pin.
29	3	CS-	Input current sense signal negative input pin.
30	5	EN/ UVLO	This pin provides enable/disable and accurate UVLO functions. The output is disabled when the pin is pulled to ground. When the voltage on the pin reaches 1.3V, the VDD and VCC5V LDOs become active. When the voltage on the pin reaches 1.8V, the PWM modulator is enabled. When the pin is floating, it is enabled by default by an internal pull-up. **Note**: The maximum current into the EN/UVLO pin should not exceed 100µA.
31	6	IMON_IN	Input current monitor. The current from this pin is proportional to the differential voltage between the CS+ and CS- pins. Connect a resistor and capacitor network between the pin and SGND to make the pin voltage proportional to the average input current. When the pin voltage reaches 1.2V, the internal average current limit loop reduces the output voltage to keep the input current constant when constant current OCP mode is set or the converter shuts down when hiccup OCP mode is set. When the input current monitor function is not used, tie this pin to VCC5V or SGND to set up phase shift for interleaved parallel operation.
32	7	CLKEN	DE mode burst operation off state enable signal. The pin is pulled up to 5V by an internal 250k resistor in PWM and DE modes and burst mode on state. It is pulled low in Burst mode off state. The pull-down MOSFET $r_{DS(ON)}$ resistance is about 4.5k. Connect this pin with other CLKEN pins in multi-chip parallel operation applications to sync all the chips together for burst operation.
-	11	SGND EPAD	Small-signal ground common to all control circuitries. Route this pin separately from the high current ground (PGND). Tie SGND and PGND together if there is one solid ground plane with no noisy currents around the chip. All voltage levels are measured with respect to this pin. EPAD at ground potential. EPAD is connected to SGND internally. However, Renesas highly recommends soldering it directly to the ground plane for better thermal performance and noise immunity.

3. Specifications

3.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
VCC5V, EN/UVLO, FB_IN to GND	-0.3	+5.9	V
VDD to GND	-0.3	+9	V
EXTBIAS to GND	-0.3	+40	V
VIN, CS+, CS-, ISEN+, ISEN- to GND	-0.3	+85	V
BOOT1, 2/UG1, 2 to PHASE1, 2	-0.3	+12	V
PHASE1, 2 to GND	-5 (<20ns)/-0.3 (DC)	+85	V
FB_OUT, SS/TRK, COMP, RT/SYNC, PLL_COMP, CLKOUT/DITHER, BSTEN, CLKEN, OV, PGOOD, IMON_IN, IMON_OUT to GND	-0.3	VCC5V + 0.3	V
LG1/PWM_MODE, LG2/OC_MODE to GND	-0.3	V_{DD} + 0.3	V
CS+ to CS- and ISEN+ to ISEN-	-0.3	+0.3	V
VCC5V, VDD Short-Circuit to GND Duration	1		s
ESD Ratings	**Value**		**Unit**
Human Body Model (Tested per JS-001-2017)	2.5		kV
Charge Device Model (Tested per JS-002-2014)	1		kV
Latch-Up (Tested per JESD78E; Class II, Level A, +125°C (T_J))	100		mA

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

3.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
32 Ld TQFN Package (Notes 4, 5)	29	1
38 Ld HTSSOP (Notes 4, 5)	29	2

Notes:

4. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.
5. For θ_{JC}, the case temperature location is the center of the exposed metal pad on the package underside.

Parameter	Minimum	Maximum	Unit
Junction Temperature	-55	+150	°C
Operating Temperature	-40	+125	°C
Storage Temperature Range	-65	+150	°C
Pb-Free Reflow Profile	see TB493		

3.3 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Temperature	-40	+125	°C
VIN to GND	4.5	80	V
VCC5V, EN/UVLO, FB_IN to GND	0	5.4	V
VDD to GND	0	8.4	V
EXTBIAS to GND	0	36	V

3.4 Electrical Specifications

Recommended operating conditions unless otherwise noted. See Block Diagram and Typical Application Schematics. V_{IN} = 4.5V to 80V, or V_{DD} = 8V ±10%, C_VCC5V = 4.7µF, T_A = -40°C to +125°C, Typical values are at T_A = +25°C, unless otherwise specified. **Boldface limits apply across the operating temperature range, -40°C to +125°C.**

Parameter	Symbol	Test Conditions	Min (Note 6)	Typ	Max (Note 6)	Unit
V_{IN} Supply						
Input Voltage Range	V_{IN}		**4.5**		**80.0**	V
V_{IN} Supply Current						
Shutdown Current (Note 7)	I_{VINQ}	EN = 0V, PGOOD is floating		2.7	**6.0**	µA
Operating Current (Note 8)	I_{VINOP}	PGOOD is floating, EXTBIAS = 0V		5	**7**	mA
		PGOOD is floating, EXTBIAS = 12V		50		µA
VCC5V Supply						
Internal LDO Output Voltage	V_{CC5V}	V_{IN} = 8V, I_L = 0mA	**4.7**	5.0	**5.4**	V
		V_{IN} = 80V, I_L = 0mA	**4.7**	5.0	**5.4**	V
		V_{IN} = 4.5V, I_L = 5mA	**4.00**	4.25		V
		V_{IN} > 5.6V, I_L = 10mA	**4.65**	5.00		V
Maximum Supply Current of Internal LDO	I_{VCC_MAX}	V_{VCC5V} = 0V, V_{IN} = 8V		120		mA
V_{DD} Supply						
Internal LDO Output Voltage	V_{DD}	V_{IN} = 12V, EXTBIAS = 0V, I_L = 0mA	**7.5**	8.0	**8.4**	V
		V_{IN} = 80V, EXTBIAS = 0V, I_L = 0mA	**7.5**	8.0	**8.4**	V
		V_{IN} = 4.5V, EXTBIAS = 12V, I_L = 0mA	**7.5**	8.0	**8.4**	V
		V_{IN} = 80V, EXTBIAS = 12V, I_L = 0mA	**7.5**	8.0	**8.4**	V
		V_{IN} = 4.5V, EXTBIAS = 0V, I_L = 30mA	**3.9**	4.3		V
		V_{IN} = 4.5V, EXTBIAS = 7.8V, I_L = 30mA	**7.4**	7.6		V
		V_{IN} > 8.6V, EXTBIAS = 0V, I_L = 75mA	**7.30**	7.85		V
		V_{IN} = 4.5V, EXTBIAS > 9.0V, I_L = 75mA	**7.30**	7.85		V
Maximum Supply Current of Internal LDO	I_{VDD_MAX}	V_{VDD} = 0V, EXTBIAS = 0V, V_{IN} = 12V		120		mA
		V_{VDD} = 4.5V, EXTBIAS = 12V, V_{IN} = 4.5V		140		mA
EXTBIAS Supply						
Switch Over Threshold Voltage, Rising	V_{EXT_THR}	EXTBIAS voltage	**7.10**	7.38	**7.55**	V
Switch Over Threshold Voltage, Falling	V_{EXT_THF}	EXTBIAS voltage	**6.60**	6.85	**7.10**	V
V_{IN} UVLO						
V_{IN} Rising UVLO Threshold (Note 10)	$V_{UVLOTHR}$	V_{IN} voltage, 0mA on VCC5V and VDD		3.50		V
V_{IN} Falling UVLO Threshold	$V_{UVLOTHF}$	V_{IN} voltage, 0mA on VCC5V and VDD	**3.0**	3.2	**3.4**	V
VCC5V Power-On Reset						
VCC5V Rising POR Threshold	V_{PORTHR}	VCC5V voltage, 0mA on VCC5V and VDD	**3.7**	4.0	**4.3**	V
VCC5V Falling POR Threshold	V_{PORTHF}	VCC5V voltage, 0mA on VCC5V and VDD	**3.30**	3.55	**3.75**	V
EN/UVLO Threshold						
EN Rise Threshold	V_{ENSS_THR}	V_{IN} > 5.6V	**0.75**	1.05	**1.30**	V
EN Fall Threshold	V_{ENSS_THF}	V_{IN} > 5.6V	**0.60**	0.90	**1.10**	V
EN Hysteresis	V_{ENSS_HYST}	V_{IN} > 5.6V	**70**	150	**300**	mV
UVLO Rise Threshold	V_{UVLO_THR}	V_{IN} > 5.6V	**1.77**	1.80	**1.83**	V
UVLO Hysteresis Current	I_{UVLO_HYST}	V_{IN} = 12V, EN/UVLO = 1.815V	**2.5**	4.4	**6.0**	µA

Recommended operating conditions unless otherwise noted. See Block Diagram and Typical Application Schematics. V_{IN} = 4.5V to 80V, or V_{DD} = 8V ±10%, C_VCC5V = 4.7µF, T_A = -40°C to +125°C, Typical values are at T_A = +25°C, unless otherwise specified. **Boldface limits apply across the operating temperature range, -40°C to +125°C. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 6)	Typ	Max (Note 6)	Unit
Soft-Start Current						
SS/TRK Soft-Start Charge Current	I_{SS}	SS/TRK = 0V		2.00		µA
Default Internal Minimum Soft-Starting						
Default Internal Output Ramping Time	t_{SS_MIN}	SS/TRK open		1.7		ms
Power-Good Monitors						
PGOOD Upper Threshold	V_{PGOV}		**107**	109	**112**	%
PGOOD Lower Threshold	V_{PGUV}		**87**	90	**92**	%
PGOOD Low Level Voltage	V_{PGLOW}	I_SINK = 2mA			**0.35**	V
PGOOD Leakage Current	I_{PGLKG}	PGOOD = 5V		0	**150**	nA
PGOOD Timing						
V_{OUT} Rising Threshold to PGOOD Rising (Note 9)	t_{PGR}			1.1	**5**	ms
V_{OUT} Falling Threshold to PGOOD Falling	t_{PGF}			80		µs
Reference Section						
Internal Voltage Loop Reference Voltage	V_{REFV}			0.800		V
Reference Voltage Accuracy		T_A = 0°C to +85°C	**-0.75**		**+0.75**	%
		T_A = -40°C to +125°C	**-1.00**		**+1.00**	%
Internal Current Loop Reference Voltage	V_{REFI}			1.200		V
Reference Voltage Accuracy		T_A = 0°C to +85°C	**-0.75**		**+0.75**	%
		T_A = -40°C to +125°C	**-1.00**		**+1.00**	%
PWM Controller Error Amplifiers						
FB_OUT Pin Bias Current	$I_{FBOUTLKG}$		**-50**	0	**+50**	nA
FB_OUT Error Amp GM	Gm1			1.85		mS
FB_OUT Error Amp Voltage Gain	AV1			82		dB
FB_OUT Error Amp Gain-BW Product	GBW1			8		MHz
FB_OUT Error Amp Output Current Capability				±310		µA
COMP Max High Voltage	V_{COMP_HIGH}	FB_OUT = 0V		3.8		V
COMP Min Low Voltage	V_{COMP_LOW}	FB_OUT = 1V		0.01		V
FB_IN Pin Bias Current	$I_{FBINLKG}$		**-50**	0	**+50**	nA
FB_IN Error Amp GM	Gm2			12		µS
FB_IN Error Amp Voltage Gain	AV2			72		dB
FB_IN Error Amp Gain-BW Product	GBW2			5		MHz
FB_IN Active Range (Note 10)	$V_{FB_IN_ACT}$	VCC5V = 5V	**0**		**4.3**	V
FB_IN Logic Low Threshold (Note 10)	$V_{FB_IN_L}$		**0.2**			V
FB_IN Logic High Threshold (Note 10)	$V_{FB_IN_H}$	VCC5V = 5V			**4.7**	V

Recommended operating conditions unless otherwise noted. See Block Diagram and Typical Application Schematics. V_{IN} = 4.5V to 80V, or V_{DD} = 8V ±10%, C_VCC5V = 4.7µF, T_A = -40°C to +125°C, Typical values are at T_A = +25°C, unless otherwise specified. **Boldface limits apply across the operating temperature range, -40°C to +125°C. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 6)	Typ	Max (Note 6)	Unit
PWM Regulator						
Buck Mode Minimum Off-Time	t_{OFF_MIN1}			200		ns
Buck Mode Minimum On-Time	t_{ON_MIN1}			100		ns
Boost Mode Minimum Off-Time	t_{OFF_MIN2}			150		ns
Boost Mode Minimum On-Time	t_{ON_MIN2}			150		ns
Buck Mode Peak-to-Peak Sawtooth Amplitude	DV_{RAMP1}	$V_{IN} = V_{OUT}$ = 12V, f_{SW} = 300kHz		1.0		V
Boost Mode Peak-to-Peak Sawtooth Amplitude	DV_{RAMP2}	$V_{IN} = V_{OUT}$ = 12V, f_{SW} = 300kHz		0.9		V
Buck Mode Ramp Offset	$V_{ROFFSET1}$		**0.88**	1.0	**1.11**	V
Boost Mode Ramp Offset	$V_{ROFFSET2}$		**2.84**	3.3	**3.7**	V
Current Sense, Current Monitors, and Average Current Loop						
Input Current Sense Differential Voltage Range	$V_{CS+} - V_{CS-}$		**-80**		**+150**	mV
Input Current Sense Common-Mode Voltage Range	$CMIR_{CS}$		**0**		**80**	V
IMON_IN Offset Current	$I_{CSOFFSET}$	CS+ = CS- = 12V	**17**	19.5	**21.5**	µA
Input Current Sense Voltage to IMON_IN Current Source Gain	Gm_{CS}	12V common-mode voltage applied to CS± pins, 0 to 40mV differential voltage	**170**	205	**230**	µS
IMON_IN Error Amp GM	Gm3			12		µS
IMON_IN Error Amp Voltage Gain	AV3			72		dB
IMON_IN Active Range (Note 10)	$V_{IMON_IN_ACT}$	VCC5V = 5V	**0**		**4.3**	V
IMON_IN Logic High Threshold (Note 10)	$V_{IMON_IN_H}$	VCC5V = 5V			**4.7**	V
IMON_IN Error Amp Gain-BW Product	GBW3			5		MHz
Output Current Sense Differential Voltage Range	$V_{ISEN+} - V_{ISEN-}$		**-80**		**+150**	mV
Output Current Sense Common-Mode Voltage Range	$CMIR_{ISEN}$		**0**		**80**	V
IMON_OUT Offset Current	$I_{ISENOFFSET}$	ISEN+ = ISEN- = 12V	**17**	19.5	**21**	µA
IMON_OUT Current		ISEN+ = 12V. ISEN- = 11.96V	**25**	27.5	**28.5**	µA
Output Current Sense Voltage to IMON_OUT Current Source Gain	Gm_{ISEN}	12V common-mode voltage applied to ISEN± pins, 0mV to 40mV differential voltage	**170**	205	**235**	µS
IMON_OUT Error Amp GM	Gm4			12		µS
IMON_OUT Error Amp Voltage Gain	AV4			72		dB
IMON_OUT Error Amp Gain-BW Product	GBW4			5		MHz
Switching Frequency and Synchronization						
Switching Frequency	f_{SW}	R_T = 144kΩ	**220**	245	**265**	kHz
		R_T = 72kΩ	**420**	450	**485**	kHz
		R_T Open or to VCC5V	**90**	120	**145**	kHz
		R_T = 0V	**470**	575	**650**	kHz
RT Voltage	V_{RT}	R_T = 72kΩ		560		mV
SYNC Synchronization Range	f_{SYNC}		**140**		**600**	kHz
SYNC Input Logic High (Note 10)	V_{SYNCH}		**3.2**			V
SYNC Input Logic Low (Note 10)	V_{SYNCL}				**0.5**	V

Recommended operating conditions unless otherwise noted. See Block Diagram and Typical Application Schematics. V_{IN} = 4.5V to 80V, or V_{DD} = 8V ±10%, C_VCC5V = 4.7µF, T_A = -40°C to +125°C, Typical values are at T_A = +25°C, unless otherwise specified. **Boldface limits apply across the operating temperature range, -40°C to +125°C. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 6)	Typ	Max (Note 6)	Unit
Clock Output and Frequency Dither						
CLKOUT Output High	V_{CLKH}	I_{SOURCE} = 1mA, VCC5V = 5V	**4.55**			V
CLKOUT Output Low	V_{CLKL}	I_{SINK} = 1mA			**0.3**	V
CLKOUT Frequency	f_{CLK}	R_T = 72kΩ	**420**	450	**485**	kHz
Dither Mode Setting Current Source	$I_{DITHER_MODE_SO}$			12		µA
Dither Mode Setting Threshold Low	$V_{DITHER_MODE_L}$		**0.26**			V
Dither Mode Setting Threshold High	$V_{DITHER_MODE_H}$				**0.34**	V
Dither Source Current	$I_{DITHERSO}$			8		µA
Dither Sink Current	$I_{DITHERSI}$			10		µA
Dither High Threshold Voltage	$V_{DITHERH}$			2.2		V
Dither Low Threshold Voltage	$V_{DITHERL}$			1.05		V
Diode Emulation Mode Detection						
LG1/PWM_MODE Current Source	$I_{MODELG1}$		**7.5**	10	**13**	µA
LG1/PWM_MODE Threshold Low	$V_{MODETHL}$		**0.26**			V
LG1/PWM_MODE Threshold High	$V_{MODETHH}$				**0.34**	V
Buck Mode Diode Emulation Phase Threshold (Note 11)	V_{CROSS1}	V_{IN} = 12V		2		mV
Boost Mode Diode Emulation Shunt Threshold (Note 12)	V_{CROSS2}	V_{IN} = 12V		-5		mV
Diode Emulation Burst Mode						
Burst Mode Enter Threshold	$V_{IMONOUTBSTEN}$	IMON_OUT pin voltage	**0.808**	0.835	**0.86**	V
Burst Mode Exit Threshold	$V_{MONOUTBSTEX}$	IMON_OUT pin voltage	**0.83**	0.88	**0.92**	V
Burst Mode Peak Current Limit Input Shunt Set Point	$V_{BST\text{-}CS}$	V_{CS+} - V_{CS-}, 12V common-mode voltage applied to CS± pins	**16**	27	**39**	mV
Burst Mode Peak FB Voltage Limit Set Point	$V_{BST\text{-}VFB\text{-}UTH}$			0.82		V
Burst Mode Exit FB Voltage Set Point	$V_{BST\text{-}VFB\text{-}LTH}$			0.78		V
BSTEN Output Logic High	$V_{BSTEN\text{-}OH}$	No load, VCC5V = 5V		4.9		V
BSTEN Output Logic Low	$V_{BSTEN\text{-}OL}$	Pull-up resistance 100kΩ		0.07		V
BSTEN Input Logic High (Note 10)	$V_{BSTEN\text{-}IH}$		**3.2**			V
BSTEN Input Logic Low (Note 10)	$V_{BSTEN\text{-}IL}$				**1**	V
CLKEN Output Logic High	$V_{CLKEN\text{-}OH}$	No load, VCC5V = 5V		4.9		V
CLKEN Output Logic Low	$V_{CLKEN\text{-}OL}$	Pull-up resistance 100kΩ		0.07		V
CLKEN Input Logic High (Note 10)	$V_{CLKEN\text{-}IH}$		**3.2**			V
CLKEN Input Logic Low (Note 10)	$V_{CLKEN\text{-}IL}$				**1**	V
PWM Gate Drivers						
Driver 1, 2 BOOT Refresh Trip Voltage	$V_{BOOTRF1,2}$	BOOT voltage - PHASE voltage	**5.4**	5.95	**6.65**	V
Driver 1, 2 Source and Upper Sink Current	$I_{GSRC1,2}$			2000		mA
Driver 1, 2 Lower Sink Current	$I_{GSNK1,2}$			3000		mA
Driver 1, 2 Upper Drive Pull-Up	$R_{UG_UP1,2}$			2.2		Ω
Driver 1, 2 Upper Drive Pull-Down	$R_{UG_DN1,2}$			1.7		Ω
Driver 1, 2 Lower Drive Pull-Up	$R_{LG_UP1,2}$			3		Ω
Driver 1, 2 Lower Drive Pull-Down	R_{LG_DN}			2		Ω

Recommended operating conditions unless otherwise noted. See Block Diagram and Typical Application Schematics. V_{IN} = 4.5V to 80V, or V_{DD} = 8V ±10%, C_VCC5V = 4.7µF, T_A = -40°C to +125°C, Typical values are at T_A = +25°C, unless otherwise specified. **Boldface limits apply across the operating temperature range, -40°C to +125°C. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 6)	Typ	Max (Note 6)	Unit
Driver 1, 2 Upper Drive Rise Time	t_{GR_UP}	C_{OUT} = 1000pF		10		ns
Driver 1, 2 Upper Drive Fall Time	t_{GF_UP}	C_{OUT} = 1000pF		10		ns
Driver 1, 2 Lower Drive Rise Time	t_{GR_DN}	C_{OUT} = 1000pF		10		ns
Driver 1, 2 Lower Drive Fall Time	t_{GF_DN}	C_{OUT} = 1000pF		10		ns
Driver 1, 2 Dead Time	t_{D_LU}	C_{OUT} = 1000pF, LG falling edge 1V to UG rising edge 1V		25		ns
Driver 1, 2 Dead Time	t_{D_UL}	C_{OUT} = 1000pF, UG falling edge 1V to LG rising edge 1V		23		ns
Overvoltage Protection						
Output OVP Threshold	V_{OVTH_OUT}		**112**	114	**116**	%
OV Pin Output Logic High	$V_{OV\text{-}OH}$	Load resistance 100k, VCC5V = 5V		4.9		V
OV Pin Output Logic Low	$V_{OV\text{-}OL}$	No load		0		V
OV Pin Input Logic High (Note 10)	$V_{OV\text{-}IH}$		**3.2**			V
OV Pin Input Logic Low (Note 10)	$V_{OV\text{-}IL}$				**1**	V
Overcurrent Protection						
LG2/OC_MODE Current Source	$I_{MODELG2}$		**7.5**	10	**13**	µA
LG2/OC_MODE Threshold Low	$V_{MODETHLOC}$		**0.26**			V
LG2/OC_MODE Threshold High	$V_{MODETHHOC}$				**0.34**	V
Pulse-by-Pulse Peak Current Limit Input Shunt Set Point	$V_{OCSET\text{-}CS}$	V_{CS+} - V_{CS-}, 12V common-mode voltage applied to CS± pins	**68**	82	**96**	mV
Hiccup Peak Current Limit Input Shunt Set Point	$V_{OCSET\text{-}CS\text{-}HIC}$	V_{CS+} - V_{CS-}		100		mV
Pulse-by-Pulse Negative Peak Current Limit Output Shunt Set Point	$V_{OCSET\text{-}ISEN}$	V_{ISEN+} - V_{ISEN-}, 12V common-mode voltage applied to ISEN± pins	**-70**	-59	**-44**	mV
Input Constant and Hiccup Current Limit Set Point	$V_{IMONINCC}$	IMON_IN Pin Voltage	**1.18**	1.2	**1.22**	V
Input Constant and Hiccup Current Limit Set Point at CS± Input	V_{AVOCP_CS}	V_{CS+} - V_{CS-}, 12V common-mode applied to CS± pins, R_{IMON_IN} = 40.2k, T_J = -40°C to +125°C	**42**	51	**63**	mV
		V_{CS+} - V_{CS-}, 12V common-mode applied to CS± pins, R_{IMON_IN} = 40.2k, T_J = -40°C to +85°C	**42**	51	**60**	mV
Output Constant and Hiccup Current Limit Set Point	$V_{IMONOUTCC}$	IMON_OUT Pin Voltage	**1.18**	1.2	**1.22**	V
Output Constant and Hiccup Current Limit Set Point at ISEN± Input	V_{AVOCP_ISEN}	V_{ISEN+} - V_{ISEN-}, 12V common-mode applied to ISEN± pins, R_{IMON_OUT} = 40.2k, T_J = -40°C to +125°C	**43**	51	**63**	mV
		V_{ISEN+} - V_{ISEN-}, 12V common-mode applied to ISEN± pins, R_{IMON_OUT} = 40.2k, T_J = -40°C to +85°C	**43**	51	**60**	mV
Hiccup OCP Off-Time	t_{HICC_OFF}			50		ms

Recommended operating conditions unless otherwise noted. See Block Diagram and Typical Application Schematics. V_{IN} = 4.5V to 80V, or V_{DD} = 8V ±10%, C_VCC5V = 4.7µF, T_A = -40°C to +125°C, Typical values are at T_A = +25°C, unless otherwise specified. **Boldface limits apply across the operating temperature range, -40°C to +125°C. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 6)	Typ	Max (Note 6)	Unit
Over-Temperature						
Over-Temperature Shutdown	T_{OT-TH}			160		°C
Over-Temperature Hysteresis	T_{OT-HYS}			20		°C

Notes:

6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
7. This is the total shutdown current with V_{IN} = 5.6V and 80V.
8. Operating current is the supply current consumed when the device is active but not switching. It does not include gate drive current.
9. When soft-start time is less than 4.5ms, t_{PGR} increases. With internal soft-start (the fastest soft-start time), t_{PGR} increases close to its max limit 5ms.
10. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.
11. Threshold voltage at the PHASE1 pin for turning off the buck bottom MOSFET during DE mode.
12. Threshold voltage between the CS+ and CS- pins for turning off the boost top MOSFET during DE mode.

4. Typical Performance Graphs

Oscilloscope plots are taken using the ISL81801EVAL1Z evaluation board, V_{IN} = 9V to 80V, V_{OUT} = 12V, I_{OUT} = 10A, unless otherwise noted.

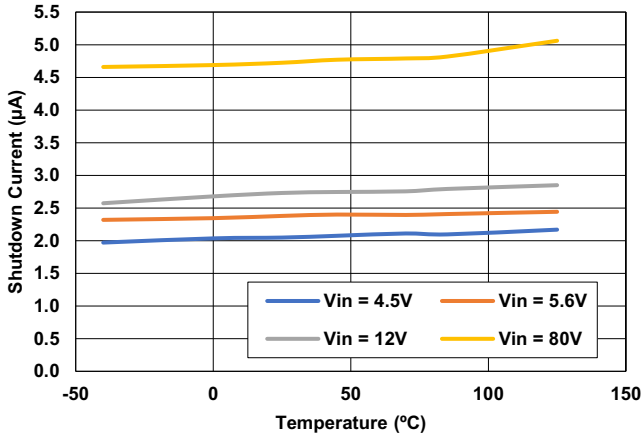


Figure 7. Shutdown Current vs Temperature

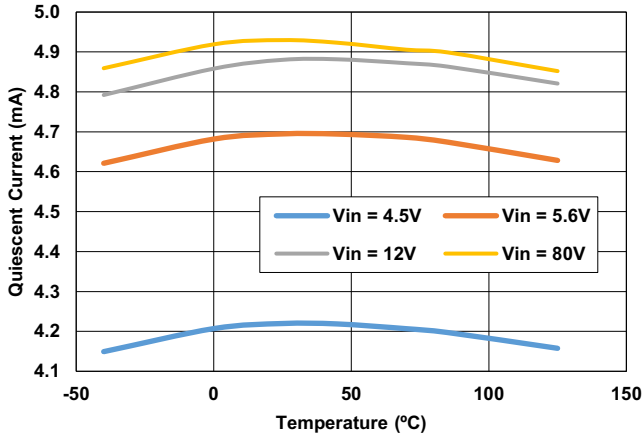


Figure 8. Quiescent Current vs Temperature

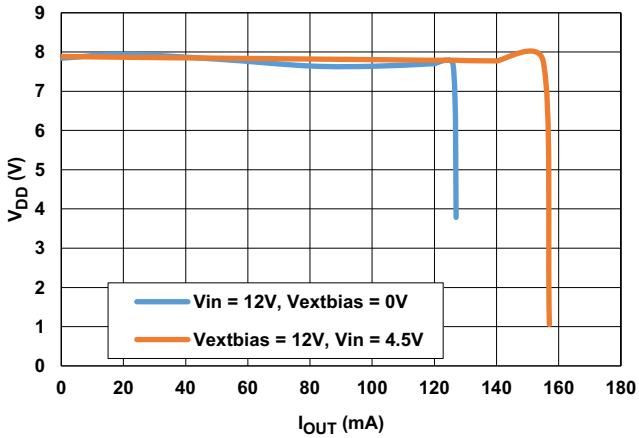


Figure 9. V_{DD} Load Regulation at 12V Input

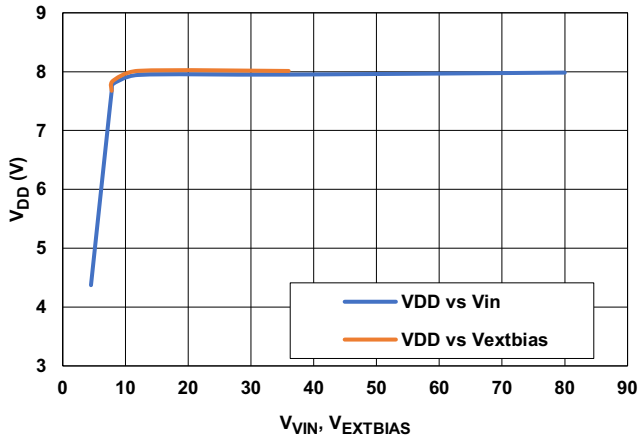


Figure 10. V_{DD} Line Regulation at 20mA Load

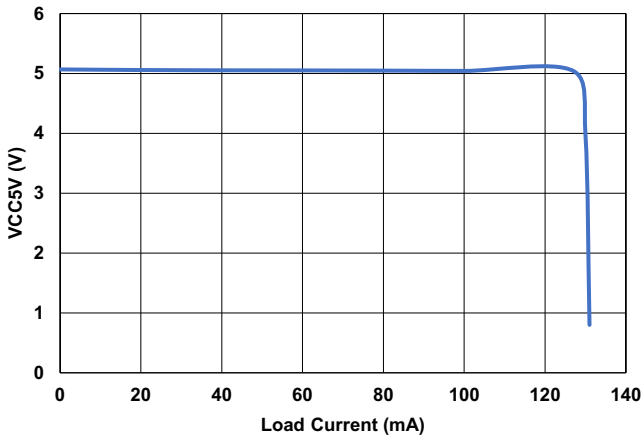


Figure 11. VCC5V Load Regulation at $12V_{IN}$

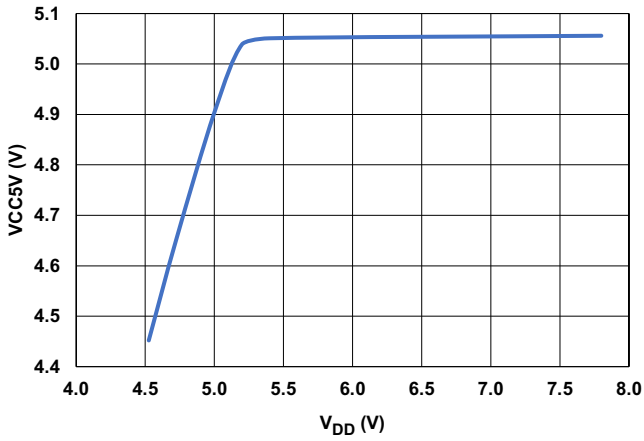


Figure 12. VCC5V Line Regulation at 20mA Load

Oscilloscope plots are taken using the ISL81801EVAL1Z evaluation board, V_{IN} = 9V to 80V, V_{OUT} = 12V, I_{OUT} = 10A, unless otherwise noted.

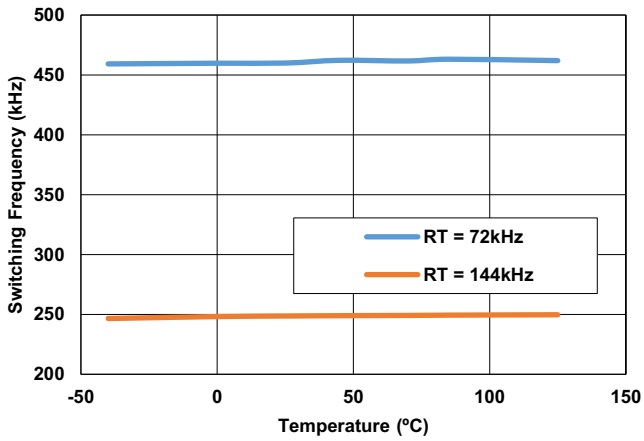


Figure 13. Switching Frequency vs Temperature

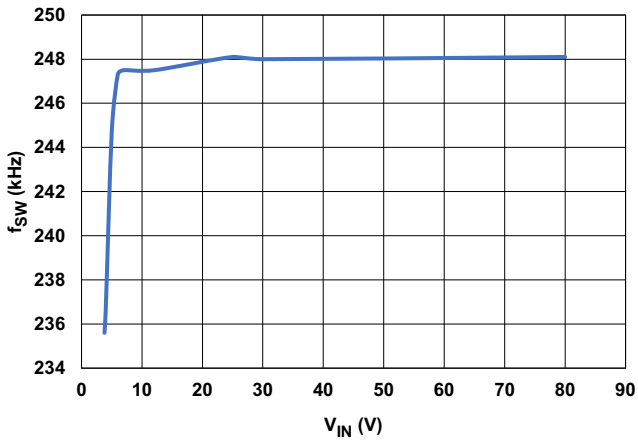


Figure 14. Switching Frequency vs V_{IN}, R_T = 144k

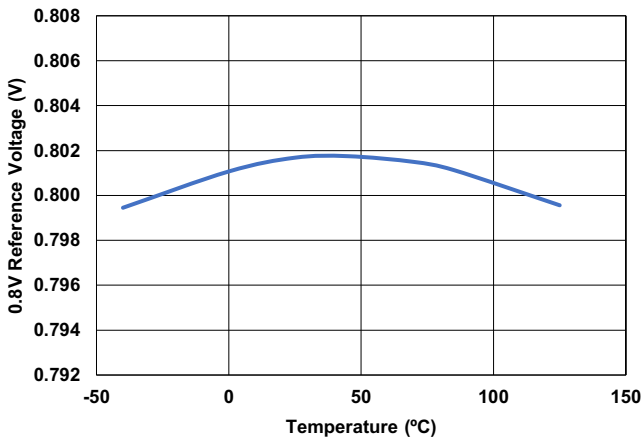


Figure 15. 0.8V Reference Voltage vs Temperature

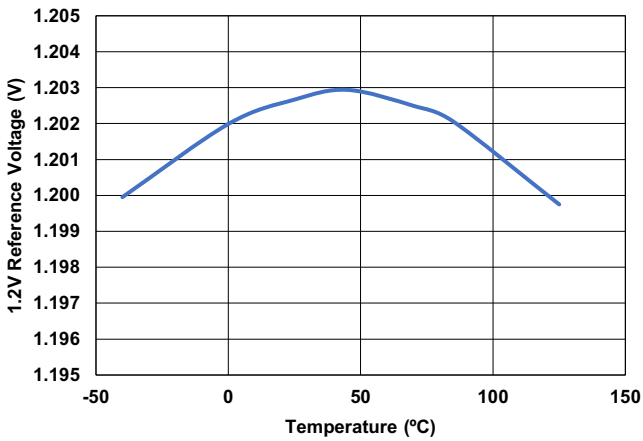


Figure 16. 1.2V Reference Voltage vs Temperature

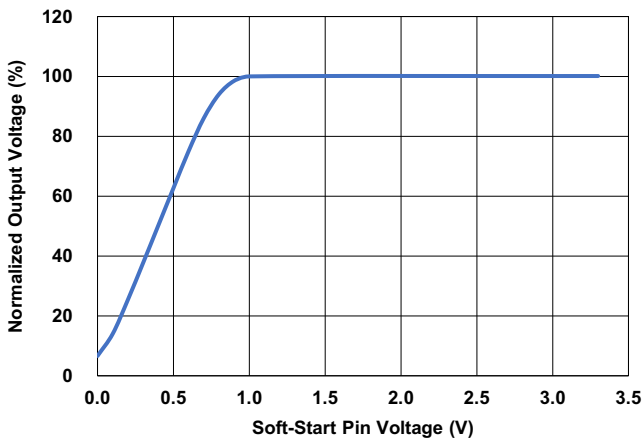


Figure 17. Normalized Output Voltage vs Voltage on Soft-Start Pin

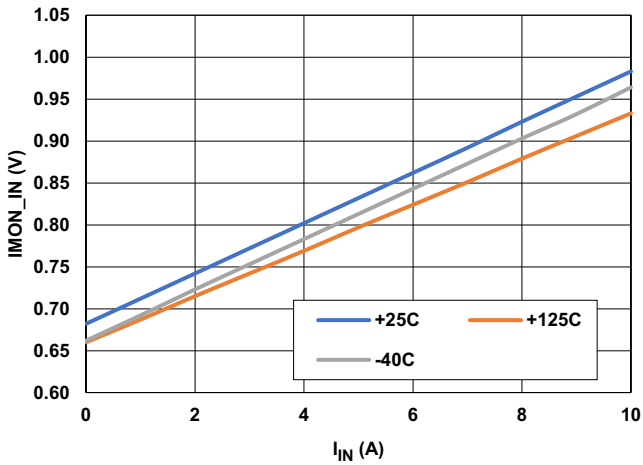


Figure 18. Input Current I_{IN} (DC) vs IMON_IN Pin Voltage, R_{S_IN} = 4mΩ, R_{IM_IN} = 36k

Oscilloscope plots are taken using the ISL81801EVAL1Z evaluation board, V_{IN} = 9V to 80V, V_{OUT} = 12V, I_{OUT} = 10A, unless otherwise noted.

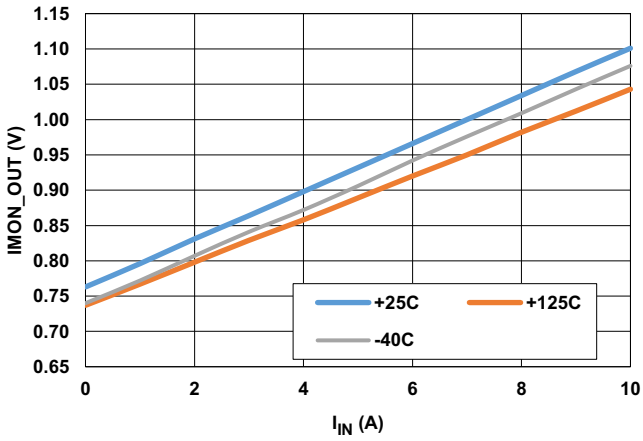


Figure 19. Output Current I_{OUT} (DC) vs IMON_OUT Pin Voltage, R_{S_OUT} = 4mΩ, R_{IM_OUT} = 40.2k

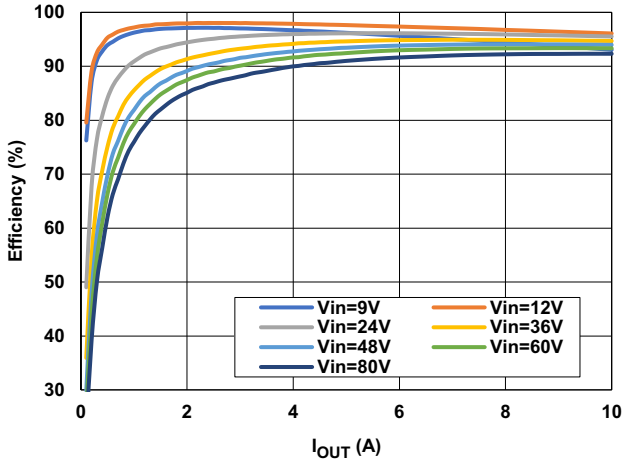


Figure 20. CCM Mode Efficiency

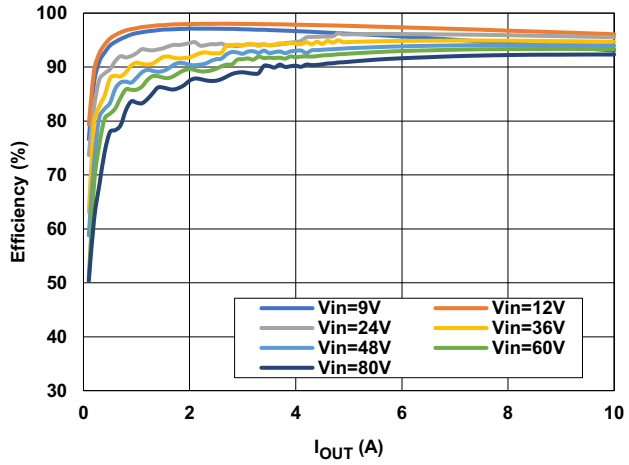


Figure 21. DE Mode Efficiency

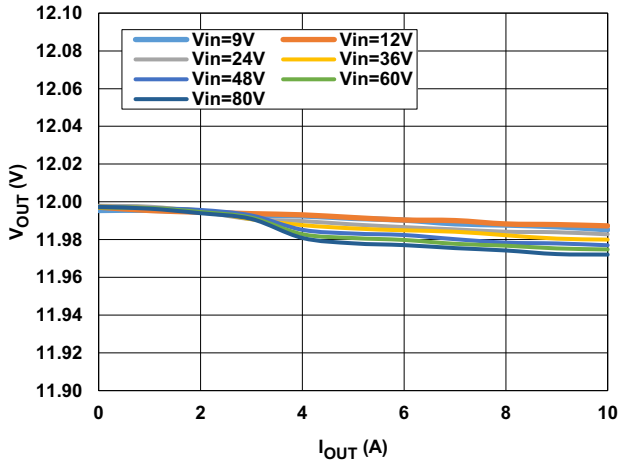


Figure 22. CCM Load Regulation at +25°C

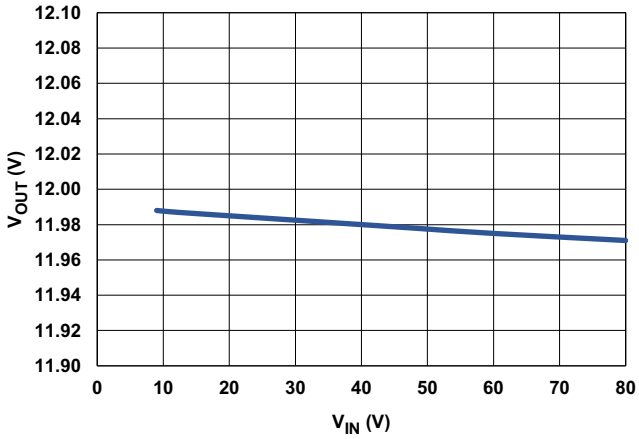


Figure 23. CCM Line Regulation at 10A Load +25°C

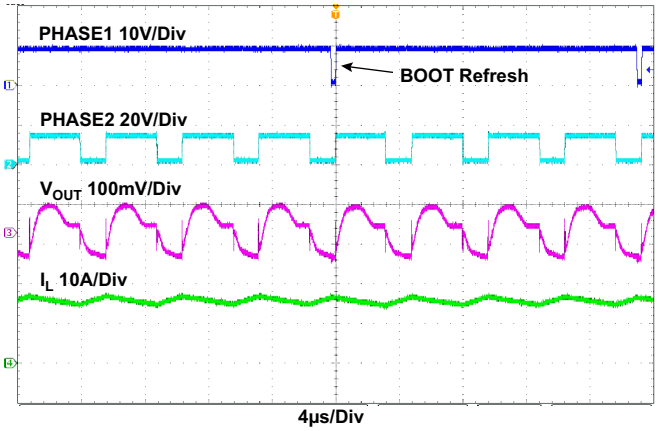


Figure 24. Boost Mode Waveforms, V_{IN} = 9V, I_{OUT} = 10A, CCM Mode

Oscilloscope plots are taken using the ISL81801EVAL1Z evaluation board, V_{IN} = 9V to 80V, V_{OUT} = 12V, I_{OUT} = 10A, unless otherwise noted.

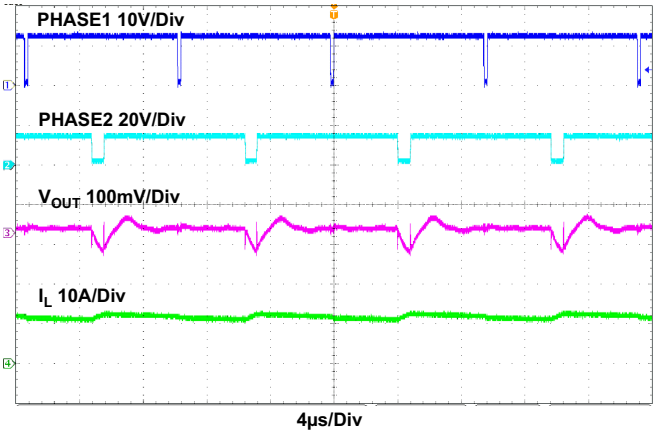


Figure 25. Buck-Boost Mode Waveforms, V_{IN} = 12V, I_{OUT} = 10A, CCM Mode

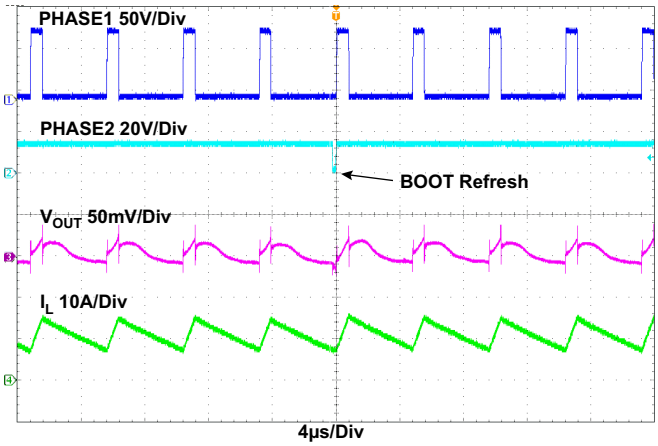


Figure 26. Buck Mode Waveforms, V_{IN} = 80V, I_{OUT} = 10A, CCM Mode

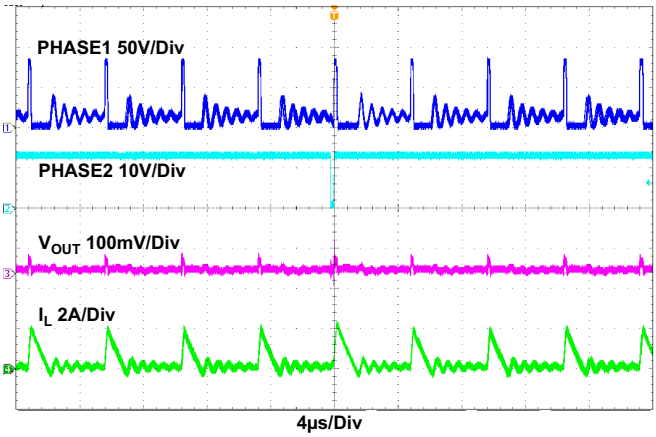


Figure 27. DE Mode Waveforms, V_{IN} = 80V, I_{OUT} = 0.2A

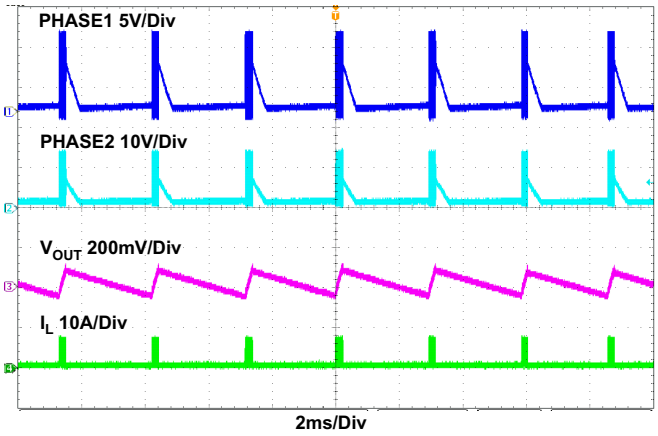


Figure 28. Burst Mode Waveforms, V_{IN} = 9V, I_{OUT} = 0.1A

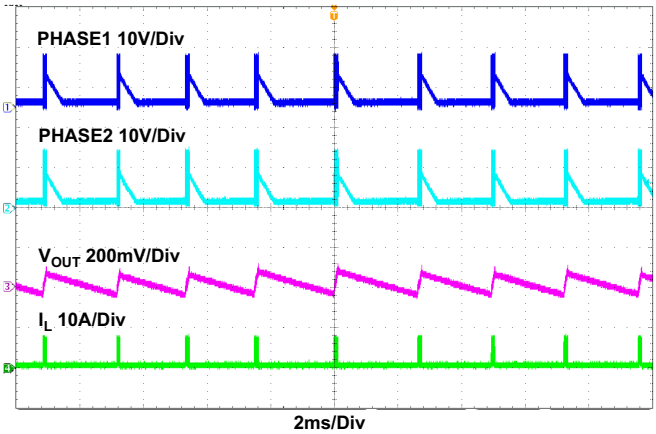


Figure 29. Burst Mode Waveforms, V_{IN} = 12V, I_{OUT} = 0.1A

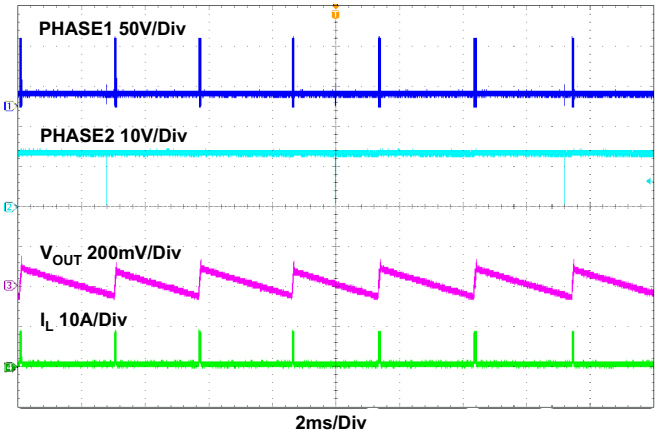


Figure 30. Burst Mode Waveforms, V_{IN} = 80V, I_{OUT} = 0.1A

Oscilloscope plots are taken using the ISL81801EVAL1Z evaluation board, V_{IN} = 9V to 80V, V_{OUT} = 12V, I_{OUT} = 10A, unless otherwise noted.

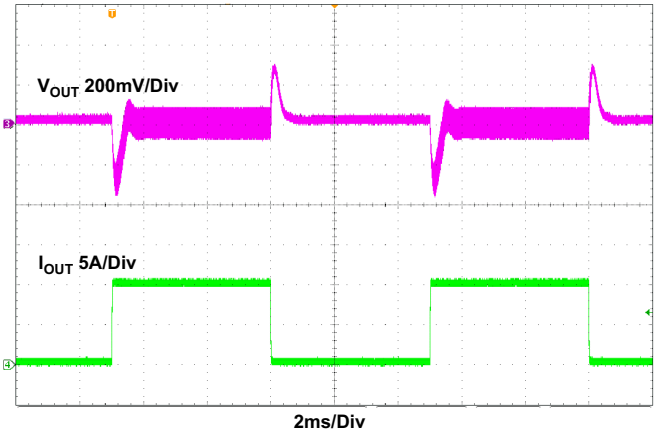


Figure 31. Load Transient, V_{IN} = 9V, I_{OUT} = 0A to 10A, 2.5A/µs, CCM

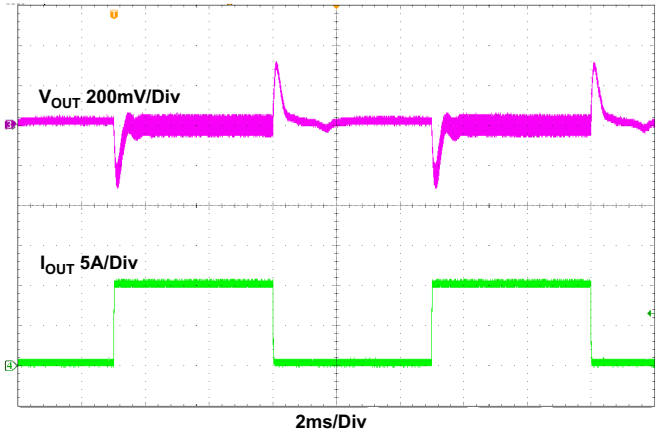


Figure 32. Load Transient, V_{IN} = 12V, I_{OUT} = 0A to 10A, 2.5A/µs, CCM

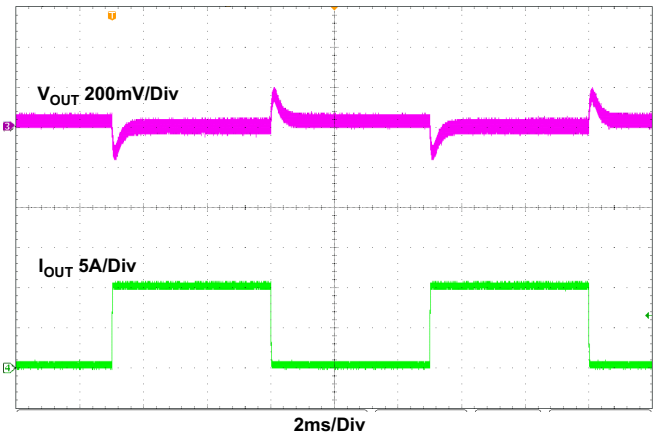


Figure 33. Load Transient, V_{IN} = 80V I_{OUT} = 0A to 10A, 2.5A/µs, CCM

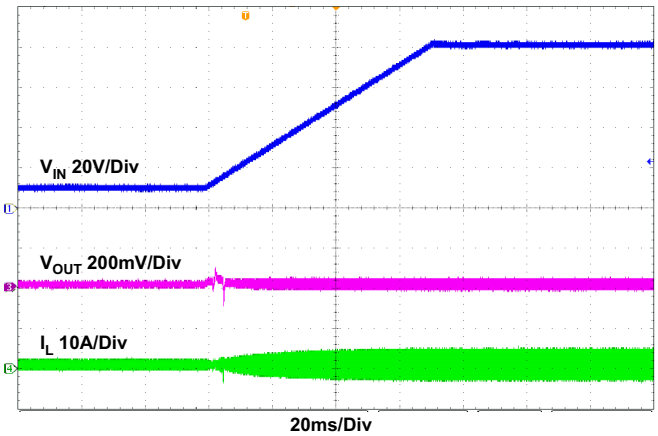


Figure 34. Line Transient, V_{IN} = 9V to 80V, 1V/ms, I_{OUT} = 0A

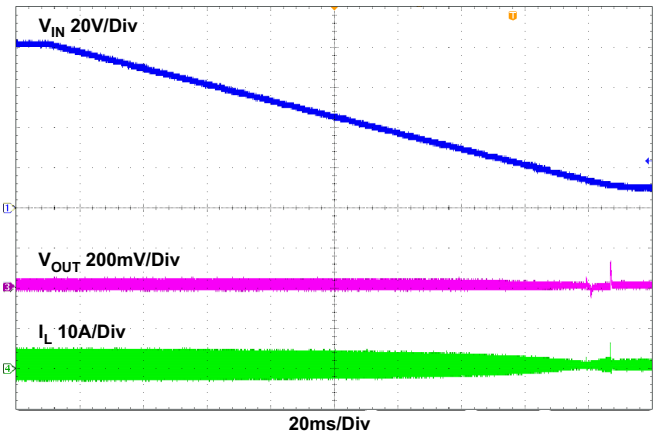


Figure 35. Line Transient, V_{IN} = 80V to 9V, 1V/ms, I_{OUT} = 0A

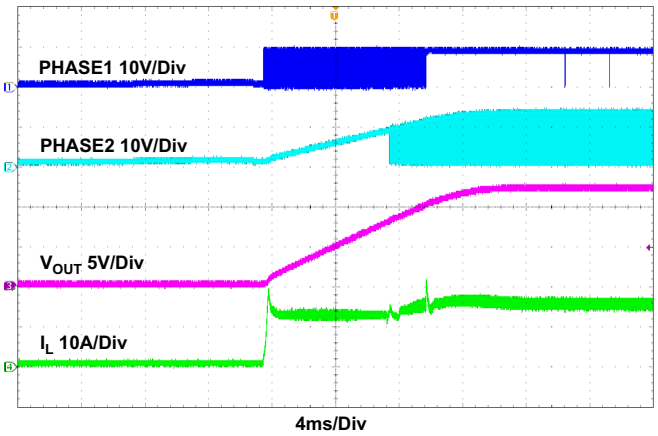


Figure 36. Start-Up Waveform, V_{IN} = 9V I_O = 10A CCM

Oscilloscope plots are taken using the ISL81801EVAL1Z evaluation board, V_{IN} = 9V to 80V, V_{OUT} = 12V, I_{OUT} = 10A, unless otherwise noted.

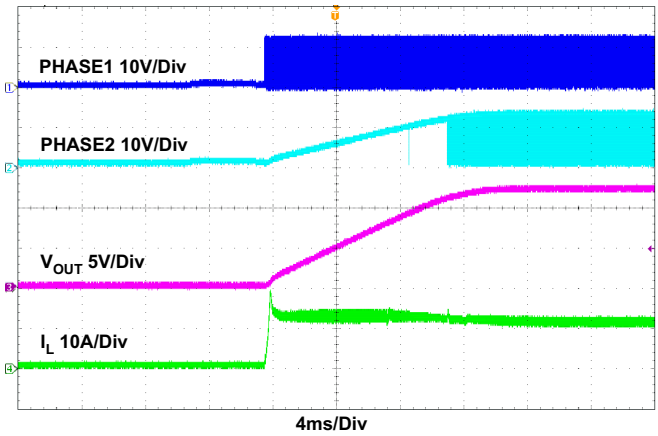


Figure 37. Start-Up Waveform, V_{IN} = 12V I_O = 10A, CCM

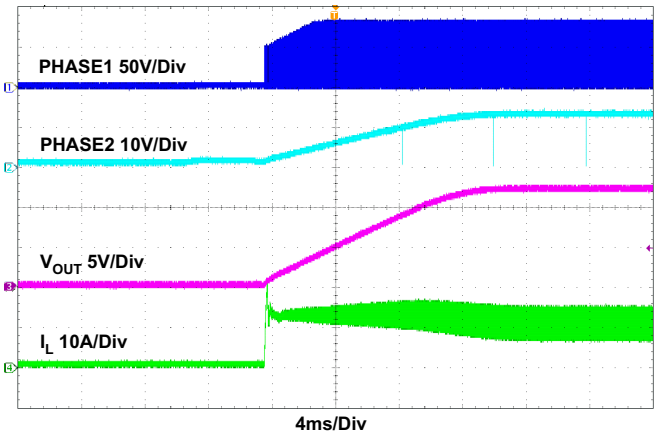


Figure 38. Start-Up Waveform, V_{IN} = 80V I_O = 10A, CCM

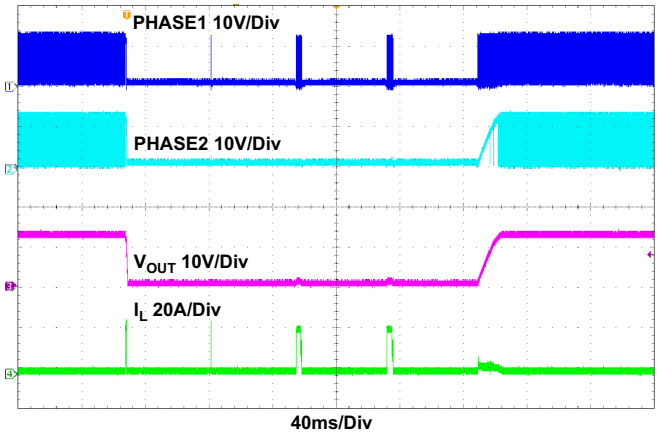


Figure 39. OCP Response, Output Short-Circuited from No Load to Ground and Released, CCM Mode, V_{IN} = 12V

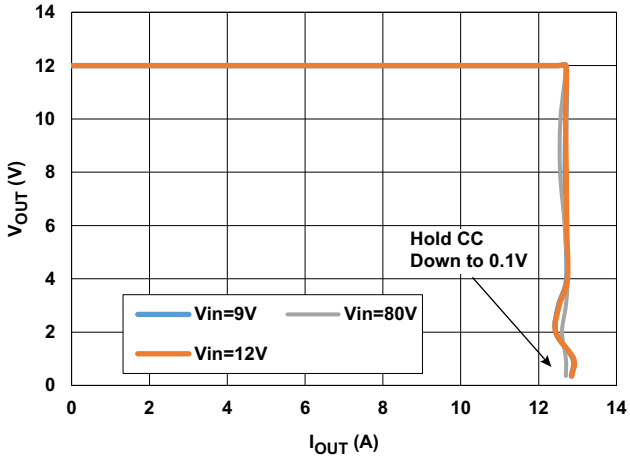


Figure 40. Constant Voltage (CV) and Constant Current (CC) Operation

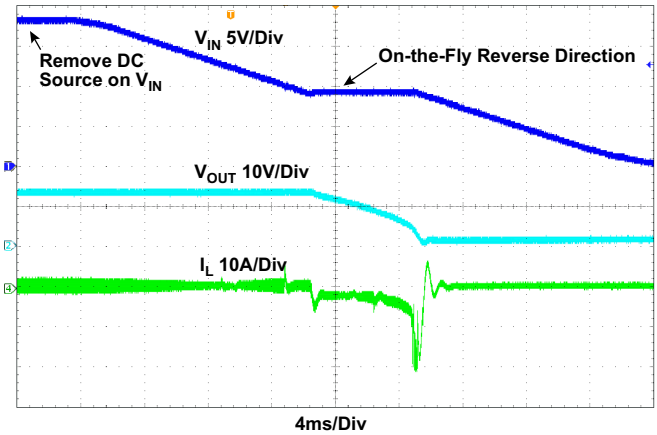


Figure 41. Bidirectional Operation
V_{IN} = 18V, V_{IN} Regulation at 9V, Remove V_{IN} DC Source with 1A Load Applied on Input Terminals

5. Functional Description

5.1 General Description

The ISL81801 implements complete buck-boost switching control with a PWM controller, internal drivers, references, protection circuitry, current and voltage control inputs, and monitor outputs. See Figure 6.

The ISL81801 is a current-mode controller. It uses a proprietary control algorithm to automatically switch between Buck and Boost modes as necessary to maintain a steady output voltage with changing input voltages and dynamic external loads. The controller integrates four control loops to regulate not only V_{OUT} but also average I_{OUT} and I_{IN} for constant current control and V_{IN} for reverse direction control.

The driver and protection circuits are also integrated to simplify the end design.

The part has an independent enable/disable control line (EN/UVLO pin), which provides flexible power-up sequencing and a simple V_{IN} UVP implementation. The soft-start time is programmable by adjusting the soft-start capacitor on the SS/TRK pin.

5.2 Internal 8V Linear Regulator (VDD), External Bias Supply (EXTBIAS), and 5V Linear Regulator (VCC5V)

The ISL81801 provides two input pins, VIN and EXTBIAS, and two internal LDOs for the VDD gate driver supply. A third LDO generates VCC5V from VDD. VCC5V provides power to all internal functional circuits other than the gate drivers. Bypass the linear regulator outputs (VDD) with a 10µF capacitor to the power ground. Also, bypass the third linear regulator output (VCC5V) with a 10µF capacitor to the signal ground. VCC5V is monitored by a power-on-reset circuit, which disables all regulators when VCC5V falls below 3.5V.

Both LDOs from VIN and EXTBIAS can source over 75mA for VDD to power the buck and boost gate drivers. When driving large FETs at a high switching frequency, little or no regulator current may be available for external loads. The LDO from VDD to VCC5V can also source over 75mA to supply the IC internal circuit. Although the current consumed by the internal circuit is low, the current supplied by VCC5V to the external loads is limited by VDD. For example, a single large FET with 15nC total gate charge requires 15nC x 300kHz = 4.5mA (15nC x 600kHz = 9mA).

Also, at higher input voltages with larger FETs, the power dissipation across the internal 8V LDO increases. Excessive power dissipation across this regulator must be avoided to prevent junction temperature rise. Thermal protection is triggered if the die temperature increases above +160°C because excessive power dissipation.

When large MOSFETs or high input voltages are used, an external 8V bias voltage is applied to the EXTBIAS pin to alleviate excessive power dissipation. When the voltage at the EXTBIAS pin is higher than typical 7.38V, the LDO from EXTBIAS activates and the LDO from VIN is disconnected. The recommended maximum voltage at the EXTBIAS pin is 36V. For applications with V_{OUT} significantly lower than V_{IN}, EXTBIAS is usually back biased by V_{OUT} to reduce the LDO power loss. EXTBIAS is allowed to activate only after soft-start is finished to avoid early activation during the V_{OUT} rising stage. An external UVLO circuit might be necessary to ensure smooth soft-starting. Renesas recommends adding a 10µF capacitor on the EXTBIAS pin and using a diode to connect the EXTBIAS pin to V_{OUT} to prevent the EXTBIAS pin voltage from being pulled low because a V_{OUT} short-circuit condition.

The two VDD LDOs have an overcurrent limit for short-circuit protection. The VIN to VDD LDO current limit is set to typical 120mA. The EXTBIAS to VDD LDO current limit is set to a typical 160mA.

5.3 Enable (EN/UVLO) and Soft-Start Operation

Pulling the EN/UVLO pin high or low can enable or disable the controller. The EN/UVLO pin has an internal 5.6V voltage clamp that allows this pin to be connected through a resistor to a higher voltage, provided that the maximum current into the EN/UVLO pin does not exceed 100µA. When the EN/UVLO pin voltage is higher than 1.3V, the three LDOs are enabled. After the VCC5V reaches the POR threshold, the controller is powered up to initialize its internal circuit. When EN/UVLO is higher than the 1.8V accurate undervoltage-lockout (UVLO) threshold, the ISL81801 soft-start circuitry becomes active. An internal 2µA current source begins charging up the soft-start capacitor connected from the SS/TRK pin to GND. The voltage on the SS/TRK pin acts as the reference

for the voltage error amplifier during soft-start, until it reaches 0.8V. The output voltage thus rises from 0V to regulation as SS/TRK rises from 0V to 0.8V. Charging of the soft-start capacitor continues until the voltage on the SS/TRK pin reaches 3V.

Typical applications for ISL81801 use programmable analog soft-start or the SS/TRK pin for tracking. The soft-start time is set by the value of the soft-start capacitor connected from SS/TRK to GND. Inrush current during start-up is alleviated by adjusting the soft-starting time.

The typical soft-start time is set according to Equation 2:

(EQ. 2) $$t_{SS} = 0.8V\left(\frac{C_{SS}}{2\mu A}\right)$$

When the soft-start time set by external C_{SS} or tracking is less than 1.7ms, an internal soft-start circuit of 1.7ms takes over the soft-start.

PGOOD toggles to high when the output voltage is in regulation.

Pulling the EN/UVLO lower than the EN falling threshold, V_{ENSS_THF} typical 0.9V, disables the PWM output and internal LDOs to achieve low standby current. The SS/TRK pin is also discharged to GND by an internal MOSFET with 70Ω $r_{DS(ON)}$. For applications with a larger than 1µF capacitor on the SS/TRK pin, Renesas recommends adding a 100Ω to 1kΩ resistor in series with the capacitor to share the power loss at the discharge.

With use of the accurate UVLO threshold, an accurate V_{IN} Undervoltage Protection (UVP) feature is implemented by feeding the V_{IN} into the EN/UVLO pin using a voltage divider, R_{UV1} and R_{UV2}, shown in Figure 42.

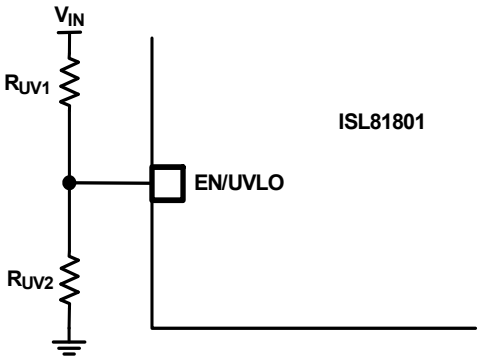


Figure 42. V_{IN} Undervoltage Protection

The V_{IN} UVP rising threshold is calculated using Equation 3.

(EQ. 3) $$V_{UVRISE} = \frac{V_{UVLO_THR}(R_{UV1} + R_{UV2}) - 1.1x10^{-6}\ R_{UV1}R_{UV2}}{R_{UV2}}$$

where V_{UVLO_THR} is the EN/UVLO pin UVLO rising threshold, typically 1.8V.

The V_{IN} UVP falling threshold is calculated using Equation 4.

(EQ. 4) $$V_{UVFALL} = \frac{V_{UVLO_THR}(R_{UV1} + R_{UV2}) - I_{UVLO_HYST}\ R_{UV1}R_{UV2}}{R_{UV2}}$$

where I_{UVLO_HYST} is the UVLO hysteresis current, typically 4.2µA.

5.4 Tracking Operation

The ISL81801 can track an external supply. To implement tracking, connect a resistive divider between the external supply output and ground. Connect the center point of the divider to the SS/TRK pin of the ISL81801. The resistive divider ratio sets the ramping ratio between the two voltage rails. To implement coincident tracking, set the tracking

resistive divider ratio the same as the ISL81801 output-resistive divider given by Equation 5. Make sure that the voltage at SS/TRK is greater than 0.8V when the master rail reaches regulation.

To minimize the impact of the 2µA soft-start current on the tracking function, Renesas recommends using resistors less than 10kΩ for the tracking resistive divider.

When the SS/TRK pin voltage is pulled down to less than 0.3V by the external tracking source, the prebias startup DE mode function is enabled again. The output voltage may not be able to be pull down if the load current is not high enough.

When Overcurrent Protection (OCP) is triggered, the internal minimum soft-start circuit determines the 50ms OCP soft-start hiccup off-time.

5.5 Control Loops

The ISL81801 is a current-mode controller that can provide an output voltage above, equal to, or below the input voltage. The Renesas proprietary control architecture uses a current sense resistor in series with the buck upper FET to sense the inductor current in Buck or Boost mode (see Figure 1 (Typical Application circuit) and Figure 6 (Block Diagram)). The inductor current is controlled by the voltage on the COMP pin, which is the lowest output of the error amplifiers Gm1 - Gm4. As the simplest example, when the output is regulated to a constant voltage, the FB_OUT pin receives the output feedback signal, which is compared to the internal reference by Gm1. Lower output voltage creates higher COMP voltage that leads to a higher PWM duty cycle to deliver more current to the output. Conversely, higher output voltage creates lower COMP voltage that leads to a lower PWM duty cycle to reduce the current delivered to the output.

The ISL81801 has four error amplifiers (Gm1-4) that can control output voltage (Gm1), input voltage (Gm2), input current (Gm3), and output current (Gm4). In a typical application, the output voltage is regulated by Gm1, and the remaining error amplifiers are monitoring for excessive input or output current or an input undervoltage condition. In other applications, such as a battery charger, the output current regulator (Gm4) implements constant current charging until a predetermined voltage is reached at which point the output voltage regulator (Gm1) takes control.

5.5.1 Output Voltage Regulation Loop

The ISL81801 provides a precision 0.8V internal reference voltage to set the output voltage. Based on this internal reference, the output voltage is set from 0.8V up to a level determined by the feedback voltage divider, as shown in Figure 43.

A resistive divider from the output to ground sets the output voltage. Connect the center point of the divider to the FB_OUT pin. The output voltage value is determined by Equation 5.

(EQ. 5) $$V_{OUT} = 0.8V\left(\frac{R_{FBO1} + R_{FBO2}}{R_{FBO2}}\right)$$

where R_{FBO1} is the top resistor of the feedback divider network and R_{FBO2} is the bottom resistor connected from FB_OUT to ground, shown in Figure 43.

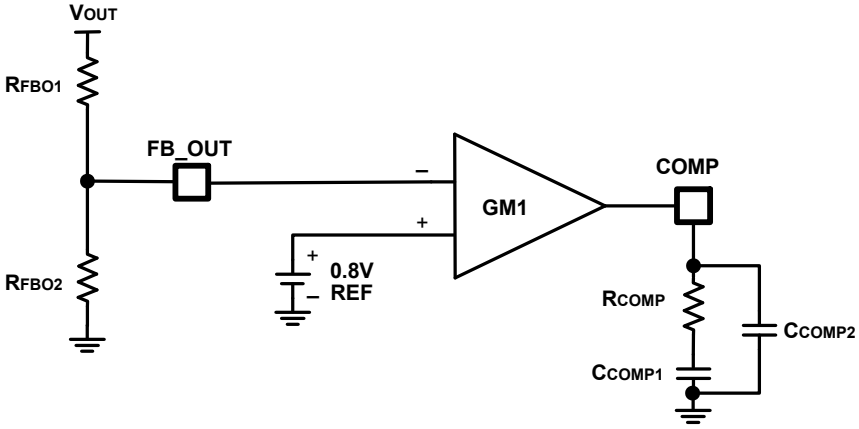


Figure 43. Output Voltage Regulator

As shown in Figure 43, the R_{COMP}, C_{COMP1}, and C_{COMP2} network connected on the Gm1 regulator output COMP pin is needed to compensate the loop for stable operation. The loop stability is affected by many different factors such as V_{IN}, V_{OUT}, load current, switching frequency, inductor value, output capacitance and the compensation network on COMP pin. For most applications, 22nF is a good value for C_{COMP1}. A larger C_{COMP1} makes the loop more stable by giving a larger phase margin, but the loop bandwidth is lower. C_{COMP2} is typically 1/10th to 1/30th of C_{COMP1} to filter high frequency noise. A good starting value for R_{COMP} is 10k. Lower R_{COMP} improves stability but slows the loop response. Optimize the final compensation network with a bench test.

5.5.2 Input Voltage Regulation Loop

As shown in Figure 44, the input voltage V_{IN} is sensed by the FB_IN pin using a resistor divider R_{FBIN1}/R_{FBIN2} and regulated by Gm2. When the FB_IN pin voltage falls below the 0.8V reference voltage, the COMP pin voltage is pulled low to reduce the PWM duty cycle and thus the input current. For applications with a high input source impedance, such as a solar panel, the input voltage regulation loop can prevent the input voltage from being pulled too low in high output load conditions. For applications with a low input source impedance, such as batteries, the V_{IN} feedback loop can prevent the battery from being over-discharged. For DC back-up system applications, with loads on the VIN supply side and a backup battery or super capacitor on the output side, the input voltage regulation loop can reverse the power conversion direction and draw energy from the output side to regulate the VIN voltage. The regulated input voltage value is determined by Equation 6.

(EQ. 6) $$V_{IN} = 0.8V\left(\frac{R_{FBIN1} + R_{FBIN2}}{R_{FBIN2}}\right)$$

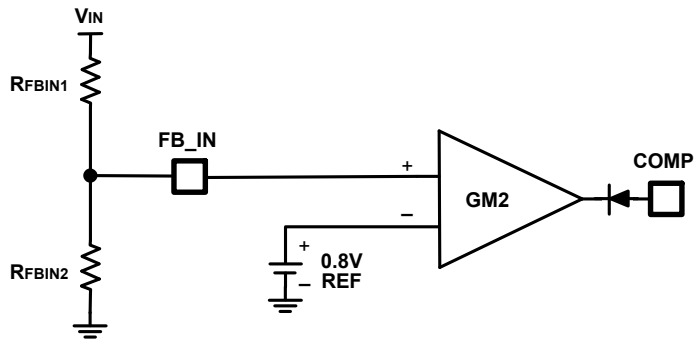


Figure 44. V_{IN} Feedback Loop

FB_IN is a dual-function pin. It also sets the phase angle of the clock output signal on the CLKOUT/DITHER pin, shown in Table 2. The V_{IN} feedback loop is disabled when the FB_IN pin voltage is below 0.3V or above 4.7V. The V_{IN} feedback loop is also disabled in DE mode and during soft-start.

5.5.3 Input and Output Average Current Monitoring and Regulation Loops

As shown in Figure 45, the ISL81801 has two current sense amplifiers, A1 and A2, which monitor both input and output current. The voltage signals on the input and output current sense resistor R_{S_IN} and R_{S_OUT} are sent to the differential inputs of CS+/CS- and ISEN+/ISEN-, respectively, after the RC filters R_{S_IN1}/C_{S_IN1}, R_{S_IN2}/C_{S_IN2}, R_{S_OUT1}/C_{S_OUT1}, and R_{S_OUT2}/C_{S_OUT2}. Renesas recommends using a 1Ω value for R_{S_IN1}, R_{S_IN2}, R_{S_OUT1}, and R_{S_OUT2}, and a 10nF value for C_{S_IN1}, C_{S_IN2}, C_{S_OUT1}, and C_{S_OUT2} to effectively damp the switching noise without delaying the current signal or introducing significant error because input bias current. The A1 and A2 amplifiers convert the current sense voltage signals to current signals I_{CS} and I_{ISEN}.

(EQ. 7) $$I_{CS} = [(I_{IN})R_{S_IN} + V_{CSOFFSET}]Gm_{CS}$$

where:

- I_{IN} is the input current in Q_1 drain
- $V_{CSOFFSET}$ is the A1 input offset voltage
- Gm_{CS} is the gain of A1, typical 200µS
- $V_{CSOFFSET}\ Gm_{CS} = I_{CSOFFSET}$

The typical value of $I_{CSOFFSET}$ is 19.5µA, then $V_{CSOFFSET}$ is 97.5mV.

(EQ. 8) $$I_{ISEN} = [(I_{OUT})R_{S_OUT} + V_{ISENOFFSET}]Gm_{ISEN}$$

where:

- I_{OUT} is the output current in Q_4 drain
- $V_{ISENOFFSET}$ is the A2 input offset voltage
- Gm_{ISEN} is the gain of A2, typical 200µS
- $V_{ISENOFFSET}\ Gm_{ISEN} = I_{ISENOFFSET}$.

The typical value of $I_{ISENOFFSET}$ is 20µA, then $V_{ISENOFFSET}$ is 100mV.

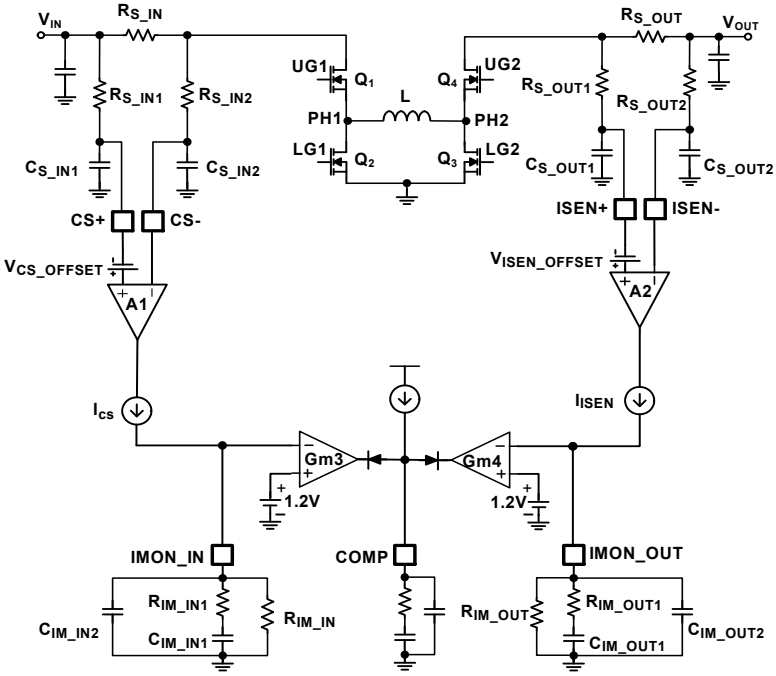


Figure 45. Input and Output Average Current Monitoring and Regulation Loops

By connecting resistor R_{IM_IN} and R_{IM_OUT} on the IMON_IN and IMON_OUT pins, the I_{CS} and I_{ISEN} current signals are transferred to voltage signals. The RC networks on the IMON_IN and IMON_OUT pins

$R_{IM_IN1}/C_{IM_IN1}/C_{IM_IN2}$ and $R_{IM_OUT1}/C_{IM_OUT1}/C_{IM_OUT2}$ are needed to remove the AC content in the I_{CS} and I_{ISEN} signals and ensure stable loop operation. The average voltages at the IMON_IN and IMON_OUT pins are regulated to 1.2V by Gm3 and Gm4 for constant input and output current control.

The input constant current loop set point I_{INCC} is calculated using Equation 9. See V_{AVOCP_CS} in the Electrical Specifications table to estimate the set point tolerance.

(EQ. 9) $$I_{INCC} = \frac{1.2 - I_{CSOFFSET} x R_{IM_IN}}{R_{IM_IN} x R_{S_IN} x Gm_{CS}}$$

The output constant current loop set point I_{OUTCC} is calculated using Equation 10. See V_{AVOCP_ISEN} in the Electrical Specifications table to estimate the set point tolerance.

(EQ. 10) $$I_{OUTCC} = \frac{1.2 - I_{ISENOFFSET} x R_{IM_OUT}}{R_{IM_OUT} x R_{S_OUT} x Gm_{ISEN}}$$

The following is an example for output current accuracy calculation based on the V_{AVOCP_ISEN} value in the T_J = -40°C to +125°C condition.

With R_{IM_OUT} = 40.2k and R_{S_OUT} = 5mΩ, $I_{OUTCC(TYP)}$ = 51mV/R_{S_OUT} = 10.2A, $I_{OUTCC(MIN)}$ = 43mV/R_{S_OUT} = 8.6A, $I_{OUTCC(MAX)}$ = 63mV/R_{S_OUT} = 12.6A. Therefore, the output current accuracy would be in the range of (-15.68% ~ +23.52%) in this condition.

Similar to the voltage control loops, the average current loop stability is affected by many different factors such as V_{IN}, V_{OUT}, switching frequency, inductor value, output and input capacitance, and the RC network on the IMON_IN or IMON_OUT pin. Because the high AC content in I_{CS} and I_{ISEN}, large C_{IM_IN1} and C_{IM_OUT1} are needed. Larger C_{IM_IN1} and C_{IM_OUT1} can also make the loop more stable by giving a larger phase margin, but the loop bandwidth is lower. For most applications 47nF is a good value for C_{IM_IN1} and C_{IM_OUT1}. C_{IM_IN2} and C_{IM_OUT2} are typically 1/10th to 1/30th of C_{IM_IN1} and C_{IM_OUT1} to filter high frequency noise. R_{IM_IN1} and R_{IM_OUT1} are needed to boost the phase margin. A good starting value for R_{IM_IN1} and R_{IM_OUT1} is 5k. Optimize the final compensation network with iSim simulation and bench testing.

5.6 Buck-Boost Conversion Topology and Control Algorithm

The ISL81801 uses Renesas proprietary buck-boost control algorithm to achieve optimized power conversion performance. The buck-boost topology is shown in Figure 46. The ISL81801 controls the four power switches Q_1, Q_2, Q_3, and Q_4 to work in either Buck or Boost mode. When V_{IN} is far lower than V_{OUT}, the converter works in Boost mode. When V_{IN} is far higher than V_{OUT}, the converter works in Buck mode. When V_{IN} is equal or close to V_{OUT}, the converter alternates between Buck and Boost mode as necessary to provide a regulated output voltage, which is called Buck-Boost mode. Figure 47 shows the relationship between the operation modes and V_{OUT} - V_{IN}.

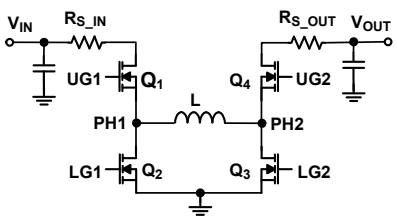


Figure 46. Buck-Boost Topology

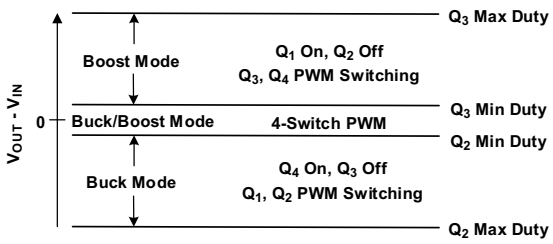


Figure 47. Operation Modes vs V_{OUT} - V_{IN}

R_{S_IN} is a current sense resistor to sense the inductor current during Q_1 on-time. As shown in the Block Diagram, the sensed signal is fed into the CS+ and CS- pins and used for peak or valley current-mode control, DE mode control, input average current monitor, constant current control, and protections.

R_{S_OUT} is a current sense resistor to sense the inductor current during Q_4 on-time. As shown in the Block Diagram, the sensed signal is fed into the ISEN+ and ISEN- pins and used for negative peak inductor current limit, output average current monitor, constant current control, and protections.

5.6.1 Buck Mode Operation ($V_{IN} > V_{OUT}$)

In Buck mode, Q_4 is always on and Q_3 is always off unless boot refresh or inductor negative peak current limit is tripped. Q_1 and Q_2 run in a normal peak current controlled sync buck operation mode. Q_1 turns on by the clock. During Q_1 on-time, the current sense amplifier (A1) senses the inductor current by the voltage on R_{S_IN}. Q_1 turns off when the sensed signal combined with the slope compensation ramp is higher than the COMP pin voltage, which is the error signal from the upper voltage or current regulator. The equivalent circuit and operation waveforms are shown in Figure 48.

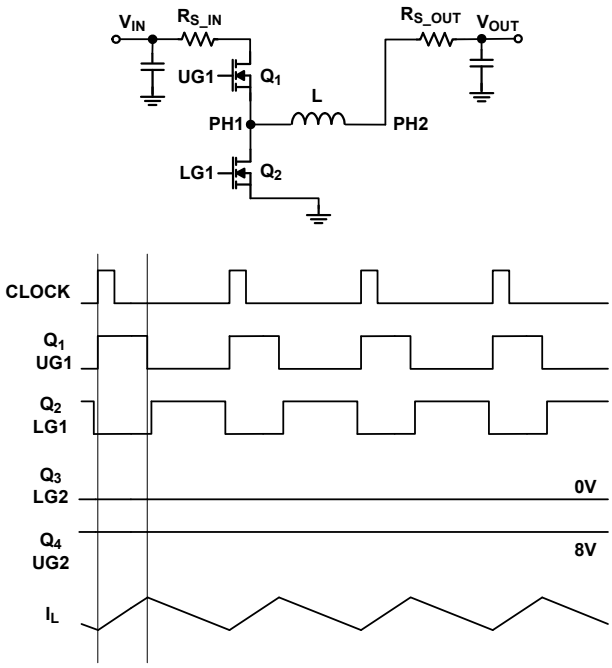


Figure 48. Buck Mode Equivalent Circuit and Operation Waveforms

In Buck mode, the Q_1 duty cycle is given by: $D_{Q1} = V_{OUT}/V_{IN} \times 100\%$.

As V_{IN} decreases to close to V_{OUT}, D_{Q1} increases to close to its maximum value decided by its minimum off-time. When D_{Q1} reaches its maximum value, the converter moves to Buck-Boost mode.

When V_{IN} is much higher than V_{OUT}, D_{Q1} decreases to close to its minimum duty cycle decided by its minimum on-time. To allow stable loop operation and avoid duty cycle jitter, Renesas recommends keeping the Q_1 on-time always two to three times higher than the minimum on-time.

5.6.2 Boost Mode Operation ($V_{IN} < V_{OUT}$)

In Boost mode, Q_1 is always on and Q_2 is always off unless boot refresh or inductor negative peak current limit is tripped. Q_3 and Q_4 run in a normal valley current controlled sync boost operation mode. Q_3 turns off by the clock. During Q_3 off-time, current sense amplifier A1 senses the inductor current by the voltage on R_{S_IN}. Q_3 turns on when the sensed signal combined with the slope compensation ramp is lower than the COMP pin voltage which is the error signal from the upper voltage or current regulator. The equivalent circuit and operation waveforms are shown in Figure 49.

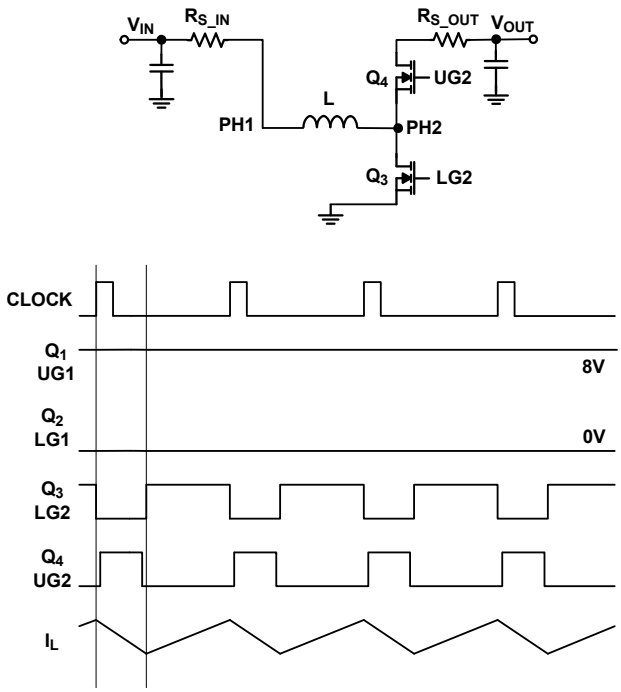


Figure 49. Boost Mode Equivalent Circuit and Operation Waveforms

In Boost mode, the Q_3 duty cycle is given by: $D_{Q3} = (1 - V_{IN}/V_{OUT}) \times 100\%$.

As V_{IN} increases close to V_{OUT}, D_{Q3} decreases close to its minimum value decided by its minimum on-time. When D_{Q3} reaches its minimum value, the converter moves to Buck-Boost mode.

When V_{IN} is much lower than V_{OUT}, D_{Q3} increases close to its maximum duty cycle decided by its minimum off-time. To allow stable loop operation and avoid duty cycle jitter, Renesas recommends keeping the Q_3 off-time always two to three times higher than the minimum off-time.

5.6.3 Buck-Boost Mode Operation ($V_{IN} \approx V_{OUT}$)

In Buck-Boost mode, the converter runs in one cycle of Buck mode followed by one cycle of Boost mode operation mode. It takes two clock cycles to finish a full buck-boost period.

When V_{IN} is higher than V_{OUT}, Q_3 runs in minimum duty in the Boost mode cycle. Q_1 duty cycle D_{Q1} is modulated in the buck cycle to keep V_{OUT} in regulation. As V_{IN} increases, D_{Q1} decreases. When D_{Q1} decreases to less than 66.7% of the clock period, the converter moves to Buck mode.

When V_{IN} is lower than V_{OUT}, Q_1 runs in maximum duty in the Buck mode cycle. Q_3 duty cycle D_{Q3} is modulated in the Boost mode cycle to keep V_{OUT} in regulation. As V_{IN} decreases, D_{Q3} increases. When D_{Q3} increases to more than 33.3% of the clock period, the converter moves to Boost mode.

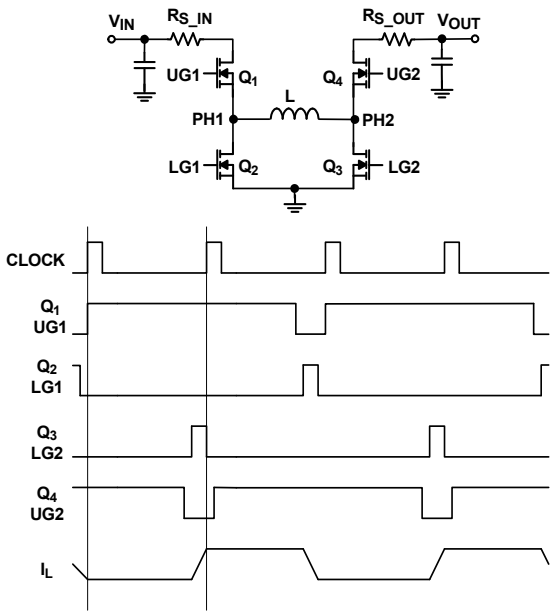


Figure 50. Buck-Boost Mode Equivalent Circuit and Operation Waveforms

5.7 Light-Load Efficiency Enhancement

The ISL81801 is set to DE and Burst mode to improve light load efficiency. The dual functional LG1/PWM_MODE pin sets the DE or PWM mode operation in the initialization period before soft-start. During the initialization period, a typical 10µA current source $I_{MODELG1}$ from the LG1/PWM_MODE pin creates a voltage drop on the resistor R_{LG1} connected between the LG1/PWM_MODE pin and GND. When the voltage is lower than typical 0.3V, PWM mode is set. Otherwise, DE mode is set. **Note**: DE or PWM mode can only be selected during the initialization period, and cannot be changed after initialization is complete.

To set for DE mode operation, select R_{LG1} to meet:

(EQ. 11) $$R_{LG1} x I_{MODELG1} > 0.34V$$

When DE mode is set, the buck sync FET driven by LG1 and the boost sync FET driven by UG2 are all running in DE mode. The inductor current is not allowed to reverse (discontinuous operation) depending on the zero cross detection reference level V_{CROSS1} for buck sync FET and V_{CROSS2} for boost sync FET. At light load conditions, the converter goes into diode emulation. When the load current is less than the level set by $V_{IMONOUTBSTEN}$ typical 0.85V on the IMON_OUT pin, the part enters Burst mode. Equation 12 sets the Burst mode operation enter condition.

(EQ. 12) $$R_{IM_OUT} x (I_{SENOFFSET} + I_{OUT} x R_{S_OUT} x Gm_{ISEN}) < V_{IMONOUTBSTEN}$$

where (see Figure 45):

$I_{SENOFFSET}$ is the output current sense op amp internal offset current, typical 20µA

Gm_{ISEN} is the output current sense op amp Gm, typical 200µS.

The part exits Burst mode when the output current increases to higher than the level set by $V_{IMONOUTBSTEX}$ typical 0.88V on the IMON_OUT pin. Equation 13 sets the Burst mode operation exit condition.

(EQ. 13) $$R_{IM_OUT} x (I_{SENOFFSET} + I_{OUT} x R_{S_OUT} x Gm_{ISEN}) > V_{IMONOUTBSTEX}$$

When the part enters Burst mode, the BSTEN pin goes low. To fully avoid any enter/exit chattering, a 4-10MΩ resistor is added between the BSTEN and IMON_OUT pins to further expand the hysteresis.

In Burst mode, an internal window comparator takes control of the output voltage. The comparator monitors the FB_OUT pin voltage. When the FB_OUT pin voltage is higher than 0.82V, the controller enters Low Power Off

mode. Some unneeded internal circuits are powered off to further reduce power dissipation. When the FB_OUT pin voltage drops to 0.8V, the controller wakes up and runs in a fixed level peak current controlled D/(1-D) Buck-Boost mode when V_{IN} - V_{OUT} < 2V and Buck mode when V_{IN} -V_{OUT} > 2V. In the D/(1-D) Buck-Boost mode, Q_1 and Q_3 conduct in D*T period, where D is the duty cycle and T is the switching period. Q_2 and Q_4 complimentary conduct in (1-D)*T period. Q_1 and Q_3 are turned on by the clock signal and turned off when inductor current rises to the level that the input current sense amplifier input voltage reaches V_{BST-CS}, typical 27mV. After Q_1 and Q_3 are turned off, Q_2 and Q_4 are turned on to pass the energy stored in the inductor to the output until the next cycle begins. The output voltage increases in the wake-up period. When the output reaches 0.82V again, the controller enters into Low Power Off mode again. When the load current increases, the Low Power Off mode period decreases. When the off mode period disappears and the load current further increases but still does not meet the Equation 13 exit condition, the output voltage drops. When the FB_OUT pin voltage drops to 0.78V, the controller exits Burst mode and runs in normal DE PWM mode. The voltage error amplifier takes control of the output voltage regulation.

In Low Power Off mode, the CLKEN pin goes low. By connecting the BSTEN and CLKEN pins in a multiple chip parallel system, the Burst mode enter/exit and burst on/off control are all synchronized.

Because V_{OUT} is controlled by a window comparator in Burst mode, higher than normal low-frequency voltage ripple appears on V_{OUT}, which can generate audible noise if the inductor and output capacitors are not chosen properly. Also, the efficiency in D/(1-D) Buck-Boost mode is low. To avoid these drawbacks, disable the Burst mode by choosing a bigger R_{IM_OUT} to set the IMON_OUT pin voltage higher than 0.88V at no load condition, shown in Equation 14. The part runs in DE mode only. Pulse Skipping mode can also be implemented to lower the light load power loss with much lower output voltage ripple as V_{OUT} is always controlled by the regulator Gm1.

(EQ. 14) $$R_{IM_OUT} \times I_{SENOFFSET} > V_{IMONOUTBSTEX}$$

5.8 Prebiased Power-Up

The ISL81801 can soft-start with a prebiased output by running in forced DE mode during soft-start. The output voltage is not pulled down during prebiased start-up. The PWM mode is not active until the soft-start ramp reaches 90% of the output voltage times the resistive divider ratio. Forced DE mode is set again when the SS/TRK pin voltage is pulled to less than 0.3V by either an internal or external circuit.

The overvoltage protection function is still operational during soft-start in DE mode.

5.9 Frequency Selection

Switching frequency selection is a trade-off between efficiency and component size. Low switching frequency improves efficiency by reducing MOSFET switching loss. To meet the output ripple and load transient requirements, operation at a low switching frequency requires larger inductance and output capacitance. The switching frequency of the ISL81801 is set by a resistor connected from the RT/SYNC pin to GND according to Equation 1.

The frequency setting curve shown in Figure 51 assists in selecting the correct value for R_T.

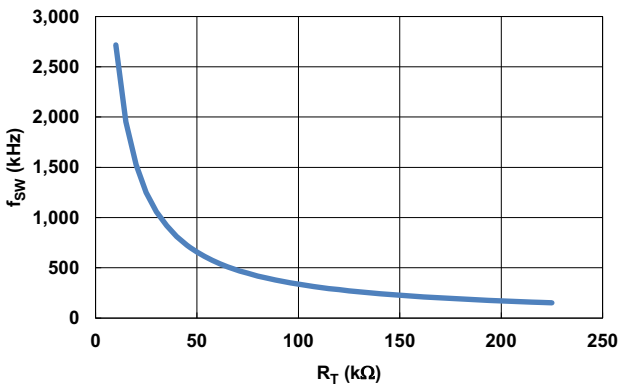


Figure 51. R_T vs Switching Frequency f_{SW}

5.10 Phase Lock Loop (PLL)

The ISL81801 integrates a high-performance PLL. The PLL ensures a wide range of accurate clock frequency and phase setting. It also makes the internal clock easily synchronized to an external clock with the frequency either lower or higher than the internal setting.

As shown in Figure 52, an external compensation network of R_{PLL}, C_{PLL1}, and C_{PLL2} is needed to connect to the PLL_COMP pin to ensure PLL stable operation. Renesas recommends choosing 2.7kΩ for R_{PLL}, 10nF for C_{PLL1}, and 820pF for C_{PLL2}. With the recommended compensation network, the PLL stability is ensured in the full clock frequency range of 100kHz to 600kHz.

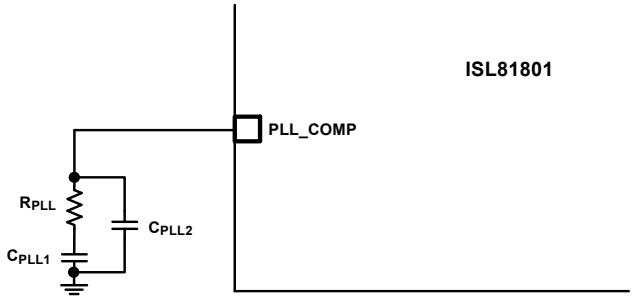


Figure 52. PLL Compensation Network

5.11 Frequency Synchronization and Dithering

The RT/SYNC pin can synchronize the ISL81801 to an external clock or the CLKOUT/DITHER pin of another ISL81801. When the RT/SYNC pin is connected to the CLKOUT/DITHER pin of another ISL81801, the two controllers operate in cascade synchronization with phase interleaving.

When the RT/SYNC pin is connected to an external clock, the ISL81801 synchronizes to this external clock frequency. The frequency set by the R_T resistor is either lower or higher than, or equal to the external clock frequency.

The CLKOUT/DITHER pin outputs a clock signal with approximately 300ns pulse width. The signal frequency is the same as the frequency set by the resistor from the RT pin to ground or the external sync clock. The signal rising edge phase angle to the rising edge of the internal clock or the external clock to the RT/SYNC pin is set by the voltage applied to the FB_IN and IMON_IN pins. The phase interleaving is implemented by the cascade connecting of the upper chip CLKOUT/DITHER pin to the lower chip RT/SYNC pin in a parallel system. Table 2 shows the CLKOUT/DITHER phase settings with different FB_IN and IMON_IN pin voltages.

Table 2. CLKOUT Phase Shift vs FB_IN and IMON_IN Voltage

CLKOUT Phase Shift	120°	90°	60°	180°
FB_IN Voltage	Active	1	1	Active
IMON_IN Voltage	1	Active	1	Active

Note: “1” means logic high 4.7V to 5V. “Active” means logic low 0V to 4.3V.

When the FB_IN is connected to 5V, the V_{IN} feedback control loop is disabled. When IMON_IN is connected to 5V, the average input current control loop and input current hiccup OCP are disabled.

In multi-chip cascade parallel operation, the CLKOUT pin of the upstream chip is connected to the RT/SYNC pin of the downstream chip. The BSTEN, SS/TRK, OV, EN/UVLO, and CLKEN pins of all the paralleled chips should be tied together.

The CLKOUT/DITHER pin provides a dual function option. When a capacitor C_{DITHER} is connected on the CLKOUT/DITHER pin, the internal circuit disables the CLKOUT function and enables the DITHER function. When the CLKOUT/DITHER pin voltage is lower than 1.05V, a typical 8µA current source $I_{DITHERSO}$ charges the capacitor on the pin. When the capacitor voltage is charged to more than 2.2V, a typical 10µA current source $I_{DITHERSI}$ discharges the capacitor on the pin. A sawtooth voltage waveform shown in Figure 53 is generated on the CLKOUT/DITHER pin. The internal clock frequency is modulated by the sawtooth voltage on the CLKOUT/DITHER pin. The clock frequency dither range is set to typically ±15% of the frequency set by the resistor on RT/SYNC pin. The dither function is lost when the chip is synchronized to an external clock.

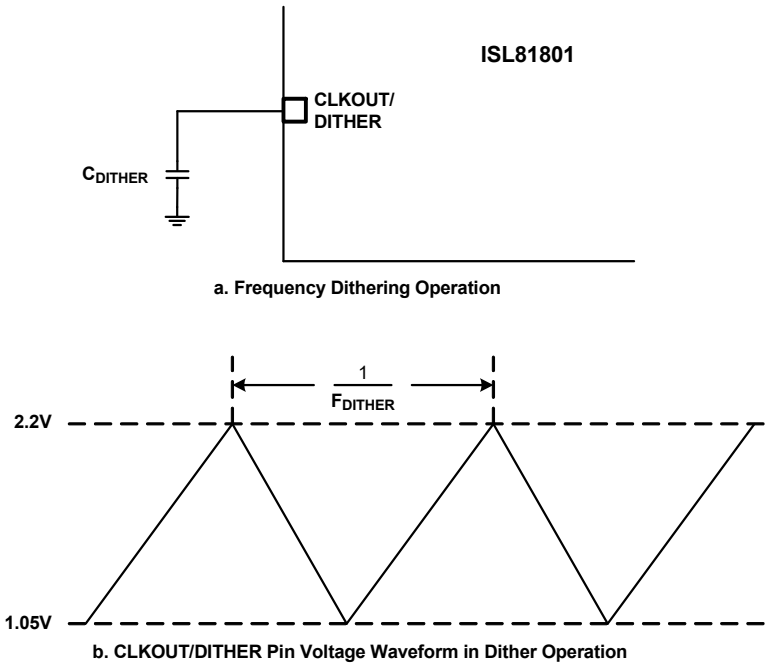


Figure 53. Frequency Dithering Operation

The dither frequency F_{DITHER} is calculated using Equation 15. Renesas recommends setting C_{DITHER} between 10nF and 1µF. With a too low C_{DITHER} the part may not be able to set to Dither mode. With a higher C_{DITHER}, the discharge power loss at disable or power off is higher, leading to a higher thermal stress to the internal discharge circuit. The recommended dither frequency is 1/10 of crossover frequency.

(EQ. 15) $$F_{DITHER} = \frac{3.865 \times 10e(-6)}{C_{DITHER}}$$

5.12 Parallel Operation Current Sharing

Multiple ISL81801 controlled buck-boost DC/DC converters are paralleled to each other in cascade as described in Frequency Synchronization and Dithering. The currents in the paralleled converters are shared by feeding the same connected COMP pin voltage signal to the reference of the current control loops in each IC. However, the current sharing accuracy is not ideal because the loose tolerance in RAMP and current sense circuit settings. To achieve an acceptable current sharing accuracy, an external active current sharing circuit is recommended, as shown in Figure 54.

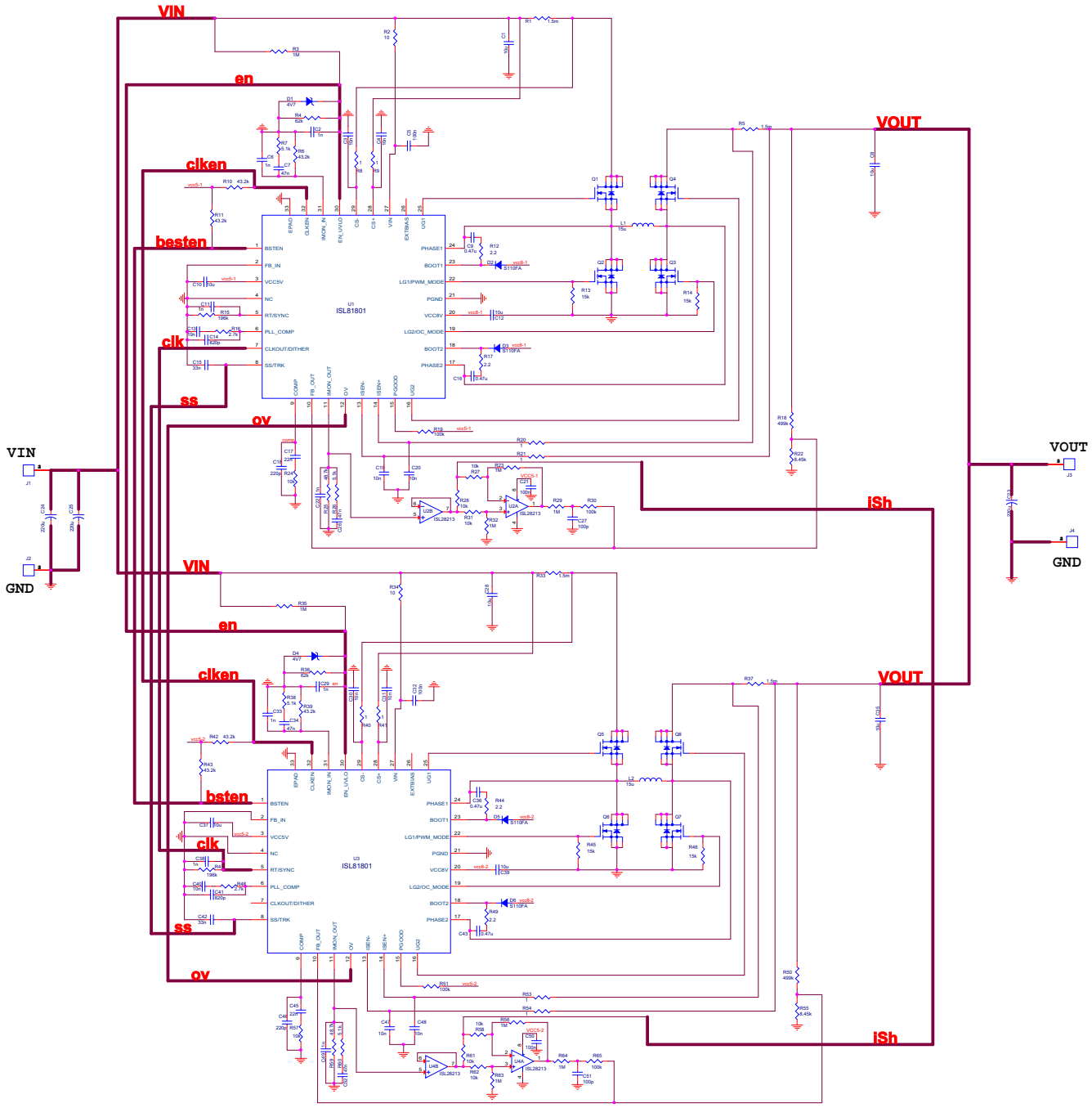


Figure 54. Current Sharing Circuit

Figure 54 shows the connections between the two paralleled converters. Two external operational amplifiers (op amps) are added for active current sharing in each converter. The first op amp, U2B in Converter 1 or U4B in Converter 2, is a buffer to send the local output current signal from the IMON_OUT pin to the current sharing

circuit. The buffer output is connected to the iSh bus using R_{28} in Converter 1 and R_{61} in Converter 2 to create the reference signal. The voltage on the iSh bus, V_{iSh}, is calculated using Equation 16.

(EQ. 16) $$V_{iSh} = (V_{IMON_OUT1} + V_{IMON_OUT2})/2$$

where V_{IMON_OUT1} is the Converter 1 IMON_OUT pin voltage and V_{IMON_OUT2} is the Converter 2 IMON_OUT pin voltage.

The second op amp, U2A in Converter 1 or U4A in Converter 2 is a differential op amp to feed the current error signal to the IC FB_OUT pin. The differential input signal is equal to V_{IMON_OUT1} - V_{iSh} for U2A and V_{IMON_OUT2} - V_{iSh} for U4A. The differential op amp gain and the value of the resistor between the op amp output and the FB_OUT pin is defined based on the current sharing accuracy and the allowed maximum output voltage change caused by the current sharing loop, assuming the current sense circuit tolerance is ignored.

The maximum allowed current sharing error is represented by the maximum allowed differential op amp input. The differential op amp outputs a maximum voltage of 5V at its maximum differential input, assuming a rail-to-rail op amp is used. The differential op amp gain Ksh is calculated using Equation 17.

(EQ. 17) $$Ksh = \frac{5}{\Delta Vsh}$$

where ΔVsh is the maximum allowed differential op amp input voltage, which is proportional to the output current sharing error $\Delta Ish = |I_{OUT1} - I_{OUT2}| / 2$. I_{OUT1} and I_{OUT2} are the output currents of Converter 1 and 2, respectively. $\Delta Vsh = \Delta Ish \times R_{IM_OUT} \times R_{S_OUT} \times Gm_{ISEN}$, referring to the descriptions in Input and Output Average Current Monitoring and Regulation Loops.

As shown in Figure 54, Ksh = R_{23}/R_{27} for Converter 1 and Ksh = R_{56}/R_{58} for Converter 2.

The value Rsh of the resistor between the differential op amp output and the FB_OUT pin is calculated using Equation 18.

(EQ. 18) $$Rsh = \frac{5 \times R_{FBO1}}{\Delta V_{OUT}}$$

where ΔV_{OUT} is the maximum allowed output voltage change caused by the current sharing loop, which is limited by the V_{OUT} regulation tolerance.

R_{FBO1} is the resistance of the upper resistor of the V_{OUT} voltage sense divider shown in Figure 43. As shown in Figure 54, Rsh = $R_{29} + R_{30}$ for Converter 1 and Rsh = $R_{64} + R_{65}$ for Converter 2. $R_{FBO1} = R_{18}$ for Converter 1 and $R_{FBO1} = R_{50}$ for Converter 2.

5.13 Gate Drivers

The ISL81801 integrates two almost identical high voltage driver pairs to drive both buck and boost MOSFET pairs. Each driver pair consists of a gate control logic circuit, a low-side driver, a level shifter, and a high-side driver.

The ISL81801 incorporates an adaptive dead time algorithm that optimizes operation with varying MOSFET conditions. This algorithm provides approximately 16ns dead time between the switching of the upper and lower MOSFETs. This dead time is adaptive and allows operation with different MOSFETs without having to externally adjust the dead time using a resistor or capacitor. During turn-off of the lower MOSFET, the LGATE voltage is monitored until it reaches a threshold of 1V, at which time the UGATE is released to rise. Adaptive dead time circuitry monitors the upper MOSFET gate voltage during UGATE turn-off. When the upper MOSFET gate-to-source voltage drops below a threshold of 1V, the LGATE is allowed to rise. Renesas recommends against using a resistor between the driver outputs and the respective MOSFET gates, because it can interfere with the dead time circuitry.

The low-side gate driver is supplied from VDD and provides a 3A peak sink and 2A peak source current. The high-side gate driver can also deliver peak 3A sink and 2A source current. Gate-drive voltage for the upper

N-channel MOSFET is generated by a flying capacitor boot circuit. A boot capacitor connected from the BOOT pin to the PHASE node provides power to the high-side MOSFET driver. As shown in Figure 55, the boot capacitor is charged up to VDD by an external Schottky diode during low-side MOSFET on-time (phase node low). To limit the peak current in the Schottky diode, an external resistor is placed between the BOOT pin and the boot capacitor. This small series resistor also damps any oscillations caused by the resonant tank of the parasitic inductances in the traces of the board and the FET's input capacitance.

At start-up, the low-side MOSFET turns on first and forces PHASE to ground to charge the BOOT capacitor to 8V if the diode voltage drop is ignored. After the low-side MOSFET turns off, the high-side MOSFET is turned on by closing an internal switch between BOOT and UGATE. This provides the necessary gate-to-source voltage to turn on the upper MOSFET, an action that boosts the 8V gate drive signal above V_{IN}. The current required to drive the upper MOSFET is drawn from the internal 8V regulator supplied from either VIN or EXTBIAS pin.

The BOOT to PHASE voltage is monitored internally. When the voltage drops to 5.95V at no switching condition, a minimum off-time pulse is issued to turn off the upper MOSFET and turn on the low-side MOSFET to refresh the bootstrap capacitor and maintain the upper driver bias voltage.

To optimize EMI performance or reduce phase node ringing, a small resistor is placed between the BOOT pin to the positive terminal of the bootstrap capacitor.

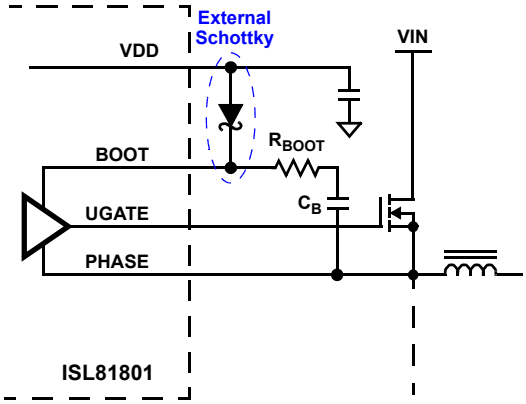


Figure 55. Upper Gate Driver Circuit

5.14 Power-Good Indicator

The power-good pin can monitor the status of the output voltage. PGOOD is true (open drain) 1.1ms after the FB_OUT pin is within ±10% of the reference voltage.

There is no extra delay when the PGOOD pin is pulled LOW.

6. Protection Circuits

The converter output and input are monitored and protected against overload, overvoltage, and undervoltage conditions.

6.1 Input Undervoltage Lockout (UVLO)

The ISL81801 includes input UVLO protection, which keeps the device in a reset condition until a proper operating voltage is applied. UVLO protection shuts down the ISL81801 if the input voltage drops below 3.2V. The controller is disabled when UVLO is asserted. When UVLO is asserted, PGOOD (Power Good) is valid and is deasserted. If the input voltage rises above 3.5V, UVLO is deasserted to allow the start-up operation.

6.2 VCC5V Power-On Reset (POR)

The ISL81801 sets its VCC5V POR rising threshold at 4V and falling threshold at 3.5V when supplied by V_{IN}. EXTBIAS can only be applied kick in only after VCC5V reaches its POR rising threshold.

6.3 Overcurrent Protection (OCP)

6.3.1 Input and Output Average Overcurrent Protection

As described in Input and Output Average Current Monitoring and Regulation Loops, the ISL81801 can regulate both input and output current with closed loop control. This provides a constant current type of overcurrent protection for both input and output average current. It is set to a hiccup type of protection by selecting a different value of the resistor connected between LG2/OC_MODE and GND.

The input and output constant or hiccup average OCP set points I_{INCC} and I_{OUTCC} are calculated using Equation 9 and Equation 10.

The average OCP mode is set by a resistor connected from the LG2/OC_MODE pin to ground during the initialization period before soft-start. During the initialization period, the LG2/OC_MODE pin sources out typical 10µA current $I_{MODELG2}$ to set the voltage on the pin. If the pin voltage is less than typical 0.3V, the OCP is set to Constant Current-mode. Otherwise, the OCP is set to hiccup mode.

In hiccup OCP mode, after the average current is higher than the set point for 32 consecutive switching cycles the converter turns off for 50ms before a restart-up is issued.

6.3.2 First Level Pulse-by-Pulse Peak Current Limit

As shown in Figure 45 in Input and Output Average Current Monitoring and Regulation Loops, the inductor peak current is sensed by the shunt resistor R_{S_IN} and amplifier A1. When the voltage drop on R_{S_IN} reaches the set point $V_{OCSET-CS}$ typical 82mV, Q_1 is turned off in Buck mode or Q_3 is turned off in Boost mode. The first level peak current limit set point I_{OCPP1} is calculated using Equation 19.

(EQ. 19) $$I_{OCPP1} = \frac{V_{OCSET-CS}}{R_{S_IN}}$$

6.3.3 Second Level Hiccup Peak Current Protection

To avoid any false trip in peak current-mode operation, a minimum on or blanking time is set to the PWM signal. The first level pulse-by-pulse current limit circuit cannot further reduce the PWM duty cycle in the minimum on-time. In an output dead short condition, especially at high V_{IN}, the inductor current increases rapidly, even with the minimum on-time PWM duty cycle. The ISL81801 integrates a second level hiccup type of peak current protection. When the voltage drop on R_{S_IN} reaches the set point $V_{OCSET-CS-HIC}$ (typical 100mV), the converter turns off by turning off all four switches Q_1, Q_2, Q_3, and Q_4 for 50ms before a re-start up is issued. The second level peak current protection set point I_{OCPP2} is calculated using Equation 20.

(EQ. 20) $$I_{OCPP2} = \frac{V_{OCSET-CS-HIC}}{R_{S_IN}}$$

6.3.4 Pulse-by-Pulse Negative Peak Current Limit

In cases of reverse direction operation and OVP protection, the inductor current becomes negative. The negative current is sensed by the shunt resistor R_{S_OUT} and amplifier A2 as shown in Figure 45. When the voltage drop on R_{S_OUT} reaches the set point $V_{OCSET-ISEN}$ (typical -59mV), Q_2 and Q_4 are turned off and Q_1 and Q_3 are turned on. The negative peak current limit set point I_{OCPPN} is calculated using Equation 21.

(EQ. 21) $$I_{OCPPN} = \frac{V_{OCSET-ISEN}}{R_{S_OUT}}$$

The device is damaged in negative peak current limit conditions. In these conditions, the energy flows from output to input. If the impedance of the input source or devices is not low enough, the V_{IN} voltage increases. When V_{IN} increases to higher than its maximum limit, the IC is damaged.

6.4 Overvoltage Protection (OVP)

The overvoltage set point is set at 114% of the nominal output voltage set by the feedback resistors. In the case of an overvoltage event, the IC attempts to bring the output voltage back into regulation by keeping Q_1 and Q_3 turned off and Q_2 and Q_4 turned on. If the OV condition continues, the inductor current goes negative to trip the negative peak current limit. The converter reverses direction to transfer energy from the output end to the input end. Input voltage is pushed high if the input source impedance is not low enough. The IC is damaged if the input voltage goes to higher than its maximum limit. If the overvoltage condition is corrected and the output voltage drops to the nominal voltage, the controller resumes normal PWM switching. The OV pin is pulled high when output OVP trips.

6.5 Over-Temperature Protection (OTP)

The ISL81801 incorporates an over-temperature protection circuit that shuts the IC down when a die temperature of +160°C is reached. Normal operation resumes when the die temperature drops below +145°C through the initiation of a full soft-start cycle. During OTP shutdown, the IC consumes only 100µA current. When the controller is disabled, thermal protection is inactive. This helps achieve a very low shutdown current of 5µA.

7. Layout Guidelines

Careful attention to layout requirements is necessary for successful implementation of an ISL81801 based DC/DC converter. The ISL81801 switches at a very high frequency, so the switching times are very short. At these switching frequencies, even the shortest trace has significant impedance. Also, the peak gate drive current rises significantly in an extremely short time. Transition speed of the current from one device to another causes voltage spikes across the interconnecting impedances and parasitic circuit elements. These voltage spikes can degrade efficiency, generate EMI, and increase device voltage stress and ringing. Careful component selection and proper Printed Circuit Board (PCB) layout minimize the magnitude of these voltage spikes.

The three sets of critical components in a DC/DC converter using the ISL81801 are the following:

- The controller
- The switching power components
- The small signal components

The switching power components are the most critical from a layout point of view because they switch a large amount of energy, which tends to generate a large amount of noise. The critical small signal components are those connected to sensitive nodes or those supplying critical bias currents. A multilayer PCB is recommended.

7.1 Layout Considerations

- Place the input capacitors, buck FETs, inductor, boost FETs, and output capacitor first. Isolate these power components on dedicated areas of the board with their ground terminals adjacent to one another. Place the input and output high frequency decoupling ceramic capacitors very close to the MOSFETs.
- If signal components and the IC are placed in a separate area to the power train, use full ground planes in the internal layers with shared SGND and PGND to simplify the layout design. Otherwise, use separate ground planes for the power ground and the small signal ground. Connect the SGND and PGND close to the IC. DO NOT connect them together anywhere else.
- Keep the loop formed by the input capacitor, the buck top FET, and the buck bottom FET as small as possible. Also, keep the loop formed by the output capacitor, the boost top FET, and the boost bottom FET as small as possible.
- Keep the current paths from the input capacitor to the buck FETs, the power inductor, the boost FETs, and the output capacitor as short as possible with maximum allowable trace widths.
- Place the PWM controller IC close to the lower FETs. The low-side FETs gate drive connections should be short and wide. Place the IC over a quiet ground area. Avoid switching ground loop currents in this area.
- Place the VDD bypass capacitor close to the VDD pin of the IC and connect its ground end to the PGND pin. Connect the PGND pin to the ground plane by a via. Do not directly connect the PGND pin to the SGND EPAD.
- Place the gate drive components (BOOT diodes and BOOT capacitors) together near the controller IC.
- Place the output capacitors as close to the load as possible. Use short, wide copper regions to connect output capacitors to load to avoid inductance and resistances.
- Use copper filled polygons or wide short traces to connect the junction of the buck or boost upper FET, buck or boost lower FET, and output inductor. Also, keep the buck and boost PHASE nodes connection to the IC short. DO NOT oversize the copper islands for the PHASE nodes. Because the phase nodes are subjected to very high dv/dt voltages, the stray capacitor formed between these islands and the surrounding circuitry tends to couple switching noise.
- Route all high speed switching nodes away from the control circuitry.
- Create a separate small analog ground plane near the IC. Connect the SGND pin to this plane. Connect a small signal grounding paths including feedback resistors, current monitoring resistors and capacitors, soft-starting capacitors, loop compensation capacitors and resistors, and EN pull-down resistors to this SGND plane.
- Use a pair of traces with minimum loop for the input or output current sensing connection.

- Keep the feedback connection to the output capacitor is short and direct.

7.2 General EPAD Design Considerations

Figure 56 shows how to use vias to remove heat from the IC.

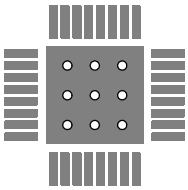


Figure 56. PCB Via Pattern

Fill the thermal pad area with vias. A typical via array fills the thermal pad footprint so that their centers are three times the radius apart from each other. Keep the vias small but not so small that their inside diameter prevents solder wicking through during reflow.

Connect all vias to the ground plane. The vias must have a low thermal resistance for efficient heat transfer. Ensure a complete connection of the plated through hole to each plane.

8. Component Selection Guideline

8.1 MOSFET Considerations

The MOSFETs are chosen for optimum efficiency given the potentially wide input voltage range and output power requirement. Select these MOSFETs based upon $r_{DS(ON)}$, gate supply requirements, and thermal management considerations.

The buck maximum operation voltage of the MOSFETs is decided by the maximum V_{IN} voltage, and the boost maximum operation voltage of the MOSFETs is decided by the maximum V_{OUT} voltage. Choose the buck or boost MOSFETs based on their maximum operation voltage with sufficient margin for safe operation.

The MOSFET power dissipations are based on: conduction loss and switching loss. In Buck mode, the power loss of the buck upper and lower MOSFETs are calculated using Equation 22 and Equation 23. The conduction losses are the main source of power dissipation for the lower MOSFET. Only the upper MOSFET has significant switching losses, because the lower device turns on and off into near zero voltage. The equations assume linear voltage current transitions and do not model power loss because of the reverse recovery of the lower MOSFET body diode.

(EQ. 22) $$P_{UPPERBUCK} = \frac{(I_{OUT}^2)(r_{DS(ON)})(V_{OUT})}{V_{IN}} + \frac{(I_{OUT})(V_{IN})(t_{SW})(f_{SW})}{2}$$

(EQ. 23) $$P_{LOWERBUCK} = \frac{(I_{OUT}^2)(r_{DS(ON)})(V_{IN} - V_{OUT})}{V_{IN}}$$

In Boost mode, there is only conduction loss on the buck upper MOSFET calculated using Equation 24.

(EQ. 24) $$P_{UPPERBUCK} = \left[\frac{(I_{OUT}^2)(V_{OUT}^2)}{(V_{IN}^2)}\right](r_{DS(ON)})$$

In Boost mode, the power losses of the boost upper and lower MOSFETs are calculated using Equation 25 and Equation 26. The conduction losses are the main component of power dissipation for the upper MOSFET. Only the lower MOSFET has significant switching losses, because the upper device turns on and off into near zero voltage. The equations assume linear voltage current transitions and do not model power loss because the reverse recovery of the upper MOSFET body diode.

(EQ. 25) $$P_{LOWERBOOST} = \left[\frac{(I_{OUT}^2)(V_{OUT}^2)}{(V_{IN}^2)}\right]\frac{(V_{OUT} - V_{IN})(r_{DS(ON)})}{V_{OUT}} + \frac{(I_{OUT})(V_{OUT}^2)(t_{SW})(f_{SW})}{2(V_{IN})}$$

(EQ. 26) $$P_{UPPERBOOST} = \frac{(I_{OUT}^2)(r_{DS(ON)})(V_{OUT})}{V_{IN}}$$

In Buck mode, the conduction loss exists on the boost upper MOSFET calculated using Equation 27.

(EQ. 27) $$P_{UPPERBOOST} = (I_{OUT}^2)(r_{DS(ON)})$$

A large gate-charge increases the switching time, t_{SW}, which increases the switching losses of the buck upper and boost lower MOSFETs. Ensure that all four MOSFETs are within their maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal resistance specifications.

8.2 Inductor Selection

The inductor is selected to meet the output voltage ripple requirements. The inductor value determines the ripple current of the converter, and the ripple voltage is a function of the ripple current and the output capacitor(s) ESR. The ripple voltage expression is given in the capacitor selection section and the ripple current is approximated by Equation 28 for Buck mode and Equation 29 for Boost mode.

(EQ. 28) $$\Delta I_{LBuck} = \frac{(V_{IN} - V_{OUT})(V_{OUT})}{(f_{SW})(L)(V_{IN})}$$

(EQ. 29) $$\Delta I_{LBoost} = \frac{(V_{OUT} - V_{IN})(V_{IN})}{(f_{SW})(L)(V_{OUT})}$$

The ripple current ratio is usually 30% to 70% of the inductor average current at the full output load condition.

8.3 Output Capacitor Selection

In general, select the output capacitors to meet the dynamic regulation requirements including ripple voltage and load transients. Selection of output capacitors is also dependent on the inductor, so some inductor analysis is required to select the output capacitors.

One of the parameters limiting the converter's response to a load transient is the time required for the inductor current to slew to its new level. The ISL81801 provides either 0% or maximum duty cycle in response to a load transient.

The response time is the time interval required to slew the inductor current from an initial current value to the load current level. During this interval, the difference between the inductor current and the transient current level must be supplied by the output capacitor(s). The output capacitance is minimized if faster loop compensation is used. Also, if the load transient rise time is slower than the inductor response time, as in a hard drive or CD drive, it reduces the requirement on the output capacitor.

The minimum capacitor value required to provide the full, rising step, transient load current during the response time of the inductor is shown in Equation 30 for Buck mode and Equation 31 for Boost mode:

(EQ. 30) $$C_{OUTBuck} = \frac{(L)(I_{TRAN})^2}{2(V_{IN} - V_{OUT})(DV_{OUT})}$$

(EQ. 31) $$C_{OUTBoost} = \frac{(L)(V_{OUT})(I_{TRAN})^2}{2(V_{IN}^2)(DV_{OUT})}$$

where C_{OUT} is the output capacitor(s) required, L is the inductor, I_{TRAN} is the transient load current step, V_{IN} is the input voltage, V_{OUT} is output voltage, and DV_{OUT} is the drop in output voltage allowed during the load transient.

High frequency capacitors initially supply the transient current and slow the load rate of change seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the Equivalent Series Resistance (ESR), voltage rating requirements, and actual capacitance requirements.

In Buck mode, the output voltage ripple is because the inductor ripple current and the ESR of the output capacitors as defined by Equation 32:

(EQ. 32) $$V_{RIPPLE} = \Delta I_{LBuck}(ESR)$$

where ΔI_{LBuck} is calculated in Equation 28.

In Boost mode, the current to the output capacitor is not continuous. The output voltage ripple is much higher as defined by Equation 33:

(EQ. 33) $$V_{RIPPLE} = \left(\frac{(I_{OUT})(V_{OUT})}{V_{IN}} + \frac{\Delta I_{LBoost}}{2}\right)(ESR)$$

where ΔI_{LBoost} is calculated in Equation 29.

Place high frequency decoupling capacitors as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. Consult with the manufacturer of the load circuitry for specific decoupling requirements.

Use only specialized low-ESR capacitors intended for switching regulator applications for the bulk capacitors. In most cases, multiple small case electrolytic capacitors perform better than a single large case capacitor.

The stability requirement on the selection of the output capacitor is that the ESR zero (f_Z) is between 2kHz and 60kHz. The ESR zero can help increase phase margin of the control loop.

This requirement is shown in Equation 34:

(EQ. 34) $$C_{OUT} = \frac{1}{2\pi(ESR)(f_Z)}$$

In conclusion, the output capacitors must meet the following criteria:

- They must have sufficient bulk capacitance to sustain the output voltage during a load transient while the output inductor current is slewing to the value of the load transient.
- The ESR must be sufficiently low to meet the desired output voltage ripple because the supplied ripple current.
- The ESR zero should be placed in a large range to provide additional phase margin.

8.4 Input Capacitor Selection

The important parameters for the input capacitor(s) are the voltage rating and the RMS current rating. For reliable operation, select input capacitors with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and 1.5 times is a conservative guideline. In Buck mode the AC RMS input current varies with the load giving in Equation 35:

(EQ. 35) $$I_{RMS} = \sqrt{DC - DC^2} \times I_{OUT}$$

where DC is duty cycle.

The maximum RMS current supplied by the input capacitance occurs at V_{IN} = 2 X V_{OUT}, DC = 50% as shown in Equation 36:

(EQ. 36) $$I_{RMS} = \frac{1}{2} \times I_{OUT}$$

In Boost mode, the input current is continuous. The RMS current supplied by the input capacitance is much smaller.

Use a mix of input bypass capacitors to control the voltage ripple across the MOSFETs. Use ceramic capacitors for the high frequency decoupling and bulk capacitors to supply the RMS current. Place small ceramic capacitors close to the MOSFETs to suppress the voltage induced in the parasitic circuit impedances.

Solid tantalum capacitors are used, but use caution with regard to the capacitor surge current rating. These capacitors must be capable of handling the surge current at power-up.

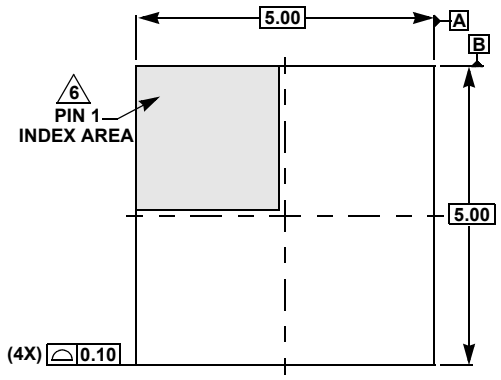
9. Revision History

Rev.	Date	Description
1.4	Mar 8, 2024	Updated Frequency Synchronization and Dithering section.
1.3	Jul 14, 2023	Updated the Input and Output Average Current Monitoring and Regulation Loops section.
1.2	Jun 2, 2021	Updated Figure 6. Updated Links throughout. Updated Ordering Information table.
1.1	Oct 16, 2020	Electrical Spec table, Operating Current - added row for EXTBIAS = 12V, Typ value 50µA.
1.0	Sep 23, 2020	Initial release

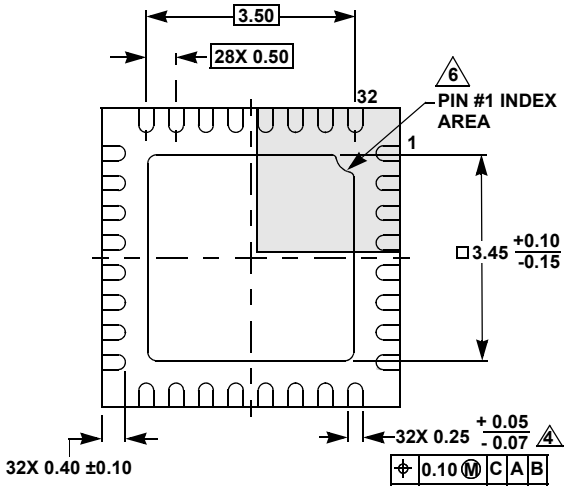
10. Package Outline Drawings

For the most recent package outline drawing, see L32.5x5A.

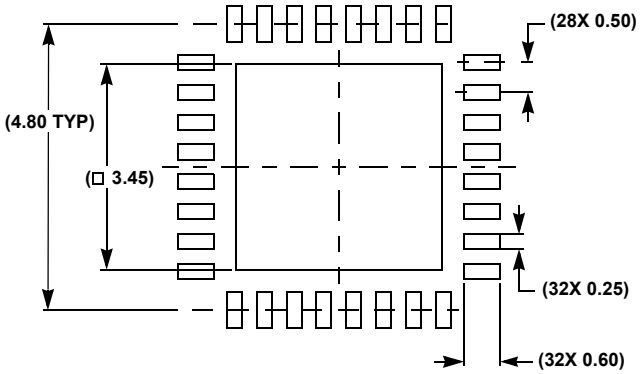
L32.5x5A
32 Lead Thin Quad Flat No-Lead Plastic Package
Rev 1, 5/17



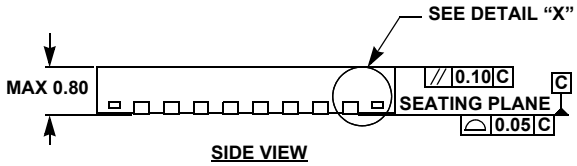
TOP VIEW



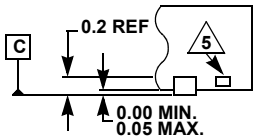
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



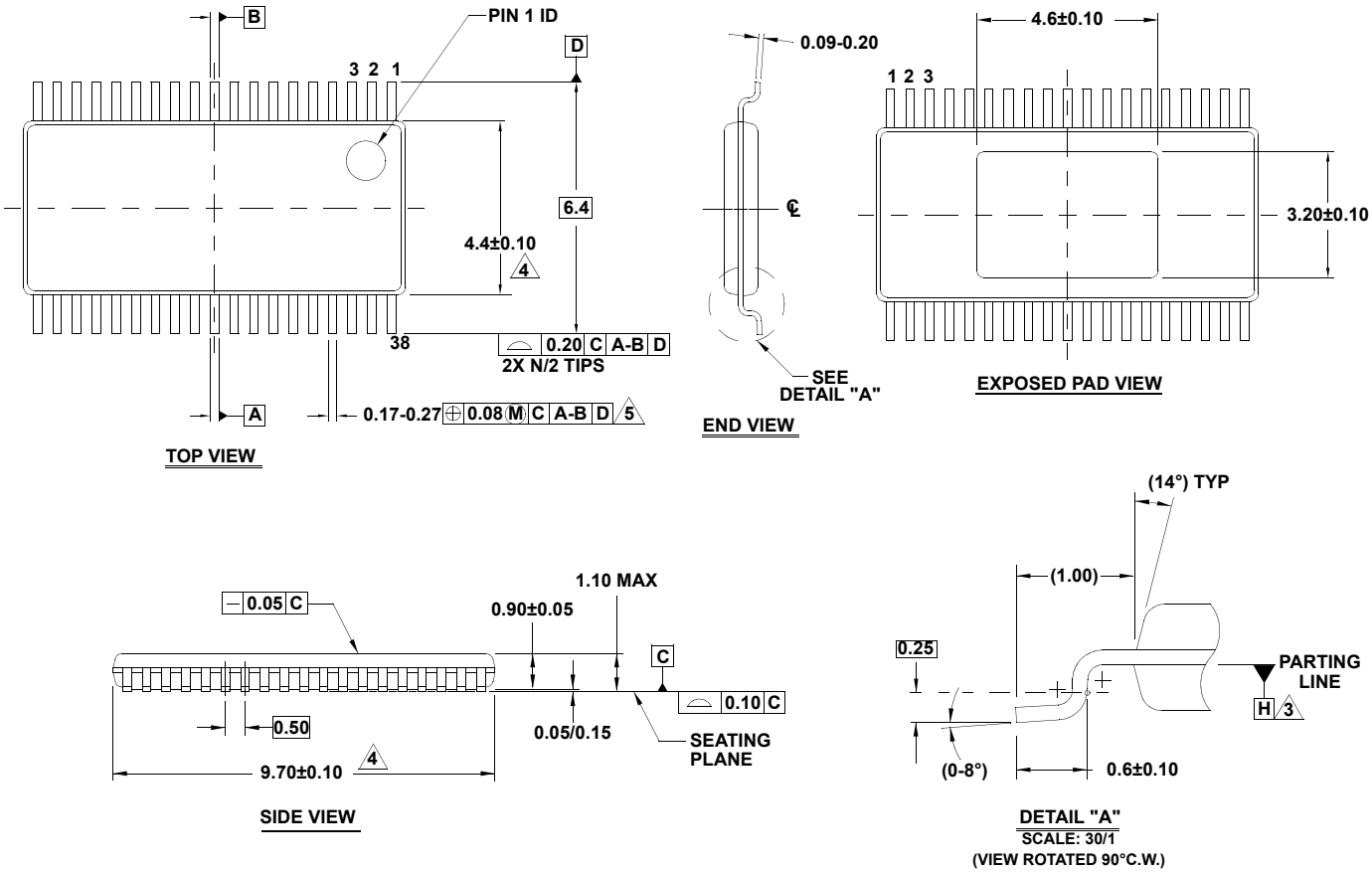
DETAIL "X"

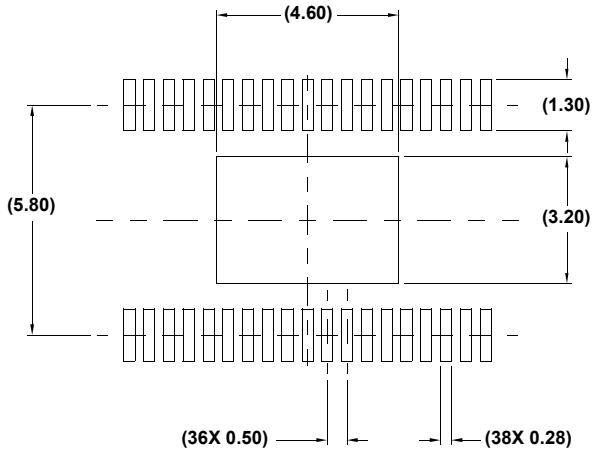
NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for reference only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ±0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

For the most recent package outline drawing, see M38.173C.

M38.173C
38 Lead Heat-Sink Thin Shrink Small Outline Plastic Package (HTSSOP)
Rev 0, 4/10





TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Die thickness allowable is 0.279±0.0127 (0.0110±0.0005 inches).
2. Dimensioning & tolerances per ASME. Y14.5m-1994.
3. Datum plane H located at mold parting line and coincident with lead where lead exits plastic body at bottom of parting line.
4. At reference datum and does not include mold flash or protrusions, and is measured at the bottom parting line. Mold flash or protrusions shall not exceed 0.15mm on the package ends and 0.25mm between the leads.
5. The lead width dimension does not include dambar protrusion. Allowable dambar protrusion shall be 0.07mm total in excess of the lead width dimension at maximum material condition. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusions and an adjacent lead should be 0.08mm.
6. This part is compliant with JEDEC specification MO-153 variation BDT-1

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01 Jan 2024)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

© 2024 Renesas Electronics Corporation. All rights reserved.