ISL8201M

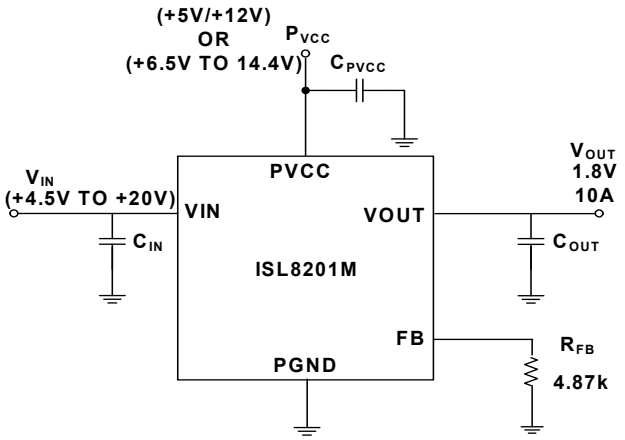
10A, High Efficiency DC/DC Module

FN6657
Rev 3.00
October 28, 2014

The ISL8201M is a 20V, 10A output current, variable output step-down power supply. Included in the 15mmx15mm package is a high performance PWM controller switching at 600kHz, power MOSFETs, an inductor, and all the passive components required for complete DC/DC power solution. The ISL8201M operates over an input voltage range of 1V to 20V and supports an output voltage range of 0.6V to 5V, which is set by a single dividing resistor. This high efficiency power module is capable of delivering 10A (17A peak) output with up to 95% efficiency, needing no heat sinks or airflow to meet power specifications. Only bulk input and output capacitors are needed to finish the design. Utilizing voltage-mode control, the output voltage can be precisely regulated to as low as 0.6V with up to ±1% output voltage regulation. The ISL8201M also features internal compensation, internal soft-start, auto-recovery overcurrent protection, an enable option, and pre-biased output start-up capability.

The ISL8201M is packaged in a thermally enhanced, compact (15mmx15mm) and low profile (3.5mm) overmolded QFN Package Module suitable for automated assembly by standard surface mount equipment. The ISL8201M is RoHS compliant.

Typical Schematic



Features

- Complete Switch Mode Power Supply
- Bias Voltage Range from +4.5 to +14.4V
  - Wide Input Voltage Range from 1V up to 20V (see "Input Voltage Considerations" on page 11)
- 10A DC Output Current, 17A Peak Output Current
- Adjustable +0.6V to +5V Output Range
- Up to 95% Efficiency
- Simple Voltage Mode Control
- Fixed 600kHz Switching Frequency
- Fast Transient Response
- Enable Function Option
- Pre-biased Output Start-up Capability
- Internal Soft-Start
- Overcurrent Protection by Low-Side MOSFET $r_{DS(ON)}$ Sensing (Non-Latching, Auto-Recovery)
- Small Footprint, Low Profile Surface Mount QFN Package (15mmx15mmx3.5mm)
- RoHS Compliant

Applications

- Servers
- Industrial Equipment
- Point of Load Regulation
- Other General Purpose Step-Down DC/DC
- Telecom and Datacom Applications

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL8201MIRZ	ISL8201M	15 Ld QFN	L15.15x15
ISL8201MEVAL1Z	Evaluation Board		

1. Add “-T” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil plastic packaged products are RoHS compliant by EU exemption 7C-I and employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3) termination finish which is compatible with both SnPb and Pb-free soldering operations. Intersil RoHS compliant products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see product information page for ISL8201M. For more information on MSL please see techbrief TB363.

Simplified Block Diagram

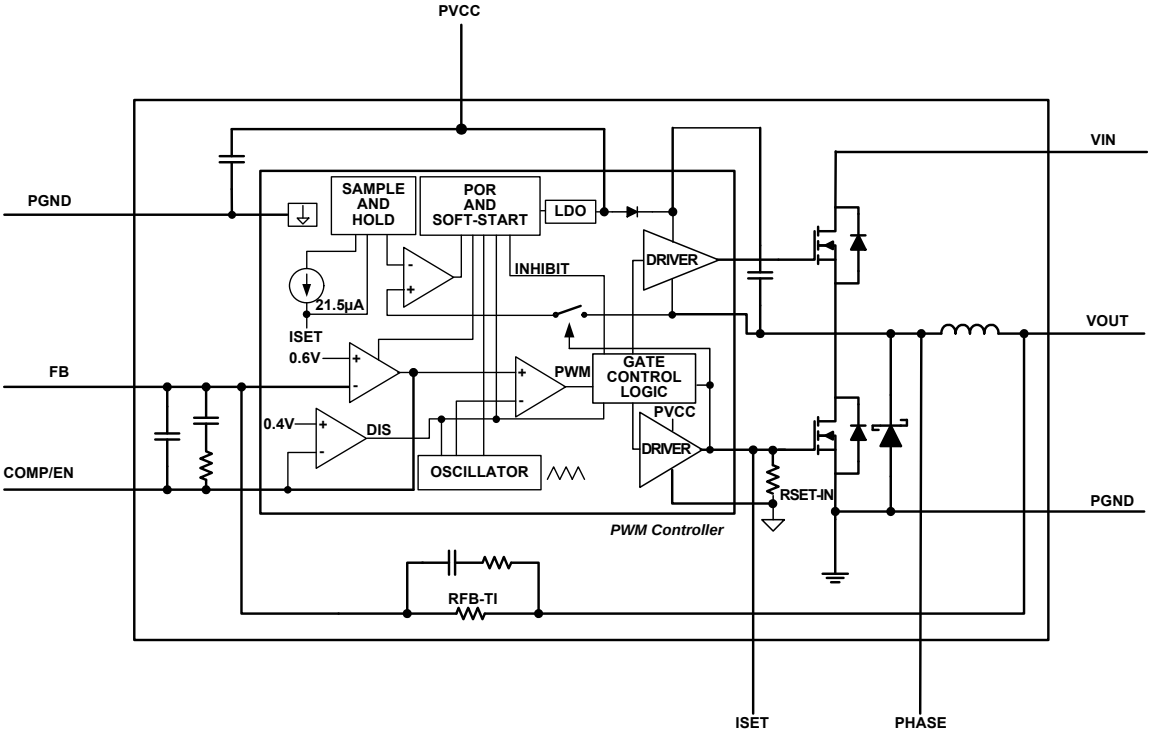
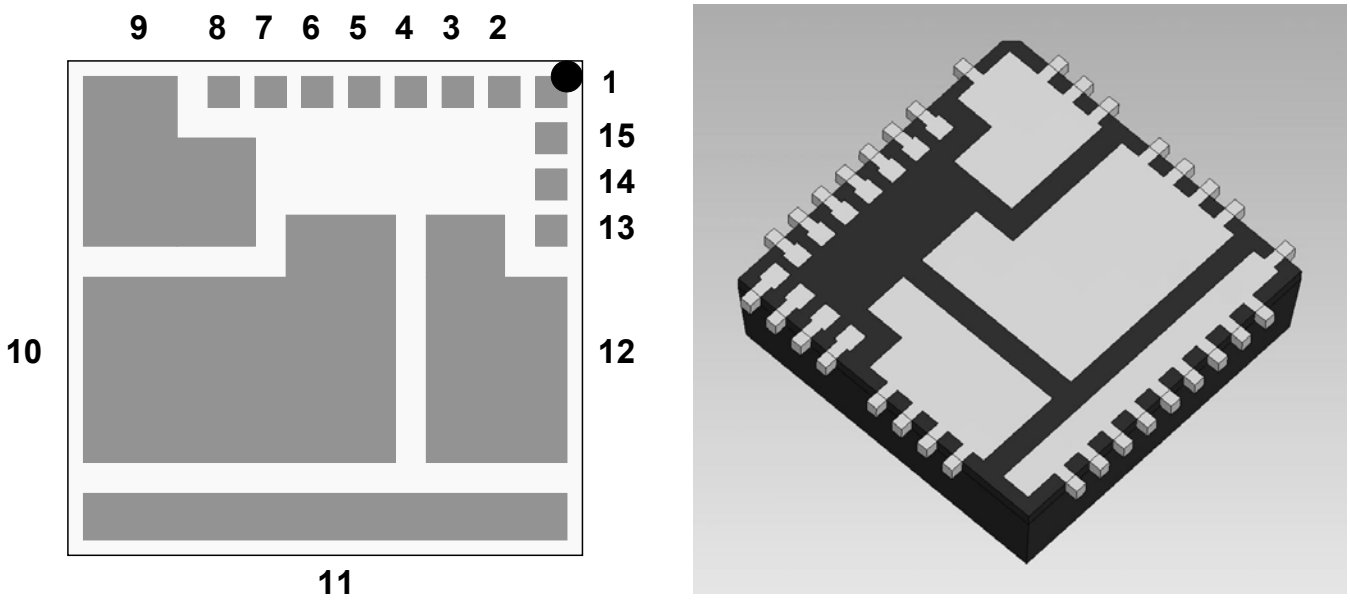


FIGURE 1. INTERNAL BLOCK DIAGRAM

Pinout

ISL8201M
(15 LD QFN)
TOP AND 3D VIEW



Pin Descriptions

PIN	SYMBOL	DESCRIPTION
1, 2, 3, 4, 11	PGND	Power ground. Connect to ground plane directly.
5	PVCC	Supply voltage. Connect 1µF ceramic capacitor to ground plane directly.
6, 8, 15	NC	Do not connect.
7	ISET	Overcurrent protection. Integrated internal 3.57kΩ resistor. Connect additional resistor between this pin and PGND pin can change initial setting.
9	VIN	Power input. Connect to input.
10	PHASE	Phase node. Node of high-side and low-side MOSFETs and output inductor connection.
12	VOUT	Power output. Connect to output.
13	COMP/EN	Compensation and enable.
14	FB	Feedback input. Connect resistor between this pin and ground for adjusting output voltage.

Absolute Maximum Ratings

$C_{OMP/EN}$ to P_{GND} . . . . . P_{GND} - 0.3V to +6V
I_{SET} to P_{GND} . . . . . P_{GND} - 0.3V to P_{VCC} + 0.3V
P_{VCC} to P_{GND} . . . . . P_{GND} - 0.3V to +15V
P_{HASE} to P_{GND} . . . . . -1.2V ~ +30V (Note 4)
V_{IN} to P_{HASE} . . . . . -1.2V ~ +30V (Note 4)

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
15 Ld QFN (Notes 5, 6)	13	2

Junction Temperature T_J . . . . . +125°C
Storage Temperature Range T_{STG} . . . . . -55°C to +125°C
Pb-Free Reflow Profile. . . . . see TB493

Recommended Operating Ratings

Input Supply Voltage (V_{IN}) . . . . . +1V to +20V
Output Voltage (V_{OUT}) . . . . . +0.6V to +5V
P_{VCC}
Fixed Supply Voltage . . . . . +5V or +12V
Wide Range Supply . . . . . +6.5V to +14.4V
Ambient Temperature Range (T_A) . . . . . -40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. V_{DS} (Drain-to-Source) specification for internal high-side and low-side MOSFET.
5. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board (i.e. 4-layer type without thermal vias – see tech brief TB379) per JEDEC standards except that the top and bottom layers assume solid planes.
6. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications

T_A = +25°C. V_{IN} = 12V, V_{OUT} = 1.5V. C_{IN} = 220µFx1, 10µF/Ceramicx2, C_{OUT} = 330µF (ESR = 10mΩ), 22µF/Ceramicx3.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS						
Input Supply Bias Current	$I_{Q(VIN)}$	I_{OUT} = 0A, V_{OUT} = 1.5V, V_{IN} = 12V, P_{VCC} = 12V	-	10	-	mA
Input In-rush Current	I_{inRush}	I_{OUT} = 0A, V_{OUT} = 1.5V, V_{IN} = 12V, P_{VCC} = 12V	-	140	-	mA
Input Supply Current	$I_{S(VIN)}$	I_{OUT} = 10A, V_{OUT} = 1.5V, V_{IN} = 12V, P_{VCC} = 12V	-	1.48	-	A
OUTPUT CHARACTERISTICS						
Output Continuous Current Range	$I_{OUT(DC)}$	V_{IN} = 12V, V_{OUT} = 1.5V	0	-	10	A
Line Regulation Accuracy	$\Delta V_{OUT}/\Delta V_{IN}$	V_{OUT} = 1.5V, I_{OUT} = 0A, V_{IN} =3.3V to 20V, P_{VCC} = 12V	-	0.1	-	%
Load Regulation Accuracy	$\Delta V_{OUT}/\Delta I_{OUT}$	I_{OUT} = 0A to 10A, V_{OUT} = 1.5V, V_{IN} = 12V, P_{VCC} = 12V	-	0.5	-	%
Peak-to-Peak Output Ripple Voltage	ΔV_{OUT}	I_{OUT} = 10A, V_{OUT} = 1.5V, V_{IN} = 12V, P_{VCC} = 12V	-	20	-	mV
DYNAMIC CHARACTERISTICS						
Voltage Change For Positive Load Step	ΔV_{OUT-DP}	I_{OUT} = 0A to 5A. Current slew rate = 2.5A/µs, V_{IN} = 12V, V_{OUT} = 1.5V, P_{VCC} = 12V	-	36	-	mV
Voltage Change For Negative Load Step	ΔV_{OUT-DN}	I_{OUT} = 0A to 5A. Current slew rate = 2.5A/µs, V_{IN} = 12V, V_{OUT} = 1.5V, P_{VCC} = 12V	-	39	-	mV
CONTROLLER						
Shutdown PVCC Supply Current	I_{PVCC_S}	P_{VCC} = 12V; Disabled (Note 7)	4	5.2	7	mA
Supply Voltage	P_{VCC}	Fixed 5V supply	4.5	5.0	5.5	V
		Wide range supply	6.5	12.0	14.4	V
P_{VCC} Operating Current	I_{PVCC}	I_{OUT} = 10A, V_{OUT} = 1.5V V_{IN} = 12V				
		5V supply	-	22	-	mA
		12V supply	-	47	-	mA
Rising P_{VCC} Threshold	V_{PORR}	(Note 7)	3.9	4.1	4.3	V
P_{VCC} Power-On-Reset Threshold Hysteresis	V_{PORH}	(Note 7)	0.30	0.35	0.40	V
Oscillator Frequency	F_{OSC}	(Note 7)	510	600	660	kHz

Electrical Specifications T_A = +25°C. V_{IN} = 12V, V_{OUT} = 1.5V. C_{IN} = 220µFx1, 10µF/Ceramicx2, C_{OUT} = 330µF (ESR = 10mΩ), 22µF/Ceramicx3. **(Continued)**

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Internal Resistor Between V_{OUT} and FB Pins	R_{FB-TI}		9.66	9.76	9.85	kΩ
Disabled Threshold Voltage (COMP/EN)	V_{ENDIS}	(Note 7)	0.375	0.4	0.425	V
Reference Voltage	V_{REF}	(Note 7)	-	0.6	-	V
Reference Voltage Tolerance		0°C to +70°C (Note 7)	-1.0	-	+1.0	%
		-40°C to +85°C (Note 7)	-1.5	-	+1.5	%
FAULT PROTECTION						
Internal Resistor Between I_{SET} and P_{GND} Pins	R_{SET-IN}		-	3.57	-	kΩ
I_{SET} Current Source	I_{SET}	(Note 7)	18.0	21.5	23.5	µA

NOTE:

7. Parameters are 100% tested for internal IC prior to module assembly.

Typical Performance Characteristics

Efficiency Performance

T_A = +25°C, V_{IN} = P_{VCC} (P_{VCC} = 5V for 18V_{IN}), C_{IN} = 220µFx1, 10µF/Ceramicx2, C_{OUT} = 330µF (ESR = 10mΩ), 22µF/Ceramicx3. The efficiency equation is: $\text{Efficiency} = \frac{\text{Output Power}}{\text{Input Power}} = \frac{P_{OUT}}{P_{IN}} = \frac{(V_{OUT} x I_{OUT})}{(V_{IN} x I_{IN})}$

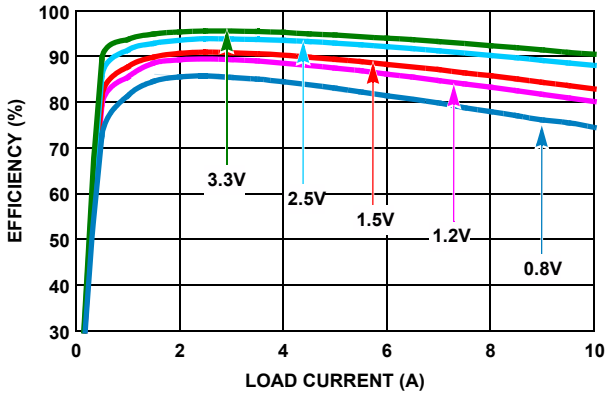


FIGURE 2. EFFICIENCY vs LOAD CURRENT ($5V_{IN}$)

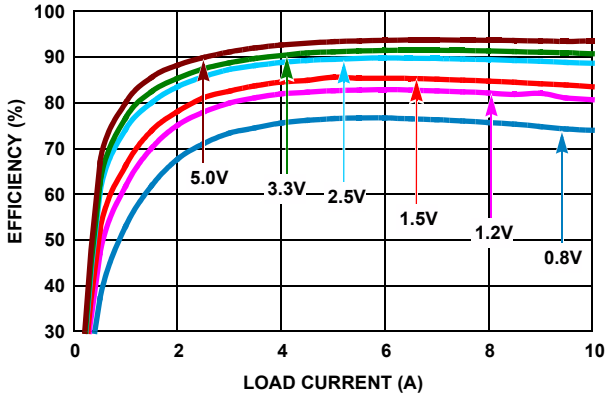


FIGURE 3. EFFICIENCY vs LOAD CURRENT ($12V_{IN}$)

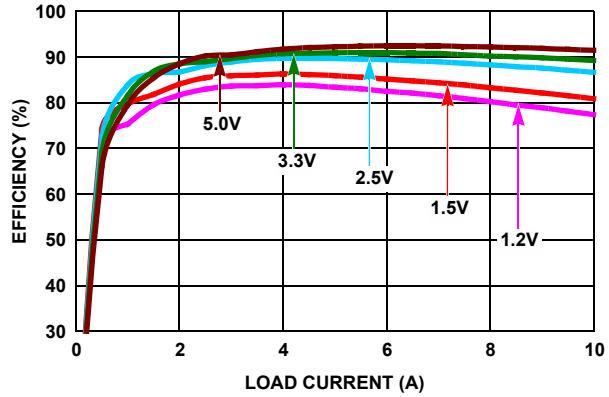


FIGURE 4. EFFICIENCY vs LOAD CURRENT ($18V_{IN}$)

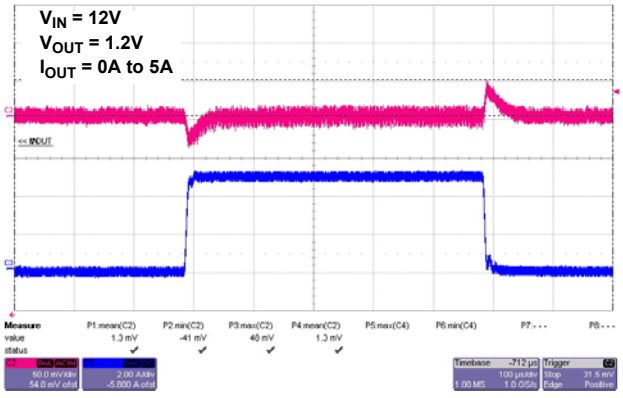


FIGURE 5. 1.2V TRANSIENT RESPONSE

Typical Performance Characteristics (Continued)

Transient Response Performance

T_A = +25°C, V_{IN} = 12V, V_{OUT} = 1.5V, P_{VCC} = 12V, C_{IN} = 220µFx1, 10µF/Ceramicx2, C_{OUT} = 330µF (ESR = 10mΩ), 22µF/Ceramicx3 I_{OUT} = 0-5A (10A), Current slew rate = 2.5A/µs

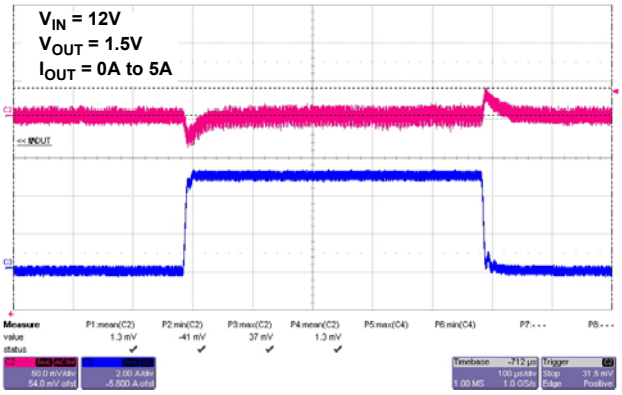


FIGURE 6. 1.5V TRANSIENT RESPONSE

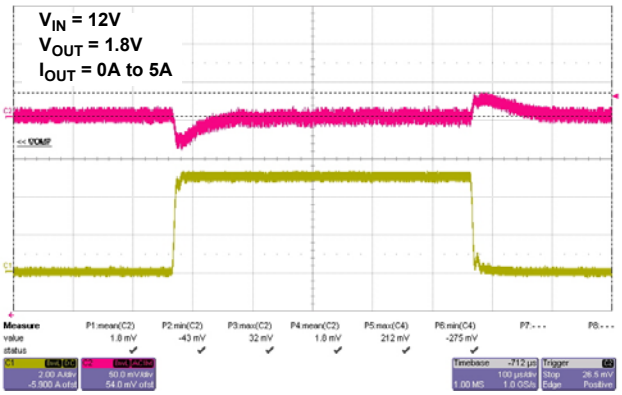


FIGURE 7. 1.8V TRANSIENT RESPONSE

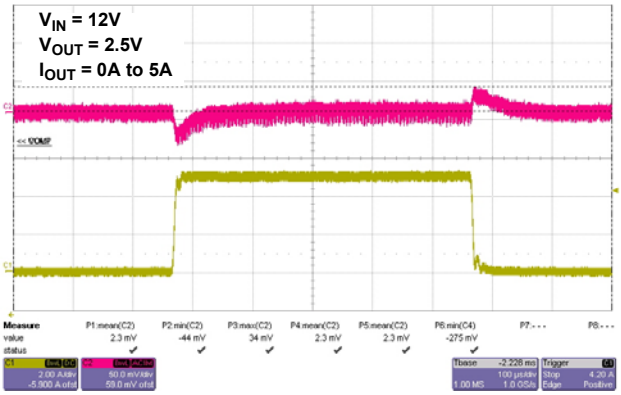


FIGURE 8. 2.5V TRANSIENT RESPONSE

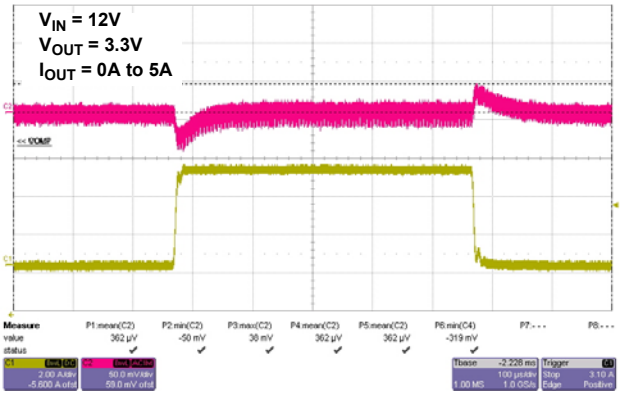


FIGURE 9. 3.3V TRANSIENT RESPONSE

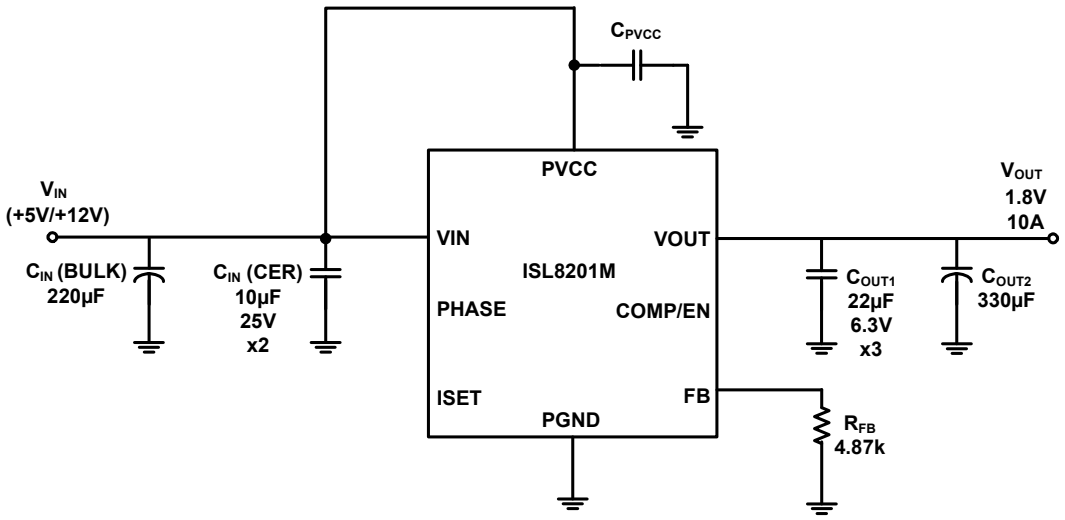


FIGURE 10. TYPICAL APPLICATION

Pin Functions

PGND (Pins 1, 2, 3, 4, 11)

Power ground pin for signal, input, and output return path. PGND needs to connect to one (or more) ground plane(s) immediately, which is recommended to minimize the effect of switching noise, copper losses, and maximize heat dissipation.

PVCC (Pin 5)

This pin provides the bias supply for ISL8201M, as well as the low-side MOSFET's gate and high-side MOSFET's gate. If PVCC rises above 6.5V, an internal 5V regulator will supply to the internal logics bias (but high-side and low-side MOSFET gate will still be sourced by PVCC). Connect a well decoupled +5V or +12V supply to this pin.

NC (Pins 6, 8, 15)

These pins have no function; do not connect.

ISET (Pin 7)

The ISET pin is the input for the overcurrent protection (OCP) setting, which compares the $r_{DS(ON)}$ of the low-side MOSFET to set the overcurrent threshold. The ISL8201M has an initial protect overcurrent limit. It has an integrated internal 3.57kΩ resistor (R_{SET-IN}) between the ISET and PGND pins, which can prevent significant overcurrent impact to the module. One can also connect an additional resistor R_{SET-EX} between the ISET pin and the PGND pin in order to reduce the current limit point by paralleling.

VIN (Pin 9)

Power input pin. Apply input voltage between the VIN pin and PGND pin. It is recommended to place an input decoupling capacitor directly between the VIN pin and the PGND pin. The input capacitor should be placed as closely as possible to the module.

PHASE (Pin 10)

The PHASE pin is the switching node between the high and low-side MOSFET. It also returns the current path for the high-side MOSFET driver and detects the low-side MOSFET drain voltage for the overcurrent limits point.

VOUT (Pin 12)

Power output pin. Apply output load between this pin and the PGND pin. It is recommended to place a high frequency output decoupling capacitor directly between the VOUT pin and the PGND pin. The output capacitor should be placed as closely as possible to the module.

COMP/EN (Pin 13)

This is the multiplexed pin of the ISL8201M. During soft-start and normal converter operation, this pin represents the output of the error amplifier. Use COMP/EN in combination with the FB pin to compensate for the voltage control feedback loop of the converter. Pulling COMP/EN low (V_{ENDIS} = 0.4V nominal) will disable (shut-down) the controller, which causes the oscillator to stop, and the high-side gate and low-side gate of the MOSFETs outputs to be held low. The external pull-down device will initially need to overcome a maximum of 5mA of COMP/EN output current. However, once the controller is disabled, the COMP/EN output will also be disabled, thus only a 20µA current source will continue to draw current.

FB (Pin 14)

The FB pin is the output voltage adjustment of the ISL8201M. It will regulate to 0.6V at the FB pin with respect to the PGND pin. The ISL8201M has an integrated voltage dividing resistor. This is a precision 9.76kΩ resistor (R_{FB-TI}) between the VOUT and FB pins. Different output voltages can be programmed with additional resistors between FB to PGND.

Reference Circuitry For General Applications

Typical Application with Single Power Supply

Figure 11 shows the ISL8201M application schematic for input voltage +5V or +12V. The PVCC pin can connect to the input supply directly.

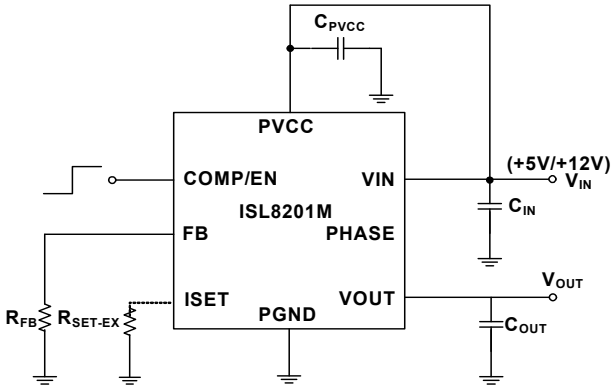


FIGURE 11. TYPICAL APPLICATION SCHEMATIC

Typical Application with Separated Power Supply

Figure 12 shows the ISL8201M application schematic for wide input voltages from +1V to +20V. The P_{VCC} supply can source +5V/+12V or +6.5V to 14.4V.

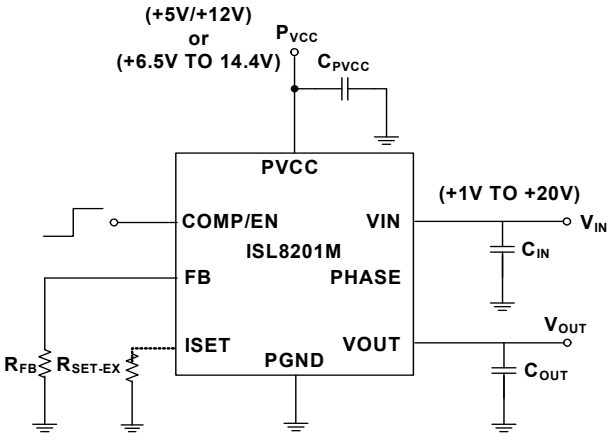


FIGURE 12. WIDE INPUT VOLTAGE APPLICATION SCHEMATIC

Applications Information

The typical ISL8201M application schematic for input voltage +5V or +12V is shown in Figure 11. External component selection is primarily determined by the maximum load current and input/output voltage.

Programming the Output Voltage

The ISL8201M has an internal 0.6V ±1.5% reference voltage. Programming the output voltage requires a dividing resistor (R_{FB}). The output voltage can be calculated as shown in Equation 1:

$$V_{OUT} = 0.6 \times \left(1 + \frac{9.76k}{R_{FB}}\right) \quad \text{(EQ. 1)}$$

Note: ISL8201M has integrated 9.76kΩ resistance into the module (dividing resistor for top side). The resistance corresponding to different output voltages is as shown in Table 1:

TABLE 1. RESISTANCE TO OUTPUT VOLTAGES

V_{OUT}	0.6V	1.05V	1.2V	1.5V
R_{FB}	open	13k	9.76k	6.49k
V_{OUT}	1.8V	2.5V	3.3V	5V
R_{FB}	4.87k	3.09k	2.16k	1.33k

Initialization (POR and OCP Sampling)

Figure 13 shows a start-up waveform of ISL8201M. The power-on-reset (POR) function continually monitors the bias voltage at the PVCC pin. Once the rising POR threshold has exceeded 4V (V_{PORR} nominal), the POR function initiates the overcurrent protection (OCP) sample and hold operation (while COMP/EN is ~1V). When the sampling is complete, V_{OUT} begins the soft-start ramp.

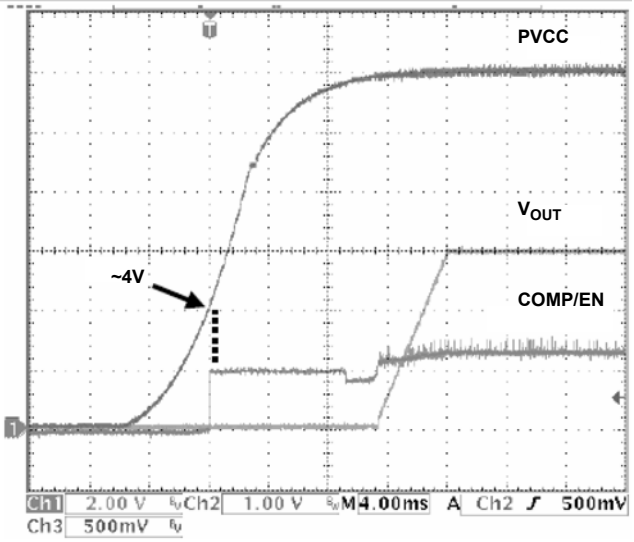


FIGURE 13. POR AND SOFT-START OPERATION

If the COMP/EN pin is held low during power-up, the initialization will be delayed until the COMP/EN is released and its voltage rises above the V_{ENDIS} trip point.

Figures 14 and 15 show a typical power-up sequence in more detail. The initialization starts at t_0, when either P_{VCC} rises above V_{PORR}, or the COMP/EN pin is released (after POR). The COMP/EN will be pulled up by an internal 20µA current source, however, the timing will not begin until the COMP/EN exceeds the V_{ENDIS} trip point (at t_1). The external capacitance of the disabling device, as well as the compensation capacitors, will determine how quickly the 20µA current source will charge the COMP/EN pin. With typical values, it should add a small delay compared to the soft-start times. The COMP/EN will continue to ramp to ~1V.

From t_1, there is a nominal 6.8ms delay, which allows the PVCC pin to exceed 6.5V (if rising up towards 12V), so that the internal bias regulator can turn on cleanly. At the same time, the ISET pin is initialized by disabling the low-side gate driver and drawing I_{SET} (nominal 21.5µA) through R_{SETI}. This sets up a voltage that will represent the I_{SET} trip point. At t_2, there is a variable time period for the OCP sample and hold operation (0.0ms to 3.4ms nominal; the longer time occurs with the higher overcurrent setting). The sample and hold uses a digital counter and DAC to save the voltage, so the stored value does not degrade, as long as the P_{VCC} is above V_{PORR} (See "Overcurrent Protection (OCP)" on page 10 for more details on the equations and variables). Upon the completion of sample and hold at t_3, the soft-start operation is initiated, and the output voltage ramps up between t_4 and t_5.

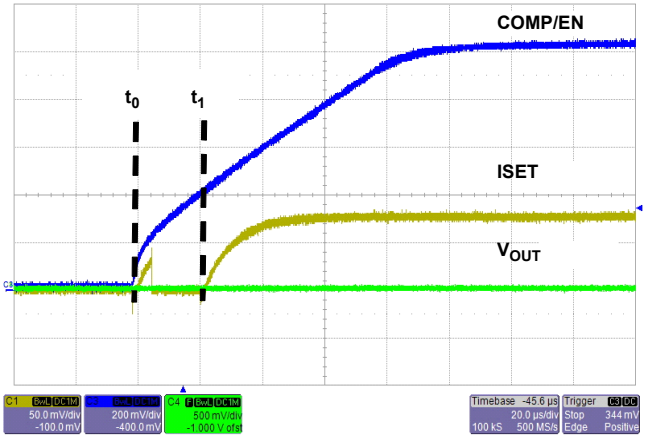


FIGURE 14. I_{SET} AND SOFT-START OPERATION

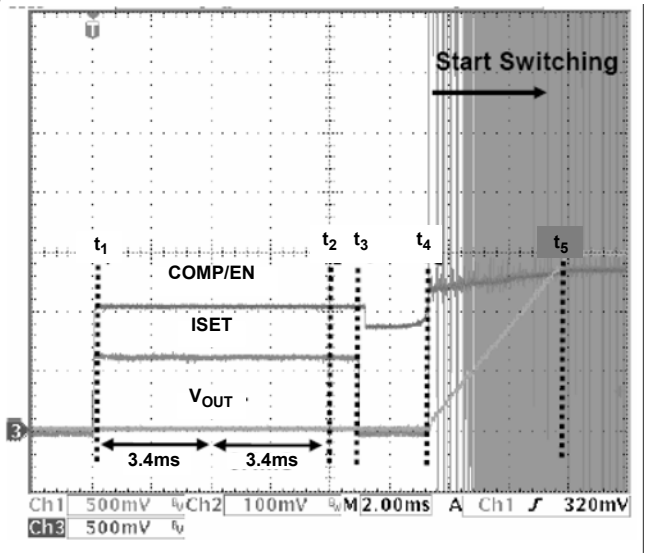


FIGURE 15. I_{SET} AND SOFT-START OPERATION

Soft-Start and Pre-Biased Outputs

The soft-start internally ramps the reference on the non-inverting terminal of the error amp from 0V to 0.6V in a nominal 6.8ms. The output voltage will thus follow the ramp, from zero to final value, in the same 6.8ms (the actual ramp seen on the V_{OUT} will be less than the nominal time), due to some initialization timing, between t_3 and t_4.

The ramp is created digitally, so there will be 64 small discrete steps. There is no simple way to change this ramp rate externally.

After an initialization period (t_3 to t_4), the error amplifier (COMP/EN pin) is enabled and begins to regulate the converter's output voltage during soft-start. The oscillator's triangular waveform is compared to the ramping error amplifier voltage. This generates PHASE pulses of increasing width that charge the output capacitors. When the internally generated soft-start voltage exceeds the reference voltage (0.6V), the soft-start is complete and the output should be in regulation at the expected voltage. This method provides a rapid and controlled output voltage rise; there is no large in-rush current charging the output capacitors. The entire start-up sequence from POR typically takes up to 17ms; up to 10.2ms for the delay and OCP sample and 6.8ms for the soft-start ramp.

Figure 16 shows the normal curve for start-up; initialization begins at t_0, and the output ramps between t_1 and t_2. If the output is pre-biased to a voltage less than the expected value (as shown Figure 17), the ISL8201M will detect that condition. Neither internal MOSFET will turn on until the soft-start ramp voltage exceeds the output; V_{OUT} starts seamlessly ramping from there.

If the output is pre-biased to a voltage above the expected value (as shown Figure 18), neither MOSFET will turn on until the end of the soft-start, at which time it will pull the output voltage down to the final value. Any resistive load connected to the output will help pull down the voltage (at the RC rate of the R of the load and the C of the output capacitance).

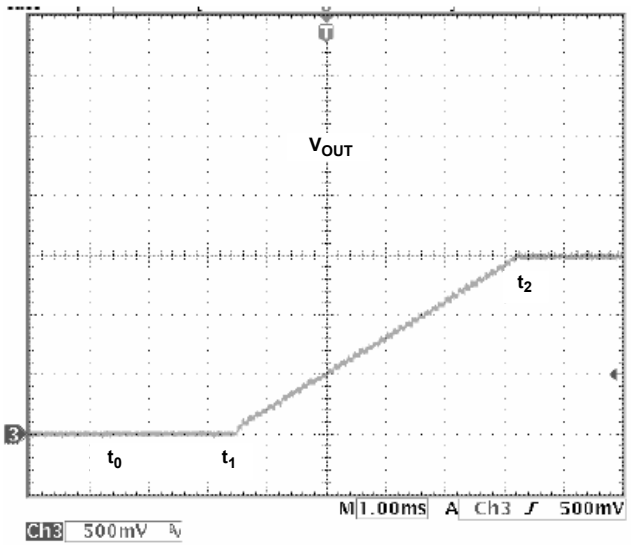


FIGURE 16. NORMAL START-UP

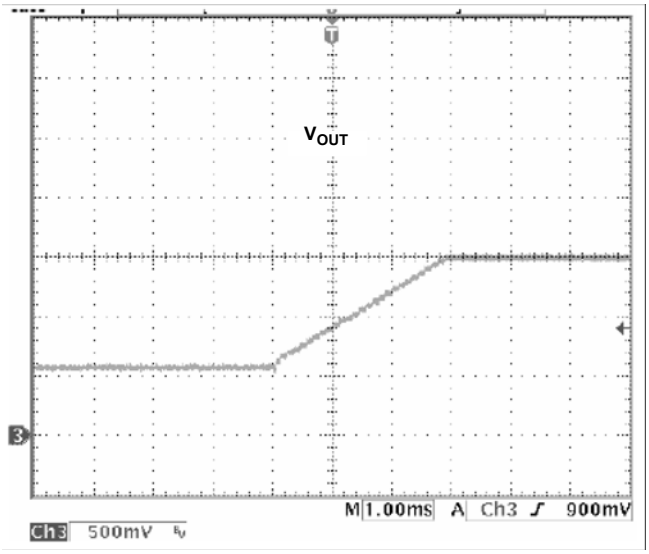


FIGURE 17. PRE-BIASED START-UP

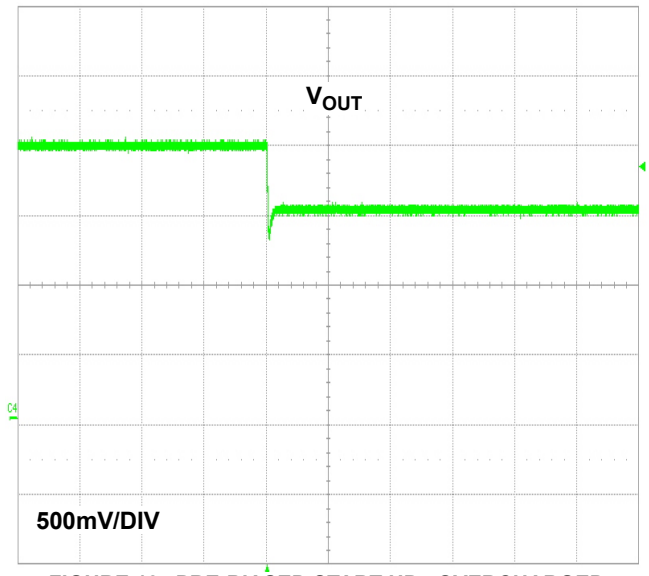


FIGURE 18. PRE-BIASED START-UP - OVERCHARGED

If the V_{IN} for the synchronous buck converter is from a different supply that comes up after P_{VCC}, the soft-start will go through its cycle, but with no output voltage ramp. When V_{IN} turns on, the output will follow the ramp of the V_{IN} from zero up to the final expected voltage (at close to 100% duty cycle, with COMP/EN pin >4V). If V_{IN} is too fast, there may be excessive in-rush current charging the output capacitors (only the beginning of the ramp, from zero to V_{OUT} matters here). If this is not acceptable, then consider changing the sequencing of the power supplies, sharing the same supply, or adding sequencing logic to the COMP/EN pin to delay the soft-start until the V_{IN} supply is ready (see "Input Voltage Considerations" on page 11).

If ISL8201M is disabled after soft-start (by pulling COMP/EN pin low), and afterwards enabled (by releasing the COMP/EN pin), then the full initialization (including OCP sample) will take place. However, there is no new OCP sampling during overcurrent retries. If the output is shorted to GND during soft-start, the OCP will handle it, as described in the next section.

Overcurrent Protection (OCP)

The overcurrent function protects the converter from a shorted output by using the low-side MOSFET ON-resistance, $r_{DS(ON)}$, to monitor the current. A resistor (R_{SET}) programs the overcurrent trip level.

This method enhances the converter's efficiency and reduces cost by eliminating a current sensing resistor. If overcurrent is detected, the output immediately shuts off. It cycles the soft-start function in a hiccup mode (2 dummy soft-start time-outs, then up to one real one) to provide fault protection. If the shorted condition is not removed, this cycle will continue indefinitely.

Following POR (and 6.8ms delay), the ISL8201M initiates the overcurrent protection sample and hold operation. The low-side gate driver is disabled to allow an internal 21.5µA current source to develop a voltage across R_{SET}. The ISL8201M samples this voltage (which is referenced to the PGND pin) at the ISET pin, and holds it in a counter and DAC combination. This sampled voltage is held internally as the overcurrent set point, for as long as power is applied, or until a new sample is taken after coming out of a shut-down.

The actual monitoring of the low-side MOSFET ON-resistance starts 200ns (nominal) after the edge of the internal PWM logic signal (that creates the rising external low-side gate signal). This is done to allow the gate transition noise and ringing on the PHASE pin to settle out before monitoring. The monitoring ends when the internal PWM edge (and thus low-side gate signal) goes low. The OCP can be detected anywhere within the above window.

If the converter is running at high duty cycles around 75% for 600kHz operation, then the low-side gate pulse width may not be wide enough for the OCP to properly sample the $r_{DS(ON)}$. For those cases, if the low-side gate signal is too narrow (or not there at all) for 3 consecutive pulses, then the third pulse will be stretched and/or inserted to the 425ns minimum width. This allows for OCP monitoring every third pulse under this condition. This can introduce a small pulse-width error on the output voltage, which will be corrected on the next pulse; and the output ripple voltage will have an unusual 3-clock pattern, which may look like jitter.

The overcurrent function will trip at a peak inductor current (I_{PEAK}) determined by Equation 2:

$$I_{PEAK} = \frac{2 \times I_{SET} \times R_{SET}}{r_{DS(ON)}} \quad \text{(EQ. 2)}$$

where:

I_{SET} is the internal I_{SET} current source (21.5µA typical).

R_{SET} is equivalent resistance between ISET and PGND pins.

$r_{DS(ON)}$ is typically 6.1mΩ at (V_{PVCC} = V_{GS} = 10V, I_{DS} = 30A) and 9mΩ at (V_{PVCC} = V_{GS} = 4.5V, I_{DS} = 30A).

Note: ISL8201M has integrated 3.57kΩ resistance (R_{SET-IN}). Therefore, the equivalent resistance of R_{SET} can be expressed in Equation 3:

$$R_{SET} = \frac{R_{SET-EX} \times R_{SET-IN}}{R_{SET-EX} + R_{SET-IN}} \quad \text{(EQ. 3)}$$

The scale factor of 2 doubles the trip point of the MOSFET voltage drop, compared to the setting on the R_{SET} resistor. The OC trip point varies in a system mainly due to the MOSFET $r_{DS(ON)}$ variations (i.e. over process, current and temperature). To avoid overcurrent tripping in the normal operating load range, find the R_{SET} resistor from Equation 4, and with Steps 1 to 3:

1. The maximum $r_{DS(ON)}$ at the highest junction temperature
2. The minimum I_{SET} from the "Electrical Specifications" table on page 3.

3. Determine I_{PEAK} for:

$$I_{PEAK} > I_{OUT(MAX)} + \frac{(\Delta I_L)}{2} \quad \text{(EQ. 4)}$$

where ΔI_L is the output inductor ripple current. In a high input voltage, high output voltage application, such as 20V input to 5V output, the inductor ripple becomes excessive due to the fixed internal inductor value. In such applications, the output current will be limited from the rating to approximately 70% of the module's rated current.

The relationships between the external R_{SET} values and the typical output current $I_{OUT(MAX)}$ OCP levels are as follows:

TABLE 2.

R_{SET} (Ω)	OCP (A) AT V_{IN} = 12V, P_{VCC} = 5V	OCP (A) AT V_{IN} = 12V P_{VCC} = 12V
OPEN	13.3	17.3
50k	12.6	16.6
20k	11.4	14.9
10k	10.2	13.3
5k	7.6	10.3
3k	6.3	8.3
2k	4.9	6.7

The range of allowable voltages detected (2 x I_{SET} x R_{SET}) is 0mV to 475mV. If the voltage drop across R_{SET} is set too low, then this can cause almost continuous OCP tripping and retry. It will also be very sensitive to system noise and in-rush current spikes, so it should be avoided. The maximum usable setting is around 0.2V across R_{SET} (0.4V across the MOSFET); values above this might disable the protection. Any voltage drop across R_{SET} that is greater than 0.3V (0.6V MOSFET trip point) will disable the OCP. Note that conditions during power-up or during a retry may look different than normal operation. During power-up in a 12V system, the ISL8201M starts operation just above 4V; if the supply ramp is slow, the soft-start ramp might be over well before 12V is reached. Therefore, with low-side gate drive voltages, the $r_{DS(ON)}$ of the MOSFET will be higher during power-up, effectively lowering the OCP trip. In addition, the ripple current will likely be different at a lower input voltage. Another factor is the digital nature of the soft-start ramp. On each discrete voltage step, there is in effect, a small load transient and a current spike to charge the output capacitors. The height of the current spike is not controlled, however, it is affected by the step size of the output and the value of the output capacitors, as well as the internal error amp compensation. Therefore, it is possible to trip the overcurrent with in-rush current, in addition to the normal load and ripple considerations.

Figure 19 shows the output response during a retry of an output shorted to PGND. At time t_0, the output has been turned off due to sensing an overcurrent condition. There are two internal soft-start delay cycles (t_1 and t_2) to allow the MOSFETs to cool down in order to keep the average power dissipation in retry at an acceptable level. At time t_2, the output starts a normal soft-start cycle, and the output tries to ramp. If the short is still applied and the current reaches the I_{SET} trip point any time during the soft-start ramp period, the output will shut off and return to time t_0 for another delay cycle. The retry period is thus two dummy soft-start cycles plus one variable one (which depends on how long it takes to trip the sensor each time). Figure 19 shows an example where the output gets about half-way up before shutting down; therefore, the retry (or hiccup) time will be around 17ms. The minimum should be nominally 13.6ms and the maximum 20.4ms. If the short condition is finally removed, the output should ramp up normally on the next t_2 cycle.

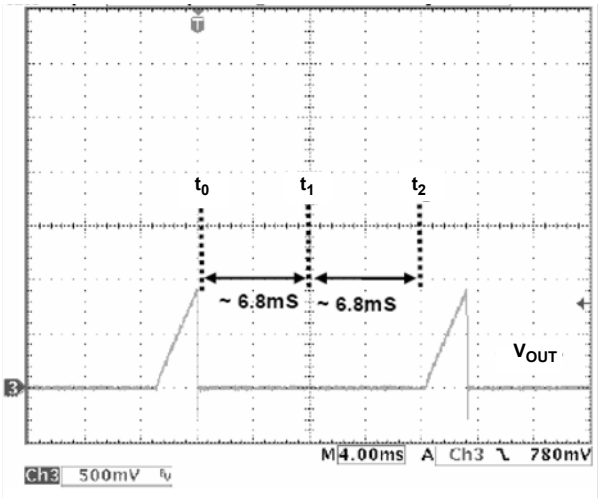


FIGURE 19. OVERCURRENT RETRY OPERATION

Starting up into a shorted load looks the same as a retry into that same shorted load. In both cases, OCP is always enabled during soft-start; once it trips, it will go into retry (hiccup) mode. The retry cycle will always have two dummy time-outs, plus whatever fraction of the real soft-start time passes before the detection and shutoff. At that point, the logic immediately starts a new two dummy cycle time-out.

Input Voltage Considerations

Figure 12 shows a standard configuration where P_{VCC} is either 5V (±10%) or 12V (±20%). In each case, the gate drivers use the P_{VCC} voltage for low-side gate and high-side gate driver. In addition, P_{VCC} is allowed to work anywhere from 6.5V up to the 14.4V maximum. The P_{VCC} range between 5.5V and 6.5V is not allowed for long-term reliability reasons, but transitions through it to voltages above 6.5V are acceptable.

There is an internal 5V regulator for bias, which turns on between 5.5V and 6.5V. Some of the delay after POR is there to allow a typical power supply to ramp-up past 6.5V before the soft-start ramps begins. This prevents a disturbance on the output, due to the internal regulator turning on or off. If the transition is slow (not a step change), the disturbance should be minimal. Thus, while the recommendation is to not have the output enabled during the transition through this region, it may be acceptable. The user should monitor the output for their

application to see if there is any problem. If P_{VCC} powers up first and the V_{IN} is not present by the time the initialization is done, then the soft-start will not be able to ramp the output, and the output will later follow part of the V_{IN} ramp when it is applied. If this is not desired, then change the sequencing of the supplies, or use the COMP/EN pin to disable V_{OUT} until both supplies are ready.

Figure 20 shows a simple sequencer for this situation. If P_{VCC} powers up first, Q_1 will be off, and R_3 pulling to P_{VCC} will turn Q_2 on, keeping the ISL8201M in shut-down. When V_{IN} turns on, the resistor divider R_1 and R_2 determines when Q_1 turns on, which will turn off Q_2 and release the shut-down. If V_{IN} powers up first, Q_1 will be on, turning Q_2 off; so the ISL8201M will start-up as soon as P_{VCC} comes up. The V_{ENDIS} trip point is 0.4V nominal, so a wide variety of N-MOSFET or NPN BJT or even some logic IC's can be used as Q_1 or Q_2. However, Q_2 must be low leakage when off (open-drain or open-collector) so as not to interfere with the COMP output. Q_2 should also be placed near the COMP/EN pin.

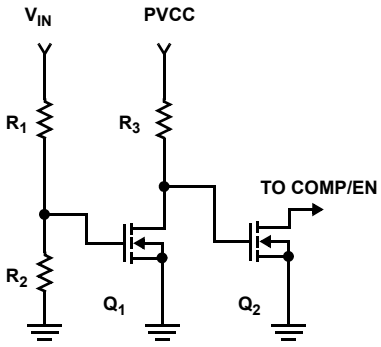


FIGURE 20. SEQUENCE CIRCUIT

The V_{IN} range can be as low as ~1V (for V_{OUT} as low as the 0.6V reference) and as high as 20V. There are some restrictions for running high V_{IN} voltage. The maximum PHASE voltage is 30V. The VIN + P_{VCC} + any ringing or other transients on the PHASE pin must be less than 30V. If V_{IN} is 20V, it is recommended to limit P_{VCC} to 5V.

Switching Frequency

The switching frequency is a fixed 600kHz clock, which is determined by the internal oscillator. However, all of the other timing mentioned (POR delay, OCP sample, soft-start, etc.) is independent of the clock frequency (unless otherwise noted).

Selection of the Input Capacitor

The input filter capacitor should be based on how much ripple the supply can tolerate on the DC input line. The larger the capacitor, the less ripple expected but consideration should be taken for the higher surge current during power-up. The ISL8201M provides the soft-start function that controls and limits the current surge. The value of the input capacitor can be calculated by Equation 5:

$$C_{IN} = \frac{I_{IN} \times \Delta t}{\Delta V} \quad \text{(EQ. 5)}$$

Where:

C_{IN} is the input capacitance (µF)

I_{IN} is the input current (A)

Δt is the turn on time of the high-side switch (µs)

ΔV is the allowable peak-to-peak voltage (V)

In addition to the bulk capacitance, some low Equivalent Series Inductance (ESL) ceramic capacitance is recommended to decouple between the drain terminal of the high-side MOSFET and the source terminal of the low-side MOSFET. This is used to reduce the voltage ringing created by the switching current across parasitic circuit elements.

Output Capacitors

The ISL8201M is designed for low output voltage ripple. The output voltage ripple and transient requirements can be met with bulk output capacitors (C_{OUT}) with low enough Equivalent Series Resistance (ESR). C_{OUT} can be a low ESR tantalum capacitor, a low ESR polymer capacitor or a ceramic capacitor. The typical capacitance is 330µF and decoupled ceramic output capacitors are used. The internally optimized loop compensation provides sufficient stability margins for all ceramic capacitor applications with a recommended total value of 400µF. Additional output filtering may be needed if further reduction of output ripple or dynamic transient spike is required.

Layout Guide

To achieve stable operation, low losses, and good thermal performance some layout considerations are necessary.

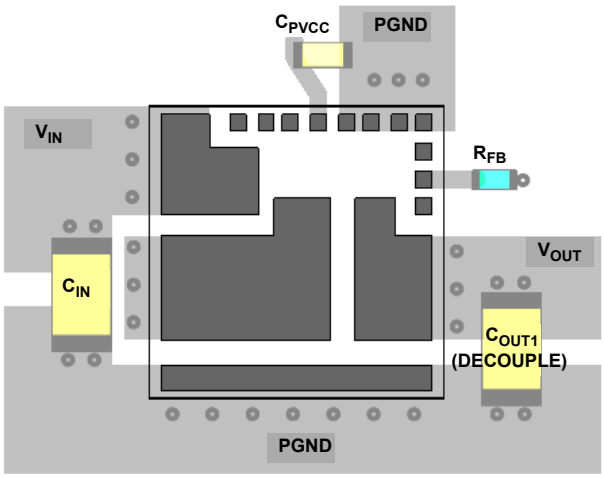


FIGURE 21. RECOMMENDED LAYOUT

- The ground connection between pin 11 and pins 1 to 4 should be a solid ground plane under the module.
- Place a high frequency ceramic capacitor between (1) VIN and PGND (pin 11) and (2) PVCC and PGND (pins 1 to 4) as

close to the module as possible to minimize high frequency noise.

- Use large copper areas for power path (VIN, PGND, VOUT) to minimize conduction loss and thermal stress. Also, use multiple vias to connect the power planes in different layers.
- Keep the trace connection to the feedback resistor short.
- Avoid routing any sensitive signal traces near the PHASE node.

Thermal Considerations

Experimental power loss curves along with θ_{JA} from thermal modeling analysis can be used to evaluate the thermal consideration for the module. The derating curves are derived from the maximum power allowed while maintaining the temperature below the maximum junction temperature of +125°C. In actual application, other heat sources and design margin should be considered.

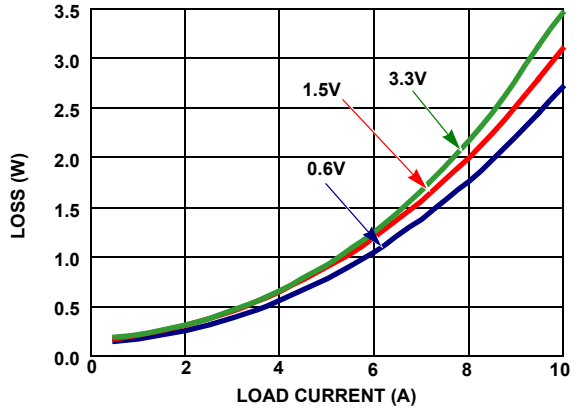


FIGURE 22. POWER LOSS vs LOAD CURRENT ($5V_{IN}$)

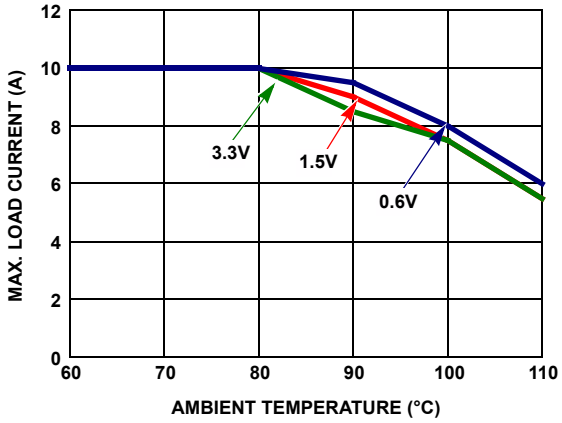


FIGURE 23. DERATING CURVE ($5V_{IN}$)

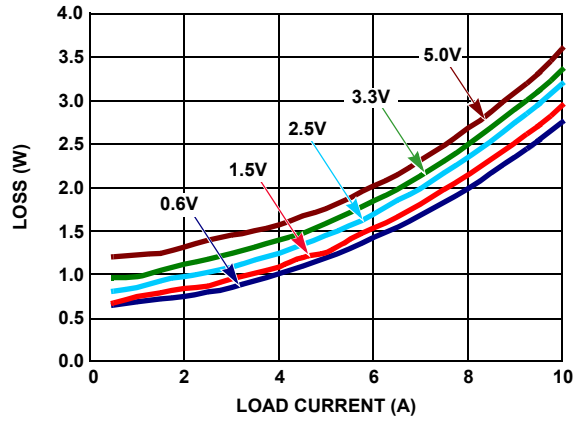


FIGURE 24. POWER LOSS vs LOAD CURRENT ($12V_{IN}$)

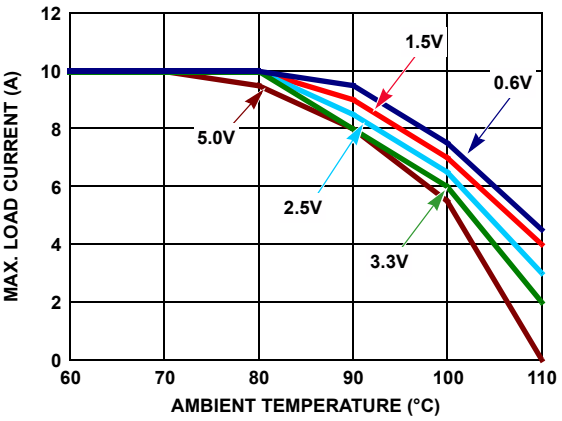


FIGURE 25. DERATING CURVE ($12V_{IN}$)

Package Description

The structure of ISL8201M belongs to the Quad Flat-pack No-lead package (QFN). This kind of package has advantages, such as good thermal and electrical conductivity, low weight and small size. The QFN package is applicable for surface mounting technology and is being more readily used in the industry. The ISL8201M contains several types of devices, including resistors, capacitors, inductors and control ICs. The ISL8201M is a copper leadframe based package with exposed copper thermal pads, which have good electrical and thermal conductivity. The copper leadframe and multi component assembly is overmolded with polymer mold compound to protect these devices.

The package outline and typical PCB layout pattern design and typical stencil pattern design are shown in the package outline drawing L15.15x15 on page 15. The module has a small size of 15mmx15mm x 3.5mm. Figure 26 shows typical reflow profile parameters. These guidelines are general design rules. Users could modify parameters according to their application.

PCB Layout Pattern Design

The bottom of ISL8201M is leadframe footprint, which is attached to PCB by surface mounting process. The PCB layout pattern is shown in the Package Outline Drawing L15.15x15 on page 15. The PCB layout pattern is essentially 1:1 with the QFN exposed pad and I/O termination dimensions, except for the PCB lands being a slightly extended distance of 0.2mm (0.4mm max) longer than the QFN terminations, which allows for solder filleting around the periphery of the package. This ensures a more complete and inspectable solder joint. The thermal lands on the PCB layout should match 1:1 with the package exposed die pads.

Thermal Vias

A grid of 1.0mm to 1.2mm pitch thermal vias, which drops down and connects to buried copper plane(s), should be placed under the thermal land. The vias should be about 0.3mm to 0.33mm in diameter with the barrel plated to about 1.0 ounce copper. Although adding more vias (by decreasing via pitch) will improve the thermal performance, diminishing returns will be seen as more and more vias are added. Simply use as many vias as practical for the thermal land size and your board design rules allow.

Stencil Pattern Design

Reflowed solder joints on the perimeter I/O lands should have about a 50µm to 75µm (2mil to 3mil) standoff height. The solder paste stencil design is the first step in developing optimized, reliable solder joins. Stencil aperture size to land size ratio should typically be 1:1. The aperture width may be reduced slightly to help prevent solder bridging between adjacent I/O lands. To reduce solder paste volume on the larger thermal lands, it is recommended that an array of smaller apertures be used instead of one large aperture. It is recommended that the stencil printing area cover 50% to 80% of the PCB layout pattern. A typical solder stencil pattern is shown in the Package Outline Drawing L15.15x15 on page 15. The gap width between pad to pad is 0.6mm. The user should consider the symmetry of the whole stencil pattern when designing its pads. A laser cut, stainless steel stencil with electropolished trapezoidal walls is recommended. Electropolishing "smoothes" the aperture walls resulting in reduced surface friction and better paste release which reduces voids. Using a trapezoidal section aperture (TSA) also promotes paste release and forms a "brick like" paste deposit that assists in firm component placement. A 0.1mm to 0.15mm stencil thickness is recommended for this large pitch (1.3mm) QFN.

Reflow Parameters

Due to the low mount height of the QFN, "No Clean" Type 3 solder paste per ANSI/J-STD-005 is recommended. Nitrogen purge is also recommended during reflow. A system board reflow profile depends on the thermal mass of the entire populated board, so it is not practical to define a specific soldering profile just for the QFN. The profile given in Figure 26 is provided as a guideline, to be customized for varying manufacturing practices and applications.

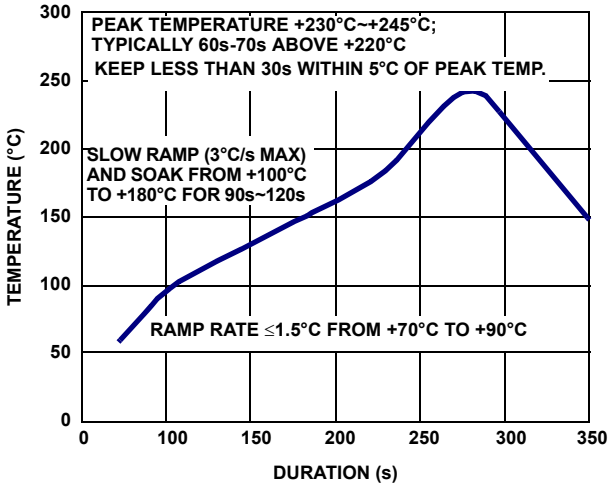


FIGURE 26. TYPICAL REFLOW PROFILE

Package Outline Drawing

L15.15x15

15 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (PUNCH QFN)

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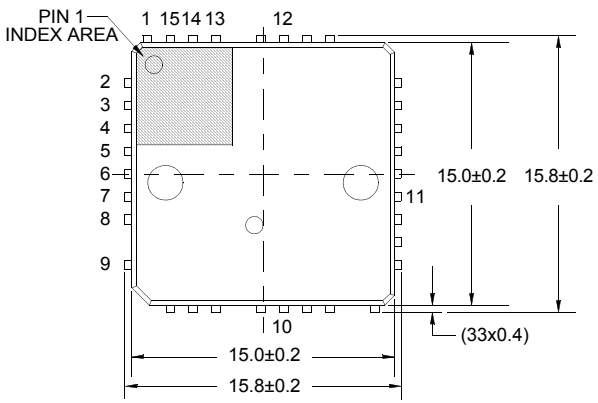
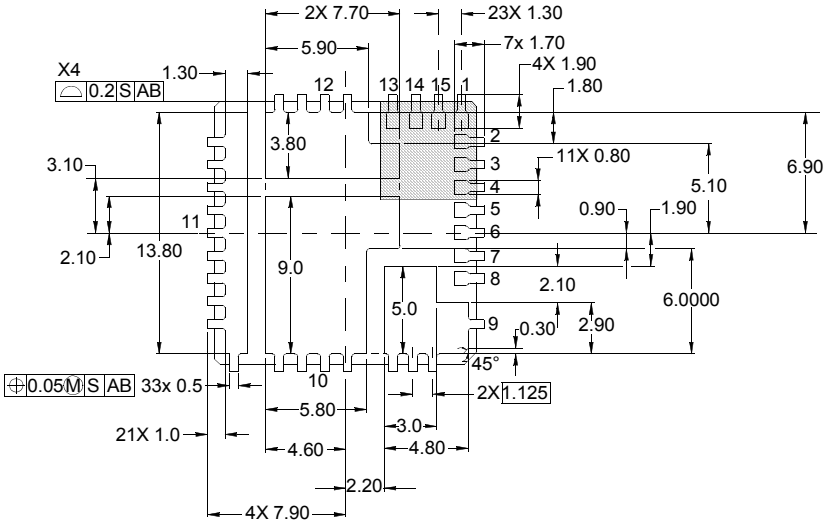
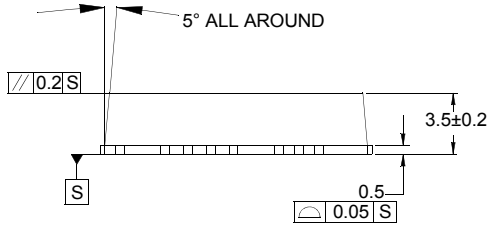


TOP VIEW



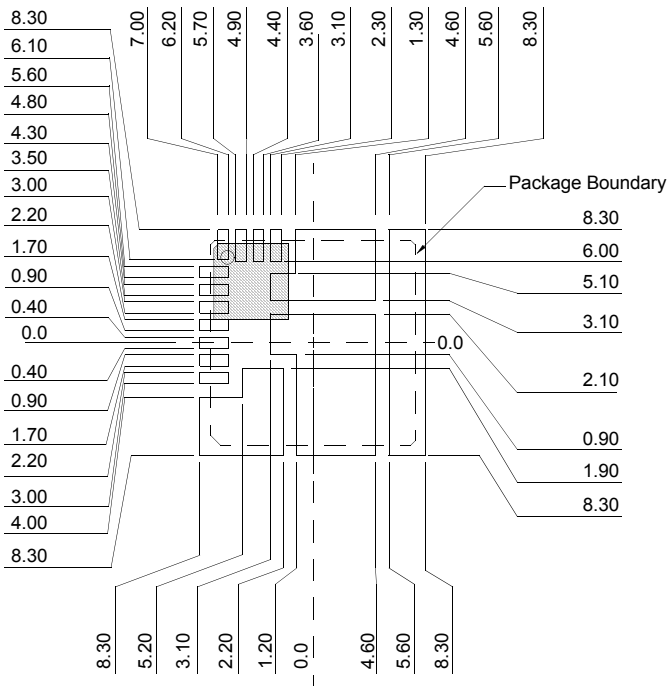
BOTTOM VIEW



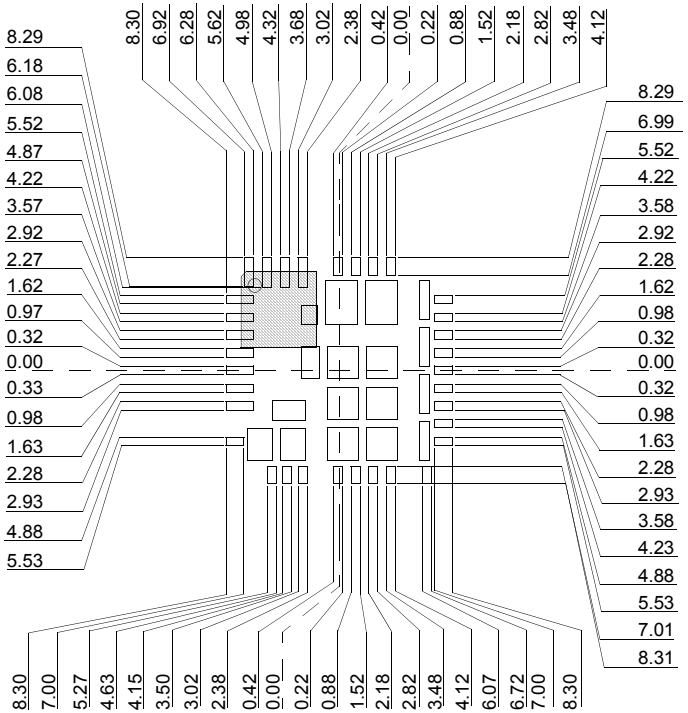
SIDE VIEW

NOTES:

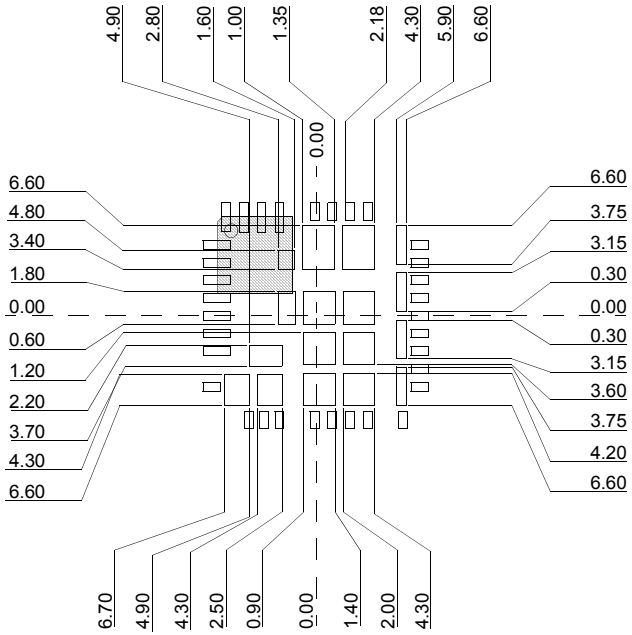
1. **Dimensions are in millimeters.**
2. **Unless otherwise specified, tolerance : Decimal ± 0.05; Body Tolerance ±0.1mm**
3. **The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.**



TYPICAL RECOMMENDED LAND PATTERN



STENCIL PATTERN WITH SQUARE PADS-2



STENCIL PATTERN WITH SQUARE PADS-1