ISL85012

12A, 3.8V to 18V Input, Synchronous Buck Regulator

FN8677
Rev.4.00
Nov 11, 2021

The ISL85012 is a highly efficient, monolithic, synchronous buck regulator that can deliver 12A of continuous output current from a 3.8V to 18V input supply. The device uses current mode control architecture with a fast transient response and excellent loop stability.

The ISL85012 integrates very low ON-resistance high-side and low-side FETs to maximize efficiency and minimize external component count. The minimum BOM and easy layout footprint are extremely friendly to space constraint systems.

The operation frequency of this device can be set using the FREQ pin: 600kHz (FREQ = float) and 300kHz (FREQ = GND). The device can also be synchronized to an external clock up to 1MHz.

Both high-side and low-side MOSFET current limit along with reverse current limit, fully protects the regulator in an overcurrent event. Selectable OCP schemes can fit various applications. Other protections, such as input/output overvoltage and over-temperature, are also integrated into the device which give required system level safety in the event of fault conditions.

The ISL85012 is offered in a space saving 15 Ld 3.5mmx3.5mm Pb-free TQFN package with great thermal performance and 0.8mm maximum height.

Features

- Power input voltage range variable 3.8V to 18V
- PWM output voltage adjustable from 0.6V
- Up to 12A output load
- Prebias start-up, fixed 3ms soft-start
- Selectable f_{SW} of 300kHz, 600kHz, and external synchronization up to 1MHz
- Peak current mode control
  - DCM/CCM
  - Thermally compensated current limit
  - Internal/external compensation
- Open-drain, PG window comparator
- Output overvoltage and thermal protection
- Input overvoltage protection
- Integrated boot diode with undervoltage detection
- Selectable OCP schemes
  - Hiccup OCP
  - Latch-off
- Compact size 3.5mmx3.5mm

Applications

- Servers and cloud infrastructure POLs
- IPCs, factory automation, PLCs
- Telecom and networking systems
- Storage systems
- Test measurement

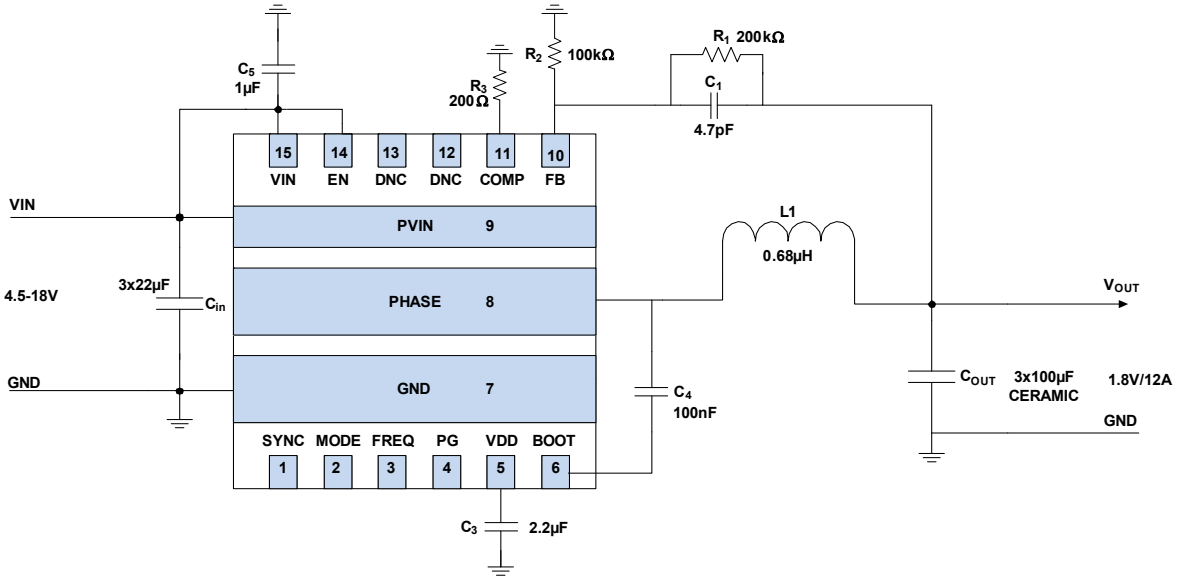


FIGURE 1. TYPICAL APPLICATION SCHEMATIC FOR INTERNAL COMPENSATION

Typical Application Schematic

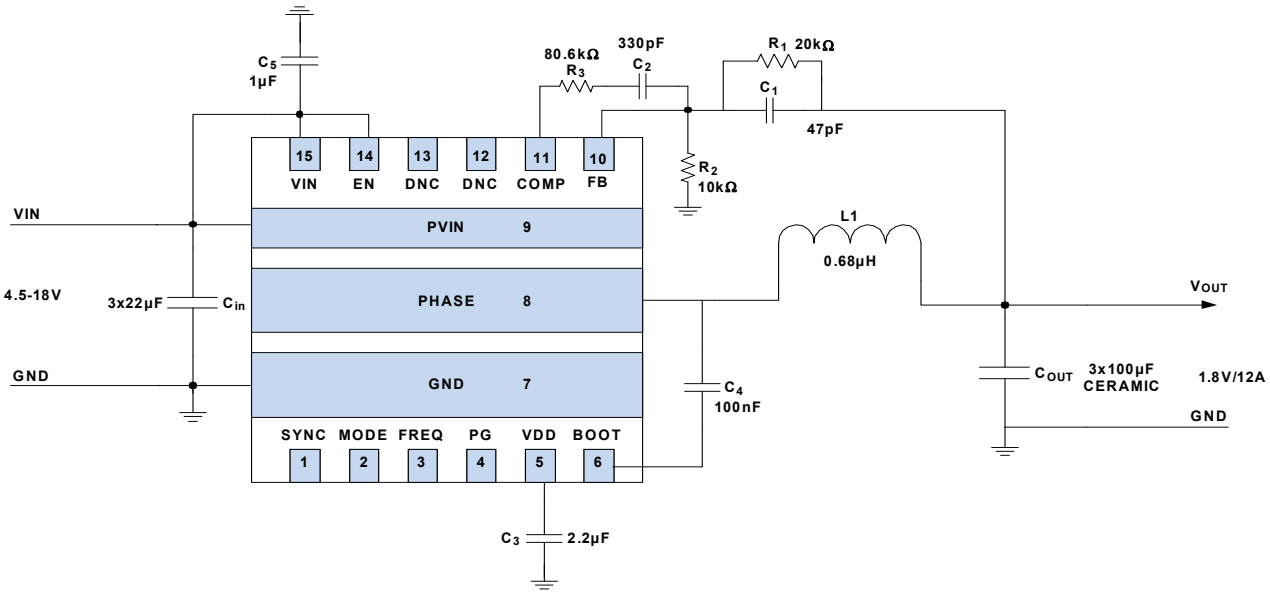


FIGURE 2. TYPICAL APPLICATION SCHEMATIC FOR EXTERNAL COMPENSATION

TABLE 1. DESIGN TABLE FOR DIFFERENT OUTPUT VOLTAGE

V_{OUT} (V)	0.9	1	1.2	1.5	1.8	2.5	3.3	5
V_{IN} (V)	4.5 to 18	4.5 to 18	4.5 to 18	4.5 to 18	4.5 to 18	4.5 to 18	4.5 to 18	6 to 18
FREQ (kHz)	300	300	300	600	600	600	600	600
Compensation	Internal	Internal	Internal	Internal	Internal	Internal	Internal	Internal
C_{in} (µF)	3x22	3x22	3x22	3x22	3x22	3x22	3x22	3x22
C_{out} (µF)	2x560 + 4x100	2x330 + 3x100	2x330 + 3x100	4x100	3x100	4x47	4x47	4x47
L_1 (µH)	0.68	0.68	1	0.68	0.68	1	1	1.5
R_1 (kΩ)	100	100	147	150	200	301	365	365
R_2 (kΩ)	200	150	147	100	100	95.3	80.6	49.9
C_1 (pF)	DNP	DNP	DNP	10	4.7	4.7	3.3	3.3

NOTES:

1. The design table is referencing the schematic shown in Figure 1.
2. Ceramic capacitors are selected for 22µF and 100µF in the table.
3. 560µF (14mΩ) and 330µF (10mΩ) are selected low ESR conductive polymer aluminum solid capacitors.
4. Inductor 7443340068 (0.68µH), 7443340100 (1µH) and 7443340150 (1.5µH) from Wurth Electronics are selected for the above applications.
5. Recommend to keep the inductor peak-to-peak current less than 5A.

TABLE 2. KEY DIFFERENCES BETWEEN FAMILY OF PARTS

PART NUMBER	INTERNAL/EXTERNAL COMPENSATION	EXTERNAL FREQUENCY SYNC	PROGRAMMABLE SOFT-START	SWITCHING FREQUENCY (kHz)	CURRENT RATING (A)
ISL85003	Yes	Yes	No	500	3
ISL85003A	Yes	No	Yes	500	3
ISL85005	Yes	Yes	No	500	5
ISL85005A	Yes	No	Yes	500	5
ISL85012	Yes	Yes	No	300 or 600 selectable	12

Ordering Information

PART NUMBER (Notes 7, 8)	PART MARKING	PACKAGE DESCRIPTION (RoHS COMPLIANT)	PKG. DWG. #	CARRIER TYPE (Note 6)	TEMP. RANGE
ISL85012FRZ-T	5012	15 Ld 3.5mmx3.5mm TQFN	L15.3.5x3.5	Reel, 6k	-40 to +125°C
ISL85012FRZ-T7A				Reel, 250	
ISL85012EVAL1Z	Evaluation Board				

NOTES:

6. See TB347 for details on reel specifications.
7. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
8. For Moisture Sensitivity Level (MSL), see product information page for ISL85012. For more information on MSL, see TB363.

Functional Block Diagram

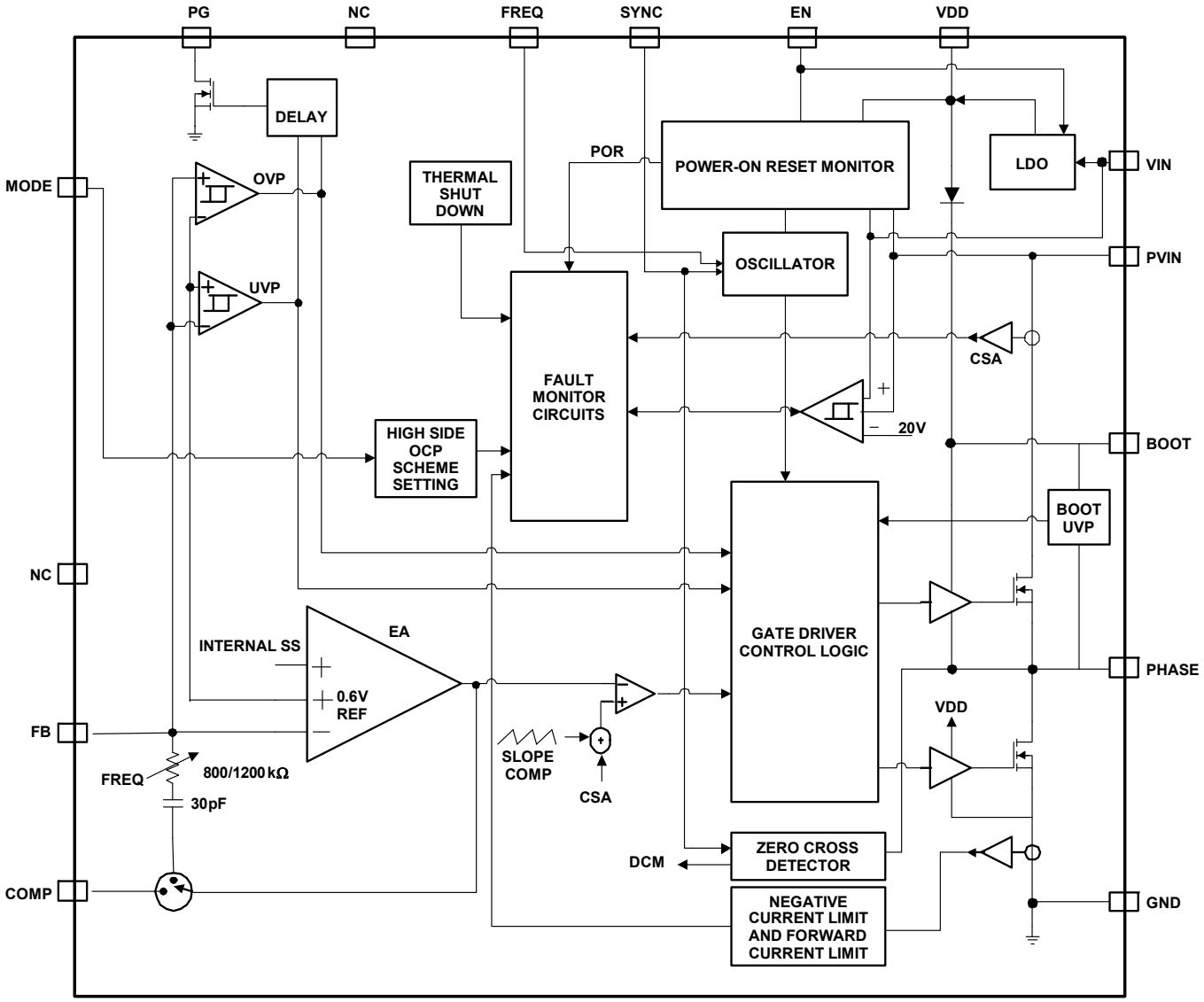
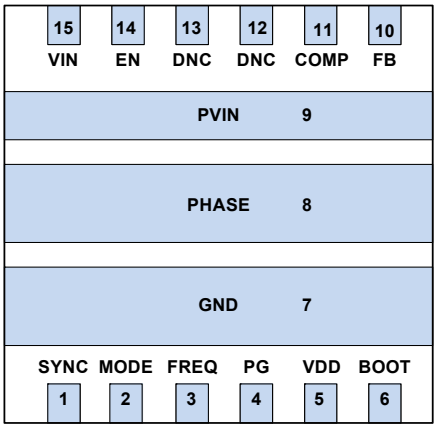


FIGURE 3. FUNCTIONAL BLOCK DIAGRAM

Pin Configuration

ISL85012
(15 LD 3.5mmx3.5mm TQFN)
TOP VIEW



Pin Descriptions

PIN#	PIN NAME	DESCRIPTION
1	SYNC	Synchronization and mode selection pin. Connect to VDD or float for PWM mode. Connect to GND for DCM mode in the light-load condition. Connect to an external clock signal for synchronization with the rising edge trigger.
2	MODE	OCP scheme select pin. Short it to GND for latch-off mode. Float it for hiccup mode.
3	FREQ	Default frequency selection pin. Short it to GND for 300kHz. Float it for 600kHz.
4	PG	Power-good, open-drain output. It requires a pull-up resistor (10kΩ to 100kΩ) between PG and VDD or a voltage not exceeding 5.5V. PG pulls high when FB is in the range of ~90% to ~116% of its intended value.
5	VDD	Low dropout linear regulator decoupling pin. The VDD is the internally generated 5V supply voltage and is derived from VIN. The VDD is used to power all the internal core analog control blocks and drivers. Connect a 2.2µF capacitor from VDD to the board ground plane. If the V_{IN} is between 3V to 5.5V, then connect VDD directly to VIN to improve efficiency.
6	BOOT	BOOT is the floating bootstrap supply pin for the high-side power MOSFET gate driver. A bootstrap capacitor, usually 0.1µF, is required from BOOT to PHASE.
7	GND	Reference of the power circuit. For thermal relief, this pin should be connected to the ground plane by vias.
8	PHASE	Switch node connection to the internal power MOSFETs (source of upper FET and drain of lower FET) and the external output inductor.
9	PVIN	Input supply for the PWM regulator power stage. A decoupling capacitor, typically ceramic, is required to be connected between this pin and GND.
10	FB	Inverting input to the voltage loop error amplifier. The output voltage is set by an external resistor divider connected to FB.
11	COMP	Output of the error amplifier. Compensation network between COMP and FB to configure external compensation. Place a 200Ω resistor between COMP and GND for internal compensation, which is used to meet most applications.
12, 13	DNC	Do Not Connect to pin. Float the pins in the design.
14	EN	Enable input. The regulator is held off when this pin is pulled to ground. The device is enabled when the voltage on this pin rises to about 0.6V.
15	VIN	Input supply for the control circuit and the source for the internal linear regulator that provides bias for the IC. A decoupling capacitor, typically 1µF ceramic, is required connected between VIN and GND.

Absolute Maximum Ratings

VIN, EN to GND ..... -0.3V to +22V
PVIN to GND ..... -0.3V to +22V
PHASE to GND..... -0.7V to +22V (DC)
PHASE to GND..... -2V to +22V (40ns)
BOOT to PHASE.....-0.3V to +7V
VDD, COMP, SYNC, PG, FB, MODE, FREQ, SS, IOCP to GND ...-0.3V to +7V
ESD Rating
Human Body Model (Tested per JS-001-2014).....2.5kV
Charged Device Model (Tested per JS-002-2014) 1kV
Latch-Up (Tested per JESD78E; Class 2, Level A, +125°C).....100mA

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
TQFN Package (Notes 9, 10).....	33	1.2

Maximum Storage Temperature Range .....-65°C to +150°C
Junction Temperature Range .....-55°C to +150°C
Pb-Free Reflow Profile ..... see TB493

Recommended Operating Conditions

VIN Supply Voltage Range..... 4.5V to 18V
PVIN Supply Voltage Range ..... 3.8V to 18V
Load Current Range.....0A to 12A

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

9. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features, except with 3 vias under the GND EPAD strip contacting the GND plane, and two vias under the VIN EPAD strip contacting the VIN plane. See TB379.
10. For θ_{JC}, the case temperature location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Unless otherwise noted, all parameter limits are established over the recommended operating conditions and the typical specification are measured at the following conditions: T_J = -40°C to +125°C, V_{IN} = 4.5V to 18V, unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +125°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 11)	TYP	MAX (Note 11)	UNIT
SUPPLY VOLTAGE						
PVIN Voltage Range	PVIN		**3.8**		**18**	V
V_{IN} Voltage Range	VIN		**4.5**		**18**	V
V_{IN} Quiescent Supply Current	I_Q	EN = 2V, FB = 0.64V		3	**5**	mA
V_{IN} Shutdown Supply Current	I_{SD}	EN = GND		8	**13**	µA
POWER-ON RESET						
PVIN POR Threshold		Rising edge			**2.9**	V
		Falling edge	**1.9**			V
V_{IN} POR Threshold		Rising edge			**4.49**	V
		Falling edge	**3.4**			V
EN POR Threshold		Rising edge	**0.5**	0.6	**0.7**	V
		Hysteresis		100		mV
V_{DD} POR Threshold		Rising edge			**3.6**	V
		Falling edge	**2.4**			V
INTERNAL VDD LDO						
V_{DD} Output Voltage Regulation Range		V_{IN} = 6V to 18V, I_{VDD} = 0mA to 30mA	**4.3**	5.0	**5.5**	V
V_{DD} Output Current Limit				80		mA
LDO Dropout Voltage		V_{IN} = 5V, I_{VDD} = 30mA			**0.65**	V
OSCILLATOR						
Nominal Switching Frequency	f_{SW1}	FREQ = float	**540**	600	**660**	kHz
Nominal Switching Frequency	f_{SW2}	FREQ = GND	**250**	280	**310**	kHz
Minimum On-Time	t_{ON}	I_{OUT} = 0mA		90	**150**	ns
Minimum Off-Time	t_{OFF}			140	**170**	ns
Synchronization Range			**100**		**1000**	kHz
SYNC Logic Input Low					**0.5**	V
SYNC Logic Input High			**1.2**			V

Electrical Specifications Unless otherwise noted, all parameter limits are established over the recommended operating conditions and the typical specification are measured at the following conditions: T_J = -40°C to +125°C, V_{IN} = 4.5V to 18V, unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +125°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 11)	TYP	MAX (Note 11)	UNIT
ERROR AMPLIFIER						
FB Regulation Voltage	V_{FB}		**0.5895**	0.600	**0.6105**	V
FB Leakage Current		V_{FB} = 0.6V			**10**	nA
Open Loop Bandwidth	BW			5.5		MHz
Gain				70		dB
Output Drive		High-side clamp = 1.5V, low-side clamp = 0.4V		±100		µA
Current-Sense Gain	RT		**0.050**	0.055	**0.063**	Ω
Slope Compensation	Se	Tested at 600kHz		470		mV/µs
SOFT-START						
Default Soft-Start Time			**1.9**	3	**4.7**	ms
PG						
Output Low Voltage		I_{PG} = 5mA		0.3		V
PG Pin Leakage Current				0.01		µA
PG Lower Threshold		Percentage of output regulation	**81**	87	**92**	%
PG Upper Threshold		Percentage of output regulation	**110**	116	**121**	%
PG Thresholds Hysteresis		SYNC is short-to-GND		3		%
Delay Time		Rising edge		1.5		ms
		Falling edge		23		µs
FAULT PROTECTION						
V_{IN}/PVIN Overvoltage Lockout		Rising edge	**19**	20.5	**22**	V
		Falling edge	**18**	19.5	**21**	V
		Hysteresis		1		V
Positive Overcurrent Protection Threshold	I_{POCP}	High-side OCP	**15.5**	18	**19.5**	A
		Low-side OCP		21		
Negative Overcurrent Protection Threshold	I_{NOCP}	Current forced into PHASE node, high-side MOSFET is off	**-10.8**	-7.5	**-5.5**	A
Hiccup Blanking Time				150		ms
FB Overvoltage Threshold			**110**	116	**121**	%
Thermal Shutdown Temperature	T_{SD}	Rising threshold		160		°C
	T_{HYS}	Hysteresis		10		°C
POWER MOSFET						
High-Side	R_{HDS}	IPHASE = 900mA		15		mΩ
Low-Side	R_{LDS}	IPHASE = 900mA		7		mΩ
PHASE Pull-Down Resistor		EN = GND		22.5		kΩ

NOTE:

11. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Typical Performance Curves

Circuit of Figure 2. Design table on page 2 shows the components value for different output voltages. Plots are captured from ISL85012EVAL1Z boards. V_{IN} = 12V, V_{OUT} = 1.8V, FREQ = 600kHz, CCM, T_J = -40°C to +125°C unless otherwise noted. Typical values are at T_A = +25°C.

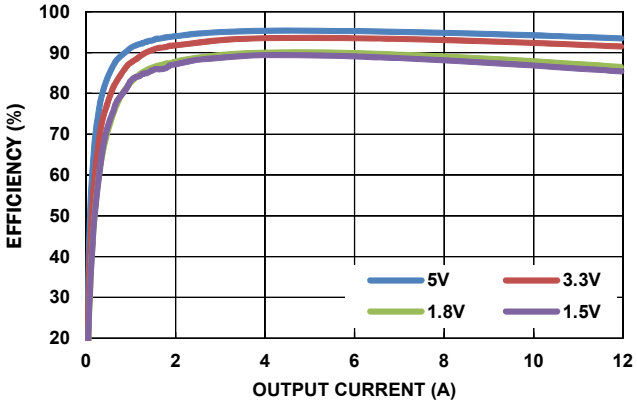


FIGURE 4. EFFICIENCY vs LOAD (V_{IN} = 12V, CCM, 600kHz)

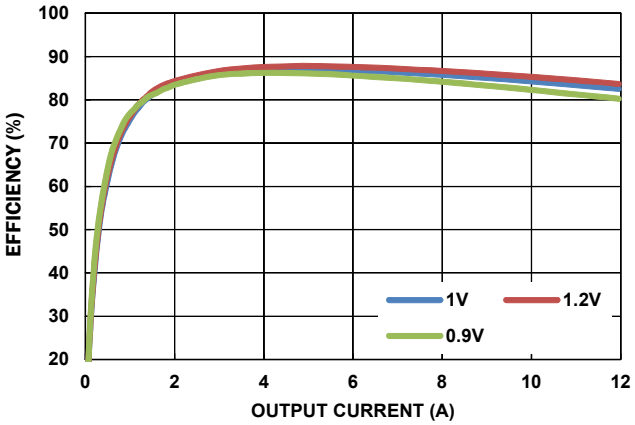


FIGURE 5. EFFICIENCY vs LOAD (V_{IN} = 12V, CCM, 300kHz)

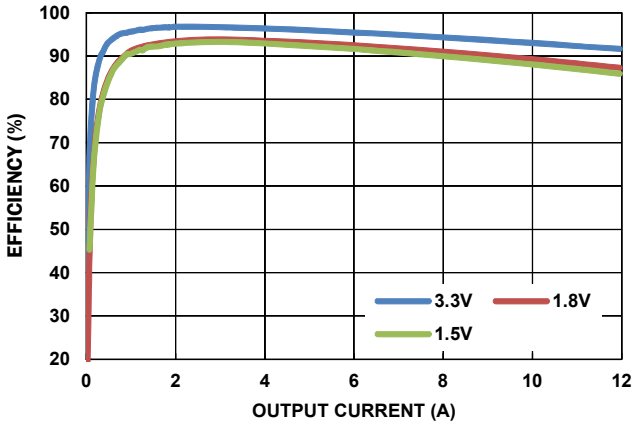


FIGURE 6. EFFICIENCY vs LOAD (V_{IN} = 5V, CCM, 600kHz)

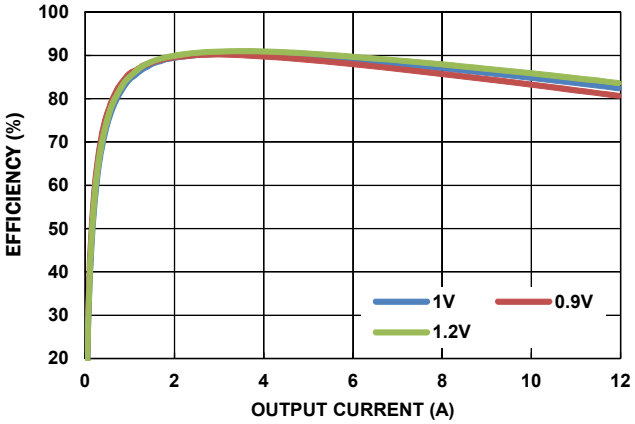


FIGURE 7. EFFICIENCY vs LOAD (V_{IN} = 5V, CCM, 300kHz)

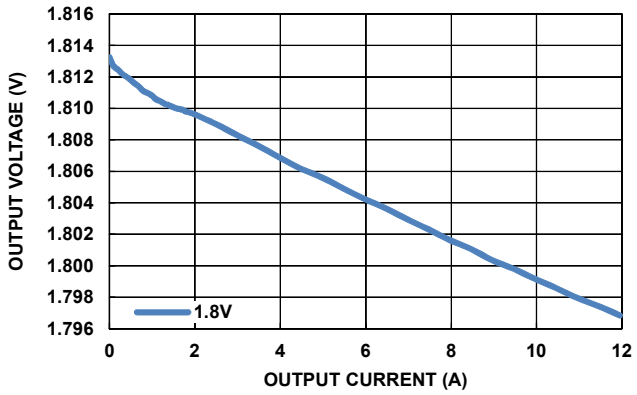


FIGURE 8. V_{OUT} REGULATION vs LOAD (V_{IN} = 12V, CCM, 600kHz)

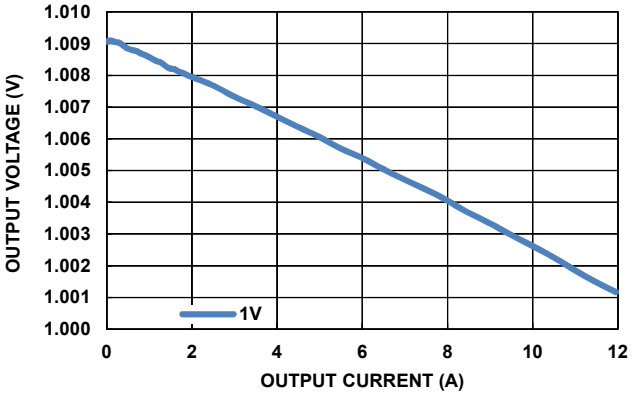


FIGURE 9. V_{OUT} REGULATION vs LOAD (V_{IN} = 12V, CCM, 300kHz)

Typical Performance Curves

Circuit of Figure 2. Design table on page 2 shows the components value for different output voltages. Plots are captured from ISL85012EVAL1Z boards. V_{IN} = 12V, V_{OUT} = 1.8V, FREQ = 600kHz, CCM, T_J = -40°C to +125°C unless otherwise noted. Typical values are at T_A = +25°C. **(Continued)**

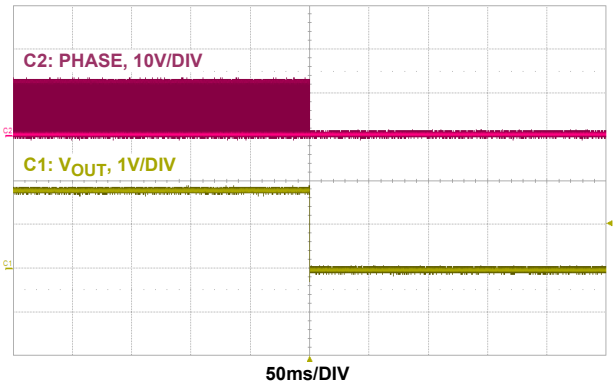


FIGURE 10. LATCH-OFF OCP (V_{IN} = 12V, V_{OUT} = 1.8V, 600kHz, CCM)

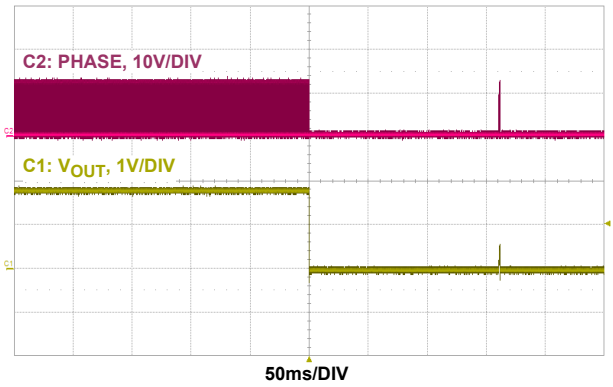


FIGURE 11. HICCUP OCP (V_{IN} = 12V, V_{OUT} = 1.8V, 600kHz, CCM)

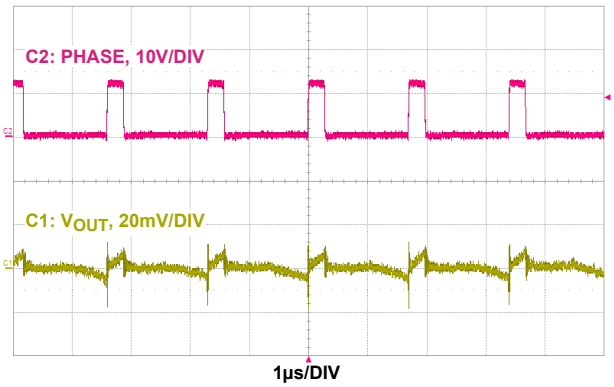


FIGURE 12. OUTPUT VOLTAGE RIPPLE (V_{IN} = 12V, V_{OUT} = 1.8V AT 12A, 600kHz, CCM)

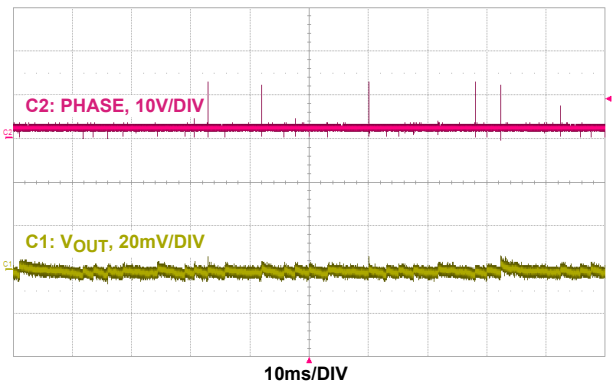


FIGURE 13. OUTPUT VOLTAGE RIPPLE (V_{IN} = 12V, V_{OUT} = 1.8V AT 0A, 600kHz, DCM)

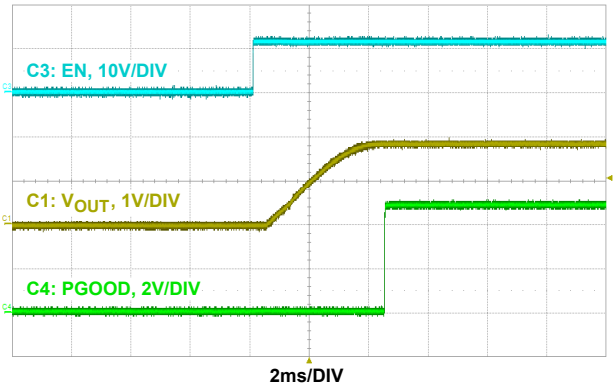


FIGURE 14. START-UP BY EN (V_{IN} = 12V, V_{OUT} = 1.8V AT 12A, 600kHz, CCM)

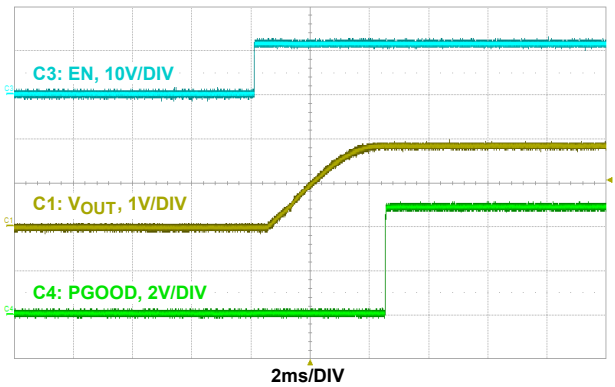


FIGURE 15. START-UP BY EN (V_{IN} = 12V, V_{OUT} = 1.8V AT 0A, 600kHz, DCM)

Typical Performance Curves

Circuit of Figure 2. Design table on page 2 shows the components value for different output voltages. Plots are captured from ISL85012EVAL1Z boards. V_{IN} = 12V, V_{OUT} = 1.8V, FREQ = 600kHz, CCM, T_J = -40°C to +125°C unless otherwise noted. Typical values are at T_A = +25°C. **(Continued)**

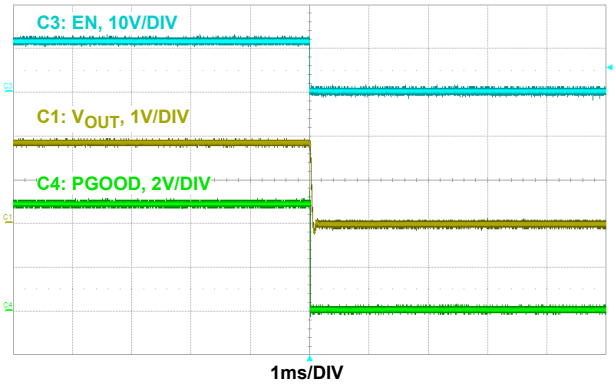


FIGURE 16. SHUTDOWN BY EN (V_{IN} = 12V, V_{OUT} = 1.8V AT 12A, 600kHz, CCM)

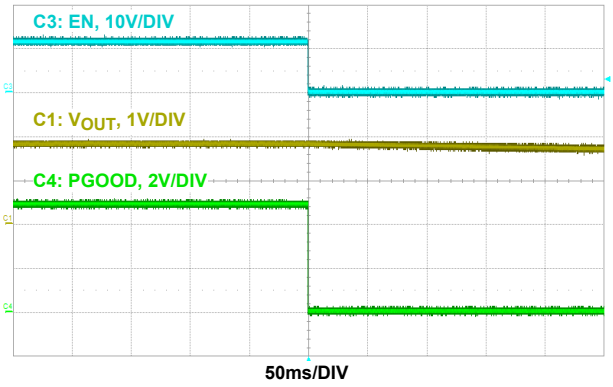


FIGURE 17. SHUTDOWN BY EN (V_{IN} = 12V, V_{OUT} = 1.8V AT 0A, 600kHz, DCM)

Typical Characteristics

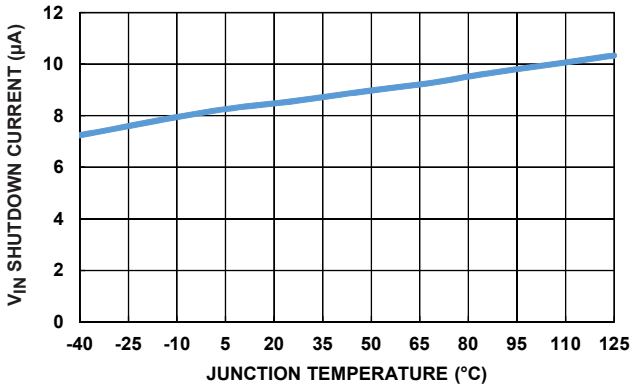


FIGURE 18. V_{IN} SHUTDOWN CURRENT vs TEMPERATURE

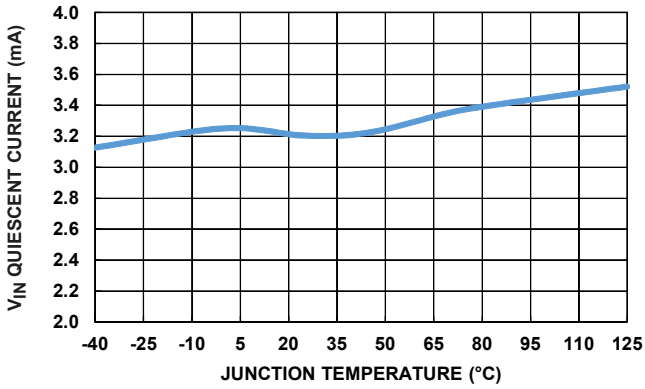


FIGURE 19. V_{IN} QUIESCENT CURRENT vs TEMPERATURE

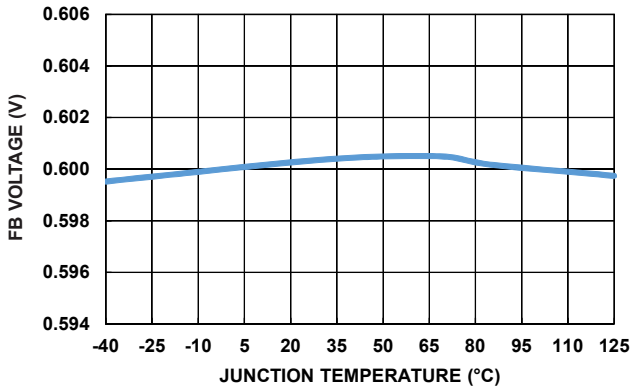


FIGURE 20. FEEDBACK VOLTAGE vs TEMPERATURE

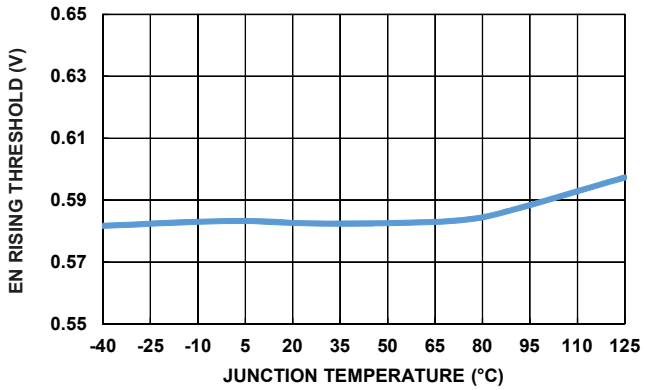


FIGURE 21. ENABLE THRESHOLD vs TEMPERATURE

Typical Characteristics (Continued)

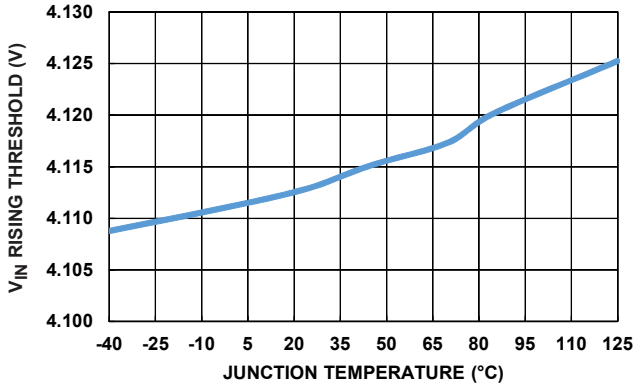


FIGURE 22. V_{IN} POR (RISING) vs TEMPERATURE

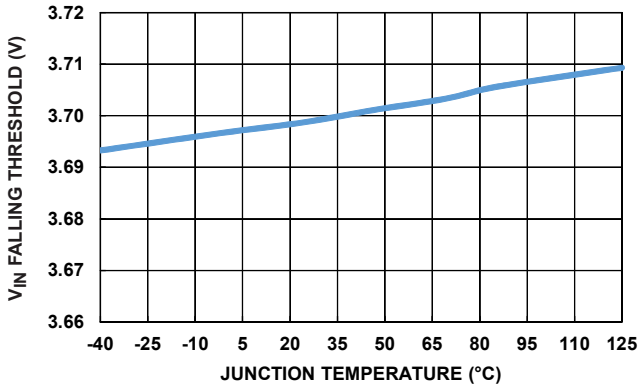


FIGURE 23. V_{IN} POR (FALLING) vs TEMPERATURE

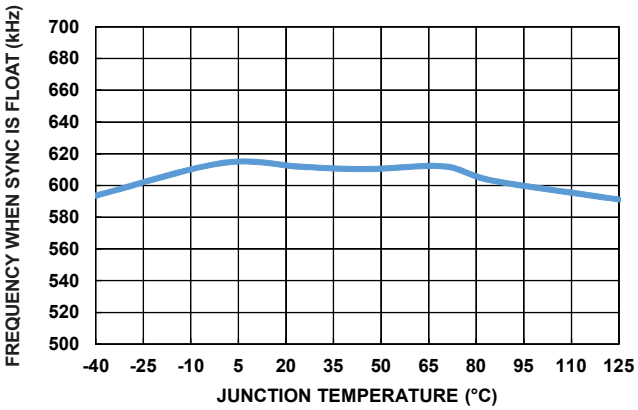


FIGURE 24. FREQUENCY (600kHz DEFAULT) vs TEMPERATURE

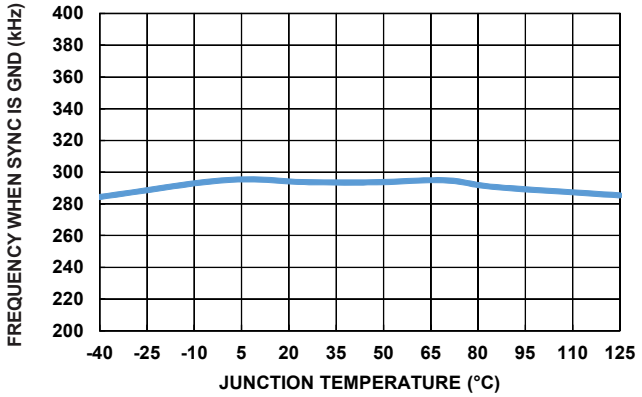


FIGURE 25. FREQUENCY (300kHz DEFAULT) vs TEMPERATURE

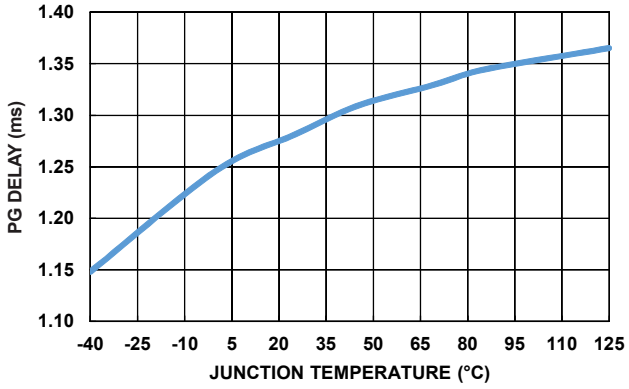


FIGURE 26. PG DELAY vs TEMPERATURE

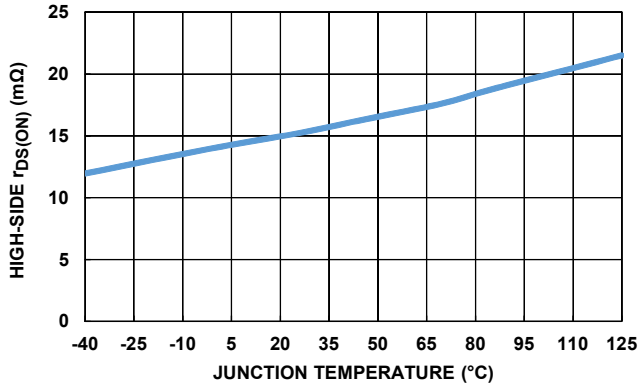


FIGURE 27. HIGH-SIDE $r_{DS(ON)}$ vs TEMPERATURE

Typical Characteristics (Continued)

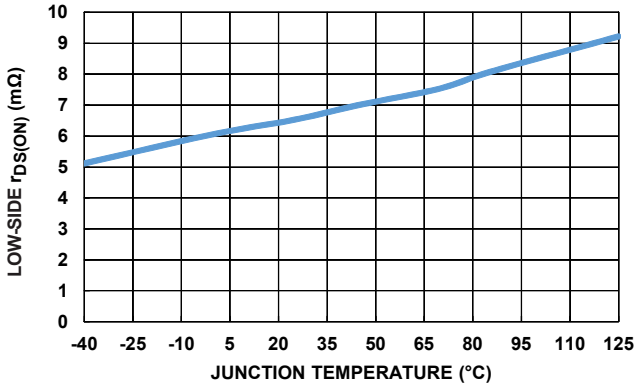


FIGURE 28. LOW-SIDE $r_{DS(ON)}$ vs TEMPERATURE

Detailed Description

The ISL85012 combines a synchronous buck controller with a pair of integrated switching MOSFETs. The buck controller drives the internal high-side and low-side N-channel MOSFETs to deliver load currents up to 12A. The buck regulator can operate from an unregulated DC source, such as a battery, with a voltage ranging from +3.8V to +18V. An internal 5V LDO voltage regulator is used to bias the controller. The converter output voltage is programmed using an external resistor divider and will generate regulated voltages down to 0.6V. These features make the regulator suited for a wide range of applications.

The controller uses a current mode loop, which simplifies the loop compensation and permits fixed frequency operation over a wide range of input and output voltages. The internal feedback loop compensation option allows for simple circuit design. 600kHz (FREQ = float) and 300kHz (FREQ = GND) can be selected as the default switching frequency. The regulator can be synchronized from 100kHz to 1MHz by SYNC pin as well.

The buck regulator is equipped with a lossless current limit scheme. The current in the output stage is derived from temperature compensated measurements of the drain-to-source voltage of the internal power MOSFETs.

Operation Initialization

The power-on reset circuitry and enable inputs prevent false start-up of the PWM regulator output. Once all the input criteria are met (see Figure 29), the controller soft-starts the output voltage to the programmed level.

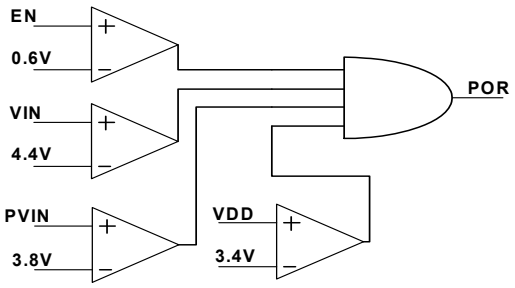


FIGURE 29. POR CIRCUIT

Enable and Soft-Start

Chip operation begins after V_{IN}, PVIN, and V_{DD} exceed their rising POR trip points. If EN is held low externally, nothing happens until this pin is released. Once the voltage on the EN pin is above 0.6V, the LDO powers up and soft-start control begins. The ISL85012 operates at Discontinuous Conduction Mode (DCM) during soft-start. The soft-start time is 3ms. EN can be directly driven by VIN or an external power supply. It is recommended to add an RC filter at the EN pin if the signal which drives the EN is noisy.

The part is designed supporting start-up into a prebiased load (the prebiased voltage requires to be less than the setting output voltage). Both high-side and low-side switches are disabled until the internal SS voltage exceeds the FB voltage during start-up.

PWM Control Scheme

The ISL85012 employs the current-mode Pulse-Width Modulation (PWM) control scheme for fast transient response. The current loop consists of the oscillator, the PWM comparator, current sensing circuit, and the slope compensation circuit. The gain of the current sensing circuit is typically 55mV/A and the slope compensation is 780mV/t_{SS} (t_{SS} = period). The control reference for the current loop comes from the Error Amplifier's (EA) output, which compares the feedback signal at FB pin to the integrated 0.6V reference.

Setting as internal compensation (COMP short to GND through a 200Ω resistor), the voltage loop is internally compensated with a 30pF and 800kΩ RC network either the switching regulator works at default 600kHz (FREQ = float) or it is synchronized externally by SYNC pin. A 30pF and 1200kΩ RC network is implemented for internal compensation when It works at default 300kHz (FREQ = GND).

The PWM operation is initialized by the clock from the oscillator. The high-side MOSFET is turned on at the beginning of a PWM cycle and the current in the MOSFET starts to ramp-up. When the sum of the current amplifier CSA, and the slope compensation (780mV/t_{SS}) reaches the control reference of the current loop (COMP), the PWM comparator sends a signal to the PWM logic to turn off the upper MOSFET and turn on the lower MOSFET. The lower MOSFET stays on until the end of the PWM cycle. Figure 30 shows the typical operating waveforms during Continuous Conduction Mode (CCM) operation. The dotted lines illustrate the sum of the compensation ramp and the current-sense amplifier's output.

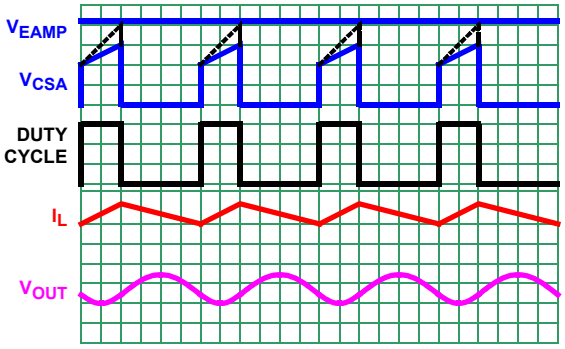


FIGURE 30. PWM OPERATION WAVEFORMS

Light-Load Operation

The ISL85012 monitor both the current in the low-side MOSFET and the voltage of the FB node for regulation. Pulling the SYNC pin low allows the regulator to enter discontinuous operation when lightly loaded by operating the low-side MOSFET in Diode Emulation Mode (DEM). In this mode, reverse current is not allowed in the inductor and the output falls naturally to the regulation voltage before the high-side MOSFET is switched for the next cycle. In CCM mode, the boundary is set by Equation 1:

$$I_{OUT} = \frac{V_{OUT}(1-D)}{2Lf_{SW}} \quad \text{(EQ. 1)}$$

where D = duty cycle, f_{SW} = switching frequency, L = inductor value, I_{OUT} = output loading current, and V_{OUT} = output voltage. Table 3 shows the operating modes determined by the SYNC pin.

TABLE 3. OPERATION MODE SETTING

SYNC	
Float	GND
Force CCM	DEM

Synchronization

The ISL85012 can be synchronized from 100kHz to 1MHz by an external signal applied to the SYNC pin. The rising edge on the SYNC triggers the rising edge of the PHASE pulse. Make sure the on-time of the SYNC pulse is longer than 100ns.

Output Voltage Selection

The regulator output voltages can be programmed using external resistor dividers that scale the voltage feedback relative to the internal reference voltage. The scaled voltage is fed back to the inverting input of the error amplifier; refer to Figure 31.

The output voltage programming resistor, R_2, will depend on the value chosen for the feedback resistor, R_1, and the desired output voltage, V_{OUT}; see Equation 2. The R_1 value will determine the gain of the feedback loop. See "Loop Compensation Design" on page 15 for more details. The value for the feedback resistor is typically between 1kΩ and 370kΩ.

$$R_2 = \frac{R_1 \cdot 0.6V}{V_{OUT} - 0.6V} \quad \text{(EQ. 2)}$$

If the desired output voltage is 0.6V, then R_2 is left unpopulated. R_1 is still required to set the low frequency pole of the modulator compensation.

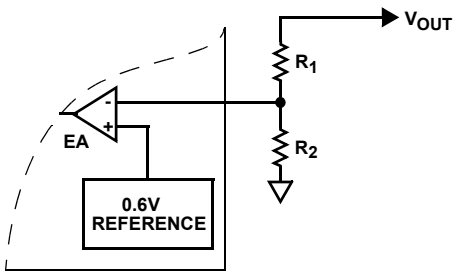


FIGURE 31. EXTERNAL RESISTOR DIVIDER

Protection Features

The regulator limits current in all on-chip power devices. Overcurrent limits are applied to the two output switching MOSFETs as well as to the LDO linear regulator that feeds V_{DD}. The output overvoltage protection circuitry on the switching regulator provides a second layer of protection.

High-Side MOSFET Overcurrent Protection

Current flowing through the internal high-side switching MOSFET is monitored during on-time. The current, which is temperature compensated, will compare to a default 18A overcurrent limit. The ISL85012 offers two OCP schemes to implement the on-time overcurrent protection, which can be configured by the MODE pin (see Table 4).

TABLE 4. OCP SCHEME SETTING

MODE	
Float	GND
Enter hiccup mode after eight consecutive cycle-by-cycle limit. Blanking time is 150ms	Enter latch-off mode after eight consecutive cycle-by-cycle limit

If the measured current exceeds the overcurrent limit, the high-side MOSFET is immediately turned off and will not turn on again until the next switching cycle. After eight consecutive cycles of overcurrent events detected, the converter will operate at the selected OCP scheme according to the MODE pin configuration. A cycle where an overcurrent condition is not detected will reset the counter.

The switching frequency will be folded back if the OCP is tripped and the on-time of the PWM is less than 250ns to lower down the average inductor current.

Low-Side MOSFET Overcurrent Protection

Low-side current limit consists of forward current limit (from GND to PHASE) and reverse current limit (from PHASE to GND).

Current through the low-side switching MOSFET is sampled during off time. The low-side OCP comparator is flagged if the low-side MOSFET current exceeds 21A (forward). It resets the flag when the current falls below 15A. The PWM will skip cycles when the flag is set, allowing the inductor current to decay to a safe level before resuming switching (see Figure 32).

Similar to the forward overcurrent, the reverse current protection is realized by monitoring the current across the low-side MOSFET. When the low-side MOSFET current reaches -7.5A, the synchronous rectifier is turned off. This limits the ability of the regulator to actively pull-down on the output.

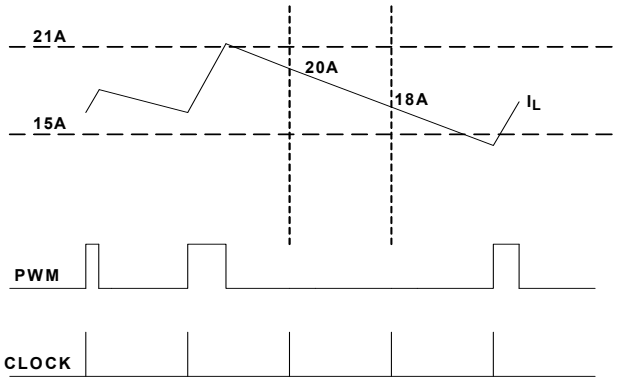


FIGURE 32. LOW-SIDE FORWARD OCP

Output Overvoltage Protection

The overvoltage protection triggers when the output voltage exceeds 116% of the set voltage. In this condition, high-side and low-side MOSFETs are off until the output drops to within the regulation band. Once the output is in regulation, the controller will restart under internal SS control.

Input Overvoltage Protection

The input overvoltage protection system prevents operation of the switching regulator whenever the input voltage is higher than 20V. The high-side and low-side MOSFETs are off and the converter will restart under internal SS control when the input voltage returns to normal.

Thermal Overload Protection

Thermal overload protection limits the maximum die temperature, and thus the total power dissipation in the regulator. A sensor on the chip monitors the junction temperature. A signal is sent to the fault monitor circuits whenever the junction temperature (T_J) exceeds +160°C, which causes the switching regulator and LDO to shut down.

The switching regulator turns on again and soft-starts after the IC's junction temperature cools by 10°C. The switching regulator exhibits hiccup mode operation during continuous thermal overload conditions. For continuous operation, do not exceed the +125°C junction temperature rating.

BOOT Undervoltage Detection

The internal driver of the high-side FET is equipped with a BOOT Undervoltage (UV) detection circuit. In the event the voltage difference between BOOT and PHASE falls below 2.8V, the UV detection circuit allows the low-side MOSFET on for 250ns, to recharge the bootstrap capacitor.

While the ISL85012 includes an internal bootstrap diode, efficiency can be improved by using an external supply voltage and bootstrap Schottky diode. The external diode is then sourced from a fixed external 5V supply or from the output of the switching regulator if this is at 5V. The bootstrap diode can be a low cost type, such as the BAT54 (see Figure 33).

Power-Good

ISL85012 has a Power-Good (PG) indicator which is an open drain of a MOSFET. It requires pull-up to VDD or other voltage source lower than 5.5V through a resistor (usually from 10k to 100kΩ). The PG asserted 1.5ms after the FB voltage reaches 90% of the reference voltage in soft-start. It pulls low if the FB voltage drops to 87% of the reference voltage or exceeds 116% of the reference voltage during the normal operation. Disabling the part also pulls the PG low. The PG will reassert when the FB voltage drops back to 113% (100%) of the reference voltage after tripping the overvoltage protection when SYNC is low (float/high).

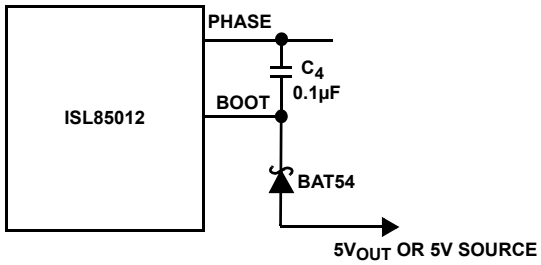


FIGURE 33. EXTERNAL BOOTSTRAP DIODE

Application Guidelines

Buck Regulator Output Capacitor Selection

An output capacitor is required to filter the inductor current and supply the load transient current. The filtering requirements are a function of the switching frequency, the ripple current and the required output ripple. The load transient requirements are a function of the slew rate (di/dt) and the magnitude of the transient load current. These requirements are generally met with a mix of capacitor types and careful layout.

High frequency ceramic capacitors initially supply the transient and slow the current load rate seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the Equivalent Series Resistance (ESR) and voltage rating requirements rather than actual capacitance requirements.

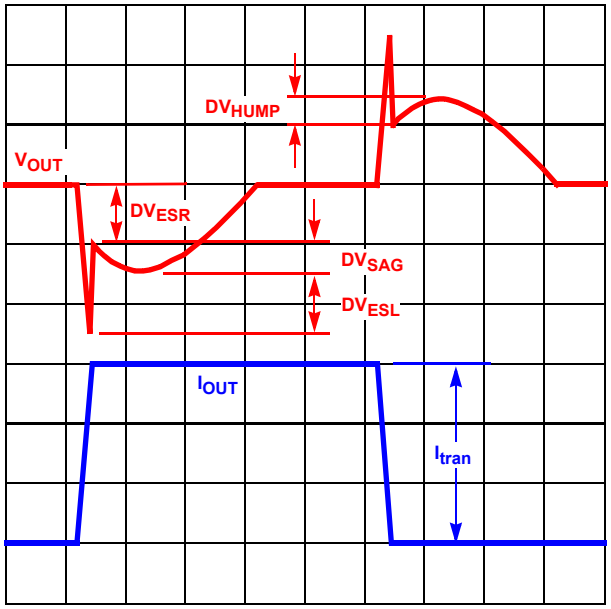


FIGURE 34. TYPICAL TRANSIENT RESPONSE

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. Consult with the manufacturer of the load on specific decoupling requirements.

The shape of the output voltage waveform during a load transient that represents the worst case loading conditions, will ultimately determine the number of output capacitors and their type. When this load transient is applied to the converter, most of the energy required by the load is initially delivered from the output capacitors. This is due to the finite amount of time required for the inductor current to slew up to the level of the output current required by the load. This phenomenon results in a temporary dip in the output voltage. At the very edge of the transient, the Equivalent Series Inductance (ESL) of each capacitor induces a spike that adds on top of the existing voltage drop due to the Equivalent Series Resistance (ESR).

After the initial spike, attributable to the ESR and ESL of the capacitors, the output voltage experiences sag. This sag is a direct consequence of the amount of capacitance on the output.

During the removal of the same output load, the energy stored in the inductor is dumped into the output capacitors. This energy dumping creates a temporary hump in the output voltage. This hump, as with the sag, can be attributed to the total amount of capacitance on the output. Figure 34 shows a typical response to a load transient.

The amplitudes of the different types of voltage excursions can be approximated using Equations 3, 4, 5 and 6.

$$\Delta V_{ESR} = ESR \bullet I_{TRAN} \quad \text{(EQ. 3)}$$

$$\Delta V_{ESL} = ESL \bullet \frac{I_{TRAN}}{dt} \quad \text{(EQ. 4)}$$

$$\Delta V_{SAG} = \frac{L_{out} \bullet I_{TRAN}^{2}}{2C_{OUT} \bullet (V_{IN} - V_{OUT})} \quad \text{(EQ. 5)}$$

$$\Delta V_{HUMP} = \frac{L_{out} \bullet I_{TRAN}^{2}}{2C_{OUT} \bullet V_{OUT}} \quad \text{(EQ. 6)}$$

where I_{TRAN} = Output Load Current Transient and C_{OUT} = Total Output Capacitance.

In a typical converter design, the ESR of the output capacitor bank dominates the transient response. The ESR and the ESL are typically the major contributing factors in determining the output capacitance. The number of output capacitors can be determined by using Equation 7, which relates the ESR and ESL of the capacitors to the transient load step and the tolerable output voltage excursion during load transient (ΔV_o):

$$\text{Number of Capacitors} = \frac{\frac{ESL \bullet I_{TRAN}}{dt} + ESR \bullet I_{TRAN}}{\Delta V_o} \quad \text{(EQ. 7)}$$

If ΔV_{SAG} and/or ΔV_{HUMP} are found to be too large for the output voltage limits, then the amount of capacitance may need to be increased. In this situation, a trade-off between output inductance and output capacitance may be necessary.

The ESL of the capacitors, which is an important parameter in the previous equations, is not usually listed in specification. Practically, it can be approximated using Equation 8 if an Impedance vs Frequency curve is given for a specific capacitor:

$$ESL = \frac{1}{C(2 \bullet \pi \bullet f_{res})^{2}} \quad \text{(EQ. 8)}$$

where f_{res} is the frequency where the lowest impedance is achieved (resonant frequency).

The ESL of the capacitors becomes a concern when designing circuits that supply power to loads with high rates of change in the current.

Output Inductor Selection

The output inductor is selected to meet the output voltage ripple requirements and minimize the converter's response time to the load transient. The inductor value determines the converter's ripple current and the ripple voltage is a function of the ripple current. The ripple voltage and current are approximated by Equations 9 and 10:

$$\Delta I = \frac{(V_{IN} - V_{OUT})}{f_{SW} \bullet L} \bullet \frac{V_{OUT}}{V_{IN}} \quad \text{(EQ. 9)}$$

$$\Delta V_{OUT} = \Delta I \bullet ESR \quad \text{(EQ. 10)}$$

Increasing the value of inductance reduces the ripple current and voltage. However, the large inductance values reduce the converter's response time to a load transient. It is recommended to set the ripple inductor current to approximately 30% of the maximum output current for optimized performance. Recommend the design of the inductor ripple current does not exceeds 5A in the applications of ISL85012.

One of the parameters limiting the converter's response to a load transient is the time required to change the inductor current. Given a sufficiently fast control loop design, the ISL85012 will provide either 0% or 100% duty cycle in response to a load transient. The response time is the time required to slew the inductor current from an initial current value to the transient current level. During this interval, the difference between the inductor current and the transient current level must be supplied by the output capacitor. Minimizing the response time can minimize the output capacitance required.

The response time to a transient is different for the application of load and the removal of load. Equations 11 and 12 give the approximate response time interval for application and removal of a transient load:

$$t_{RISE} = \frac{L \times I_{TRAN}}{V_{IN} - V_{OUT}} \quad \text{(EQ. 11)}$$

$$t_{FALL} = \frac{L \times I_{TRAN}}{VOUT} \quad \text{(EQ. 12)}$$

where I_{TRAN} is the transient load current step, t_{RISE} is the response time to the application of load, and t_{FALL} is the response time to the removal of load. The worst case response time can be either at the application or removal of load. Be sure to check both of these equations at the minimum and maximum output levels for the worst case response time.

Input Capacitor Selection

Use a mix of input bypass capacitors to control the input voltage ripple. Use ceramic capacitors for high frequency decoupling and bulk capacitors to supply the current needed each time the switching MOSFET turns on. Place the ceramic capacitors physically close to the MOSFET VIN pins (switching MOSFET drain) and PGND.

The important parameters for the bulk input capacitance are the voltage rating and the RMS current rating. For reliable operation, select bulk capacitors with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. Their voltage rating should be at least 1.25 times greater than the maximum input voltage, while a voltage rating of 1.5 times is a conservative guideline. For most cases, the RMS current rating requirement for the input capacitor of a buck regulator is approximately 1/2 the DC load current.

The maximum RMS current required by the regulator may be closely approximated through Equation 13:

$$I_{RMS_{MAX}} = \sqrt{\frac{V_{OUT}}{V_{IN}} \bullet \left({I_{OUT_{MAX}}}^2 + \frac{1}{12} \bullet \left(\frac{V_{IN} - V_{OUT}}{L \bullet f_{SW}} \bullet \frac{V_{OUT}}{V_{IN}} \right)^2 \right)} \quad \text{(EQ. 13)}$$

For a through-hole design, several electrolytic capacitors may be needed, especially at temperatures less than -25°C. The electrolytic's ESR can increase ten times higher than at room temperature and cause input line oscillation. In this case, a more thermally stable capacitor such as X7R ceramic should be used. For surface mount designs, solid tantalum capacitors can be used, but caution must be exercised with regard to the capacitor surge current rating. Some capacitor series available from reputable manufacturers are surge current tested.

Loop Compensation Design

When COMP is not connected to GND through a 200Ω resistor, the COMP pin is active for external loop compensation. The regulator uses constant frequency peak current mode control architecture to achieve a fast loop transient response. An accurate current sensing pilot device in parallel with the high-side switch is used for peak current control signal and overcurrent protection. The inductor is not considered as a state variable since its peak current is constant, and the system becomes a single order system. It is much easier to design a type II compensator to stabilize the loop than to implement voltage mode control. Peak current mode control has an inherent input voltage feed-forward function to achieve good line regulation. Figure 35 shows the small signal model of the synchronous buck regulator.

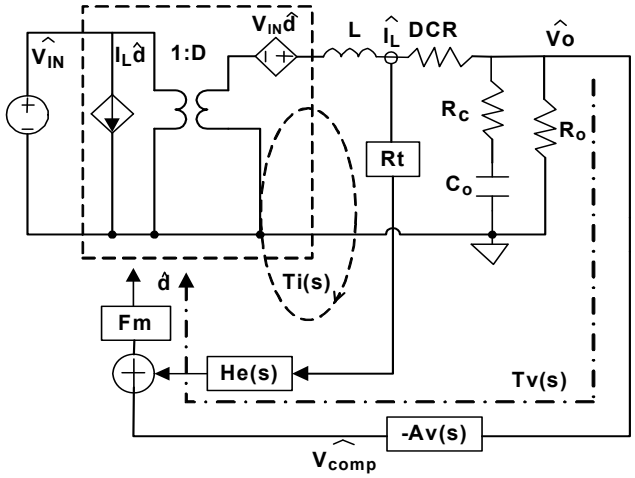


FIGURE 35. SMALL SIGNAL MODEL OF SYNCHRONOUS BUCK REGULATOR

To simplify the analysis, sample and hold effect block He(s) and slope compensation are not taken into account. Assume V_{comp} is equal to the current sense signal ILxRt and ignore the DCR of the inductor, the power train can be approximated by a voltage controlled current source supplying current to the output capacitor and load resistor (see Figure 36). The transfer function frequency response is presented in Figure 37.

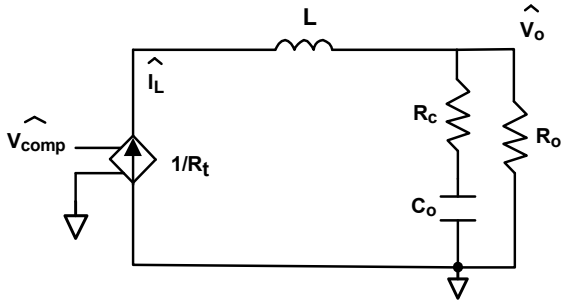


FIGURE 36. POWER TRAIN SMALL SIGNAL MODEL

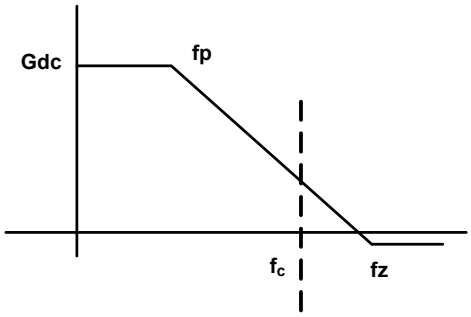


FIGURE 37. POWER TRAIN SMALL FREQUENCY RESPONSE

The simplified transfer function is derived in Equation 14.

$$Gp(S) = \frac{\hat{v}_o}{\hat{v}_{comp}} = Gdc \frac{1+\frac{S}{\omega_z}}{1+\frac{S}{\omega_p}} \quad \text{(EQ. 14)}$$

where:

$$Gdc = \frac{R_o}{R_t};\ \omega_z = 2\pi fz = \frac{1}{R_c x C_o};\ \omega_p = 2\pi fp = \frac{1}{(R_o + R_c) x C_o} \quad \text{(EQ. 15)}$$

Note that C_o is the actual capacitance seen by the regulator, which may include ceramic high frequency decoupling and bulk output capacitors. Ceramic may have to be derated by approximately 40% depending on dielectric, voltage stress, and temperature.

Usually, a type II compensation network is used to compensate the peak current mode control converter. Figure 38 shows a typical type II compensation network and its transfer function is expressed in Equation 16. The frequency response is shown in Figure 39.

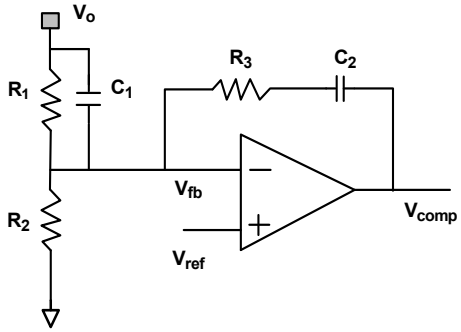


FIGURE 38. TYPE II COMPENSATION NETWORK

$$A_v(S) = \frac{\hat{v}_{comp}}{\hat{v}_o} = \frac{\left(1+\frac{S}{\omega_{cz1}}\right)\left(1+\frac{S}{\omega_{cz2}}\right)}{SC_2R_1} \quad \text{(EQ. 16)}$$

where:

$$\omega_{cz1} = 2\pi f_{z1} = \frac{1}{R_3C_2},\ \omega_{cz2} = 2\pi f_{z2} = \frac{1}{R_1C_1},\ f_{pc} = \frac{1}{2\pi R_1C_2}$$

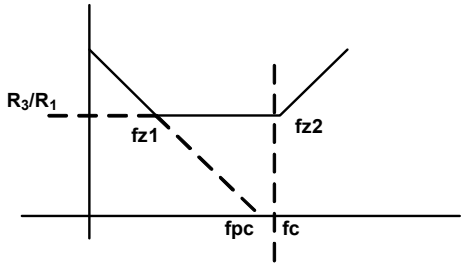


FIGURE 39. POWER TRAIN FREQUENCY RESPONSE

Design example: V_{IN} = 12V, V_O = 1.8V, I_O = 10A, f_{SW} = 600kHz, R_1 = 200kΩ, R_2 = 100kΩ, C_o = 3x100µF/3mΩ 6.3V ceramic (actually ~150µF), L = 0.68µH.

Select f_c = 80kHz. The gain of the Gp(s)xAv(s) should has a unity gain at crossover frequency. Thus, R_3 can be derived as:

$$R_3 = 2\pi f_c C_o R_t R_1 = 829k\Omega \quad \text{(EQ. 17)}$$

Select 800kΩ for R_3. Place the zero f_{z1} around the pole fp to achieve -20db/dec roll off.

$$C_2 = \frac{(Ro + Rc) x C_o}{R_3} = 29pF \quad \text{(EQ. 18)}$$

where Rc is the ESR of the output capacitor.

Select 30pF for C_2. Zero f_{z2} is a phase boost zero to increase the phase margin. Place it between f_c and 1/2 switching frequency. In this case, 4.7pF capacitor is selected and the zero is placed at f_{z2}:

$$f_{z2} = \frac{1}{2\pi R_1 C_1} = 169kHz \quad \text{(EQ. 19)}$$

The calculated values for R_1, R_2, C_1, and R_3, C_2 match with the 1.8V output application in the recommended design with internal compensation shown in Table 1 on page 2. Do not select resistance higher than 370kΩ for R_1 in real applications to avoid parasitic impaction.

In practice, it is recommended to select lower resistance for R_1/R_2 and R_3 in the external compensation applications. Usually, 10 times lower compared with the internal compensation is a good start.

Layout Considerations

The layout is very important in high frequency switching converter design. With power devices switching efficiently at 600kHz, the resulting current transitions from one device to another causing voltage spikes across the interconnecting impedances and parasitic circuit elements. These voltage spikes can degrade efficiency, radiate noise into the circuit and lead to device overvoltage stress. Careful component layout and printed circuit board design minimizes these voltage spikes.

As an example, consider the turn-off transition of the upper MOSFET. Prior to turn-off, the MOSFET is carrying the full load current. During turn-off, current stops flowing in the MOSFET and is picked up by the internal body diode of the low-side MOSFET. Any parasitic inductance in the switched current path generates a large voltage spike during the switching interval. Careful component selection, tight layout of the critical components, and short, wide traces minimize the magnitude of voltage spikes.

A multilayer printed circuit board is recommended. Figures 40 and 41 show the recommended layout of the top layer and the inner Layer 1 of the schematic in Figure 1 on page 1.

1. Place the input ceramic capacitors between PVIN and GND pins. Put them as close to the pins as possible.
2. A 1µF decoupling input ceramic capacitor is recommended. Place it as close to the VIN pin as possible.
3. A 2.2µF decoupling ceramic capacitor is recommended for VDD pin. Place it as close to the VDD pin as possible.
4. The entire inner Layer 1 is recommended to be the GND plane in order to reduce the noise coupling.
5. The switching node (PHASE) plane needs to be kept away from the feedback network. Place the resistor divider close to the IC.
6. Put three to five vias on the GND pin to connect the GND plane of other layers for better thermal performance. This allows the heat to move away from the IC. Keep the vias small but not so small that their inside diameter prevents solder wicking through the holes during reflow. An 8 mil hole with 15 mil diameter vias are used on the evaluation board. Do not use “thermal relief” patterns to connect the vias. It is important to have a complete connection of the plated-through hole to each plane.

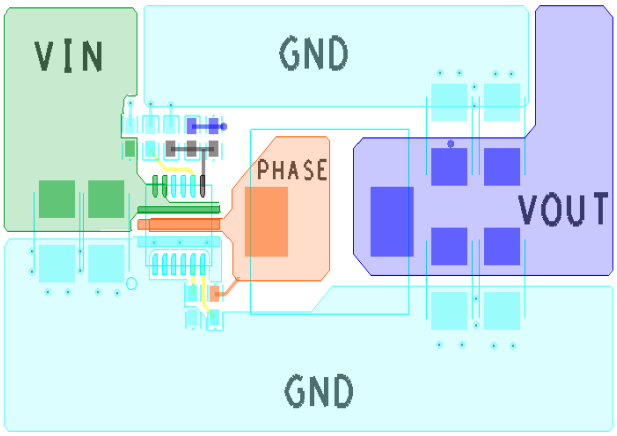


FIGURE 40. RECOMMENDED TOP LAYER LAYOUT

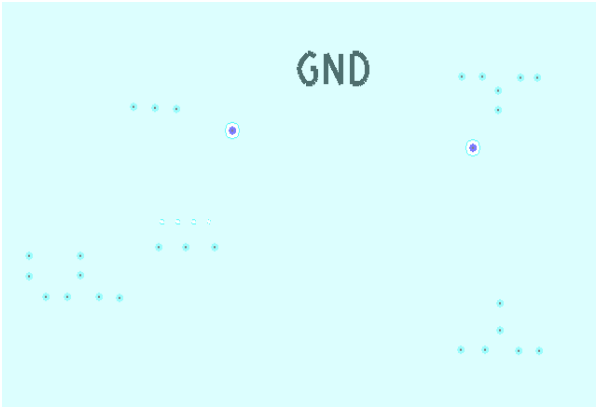


FIGURE 41. SOLID GND PLANE OF INNER LAYER 1

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure that you have the latest revision.

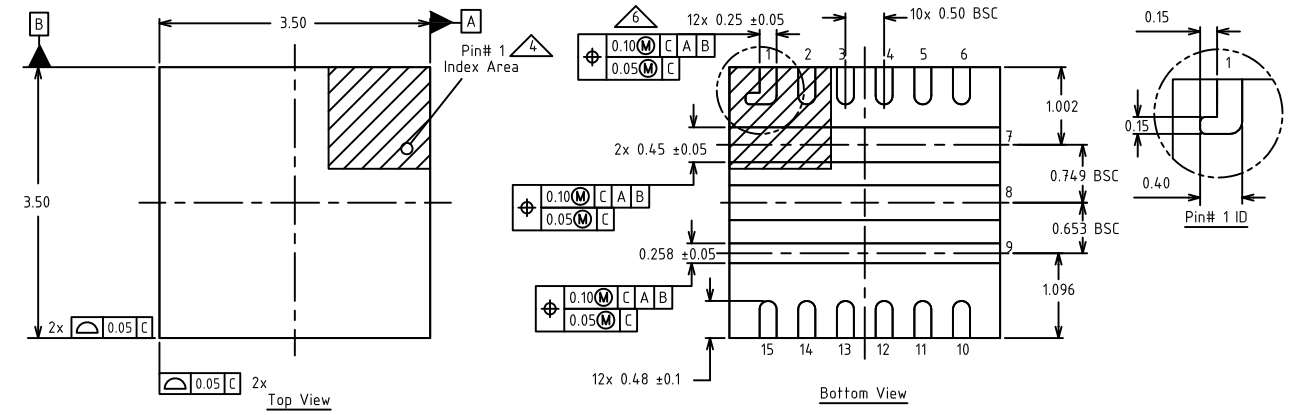
DATE	REVISION	CHANGE
Nov 11, 2021	4.00	Removed Related Literature section Updated Ordering Information table formatting. Updated POD L15.3.5x3.5 to the latest version, changes are as follows. -Revised pin#1 L-shape width from 0.37 to 0.4 to reflect actual dimension.
Jul 31, 2020	3.00	Updated the abs max section by changing the maximum rating of the following from +24V to +22V • VIN, EN to GND • PVIN to GND • PHASE to GND .... (DC) • PHASE to GND —(40ns) On page 6 changed the FB Regulation Voltage parameter minimum value from 0.588 to 0.5895 and the maximum value from 0.612 to 0.6105. Removed About Intersil section
Mar 17, 2017	2.00	In “Power-Good” on page 13, updated 88% to 87% and 114% to 113%. Updated verbiage above Equation 7. Updated Equations 10 and 18. Updated verbiage above Equations 17 (changed 60kHz to 80kHz), 18 (changed 800Ω to 800kΩ), 19 (changed R3 to C2). Updated Layout Considerations for more clarification.
Jan 5, 2017	1.00	Updated ordering information table to remove bulk part and add tape and reel versions. Added Table 2 on page 2. Added the last two sentences in 1st paragraph in “Enable and Soft-Start” on page 11 to instruct how to use the EN pin.
Oct 3, 2016	0.00	Initial Release

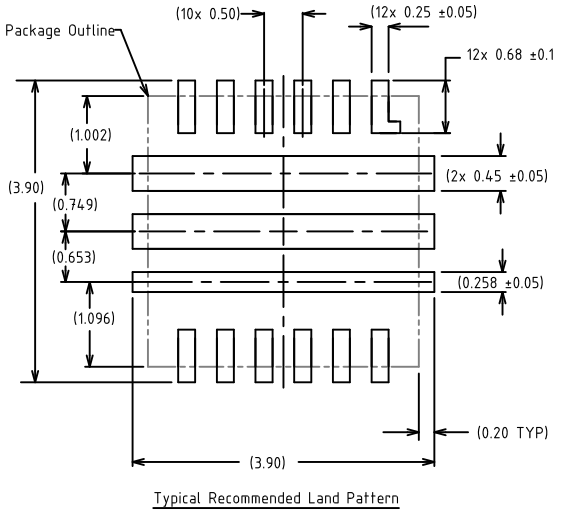
Package Outline Drawing

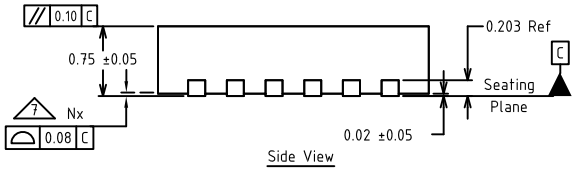
For the most recent package outline drawing, see L15.3.5x3.5.

L15.3.5x3.5

15 Lead Thin Quad Flat No-Lead Package (TQFN)
Rev 3, 10/2021







NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-2009.
2. All dimensions are in millimeters.
3. N is the total number of terminals.
4. The location of the marked terminal #1 identifier is within the hatched area.
5. ND and NE refer to the number of terminals on D and E side respectively.
6. Dimension applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has a radius on the other end of it, dimension b should not be measured in that radius area.
7. Coplanarity applies to the terminals and all other bottom surface metallization.

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