ISL9110A

1.2A High Efficiency Buck-Boost Regulator

FN8299
Rev 1.01
Oct 6, 2022

The ISL9110A is a highly-integrated Buck-Boost switching regulator that accepts input voltages either above or below the regulated output voltage. Unlike other Buck-Boost regulators, this regulator automatically transitions between operating modes without significant output disturbance.

This part is capable of delivering up to 1.2A output current, and provides excellent efficiency due to its fully synchronous 4-switch architecture. No-load quiescent current of only 35µA also optimizes efficiency under light-load conditions. Forced PWM and/or synchronization to an external clock may also be selected for noise sensitive applications.

The ISL9110A is designed for standalone applications and supports 3.3V and 5V fixed output voltages or variable output voltages with an external resistor divider. Output voltages as low as 1V, or as high as 5.2V are supported using an external resistor divider.

The ISL9110A requires only a single inductor and very few external components. Power supply solution size is minimized by a 2.4mm x 1.6mm WLCSP package and a 2.5MHz switching frequency, which further reduces the size of external components.

Features

- Accepts Input Voltages Above or Below Regulated Output Voltage
- Automatic and Seamless Transitions Between Buck and Boost Modes
- Input Voltage Range: 1.8V to 5.5V
- Output Current: Up to 1.2A
- High Efficiency: Up to 95%
- 35µA Quiescent Current Maximizes Light-load Efficiency
- 2.5MHz Switching Frequency Minimizes External Component Size
- Selectable Forced-PWM Mode and External Synchronization
- Fully Protected for Overcurrent, Over-temperature and Undervoltage
- Small 2.4mmx1.6mm WLCSP Package

Applications

- Regulated 3.3V from a Single Li-Ion Battery
- Smart Phones and Tablet Computers
- Handheld Devices
- Point-of-Load Regulators

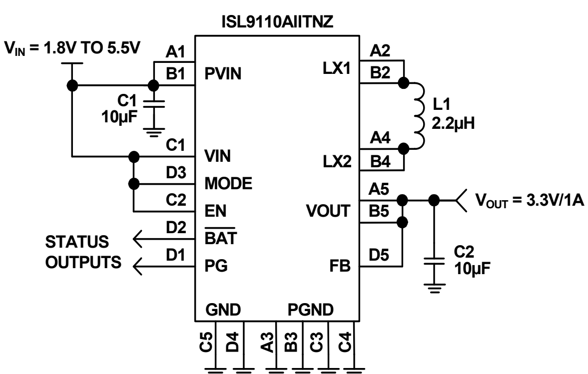


FIGURE 1. TYPICAL APPLICATION

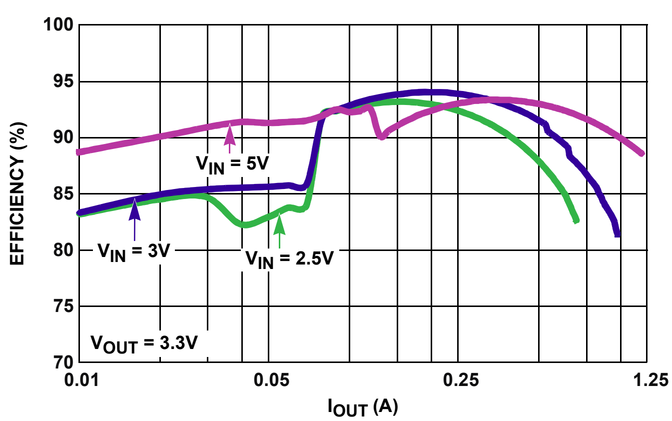
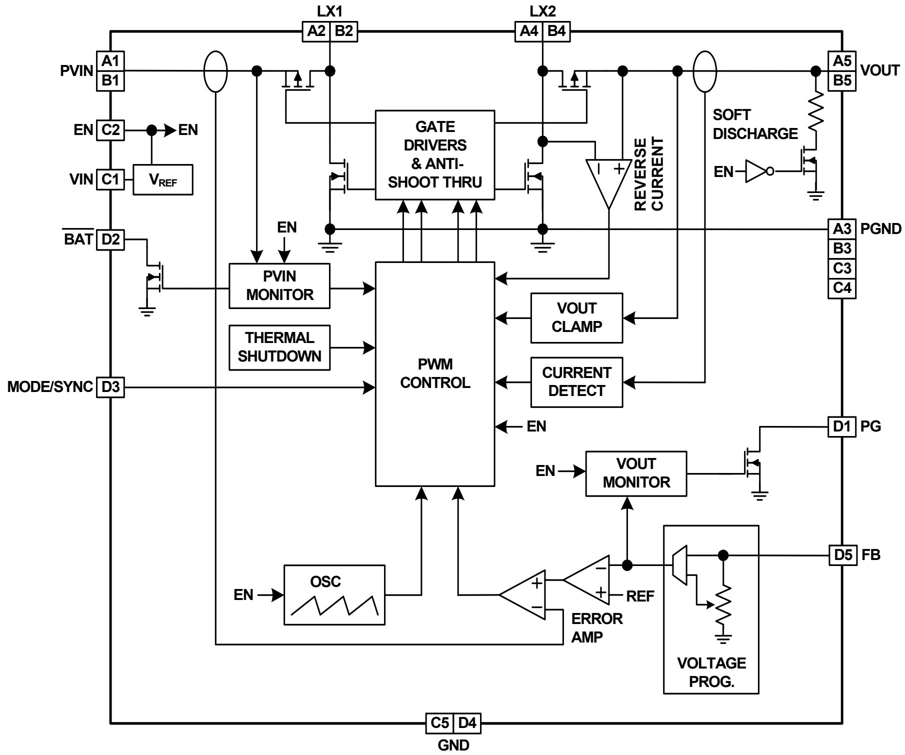


FIGURE 2. EFFICIENCY

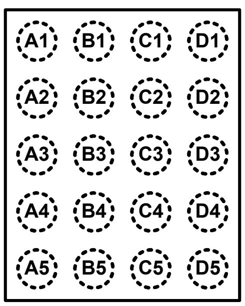
Table of Contents

Block Diagram



Pin Configurations

ISL9110A
(20 BALL WLCSP)
TOP VIEW



Pin Descriptions

PIN #	PIN NAMES	DESCRIPTION
A5, B5	VOUT	Buck/boost output. Connect a 10µF capacitor to PGND.
A4, B4	LX2	Inductor connection, output side.
A3, B3, C3, C4	PGND	Power ground for high switching current.
A2, B2	LX1	Inductor connection, input side.
A1, B1	PVIN	Power input. Range: 1.8V to 5.5V. Connect a 10µF capacitor to PGND.
C1	VIN	Supply input. Range: 1.8V to 5.5V.
D1	PG	Open drain output. Provides output-power-good status.
D2	$\overline{\text{BAT}}$	Open drain output. Provides input-power-good status.
C2	EN	Logic input, drive high to enable device.
D3	MODE/ SYNC	Logic input, high for auto PFM mode. Low for forced PWM operation. Ext. clock sync input. Range: 2.75MHz to 3.25MHz.
C5, D4	GND	Analog ground pin.
D5	FB	Voltage feedback pin.

Ordering Information

PART NUMBER (Notes 2, 3)	PART MARKING	V_{OUT} (V)	PACKAGE DESCRIPTION (RoHS Compliant)	PKG. DWG. #	CARRIER TYPE (Note 1)	TEMP. RANGE
ISL9110AIITNZ-T	DZBE	3.3	20 Ball WLCSP	W4x5.20S	Reel, 3k	-40 to +85°C
ISL9110AIITAZ-T	DZBD	ADJ				

NOTES:

1. Please see TB347 for details about reel specifications.
2. These Pb-free WLCSP packaged products employ special Pb-free material sets; molding compounds/die attach materials and SnAgCu - e1 solder ball terminals, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free WLCSP packaged products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), see the ISL9110A product information page. For more information about MSL, see TB363.

Absolute Maximum Ratings

PVIN, VIN . . . . -0.3V to 6.5V
LX1, LX2 (Note 6) . . . . -0.3V to 6.5V
FB (Adjustable Version) . . . . -0.3V to 2.7V
FB (Fixed V_{OUT} Versions) . . . . -0.3V to 6.5V
GND, PGND . . . . -0.3V to 0.3V
All Other Pins . . . . -0.3V to 6.5V
ESD Rating
Human Body Model (Tested per JESD22-A114E). 3kV
Machine Model (Tested per JESD22-A115-A) 250V
Latch Up (Tested per JESD-78B; Class 2, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
20 Ball WLSCP Package (Notes 4, 5)	66	1

Maximum Junction Temperature . . . .+125°C
Storage Temperature Range. . . . .-65°C to +150°C
Pb-Free Reflow Profile . . . . see TB493

Recommended Operating Conditions

Ambient Temperature Range . . . .-40°C to +85°C
Supply Voltage Range . . . . 1.8V to 5.5V
Load Current Range . . . . 0A to 1.2A

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with direct attach features. See TB379
5. For θ_{JC}, the case temperature location is taken at the package top center.
6. LX1 and LX2 pins can withstand switching transients of -1.5V for 100ns, and 7V for 20ms.

Analog Specifications

$V_{VIN} = V_{PVIN} = V_{EN} = 3.6V$, $V_{OUT} = 3.3V$, L1 = 2.2µH, C1 = C2 = 10µF, T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP (Note 8)	MAX (Note 7)	UNIT
POWER SUPPLY						
Input Voltage Range	V_{IN}		**1.8**		**5.5**	V
V_{IN} Undervoltage Lockout Threshold	V_{UVLO}	Rising		1.725	**1.775**	V
		Falling	**1.550**	1.650		V
V_{IN} Supply Current	I_{VIN}	PFM mode, no external load on Vout (Note 9)		35	**60**	µA
V_{IN} Supply Current, Shutdown	I_{SD}	EN = GND, V_{IN} = 3.6V		0.05	**1.0**	µA
OUTPUT VOLTAGE REGULATION						
Output Voltage Range	V_{OUT}	ISL9110AIITAZ, I_{OUT} = 100mA	**1.00**		**5.20**	V
Output Voltage Accuracy		V_{IN} = 3.7V, V_{OUT} = 3.3V, I_{OUT} = 0mA, PWM mode	**-2**		**+2**	%
		V_{IN} = 3.7V, V_{OUT} = 3.3V, I_{OUT} = 1mA, PFM mode	**-3**		**+4**	%
FB Pin Voltage Regulation	V_{FB}	For adjustable output version	**0.79**	0.80	**0.81**	V
FB Pin Bias Current	I_{FB}	For adjustable output version			**1**	µA
Line Regulation, PWM Mode	$\Delta V_{OUT}/\Delta V_{IN}$	I_{OUT} = 500mA, V_{OUT} = 3.3V, MODE = GND, V_{IN} step from 2.3V to 5.5V		±0.005		mV/mV
Load Regulation, PWM Mode	$\Delta V_{OUT}/\Delta I_{OUT}$	V_{IN} = 3.7V, V_{OUT} = 3.3V, MODE = GND, I_{OUT} step from 0mA to 500mA		±0.005		mV/mA
Line Regulation, PFM Mode	$\Delta V_{OUT}/\Delta V_I$	I_{OUT} = 100mA, V_{OUT} = 3.3V, MODE = V_{IN}, V_{IN} step from 2.3V to 5.5V		±12.5		mV/V
Load Regulation, PFM Mode	$\Delta V_{OUT}/\Delta I_{OUT}$	V_{IN} = 3.7V, V_{OUT} = 3.3V, MODE = V_{IN}, I_{OUT} step from 0mA to 100mA		±0.4		mV/mA
Output Voltage Clamp	V_{CLAMP}	Rising, V_{IN} = 3.6V	**5.25**		**5.95**	V
Output Voltage Clamp Hysteresis		V_{IN} = 3.6V		400		mV
DC/DC SWITCHING SPECIFICATIONS						
Oscillator Frequency	f_{SW}		**2.25**	2.50	**2.75**	MHz
Minimum On Time	t_{ONMIN}			80		ns
LX1 Pin Leakage Current	$I_{PFETLEAK}$		**-1**		**1**	µA
LX2 Pin Leakage Current	$I_{NFETLEAK}$		**-1**		**1**	µA

Analog Specifications $V_{VIN} = V_{PVIN} = V_{EN} = 3.6V$, $V_{OUT} = 3.3V$, L1 = 2.2µH, C1 = C2 = 10µF, T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP (Note 8)	MAX (Note 7)	UNIT
SOFT-START and SOFT DISCHARGE						
Soft-Start Time	t_{SS}	Time from when EN signal asserts to when output voltage ramp starts.		1		ms
		Time from when output voltage ramp starts to when output voltage reaches 95% of its nominal value with device operating in buck mode. $V_{IN} = 4V$, $V_{OUT} = 3.3V$, $I_O = 200mA$		1		ms
		Time from when output voltage ramp starts to when output voltage reaches 95% of its nominal value with device operating in boost mode. $V_{IN} = 2V$, $V_{OUT} = 3.3V$, $I_O = 200mA$		2		ms
V_{OUT} Soft-Discharge ON-Resistance	R_{DISCHG}	$V_{IN} = 3.6V$, EN < VIL		120		Ω
POWER MOSFET						
P-Channel MOSFET ON-Resistance	R_{DSON_P}	$V_{IN} = 3.6V$, $I_O = 200mA$		0.10	**0.17**	Ω
		$V_{IN} = 2.5V$, $I_O = 200mA$		0.13	**0.23**	Ω
N-Channel MOSFET ON-Resistance	R_{DSON_N}	$V_{IN} = 3.6V$, $I_O = 200mA$		0.09	**0.15**	Ω
		$V_{IN} = 2.5V$, $I_O = 200mA$		0.11	**0.23**	Ω
P-Channel MOSFET Peak Current Limit	I_{PK_LMT}	$V_{IN} = 3.6V$	**2.0**	2.4	**2.8**	A
PFM/PWM TRANSITION						
Load Current Threshold, PFM to PWM		$V_{IN} = 3.6V$, $V_{OUT} = 3.3V$		200		mA
Load Current Threshold, PWM to PFM		$V_{IN} = 3.6V$, $V_{OUT} = 3.3V$		75		mA
External Synchronization Frequency Range			**2.75**		**3.25**	MHz
Thermal Shutdown				155		°C
Thermal Shutdown Hysteresis				30		°C
BATTERY MONITOR AND POWER GOOD COMPARATORS						
Battery Monitor Voltage Threshold	VT_{BMON}		**1.85**	2.0	**2.15**	V
Battery Monitor Voltage Hysteresis	VH_{BMON}			100		mV
Battery Monitor Debounce Time	t_{BMON}			25		µs
PG Delay Time (Rising)				1		ms
PG Delay Time (Falling)				20		µs
Minimum Supply Voltage for Valid PG Signal		EN = VIN	**1.2**			V
PG Range - Lower (Rising)	PG_{RNGLR}	Percentage of programmed voltage		90		%
PG Range - Lower (Falling)	PG_{RNGLF}	Percentage of programmed voltage		87		%
PG Range - Upper (Rising)	PG_{RNGUR}	Percentage of programmed voltage		112		%
PG Range - Upper (Falling)	PG_{RNGUF}	Percentage of programmed voltage		110		%
Compliance Voltage - PG, $\overline{BAT}$		$V_{IN} = 3.6V$, $I_{SINK} = 1mA$			**0.3**	V

Analog Specifications

$V_{VIN} = V_{PVIN} = V_{EN} = 3.6V$, $V_{OUT} = 3.3V$, L1 = 2.2µH, C1 = C2 = 10µF, $T_A = +25°C$. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP (Note 8)	MAX (Note 7)	UNIT
LOGIC INPUTS						
Input Leakage	I_{LEAK}			0.05	**1**	µA
Input HIGH Voltage	V_{IH}		**1.4**			V
Input LOW Voltage	V_{IL}				**0.4**	V

NOTES:

7. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
8. Typical values are for $T_A = +25°C$ and $V_{IN} = 3.6V$.
9. Quiescent current measurements are taken when the output is not switching.

Typical Performance Curves

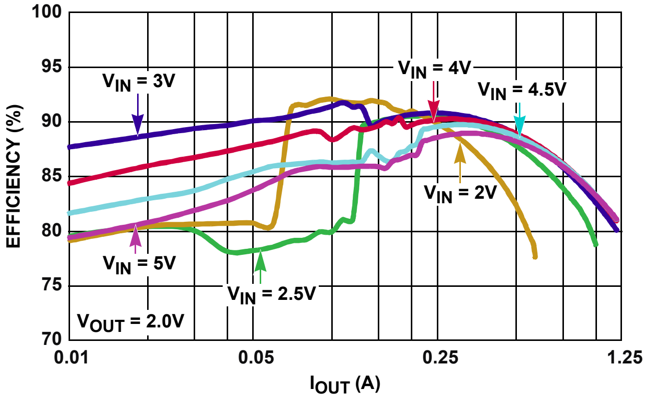


FIGURE 3. EFFICIENCY vs OUTPUT CURRENT, V_{OUT} = 2V

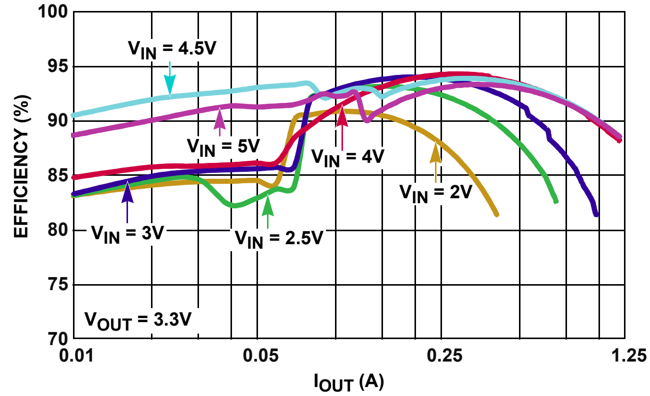


FIGURE 4. EFFICIENCY vs OUTPUT CURRENT, V_{OUT} = 3.3V

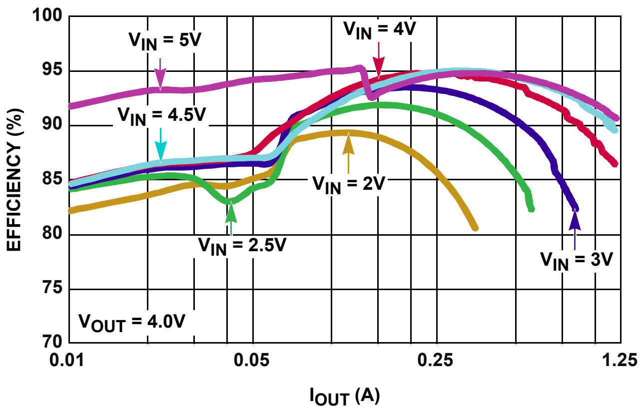


FIGURE 5. EFFICIENCY vs OUTPUT CURRENT, V_{OUT} = 4V

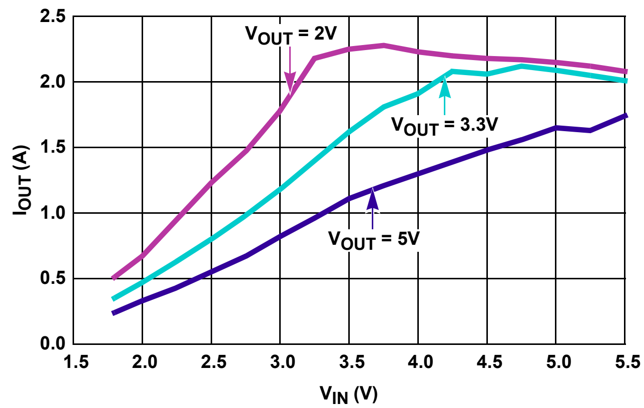


FIGURE 6. MAXIMUM OUTPUT CURRENT vs INPUT VOLTAGE

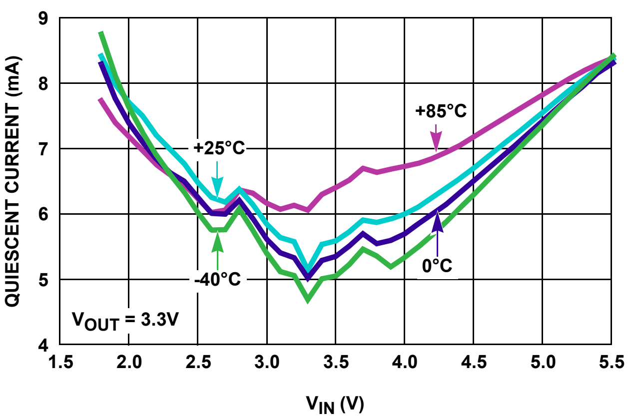


FIGURE 7. PWM MODE QUIESCENT CURRENT, V_{OUT} = 3.3V, NO LOAD

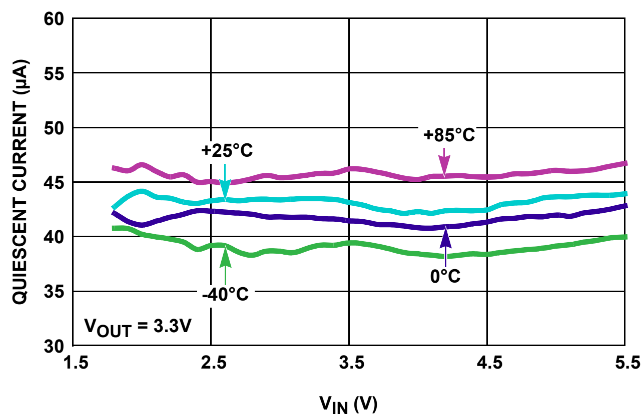


FIGURE 8. PFM MODE QUIESCENT CURRENT, V_{OUT} = 3.3V, NO LOAD

Typical Performance Curves (Continued)

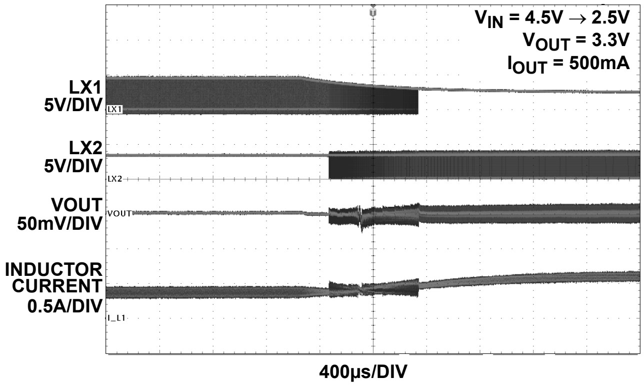


FIGURE 9. STEADY STATE TRANSITION FROM BUCK TO BOOST

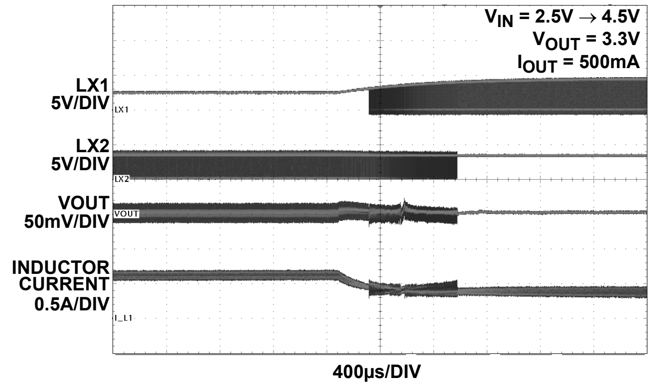


FIGURE 10. STEADY STATE TRANSITION FROM BOOST TO BUCK

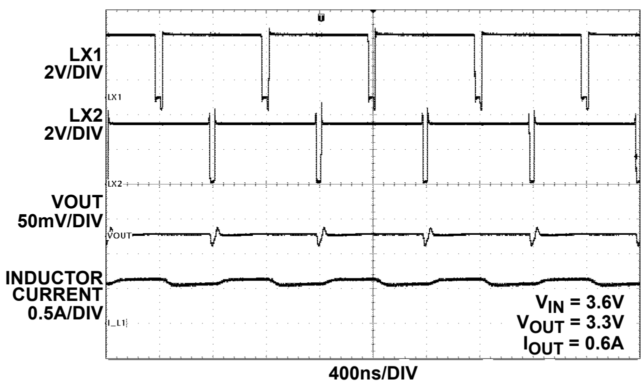


FIGURE 11. STEADY STATE V_{IN} NEAR V_{OUT}

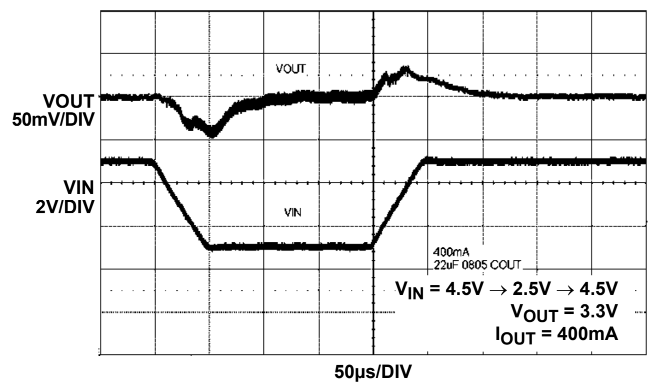


FIGURE 12. INPUT TRANSIENT

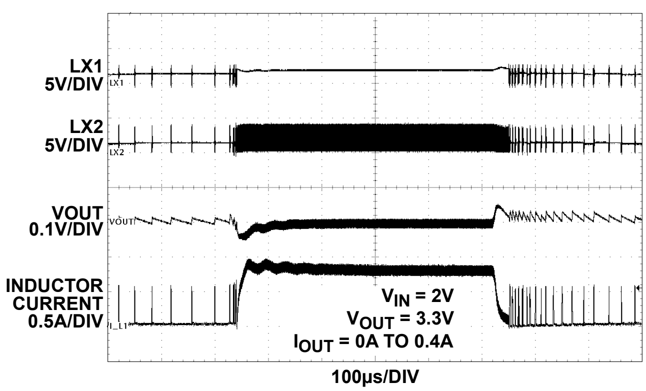


FIGURE 13. TRANSIENT LOAD RESPONSE

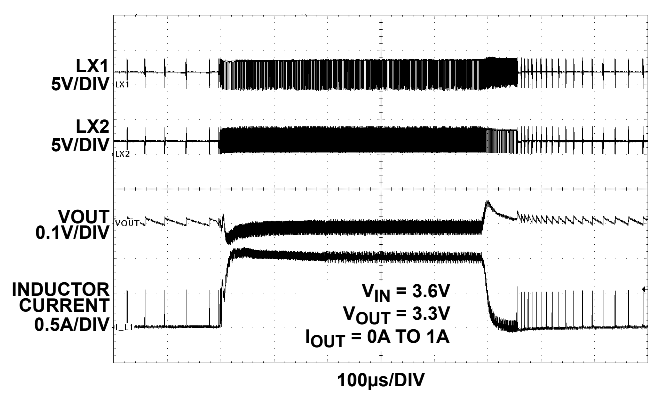


FIGURE 14. TRANSIENT LOAD RESPONSE

Typical Performance Curves (Continued)

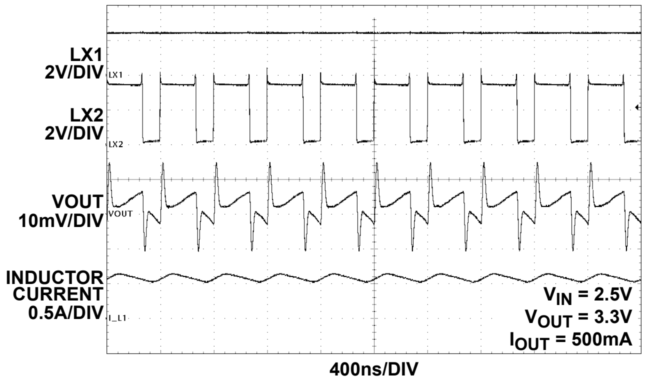


FIGURE 15. SWITCHING WAVEFORMS, BOOST MODE

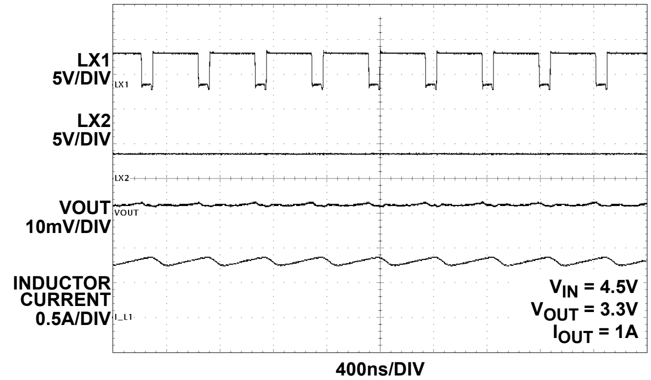


FIGURE 16. SWITCHING WAVEFORMS, BUCK MODE

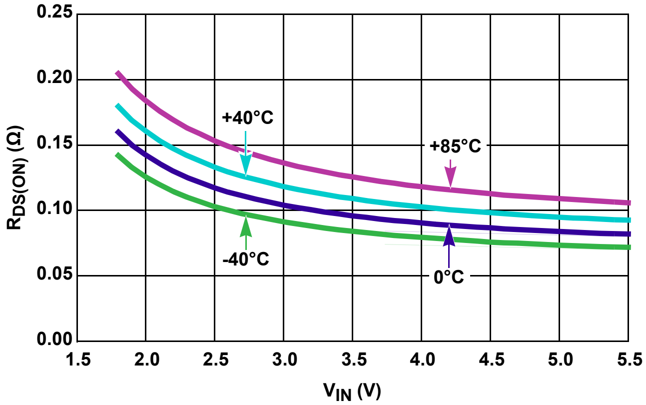


FIGURE 17. NFET $r_{DS(ON)}$ vs INPUT VOLTAGE

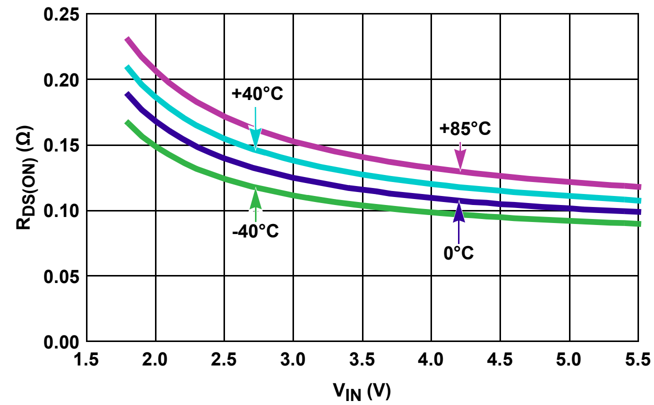


FIGURE 18. PFET $r_{DS(ON)}$ vs INPUT VOLTAGE

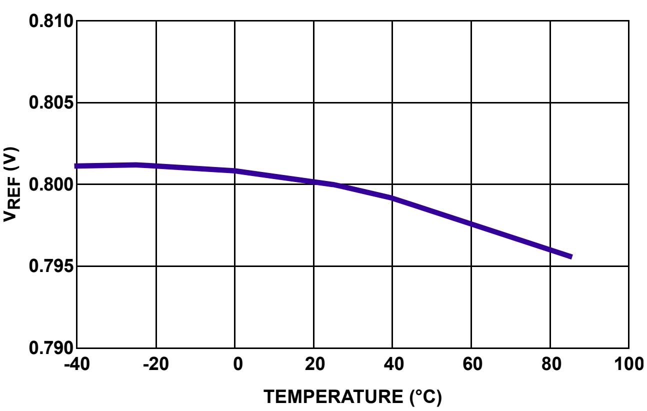


FIGURE 19. V_{REF} vs TEMPERATURE, T_A = -40°C TO +85°C

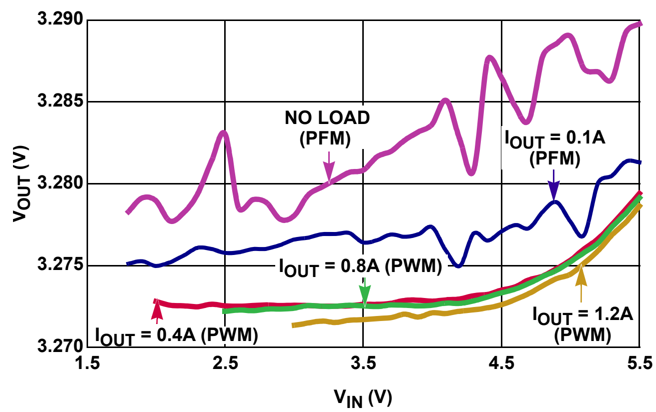


FIGURE 20. OUTPUT VOLTAGE vs V_{IN} VOLTAGE (V_{OUT} = 3.3V)

Typical Performance Curves (Continued)

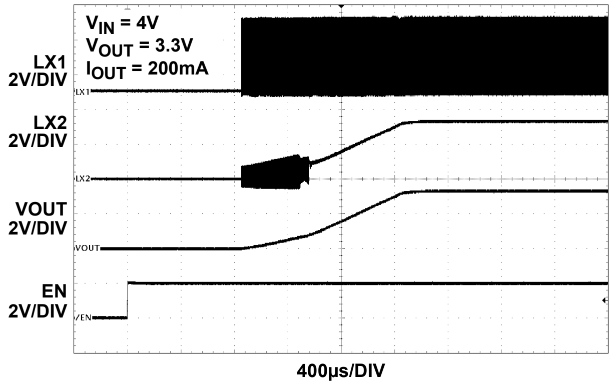


FIGURE 21. SOFT-START, V_{IN} = 4V, V_{OUT} = 3.3V

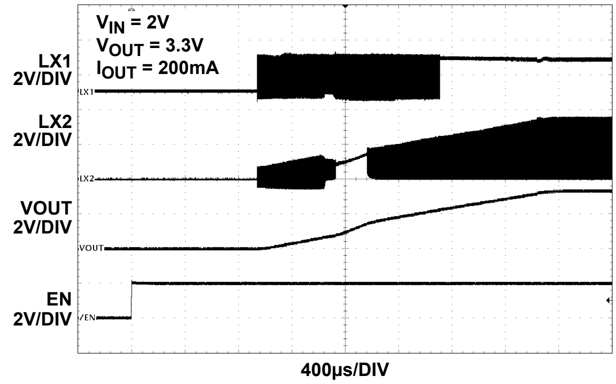


FIGURE 22. SOFT-START, V_{IN} = 2V, V_{OUT} = 3.3V

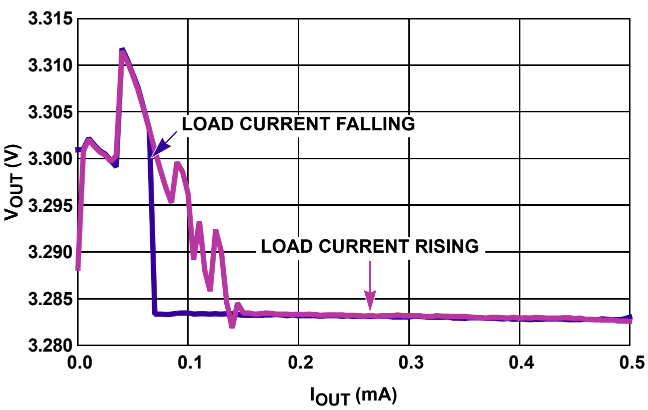


FIGURE 23. OUTPUT VOLTAGE vs LOAD CURRENT (V_{IN} = 2.5V, V_{OUT} = 3.3V, AUTO PFM/PWM MODE)

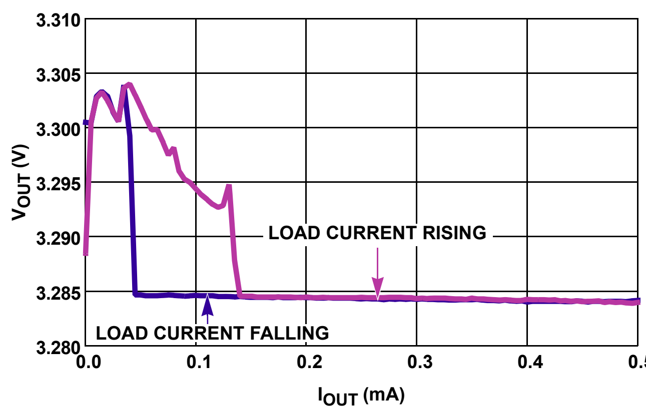


FIGURE 24. OUTPUT VOLTAGE vs LOAD CURRENT (V_{IN} = 4.5V, V_{OUT} = 3.3V, AUTO PFM/PWM MODE)

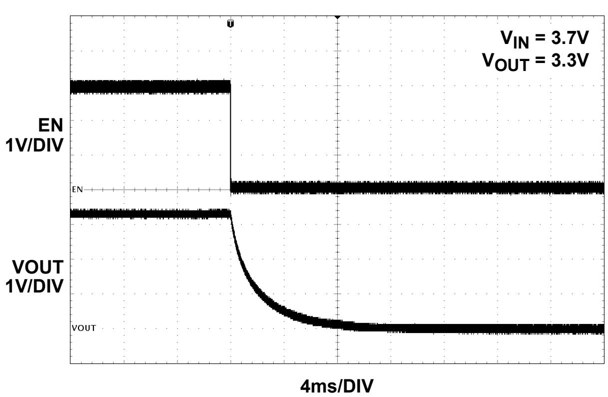


FIGURE 25. OUTPUT SOFT-DISCHARGE

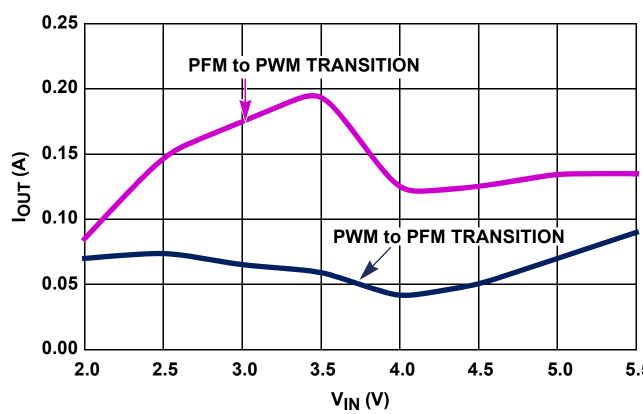


FIGURE 26. PFM to PWM MODE CHANGE THRESHOLD CURRENT vs INPUT VOLTAGE (V_{OUT} = 3.3V)

Functional Description

Functional Overview

Refer to the “Block Diagram” on page 3. The ISL9110A implements a complete buck boost switching regulator, with PWM controller, internal switches, references, protection circuitry, and control inputs.

The PWM controller automatically switches between buck and boost modes as necessary to maintain a steady output voltage, with changing input voltages and dynamic external loads.

The ISL9110A provides output-power-good and input-power-good open-drain status outputs on pins 7 and 8.

Internal Supply and References

Referring to the “Block Diagram” on page 3, the ISL9110A provides two power input pins. The PVIN pin supplies input power to the DC/DC converter, while the VIN pin provides operating voltage source required for stable V_{REF} generation. Separate ground pins (GND and PGND) are provided to avoid problems caused by ground shift due to the high switching currents.

Enable Input

A master enable pin EN allows the device to be enabled. Driving EN low invokes a power-down mode, where most internal device functions, including input and output power good detection, are disabled.

Soft Discharge

When the device is disabled by driving EN low, an internal resistor between V_{OUT} and GND is activated. This internal resistor has a typical 120Ω resistance.

POR Sequence and Soft-start

Bringing the EN pin high allows the device to power-up. A number of events occur during the start-up sequence. The internal voltage reference powers up, and stabilizes. The device then starts operating. There is a typical 1ms delay between assertion of the EN pin and the start of switching regulator soft-start ramp.

The soft-start feature minimizes output voltage overshoot and input inrush currents. During soft-start, the reference voltage is ramped to provide a ramping V_{OUT} voltage. While output voltage is lower than approximately 20% of the target output voltage, switching frequency is reduced to a fraction of the normal switching frequency to aid in producing low duty cycles necessary to avoid input inrush current spikes. Once the output voltage exceeds 20% of the target voltage, switching frequency is increased to its nominal value.

When the target output voltage is higher than the input voltage, there will be a transition from buck mode to boost mode during the soft-start sequence. At the time of this transition, the ramp rate of the reference voltage is decreased, such that the output voltage slew rate is decreased. This provides a slower output voltage slew rate.

The V_{OUT} ramp time is not constant for all operating conditions. Soft-start into boost mode will take longer than soft-start into buck mode. The total soft-start time into buck operating mode is typically 2ms, whereas the typical soft-start time into boost mode operating mode is typically 3ms. Increasing the load current will increase these typical soft-start times.

Overcurrent Protection

When the current in the P-Channel MOSFET is sensed to reach the current limit for 16 consecutive switching cycles, the internal protection circuit is triggered, and switching is stopped for approximately 20ms. The device then performs a soft-start cycle. If the external output overcurrent condition exists after the soft-start cycle, the device will again detect 16 consecutive switching cycles reaching the peak current threshold. The process will repeat as long as the external overcurrent condition is present. This behavior is called ‘hiccup mode’.

Short-Circuit Protection

The ISL9110A provides short-circuit protection by monitoring the feedback voltage. When feedback voltage is sensed to be lower than a certain threshold, the PWM oscillator frequency is reduced in order to protect the device from damage. The P-Channel MOSFET peak current limit remains active during this state.

Undervoltage Lockout

The undervoltage lockout (UVLO) feature prevents abnormal operation in the event that the supply voltage is too low to guarantee proper operation. When the V_{IN} voltage falls below the UVLO threshold, the regulator is disabled.

PG Status Output

An open drain output-power-good signal is provided in the ISL9110A. An internal window comparator is used to detect when V_{OUT} is significantly higher or lower than the target output voltage. The PG output will be driven low when sensed V_{OUT} voltage is outside of this ‘power good’ window. When V_{OUT} voltage is inside the ‘power-good’ window, the PG pin goes Hi-Z.

The PG detection circuit detects this condition by monitoring voltage on the FB pin. Hysteresis is provided for the upper and lower PG thresholds to avoid oscillation of the PG output.

$\overline{BAT}$ Status Output

The ISL9110A provides an open drain input-power-good status output. The $\overline{BAT}$ status pin will be driven low when V_{IN} rises above the VT_{BMON} threshold. The $\overline{BAT}$ status output goes Hi-Z when V_{BAT} falls below the VT_{BMON} threshold. Hysteresis is provided for the VT_{BMON} threshold to avoid oscillation of the $\overline{BAT}$ output.

Ultrasonic Mode

(Available Upon Request)

The ISL9110A provides an ultrasonic mode that can be enabled during IC manufacturing upon request.

In ultrasonic mode, the PFM switching frequency is forced to be above the audio frequency range.

This ultrasonic mode applies only to PFM mode operation. When enabled, the PFM mode switching frequency is forced well above the audio frequency range (f_{SW} becomes typically 60kHz). This mode of operation, however, reduces the efficiency at light load.

Thermal Shutdown

A built-in thermal protection feature protects the ISL9110A, if the die temperature reaches +155°C (typical). At this die temperature, the regulator is completely shut down. The die temperature continues to be monitored in this thermal-shutdown mode. When the die temperature falls to +125°C (typical), the device will resume normal operation.

When exiting thermal shutdown, the ISL9110A will execute its soft-start sequence.

External Synchronization

An external sync feature is provided. Applying a clock signal with a frequency between 2.75MHz and 3.25MHz at the MODE/SYNC input forces the ISL9110A to synchronize to this external clock. The MODE/SYNC input supports standard logic levels.

Buck-Boost Conversion Topology

The ISL9110A operates in either buck or boost mode. When operating in conditions where V_{IN} is close to V_{OUT}, the ISL9110A alternates between buck and boost mode as necessary to provide a regulated output voltage.

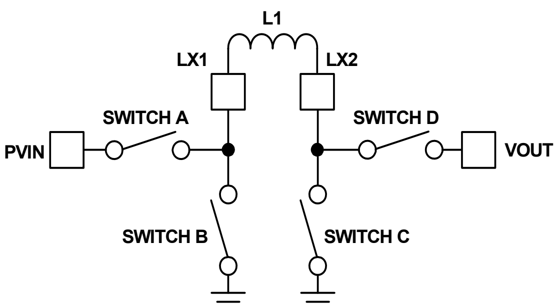


FIGURE 27. BUCK BOOST TOPOLOGY

Figure 27 shows a simplified diagram of the internal switches and external inductor.

PWM Operation

In buck PWM mode, Switch D is continuously closed, and Switch C is continuously open. Switches A and B operate as a synchronous buck converter when in this mode.

In boost PWM mode, Switch A remains closed and Switch B remains open. Switches C and D operate as a synchronous boost converter when in this mode.

PFM Operation

During PFM operation in buck mode, Switch D is continuously closed, and Switch C is continuously open. Switches A and B operate in discontinuous mode during PFM operation.

During PFM operation in boost mode, the ISL9110A closes Switch A and Switch C to ramp up the current in the inductor. When inductor current reaches a certain threshold, the device turns off Switches A and C, then turns on Switches B and D. With Switches B and D closed, output voltage increases as the inductor current ramps down.

In most operating conditions, there will be multiple PFM pulses to charge up the output capacitor. These pulses continue until V_{OUT} has achieved the upper threshold of the PFM hysteretic controller. Switching then stops, and remains stopped until V_{OUT} decays to the lower threshold of the hysteretic PFM controller.

Operation With V_{IN} Close to V_{OUT}

When the output voltage is close to the input voltage, the ISL9110A will rapidly and smoothly switch from boost to buck mode as needed to maintain the regulated output voltage. This behavior provides excellent efficiency and very low output voltage ripple.

Output Voltage Programming

The ISL9110A is available in fixed and adjustable output voltage versions. To use the fixed output version, the VOUT pin must be connected directly to FB.

In the adjustable output voltage version (ISL9110AIITAZ), an external resistor divider is required to program the output voltage. The FB pin has very low input leakage current, so it is possible to use large value resistors (e.g. R1 = 1MΩ and R2 = 324kΩ) in the resistor divider connected to the FB input.

Applications Information

Component Selection

The fixed-output version of the ISL9110A requires only three external power components to implement the buck boost converter: an inductor, an input capacitor, and an output capacitor.

The adjustable ISL9110A versions require three additional components to program the output voltage. Two external resistors program the output voltage, and a small capacitor is added to improve stability and response.

An optional input supply filtering capacitor (“C3” in Figure 28) can be used to reduce the supply noise on the VIN pin, which provides power to the internal reference. In most applications, this capacitor is not needed.

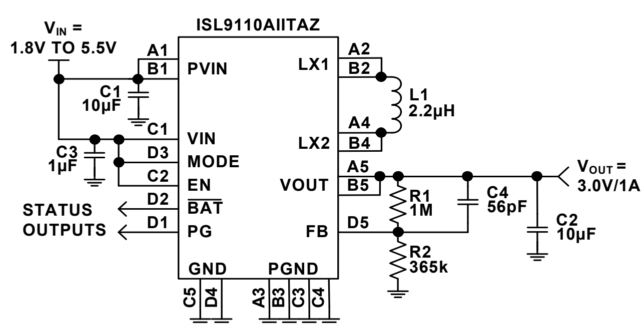


FIGURE 28. TYPICAL ISL9110AIITAZ APPLICATION

Output Voltage Programming, Adj. Version

Setting and controlling the output voltage of the ISL9110AIITAZ (adjustable output version) can be accomplished by selecting the external resistor values.

Equation 1 can be used to derive the R1 and R2 resistor values:

$$V_{OUT} = 0.8V \bullet \left(1 + \frac{R1}{R2}\right) \quad \text{(EQ. 1)}$$

When designing a PCB, include a GND guard band around the feedback resistor network to reduce noise and improve accuracy and stability. Resistors R1 and R2 should be positioned close to the FB pin.

Feed-Forward Capacitor Selection

A small capacitor (C4 in Figure 28) in parallel with resistor R1 is required to provide the specified load and line regulation. The suggested value of this capacitor is 56pF for R1 = 1MΩ. An NPO type capacitor is recommended.

Non-Adjustable Version FB Pin Connection

The fixed output versions of the ISL9110A does not require external resistors or a capacitor on the FB pin. Simply connect V_{OUT} to FB, as shown in Figure 29.

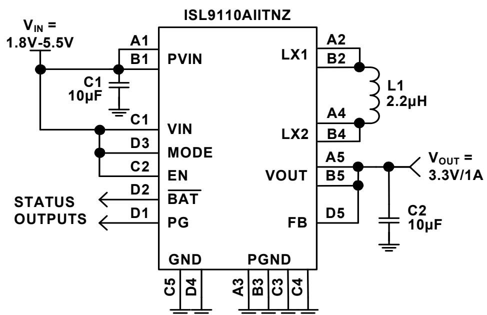


FIGURE 29. TYPICAL ISL9110AIITNZ APPLICATION

Inductor Selection

An inductor with high frequency core material (e.g. ferrite core) should be used to minimize core losses and provide good efficiency. The inductor must be able to handle the peak switching currents without saturating.

A 2.2µH inductor with ≥2.4A saturation current rating is recommended. Select an inductor with low DCR to provide good efficiency. In applications where radiated noise must be minimized, a toroidal or shielded inductor can be used.

TABLE 1. INDUCTOR VENDOR INFORMATION

MANUFACTURER	SERIES	WEBSITE
Coilcraft	LPS4018	www.coilcraft.com
Murata	LQH44P	www.murata.com
Taiyo Yuden	NRS4018 NRS5012	www.t-yuden.com
Sumida	CDRH3D23/HP CDRH4D22/HP	www.sumida.com
Toko	DEM3518C	www.toko.co.jp

PVIN and V_{OUT} Capacitor Selection

The input and output capacitors should be ceramic X5R type with low ESL and ESR. The recommended input capacitor value is 10µF. The recommended V_{OUT} capacitor value is 10µF to 22µF.

TABLE 2. CAPACITOR VENDOR INFORMATION

MANUFACTURER	SERIES	WEBSITE
AVX	X5R	www.avx.com
Murata	X5R	www.murata.com
Taiyo Yuden	X5R	www.t-yuden.com
TDK	X5R	www.tdk.com

Application Example 1

An application using the fixed-output ISL9110AIITNZ is shown in Figure 30. This application requires only three external components.

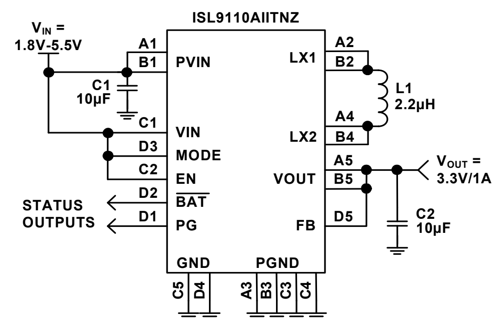


FIGURE 30. TYPICAL ISL9110AIITNZ APPLICATION

Application Example 2

An application requiring V_{OUT} = 3.0V, using the adjustable-output ISL9110AIITAZ is shown in Figure 31. This application requires six external components.

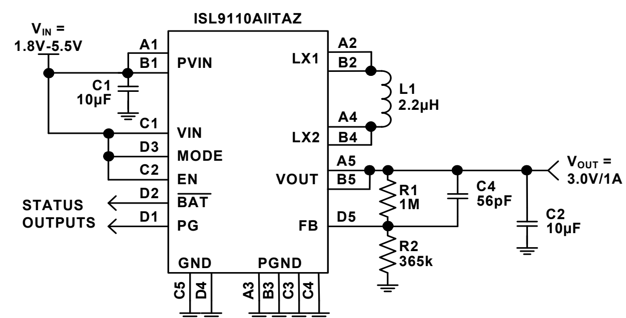


FIGURE 31. TYPICAL ISL9110AIITAZ APPLICATION

Recommended PCB Layout

Correct PCB layout is critical for proper operation of the ISL9110A. The input and output capacitors should be positioned as closely to the IC as possible. The ground connections of the input and output capacitors should be kept as short as possible, and should be on the component layer to avoid problems that are caused by high switching currents flowing through PCB vias.

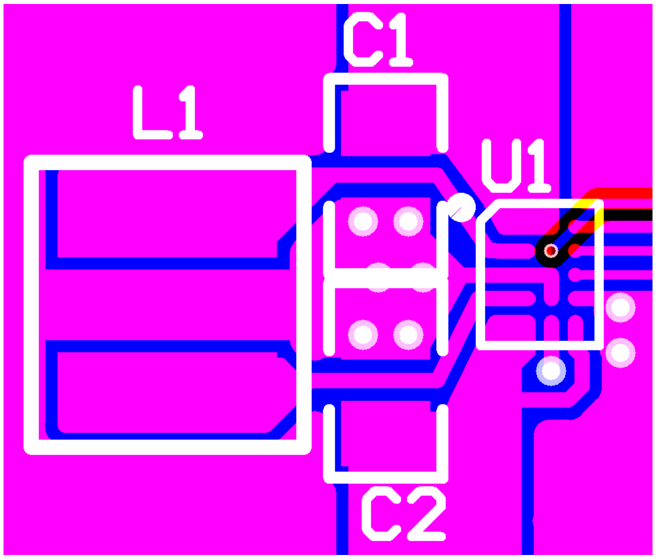


FIGURE 32. RECOMMENDED ISL9110AIITNZ PCB LAYOUT

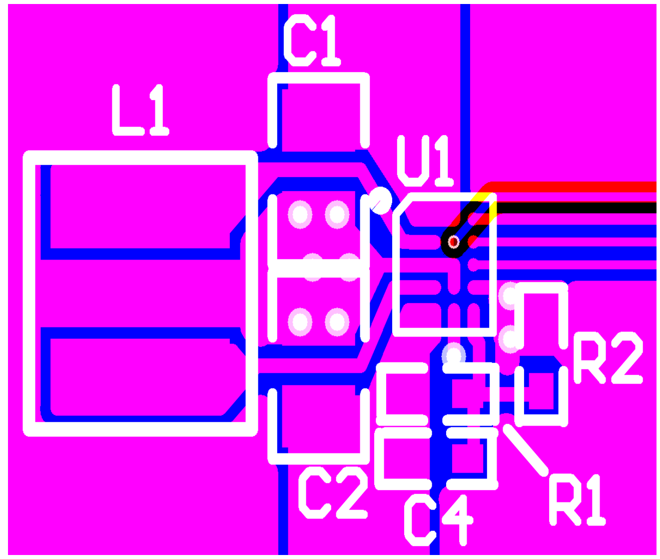


FIGURE 33. RECOMMENDED ISL9110AIITAZ PCB LAYOUT

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

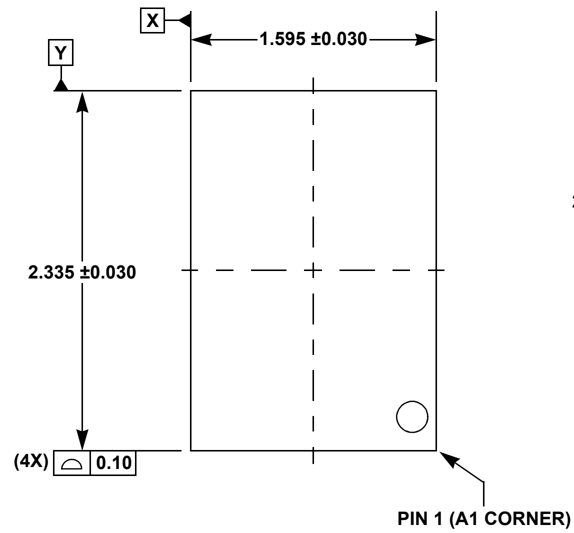
DATE	REVISION	CHANGE
Oct 6, 2022	1.01	Updated links throughout. Updated Ordering Information table formatting, removed eval board part numbers. Removed Related Literature section. Removed Products section. Changed POD from W4X5.20A to W4X5.20S.
May 29, 2012	1.00	Corrected “Pin Configuration” on page 3.
May 11, 2012	0.00	Initial Release.

Package Outline Drawing

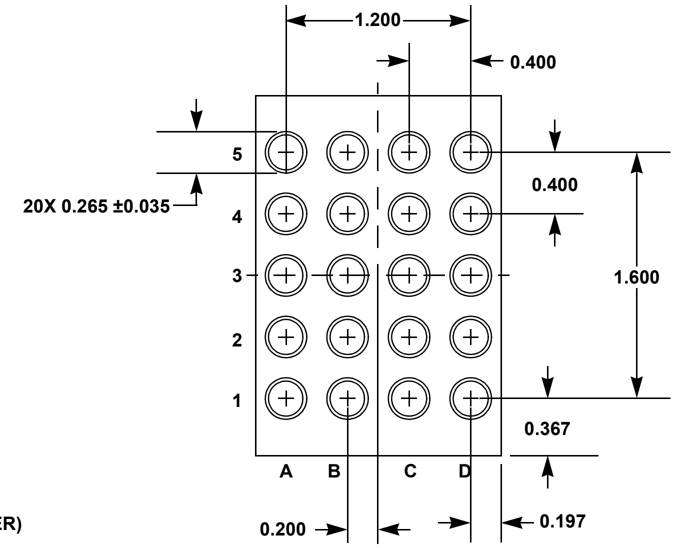
Rev 0, 12/16

For the most recent package outline drawing, see W4x5.20S.

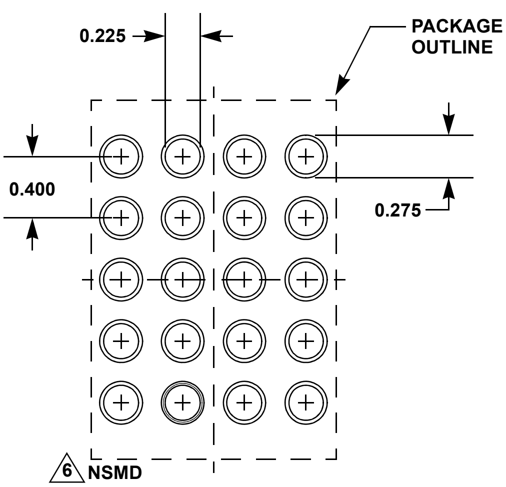
W4x5.20S
20 Ball Wafer Level Chip Scale Package (WLCSP)



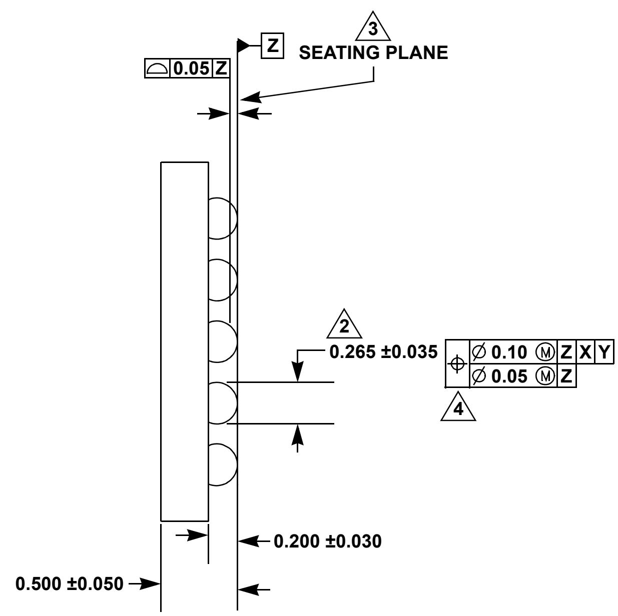
TOP VIEW



BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW

NOTES:

1. Dimensions and tolerance per ASME Y 14.5M - 1994.
2. Dimension is measured at the maximum bump diameter parallel to primary datum Z.
3. Primary datum Z and seating plane are defined by the spherical crowns of the bump.
4. Bump position designation per JESD 95-1, SPP-010.
5. All dimensions are in millimeters.
6. NSMD refers to non-solder mask defined pad design per Techbrief TB451.pdf

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