ISL91212A, ISL91212B

Triple/Quad Output PMIC with I²C Interface

FN8962
Rev.1.00
Feb 20, 2020

The ISL91212A is a four-phase, three output programmable Power Management IC (PMIC) and the ISL91212B is a four-phase, four output programmable PMIC. They are optimized with highly efficient synchronous buck converters capable of multiphase and single-phase operations that can deliver up to 5A per phase continuous output current. They feature four buck controllers and can reconfigure their power stages to these controllers. This flexibility allows seamless design-in for a wide range of applications that require high output power and small solution size.

The ISL91212A and ISL91212B integrate low ON-resistance MOSFETs and programmable PWM frequency, allowing the use of very small external inductors and capacitors. They feature automatic Diode Emulation and Pulse Skipping modes under light-load conditions to further improve efficiency and maximize battery life. The ISL91212A and ISL91212B deliver a highly robust power solution by featuring a controller based on the proprietary Renesas R5 Technology, which provides tight output accuracy and load regulation, ultra-fast transient response, seamless DCM/CCM transitions, and requires no external compensation.

In addition to standard interrupt and chip enable functions, the ISL91212A and ISL91212B feature three MPIOs and two GPIOs capable of supporting the I²C communication protocol and various other pin mode functions.

Related Literature

For a full list of related documents, visit our website:

- ISL91212A, ISL91212B device page

Features

- Triple output 2+1+1 phases (ISL91212A) or quad output 1+1+1+1 single phase (ISL91212B)
- 2.5V to 5.5V supply voltage
- 5A per phase output current capability
- Small solution size (7x10mm² for 4-phase design)
- High efficiency (94.7% for $3.8V_{IN}/1.8V_{OUT}$)
- Low I_Q in low power mode
- Patented control scheme reduces output capacitor and supports fast load transient (such as 50A/µs per phase)
- ±0.7% system accuracy, remote voltage sensing
- Programmable PWM frequency from 2MHz to 6MHz
- I²C programmable output from 0.3V to 2V
- Independent Dynamic Voltage Scaling (DVS) for each output
- Soft-start and fault detection (UV, OV, OC, OT), short-circuit protection
- 2.551mm x 3.67mm 35 ball WLCSP with 0.5mm pin pitch

Applications

- Smartphones, AR/VR Glasses, Drones
- Optical Transceiver Modules
- Artificial Intelligence (AI) Processors
- Client/Enterprise/Data Center SSD, NAS

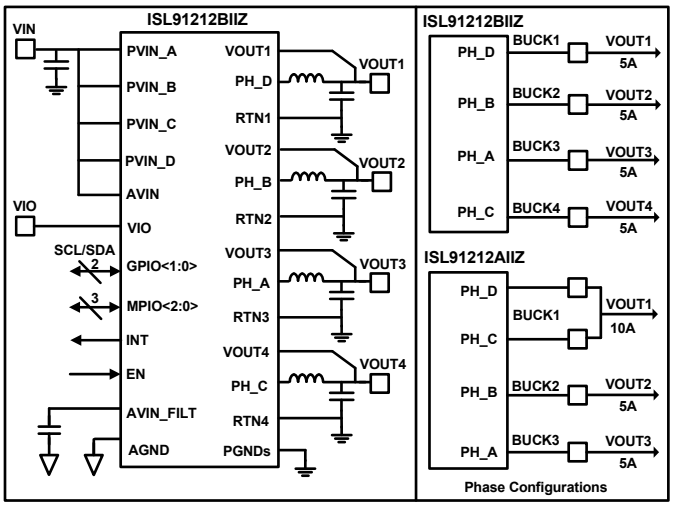


Figure 1. Simplified Block Diagram

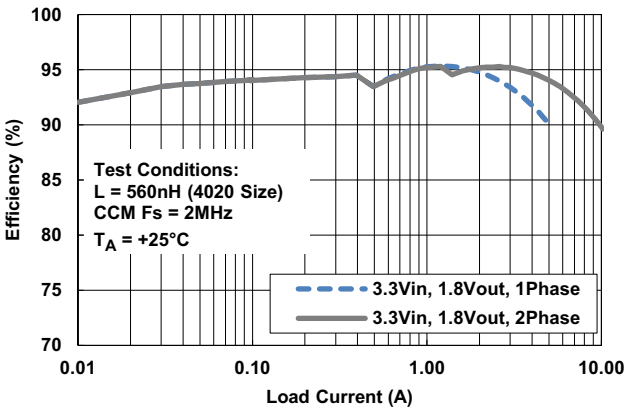


Figure 2. Efficiency vs Load Current

Contents

1. Overview . . . 3
- 1.1 Typical Applications . . . 3
- 1.2 Block Diagram . . . 4
- 1.3 Ordering Information . . . 5
- 1.4 Pin Configuration . . . 6
- 1.5 Pin Descriptions . . . 7
- 1.6 I/O Pin Configuration . . . 8

2. Specifications . . . 9
- 2.1 Absolute Maximum Ratings . . . 9
- 2.2 Thermal Information . . . 9
- 2.3 Recommended Operating Conditions . . . 9
- 2.4 Analog Specifications . . . 10

3. Output Configurations . . . 12

4. Typical Operating Performance . . . 14

5. Application Information . . . 20
- 5.1 Inductor Selection . . . 20
- 5.2 Output Capacitor Selection . . . 20
- 5.3 Input Capacitor Selection . . . 21
- 5.4 Dynamic Voltage Scaling (DVS) . . . 21
- 5.5 Configuring DVS Speed . . . 23
- 5.6 Output Voltage Setting . . . 23
- 5.7 Power Sequencing . . . 23
- 5.8 Interrupt Pin . . . 26

6. Protection Features (Faults) . . . 27
- 6.1 Over-Temperature Protection . . . 27
- 6.2 Overcurrent Protection Mode . . . 27
- 6.3 Overvoltage (OV)/Undervoltage (UV) Protection . . . 27

7. I^2C Serial Interface . . . 28
- 7.1 Write Operation . . . 28
- 7.2 Read Operation . . . 29
- 7.3 I^2C Timing . . . 30

8. Board Layout Recommendations . . . 32
- 8.1 PCB Layout Summary . . . 33
- 8.2 PCB Design for WLCSP Recommendations . . . 34

9. Register Address Map . . . 35

10. Register Description by Address . . . 36

11. Revision History . . . 50

12. Package Outline Drawing . . . 51

1. Overview

1.1 Typical Applications

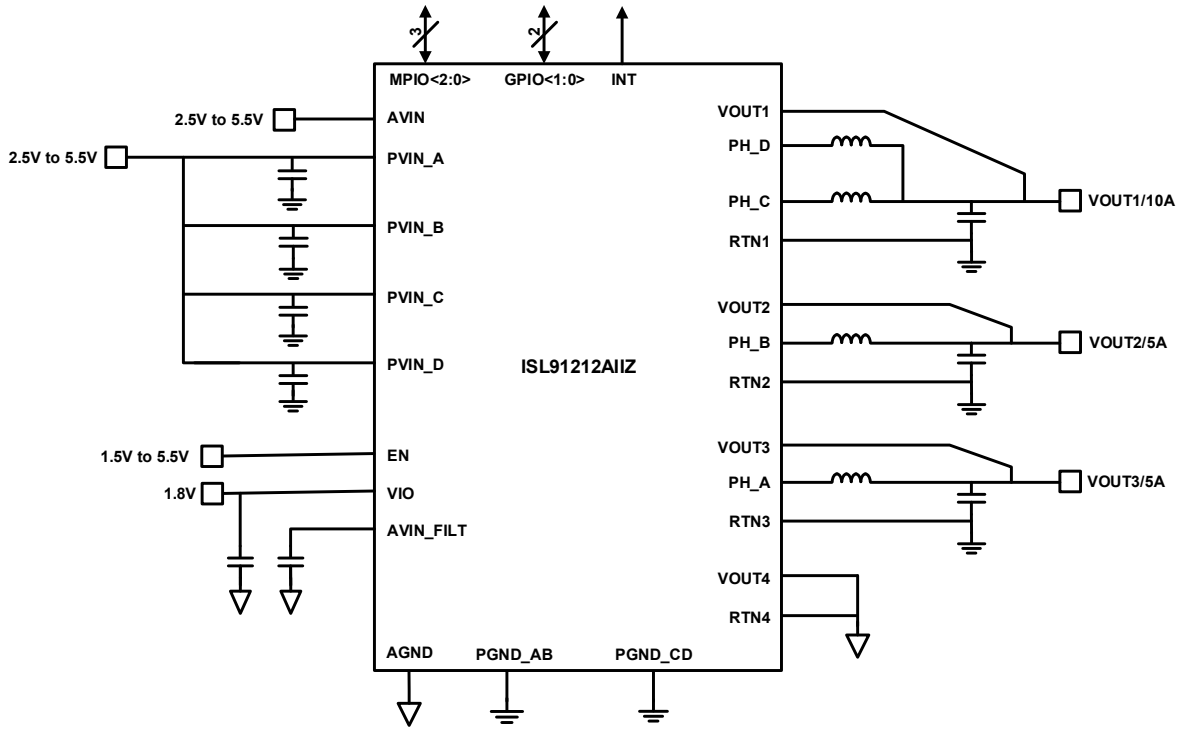


Figure 3. 2 Phase + 1 Phase + 1 Phase

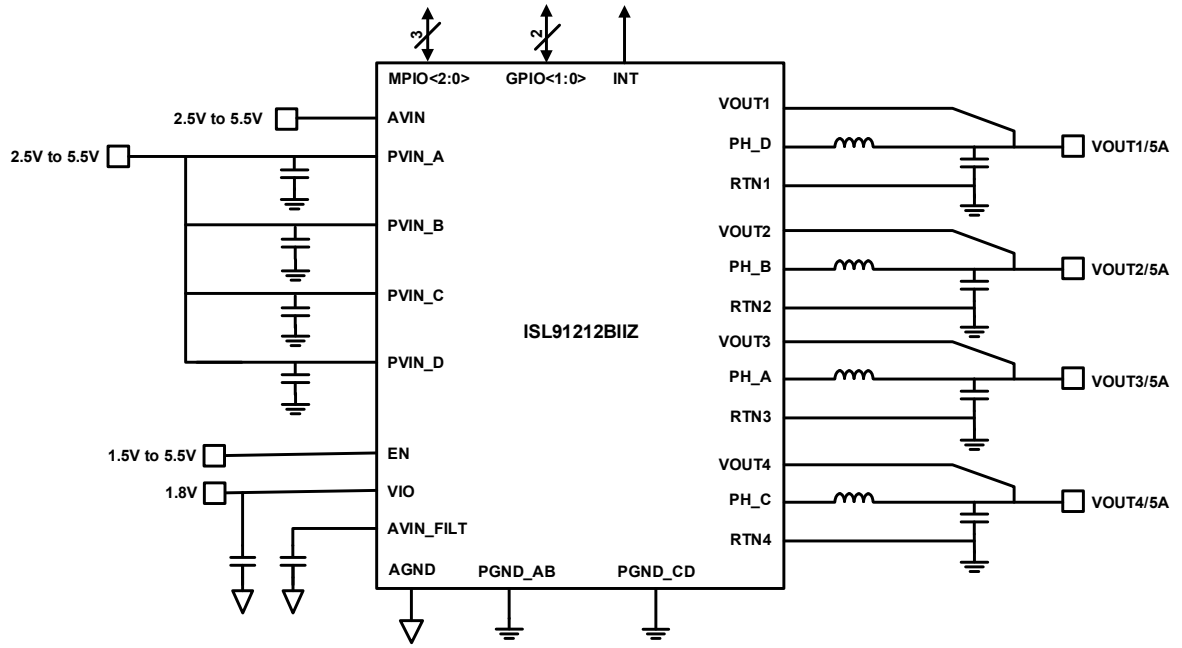


Figure 4. 1 Phase + 1 Phase + 1 Phase + 1 Phase

1.2 Block Diagram

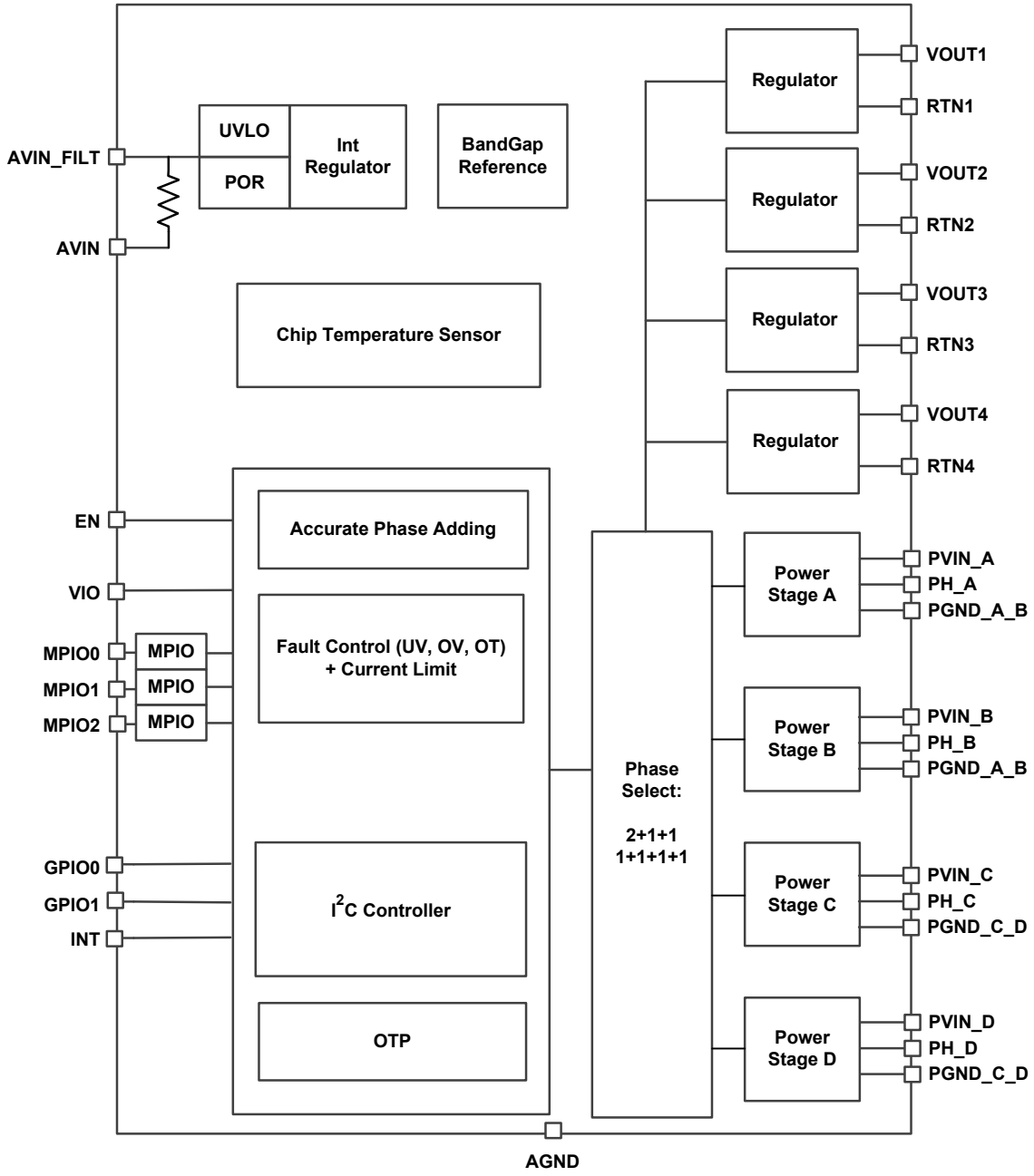


Figure 5. Block Diagram

1.3 Ordering Information

Part Number (Notes 3, 4)	Part Marking	Temp Range (°C)	Tape and Reel (Units) (Note 2)	Package (RoHS Compliant)	Pkg. Dwg
ISL91212AIIZ-T	212A	-40 to +85	3k	2.551mmx3.67mm 35 ball WLCSP with 0.5mm pin pitch	W5x7.35C
ISL91212BIIZ-T	212B	-40 to +85	3k	2.551mmx3.67mm 35 ball WLCSP with 0.5mm pin pitch	W5x7.35C
ISL91212AEVAL1Z	Evaluation Board				
ISL91212BEVAL1Z	Evaluation Board				

Notes:

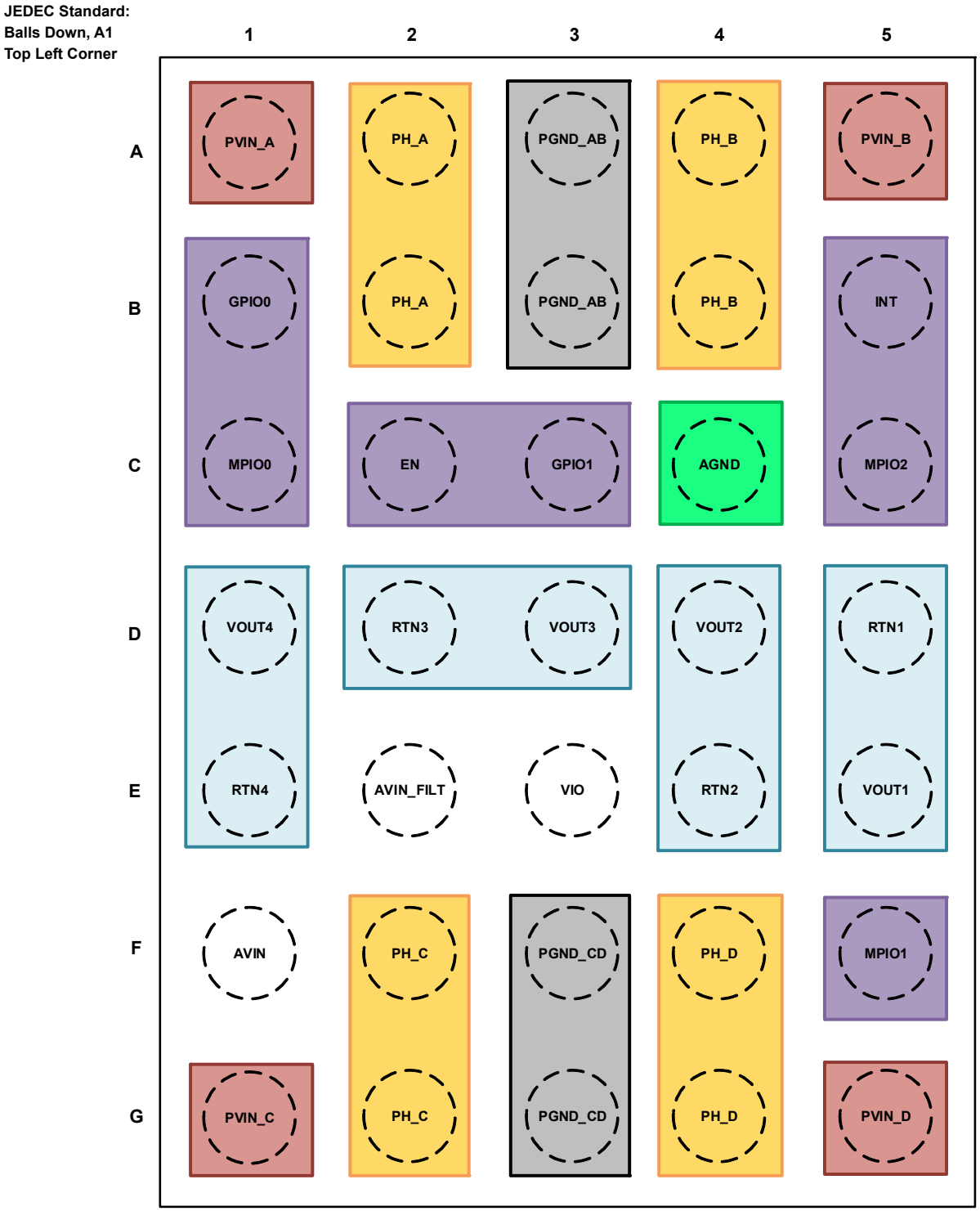
1. For additional part options contact your local sales office.
2. See TB347 for details about reel specifications.
3. These Pb-free WLCSP packaged products employ special Pb-free material sets; molding compounds/die attach materials and SnAgCuNi - e8 solder ball terminals, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free WLCSP packaged products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
4. For Moisture Sensitivity Level (MSL), see the ISL91212A, ISL91212B device page. For more information about MSL, see TB363.

Table 1. Key Differences Between Family of Parts

Part Number	Pin Configuration	Pitch	Output Configuration	Maximum Load
ISL91212A	35 Ball 5x7 WLCSP	0.5mm	Triple Output (2+1+1 Phase)	5A
ISL91212B	35 Ball 5x7 WLCSP	0.5mm	Quad Output (1+1+1+1 Phase)	5A
ISL91302B	54 Ball 6x9 WLCSP	0.4mm	Single Output (4 + 0 Phase)	5A
	54 Ball 6x9 WLCSP	0.4mm	Dual Output (3 + 1 Phase)	5A
	54 Ball 6x9 WLCSP	0.4mm	Dual Output (2 + 2 Phase)	5A
ISL91301A	42 Ball 6x7 WLCSP	0.4mm	Triple Output (2+1+1 Phase)	4A
ISL91301B	42 Ball 6x7 WLCSP	0.4mm	Quad Output (1+1+1+1 Phase)	4A
ISL91211A	54 Ball 6x9 WLCSP	0.4mm	Triple Output (2+1+1 Phase)	5A
ISL91211B	54 Ball 6x9 WLCSP	0.4mm	Quad Output (1+1+1+1 Phase)	5A

1.4 Pin Configuration

35 Ball 5x7 WLCSP
Top View



1.5 Pin Descriptions

Pin Location	Pin Name	Type	Description
A1	PVIN_A	Input	Power supply for Power Stage A
A2, B2	PH_A	Output	Switching node for Power Stage A
A3, B3	PGND_AB	Input	Ground connection for Power Stage A and Power Stage B
A4, B4	PH_B	Output	Switching node for Power Stage B
A5	PVIN_B	Input	Power supply for Power Stage B
B1	GPIO0	Input	GPIO0/I^2C Clock
C2	EN	Input	Master chip enable input, NMOS logic threshold
C3	GPIO1	Input/Output	GPIO1/I^2C Data
B5	INT	Output	Interrupt output for IRQ interrupt request signal
C4	AGND	Input	Analog chip ground
D5	RTN1	Input	Remote ground sense for Buck1
D1	VOUT4	Input	Buck4 remote output voltage sense for ISL91212B Note: Short to ground for ISL91212A
D2	RTN3	Input	Remote ground sense for Buck3
D3	VOUT3	Input	Remote output voltage sense for Buck3
D4	VOUT2	Input	Remote output voltage sense for Buck2
E4	RTN2	Input	Remote ground sense for Buck2
E5	VOUT1	Input	Remote output voltage sense for Buck1
E1	RTN4	Input	Buck4 remote ground sense for ISL91212B Note: Short to ground for ISL91212A
E2	AVIN_FILT	Output	Filtered analog supply voltage, 2.5V to 5.5V Place a decoupling capacitor close to the IC
E3	VIO	Input	I/O supply voltage for digital communications. Nominally connected to a 1.8V supply
C1	MPIO0	Input/Output	Multipurpose I/O, see IO_PINMODE table in "I/O Pin Configuration" on page 8. Can be NC if not used
F5	MPIO1	Input/Output	Multipurpose I/O, see IO_PINMODE table in "I/O Pin Configuration" on page 8. Can be NC if not used
C5	MPIO2	Input/Output	Multipurpose I/O, see IO_PINMODE table in "I/O Pin Configuration" on page 8. Can be NC if not used
F1	AVIN	Input	Analog supply voltage, 2.5 to 5.5V
F2, G2	PH_C	Output	Switching node for Power Stage C
F3, G3	PGND_CD	Input	Ground connection for Power Stage C and Power Stage D
F4, G4	PH_D	Output	Switching node for Power Stage D
G1	PVIN_C	Input	Power supply connection for Power Stage C
G5	PVIN_D	Input	Power supply connection for Power Stage D

1.6 I/O Pin Configuration

The ISL91212 features two general purpose I/O pins for I^{2}C and three multipurpose I/O pins. These pins can perform different functions depending on the “IO_PINMODE” setting. The default factory setting for IO_PINMODE is 0x2. For features that require “IO_PINMODE” to be different than the default value, contact Renesas for factory OTP programming.

Table 2. IO_PINMODE

IO_PINMODE	MPIO0	MPIO1	MPIO2	GPIO0	GPIO1	Description
0x2	PGOOD1	PGOOD2	PGOOD3	I2C_CLK	I2C_SDA	I^{2}C with Individual PGOODs for Bucks1-3
0x4	DVS_PIN1	DVS_PIN0	PGOOD1	I2C_CLK	I2C_SDA	I^{2}C with Global DVS mode and PGOOD1
0x6	BUCK1_DVS0	BUCK1_DVS1	BUCK2_DVS0	I2C_CLK	I2C_SDA	I^{2}C with full DVS for Buck1, 1-pin DVS for Buck2
0x7	BUCK1_DVS0	BUCK2_DVS0	BUCK3_DVS0	I2C_CLK	I2C_SDA	I^{2}C with 1-pin DVS for each buck up to Buck3
0xC	MPIO_DATA [0]	MPIO_DATA [1]	MPIO_DATA [2]	I2C_CLK	I2C_SDA	I^{2}C with internal register pass-through

Name	Definition
I2C_CLK	I^{2}C clock
I2C_SDA	I^{2}C data
PGOOD1, PGOOD2, PGOOD3	Three power-good output pins (one per buck)
DVS_PIN1, DVS_PIN0	DVS look-up table to allow two pins to control up to four bucks
BUCK1_DVS0	DVS input pins for Buck1
BUCK2_DVS0	DVS input pins for Buck2
BUCK3_DVS0	DVS input pins for Buck3
MPIO_DATA[2:0]	Three output pins to create additional system level GPIOs Note: Contact Renesas for more information

2. Specifications

2.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
PVIN and AVIN Pins to PGND	-0.3	+6	V
VOUT Pin (BUCKx_VOUTFBDIV[1:0] = 0x00)	-0.3	+2.0	V
VOUT Pin (BUCKx_VOUTFBDIV[1:0] = 0x01)	-0.3	+2.4	V
VOUT Pin (BUCKx_VOUTFBDIV[1:0] = 0x02)	-0.3	+3.0	V
PH Pins to PGND	-0.3	+0.3 + PVIN	V
VIO, EN Pins to GND	-0.3	+0.3 + AVIN	V
RTN, GND to PGND	-0.3	+0.3	V
INT, MPIO, GPIO Pins to GND	-0.3	+0.3 + VIO	V
ESD Rating (Note 5)	**Value**		**Unit**
Human Body Model (Tested per JS-001-2017)	2.5		kV
Charged Device Model (Tested per JS-002-2014)	1		kV
Latch-Up (Tested per JESD78E; Class 2, Level A)	100		mA

Note:

5. ESD ratings apply to external pins only.

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

2.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
35 Ball WLCSP Package (Notes 6, 7)	43	0.6

Notes:

6. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with “direct attach” features. See TB379.
7. For θ_{JC}, the “case temp” location is taken at the package top center.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature		+150	°C
Maximum Storage Temperature Range	-65	+150	°C
Pb-Free Reflow Profile	See TB493		

2.3 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Junction Temperature	-40	+125	°C
VIO Voltage (VIO to AGND)	1.7	AVIN	V
INT, MPIO, GPIO Pins to GND	0	VIO	V
Supply Voltage			
AVIN to AGND	2.5	5.5	V
PVIN to PGNDx	2.5	5.5	V

2.4 Analog Specifications

AVIN/PVIN = 3.7V, V_{OUT} = 1V, L = 220nH, Frequency = 4MHz, V_{IO} = 1.8V, T_A = +25°C. **Boldface limits apply across the operating junction temperature range, -40°C to +85°C unless otherwise noted**.

Parameter	Symbol	Test Conditions	Min (Note 8)	Typ	Max (Note 8)	Unit
Input Supply						
Supply Voltage	AVIN		**2.5**		**5.5**	V
Supply Voltage	PVIN		**2.5**		**5.5**	V
AVIN Supply Current	I_Q	EN = 0V		0.1	**1**	µA
AVIN + PVINx Supply Current		EN = 0V		<1	**6**	µA
AVIN + PVINx Supply Current EN = AVIN = PVINx = 3.7V		All BUCKs EN[0] = 0x0		17		µA
		BUCK1_EN[0] = 0x1, all other BUCKs EN[0] = 0x0, not switching DCM operation		82		µA
		BUCK2, 3 or 4_EN[0] = 0x1, all other BUCKs EN[0] = 0x0, not switching DCM operation		62		µA
		BUCK1_EN[0] = 0x1, all other BUCKs EN[0] = 0x0, not switching, forced CCM operation		1.2		mA
		BUCK2, 3 or 4_EN[0] = 0x1, all other BUCKs EN[0] = 0x0, not switching, forced CCM operation		1		mA
AVIN UVLO Rising Threshold	VUVLOR		**2.50**	2.58	**2.65**	V
AVIN UVLO Falling Threshold	VUVLOF		**2.29**	2.34	**2.39**	V
Buck Regulation						
Buck Output Voltage Range (Each Output)	V_{OUT}	BUCKx_VOUTFBDIV[1:0] = 0x00	**0.300**		**1.2**	V
		BUCKx_VOUTFBDIV[1:0] = 0x01	**0.375**		**1.5**	V
		BUCKx_VOUTFBDIV[1:0] = 0x02	**0.500**		**2.0**	V
Output Voltage Step Size	V_{STEP}	10-bit control, BUCKx_VOUTFBDIV[1:0] = 0x00		1.2		mV
		10-bit control, BUCKx_VOUTFBDIV[1:0] = 0x01		1.5		mV
		10-bit control, BUCKx_VOUTFBDIV[1:0] = 0x02		2.0		mV
Output Voltage Accuracy (Note 9)	V_{ACC}	CCM, V_{OUT} > 0.6V	-0.3		0.3	%
		CCM, V_{OUT} > 0.6V T_A = -10°C to +85°C	-0.7		0.7	%
		CCM, V_{OUT} < 0.6V	-4		4	mV
		CCM, V_{OUT} < 0.6V T_A = -10°C to +85°C	-5.5		5.5	mV
Current Matching	I_{MATCH}	I_{OUT} = 5A per phase in ISL91212A		10		%
Dynamic Response						
Boot-Up Time	V_{BT}	Delay time from when PVIN, AVIN, and EN are asserted to Buck1 PWM switching. This time includes internal reference startup, OTP load, and Buck controller calibration time.		1.4		ms
Dynamic Voltage Scaling (Output Slew Rate)	V_{DVS}	2.5V < V_{IN} < 5.5V 3mV/µs	**-15**		**15**	%

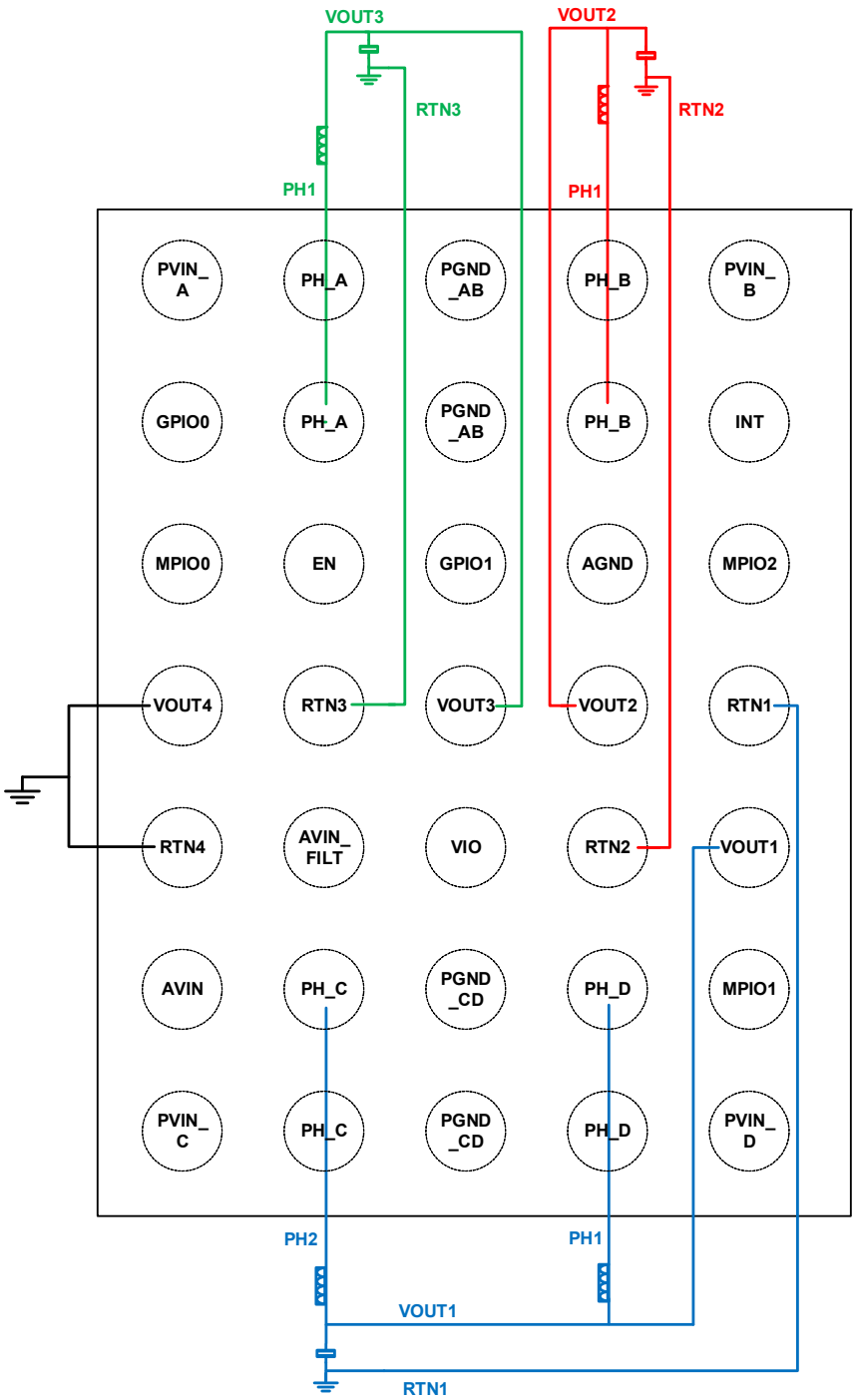
AVIN/PVIN = 3.7V, V_{OUT} = 1V, L = 220nH, Frequency = 4MHz, V_{IO} = 1.8V, T_A = +25°C. **Boldface limits apply across the operating junction temperature range, -40°C to +85°C unless otherwise noted. (Continued)**

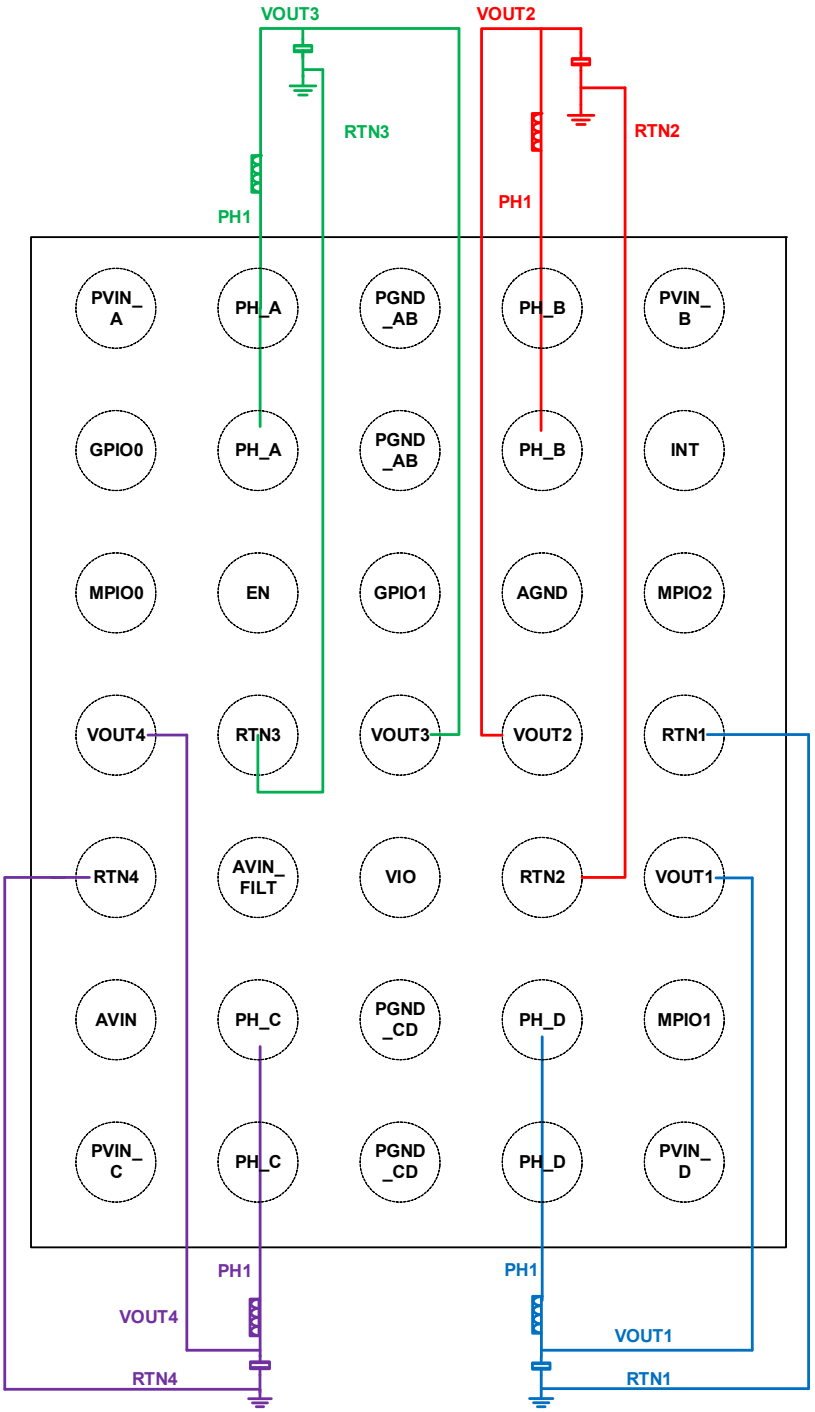
Parameter	Symbol	Test Conditions	Min (Note 8)	Typ	Max (Note 8)	Unit
Frequency						
Switching Frequency (CCM)	f_{SW}			4		MHz
CCM Frequency Tolerance	f_{SW_TOL}		**-15**		**15**	%
Power Stage						
Buck Output Current (Each Phase)		2.5V < V_{IN} < 5.5V			**5**	A
High-Side Switch ON-Resistance	HS $r_{DS(ON)}$	Conditions: PVIN = 3.7V, current = 300mA		23		mΩ
Low-Side Switch ON-Resistance	LS $r_{DS(ON)}$	Conditions: PVIN = 3.7V, current = 300mA		9		mΩ
MPIO/GPIO						
MPIO/GPIO Operating Conditions						
Allowable Range of Supply for Operation	VIO		1.7	1.8	AVIN	V
Chip Enable Logic Threshold Level						
Low-Level Input Voltage Range	V_{IL}				**0.5**	V
High-Level Input Voltage	V_{IH}		**1.35**			V
MPIO/GPIO Logic Threshold Levels						
Low-Level Input Voltage Range	V_{IL}				**0.25 * V_{IO}**	V
High-Level Input Voltage	V_{IH}		**0.75 * V_{IO}**			V
Hysteresis On Input	V_{HYS}		**0.1 * V_{IO}**			V
Low-Level Output	V_{OL}	1mA			**0.4**	V
High-Level Output	V_{OH}	1mA (250µA for 20% drive configuration)	**V_{IO} - 0.4**			V
Serial Interfaces						
I^2C Frequency Capability	f_{I2C}				**3.4**	MHz
Protection						
HSD Current Limit	I_{LIMIT}	2.5V < V_{IN} < 5.5V ISL91212A Phase D, OC = 12A	**-10**		**10**	%
		2.5V < V_{IN} < 5.5V ISL91212A Phase A, B, OC = 8A	**-10**		**10**	%
		2.5V < V_{IN} < 5.5V ISL91212B Phase A, B, C, D, OC = 8A	**-10**		**10**	%
Output UVP Threshold Accuracy	V_{UVP}	Thresholds: -250mV	**-35**		**35**	mV
Output OVP Threshold Accuracy	V_{OVP}	Thresholds: +250mV	**-35**		**35**	mV
Thermal Shutdown Threshold	T_{SPS}	2.5V < V_{IN} < 5.5V	**143**		**162**	°C
		Hysteresis		55		°C

Notes:

8. Parameters with MIN and/or MAX limits established by test, characterization, and/or design.
9. V_{OUT} feedback divider ratio equals 1 (BUCKx_VOUTFBDIV[1:0] = 0x00).
10. Per "Thermal Information" on page 9, operating beyond thermal limits can cause permanent damage.

3. Output Configurations

Output Configuration	Power Stage Assignment	Diagram
2-phase + 1-phase + 1-phase Connect: VOUT4/RTN4 to PGND Plane	2-phase: Controller #1 (VOUT1) • PH_D (PHASE #1) • PH_C 1-phase: Controller #2 (VOUT2) • PH_B 1-phase: Controller #3 (VOUT3) • PH_A	ISL91212A Configuration 

Output Configuration	Power Stage Assignment	Diagram
1-phase + 1-phase + 1-phase + 1-phase	1-phase: Controller #1 (VOUT1) • PH_D 1-phase: Controller #2 (VOUT2) • PH_B 1-phase: Controller #3 (VOUT3) • PH_A 1-phase: Controller #4 (VOUT4) • PH_C	ISL91212B Configuration 

4. Typical Operating Performance

Unless otherwise noted, operating conditions are: V_{IN} = 3.8V, V_{OUT} = 1V, V_{IO} and Enable = 1.8V, T_A = +25°C, f_{SW} = 4MHz, 2+1+1 configuration, L = 220nH per phase, SW1: C_{OUT} = 2x22µF + 2x4.3µF + 4x1µF, SW2-3: C_{OUT} = 1x22µF + 4x4.3µF.

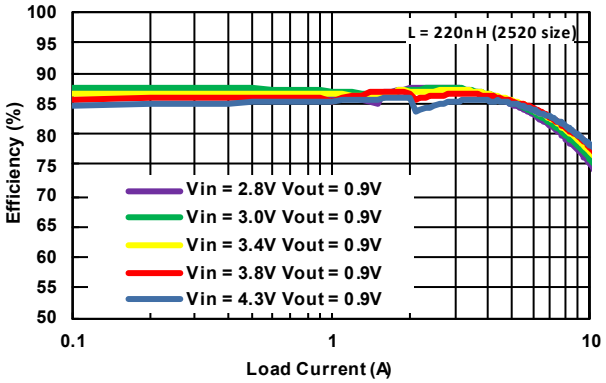


Figure 6. Dual-Phase Efficiency (V_{OUT} = 0.9V), Continuous Load Sweep (0.1A to 10A)

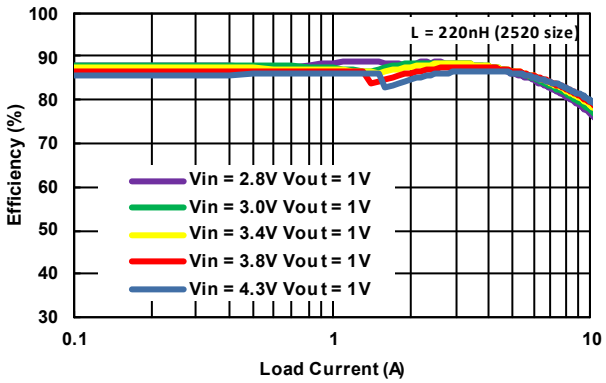


Figure 7. Dual-Phase Efficiency (V_{OUT} = 1V), Continuous Load Sweep (0.1A to 10A)

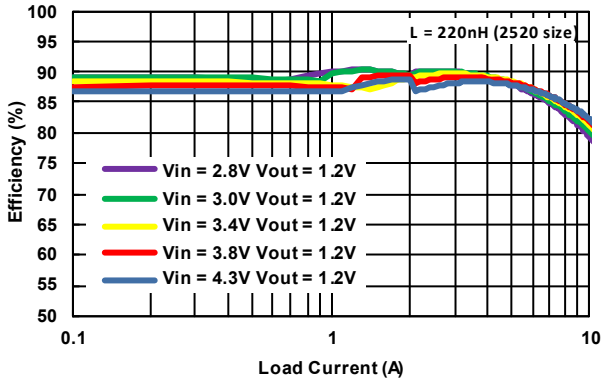


Figure 8. Dual-Phase Efficiency (V_{OUT} = 1.2V), Continuous Load Sweep (0.1A to 10A)

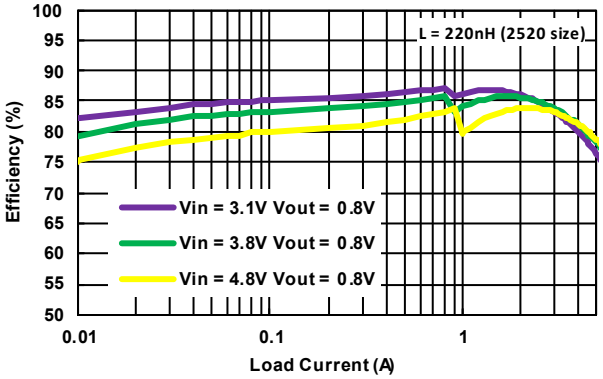


Figure 9. Single-Phase Efficiency (V_{OUT} = 0.8V), Continuous Load Sweep (0.01A to 5A)

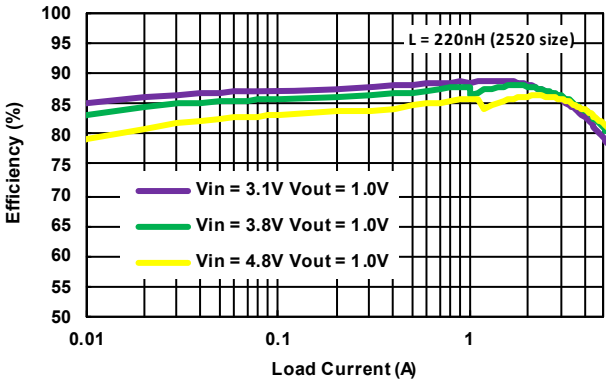


Figure 10. Single-Phase Efficiency (V_{OUT} = 1V), Continuous Load Sweep (0.01A to 5A)

Unless otherwise noted, operating conditions are: V_{IN} = 3.8V, V_{OUT} = 1V, V_{IO} and Enable = 1.8V, T_A = +25°C, f_{SW} = 4MHz, 2+1+1 configuration, L = 220nH per phase, SW1: C_{OUT} = 2x22µF + 2x4.3µF + 4x1µF, SW2-3: C_{OUT} = 1x22µF + 4x4.3µF. **(Continued)**

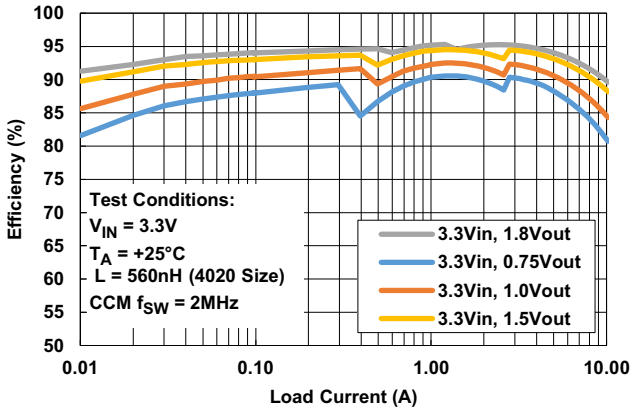


Figure 11. 2-Phase Efficiency V_{IN} = 3.3V

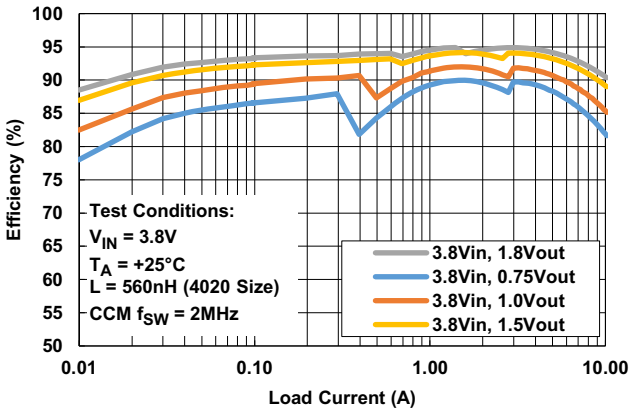


Figure 12. 2-Phase Efficiency V_{IN} = 3.8V

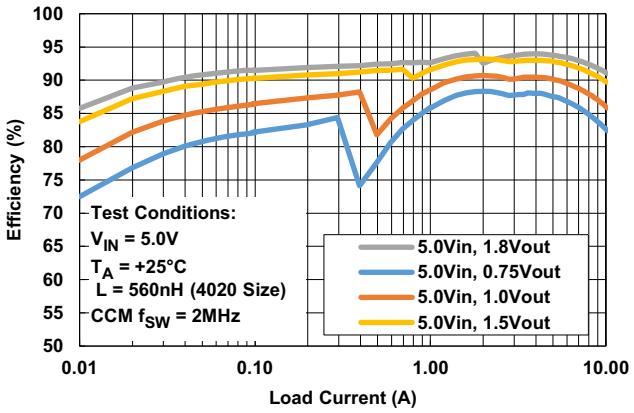


Figure 13. 2-Phase Efficiency V_{IN} = 5.0V

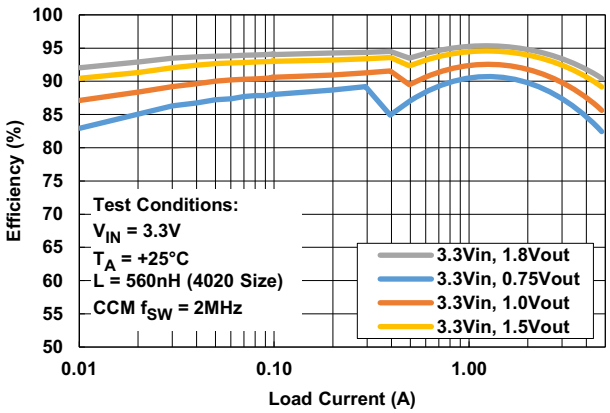


Figure 14. Single-Phase Efficiency V_{IN} = 3.3V

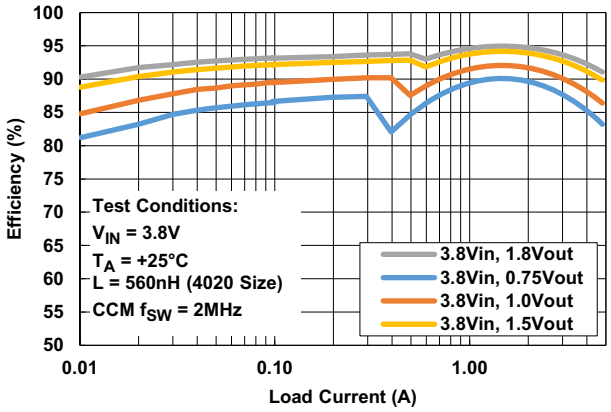


Figure 15. Single-Phase Efficiency V_{IN} = 3.8V

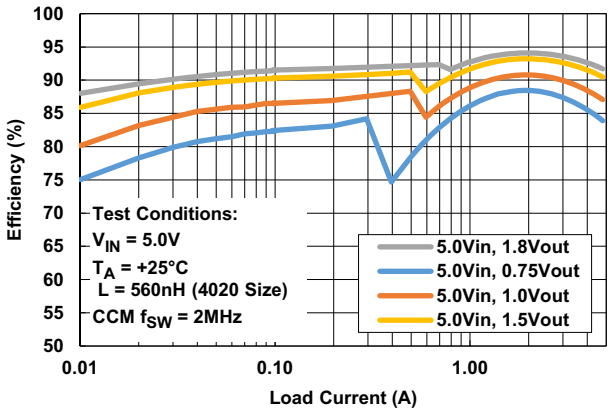
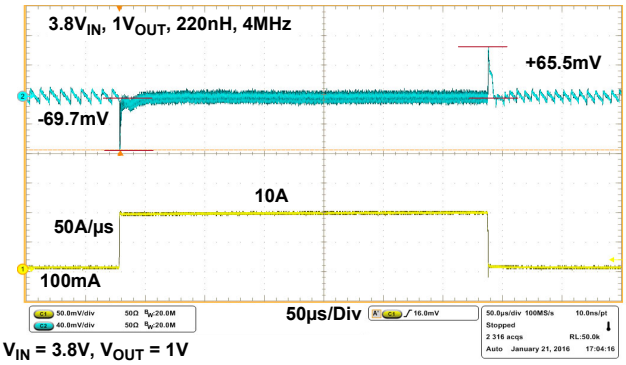


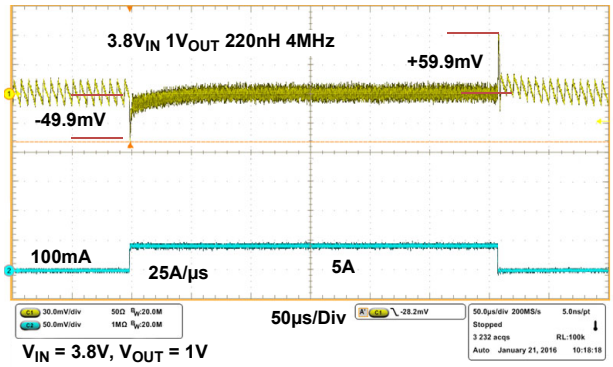
Figure 16. Single-Phase Efficiency V_{IN} = 5.0V

Unless otherwise noted, operating conditions are: V_{IN} = 3.8V, V_{OUT} = 1V, V_{IO} and Enable = 1.8V, T_A = +25°C, f_{SW} = 4MHz, 2+1+1 configuration, L = 220nH per phase, SW1: C_{OUT} = 2x22µF + 2x4.3µF + 4x1µF, SW2-3: C_{OUT} = 1x22µF + 4x4.3µF. **(Continued)**



V_{IN} = 3.8V, V_{OUT} = 1V
Load Step Slew Rate: 50A/µs, 0.1A to 10A
220nH Inductor (Cyntec)
3x22µF Capacitor (0603 6.3V Murata)
6x4.7µF Capacitor (0603 10V)

Figure 17. Dual-Phase Load Transient (10A/200ns)



V_{IN} = 3.8V, V_{OUT} = 1V
Load Step Slew Rate: 25A/µs, 0.1A to 5A
220nH Inductor (Cyntec)
1x22µF Capacitor (0603 6.3V Murata)
6x4.3µF Capacitor (Low ESL)

Figure 18. Single-Phase Transient (5A/200ns)

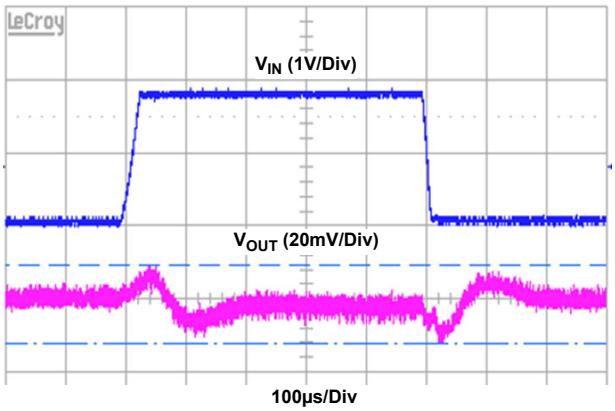


Figure 19. Dual-Phase Line Transient, V_{OUT} = 1V, V_{IN} = 3.1V to 4.8V, Load = 8A, TR and TF = 15µs

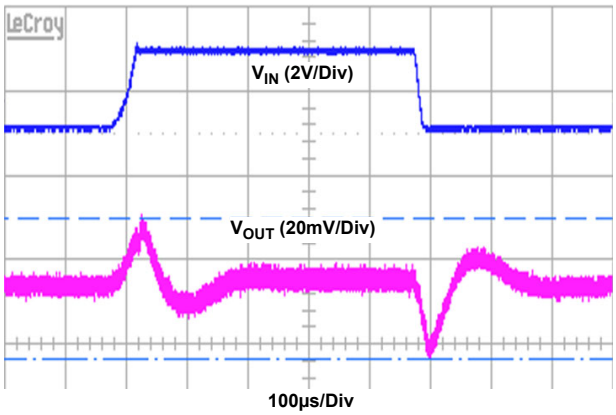


Figure 20. Single-Phase Line Transient, V_{OUT} = 1V, V_{IN} = 3.1 to 4.8V, Load = 5A, TR and TF = 15µs

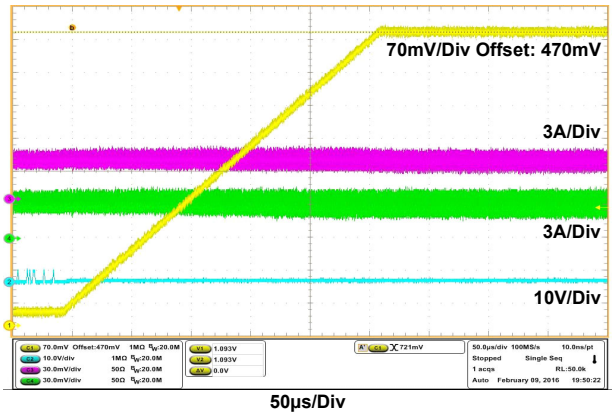


Figure 21. 0.5V to 1.1V DVS (A), Load = 5A, Slew Rate = 3mV/µs, CH1 - V_{OUT}, CH4 - I_{LX1}, CH3 - I_{LX2}, CH2 - DVS Command

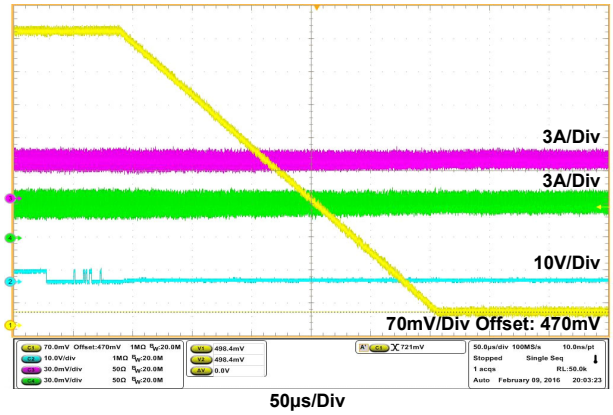


Figure 22. 0.5V to 1.1V DVS (B), Load = 5A, Slew Rate = 3mV/µs, CH1 - V_{OUT}, CH4 - I_{LX1}, CH3 - I_{LX2}, CH2 - DVS Command

Unless otherwise noted, operating conditions are: V_{IN} = 3.8V, V_{OUT} = 1V, V_{IO} and Enable = 1.8V, T_A = +25°C, f_{SW} = 4MHz, 2+1+1 configuration, L = 220nH per phase, SW1: C_{OUT} = 2x22µF + 2x4.3µF + 4x1µF, SW2-3: C_{OUT} = 1x22µF + 4x4.3µF. **(Continued)**

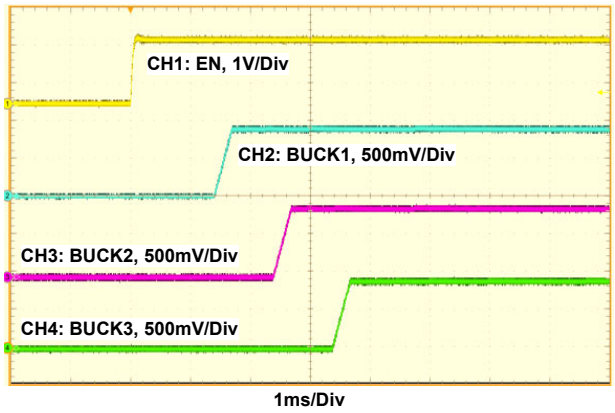


Figure 23. ISL91212A Startup by EN, V_{OUT1}, 2, 3 = 0.9V

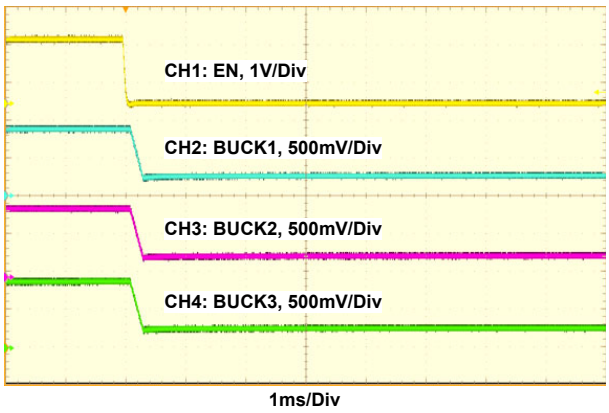


Figure 24. ISL91212A Shutdown by EN, V_{OUT1}, 2, 3 = 0.9V

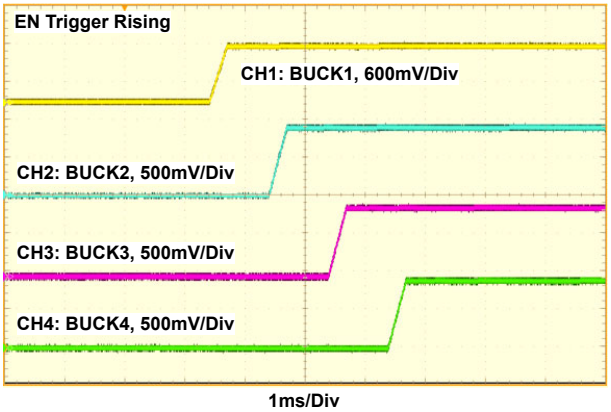


Figure 25. ISL91212B Startup by EN, V_{OUT1}, 2, 3, 4 = 0.9V

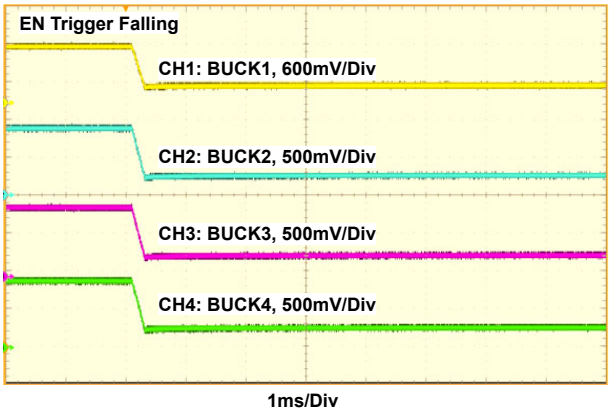


Figure 26. ISL91212B Shutdown by EN, V_{OUT1}, 2, 3, 4 = 0.9V

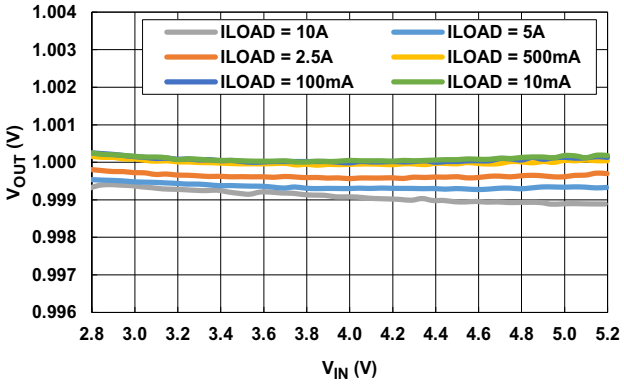


Figure 27. Dual-Phase, V_{OUT} vs V_{IN} (10mA to 10A)

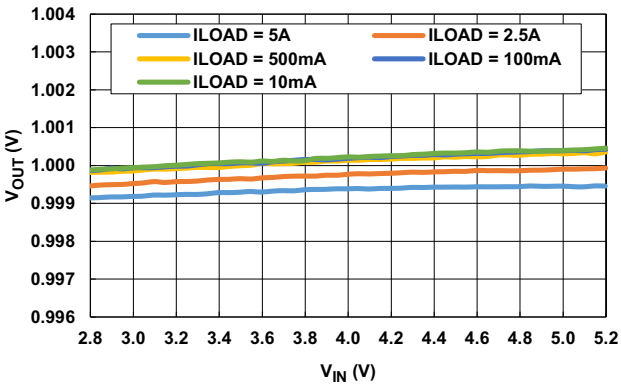


Figure 28. Single-Phase, V_{OUT} vs V_{IN} (10mA to 5A)

Unless otherwise noted, operating conditions are: V_{IN} = 3.8V, V_{OUT} = 1V, V_{IO} and Enable = 1.8V, T_A = +25°C, f_{SW} = 4MHz, 2+1+1 configuration, L = 220nH per phase, SW1: C_{OUT} = 2x22µF + 2x4.3µF + 4x1µF, SW2-3: C_{OUT} = 1x22µF + 4x4.3µF. **(Continued)**

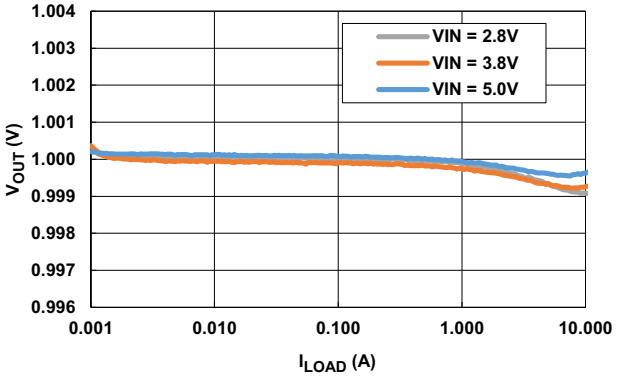


Figure 29. Dual Phase, V_{OUT} vs Load (1mA to 10A)

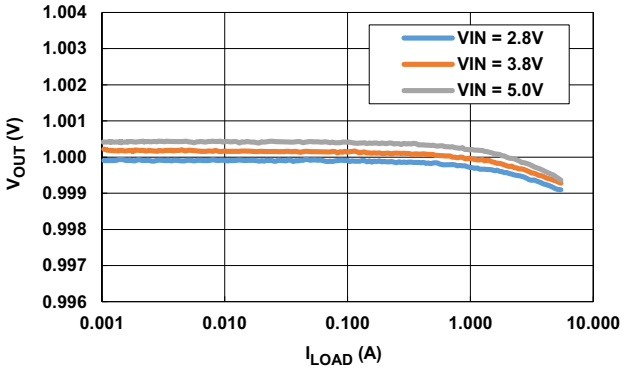


Figure 30. Single Phase, V_{OUT} vs Load (1mA to 5A)

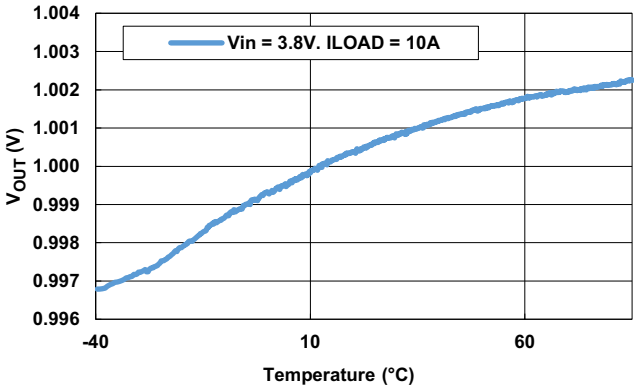


Figure 31. Dual-Phase Forced CCM, V_{OUT} vs Temperature (-40°C to +85°C)

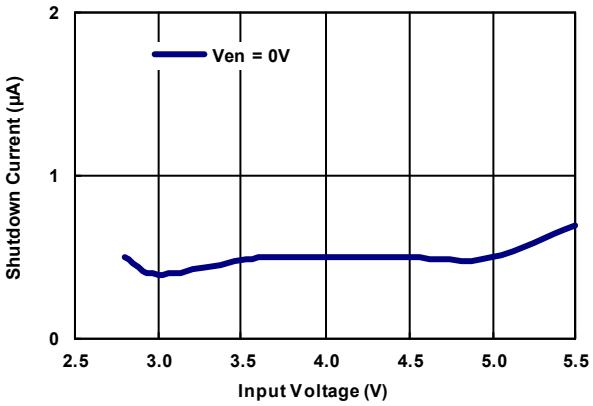


Figure 32. Shutdown Current vs V_{IN}

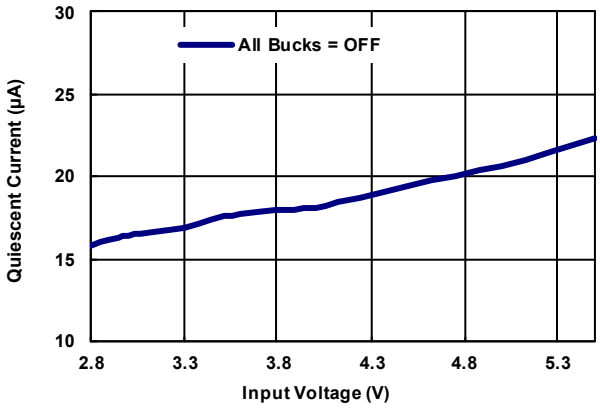


Figure 33. Quiescent Current (All Bucks Off) vs V_{IN}

Unless otherwise noted, operating conditions are: V_{IN} = 3.8V, V_{OUT} = 1V, V_{IO} and Enable = 1.8V, T_A = +25°C, f_{SW} = 4MHz, 2+1+1 configuration, L = 220nH per phase, SW1: C_{OUT} = 2x22µF + 2x4.3µF + 4x1µF, SW2-3: C_{OUT} = 1x22µF + 4x4.3µF. **(Continued)**

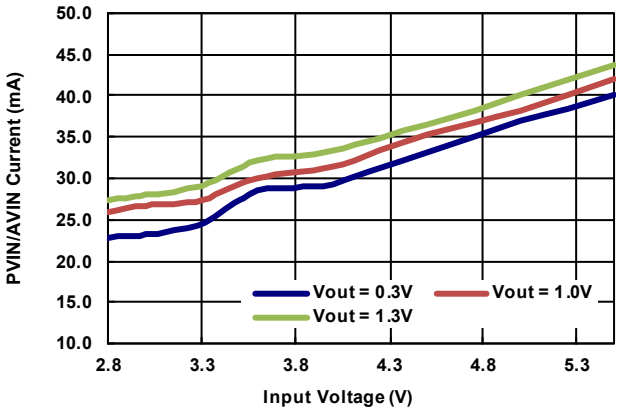


Figure 34. Single-Phase PVIN/AVIN Current (PWM Switching) vs V_{IN}

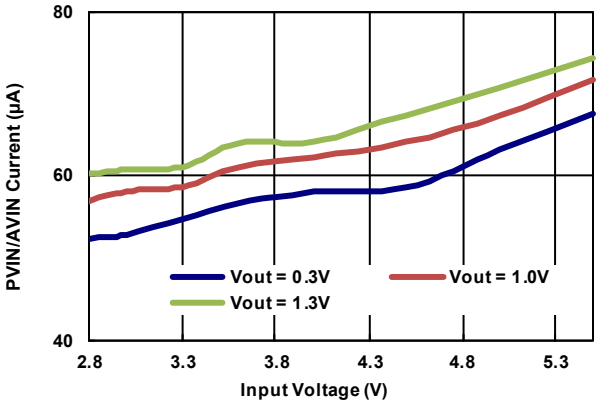


Figure 35. Single-Phase PVIN/AVIN Current (PFM Switching) vs V_{IN}

5. Application Information

5.1 Inductor Selection

The ISL91212A and ISL91212B are high performance PMICs with integrated synchronous buck converters that can deliver up to 5A of continuous current per phase at 0.3V to 2.0V regulated voltage. The ISL91212B is designed to operate with up to four single phases (1+1+1+1 configuration), and the ISL91212A is designed to work with two single phases and one dual phase (2+1+1 configuration) at an optimized switching frequency of 2MHz ~ 4MHz. Contact Renesas Support for questions relating to a switching frequency of 6MHz. In the dual phase configuration, each channel requires an inductor of equal value and should be capable of delivering the maximum load divided by two.

Table 3. Recommended Output Inductors

Mfr	Part Number	L x W x H (mm)	Value (nH)	DCR mΩ (Typ)	$\overline{ISAT}$ (Typ)
Cyntec	HMLR25201T	2.5x2.0x1.0	220	12	7.0
Cyntec	HTTN2016T	2.0x1.6x1.0	220	13	7.2
Murata	DFE2016E	2.0x1.6x1.0	240	16	7.0
Murata	DFE252012F	2.5x2.0x1.2	470	23	6.7
Coilcraft	XEL4020-561ME	4.0x4.0x2.0	560	8	11.3

5.2 Output Capacitor Selection

Output capacitors are needed to filter square voltage at the phase node into a regulated output voltage. The amount of output capacitance required is based on parameters of maximum load step, the slew rate of the load step, and the maximum allowable voltage regulation tolerance during the transient. The amount of ripple voltage at the output capacitor is also a design constraint. The total peak-to-peak ripple voltages produced from the output capacitor is equal to its ESR multiplied by the worst case inductor ripple current.

Use ceramic capacitors due to their low ESR and ESL properties. Select X7R or X5R type capacitors and consider DC bias effects. A wide range of output capacitor values can be used. Each phase is recommended to have at least one 22µF filter capacitor.

Table 4. Recommended Output Capacitors

Mfr	Part Number	Case Size	Value (µF)	Voltage (V)
TDK	C1608X5R1A226M080AC	0603	22	10
TDK	C0510X6S0G105M030AC	0204	1	4
Murata	LLD154R60G435ME01	0402	4.3	4
Murata	LLL1U4R60G435ME22	0204	4.3	4

5.3 Input Capacitor Selection

Ceramic input capacitors source the AC component of the input current flowing into the high-side MOSFETs. Place them as close to the IC as possible. A 10µF local decoupling capacitor is recommended for each phase PVIN.

If long wires are used to bring power to the IC, use additional "bulk" capacitors between C_{IN} and the battery/power supply to dampen ringing and overshoot at start-up.

Internal analog reference circuits also require additional filtering at the AVIN_FILT pin.

Table 5. Recommended Input Capacitors

Mfr	Part Number	Case Size	Value (µF)	Volt (V)	Input
TDK Corp	CGB2A1X5R1A105M033BC	0402	1	10	AVIN_FILT
KEMET	C0402C104K8RACTU	0402	0.1	10	AVIN_FILT
Samsung	CL05A10MP5NUNC	0402	10	10	PVIN
Murata	GRM188R61A106MAAL	0603	10	10	PVIN

5.4 Dynamic Voltage Scaling (DVS)

The ISL91212A and ISL91212B have several options to achieve dynamic voltage scaling. Each buck controller has four independently programmable voltage settings that can set the output voltage. The settings are DVS0, DVS1, DVS2, and DVS3. By changing the DVS number selected, the corresponding output voltage is selected. The two methods to select the DVS are:

Method 1) - Use internal registers to set DVS by writing to BUCKx_DVSSELECT[1:0] in the BUCKx_DVSSEL register for each buck using I^2C.

To use this method, set BUCKx_DVSCTRL[0] to "0x0" for the corresponding BUCK.

BUCK1_DVSCTRL[0]	
0x0	Use BUCKx_DVSSELECT[1:0] to select active DVS configuration
0x1	Use DVS pin(s) to control DVS selection

The BUCKx_DVSSELECT[1:0] settings allow you to switch between four different DVS settings, each of which corresponds to a set of DVS registers holding the DVS information.

For example, DVS0 corresponds to BUCKx_DVS0VOUT92[7:0] and BUCKx_DVS0VOUT10[1:0]. The two register values combined represent the 10-bit DAC code for DVS0.

BUCKx_DVSSELECT[1:0]	Active DVS for BUCKx
0x0	DVS0
0x1	DVS1
0x2	DVS2
0x3	DVS3

Method 2) - Use the MPIO pins to configure DVS. There are two variations depending on the setting for IO_PINMODE. See the I/O Pin Configuration table in "I/O Pin Configuration" on page 8.

Note: To use DVS with the MPIO pins, IO_PINMODE must be OTP programmed before a start-up boot sequence is initiated. On-the-fly programming is not recommended for the following configurations.

(i) IO_PINMODE = 0x4: I^2C with Global DVS pins.

MPIO0	MPIO1	GPIO0	GPIO1
DVS_PIN1	DVS_PIN0	I2C_CLK	I2C_SDA

BUCKx_DVSPIN_CTRL[1:0] in BUCKx_DVSCFG in combination with the DVS_PIN1 and DVS_PIN2 sets the active DVS for the respective BUCK. BUCKx_DVSCTRL[0] should be OTP programmed high before the start-up sequence. (the 'X' in Table 6 indicates that either a 0 or 1 is acceptable).

Table 6. Global DVS Pin Logic

BUCKX_DVSPIN_CTRL[1:0]	DVS_PIN1	DVS_PIN0	Active DVS
0x0	X	X	DVS0
0x1	X	0	DVS0
	X	1	DVS1
0x2	0	X	DVS0
	1	X	DVS2
0x3	0	0	DVS0
	0	1	DVS1
	1	0	DVS2
	1	1	DVS3

(ii) IO_PINMODE = 0x6: I^2C with two DVS pins for BUCK1, one DVS pin for BUCK2.

MPIO0	MPIO1	MPIO2	GPIO0	GPIO1
BUCK1_ DVS0	BUCK1_ DVS1	BUCK2_ DVS0	I2C_ CLK	I2C_ SDA

Table 7. 2 DVS Pins Logic

BUCKx_DVS1	BUCKx_DVS0	Active DVS for BUCKx
0	0	DVS0
0	1	DVS1
1	0	DVS2
1	1	DVS3

(iii) IO_PINMODE = 0x7: I^2C with one DVS pin for BUCK1, BUCK2, BUCK3.

MPIO0	MPIO1	MPIO2	GPIO0	GPIO1
BUCK1_ DVS0	BUCK2_ DVS0	BUCK3_ DVS0	I2C_ CLK	I2C_ SDA

BUCKx_DVSCTRL[0] should be OTP programmed high before the start-up sequence.

Table 8. Single DVS Pin Logic

Function	
Buckx_DVS0	Active DVS for BUCKx
0	DVS0
1	DVS1

5.5 Configuring DVS Speed

5.5.1 Power-Up and Shutdown Slew Rate Setting

The BUCKx_RSPPUP[2:0] bits in the BUCKx_RSPCFG0 register set the slew rates (DVS speed) in BUCKx only during V_{OUTx} power-up. Similarly, BUCKx_RSPPDN[2:0] in the BUCKx_RSPCFG0 register sets the slew rates in BUCKx during normal V_{OUTx} shutdown. The achievable slew rates vary with different FBDIV settings (factory OTP programmed). For more details see Register "BUCK1_RSPCFG0" on page 43.

5.5.2 DVS Transition Slew Rate Setting

BUCKx_RSPUP[2:0] and BUCKx_RSPDN[2:0] in the BUCKx_RSPCFG1 register set the slew rates (DVS speed) in BUCKx during normal DVS transition. The achievable slew rates vary with different FBDIV settings (factory OTP programmed). For more details see Register "BUCK1_RSPCFG1" on page 42.

5.6 Output Voltage Setting

Each output voltage is set by writing a 10-bit word to DVS Configuration 1 (BUCKx_DVS0CFG1 register) and DVS Configuration 0 (BUCKx_DVS0CFG0 register) in each buck. Configuration 1 holds the MSB and Configuration 0 holds the last two bits of the 10-bit word. The output voltage does not change until the LSB register has been written. "BUCK1_DVS0CFG1" on page 40 shows the relationship between the DVS word and V_{OUT}.

5.7 Power Sequencing

When the Master Chip Enable pin (EN) is brought above an NMOS threshold, the ISL91212A and ISL91212B power up their key biasing circuits, load the OTP configuration registers, and then start the power-up sequence.

Note: The ISL91212A and ISL91212B support flexible power sequencing, delay timing, and slew rate. For more information, contact your local Renesas sales office.

5.7.1 Buck Start-Up from Master Chip Enable Pin (EN)

ISL91212A and ISL91212B use a chip enable pin (EN) as a master enable control signal for all buck instances. In addition, there are also digital enable bits (IO_BUCKx_EN) as seen per register "IO_MODECTRL" on page 38, with an individual enable control bit for each buck output, each with a default value per OTP of "1", or enabled for each buck instance. The resulting enable state for a given buck output is the state of the chip enable pin (EN) logically ANDed with the respective IO_BUCKx_EN bit. For example, to enable BUCK1, the chip enable pin needs to be high and IO_BUCK1_EN needs to be high. When the enable state of a buck output changes, the sequencing is governed per OTP settings described in the following.

When power is applied to ISL91212A/ISL91212B and the master chip enable pin (EN) transitions logically from 0 to 1, ISL91212A/ISL91212B run an internal boot sequence to load OTP values. This OTP loading nominally takes 1.4ms. After the OTP boot, ISL91212A/ISL91212B execute the OTP-programmed startup sequence for each buck output. Each buck output ramps at a default value of 3mV/µs.

The delay time for startup/shutdown from the master chip enable pin (EN) toggling is configurable from 0ms to 63ms with increments of 1ms for each buck output. The startup delay is set by the BUCKx_EN_DLY registers. The shutdown delay is set by the BUCKx_SHUTDN_DLY registers.

Figure 36 provides an example of power-up configurability. The master chip enable pin (EN) transitions from 0 to 1 and OTP is loaded over 1.4ms. After that initial 1.4ms boot interval, the buck output startup sequence begins. In the Figure 36 example, BUCK1_EN_DLY is set for 0ms, BUCK2_EN_DLY is set for 1ms, BUCK3_EN_DLY is set for 2ms and BUCK4_EN_DLY is set for 3ms.

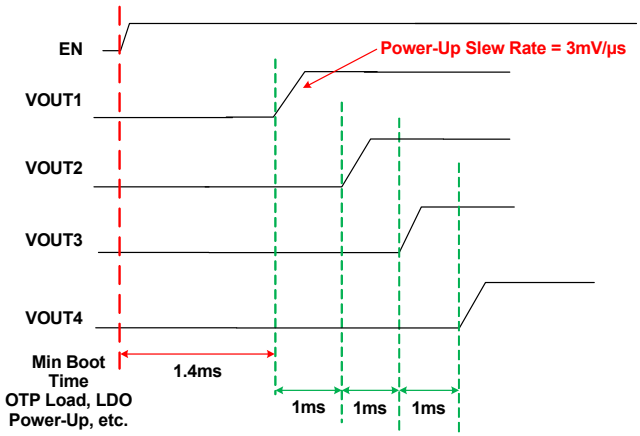


Figure 36. Chip Power-Up Example

5.7.2 Buck Power-Down from Master Chip Enable Pin (EN)

When buck outputs are disabled due to the master chip enable pin (EN) falling below its logic high threshold, all the buck instances become disabled and ramp down at 3mV/µs, following the programmed BUCKx_SHUTDN_DLY values. This is then followed by the power-down of the bias circuits, forcing the PMIC into a shutdown state.

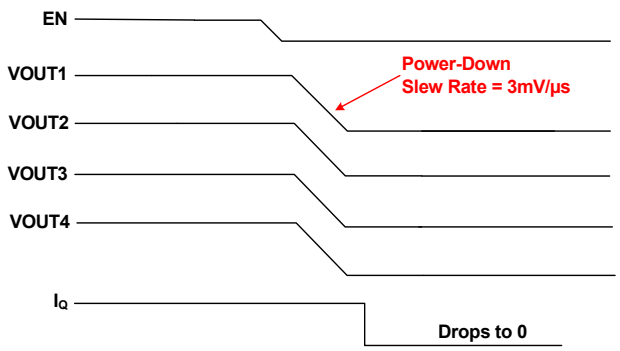


Figure 37. Chip Power-Down Example

The default slew rate for each buck discharging during power-down sequence is 3mV/µs. This slew rate is controlled until the output voltage is ~250mV. Below 250mV, there are two output voltage decay options:

Option 1: If the disable event for a buck output is the master chip enable pin (EN) falling below its logic high threshold, then when the output falls below 250mV, the output voltage decay is dictated by the system load passively discharging the buck output capacitance.

Option 2: If the disable event for a buck output is the master chip enable pin (EN) remaining high and the enable register bit (IO_BUCKx_EN) transitioning form a logic 1 to a logic 0, then it is possible to use the PULL_DOWN_DISCHARGE bit per the BUCK2_CFG2 register to globally enable weak pull-down resistors (1 per buck output) to actively discharge each output below the 250mV threshold.

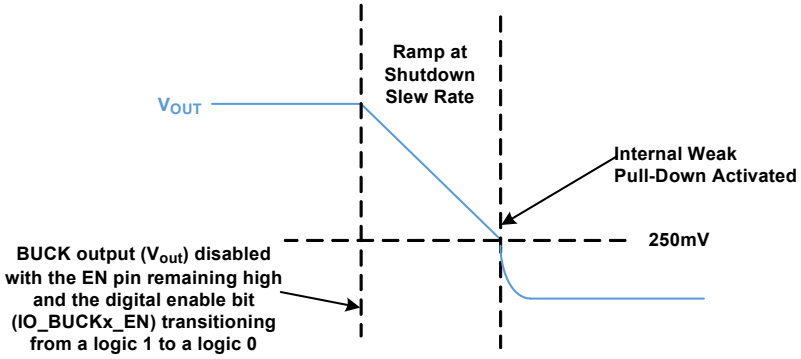


Figure 38. Buck Disable Waveform Using PULL_DOWN_DISCHARGE

5.8 Interrupt Pin

The ISL91212A and ISL91212B can alert the host when a warning or a fault has occurred through an IRQ interrupt request signal with configurable masking options that is connected to a configurable interrupt (INT) pin. The interrupt pin can be programmed to be active high, active low, an open drain, or a CMOS output.

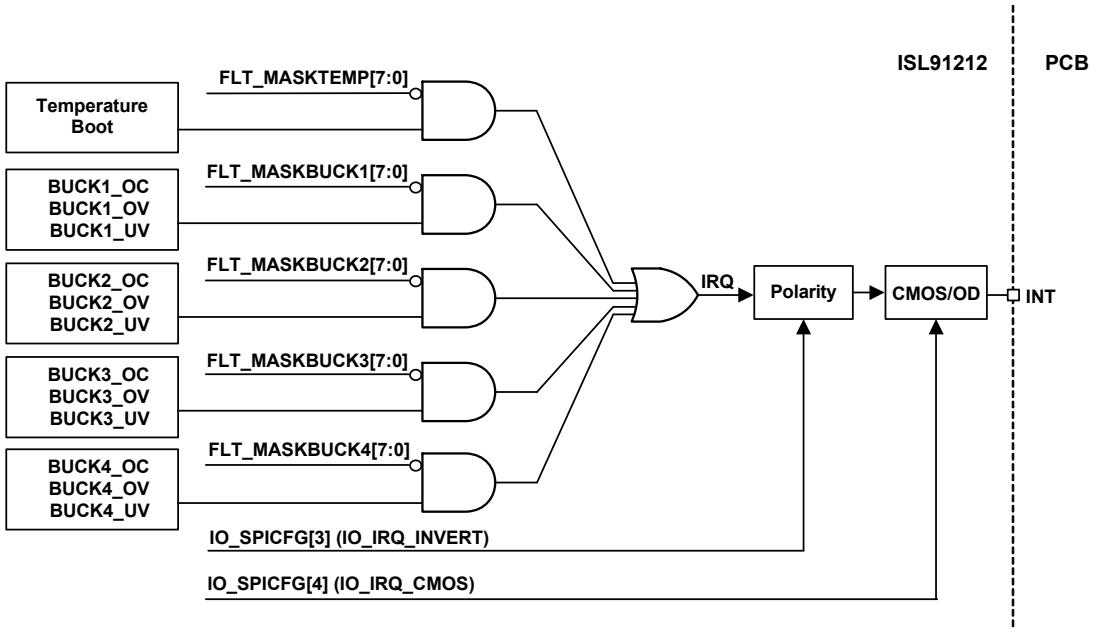


Figure 39. Interrupt Tree

6. Protection Features (Faults)

The ISL91212A and ISL91212B have overcurrent, overvoltage, undervoltage, and over-temperature protection features.

6.1 Over-Temperature Protection

The ISL91212A and ISL91212B provide protection against over-temperature conditions. The over-temperature protection circuit continuously monitors the chip's die temperature and raises a fault when the temperature exceeds +150°C. When the over-temperature fault occurs, all the buck converters, by default, shut down and then re-enable when the OT fault deasserts. Hysteresis enables the circuit to clear the fault after the temperature is below a predefined safe temperature. Hysteresis is hard coded as the difference between +95°C and +150°C.

6.2 Overcurrent Protection Mode

The overcurrent protection block has a current comparator that compares the load current through the high-side power FET with the reference current level through a replica device. After R-C delay filtering and/or cycle detection filtering, the output of the overcurrent protection block goes to the fault detection block, which makes the decision to disable the buck and latch the power-stage into high impedance mode. The digital core periodically re-enables the buck to detect if the fault has cleared.

6.3 Overvoltage (OV)/Undervoltage (UV) Protection

The ISL91212A and ISL91212B protect against output overvoltage and undervoltage fault conditions. The OV/UV protection circuitry has low power comparators configured with differential input and single-ended outputs capable of working over a large common-mode input range. This comparator monitors the output voltage in both DCM and CCM for faults. By default, when an OV event is triggered, the buck converter crowbars the output by turning on the low-side NMOS for a duration of 32µs to 64µs. After that the buck shuts down and exits crowbar. The buck tries to start up and if the fault condition still exists, the buck reacts to OV again until the fault is removed. When an UV event is triggered, the buck converter shuts down and re-start up until the fault is cleared. The UV/OV threshold is a configurable window around the V_{OUT} DAC target. The default setting is ±250mV.

7. I2C Serial Interface

The I2C interface is a simple bidirectional 2-wire bus protocol, consisting of serial clock control (SCL/I2C_CLK) and serial data signal (SDA). The I2C address for the ISL91212A and ISL91212B is 0x1E. The ISL91212A and ISL91212B host a slave I2C interface that supports data speeds up to 3.4Mbps. I2C_CLK is an input to the ISL91212A and ISL91212B and is supplied by the controller, whereas SDA is bidirectional. The ISL91212A and ISL91212B have an open-drain output to transmit data on SDA. An external pull-up resistor must be placed on the serial data line to pull the drain output high during data transmission.

The chip supports 7-bit addressing. The ISL91212A and ISL91212B I2C device address is reconfigurable through the OTP.

All communication over the I2C interface is conducted by sending the MSB of each byte of data first. Data states on the SDA line can change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions.

All I2C interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The ISL91212A and ISL91212B continuously monitor the SDA and SCL lines for the START condition and do not respond to any command until this condition is met. All I2C interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH.

An ACK (Acknowledge) is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data. The ISL91212A and ISL91212B respond with an ACK after recognizing a START condition followed by a valid Identification (I2C Address) Byte. The ISL91212A and ISL91212B also respond with an ACK after receiving a Data Byte of a write operation. The master must respond with an ACK after receiving a Data Byte of a read operation.

7.1 Write Operation

A Write operation requires a START condition, followed by the ISL91212A and ISL91212B I2C Address byte with the R/W bit set to 0, a Register Address Byte, data bytes, and a STOP condition. After each byte, the ISL91212A and ISL91212B respond with an ACK. After every data byte, the ISL91212A and ISL91212B auto increment the register address so subsequent data bytes get written to sequentially incremental register locations. A STOP condition that terminates the write operation must be sent by the master after sending at least one full data byte and its associated ACK signal. If a STOP byte is issued in the middle of a data byte, the write is not performed.

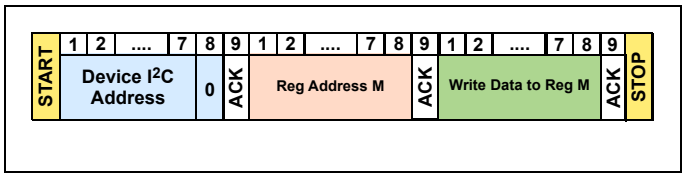


Figure 40. 1 Byte Write to Register M

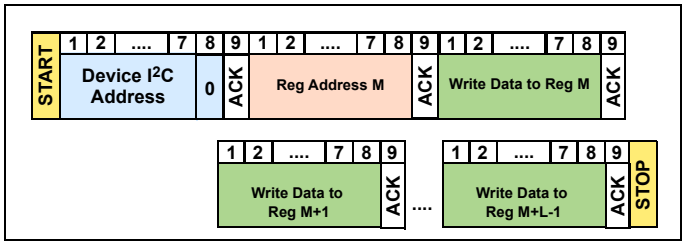


Figure 41. L Byte Sequential Data Write Starting Register M

7.2 Read Operation

The Read operation consists of a three byte “dummy write” instruction to send the register address to begin reading from, followed by a Current Address Read operation. The master initiates the operation by issuing the following sequence: a START condition, followed by the ISL91212A and ISL91212B I²C Address byte with the R/W bit set to “0”, a Register Address Byte, a second START, and a second ISL91212A and ISL91212B I²C Address byte with the R/W bit set to “1”. After each of the three bytes, the ISL91212A and ISL91212B respond with an ACK. The ISL91212A and ISL91212B then transmit data bytes. The master terminates the Read operation from the ISL91212A and ISL91212B by issuing a STOP condition following the last bit of the last data byte. After every data byte, the ISL91212A and ISL91212B auto increment the register address so subsequent data bytes are sent from sequentially incremental register locations.

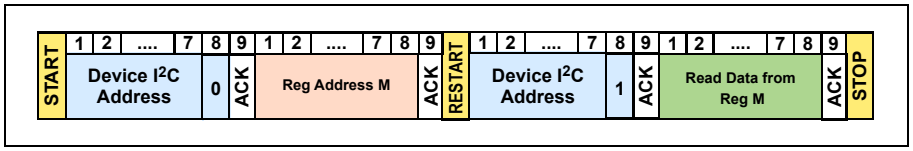


Figure 42. 1 Byte Data Read from Register M

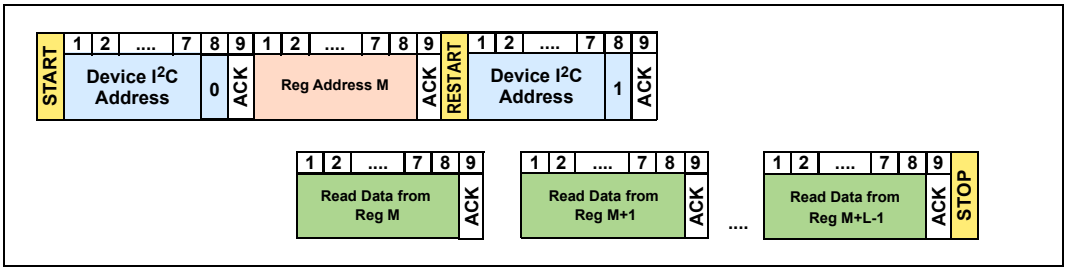


Figure 43. L Byte Sequential Data Read Starting with Register M

7.3 I²C Timing

The timing specifications of the I²C I/O from the I²C specification are shown in Figure 44 and Table 9. The I²C controller provides a slave I²C transceiver capable of interpreting the I²C protocol in Standard, Fast, Fast+, and High Speed modes.

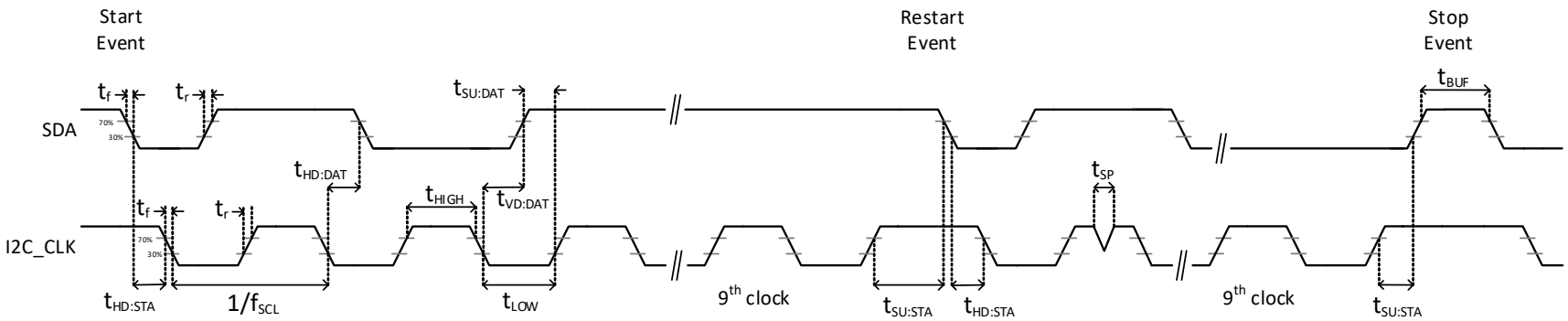


Figure 44. I²C Timing

Table 9. I²C Timing

Parameter	Symbol	Standard Mode		Fast Mode		Fast Mode Plus		High Speed Mode		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Clock frequency	f_{SCL}	0	100	0	400	0	1000	0	3400	kHz
Hold Time (repeated) START Condition (after this period, the first clock pulse is generated)	$t_{HD;STA}$	4000	-	600	-	260	-	160	-	ns
LOW Period of the SCL Clock	t_{LOW}	4700	-	1300	-	500	-	160	-	ns
HIGH Period of the SCL Clock	t_{HIGH}	4000	-	600	-	260	-	60	-	ns
Set-Up Time for a Repeated START Condition	$t_{SU;STA}$	4700	-	600	-	260	-	160	-	ns
Data Hold Time	$t_{HD;DAT}$	15	-	15	-	15	-	15	70	ns
Data Set-Up Time	$t_{SU;DAT}$	250	-	100	-	50	-	10	-	ns
Rise Time of SCL	t_{rCL}	-	1000	-	300	-	120	-	40	ns
Fall Time of SCL	t_{fCL}	-	300	-	300	-	120	-	40	ns
Rise Time of SDA	t_{rDA}	-	1000	-	300	-	120	-	80	ns
Fall Time of SDA	t_{fDA}	-	300	-	300	-	120	-	80	ns
Set-Up Time for STOP Condition	$t_{SU;STO}$	4000	-	600	-	260	-	160	-	ns
Bus Free Time between a STOP and START Condition	t_{BUF}	4700	-	1300	-	500	-	-	-	ns
Capacitive Load for each Bus Line	C_b	-	400	-	400	-	400		100	pF
Output Fall Time from VIHmin to VILmax	t_{of}	-	250[5]	20 × (V_{DD} /5.5V)[6]	250[5]	20 × (V_{DD}/5.5V)[6]	120[7]	10 (Note 12)	80	ns
Pulse Width of Spikes Suppressed by the Input Filter	t_{SP}	-	-	0	50	0	50	0	10	ns

Notes:

11. Only valid for V_{DD} < 4V.
12. Only valid for V_{DD} < 1.9V.
13. V_{DD} is the pull-up source to the I²C lines (GPIO0, GPIO1).

8. Board Layout Recommendations

The ISL91212A and ISL91212B are 4-channel PMICs consisting of high frequency switching regulators with dual and single phase capability. The PCB layout is important to ensure satisfactory performance. The power loop is composed of the output inductor L, the output capacitor C_{OUT}, the SW pin, and the PGND pin. Make the power loop as small as possible. The connecting traces among them should be direct, short, and wide. The same practice should be applied to connections at the PVIN. Place the input capacitor as close as possible to PVIN and PGND pins of the corresponding power stage.

The switching node of the converter, the SW pin, and the traces connected to this node are very noisy, so keep the remote sense lines and other noise sensitive traces away from these traces. Keep the trace connecting between the SW pin and the inductor short and wide, and use multiple copper planes in parallel with sufficient vias in between to maximize thermal performance and efficiency. Renesas recommends descending only one layer for the phase traces to reduce the effective path to the inductor. Also, ensure the length and width of each inductor trace and number of vias used match resistances to help ensure proper current matching when using the dual phase configuration in the ISL91212A.

The ground of the input and output capacitors should be connected as close as possible. Use as much ground plane as possible underneath the ISL91212A and ISL91212B to support high current flow, and create a low impedance path for return current between the ISL91212A and ISL91212B and the load. Use solid ground plane as much as possible, which helps isolate SW node traces and high-speed clock signals from interfering with remote sense lines in adjacent layers, and is helpful for good EMI performance.

Place an AVIN filter capacitor as close as possible to the ISL91212A and ISL91212B but away from noise sources, and always reference the GND pad of the decoupling capacitor to a quiet GND plane. The AVIN and AGND pins of the ISL91212A and ISL91212B should reference to a copper plane.

Do not use plated through-holes when passing the WLCSP pins to lower layers. Renesas recommends staggering microvias if they pass down multiple layers.

VOUT and RTN lines are used to sense the output voltage and should be routed directly to the load. Connecting the RTN line to ground away from the load causes a ground error in the output voltage load regulation due to parasitic ground resistance. Also, keep these traces away from switching nodes such as phase nodes or high-speed digital signals. Use small low inductance (ESL) capacitors at the load to improve noise immunity and transient response to the ISL91212A and ISL91212B.

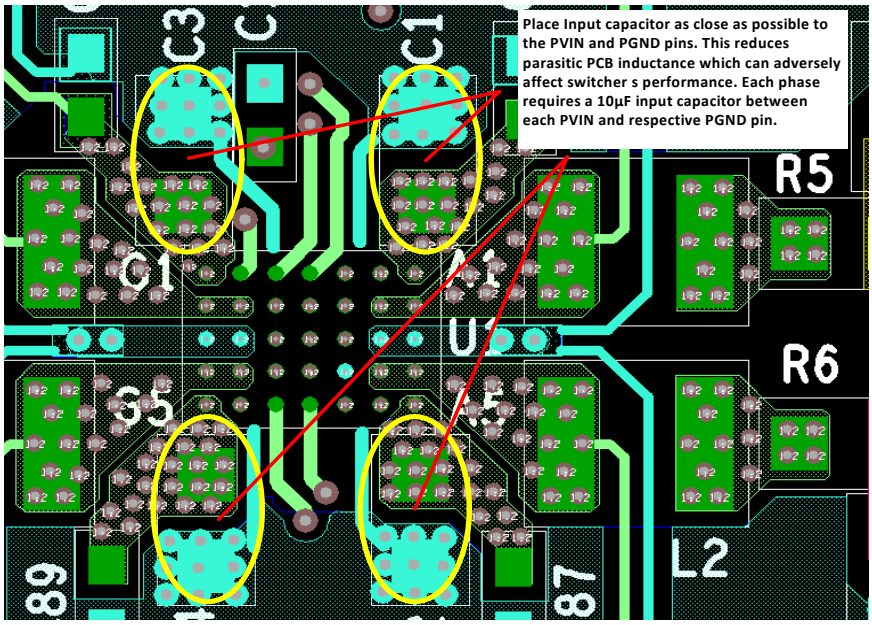


Figure 45. Recommended PCB Layout Top Layer

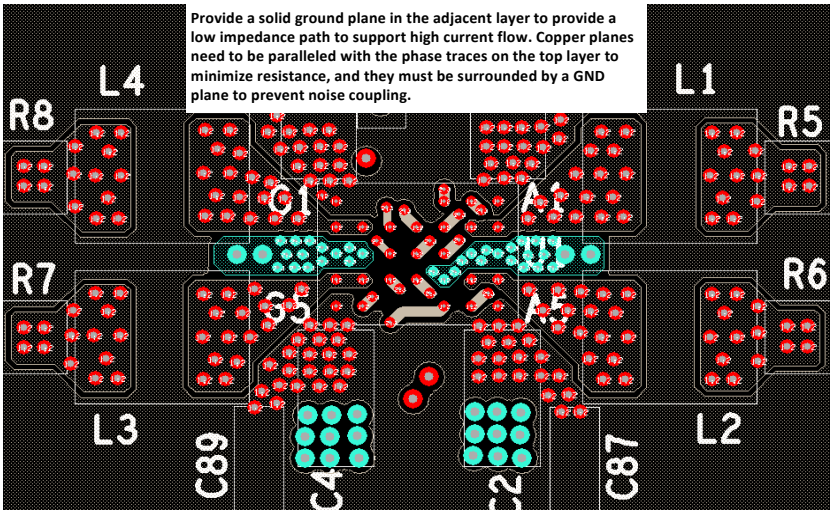


Figure 46. Recommended PCB Layout Second Layer

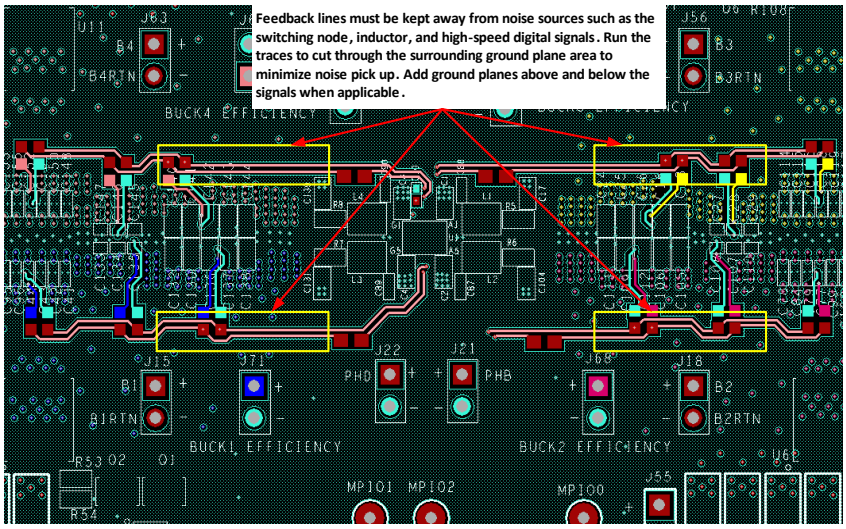


Figure 47. Recommended PCB Layout Bottom Layer

8.1 PCB Layout Summary

- Place input capacitors as close as possible to their respective PVIN and PGND pins
- Route phase nodes with short, wide traces and avoid any sensitive nodes
- Route VOUT and RTN lines directly to the load using small low inductance capacitors at the load for bypassing
- Place output capacitors close to the inductors and with a low impedance path to the PGND pins
- Keep digital and phase nodes from intersecting AVIN_FILT, VOUT, and RTN lines
- Create a PGND plane on the second layer of the PCB below the power components and bumps carrying high switching currents

8.2 PCB Design for WLCSP Recommendations

Table 10. PCB Design for WLCSP Recommendations

Design Feature	Design Specification
Cu Pad Diameter	0.5mm pitch: 0.250 mm
Microvia Structure	All microvias should be copper filled vias.
Microvia Stacking	Avoid microvia stacking if possible. Use staggered vias instead. If microvia stacking is absolutely necessary for the layout, the maximum number of recommended via stacks is two.
Plated Through-Hole (PTH) Location	No PTH should be placed under the CSP bump pads. Microvias and trace routing should be used to fan the PTH away from the CSP bump array.

9. Register Address Map

Address	Register	Address	Register	Address	Register
0x01	IO_CHIPNAME	0x55	BUCK1_RSPCFG0	0x7F	BUCK3_DVS1CFG0
0x13	FLT_RECORDTEMP	0x56	BUCK1_EN_DLY	0x80	BUCK3_DVS2CFG1
0x14	FLT_RECORDBUCK1	0x57	BUCK1_SHUTDN_DLY	0x81	BUCK3_DVS2CFG0
0x15	FLT_RECORDBUCK2	0x58	BUCK2_EA2	0x82	BUCK3_DVS3CFG1
0x16	FLT_RECORDBUCK3	0x5B	BUCK2_DCM	0x83	BUCK3_DVS3CFG0
0x17	FLT_RECORDBUCK4	0x5C	BUCK2_CFG3	0x87	BUCK3_DVSSEL
0x23	IO_SPICFG	0x5D	BUCK2_CFG2	0x88	BUCK3_RSPCFG1
0x24	IO_MODECTRL	0x62	BUCK2_DVS0CFG1	0x89	BUCK3_RSPCFG0
0x32	FLT_MASKTEMP	0x63	BUCK2_DVS0CFG0	0x8A	BUCK3_EN_DLY
0x33	FLT_MASKBUCK1	0x64	BUCK2_DVS1CFG1	0x8B	BUCK3_SHUTDN_DLY
0x34	FLT_MASKBUCK2	0x65	BUCK2_DVS1CFG0	0x8C	BUCK4_EA2
0x35	FLT_MASKBUCK3	0x66	BUCK2_DVS2CFG1	0x8F	BUCK4_DCM
0x36	FLT_MASKBUCK4	0x67	BUCK2_DVS2CFG0	0x90	BUCK4_CFG3
0x3B	BUCK1_EA2	0x68	BUCK2_DVS3CFG1	0x96	BUCK4_DVS0CFG1
0x3E	BUCK1_DCM	0x69	BUCK2_DVS3CFG0	0x97	BUCK4_DVS0CFG0
0x3F	BUCK1_CFG3	0x6D	BUCK2_DVSSEL	0x98	BUCK4_DVS1CFG1
0x48	BUCK1_DVS0CFG1	0x6E	BUCK2_RSPCFG1	0x99	BUCK4_DVS1CFG0
0x49	BUCK1_DVS0CFG0	0x6F	BUCK2_RSPCFG0	0x9A	BUCK4_DVS2CFG1
0x4A	BUCK1_DVS1CFG1	0x70	BUCK2_EN_DLY	0x9B	BUCK4_DVS2CFG0
0x4B	BUCK1_DVS1CFG0	0x71	BUCK2_SHUTDN_DLY	0x9C	BUCK4_DVS3CFG1
0x4C	BUCK1_DVS2CFG1	0x72	BUCK3_EA2	0x9D	BUCK4_DVS3CFG0
0x4D	BUCK1_DVS2CFG0	0x75	BUCK3_DCM	0xA1	BUCK4_DVSSEL
0x4E	BUCK1_DVS3CFG1	0x76	BUCK3_CFG3	0xA2	BUCK4_RSPCFG0
0x4F	BUCK1_DVS3CFG0	0x7C	BUCK3_DVS0CFG1	0xA3	BUCK4_RSPCFG1
0x53	BUCK1_DVSSEL	0x7D	BUCK3_DVS0CFG0	0xA4	BUCK4_EN_DLY
0x54	BUCK1_RSPCFG1	0x7E	BUCK3_DVS1CFG1	0xA5	BUCK4_SHUTDN_DLY

Note: The registers not listed in the register map and RESERVED bits in the register map are reserved for factory use only. Changing these registers/bits can result in unexpected operation.

10. Register Description by Address

Address	Bit	Name	R/W	Default	Description
IO_CHIPNAME					
0x01	7:0	IO_CHIPNAME	R	0x03	Chip Name 0x03: ISL91212A and ISL91212B
FLT_RECORDTEMP					
0x13	7	FLT_BOOT	R	0x0	BOOT Occurred Read only, cleared when read 0x0: No boot process has occurred. 0x1: Boot process has occurred, OTP read is finished.
	6:2	RSVD	R	0x0	Reserved
	1	FLT_TEMPSDR	R	0x0	Over-Temperature (OT) Shutdown (Rising Threshold) Read only, cleared when read 0x0: No fault, less than threshold. 0x1: Fault, greater than threshold.
	0	FLT_TEMPSDF	R	0x0	Over-Temperature (OT) Shutdown (Falling Threshold) Read only, cleared when read 0x0: No fault, less than threshold. 0x1: Fault, greater than threshold.
FLT_RECORDBUCK1					
0x14	7	RSVD	R	0x0	Reserved
	6	FLT_BUCK1_OC	R	0x0	Overcurrent (OC) for BUCK1 Read only, cleared when read 0x0: No fault, less than threshold. 0x1: Fault, greater than threshold.
	5	FLT_BUCK1_OV	R	0x0	Overvoltage (OV) Read only, cleared when read 0x0: No fault, less than threshold. 0x1: Fault, greater than threshold.
	4	FLT_BUCK1_UV	R	0x0	Undervoltage (UV) Read only, cleared when read 0x0: No fault, less then threshold. 0x1: Fault, greater than threshold.
	3:0	RSVD	R	0x0	Reserved

Address	Bit	Name	R/W	Default	Description
FLT_RECORDBUCK2					
0x15	7	RSVD	R	0x0	See "FLT_RECORDBUCK1"
	6	FLT_BUCK2_OC	R	0x0	
	5	FLT_BUCK2_OV	R	0x0	
	4	FLT_BUCK2_UV	R	0x0	
	3:0	RSVD	R	0x0	
FLT_RECORDBUCK3					
0x16	7	RSVD	R	0x0	See "FLT_RECORDBUCK1"
	6	FLT_BUCK3_OC	R	0x0	
	5	FLT_BUCK3_OV	R	0x0	
	4	FLT_BUCK3_UV	R	0x0	
	3:0	RSVD	R	0x0	
FLT_RECORDBUCK4					
0x17	7	RSVD	R	0x0	See "FLT_RECORDBUCK1"
	6	FLT_BUCK4_OC	R	0x0	
	5	FLT_BUCK4_OV	R	0x0	
	4	FLT_BUCK4_UV	R	0x0	
	3:0	RSVD	R	0x0	
IO_SPICFG					
0x23	7:5	RSVD	R	0x0	Reserved
	4	IO_IRQ_CMOS	R/W	0x0	IRQ Type 0x0 OD Output 0x1 CMOS Output
	3	IO_IRQ_INVERT	R/W	0x1	IRQ Polarity 0x0 Active High 0x1 Active Low
	2:1	RSVD	R	0x0	Reserved
	0	RSVD	R	0x1	Reserved

Address	Bit	Name	R/W	Default	Description
IO_MODECTRL					
0x24	7	IO_BUCK1_EN	R/W	0x1	Enable for BUCK1 0x0 Buck1 disabled. 0x1 Buck1 enabled.
	6	IO_BUCK2_EN	R/W	0x1	Enable for BUCK2 0x0 Buck2 disabled. 0x1 Buck2 enabled.
	5	IO_BUCK3_EN	R/W	0x1	Enable for BUCK3 0x0 Buck3 disabled. 0x1 Buck3 enabled.
	4	IO_BUCK4_EN	R/W	0x1	Enable for BUCK4 0x0 Buck4 disabled. 0x1 Buck4 enabled.
	3	RSVD	R	0x0	Reserved
	2	IO_ENVPPPULLDOWN	R/W	0x01	Enable for Weak Pull-Down on EN/VPP Pin 0x0 Weak Pull-Down disabled. 0x1 Weak Pull-Down enabled.
	1	RSVD	R	0x0	Reserved
	0	RSVD	R	0x1	Reserved
FLT_MASKTEMP					
0x32	7	FLT_MASKBOOT	R/W	0x0	Mask IRQ for FLT_BOOT 0x0 IRQ passed to output pin. 0x1 IRQ masked from output pin.
	6:2	RSVD	R	0x0	Reserved
	1	FLT_MASKEMPSDR	R/W	0x0	Mask IRQ for FLT_TEMPSDR 0x0 IRQ passed to output pin. 0x1 IRQ masked from output pin.
	0	FLT_MASKTEMPSDF	R/W	0x0	Mask IRQ for FLT_TEMPSDF 0x0 IRQ passed to output pin. 0x1 IRQ masked from output pin.

Address	Bit	Name	R/W	Default	Description
FLT_MASKBUCK1					
0x33	7	RSVD	R	0x0	Reserved
	6	FLT_BUCK1_MASKOC	R/W	0x0	Mask IRQ for FLT_BUCK1_OC 0x0 IRQ passed to output pin. 0x1 IRQ masked from output pin.
	5	FLT_BUCK1_MASKOV	R/W	0x0	Mask IRQ for FLT_BUCK1_OV 0x0 IRQ passed to output pin. 0x1 IRQ masked from output pin.
	4	FLT_BUCK1_MASKUV	R/W	0x0	Mask IRQ for FLT_BUCK1_UV 0x0 IRQ passed to output pin. 0x1 IRQ masked from output pin.
	3:0	RSVD	R	0x0	Reserved
FLT_MASKBUCK2					
0x34	7	RSVD	R	0x0	See "FLT_MASKBUCK1"
	6	FLT_BUCK2_MASKOC	R/W	0x0	
	5	FLT_BUCK2_MASKOV	R/W	0x0	
	4	FLT_BUCK2_MASKUV	R/W	0x0	
	3:0	RSVD	R	0x0	
FLT_MASKBUCK3					
0x35	7	RSVD	R	0x0	See "FLT_MASKBUCK1"
	6	FLT_BUCK3_MASKOC	R/W	0x0	
	5	FLT_BUCK3_MASKOV	R/W	0x0	
	4	FLT_BUCK3_MASKUV	R/W	0x0	
	3:0	RSVD	R	0x0	
FLT_MASKBUCK4					
0x36	7	RSVD	R	0x0	See "FLT_MASKBUCK1"
	6	FLT_BUCK4_MASKOC	R/W	0x0	
	5	FLT_BUCK4_MASKOV	R/W	0x0	
	4	FLT_BUCK4_MASKUV	R/W	0x0	
	3:0	RSVD	R	0x0	

<table>
<tr><th>Address</th><th>Bit</th><th>Name</th><th>R/W</th><th>Default</th><th>Description</th></tr>
<tr><td colspan="6">BUCK1_EA2</td></tr>
<tr><td rowspan="2">0x3B</td><td>7:6</td><td>BUCK1_VOUTFBDIV</td><td>R/W</td><td>0x0</td><td>V_{OUT} feedback divider ratio for the control loop. Should only be changed when the Buck is Disabled (BUCK1_EN = 0).
<table>
<tr><th></th><th>Feedback Divider (FBDIV) (%)</th><th>V_{OUT} Max (V)</th></tr>
<tr><td>0x0</td><td>100</td><td>1.2</td></tr>
<tr><td>0x1</td><td>80</td><td>1.5</td></tr>
<tr><td>0x2</td><td>60</td><td>2.0</td></tr>
<tr><td>0x3</td><td>Reserved</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>5:0</td><td>RSVD</td><td>R/W</td><td>N/A</td><td>Reserved. Not Available.</td></tr>
<tr><td colspan="6">BUCK1_DCM</td></tr>
<tr><td rowspan="3">0x3E</td><td>7:3</td><td>Reserved</td><td>R</td><td>0x0</td><td>Reserved</td></tr>
<tr><td>2</td><td>BUCK1_FCCM</td><td>R/W</td><td>0x0</td><td>
<table>
<tr><td colspan="2">Forced Continuous Conduction Mode</td></tr>
<tr><td>0x0</td><td>DCM allowed when load reaches 0A</td></tr>
<tr><td>0x1</td><td>Always operate in CCM (Continuous Conduction Mode)</td></tr>
</table></td></tr>
<tr><td>1:0</td><td>Reserved</td><td>R/W</td><td>0x0</td><td>Reserved</td></tr>
<tr><td colspan="6">BUCK1_CFG3</td></tr>
<tr><td rowspan="2">0x3F</td><td>7:6</td><td>BUCK1_FSEL[1:0]</td><td>R/W</td><td>0x0</td><td>Buck’s steady-state switching frequency.
<table>
<tr><td>0x0</td><td>2MHz</td></tr>
<tr><td>0x1</td><td>3MHz</td></tr>
<tr><td>0x2</td><td>4MHz</td></tr>
<tr><td>0x3</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>5:0</td><td>RSVD</td><td>N/A</td><td>N/A</td><td>Reserved</td></tr>
<tr><td colspan="6">BUCK1_DVS0CFG1</td></tr>
<tr><td>0x48</td><td>7:0</td><td>BUCK1_DVS0VOUT92</td><td>R/W</td><td>TRIM For 0.9V</td><td>Upper eight bits of a 10-bit DAC[9:0] value to generate V_{OUT} for DVS Configuration 0.
Note: V_{OUT} must be programmed above 0.3V.
FBDIV is set by factory OTP to 1x, 0.8x, 0.6x.
<table>
<tr><th>FBDIV</th><th>1.0</th><th>0.8</th><th>0.6</th></tr>
<tr><th>DAC [9:0]</th><th>V_{OUT} (V)</th><th>V_{OUT} (V)</th><th>V_{OUT} (V)</th></tr>
<tr><td>0x000</td><td>0.0000</td><td>0.0000</td><td>0.0000</td></tr>
<tr><td>0x001</td><td>0.0012</td><td>0.0015</td><td>0.0020</td></tr>
<tr><td>…</td><td></td><td></td><td></td></tr>
<tr><td>0x200</td><td>0.6173</td><td>0.7716</td><td>1.0288</td></tr>
<tr><td>0x201</td><td>0.6185</td><td>0.7731</td><td>1.0308</td></tr>
<tr><td>…</td><td></td><td></td><td></td></tr>
<tr><td>0x3E5</td><td>1.1990</td><td>1.4988</td><td>1.9983</td></tr>
</table></td></tr>
</table>

Address	Bit	Name	R/W	Default	Description
BUCK1_DVS0CFG0					
0x49	7:6	BUCK1_DVS0VOUT10	R/W	TRIM For 0.9V	The lower two bits of a 10-bit DAC[9:0] value to generate V_{OUT} for the DVS configuration. Note: When DVS Configuration 0 is selected (through pins or registers) any write to BUCK1_DVS0CFG0 causes a DVS ramping event to occur. For details, see "Dynamic Voltage Scaling (DVS)" on page 21.
	5	RSVD	R	0x0	Reserved
	4:1	RSVD	R	0x0	Reserved
	0	RSVD	R	0x0	Reserved
BUCK1_DVS1CFG1					
0x4A	7:0	BUCK1_DVS1VOUT92	R/W	0xBF	See "BUCK1_DVS0CFG1"
BUCK1_DVS1CFG0					
0x4B	7:6	BUCK1_DVS1VOUT10	R/W	0x3	See "BUCK1_DVS0CFG0"
	5	RSVD	R	0x0	
	4:1	RSVD	R	0x0	
	0	RSVD	R	0x0	
BUCK1_DVS2CFG1					
0x4C	7:0	BUCK1_DVS2VOUT92	R/W	0x58	See "BUCK1_DVS0CFG1"
BUCK1_DVS2CFG0					
0x4D	7:6	BUCK1_DVS2VOUT10	R/W	0x0	See "BUCK1_DVS0CFG0"
	5	RSVD	R	0x0	
	4:1	RSVD	R	0x0	
	0	RSVD	R	0x0	
BUCK1_DVS3CFG1					
0x4E	7:0	BUCK1_DVS3VOUT92	R/W	0x00	See "BUCK1_DVS0CFG1"
BUCK1_DVS3CFG0					
0x4F	7:6	BUCK1_DVS3VOUT10	R/W	0x0	See "BUCK1_DVS0CFG0"
	5	RSVD	R	0x0	
	4:1	RSVD	R	0x0	
	0	RSVD	R	0x0	

Address	Bit	Name	R/W	Default	Description
BUCK1_DVSSEL					
0x53	7:3	RSVD	R	0x0	Reserved
	2	BUCK1_DVSCTRL	R/W	0x0	BUCK1 DVS Control 0x0: Use BUCK1_DVSSELECT to select the active DVS configuration.
	1:0	BUCK1_DVSSELECT	R/W	0x0	BUCK1 DVS Selection 0x0: Use DVS Configuration 0 in BUCK1_DVS0CFG and BUCK1_DVS0VOUT. 0x1: Use DVS Configuration 1 in BUCK1_DVS1CFG and BUCK1_DVS1VOUT. 0x2: Use DVS Configuration 2 in BUCK1_DVS2CFG and BUCK1_DVS2VOUT. 0x3: Use DVS Configuration 3 in BUCK1_DVS3CFG and BUCK1_DVS3VOUT. Note: When BUCK1_DVSCTRL = 0x0 any write to the register BUCK1_DVSSEL causes a DVS ramping event to occur.
BUCK1_RSPCFG1					
0x54	7	RSVD	R	0x0	Reserved
	6:4	BUCK1_RSPUP	R/W	0x7	V_{OUT} Ramp Slew Rate RSP = BUCK1_RSPUP[1:0], Ramp Speed FBDIV = BUCK1_VOUTFBDIV[1:0] = (1.0, 0.8, 0.6) Slow = BUCK1_RSPUP[2] = 0 Fast = BUCK1_RSPUP[2] = 1
	3	RSVD	R/W	0x0	Reserved
	2:0	BUCK1_RSPDN	R/W	0x3	See "BUCK1_RSPUP" for rate definition

RSP	FBDIV	V_{OUT} Ramp Speed mV/µs Fast	V_{OUT} Ramp Speed mV/µs Slow
0x0	1.0	12	3
0x1	1.0	24	6
0x2	1.0	58	14
0x3	1.0	115	29

RSP	FBDIV	V_{OUT} Ramp Speed mV/µs Fast	V_{OUT} Ramp Speed mV/µs Slow
0x0	0.8	12	3
0x1	0.8	24	6

RSP	FBDIV	V_{OUT} Ramp Speed mV/µs Fast	V_{OUT} Ramp Speed mV/µs Slow
0x0	0.6	12	3
0x1	0.6	24	6

Address	Bit	Name	R/W	Default	Description
BUCK1_RSPCFG0					
0x55	7	RSVD	R	0x0	Reserved
	6:4	BUCK1_RSPPUP	R/W	0x7	VOUT Ramp Slew Rate RSP = BUCK1_RSPUP[1:0], Ramp Speed FBDIV = BUCK1_VOUTFBDIV[1:0] = (1.0, 0.8, 0.6) Slow = BUCK1_RSPUP[2] = 0 Fast = BUCK1_RSPUP[2] = 1
	3	BUCK	R/W	0x0	Reserved
	2:0	BUCK1_RSPPDN	R/W	0x3	See "BUCK1_RSPPUP" for rate definition
BUCK1_EN_DLY					
0x56	7:6	BUCK1_ENPIN_CFG	R/W	0x0	EN_X pin control is valid only in PINMODE 1. BUCK EN Control = IO_BUCK1_EN and BUCK1_EN_PIN If not in PINMODE 1, BUCK1_EN_PIN is default high, only IO_BUCK1_EN can toggle BUCK1 EN
	5:0	BUCK1_EN_DLY	R/W	0x0	Delay time from BUCK_EN pin and IO_REGVAID going high to BUCK1_EN control asserted. Delay = (integer value of register) ms [1ms/LSB]

RSP	FBDIV	V_{OUT} Ramp Speed mV/µs Fast	V_{OUT} Ramp Speed mV/µs Slow
0x0	1.0	6	1.2
0x1	1.0	12	3
0x2	1.0	29	7.2
0x3	1.0	58	15

RSP	FBDIV	V_{OUT} Ramp Speed mV/µs Fast	V_{OUT} Ramp Speed mV/µs Slow
0x0	0.8	12	3
0x1	0.8	24	6

RSP	FBDIV	V_{OUT} Ramp Speed mV/µs Fast	V_{OUT} Ramp Speed mV/µs Slow
0x0	0.6	12	3
0x1	0.6	24	6

BUCK1_EN_PIN	
0x0	EN_A
0x1	EN_B
0x2	EN_C
0x3	1

Address	Bit	Name	R/W	Default	Description
BUCK1_SHUTDN_DLY					
0x57	7:6	BUCK1_DVSPIN_CFG	R/W	0x0	DVS_PIN_X pin control is valid only in PINMODE 3. DVS_1 = 0 DVS_0 = BUCK1_DVS_PIN0 and BUCK1_DVS_CTRL If not in PINMODE 3, DVS_PIN_x function is disabled BUCK1_DVS_PIN0 0x0 EN_A 0x1 EN_B 0x2 EN_C 0x3 1
	5:0	BUCK1_SHUTDN_DLY	R/W	0x0	Delay time from BUCK_EN pin or IO_REGVAID going low to BUCK1_EN control de-asserted. Delay = (integer value of register) ms [1ms/LSB]
BUCK2_EA2					
0x58	7:6	BUCK2_VOUTFBDIV	R/W	0x0	See "BUCK1_EA2"
	5:0	RSVD	R/W	N/A	
BUCK2_DCM					
0x5B	7:3	Reserved	R	0x0	Reserved
	2	BUCK2_FCCM	R/W	0x0	See "BUCK1_DCM"
	1:0	Reserved	R/W	0x0	Reserved
BUCK2_CFG3					
0x5C	7:6	BUCK2_FSEL[1:0]	R/W	0x0	See "BUCK1_CFG3"
	5:0	RSVD	R/W	N/A	
BUCK2_CFG2					
0x5D	7:4	RSVD	R/W	0x8	Reserved
	3	RSVD	R	TRIM	Reserved
	2	RSVD	R	0x0	Reserved
	1:0	PULL_DOWN_ DISCHARGE	R/W	0x0	VOUT pulldown when BUCK is shut off 0x0 Disable VOUT pulldown 0x1 Enable VOUT pulldown. Applies the weak pull-down feature for all the buck outputs. 1: Weak pull-down resistor is enabled when the buck output is turned off by software and master EN remains asserted. 0: Weak pull-down resistor is disabled when the buck output is turned off by software and master EN remains asserted.

Address	Bit	Name	R/W	Default	Description
BUCK2_DVS0CFG1					
0x62	7:0	BUCK2_DVS0VOUT92	R/W	TRIM For 0.9V	See "BUCK1_DVS0VOUT92"
BUCK2_DVS0CFG0					
0x63	7:6	BUCK2_DVS0VOUT10	R/W	TRIM for 0.9V	See "BUCK1_DVS0CFG0"
	5	RSVD	R	0x0	
	4:1	RSVD	R	0x0	
	0	RSVD	R	0x0	
BUCK2_DVS1CFG1					
0x64	7:0	BUCK2_DVS1VOUT92	R/W	0xBF	See "BUCK1_DVS0CFG1"
BUCK2_DVS1CFG0					
0x65	7:6	BUCK2_DVS1VOUT10	R/W	0x3	See "BUCK1_DVS0CFG0"
	5	RSVD	R	0x0	
	4:1	RSVD	R	0x0	
	0	RSVD	R	0x0	
BUCK2_DVS2CFG1					
0x66	7:0	BUCK2_DVS2VOUT92	R/W	0x58	See "BUCK1_DVS0CFG1"
BUCK2_DVS2CFG0					
0x67	7:6	BUCK2_DVS2VOUT10	R/W	0x0	See "BUCK1_DVS0CFG0"
	5	RSVD	R	0x0	
	4:1	RSVD	R	0x0	
	0	RSVD	R	0x0	
BUCK2_DVS3CFG1					
0x68	7:0	BUCK2_DVS3VOUT92	R/W	0x00	See "BUCK1_DVS0CFG1"
BUCK2_DVS3CFG0					
0x69	7:6	BUCK2_DVS3VOUT10	R/W	0x0	See "BUCK1_DVS0CFG0"
	5	RSVD	R	0x0	
	4:1	RSVD	R	0x0	
	0	RSVD	R	0x0	
BUCK2_DVSSEL					
0x6D	7:3	RSVD	R	0x0	See "BUCK1_DVSSEL"
	2	BUCK1_DVSCTRL	R/W	0x0	
	1:0	BUCK1_DVSSELECT	R/W	0x0	
BUCK2_RSPCFG1					
0x6E	7	RSVD	R	0x0	See "BUCK1_RSPCFG1"
	6:4	BUCK2_RSPUP	R/W	0x7	
	3	RSVD	R	0x0	
	2:0	BUCK2_RSPDN	R/W	0x3	

Address	Bit	Name	R/W	Default	Description
BUCK2_RSPCFG0					
0x6F	7	RSVD	R	0x0	See "BUCK1_RSPCFG0"
	6:4	BUCK2_RSPPUP	R/W	0x7	
	3	RSVD	R	0x0	
	2:0	BUCK2_RSPPDN	R/W	0x3	
BUCK2_EN_DLY					
0x70	7:6	BUCK2_ENPIN_CFG	R/W	0x1	See "BUCK1_ENPIN_CFG"
	5:0	BUCK2_EN_DLY	R/W	0x0	See "BUCK1_EN_DLY"
BUCK2_SHUTDN_DLY					
0x71	7:6	BUCK2_DVSPIN_CFG	R/W	0x1	See "BUCK1_DVSPIN_CFG"
	5:0	BUCK2_SHUTDN_DLY	R/W	0x0	See "BUCK1_SHUTDN_DLY"
BUCK3_EA2					
0x72	7:6	BUCK3_VOUTFBDIV	R/W	0x0	See "BUCK1_EA2"
	5:0	RSVD	R/W	N/A	
BUCK3_DCM					
0x75	7:3	Reserved	R	0x0	Reserved
	2	BUCK3_FCCM	R/W	0x0	See "BUCK1_DCM"
	1:0	Reserved	R/W	0x0	Reserved
BUCK3_CFG3					
0x76	7:6	BUCK3_FSEL[1:0]	R/W	0x0	See "BUCK1_CFG3"
	5:0	RSVD	R/W	N/A	
BUCK3_DVS0CFG1					
0x7C	7:0	BUCK3_DVS0VOUT92	R/W	TRIM For 0.9V	See "BUCK1_DVS0VOUT92"
BUCK3_DVS0CFG0					
0x7D	7:6	BUCK3_DVS0VOUT10	R/W	TRIM For 0.9V	See "BUCK1_DVS0CFG0"
	5	RSVD	R	0x0	
	4:1	RSVD	R	0x0	
	0	RSVD	R	0x0	
BUCK3_DVS1CFG1					
0x7E	7:0	BUCK3_DVS1VOUT92	R/W	0xBF	See "BUCK1_DVS0CFG1"
BUCK3_DVS1CFG0					
0x7F	7:6	BUCK3_DVS1VOUT10	R/W	0x3	See "BUCK1_DVS0CFG0"
	5	RSVD	R	0x0	
	4:1	RSVD	R	0x0	
	0	RSVD	R	0x0	
BUCK3_DVS2CFG1					
0x80	7:0	BUCK3_DVS2VOUT92	R/W	0x58	See "BUCK1_DVS0CFG1"

Address	Bit	Name	R/W	Default	Description
BUCK3_DVS2CFG0					
0x81	7:6	BUCK3_DVS2VOUT10	R/W	0x0	See "BUCK1_DVS0CFG0"
	5	RSVD	R	0x0	
	4:1	RSVD	R	0x0	
	0	RSVD	R	0x0	
BUCK3_DVS3CFG1					
0x82	7:0	BUCK3_DVS3VOUT92	R/W	0x00	See "BUCK1_DVS0CFG1"
BUCK3_DVS3CFG0					
0x83	7:6	BUCK3_DVS3VOUT10	R/W	0x0	See "BUCK1_DVS0CFG0"
	5	RSVD	R	0x0	
	4:1	RSVD	R	0x0	
	0	RSVD	R	0x0	
BUCK3_DVSSEL					
0x87	7:3	RSVD	R	0x0	Refer "BUCK1_DVSSEL"
	2	BUCK3_DVSCTRL	R/W	0x0	
	1:0	BUCK3_DVSSELECT	R/W	0x0	
BUCK3_RSPCFG1					
0x88	7	RSVD	R	0x0	See "BUCK1_RSPCFG1"
	6:4	BUCK3_RSPUP	R/W	0x7	
	3	RSVD	R	0x0	
	2:0	BUCK3_RSPDN	R/W	0x3	
BUCK3_RSPCFG0					
0x89	7	RSVD	R	0x0	See "BUCK1_RSPCFG0"
	6:4	BUCK3_RSPPUP	R/W	0x7	
	3	RSVD	R	0x0	
	2:0	BUCK3_RSPPDN	R/W	0x3	
BUCK3_EN_DLY					
0x8A	7:6	BUCK3_ENPIN_CFG	R/W	0x2	See "BUCK1_ENPIN_CFG"
	5:0	BUCK3_EN_DLY	R/W	0x0	See "BUCK1_EN_DLY"
BUCK3_SHUTDN_DLY					
0x8B	7:6	BUCK3_DVSPIN_CFG	R/W	0x2	See "BUCK1_DVSPIN_CFG"
	5:0	BUCK3_SHUTDN_DLY	R/W	0x0	See "BUCK1_SHUTDN_DLY"
BUCK4_EA2					
0x8C	7:6	BUCK4_VOUTFBDIV	R/W	0x0	See "BUCK1_EA2"
	5:0	RSVD	R/W	N/A	
BUCK4_DCM					
0x8F	7:3	Reserved	R	0x0	Reserved
	2	BUCK4_FCCM	R/W	0x0	See "BUCK1_DCM"
	1:0	Reserved	R/W	0x0	Reserved
BUCK4_CFG3					
0x90	7:6	BUCK4_FSEL[1:0]	R/W	0x0	See "BUCK1_CFG3"
	5:0	RSVD	R/W	N/A	

Address	Bit	Name	R/W	Default	Description
BUCK4_DVS0CFG1					
0x96	7:0	BUCK4_DVS0VOUT92	R/W	TRIM For 0.9V	See "BUCK1_DVS0VOUT92"
BUCK4_DVS0CFG0					
0x97	7:6	BUCK4_DVS0VOUT10	R/W	TRIM For 0.9V	See "BUCK1_DVS0CFG0"
	5	RSVD	R	0x0	
	4:1	RSVD	R	0x0	
	0	RSVD	R	0x0	
BUCK4_DVS1CFG1					
0x98	7:0	BUCK4_DVS1VOUT92	R/W	0xBF	See "BUCK1_DVS0CFG1"
BUCK4_DVS1CFG0					
0x99	7:6	BUCK4_DVS1VOUT10	R/W	0x3	See "BUCK1_DVS0CFG0"
	5	RSVD	R	0x0	
	4:1	RSVD	R	0x0	
	0	RSVD	R	0x0	
BUCK4_DVS2CFG1					
0x9A	7:0	BUCK4_DVS2VOUT92	R/W	0x58	See "BUCK1_DVS0CFG1"
BUCK4_DVS2CFG0					
0x9B	7:6	BUCK4_DVS2VOUT10	R/W	0x0	See "BUCK1_DVS0CFG0"
	5	RSVD	R	0x0	
	4:1	RSVD	R	0x0	
	0	RSVD	R	0x0	
BUCK4_DVS3CFG1					
0x9C	7:0	BUCK4_DVS3VOUT92	R/W	0x00	See "BUCK1_DVS0CFG1"
BUCK4_DVS3CFG0					
0x9D	7:6	BUCK4_DVS3VOUT10	R/W	0x0	See "BUCK1_DVS0CFG0"
	5	RSVD	R	0x0	
	4:1	RSVD	R	0x0	
	0	RSVD	R	0x0	
BUCK4_DVSSEL					
0xA1	7:3	RSVD	R	0x0	See "BUCK1_DVSSEL"
	2	BUCK4_DVSCTRL	R/W	0x0	
	1:0	BUCK4_DVSSELECT	R/W	0x0	
BUCK4_RSPCFG0					
0xA2	7	RSVD	R	0x0	See "BUCK1_RSPCFG0"
	6:4	BUCK4_RSPUP	R/W	0x7	
	3	RSVD	R	0x0	
	2:0	BUCK4_RSPDN	R/W	0x3	

Address	Bit	Name	R/W	Default	Description
BUCK4_RSPCFG1					
0xA3	7	RSVD	R	0x0	See "BUCK1_RSPCFG1"
	6:4	BUCK4_RSPPUP	R/W	0x7	
	3	RSVD	R	0x0	
	2:0	BUCK4_RSPPDN	R/W	0x3	
BUCK4_EN_DLY					
0xA4	1:0	BUCK4_ENPIN_CFG	R/W	0x2	See "BUCK1_ENPIN_CFG"
	5:0	BUCK4_EN_DLY	R/W	0x0	See "BUCK1_EN_DLY"
BUCK4_SHUTDN_DLY					
0xA5	1:0	BUCK4_DVSPIN_CFG	R/W	0x2	See "BUCK1_DVSPIN_CFG"
	5:0	BUCK4_SHUTDN_DLY	R/W	0x0	See "BUCK1_SHUTDN_DLY"

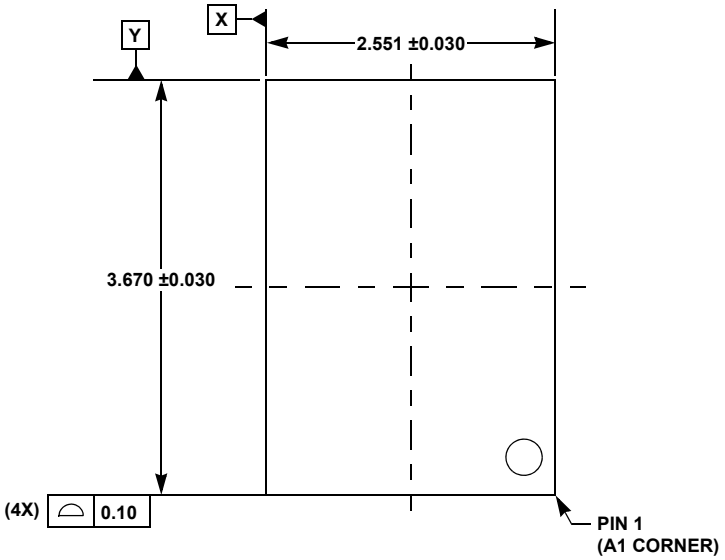
11. Revision History

Rev.	Date	Description
2.0	Feb 20, 2020	Added note 1 to Ordering Information table. Updated Figures 3 and 4 Typical Applications Updated Pin Configuration and Pin Description table Added Note 10 to Electrical Spec table Updated Output Configurations Table 9 I2C Timing - removed Min values from rise time SCL, fall time SCL, Rise time SDA and Fall time SDA for fast mode, fast mode plus and high speed mode. Added note to Register Address Map table. Register Map and Register Description tables: Changed BUCK4_RSPCFG1 to BUCK4_RSPCFG0 and changed BUCK4_RSPCFG0 to BUCK4_RSPCFG1.
1.00	May 10, 2019	On page 1, updated 1st bullet in Features and updated Applications section. I/O Pin Configuration section table page 8, Descriptions for IO_PINMODE 0x2 and 0x4 updated: 0x2 from: All PGOODs on pins to: I^2C with individual PGOOD outputs for Bucks1-3 0x4 from: I^2C with Global DVS mode with PGOOD1 and PGOOD2 to: I^2C with Global DVS mode and PGOOD1 ESD Ratings on page 9 - Changed HBM from 2kV to 2.5kV, and changed CDM from 750V to 1kV. 5.1 Inductor Selection section updated 5.7.1 Buck Start-Up from Master Chip Enable Pin (EN) section updated 5.7.2 Buck Power-Down from Master Chip Enable Pin (EN) section updated. Figure 38 updated Register Address Map - Added: 0x23 IO_SPICFG Changed: 0x5C BUCK2_CFG3 to: 0x5B BUCK2_DCM 0x62 BUCK2_DVS0CFG1 to: 0x5D BUCK2_CFG2 0x72 BUCK3_EA2 to: 0x75 BUCK3_DCM 0x90 BUCK4_CFG3 to: 0x8F BUCK4_DCM Removed 0xA5 BUCK2_CFG3 Register Description by Address - Added: 0x23 IO_SPICFG Updated: BUCK1_DVS0VOUT92 Description, removed 0x1FF row Changed: BUCK1_EA2 section to BUCK1_DCM, and updated contents Changed: BUCK4_EA2 section to BUCK2_DCM and updated contents Changed: BUCK2_DVS0CFG0 section to BUCK2_CFG2 and updated contents Changed: BUCK4_EA2 section to BUCK3_DCM and updated contents Changed: BUCK1_EA2 section to BUCK4_DCM and updated contents Updated: BUCK1_RSPUP/BUCKx_RSPDN description Updated: BUCK1_RSPPUP/BUCK1_RSPPDN description Updated: Buck2_CFG2 - updated name from: BUCK2_CFG2RSVD to: BUCK2_CFG2RSVD. Updated Description Updated disclaimer
0.00	Jul 2, 2018	Initial release

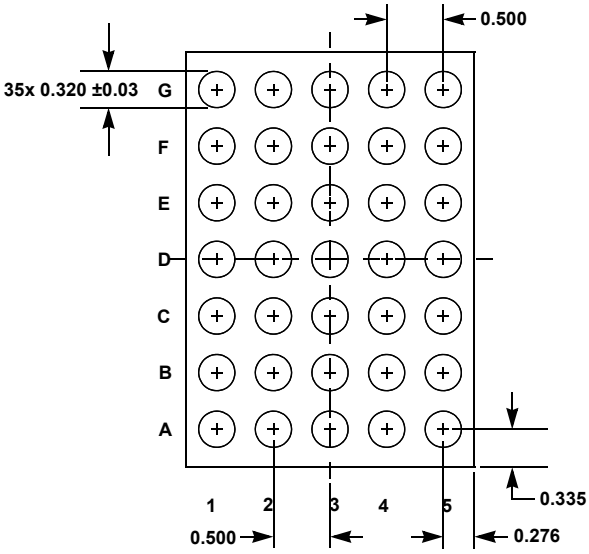
12. Package Outline Drawing

For the most recent package outline drawing, see W5x7.35C.

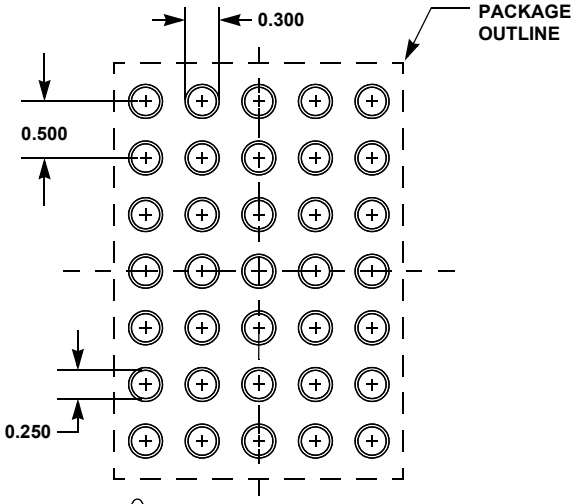
W5x7.35C
35 Ball Wafer Level Chip Scale Package (WLCSP 0.5mm Pitch)
Rev 0, 12/16



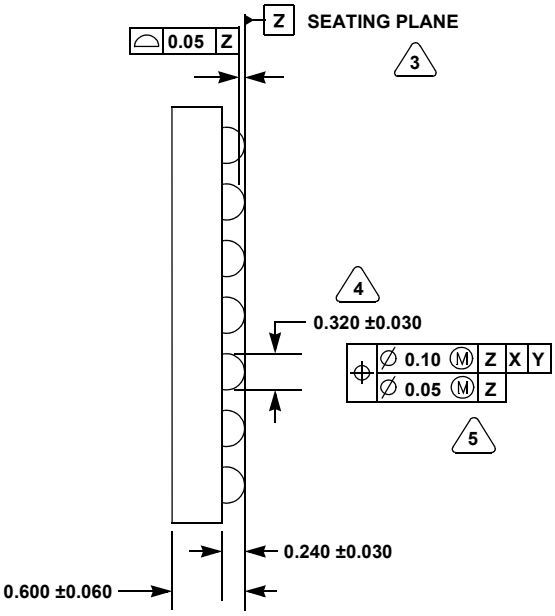
TOP VIEW



BOTTOM VIEW



RECOMMENDED LAND PATTERN



SIDE VIEW

NOTES:
1. All dimensions are in millimeters.
2. Dimensions and tolerance per ASME Y14.5 - 1994.
3. Primary datum Z and seating plane are defined by the spherical crowns of the bump.
4. Dimension is measured at the maximum bump diameter parallel to primary datum Z.
5. Bump position designation per JESD 95-1, SPP-010.
6. NSMD refers to non-solder mask defined pad design per TB451.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

© 2020 Renesas Electronics Corporation. All rights reserved.