KGF20N05D

N-Channel 5.5V Dual Power MOSFET

FN8963
Rev.0.00
Feb 1, 2018

The KGF20N05D is a dual 5.5V, 1.6mΩ, chip-scale, N-channel power MOSFET. The device uses technology that uniquely integrates low cost CMOS and WLCSP fabrication processes. The chip-scale package offers small area, low vertical profile, and is fully compatible with standard SMT assembly processes. The KGF20N05D offers unprecedented low ON-resistance and total gate charge, outperforming conventional trench MOSFETs and enabling high frequency, low voltage switching. The device offers extremely high power density, reducing the board size of DC/DC converters and other power management systems.

Features

- Industry leading figures of merit: $r_{DS(ON)} \times Q_g$ and $r_{DS(ON)} \times Q_{gd}$
- Low profile/small footprint chip-scale WLCSP package
- High frequency switching
- Known Good FET (KGF) quality assurance process
- Low thermal resistance

Applications

- Point-of-load DC/DC converters
- Portable electronics
- OR'ing diodes

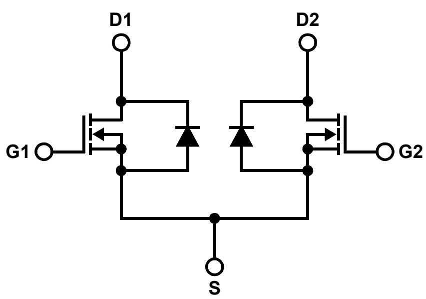


Figure 1. Equivalent Circuit

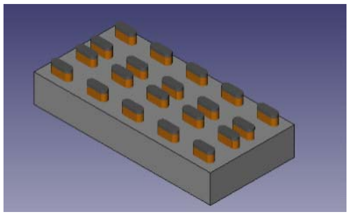


Figure 2. WLCSP, Die Size 2.475mmx1.170mm

1. Overview

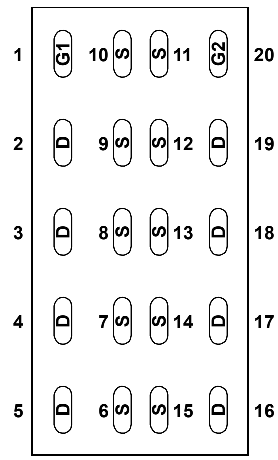
1.1 Ordering Information

Part Number (Notes 1, 2, 3)	Part Marking	Temp Range (°C)	Tape and Reel (Units)	Package (RoHS Compliant)
KGF20N05D	AO	-55°C to +150°C	4k	20 Bump WLCSP

Notes:
1. Refer to TB347 for details about reel specifications.
2. For more information about MSL, refer to TB363.
3. The part marking is located on the bottom of the part.

1.2 Pin Configuration

KGF20N05D
(20 Bump WLCSP)
Bottom View



1.3 Pin Descriptions

Pin Number	Pin Name	Description
1	G1	MOSFET 1 gate
2, 3, 4, 5	D1	MOSFET 1 drain
6, 7, 8, 9, 10, 11, 12, 13, 14, 15	S	Source of both MOSFETs
16, 17, 18, 19	D2	MOSFET 2 drain
20	G2	MOSFET 2 gate

2. Specifications

2.1 Absolute Maximum Ratings

T_J = +25°C unless otherwise noted.

Parameter	Minimum	Maximum	Unit
Drain-to-Source Voltage (V_{DS})		5.5	V
Gate-to-Source Voltage (V_{GS})		±5.5	V
Drain Current (I_{D1} + I_{D2})			
Continuous (I_D)		20	A
Pulsed (I_{DM})		40	A
Single Pulse Avalanche Current (I_{AS}), (I_{D1} + I_{D2})			
L ≤ 50µH, R_G ≤ 25Ω		10	A

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

2.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
WLCSP Package (Note 4)	50	10

Note:
4. When mounted on 1 inch square 2oz copper clad FR-4.

Parameter	Minimum	Maximum	Unit
Maximum Power Dissipation (P_D) (Note 4)			
T_A = +25°C		2.5	W
T_A = +70°C		1.6	W
Junction and Storage Temperature Range (T_J, T_{stg})	-55	+150	°C
Pb-Free Reflow Profile	Refer to TB493		

2.3 Electrical Specifications

Specifications are for single MOSFET unless otherwise specified. T_J = +25°C unless otherwise noted

Parameter	Symbol	Test Condition	Min (Note 5)	Typ	Max (Note 5)	Units
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 5mA	5.5			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 4V, V_{GS} = 0V, T_J = +25°C			0.01	mA
		V_{DS} = 5V, V_{GS} = 0V, T_J = +25°C			0.1	mA
		V_{DS} = 5V, V_{GS} = 0V, T_J = +125°C			1	mA
Gate-Body Leakage	I_{GSS}	V_{GS} = 5.5V, V_{DS} = 0V			75	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250µA	0.55	0.73	0.90	V
Drain-to-Source On-State Resistance (per MOSFET)	$r_{DS(ON)}$	V_{GS} = 3.5 V, I_D = 10A		1.70		mΩ
		V_{GS} = 4.5V, I_D = 10A		1.60		mΩ
Drain-to-Source On-State Resistance (in Parallel)	$r_{DS(ON)}$	V_{GS} = 3.5V, I_D = 10A		0.85		mΩ
		V_{GS} = 4.5V, I_D = 10A		0.80		mΩ
Input Capacitance	C_{iss}	V_{DS} = 5V, V_{GS} = 0V, f = 1MHz		865		pF
Output Capacitance	C_{oss}			270		pF
Reverse Transfer Capacitance	C_{rss}			1100		pF
Input Capacitance	C_{iss}	V_{DS} = 0V, V_{GS} = 0V, f = 1MHz		890		pF
Output Capacitance	C_{oss}			295		pF
Reverse Transfer Capacitance	C_{rss}			1390		pF
Gate Resistance	R_g	V_{DS} = 0V, f = 1MHz		1.2		Ω
Total Gate Charge	Q_g	V_{GS} = 3.5V, I_D = 4A, V_{DS} = 4V		5.3		nC
Gate-to-Source Charge	Q_{gs}			1.1		nC
Gate-to-Drain Charge	Q_{gd}			1.3		nC
Total Gate Charge	Q_g	V_{GS} = 4.5V, I_D = 4A, V_{DS} = 4V		6.7		nC
Source-to-Drain Reverse Recovery Time	t_{rr}	I_S = 10A, di/dt = 33A/µs		69		ns
Diode Forward Voltage	V_{SD}	I_S = 10A, V_{GS} = 0V		0.7	1.0	V

Note:
5. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.

3. Typical Performance Curves

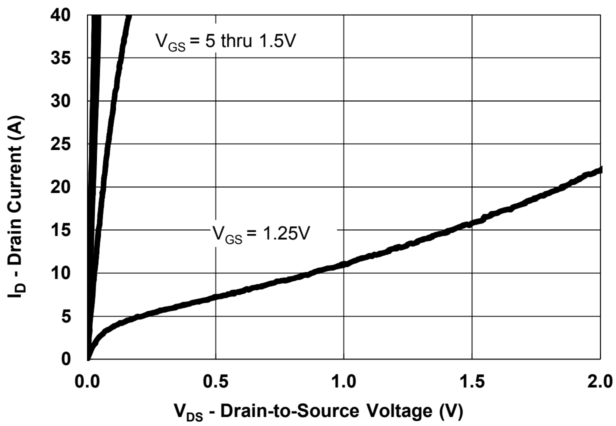


Figure 3. Output Characteristics

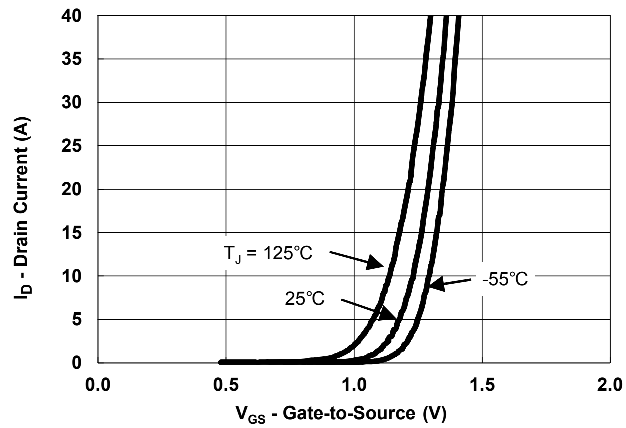


Figure 4. Transfer Characteristics

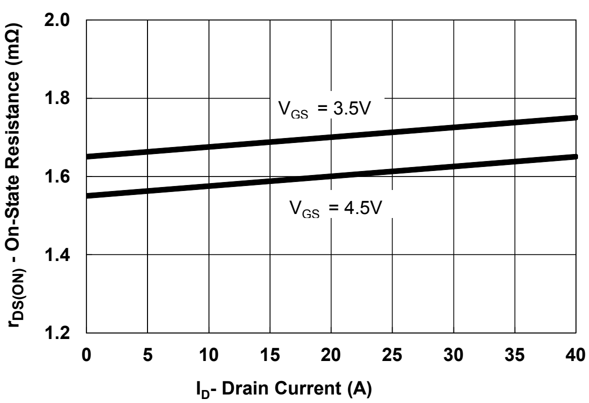


Figure 5. Drain-to-Source On-State Resistance vs Drain Current

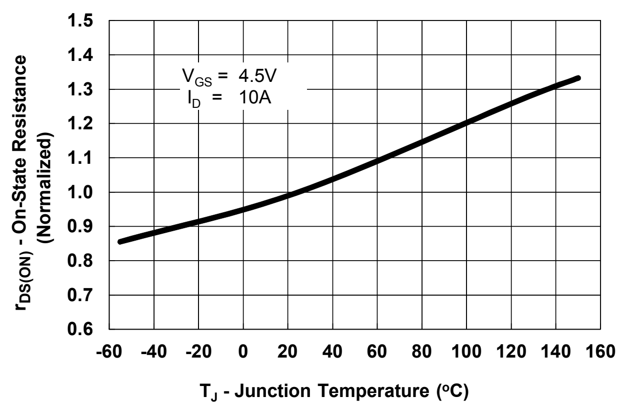


Figure 6. Drain-to-Source On-State Resistance vs Junction Temperature

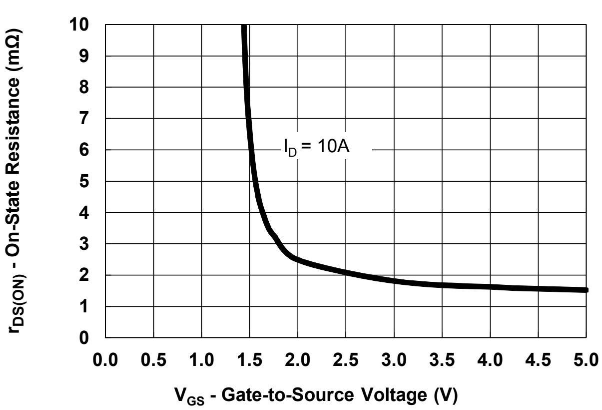


Figure 7. Drain-to-Source On-State Resistance vs Gate-to-Source Voltage

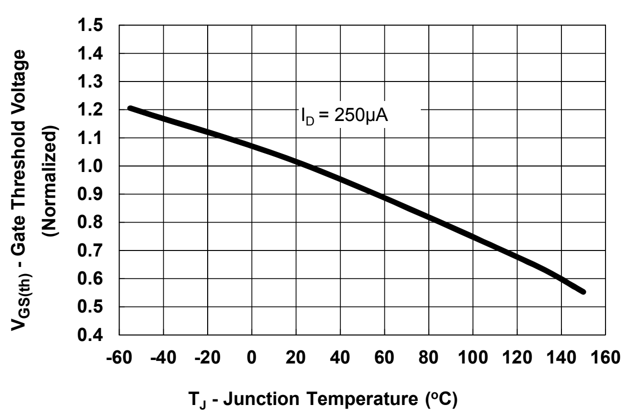


Figure 8. Gate Threshold Voltage vs Junction Temperature

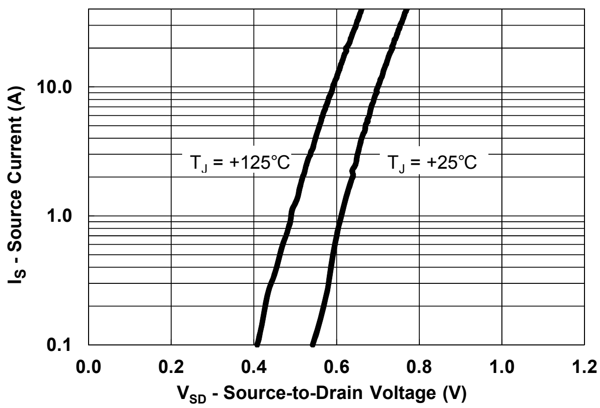


Figure 9. Source-to-Drain Diode Forward Voltage

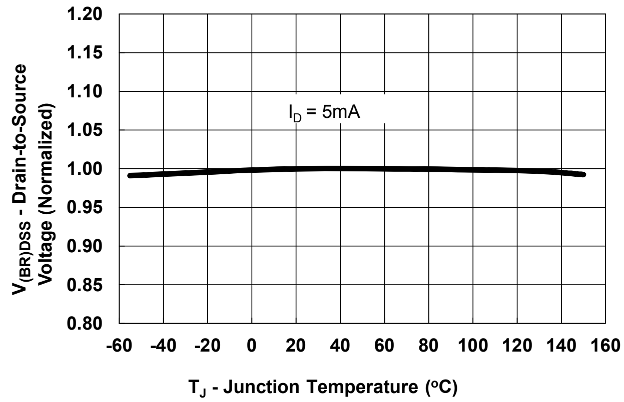


Figure 10. Drain-to-Source Breakdown Voltage vs Junction Temperature

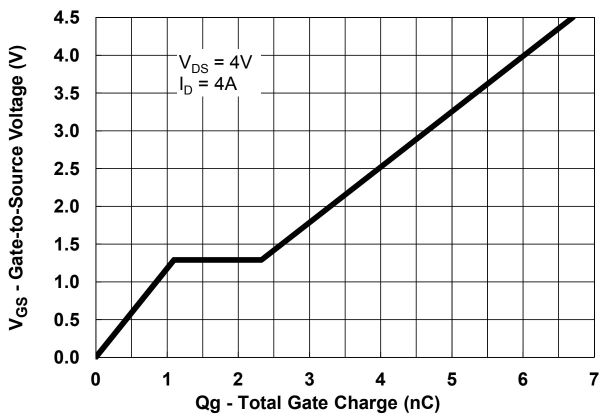


Figure 11. Gate Charge

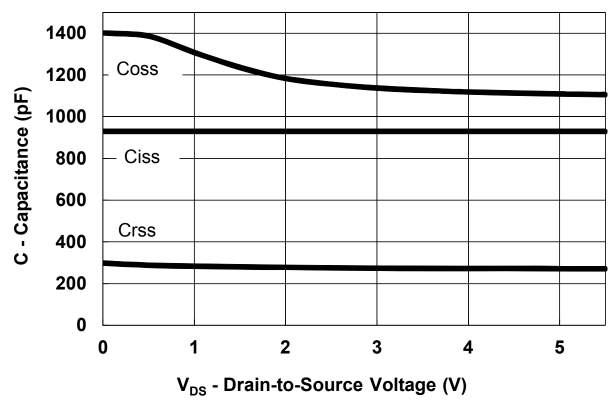


Figure 12. Capacitance

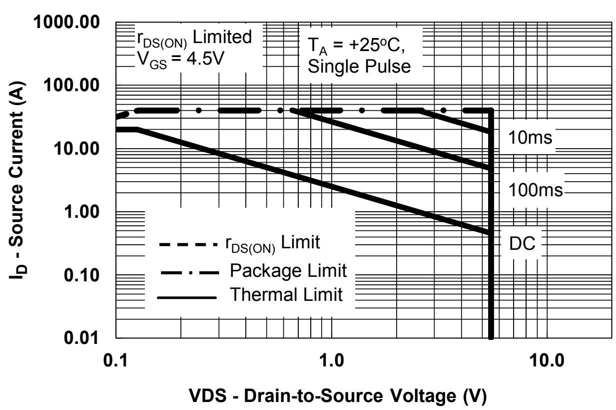


Figure 13. Maximum Rated Forward Biased Safe Operating Area (in Parallel)

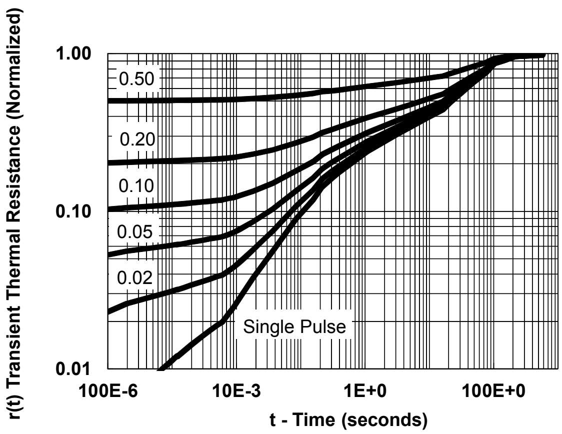


Figure 14. Transient Thermal Response, Junction-to-Ambient (in Parallel)

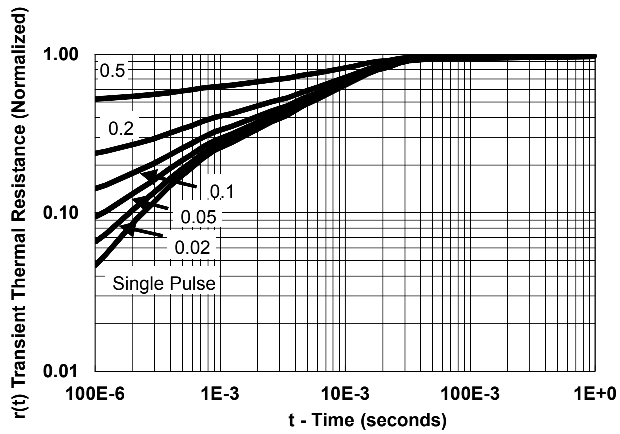


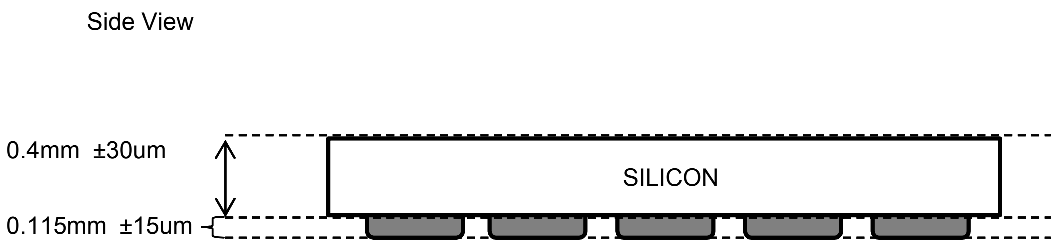
Figure 15. Transient Thermal Response, Junction-to-Ball

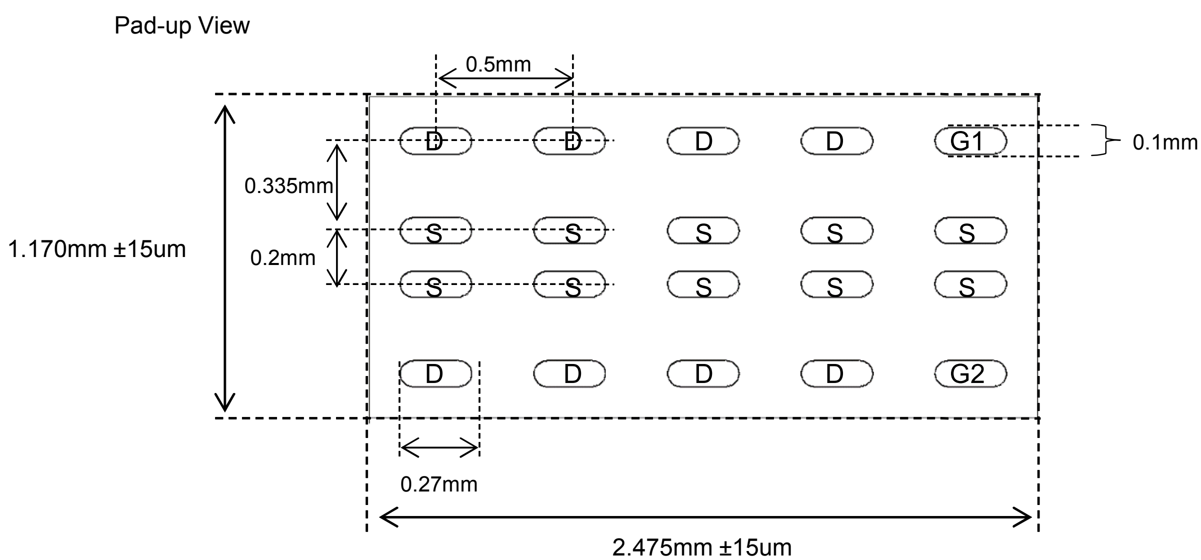
4. Revision History

Rev.	Date	Description
0.00	Feb 1, 2018	Initial release.

5. Package Outline Drawing

Dimensional Outline and Pad Layout





Renesas Electronics Corporation

SALES OFFICES

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Renesas Electronics America Inc.
1001 Murphy Ranch Road, Milpitas, CA 95035, U.S.A.
Tel: +1-408-432-8888, Fax: +1-408-434-5351

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709 Quantum Plaza, No.27 ZhichunLu, Haidian District, Beijing, 100191 P. R. China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, 200333 P. R. China
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
17F, KAMCO Yangjae Tower, 262, Gangnam-daero, Gangnam-gu, Seoul, 06265 Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5338