

# KGF20N05D

N-Channel 5.5V Dual Power MOSFET

FN8963  
Rev.0.00  
Feb 1, 2018

The KGF20N05D is a dual 5.5V, 1.6mΩ, chip-scale, N-channel power MOSFET. The device uses technology that uniquely integrates low cost CMOS and WLCSP fabrication processes. The chip-scale package offers small area, low vertical profile, and is fully compatible with standard SMT assembly processes. The KGF20N05D offers unprecedented low ON-resistance and total gate charge, outperforming conventional trench MOSFETs and enabling high frequency, low voltage switching. The device offers extremely high power density, reducing the board size of DC/DC converters and other power management systems.

## Features

- Industry leading figures of merit:  
 $r_{DS(ON)} \times Q_g$  and  $r_{DS(ON)} \times Q_{gd}$
- Low profile/small footprint chip-scale WLCSP package
- High frequency switching
- Known Good FET (KGF) quality assurance process
- Low thermal resistance

## Applications

- Point-of-load DC/DC converters
- Portable electronics
- OR'ing diodes

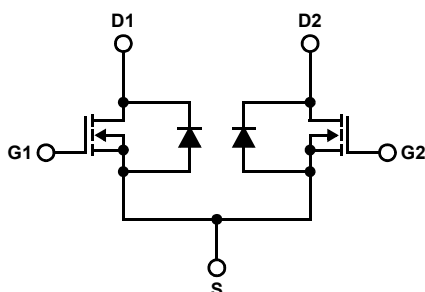


Figure 1. Equivalent Circuit

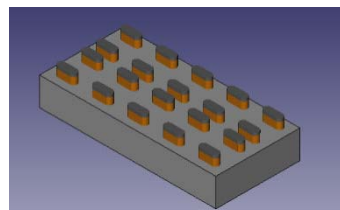


Figure 2. WLCSP, Die Size 2.475mmx1.170mm



## 2. Specifications

### 2.1 Absolute Maximum Ratings

$T_J = +25^{\circ}\text{C}$  unless otherwise noted.

Parameter	Minimum	Maximum	Unit
Drain-to-Source Voltage ( $V_{DS}$ )		5.5	V
Gate-to-Source Voltage ( $V_{GS}$ )		$\pm 5.5$	V
<b>Drain Current (<math>I_{D1} + I_{D2}</math>)</b>			
Continuous ( $I_D$ )		20	A
Pulsed ( $I_{DM}$ )		40	A
<b>Single Pulse Avalanche Current (<math>I_{AS}</math>), (<math>I_{D1} + I_{D2}</math>)</b>			
$L \leq 50\mu\text{H}$ , $R_G \leq 25\Omega$		10	A

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

### 2.2 Thermal Information

Thermal Resistance (Typical)	$\theta_{JA}$ ( $^{\circ}\text{C/W}$ )	$\theta_{JC}$ ( $^{\circ}\text{C/W}$ )
WLCSP Package ( <a href="#">Note 4</a> )	50	10

Note:

- When mounted on 1 inch square 2oz copper clad FR-4.

Parameter	Minimum	Maximum	Unit
<b>Maximum Power Dissipation (<math>P_D</math>) (<a href="#">Note 4</a>)</b>			
$T_A = +25^{\circ}\text{C}$		2.5	W
$T_A = +70^{\circ}\text{C}$		1.6	W
Junction and Storage Temperature Range ( $T_J$ , $T_{stg}$ )	-55	+150	$^{\circ}\text{C}$
Pb-Free Reflow Profile	Refer to <a href="#">TB493</a>		

## 2.3 Electrical Specifications

Specifications are for single MOSFET unless otherwise specified.  $T_J = +25^\circ\text{C}$  unless otherwise noted

Parameter	Symbol	Test Condition	Min ( <a href="#">Note 5</a> )	Typ	Max ( <a href="#">Note 5</a> )	Units
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 5\text{ mA}$	5.5			V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 4\text{ V}, V_{GS} = 0\text{ V}, T_J = +25^\circ\text{C}$			0.01	mA
		$V_{DS} = 5\text{ V}, V_{GS} = 0\text{ V}, T_J = +25^\circ\text{C}$			0.1	mA
		$V_{DS} = 5\text{ V}, V_{GS} = 0\text{ V}, T_J = +125^\circ\text{C}$			1	mA
Gate-Body Leakage	$I_{GSS}$	$V_{GS} = 5.5\text{ V}, V_{DS} = 0\text{ V}$			75	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	0.55	0.73	0.90	V
Drain-to-Source On-State Resistance (per MOSFET)	$r_{DS(ON)}$	$V_{GS} = 3.5\text{ V}, I_D = 10\text{ A}$		1.70		mΩ
		$V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$		1.60		mΩ
Drain-to-Source On-State Resistance (in Parallel)	$r_{DS(ON)}$	$V_{GS} = 3.5\text{ V}, I_D = 10\text{ A}$		0.85		mΩ
		$V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$		0.80		mΩ
Input Capacitance	$C_{iss}$	$V_{DS} = 5\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		865		pF
Output Capacitance	$C_{oss}$			270		pF
Reverse Transfer Capacitance	$C_{rss}$			1100		pF
Input Capacitance	$C_{iss}$	$V_{DS} = 0\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		890		pF
Output Capacitance	$C_{oss}$			295		pF
Reverse Transfer Capacitance	$C_{rss}$			1390		pF
Gate Resistance	$R_g$	$V_{DS} = 0\text{ V}, f = 1\text{ MHz}$		1.2		Ω
Total Gate Charge	$Q_g$	$V_{GS} = 3.5\text{ V}, I_D = 4\text{ A}, V_{DS} = 4\text{ V}$		5.3		nC
Gate-to-Source Charge	$Q_{gs}$			1.1		nC
Gate-to-Drain Charge	$Q_{gd}$			1.3		nC
Total Gate Charge	$Q_g$	$V_{GS} = 4.5\text{ V}, I_D = 4\text{ A}, V_{DS} = 4\text{ V}$		6.7		nC
Source-to-Drain Reverse Recovery Time	$t_{rr}$	$I_S = 10\text{ A}, di/dt = 33\text{ A}/\mu\text{s}$		69		ns
Diode Forward Voltage	$V_{SD}$	$I_S = 10\text{ A}, V_{GS} = 0\text{ V}$		0.7	1.0	V

Note:

5. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.

### 3. Typical Performance Curves

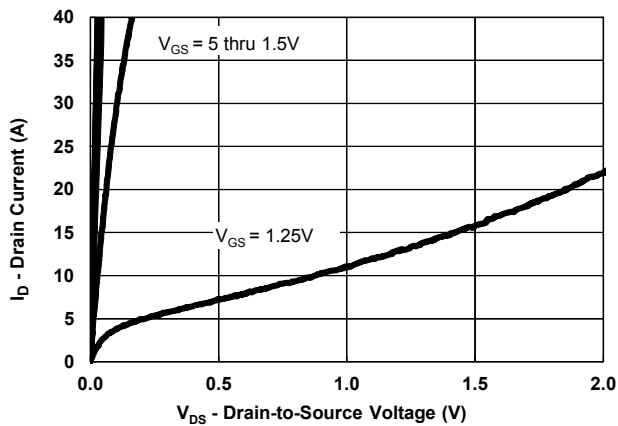


Figure 3. Output Characteristics

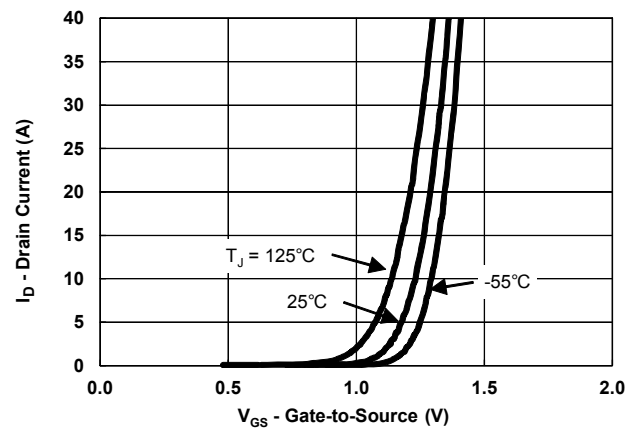


Figure 4. Transfer Characteristics

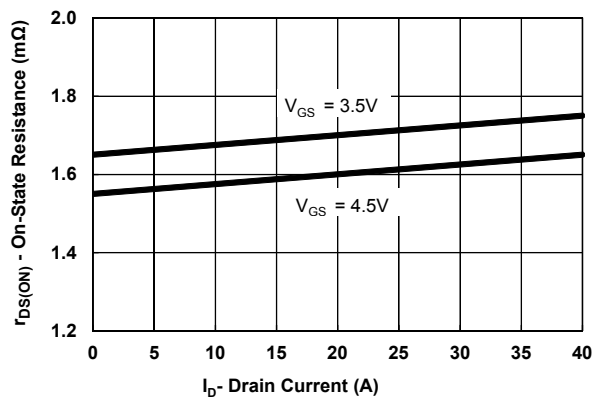


Figure 5. Drain-to-Source On-State Resistance vs Drain Current

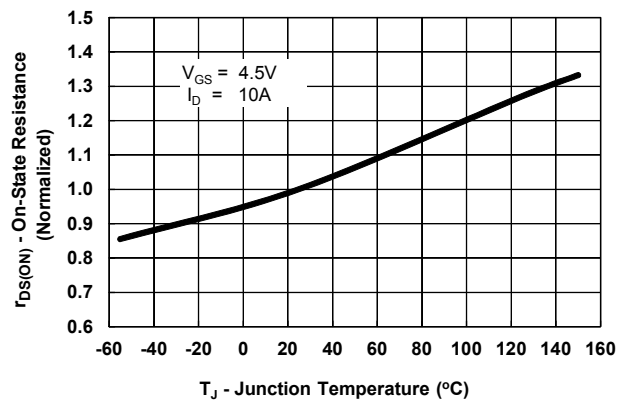


Figure 6. Drain-to-Source On-State Resistance vs Junction Temperature

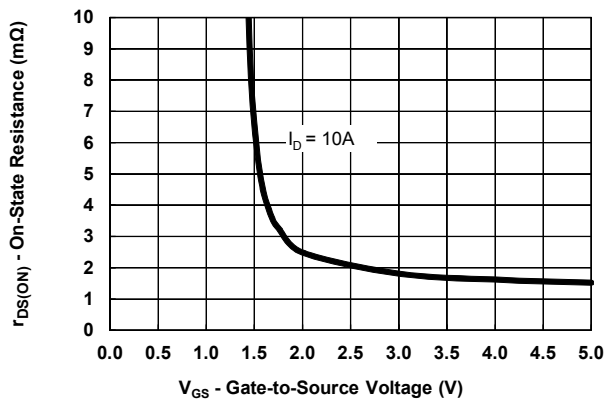


Figure 7. Drain-to-Source On-State Resistance vs Gate-to-Source Voltage

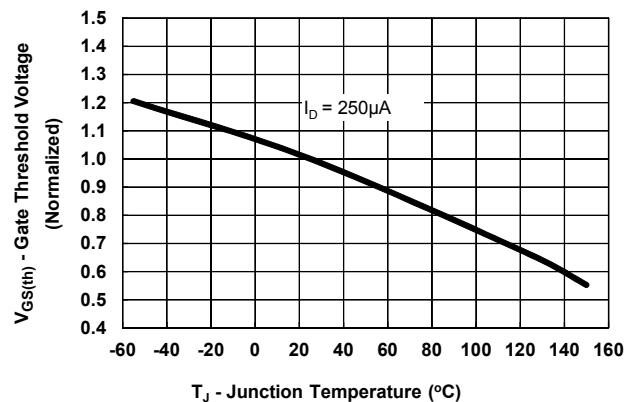


Figure 8. Gate Threshold Voltage vs Junction Temperature

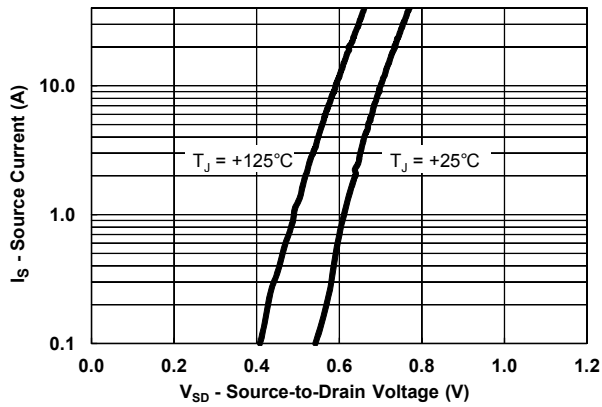


Figure 9. Source-to-Drain Diode Forward Voltage

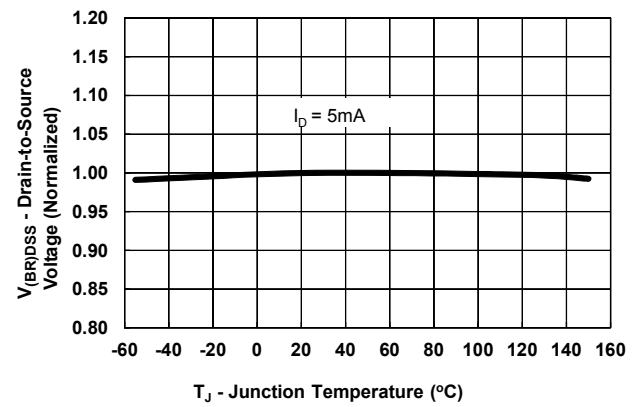


Figure 10. Drain-to-Source Breakdown Voltage vs Junction Temperature

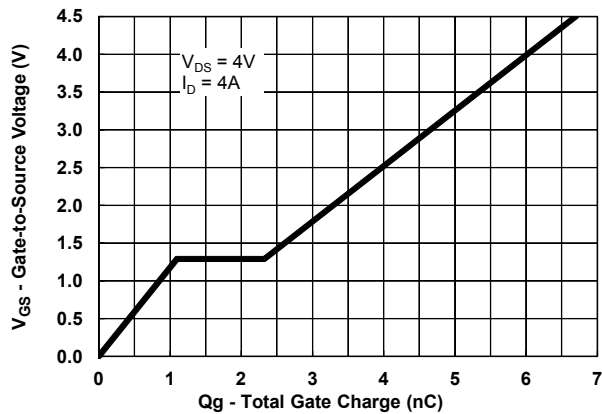


Figure 11. Gate Charge

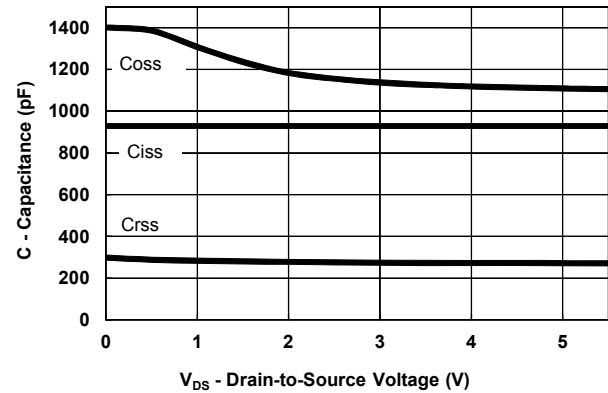


Figure 12. Capacitance

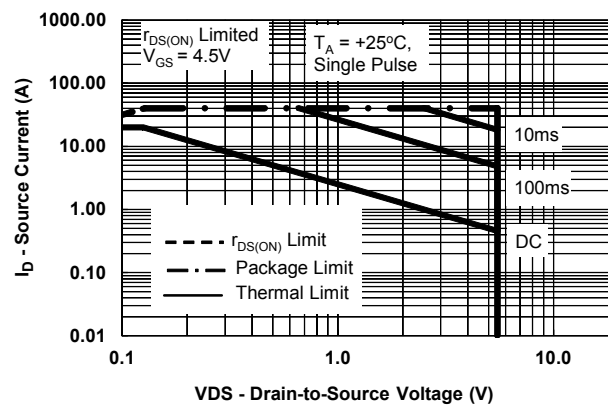


Figure 13. Maximum Rated Forward Biased Safe Operating Area (in Parallel)

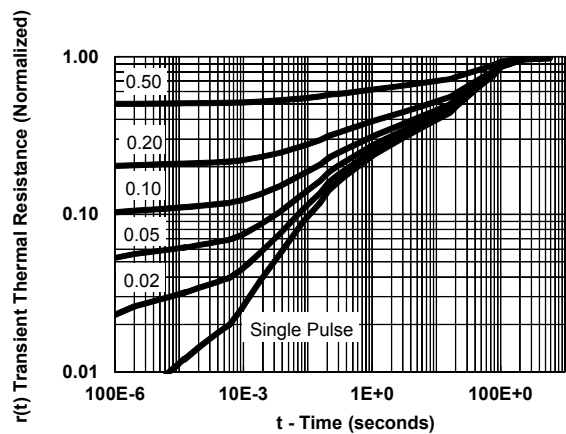


Figure 14. Transient Thermal Response, Junction-to-Ambient (in Parallel)

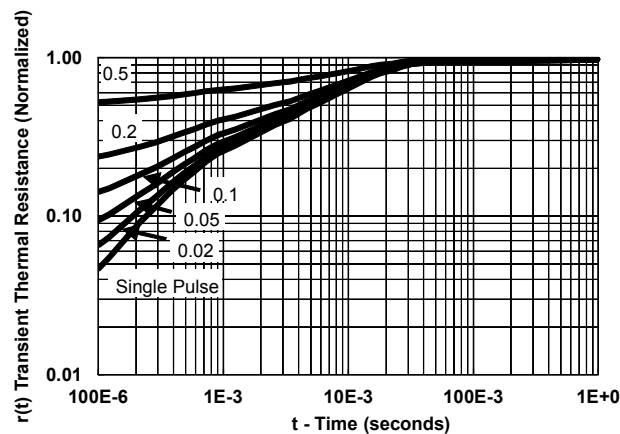


Figure 15. Transient Thermal Response, Junction-to-Ball

## 4. Revision History

Rev.	Date	Description
0.00	Feb 1, 2018	Initial release.

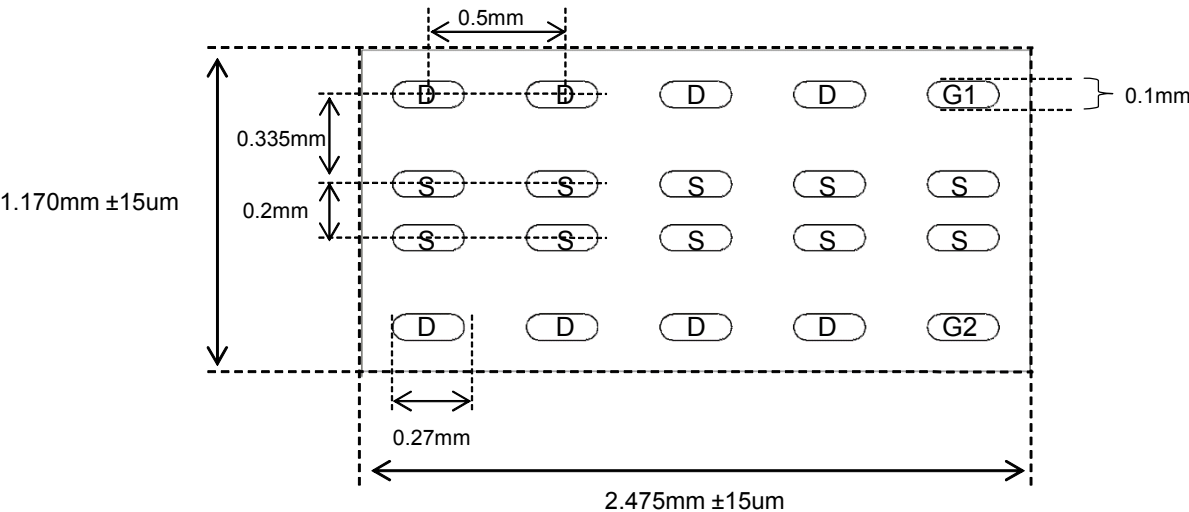
5. Package Outline Drawing

Dimensional Outline and Pad Layout

Side View



Pad-up View



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