LOW DRIVE 3.3 VOLT VCXO

MK3727H

Description

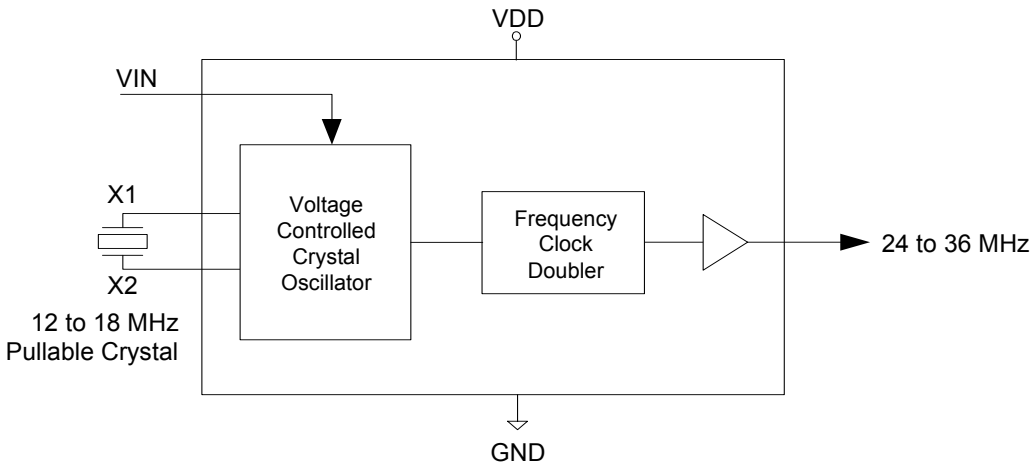
The MK3727H is a low drive, low cost, single output 3.3 Volt VCXO and PLL clock synthesizers designed to replace expensive VCXOs and crystals. The patented on-chip Voltage Controlled Crystal Oscillator accepts a 0 to 3.3 V input voltage to cause the output clocks to vary by ±115 ppm minimum. Using our analog Phase Locked Loop (PLL) techniques, the devices uses an external, fundamental mode 13.5 MHz pullable crystal input to produce output clocks of 27 MHz. The drive parameters are optimized for low EMI.

The frequency of the on-chip VCXO is adjusted by an external control voltage input into pin VIN. Because VIN is a high-impedance input, it can be driven directly from an PWM RC integrator circuit.

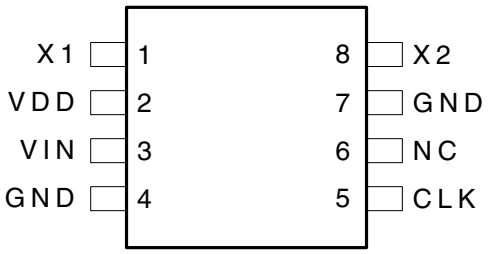
Features

- Packaged in 8-pin SOIC
- Operating voltage of 3.3 V (±5%)
- Single pullable output clock of 24 to 36 MHz
- Uses a fundamental mode 12 to 18 MHz pullable crystal
- On-chip patented VCXO with pull range of 230 ppm (minimum)
- VCXO tuning voltage of 0 to 3.3 V
- Low-drive output stage to reduce EMI
- Advanced, low-power, sub-micron CMOS process
- RoHS 5 (green) or RoHS 6 (green and lead free) compliant package

Block Diagram



Pin Assignment



8 Pin (150 mil) SOIC

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	X1	Input	Crystal connection. Connect to a 12 to 18 MHz external pullable crystal.
2	VDD	Power	Connect to +3.3 V.
3	VIN	Input	Voltage input to VCXO. 0 to 3.3 V analog input which controls the oscillation frequency of the VCXO.
4	GND	Input	Connect to ground.
5	CLK	Output	VCXO clock output; 2x input frequency.
6	NC	—	No connect. Do not connect to anything.
7	GND	Input	Connect to ground.
8	X2	Output	Crystal connection. Connect to a 12 to 18 MHz external pullable crystal.

External Component Selection

The MK3727H requires a minimum number of external components for proper operation.

Decoupling Capacitor

A decoupling capacitor of 0.01µF must be connected between VDD (pin 2) and GND (pin 4 & 7), as close to these pins as possible. For optimum device performance, the decoupling capacitor should be mounted on the component side of the PCB. Avoid the use of vias in the decoupling circuit.

Series Termination Resistor

Use series termination when the PCB trace between the clock outputs and the loads are over 1 inch. To series terminate a 50Ω trace (a commonly used trace impedance), place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω

Quartz Crystal

The MK3727H VCXO function consists of the external crystal and the integrated VCXO oscillator circuit. To assure the best system performance (frequency pull range) and reliability, a crystal device with the recommended parameters (as described in application note MAN05) must be used, and the layout guidelines discussed in the following section must be followed.

The frequency of oscillation of a quartz crystal is determined by its “cut” and by the load capacitors connected to it. The MK3727H incorporates on-chip variable load capacitors that “pull” (change) the frequency of the crystal. The crystal specified for use with the MK3727H is designed to have zero frequency error when the total of on-chip + stray capacitance is
14 pF.

The external crystal must be connected as close to the chip as possible and should be on the same side of the PCB as the MK3727H. There should be no vias between the crystal pins and the X1 and X2 device pins. There should be no signal traces underneath or close to the crystal.

Crystal Tuning Load Capacitors

The crystal traces should include pads for small fixed capacitors, one between X1 and ground, and another between X2 and ground. Stuffing of these capacitors on the PCB is optional. The need for these capacitors is determined at system prototype evaluation, and is influenced by the particular crystal used (manufacture and frequency) and by PCB layout. The typical required capacitor value is 1 to 4 pF.

To determine the need for and value of the crystal adjustment capacitors, you will need a PC board of your final layout, a frequency counter capable of about 1 ppm resolution and accuracy, two power supplies, and some samples of the crystals which you plan to use in production, along with measured initial accuracy for each crystal at the specified crystal load capacitance, CL.

To determine the value of the crystal capacitors:

1. Connect VDD of the MK3727H to 3.3 V. Connect pin 3 of the MK3727H to the second power supply. Adjust the voltage on pin 3 to 0V. Measure and record the frequency of the CLK output.

2. Adjust the voltage on pin 3 to 3.3 V. Measure and record the frequency of the same output.

To calculate the centering error:

$$Error = 10^6 x\left[\frac{(f_{3.0V} - f_{target}) + (f_{0V} - f_{target})}{f_{target}}\right] - error_{xtal}$$

Where:

f_{target} = nominal crystal frequency

$error_{xtal}$ =actual initial accuracy (in ppm) of the crystal being measured

If the centering error is less than ±25 ppm, no adjustment is needed. If the centering error is more than 25 ppm negative, the PC board has excessive stray capacitance and a new PCB layout should be considered to reduce stray capacitance. (Alternately, the crystal may be re-specified to a higher load capacitance. Contact IDT for details.) If the centering error is more than 25 ppm positive, add identical

fixed centering capacitors from each crystal pin to ground. The value for each of these caps (in pF) is given by:

External Capacitor =

2 x (centering error)/(trim sensitivity)

Trim sensitivity is a parameter which can be supplied by your crystal vendor. If you do not know the value, assume it is 30 ppm/pF. After any changes, repeat the measurement to verify that the remaining error is acceptably low (typically less than ±25 ppm).

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the MK3727H. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature	0 to +70° C
Storage Temperature	-65 to +150° C
Soldering Temperature	260° C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	0		+70	° C
Power Supply Voltage (measured in respect to GND)	+3.13		+3.46	V
Reference crystal parameters	Refer to MAN05			

DC Electrical Characteristics

VDD=3.3 V ±5% , Ambient temperature 0 to +70° C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.13		3.46	V
Output High Voltage	V_{OH}	I_{OH} = -8 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 8 mA			0.5	V
Output High Voltage (CMOS Level)	V_{OH}	I_{OH} = -4 mA	VDD-0.4			V
Operating Supply Current	IDD	No load		10		mA
Short Circuit Current	I_{OS}			±25		mA
VIN, VCXO Control Voltage	V_{IA}		0		3.3	V
Nominal output impedance	Z_{OUT}			20		Ω

AC Electrical Characteristics

VDD = 3.3 V ±5%, Ambient Temperature 0 to +70° C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Crystal Pullability	F_P	0V≤ VIN ≤ 3.3 V, Note 1	± 115			ppm
VCXO Gain		VIN = VDD/2 ± 1 V, Note 1		120		ppm/V
Output Rise Time	t_{OR}	0.3 to 3.0 V, C_L=10 pF		3.0		ns
Output Fall Time	t_{OF}	3.0 to 0.3 V, C_L=10 pF		3.0		ns
Output Clock Duty Cycle	t_D	Measured at VDD/2, C_L=10 pF	45		55	%
Maximum Output Jitter, short term	t_J	C_L=10 pF		±100		ps

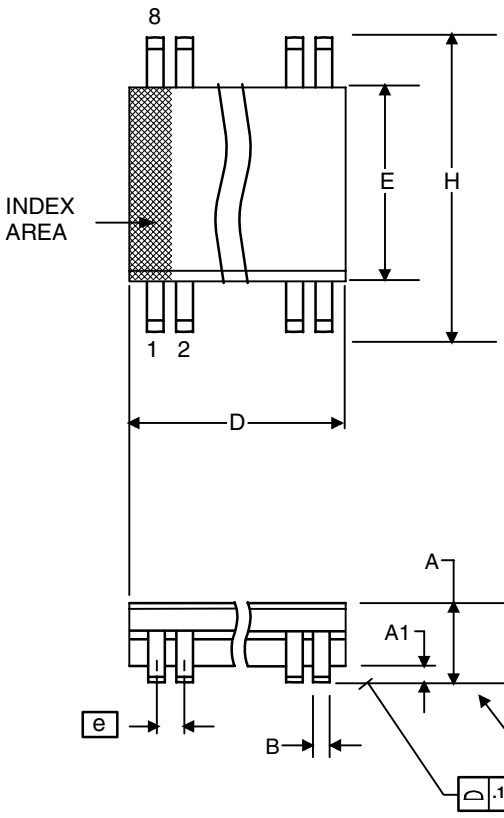
Note 1: External crystal device must conform with Pullable Crystal Specifications listed in MAN05.

Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		150		°C/W
	θ_{JA}	1 m/s air flow		140		°C/W
	θ_{JA}	3 m/s air flow		120		°C/W
Thermal Resistance Junction to Case	θ_{JC}			40		°C/W

Package Outline and Package Dimensions (8-pin SOIC, 150 Mil. Narrow Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches	
Symbol	Min	Max	Min	Max
A	1.35	1.75	.0532	.0688
A1	0.10	0.25	.0040	.0098
B	0.33	0.51	.013	.020
C	0.19	0.25	.0075	.0098
D	4.80	5.00	.1890	.1968
E	3.80	4.00	.1497	.1574
e	1.27 BASIC		0.050 BASIC	
H	5.80	6.20	.2284	.2440
h	0.25	0.50	.010	.020
L	0.40	1.27	.016	.050
α	0°	8°	0°	8°

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
MK3727HLF	3727HLF	Tubes	8-pin SOIC	0 to +70° C
MK3727HLFTR	3727HLF	Tape and Reel	8-pin SOIC	0 to +70° C

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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