LOW EMI CLOCK GENERATOR

MK5814C

Description

The MK5814C device generates a low EMI output clock from a clock or crystal input. The device is designed to dither a high emissions clock to lower EMI in consumer applications. Using IDT's proprietary mix of analog and digital Phase Locked Loop (PLL) technology, the device spreads the frequency spectrum of the output and reduces the frequency amplitude peaks by several dB. The MK5814C offers both centered and down spread from a high-speed clock input. The multiplier is a fixed 4x.

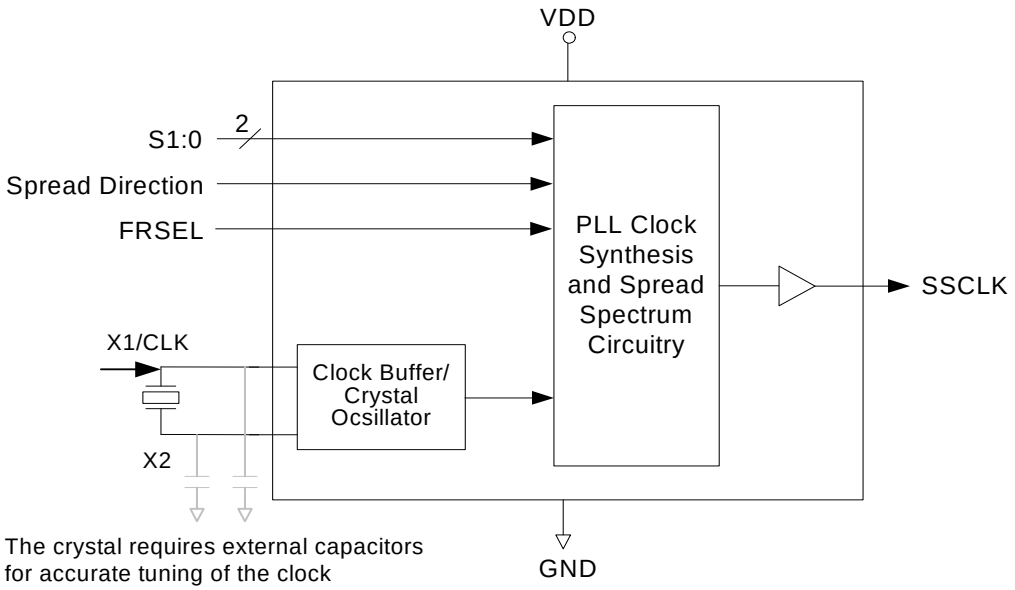
For different multiplier configurations, use the MK5811C (1x) or MK5812 (2x).

IDT offers many other clocks for computers and computer peripherals. Consult IDT when you need to remove crystals and oscillators from your board.

Features

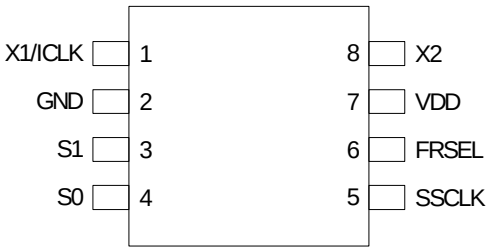
- Packaged in 8-pin SOIC
- Provides a spread spectrum output clock
- Supports printers and flat panel controllers
- Accepts a clock or crystal input (provides same frequency dithered output)
- Input frequency range of 4 to 32 MHz with spread off
- Input frequency range of 4 to 25 MHz with spread on
- 4X frequency multiplication
- Center spread, down spread, and spread off settings
- Peak reduction by 8 dB to 16 dB typical on 3rd through 19th odd harmonics
- Operating voltage of 3.3 V
- Advanced, low-power CMOS process

Block Diagram



The crystal requires external capacitors for accurate tuning of the clock

Pin Assignment



8-pin (150 mil) SOIC

Spread Direction and Spread Percentage

S1 Pin 3	S0 Pin 4	Spread Direction	Spread Percentage
0	0	Center	±1.4
0	M	Center	±1.1
0	1	Center	±0.6
M	0	Center	±0.5
M	M	No Spread	-
M	1	Down	-1.6
1	0	Down	-2.0
1	M	Down	-0.7
1	1	Down	-3.0

0 = connect to GND
M = unconnected (floating)
1 = connect directly to VDD

Frequency Selection

Product	FRSEL (pin 6)	Input Freq. Range	Multiplier	Output Freq. Range
MK5811C[1]	0	4.0 to 8.0 MHz	X1	4.0 to 8.0 MHz
	1	8.0 to 16.0MHz	X1	8.0 to 16.0MHz
	M	16.0 to 32.0MHz	X1	16.0 to 32.0MHz
MK5812[1]	0	4.0 to 8.0 MHz	X2	8.0 to 16.0MHz
	1	8.0 to 16.0MHz	X2	16.0 to 32.0MHz
	M	16.0 to 32.0MHz	X2	32.0 to 64.0MHz
MK5814C	0	4.0 to 8.0 MHz	X4	16.0 to 32.0MHz
	1	8.0 to 16.0MHz	X4	32.0 to 64.0MHz
	M	16.0 to 32.0MHz	X4	64.0 to 128MHz

0 = connect to GND
M = unconnected (floating)
1 = connect directly to VDD

Note 1: The information in this datasheet does not apply to the MK5811C and MK5812 as each have independent datasheets available at www.idt.com.

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	X1/ICLK	Input	Connect to 4-32 MHz crystal or clock input.
2	GND	Power	Connect to ground.
3	S1	Input	Function select 1 input. Selects spread amount and direction per table above. (default-internal mid-level).
4	S0	Input	Function select 0 input. Selects spread amount and direction per table above. (default-internal mid-level).
5	SSCLK	Output	Clock output with Spread spectrum
6	FRSEL	Input	Function select for input frequency range. Default to mid-level “M”.
7	VDD	Power	Connect to +3.3 V.
8	X2	XO	Crystal connection to 4-32 MHz crystal. Leave unconnected for clock

External Components

The MK5814C requires a minimum number of external components for proper operation.

Decoupling Capacitor

A decoupling capacitor of 0.01µF must be connected between VDD and GND on pins 7 and 2. Connect the capacitor as close to these pins as possible. For optimum device performance, mount the decoupling capacitor on the component side of the PCB. Avoid the use of vias in the decoupling circuit.

Series Termination Resistor

Use series termination when the PCB trace between the clock output and the load is over 1 inch. To series terminate a 50Ω trace (a commonly used trace impedance), place a 33Ω resistor in series with the clock line. Place the resistor as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω

Tri-level Select Pin Operation

The S1 and S0 select pins are tri-level, meaning that they have three separate states to make the selections shown in the table on page 2. To select the M (mid) level, the connection to these pins must be eliminated by either floating them originally, or tri-stating the GPIO pins which drive the select pins.

PCB Layout Recommendations

For optimum device performance and lowest output phase noise, observe the following guidelines:

1) Mount the 0.01µF decoupling capacitor on the component side of the board as close to the VDD pin as possible. No vias should be used between the decoupling capacitor and VDD pin. The PCB trace to the VDD pin and the PCB trace to the ground via should be kept as short as possible.

2) To minimize EMI, place the 33Ω series-termination resistor (if needed) close to the clock output.

3) An optimum layout is one with all components on the same side of the board, thus minimizing vias through other signal layers. Other signal traces should be routed away from the MK5814C device. This includes signal traces located underneath the device, or on layers adjacent to the ground plane layer used by the device.

Crystal Information

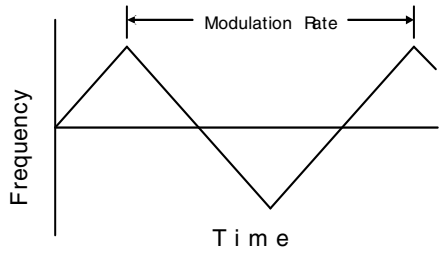
The crystal used should be a fundamental mode (do not use third overtone), parallel resonant crystal. To optimize the initial accuracy, connect crystal capacitors from pins X1 to ground and X2 to ground. The value of these capacitors is given by the following equation:

$$\text{Crystal caps (pF)} = (C_L - 6) \times 2$$

In the equation, C_L is the crystal load capacitance. For example, a crystal with a 16 pF load capacitance uses two 20 pF [(16-6) x 2] capacitors.

Spread Spectrum Profile

The MK5814C is a low EMI clock generator using a optimized frequency slew rate algorithm to facilitate down stream tracking of zero delay buffers and other PLL devices.



Modulation Rate

Spread Spectrum Clock Generators utilize frequency modulation (FM) to distribute energy over a specific band of frequencies. The maximum frequency of the clock (fmax) and minimum frequency of the clock (fmin) determine this band of frequencies. The time required to transition from fmin to fmax and back to fmin is the period of the Modulation Rate. The Modulation Rate of SSCG clocks are generally referred to in terms of frequency, or

fmod = 1/Tmod

The input clock frequency, fin, and the internal divider determine the Modulation Rate.

The Spread Spectrum modulation Rate, fmod, is given by the following formula:

fmod = fin/DR

where; fmod is the Modulation Rate, fin is the Input Frequency and DR is the Divider Ratio as given in the “Modualtion Rate Divider Ratios” table. Notice that Input Frequency Range is set by FRSEL

Modulation Rate Divider Ratios

FRSEL	Input Freq. Range	Divider Ratio (DR)
0	4 to 8 MHz	128
1	8 to 16 MHz	256
M	16 to 32 MHz	512

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the MK5814C. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device, at these or any other conditions, above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature	0 to +85° C
Storage Temperature	-65 to +150° C
Junction Temperature	125° C
Soldering Temperature	260° C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	0		+85	° C
Power Supply Voltage (measured in respect to GND)	+3.0		3.63	V

DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±10%**, Ambient Temperature 0 to +85° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.0	3.3	3.63	V
Supply Current	IDD	No load, at 3.3 V, Fin=12 MHz		23	25	mA
		No load, at 3.3 V, Fin=24 MHz			30	mA
		No load, at 3.3 V, Fin=32 MHz			35	mA
Input High Voltage	V_{IH}		0.85VDD	VDD	VDD	V
Input Middle Voltage	V_{IHM}		0.4VDD	0.5VDD	0.6VDD	V
Input Low Voltage	V_{IL}		0.0	0.0	0.15VDD	V
Output High Voltage	V_{OH}	CMOS, I_{OH} = -4 mA	2.4			V
Output High Voltage	V_{OH}	I_{OH} = -6 mA	2.0			V
Output Low Voltage	V_{OL}	I_{OL} = -4 mA			0.4	V
		I_{OL} = -10 mA			1.2	V
Input Capacitance	C_{IN1}	S0, S1, FRSEL pins		4	6	pF
	C_{IN2}	X1, X2 pins		6	9	pF

AC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±10%**, Ambient Temperature 0 to +85° C, C_L = 15 pF

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Clock Frequency		S1, S0 = ANY VALUE	4	12	25	MHz
Output Clock Frequency		S1, S0 = ANY VALUE	16	48	100	MHz
Input Clock Frequency		S1, S0 = M, M (spread off)	4	12	32	MHz
Output Clock Frequency		S1, S0 = M, M (spread off)	16	48	128	MHz
Input Clock Duty Cycle		Time above VDD/2	40		60	%
Output Clock Duty Cycle		Time above 1.5 V	45	50	55	%
Cycle-to-cycle Jitter[1]		Fin=16 MHz, Fout=32 MHz		250	380	ps
Cycle-to-cycle Jitter[1]		Fin=32 MHz, Fout=128 MHz		250	380	ps
Output Rise Time	t_R	FSEL=M, 0.4 to 2.4 V	0.8		2.2	ns
	t_R	FSEL=1,0; 0.4 to 2.4 V	1.0		2.2	ns
Output Fall Time	t_F	FSEL=M, 0.4 to 2.4 V	0.8		2.2	ns
	t_F	FSEL=1,0; 0.4 to 2.4 V	1.0		2.2	ns
EMI Peak Frequency Reduction				8 to 16		dB

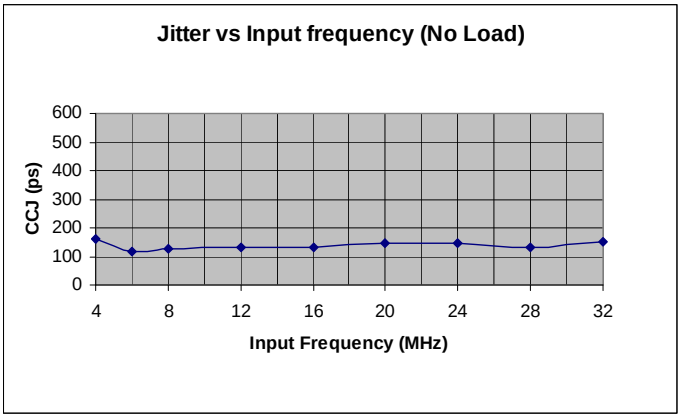
Note 1: Spread is enabled.

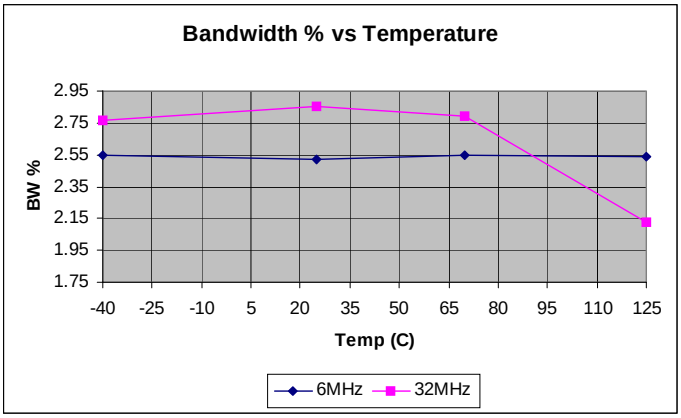
Thermal Characteristics for 8-pin SOIC

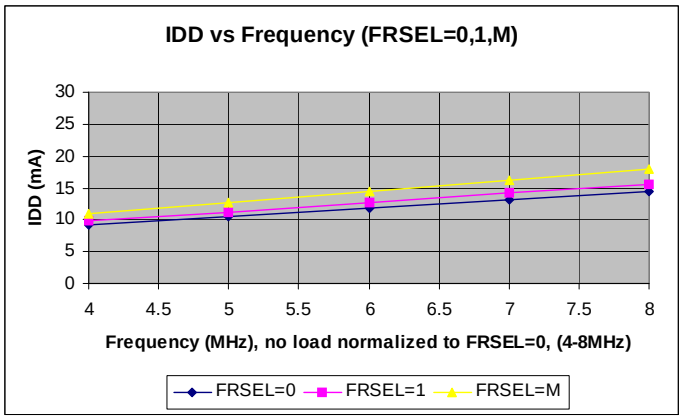
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		150		°C/W
	θ_{JA}	1 m/s air flow		140		°C/W
	θ_{JA}	3 m/s air flow		120		°C/W
Thermal Resistance Junction to Case	θ_{JC}			40		°C/W

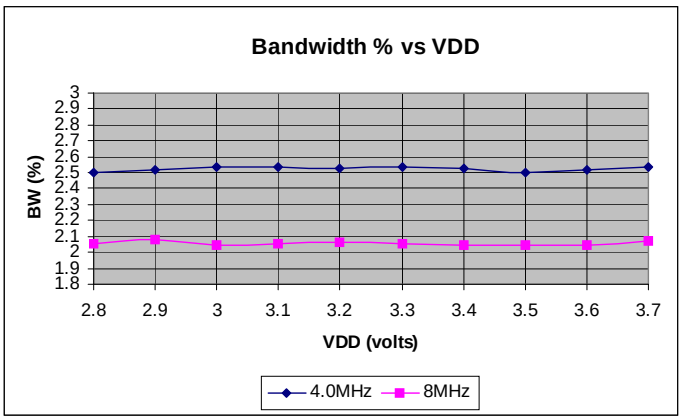
Characteristic Curves

The following curves determine the characteristic behavior of the MK5814C when tested over a number of environmental and application-specific parameters. These are typical performance curves and are not meant to replace any parameter specified in DC and AC Characteristics tables.

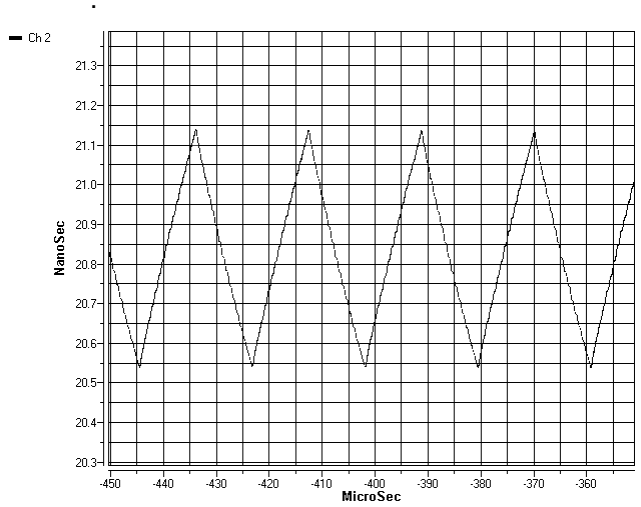




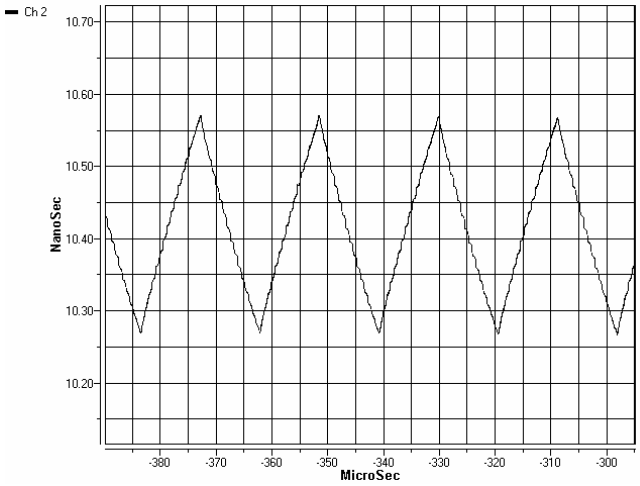




SSCG Profiles

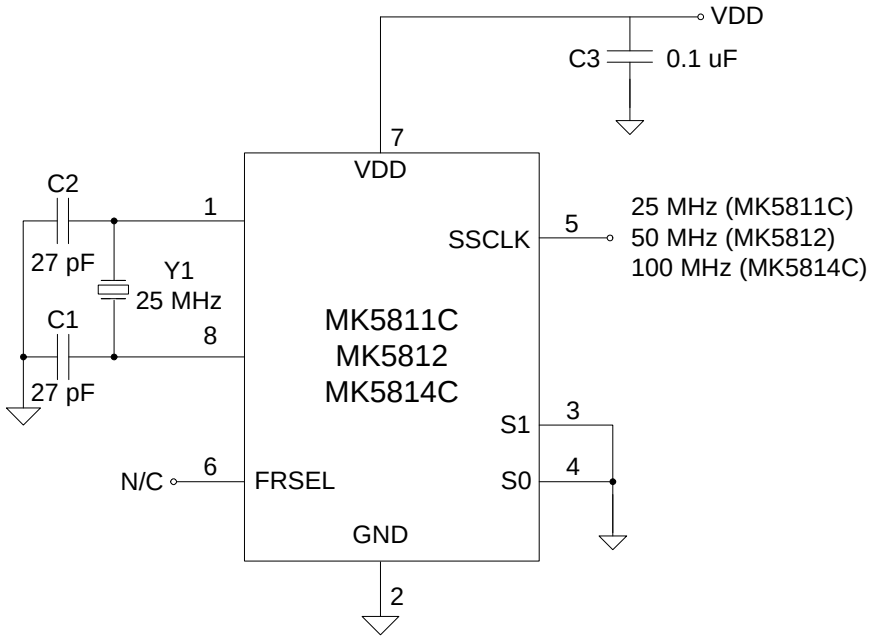


Min: 47.29 MHz
Max: 48.80 MHz
Rate: 46.92 kHz
Pk-Pk Jitter: 220 ps
Xin = 12.0 MHz
SSCLK1 = 48.0 MHz
S1, S0 = 0
FRSEL = 1
P/N = MK5814C



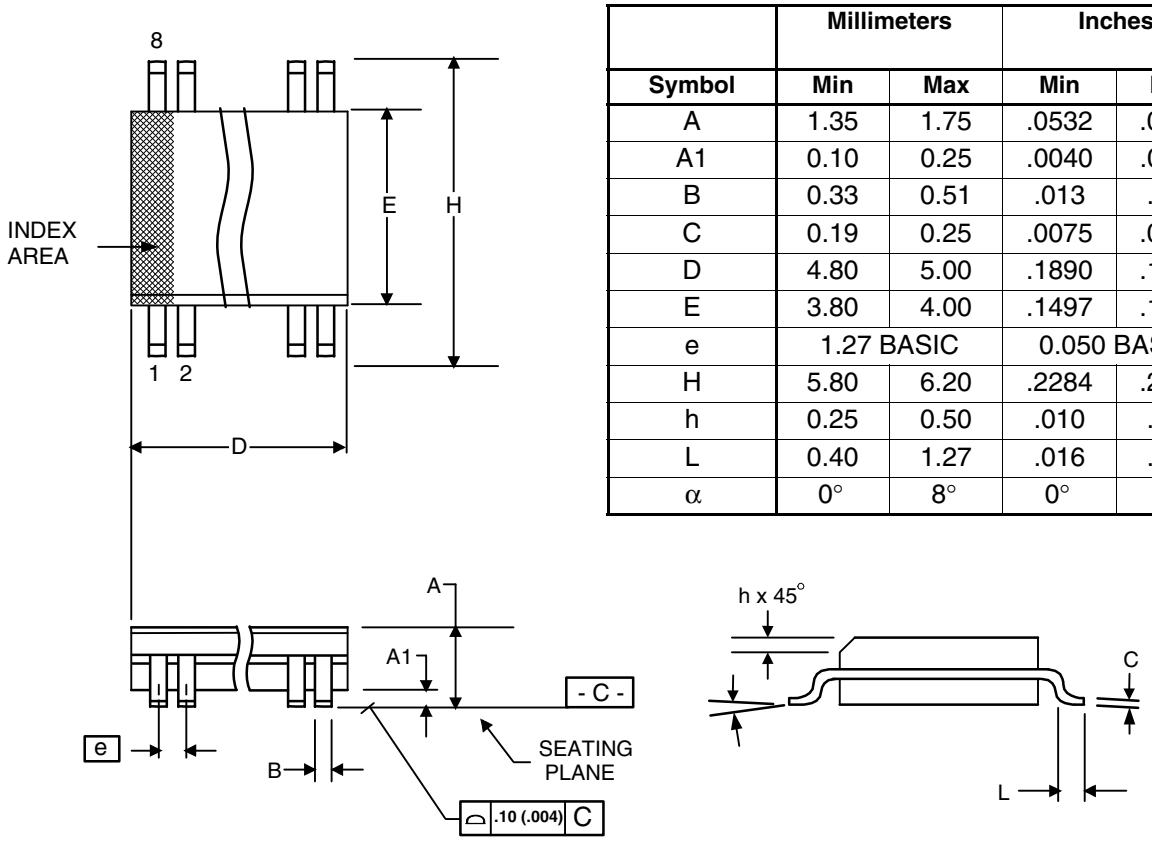
Min: 94.73 MHz
Max: 97.32 MHz
Rate: 46.87 kHz
Pk-Pk Jitter: 190 ps
Xin = 24.0 MHz
SSCLK1 = 96.0 MHz
S1, S0 = 0
FRSEL = M
P/N = MK5814C

Application Schematic



Package Outline and Package Dimensions (8-pin SOIC, 150 Mil. Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches	
Symbol	Min	Max	Min	Max
A	1.35	1.75	.0532	.0688
A1	0.10	0.25	.0040	.0098
B	0.33	0.51	.013	.020
C	0.19	0.25	.0075	.0098
D	4.80	5.00	.1890	.1968
E	3.80	4.00	.1497	.1574
e	1.27 BASIC		0.050 BASIC	
H	5.80	6.20	.2284	.2440
h	0.25	0.50	.010	.020
L	0.40	1.27	.016	.050
α	0°	8°	0°	8°

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
MK5814CMLF	5814CL	Tubes	8-pin SOIC	0 to +85° C
MK5814CMLFT	5814CL	Tape and Reel	8-pin SOIC	0 to +85° C

Parts that are ordered with a "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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Revision History

Rev.	Date	Originator	Description of Change
C	07/06/12	RDW	1. Max input frequency when using spread reduced from 32MHz to 25MHz. 2. Max output when using spread correspondingly reduced to 100MHz.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

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