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DATASHEET

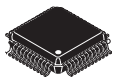
The MPC9893 is a 2.5 V and 3.3 V compatible, PLL based intelligent dynamic clock switch and generator specifically designed for redundant clock distribution systems. The device receives two LVCMOS clock signals and generates 12 phase aligned output clocks. The MPC9893 is able to detect a failing reference clock signal and to dynamically switch to a redundant clock signal. The switch from the failing clock to the redundant clock occurs without interruption of the output clock signal (output clock slews to alignment). The phase bump typically caused by a clock failure is eliminated.

The device offers 12 low skew clock outputs organized into two output banks, each configurable to support the different clock frequencies.

The extended temperature range of the MPC9893 supports telecommunication and networking requirements. The device employs a fully differential PLL design to minimize jitter.

MPC9893

LOW VOLTAGE
2.5 V AND 3.3 V IDCS AND
PLL CLOCK GENERATOR



AE SUFFIX
48-LEAD LQFP PACKAGE
Pb-FREE PACKAGE
CASE 932-03

Features

- 12-output LVCMOS PLL clock generator
- 2.5 V and 3.3 V compatible
- IDCS - on-chip intelligent dynamic clock switch
- Automatically detects clock failure
- Smooth output phase transition during clock failover switch
- 7.5 – 200 MHz output frequency range
- LVCMOS compatible inputs and outputs
- External feedback enables zero-delay configurations
- Supports networking, telecommunications and computer applications
- Output enable/disable and static test mode (PLL bypass)
- Low skew characteristics: maximum 50 ps output-to-output (within bank)
- 48-lead LQFP package, Pb-free
- Ambient operating temperature range of -40 to 85°C
- For functional replacement use 87973

Functional Description

The MPC9893 is a 3.3 V or 2.5 V compatible PLL clock driver and clock generator. The clock generator uses a fully integrated PLL to generate clock signals from redundant clock sources. The PLL multiplies the input reference clock signal by one, two, three, four or eight. The frequency-multiplied clock drives six bank A outputs. Six bank B outputs can run at either the same frequency than bank A or at half of the bank A frequency. Therefore, bank B outputs additionally support the frequency multiplication of the input reference clock by 3÷2 and 1÷2. Bank A and bank B outputs are phase-aligned[(1)]. Due to the external PLL feedback, the clock signals of both output banks are also phase-aligned[(1)] to the selected input reference clock, providing virtually zero-delay capability. The integrated IDCS continuously monitors both clock inputs and indicates a clock failure individually for each clock input. When a false clock signal is detected, the MPC9893 switches to the redundant clock input, forcing the PLL to slowly slew to alignment and not produce any phase bumps at the outputs. Both clock inputs are interchangeable, also supporting the switch to a failed clock that was restored. The MPC9893 also provides a manual mode that allows for user-controlled clock switches.

The PLL bypass of the MPC9893 disables the IDCS and PLL-related specifications do not apply. In PLL bypass mode, the MPC9893 is fully static in order to distribute low-frequency clocks for system test and diagnosis. Outputs of the MPC9893 can be disabled (high-impedance tristate) to isolate the device from the system. Applying output disable also resets the MPC9893. On power-up this reset function needs to be applied for correct operation of the circuitry. Please see the application section for power-on sequence recommendations.

1. At coincident rising edges.

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The device is packaged in a 7x7 mm^2 48-lead LQFP package.

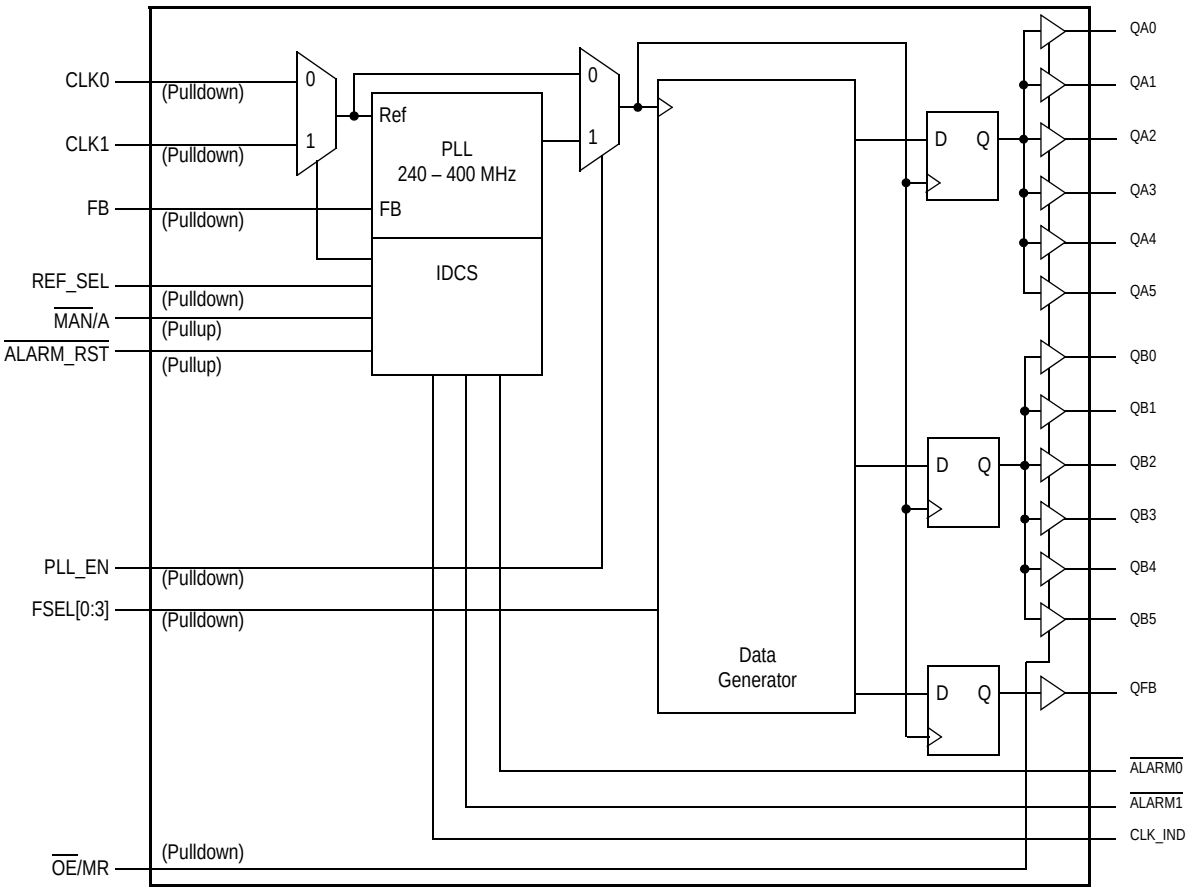
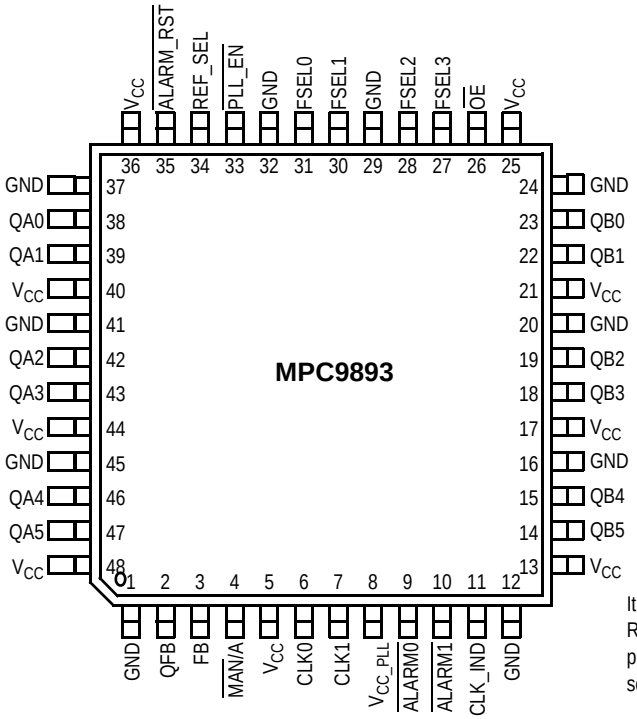


Figure 1. MPC9893 Logic Diagram



It is recommended to use an external RC filter for the analog power supply pin V_{CC_PLL}. Please see application section for details.

Figure 2. MPC9893 48-Lead Pinout (Top View)

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Table 1. Pin Configurations

Number	Name	Type	Description
CLK0, CLK1	Input	LVCMOS	PLL reference clock inputs
FB	Input	LVCMOS	PLL feedback signal input, connect directly to QFB output
REF_SEL	Input	LVCMOS	Selects the primary reference clock
$\overline{\text{MAN}}$/A	Input	LVCMOS	Selects automatic switch mode or manual reference clock selection
$\overline{\text{ALARM_RST}}$	Input	LVCMOS	Reset of alarm flags and selected reference clock
$\overline{\text{PLL_EN}}$	Input	LVCMOS	Select PLL or static test mode
FSEL[0:3]	Input	LVCMOS	Clock frequency selection and configuration of clock divider modes
$\overline{\text{OE}}$/MR	Input	LVCMOS	Output enable/disable and device reset
QA[0:5]	Output	LVCMOS	Bank A clock outputs
QB[0:5]	Output	LVCMOS	Bank B clock outputs
QFB	Output	LVCMOS	Clock feedback output. QFB must be connected to FB for correct operation
$\overline{\text{ALARM0}}$	Output	LVCMOS	Indicates clock failure on CLK0
$\overline{\text{ALARM1}}$	Output	LVCMOS	Indicates clock failure on CLK1
CLK_IND	Output	LVCMOS	Indicates currently selected input reference clock
GND	Supply	Ground	Negative power supply
V_{CC_PLL}	Supply	V_{CC}	Positive power supply for the PLL (analog power supply). It is recommended to use an external RC filter for the analog power supply pin V_{CC_PLL}. Please see the application section for details.
V_{CC}	Supply	V_{CC}	Positive power supply for I/O and core

Table 2. Function Table

Control	Default	0	1
Inputs			
PLL_EN	0	PLL enabled. The input to output frequency relationship is that according to Table 3 if the PLL is frequency locked.	PLL bypassed and IDCS disabled. The VCO output is replaced by the reference clock signal fref. The MPC9893 is in manual mode.
$\overline{\text{MAN}}$/A	1	Manual clock switch mode. **IDCS disabled**. Clock failure detection and output flags ALARM0, ALARM1, CLK_IND are enabled.	Automatic clock switch mode. **IDCS enabled**. Clock failure detection and output flags ALARM0, ALARM1, CLK_IND are enabled. IDCS overrides REF_SEL on a clock failure. IDCS operation requires $\overline{\text{PLL_EN}}$ = 0.
$\overline{\text{ALARM_RST}}$	1	$\overline{\text{ALARM0}}$, $\overline{\text{ALARM1}}$ and CLK_IND flags are reset: $\overline{\text{ALARM0}}$=H, $\overline{\text{ALARM1}}$=H and CLK_IND=REF_SEL. $\overline{\text{ALARM_RST}}$ is a one-shot function.	$\overline{\text{ALARM0}}$, $\overline{\text{ALARM1}}$ and CLK_IND active
REF_SEL	0	Selects CLK0 as the primary clock source	Selects CLK1 as the secondary clock source
FSEL[0:3]	0000	See Table 3	
$\overline{\text{OE}}$/MR	0	Outputs enabled (active)	Outputs disabled (high impedance tristate), reset of data generators and output dividers. The MPC9893 requires reset at power-up and after any loss of PLL lock. Loss of PLL lock may occur when the external feedback path is interrupted. The length of the reset pulse should be greater than two reference clock cycles (CLK0,1). $\overline{\text{OE}}$/MR does not tristate the QFB output.
Outputs ($\overline{\text{ALARM0}}$, $\overline{\text{ALARM1}}$, CLK_IND are valid if PLL is locked)			
$\overline{\text{ALARM0}}$		CLK0 failure	
$\overline{\text{ALARM1}}$		CLK1 failure	
CLK_IND		CLK0 is the reference clock	CLK1 is the reference clock

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Table 3. Clock Frequency Configuration

Name	FSEL0	FSEL1	FSEL2	FSEL3	f_{REF} range [MHz]	QAx		QBx		QFB	FB[1]
						Ratio	f_{QAX} [MHz]	Ratio	f_{QBX}[MHz]		
M8	0	0	0	0	15–25	f_{REF} * 8	120–200	f_{REF} * 8	120–200	f_{REF}	16
M82	0	0	0	1				f_{REF} * 4	60–100		
M4	0	0	1	0	30–50	f_{REF} * 4	120–200	f_{REF} * 4	120–200	f_{REF}	8
M42	0	0	1	1				f_{REF} * 2	60–100		
M3	0	1	0	0	40–66.6	f_{REF} * 3	120–200	f_{REF} * 3	120–200	f_{REF}	6
M32	0	1	0	1				f_{REF} * 3 ÷ 2	60–100		
M2M	0	1	1	0	30–50	f_{REF} * 2	60–100	f_{REF} * 2	60–100	f_{REF}	8
M22M	0	1	1	1				f_{REF}	30–50		
M2H	1	0	0	0	60–100	f_{REF} * 2	120–200	f_{REF} * 2	120–200	f_{REF}	4
M22H	1	0	0	1				f_{REF}	60–100		
M1L	1	0	1	0	15–25	f_{REF}	15–25	f_{REF}	15–25	f_{REF}	16
M12L	1	0	1	1				f_{REF} ÷ 2	7.5–12.5		
M1M	1	1	0	0	30–50	f_{REF}	30–50	f_{REF}	30–50	f_{REF}	8
M12M	1	1	0	1				f_{REF} ÷ 2	15–25		
M1H	1	1	1	0	60–100	f_{REF}	60–100.0	f_{REF}	60–100	f_{REF}	4
M12H	1	1	1	1				f_{REF} ÷ 2	30–50		

1. FB: Internal PLL feedback divider

Table 4. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		V_{CC} ÷ 2		V	
MM	ESD Protection (Machine Model)	200			V	
HBM	ESD Protection (Human Body Model)	2000			V	
CDM	ESD Protection (Charged Device Model)	1500			V	
LU	Latch-Up Immunity	200			mA	
C_{PD}	Power Dissipation Capacitance		10		pF	Per output
C_{IN}	Input Capacitance		4.0		pF	Inputs

Table 5. Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	–0.3	3.6	V	
V_{IN}	DC Input Voltage	–0.3	V_{CC}+0.3	V	
V_{OUT}	DC Output Voltage	–0.3	V_{CC}+0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	–65	125	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

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Table 6. DC Characteristics (V_{CC} = 3.3 V ± 5%, T_A = –40° to 85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage	2.0		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage			0.8	V	LVCMOS
V_{OH}	Output High Voltage	2.4			V	I_{OH} = –24 mA(1)
V_{OL}	Output Low Voltage			0.55 0.30	V V	I_{OL} = 24 mA I_{OL} = 12 mA
Z_{OUT}	Output Impedance		14–17		Ω	
I_{IN}	Input Current			±200	μA	V_{IN} = V_{CC} or GND
I_{CC_PLL}	Maximum PLL Supply Current		2.0	5.0	mA	V_{CC_PLL} Pin
I_{CC}	Maximum Quiescent Supply Current			4.0	mA	All V_{CC} Pins
V_{TT}	Output Termination Voltage		V_{CC}÷2		V	

1. The MPC9893 is capable of driving 50 Ω transmission lines on the incident edge. Each output drives one 50 Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50 Ω series terminated transmission lines.

Table 7. DC Characteristics (V_{CC} = 2.5 V ± 5%, T_A = –40° to 85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage	1.7		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage			0.7	V	LVCMOS
V_{OH}	Output High Voltage	1.8			V	I_{OH} = –15 mA(1)
V_{OL}	Output Low Voltage			0.6	V	I_{OL} = 15 mA
Z_{OUT}	Output Impedance		17–20		Ω	
I_{IN}	Input Current			±200	μA	V_{IN} = V_{CC} or GND
I_{CC_PLL}	Maximum PLL Supply Current		2.0	5.0	mA	V_{CC_PLL} Pin
I_{CC}	Maximum Quiescent Supply Current			4.0	mA	All V_{CC} Pins
V_{TT}	Output Termination Voltage		V_{CC}÷2		V	

1. The MPC9893 is capable of driving 50 Ω transmission lines on the incident edge. Each output drives one 50 Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50 Ω series terminated transmission lines per output.

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Table 8. AC Characteristics (V_{CC} = 3.3 V ± 5% or V_{CC} = 2.5 V ± 5%, T_A = –40° to 85°C)[1]

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
f_{ref}	Input Frequency					PLL locked
	FSEL=000x	15.0		25.0	MHz	
	FSEL=001x	30.0		50.0	MHz	
	FSEL=010x	40.0		66.6	MHz	
	FSEL=011x	30.0		50.0	MHz	
	FSEL=100x	60.0		100.0	MHz	
	FSEL=101x	15.0		12.5	MHz	
	FSEL=110x	30.0		50.0	MHz	
	FSEL=111x	60.0		100.0	MHz	
f_{MAX}	Maximum Output Frequency					PLL locked
	FSEL=000x	60.0		200.0	MHz	
	FSEL=001x	60.0		200.0	MHz	
	FSEL=010x	60.0		200.0	MHz	
	FSEL=011x	30.0		100.0	MHz	
	FSEL=100x	60.0		200.0	MHz	
	FSEL=101x	7.5		25.0	MHz	
	FSEL=110x	15.0		50.0	MHz	
	FSEL=111x	30.0		100.0	MHz	
f_{refDC}	Reference Input Duty Cycle	40		60	%	
t_r, t_f	CLK0, 1 Input Rise/Fall Time			1.0	ns	0.8 to 2.0 V
$t_{(\varnothing)}$	Propagation Delay (static phase offset, CLKx to FB)					PLL locked
	V_{CC}=3.3 V±5% and FSEL[0:2]=111	–60		+50	ps	
	V_{CC}=3.3 V±5%	–200		+100	ps	
	V_{CC}=2.5 V±5% and FSEL[0:2]=111	–125		+25	ps	
	V_{CC}=2.5 V±5%	–400		+100	ps	
Δ t	Rate of Period Change (phase slew rate)					Failover switch
	QAx outputs			150	ps/cycle	
	QBx outputs (FSEL=xxx0)			150		
	QBx outputs (FSEL=xxx1)			300		
$t_{sk(O)}$	Output-to-Output Skew[2] (within bank)			150	ps	
	(bank-to-bank)			100	ps	
	(any output to QFB)			125	ps	
DC_O	Output Duty Cycle	45	50	55	%	
t_r, t_f	Output Rise/Fall Time	0.1		1.0	ns	0.55 to 2.4 V
$t_{PLZ, HZ}$	Output Disable Time			10	ns	
$t_{PZL, LZ}$	Output Enable Time			10	ns	
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter[3] FSEL3=0			225	ps	See applications section
	FSEL3=1			425	ps	
$t_{JIT(PER)}$	Period Jitter[3] FSEL3=0			150	ps	See applications section
	FSEL3=1			250	ps	
$t_{JIT(\varnothing)}$	I/O Phase Jitter[4]					See applications section
	FB=4: FSEL[0:2]=100 or 111 RMS (1 σ)			40	ps	
	FB=6: FSEL[0:2]=010 RMS (1 σ)			50	ps	
	FB=8: FSEL[0:2]=001, 011, or 110 RMS (1 σ)			55	ps	
	FB=16: FSEL[0:2]=000 or 101 RMS (1 σ)			70	ps	
BW	PLL Closed Loop Bandwidth[5] FSEL=111x		0.8-4.0		MHz	
t_{LOCK}	Maximum PLL Lock Time			10	ms	

1. AC characteristics apply for parallel output termination of 50 Ω to V_{TT}.
2. See application section for part-to-part skew calculation.
3. Cycle-to-cycle and period jitter depend on the VCO frequency and output configuration. See the application section.
4. I/O jitter depends on the VCO frequency and internal PLL feedback divider FB. See APPLICATIONS INFORMATION for more information and for the calculation for other confidence factors than 1σ.
5. –3dB point of PLL transfer characteristics.

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APPLICATIONS INFORMATION

Definitions

IDCS: Intelligent Dynamic Clock Switch. The IDCS monitors both primary and secondary clock signals. Upon a failure of the primary clock signal, the IDCS switches to a valid secondary clock signal and status flags are set.

Reference clock signal fref: The clock signal that is selected by the IDCS or REF_SEL as the input reference to the PLL.

Manual mode: The reference clock frequency is selected by REF_SEL.

Automatic mode: The reference clock frequency is determined by the internal IDCS logic.

Primary clock: The input clock signal selected by REF_SEL. The primary clock may or may not be the reference clock, depending on switch mode and IDCS status.

Secondary clock: The input clock signal not selected by REF_SEL

Selected clock: The CLK_IND flag indicates the reference clock signal: CLK_IND = 0 indicates CLK0 is the clock reference signal, CLK_IND =1 indicates CLK1 is the reference clock signal.

Clock failure: A valid clock signal that is stuck (high or low) for at least one input clock period. The primary clock and the secondary clock is monitored for failure. Valid clock signals must be within the AC and DC specification for the input reference clock. A loss of clock is detected if as well as the loss of both clocks. In the case of both clocks lost, the MPC9893 will set the alarm flags and the PLL will stall. The MPC9893 does not monitor and detect changes in the input frequency.

Automatic Mode and IDCS Commanded Clock Switch

$\overline{\text{MAN}}$/A = 1, IDCS enabled: Both primary and secondary clocks are monitored. The first clock failure is reported by its $\overline{\text{ALARM}}$x status flag (clock failure is indicated by a logic low). The $\overline{\text{ALARM}}$x status is flag latched and remains latched until reset by assertion of $\overline{\text{ALARM_RST}}$.

If the clock failure occurs on the primary clock, the IDCS attempts to switch to the secondary clock. The secondary clock signal needs to be valid for a successful switch. Upon a successful switch, CLK_IND indicates the reference clock, which may now be different as that originally selected by REF_SEL.

Manual Mode

$\overline{\text{MAN}}$/A = 0, IDCS disabled: PLL functions normally and both clocks are monitored. The reference clock signal will always be the clock signal selected by REF_SEL and will be indicated by CLK_IND.

Clock Output Transition

A clock switch, either in automatic or manual mode, follows the next negative edge of the newly selected reference clock signal. The feedback and newly selected reference clock edge will start to slew to alignment at the next positive edge of both signals. Output runt pulses are eliminated.

Reset

$\overline{\text{ALARM_RST}}$ is asserted by a negative edge. It generates a one-shot reset pulse that clears both $\overline{\text{ALARM}}$x latches and the CLK_IND latch. If both CLK0 and CLK1 are invalid or fail when $\overline{\text{ALARM_RST}}$ is asserted, both $\overline{\text{ALARM}}$x flags will be latched after one FB signal period and CLK_IND will be latched (L) indicating CLK0 is the reference signal. While neither $\overline{\text{ALARM}}$x flag is latched ($\overline{\text{ALARM}}$x = H), the CLK_IND can be freely changed with REF_SEL.

$\overline{\text{OE}}$/MR: Reset the data generator and output disable. Does not reset the IDCS flags.

Acquiring Frequency Lock at Startup

1. On startup, $\overline{\text{OE}}$/MR must be asserted to reset the output dividers. The IDCS should be disabled ($\overline{\text{MAN}}$/A=0) during startup to select the manual mode and the primary clock.
2. The PLL will attempt to gain lock if the primary clock is present on startup. PLL lock requires the specified lock time.
3. Applying a high to low transition to $\overline{\text{ALARM_RST}}$ will clear the alarm flags.
4. Enable the IDCS ($\overline{\text{MAN}}$/A=1) to enable to IDCS.

Power Supply Filtering

The MPC9893 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the $V_{CC_PLL\ (PLL)}$ power supply impacts the device characteristics, for instance I/O jitter. The MPC9893 provides separate power supplies for the output buffers (V_{CC}) and the phase-locked loop (V_{CC_PLL}) of the device. The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the V_{CC_PLL} pin for the MPC9893. Figure 3 illustrates a typical power supply filter scheme. The MPC9893 frequency and phase stability is most susceptible to noise with spectral content in the 100kHz to 20MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor R_F. From the data sheet the I_{CC_PLL} current (the current sourced through the V_{CC_PLL} pin) is typically 2 mA (5 mA maximum), assuming that a minimum of 2.325 V (V_{CC} = 3.3 V or V_{CC} = 2.5 V) must be maintained on the V_{CC_PLL} pin. The resistor R_F shown in Figure 3 must have a resistance of 9-10 Ω to meet the voltage drop criteria.

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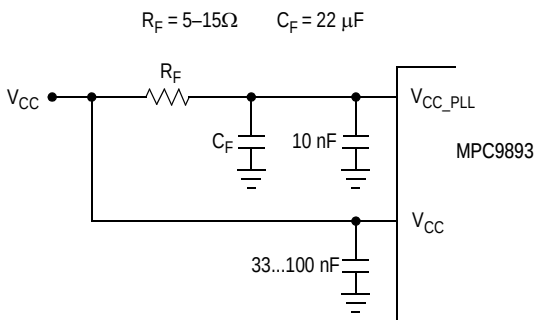

Figure 3. V_{CC_PLL} Power Supply Filter

The minimum values for R_F and the filter capacitor C_F are defined by the required filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example RC filter shown in Figure 3, the filter cut-off frequency is around 3-5 kHz and the noise attenuation at 100 kHz is better than 42 dB.

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC9893 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Using the MPC9893 in Zero-Delay Applications

Nested clock trees are typical applications for the MPC9893. Designs using the MPC9893 as LVCMOS PLL fanout buffer with zero insertion delay will show significantly lower clock skew than clock distributions developed from CMOS fanout buffers. The external feedback option of the MPC9893 clock driver allows for its use as a zero delay buffer. The the propagation delay through the device is virtually eliminated. The PLL aligns the feedback clock output edge with the clock input reference edge resulting a near zero delay through the device. The maximum insertion delay of the device in zero-delay applications is measured between the reference clock input and any output. This effective delay consists of the static phase offset, I/O jitter (phase or long-term jitter), feedback path delay and the output-to-output skew error relative to the feedback output.

Calculation of Part-to-Part Skew

The MPC9893 zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs of two or more MPC9893 are connected together, the maximum overall timing uncertainty from the common CLK0 or CLK1 input to any output is:

$$t_{SK(PP)} = t_{(\varnothing)} + t_{SK(O)} + t_{PD,\ LINE(FB)} + t_{JIT(\varnothing)} \cdot CF$$

This maximum timing uncertainty consist of four components: static phase offset, output skew, feedback board trace delay and I/O (phase) jitter:

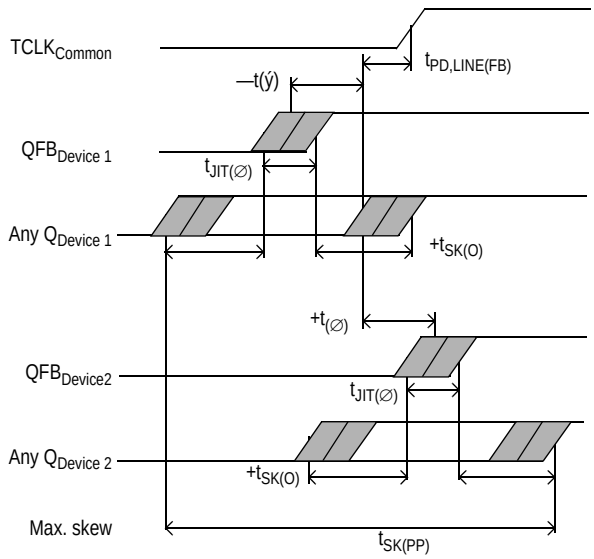

Figure 4. MPC9893 Max. Device-to-Device Skew

Due to the statistical nature of I/O jitter a RMS value (1 σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 9.

Table 9. Confidence Factor CF

CF	Probability of clock edge within the distribution
± 1σ	0.68268948
± 2σ	0.95449988
± 3σ	0.99730007
± 4σ	0.99993663
± 5σ	0.99999943
± 6σ	0.99999999

The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device. In the following example calculation a I/O jitter confidence factor of 99.7% (± 3σ) is assumed, resulting in a worst case timing uncertainty from the common clock input to any MPC9893 output of –275 ps to +265 ps relative to the reference clock input CLK0/1:

$$t_{SK(PP)} = [-60ps...50ps] + [-125ps...125ps] + [(30ps \cdot -3)...(30ps \cdot 3)] + t_{PD,\ LINE(FB)}$$

$$t_{SK(PP)} = [-275ps...265ps] + t_{PD,\ LINE(FB)}$$

Example configuration: f_{ref} = 100 MHz, V_{CC} = 3.3 V
f_{VCO} = 400 MHz, FSEL[0:2]=111

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The I/O (Phase) jitter of the MPC9893 depends on the internal VCO frequency and the PLL feedback divider configuration. A high internal VCO frequency and a low PLL feedback divider result in lower I/O jitter than the jitter limits in the AC characteristics (Table 8). When calculating the part-to-part skew, Table 10 should be used to determine the actual VCO frequency, then use Figure 5 to determine the maximum I/O jitter for the specific VCO frequency and divider configuration. In above example calculation, the internal VCO frequency of 400 MHz corresponds to a maximum I/O jitter of 30 ps (RMS).

Table 10. Internal VCO Frequency f_{VCO}

MPC9893 Configuration	f_{VCO}	PLL Feedback Divider FB
M1H, M12H, M2H, M22H	$4 * f_{ref}$	4
M3, M32	$6 * f_{ref}$	6
M1M, M12M, M2M, M22M, M4, M42	$8 * f_{ref}$	8
M1L, M12L, M8, M82	$16 * f_{ref}$	16

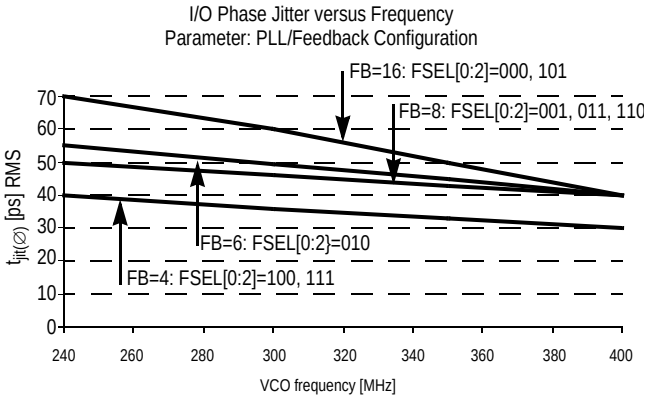

Figure 5. Max. I/O Phase Jitter versus VCO Frequency

The cycle-to-cycle jitter and period jitter of the MPC9893 depend on the output configuration and on the frequency of the internal VCO. Using the outputs of bank A and bank B at the same frequency (FSEL3=0) results in a lower jitter than the split output frequency configuration (FSEL3=1). The jitter also decreases with an increasing internal VCO frequency. Figure 5 to Figure 7 represent the maximum jitter of the MPC9893.

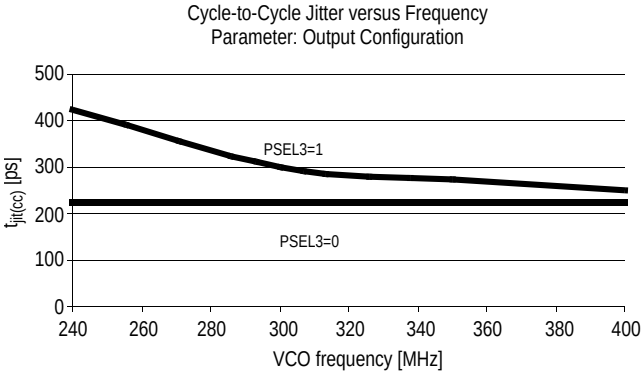

Figure 6. Max. Cycle-to-Cycle Jitter versus VCO Frequency

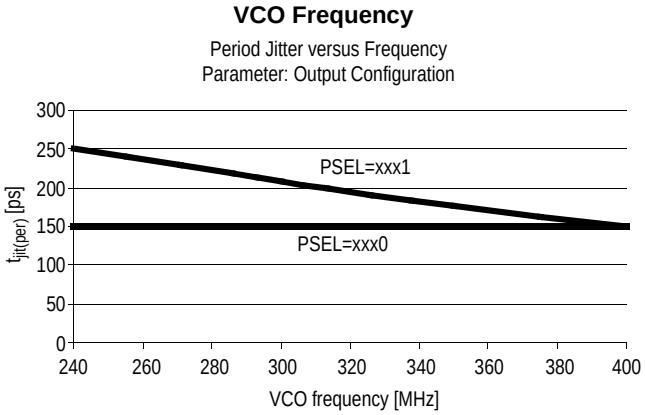

Figure 7. Max. Period Jitter versus VCO Frequency

Driving Transmission Lines

The MPC9893 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20 Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Freescale Semiconductor application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50 Ω resistance to V_{CC}÷2.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9893 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 8 illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9893 clock driver is effectively doubled due to its capability to drive multiple lines.

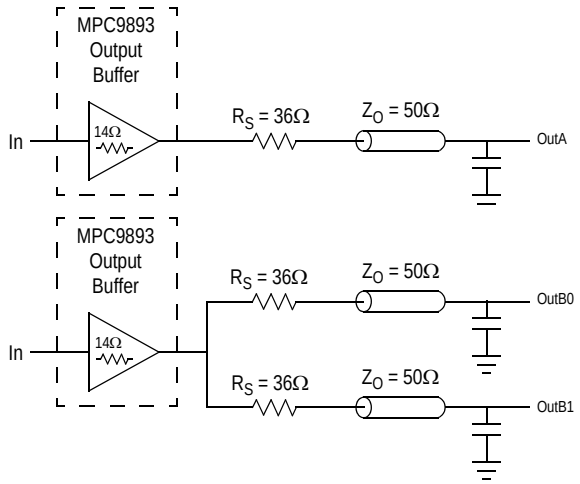

Figure 8. Single versus Dual Transmission Lines

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The waveform plots in Figure 9 show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9893 output buffer is more than sufficient to drive 50 Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43 ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9893. The output waveform in Figure 9 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S (Z_0 \div (R_S + R_0 + Z_0))$$
$$Z_0 = 50\ \Omega \parallel 50\ \Omega$$
$$R_S = 36\ \Omega \parallel 36\ \Omega$$
$$R_0 = 14\ \Omega$$
$$V_L = 3.0\ (25 \div (18+17+25)$$
$$= 1.31\ V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.6 V. It will then increment towards the quiescent 3.0 V in steps separated by one round trip delay (in this case 4.0 ns).

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 10 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

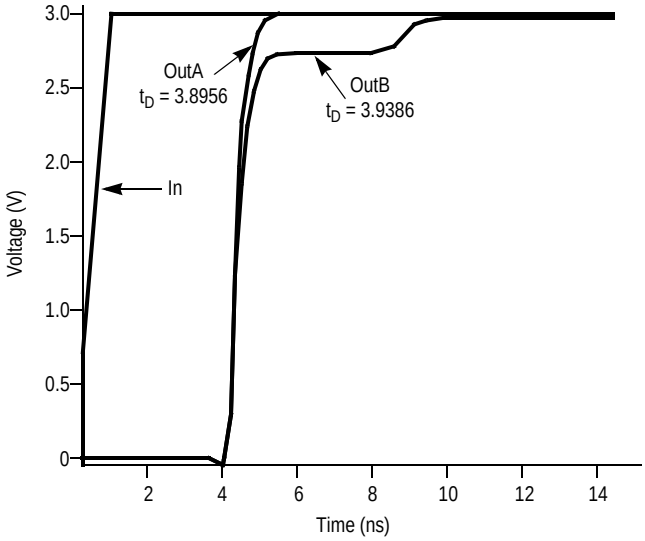
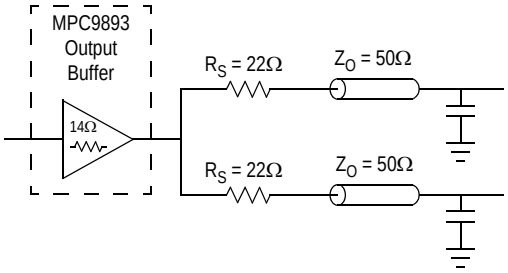


Figure 9. Single versus Dual Waveforms



14Ω + 22Ω || 22Ω = 50Ω || 50Ω
25Ω = 25Ω

Figure 10. Optimized Dual Line Termination

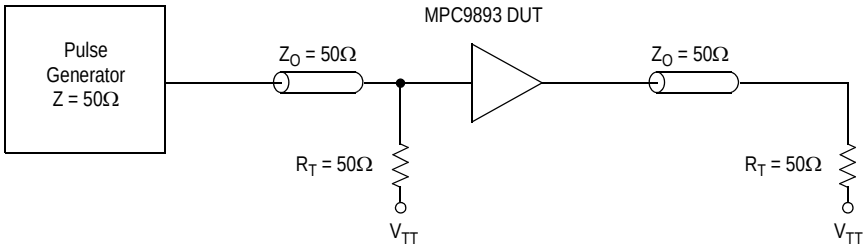


Figure 11. CLK0, CLK1 MPC9893 AC Test Reference for V_{CC} = 3.3 V and V_{CC} = 2.5 V

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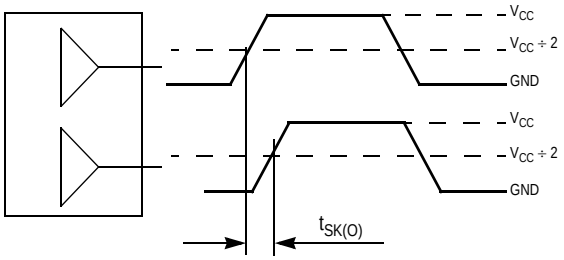


The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 12. Output-to-Output Skew $t_{SK(O)}$

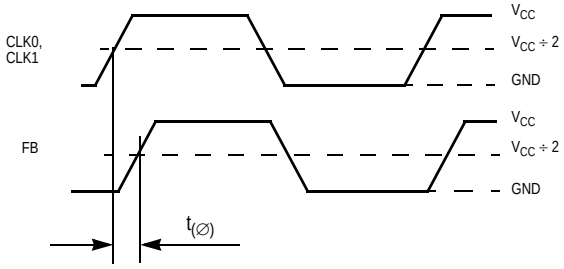
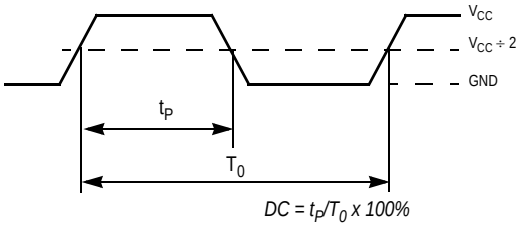
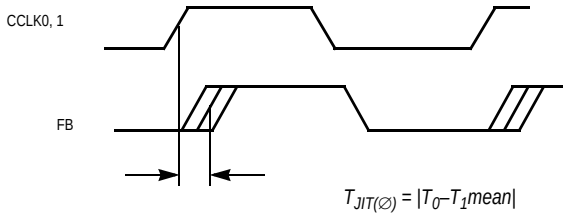


Figure 13. Propagation Delay ($t_{(\varnothing)}$, static phase offset) Test Reference



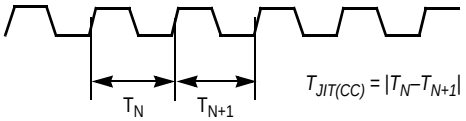
The time from the PLL controlled edge to the noncontrolled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 14. Output Duty Cycle (DC)



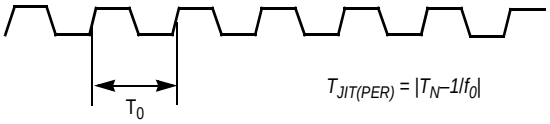
The deviation in t_0 for a controlled edge with respect to a t_0 mean in a random sample of cycles

Figure 15. I/O Jitter



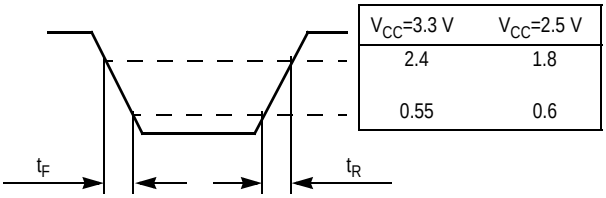
The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 16. Cycle-to-Cycle Jitter



The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

Figure 17. Period Jitter



V_{CC}=3.3 V	V_{CC}=2.5 V
2.4	1.8
0.55	0.6

Figure 18. Output Transition Time Test Reference

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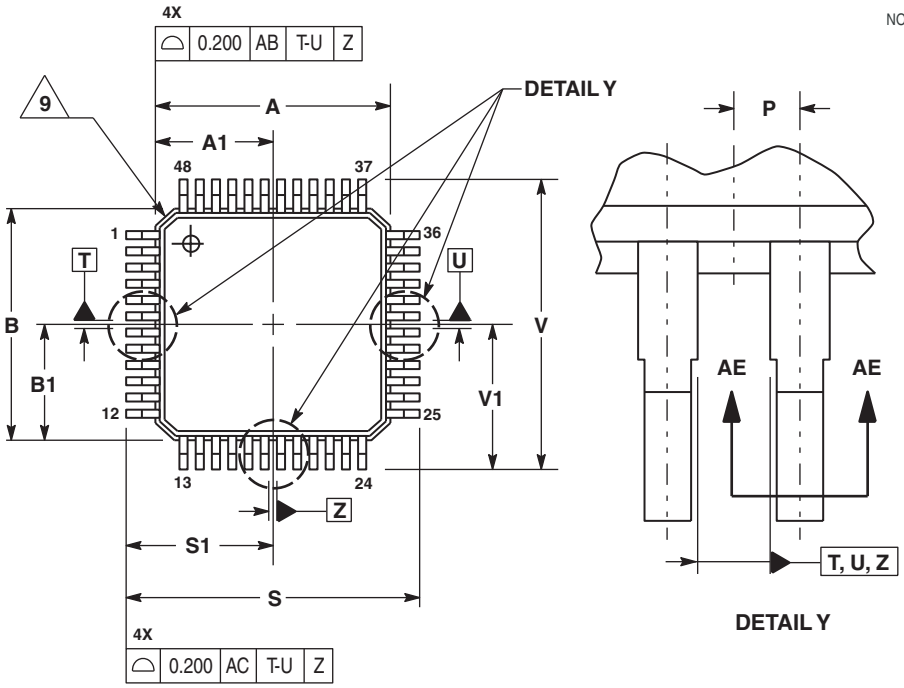
PACKAGE DIMENSIONS

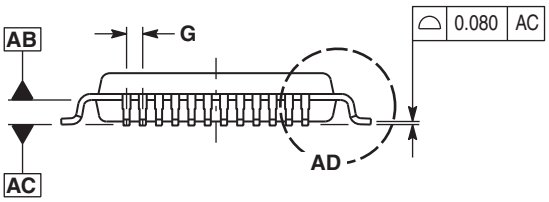


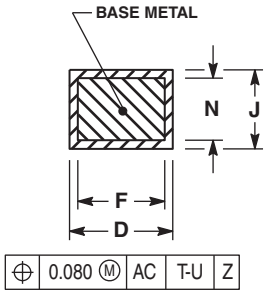
DETAIL Y

NOTES:

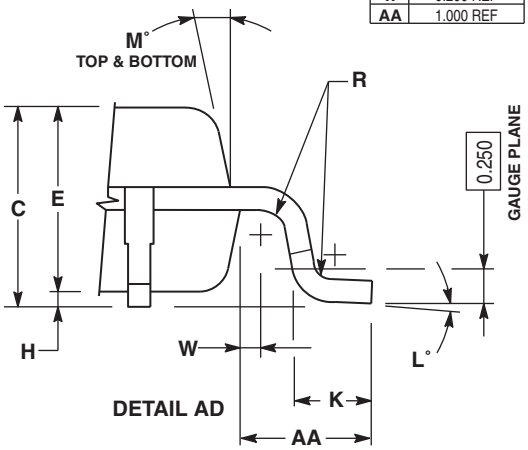
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5m, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLAN AB IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS T, U, AND Z TO BE DETERMINED AT DATAUM PLANE AB.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE AC.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE AB.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.350.
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076.
9. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

	MILLIMETERS	
DIM	MIN	MAX
A	7.000 BSC	
A1	3.500 BSC	
B	7.000 BSC	
B1	3.500 BSC	
C	1.400	1.600
D	0.170	0.270
E	1.350	1.450
F	0.170	0.230
G	0.500 BSC	
H	0.050	0.150
J	0.090	0.200
K	0.500	0.700
L	0°	7°
M	12° REF	
N	0.090	0.160
P	0.250 BSC	
R	0.150	0.250
S	9.000 BSC	
S1	4.500 BSC	
V	9.000 BSC	
V1	4.500 BSC	
W	0.200 REF	
AA	1.000 REF	





SECTION AE-AE



DETAIL AD

CASE 932-03
ISSUE F
48-LEAD LQFP PACKAGE

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Revision History Sheet

Rev	Table	Page	Description of Change	Date
8		1	NRND – Not Recommend for New Designs	1/9/13
8		1	Removed NRND	5/5/15
8		1	Product Discontinuation Notice - Last time buy expires September 7, 2016. PDN N-16-02	3/16/16

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